IBM z15 Highlights

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Agenda

- **z15 T02 (/T01)**
- **Compression**
- **HMC / SE**

IBM z15 T02 und T01

IBM z15 Model T02 Announcement – 14. April 2020
(General Availability 15. May 2020)

IBM Z – Naming for IBM z15™ Model T01 and T02

Brand Name:	**IBM**
Product Class:	**IBM mainframe**
Family Name:	**IBM Z®**
Family Short Name:	**Z**
Product Line Name:	**IBM Z®**
Product Line Short Name:	**Z**
Product Name:	**IBM z15™**
Short Name:	**z15™**
Model and Processor Capacity Features:	**T01, Features: Max34, Max71, Max108, Max145, Max190** **T02, Features: Max4, Max13, Max21, Max31, Max65**
Machine Type:	**T01 -> 8561** **T02 -> 8562**

IBM Z and LinuxONE

IBM Z

Can run all workload

- z/OS
- z/VM
- z/VSE
- z/TPF
- Linux on Z
- KVM on Z

LinuxONE

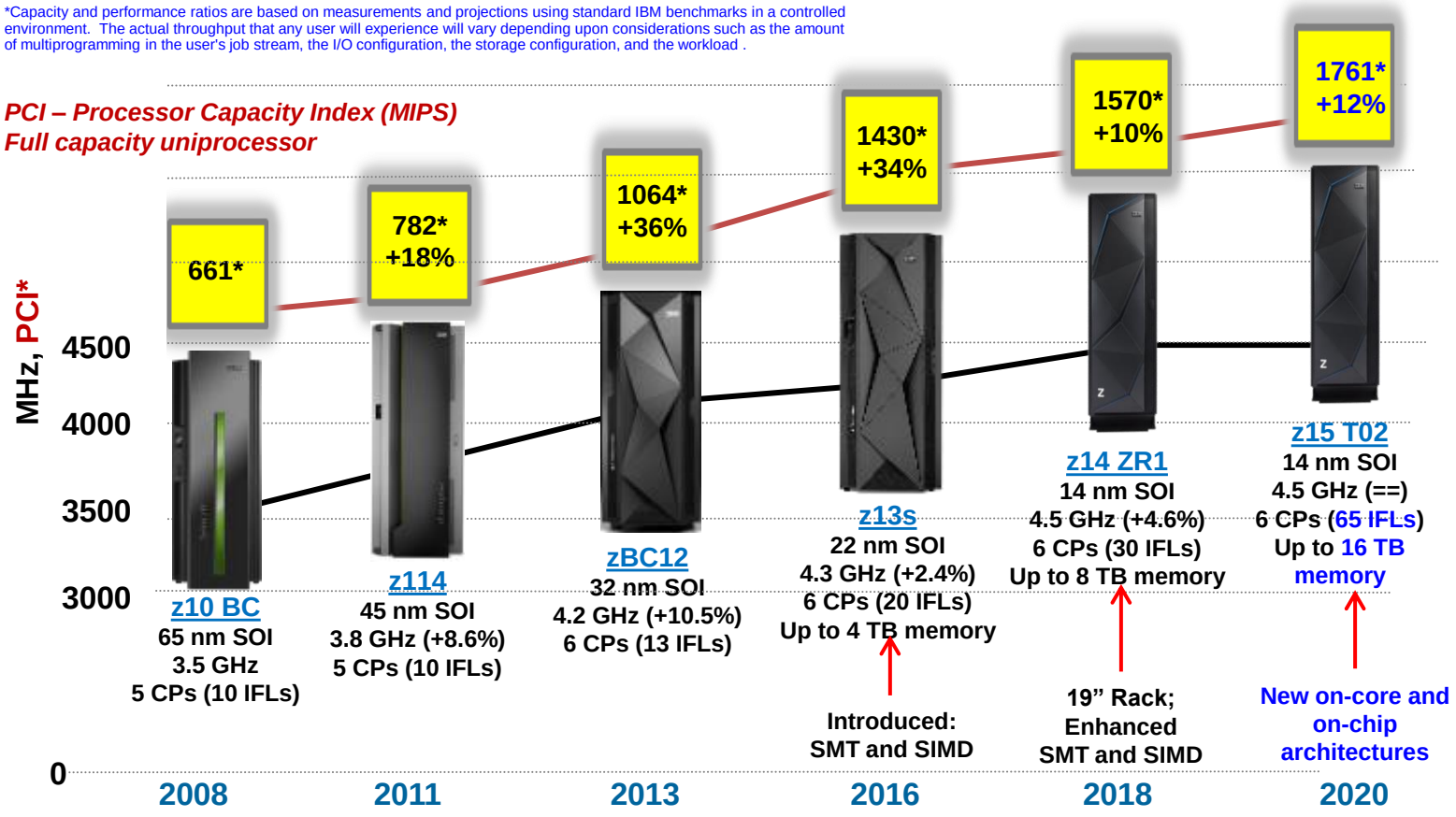
Specialized for Linux on Z workload

LinuxONE III LT1 / LT2

In Switzerland, Phoenix Systems AG has now a LinuxONE III

z15 T02 Continues the CMOS Mainframe Heritage

*Capacity and performance ratios are based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload .



*NOTE: PCI (MIPS) Tables are NOT adequate for making comparisons of IBM Z processors in proposals

8562-T02 Processing Units

Model	Feature	Drawers/ Cores	PU SCM/ CPs	IFLs/ uIFLs	zIIPs	ICFs	Std SAPs	Optional SAPs	Std. Spares	IFP
T02	Max4	1/8	1 0-4	0-4 0-3	0-2	0-4	2	0-2	1	1
	Max13	1/17	2 0-6	0-13 0-12	0-7	0-13	2	0-2	1	1
	Max21	1/27	3 0-6	0-21 0-20	0-12	0-21	3	0-2	2	1
	Max31	1/38	4 0-6	0-31 0-30	0-12	0-31	4	0-8	2	1
	Max65	2/76	8 0-6	0-65 0-64	0-12	0-65	8	0-8	2	1

1. At least one CP, IFL, or ICF must be purchased in every machine.
2. Two zIIPs may be purchased for each CP purchased if cores are available. (2:1). This remains true for sub-capacity CPs and for “banked” CPs.
3. “uIFL” = Unassigned IFL
4. The IFP is conceptually an additional, special purpose SAP – used by PCIe I/O features (e.g. RoCE, CE LR), and some other functions.

CPC drawer

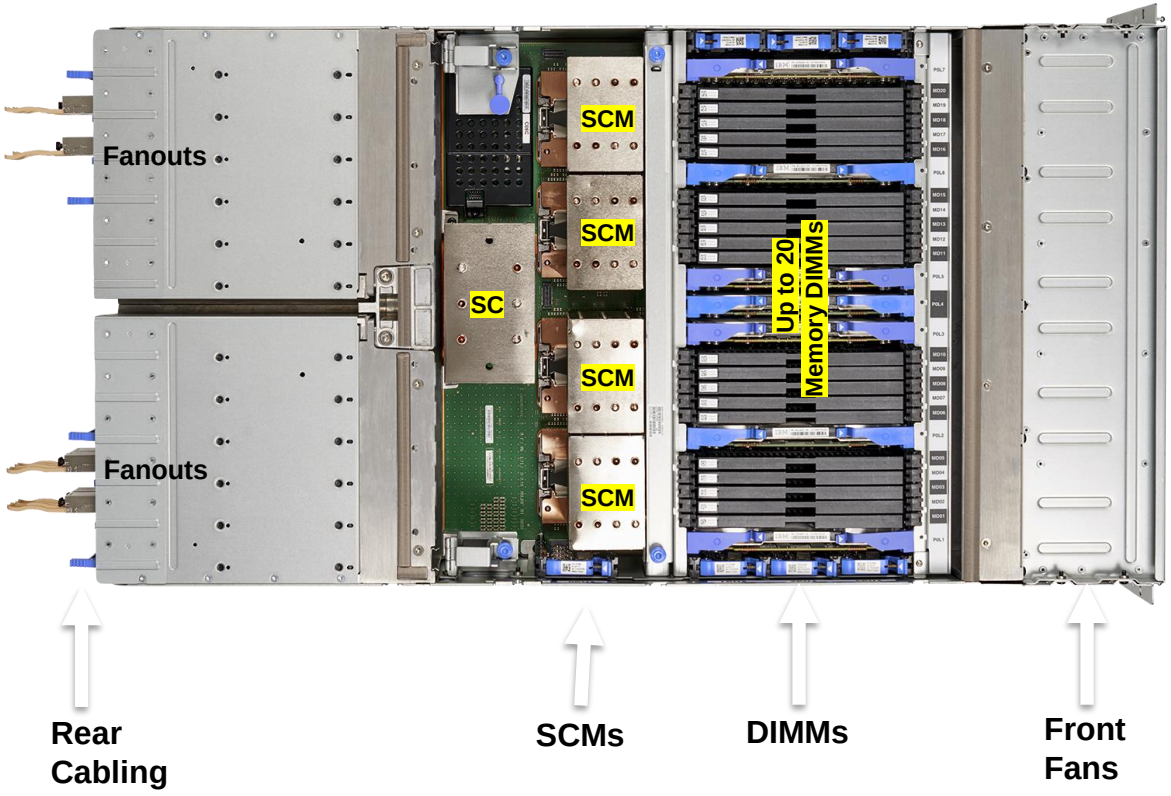
Each PU Single Chip Module (SCM):

- 14nm
- 7 to 11 cores
- One Memory controller
- Five DDR4 DIMM

Each CPC drawer:

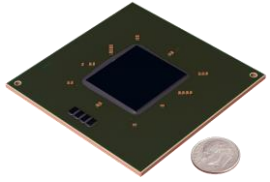
- 12 PCIe+ fanout slots for PCIe+ I/O drawer fanout or ICA SR coupling link.

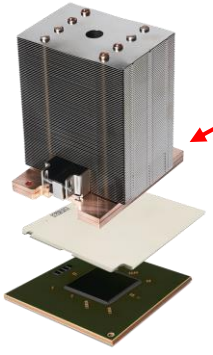
- Single System Controller (SC) 960MB L4



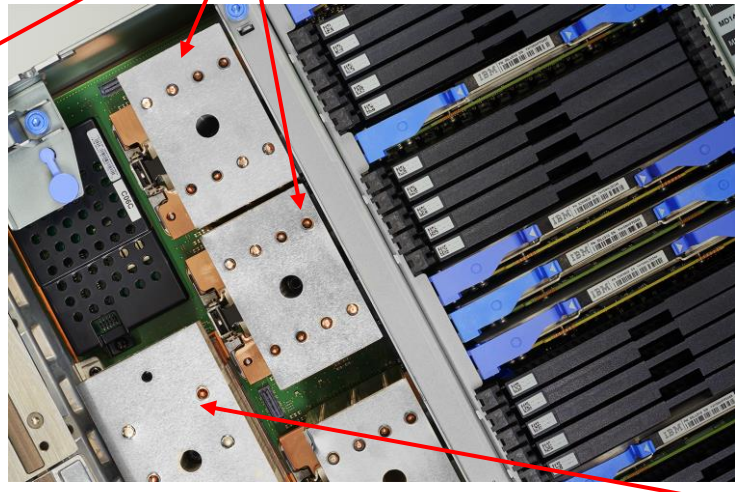
z15 Model T02 PU and SC SCM assemblies

PU SCM

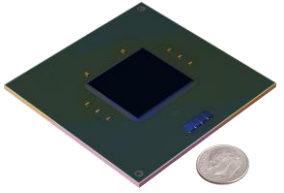


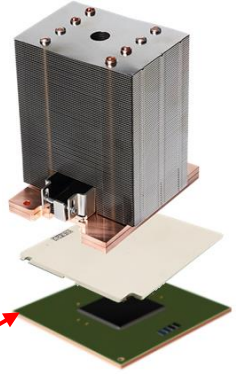


PU SCM (air cooled)
with heatsink



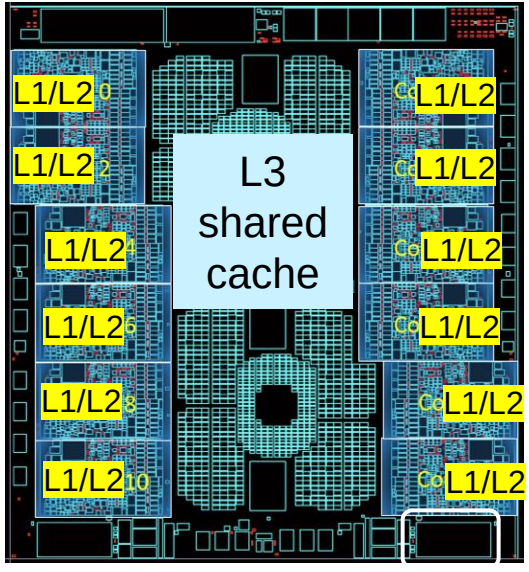
SC
SCM





1x SC SCM (air cooled)
with heatsink

12-Core / PU SCM detail



- On Core L1/L2 Cache
  - Protocol changes to reduce latency
- On chip L3 Cache
  - Protocol changes to reduce latency
  - Communicates with cores, memory, I/O and system controller single chip module.

- 14nm technology
  - 17 layers of metal
  - 9.2B transistors versus 6.2B on z14

- 20% reduction area
- 20% reduction in power
- 4.5 GHz
- Reduced cycles per instruction

Cache Summary - Comparison to z14 ZR1

Grow L2 (instruction) increase by 2x.	**2MB[i] 4MB[d] to 4MB[i] 4MB[d]**
Grow L3 increase by 2x.	**128MB to 256MB**
Grow L4 by 43%	**672MB to 960MB***

*For a Max65 system (two CPC drawer), the L4 cache is 1920 MB

Memory Considerations

Model	Feature	Min	Max
T02/LT2	Max4	64 GB	2 TB
T02/LT2	Max13	64 GB	4 TB
T02/LT2	Max21	64 GB	4 TB
T02/LT2	Max31	64 GB	8 TB
T02/LT2	Max65	64 GB	16 TB

Concurrent memory upgrades via licensed internal code (LICC) are available at several capacity levels.

- DDR4 Memory DIMMS (32, 64, 128, 256, 512 GB)
- An additional **160 GB** of memory is reserved above the customer purchase amount for the Hardware System Area (HSA).
- An additional **20%** of memory is reserved above the customer purchase amount for Redundant Array of Independent Memory (RAIM).

z15 8561 vs. 8562

- Announced – 09/12/2019, GA – 09/23/2019
- M/T 8561 - Model T01
- Five features – Max34, Max71, Max108, Max145, Max190
  - Up to 190 customer configurable engines
- Sub-capacity Offerings for up to 34 CPs
- PU (Engine) Characterization
  - CP, IFL, ICF, zIIP, SAP, IFP (No zAAPs)
- On Demand Capabilities
  - CoD: CIU, CBU, On/Off CoD, CPE
  - System Recovery Boost Upgrade
- Memory – up to 40 TB
  - Up to 16 TB per LPAR (OS dependent)
  - 256 GB Fixed HSA
  - Virtual Flash Memory (zFlash Express replacement (0.5 TB/feature, up to 12 features)
- 8561 Channels
  - Dual PCIe+ Gen3 16 GBps channel buses
  - Six LCSSs, up to 85 LPARs
  - Four Subchannel Sets per LCSS
  - OSA-Express7S (NB, 25GbE NB or CF)
  - OSA-Express6S and 5S (CF)
  - FICON Express16SA (NB)
  - FICON Express16S+, 16S and 8S (CF)

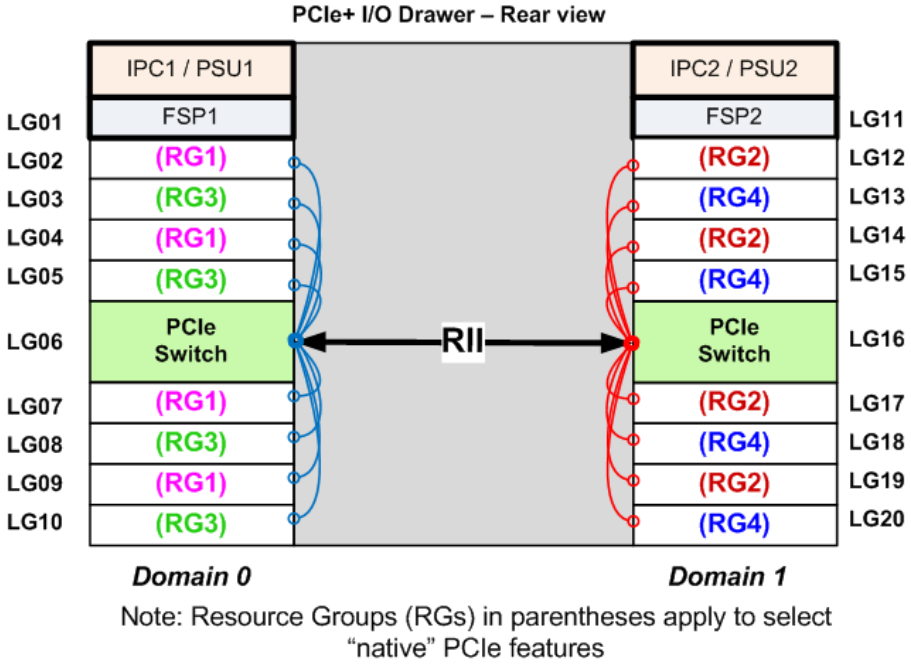
- Common Channels
  - IBM zHyperLink Express1.1 (NB)
  - IBM zHyperLink Express (CF)
  - 10 and 25 GbE RoCE Express2.1 (NB)
  - 10 and 25GbE RoCE Express2 (CF)
  - HiperSockets™ – up to 32
  - 10 GbE RoCE Express (CF)
  - Shared Memory Communications - Direct Memory Access (SMC-D)
- Crypto Express7S (6S and 5S CF)
- Parallel Sysplex clustering:
  - Coupling Facility Control Code Level 24
  - Support for 384 Coupling CHPIDs per CPC
  - Support for 64 Internal Coupling Links
  - CF Resiliency enhancements
  - ICA SR1.1 (PCIe) Coupling (NB)
  - ICA SR (PCIe) Coupling (CF)
  - Coupling Express Long Reach (NB or CF)

- Operating Systems
  - z/OS®, z/VM®, z/VSE, z/TPF, Linux on IBM Z, KVM for IBM Z
  - System Recovery Boost
  - Dynamic I/O for Standalone CF CPCs
- IBM Dynamic Partition Manager (DPM)
- IBM Secure Service Container
- IBM Integrated Accelerator for zEDC (On-chip compression Accelerator – zEDC Express replacement)
- IBM Z Hardware Management Appliance
- Secure Execution for Linux
- IBM Fibre Channel Endpoint Security (8561 only)
- Precision Time Protocol

- Announced – 04/14/2020, GA – 05/15/2020
- M/T 8562 - Model T02
- Five features – Max4, Max13, Max21, Max31, Max65
  - Up to 65 customer configurable engines (max. 6 CPs)
- Sub-capacity Offerings for up to 6 CPs
- PU (Engine) Characterization
  - CP, IFL, ICF, zIIP, SAP, IFP (No zAAPs)
- On Demand Capabilities
  - CoD: CIU, CBU, On/Off CoD, CPE
- Memory – up to 16 TB
  - Up to 8 TB per LPAR (OS dependent)
  - 160 GB Fixed HSA
  - Virtual Flash Memory (zFlash Express replacement (0.5 TB/feature, up to 4 features)
- 8562 Channels
  - Dual PCIe+ Gen3 16 GBps channel buses
  - Three LCSSs, up to 40 LPARs
  - Three Subchannel Sets per LCSS
  - OSA-Express7S 25 GbE (NB and CF)
  - OSA-Express 6S (NB and CF)
  - OSA-Express5S (CF)
  - FICON Express16S+ (NB or CF),
  - FICON Express16S and 8S (CF)

in blue: new

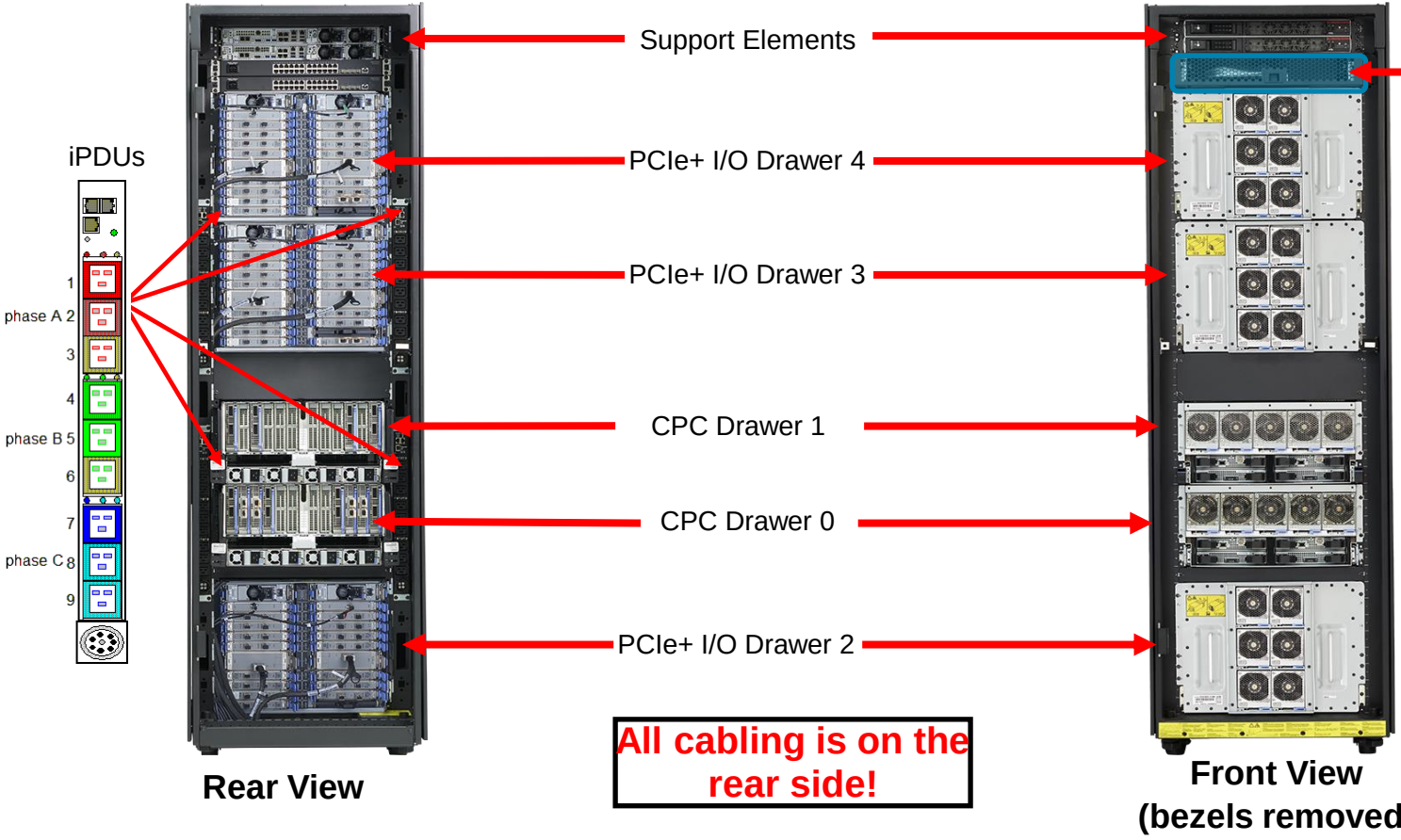
PCIe+ I/O drawer – 16 slots



Note: Resource Groups (RGs) in parentheses apply to select "native" PCIe features

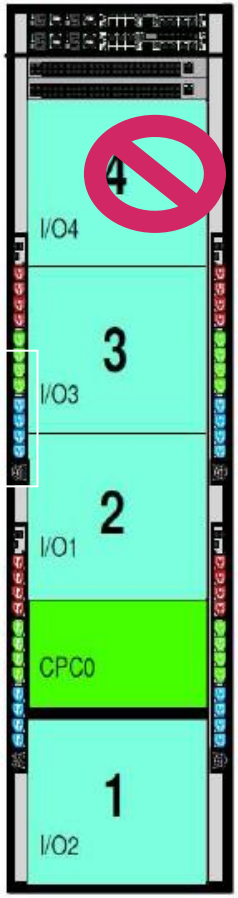
- First introduced on the z14 ZR1/Rockhopper II
- Supports 16 PCIe+ I/O adapters, horizontal orientation, in two 8-card domains.
- Requires two 16 GBps PCIe+ Interconnect adapters (✸), each connected to a 16 GBps PCIe+ Fanout Gen4 to activate both domains.
- To support Redundant I/O Interconnect (RII) between domain pairs 0/1 the interconnects to each pair will be from 2 different PCIe+ Fanouts.
- Concurrent repair of drawer & concurrent install of all I/O features (hot plug).

z15 Model T02 Max65

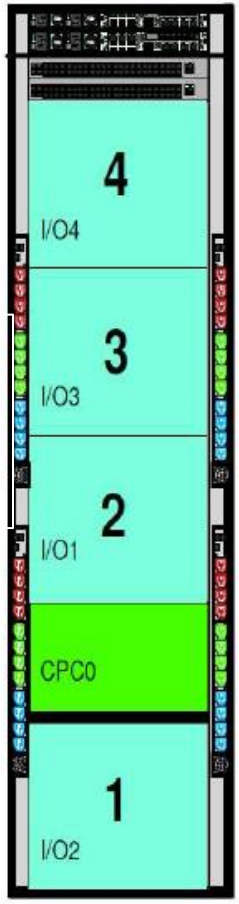


z15 T02 / LT2 I/O and CPC drawer config options

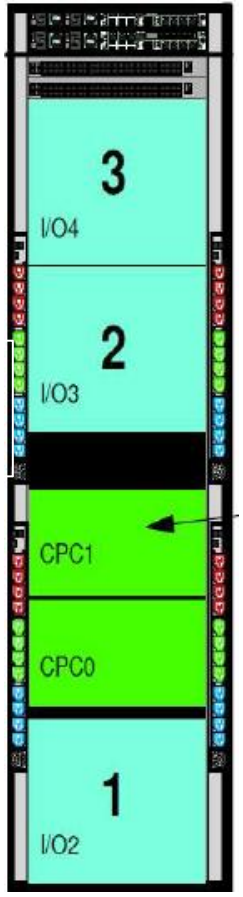
Max4
Up to
48 slots



Max13
Max21
Max31
Up to 64
slots



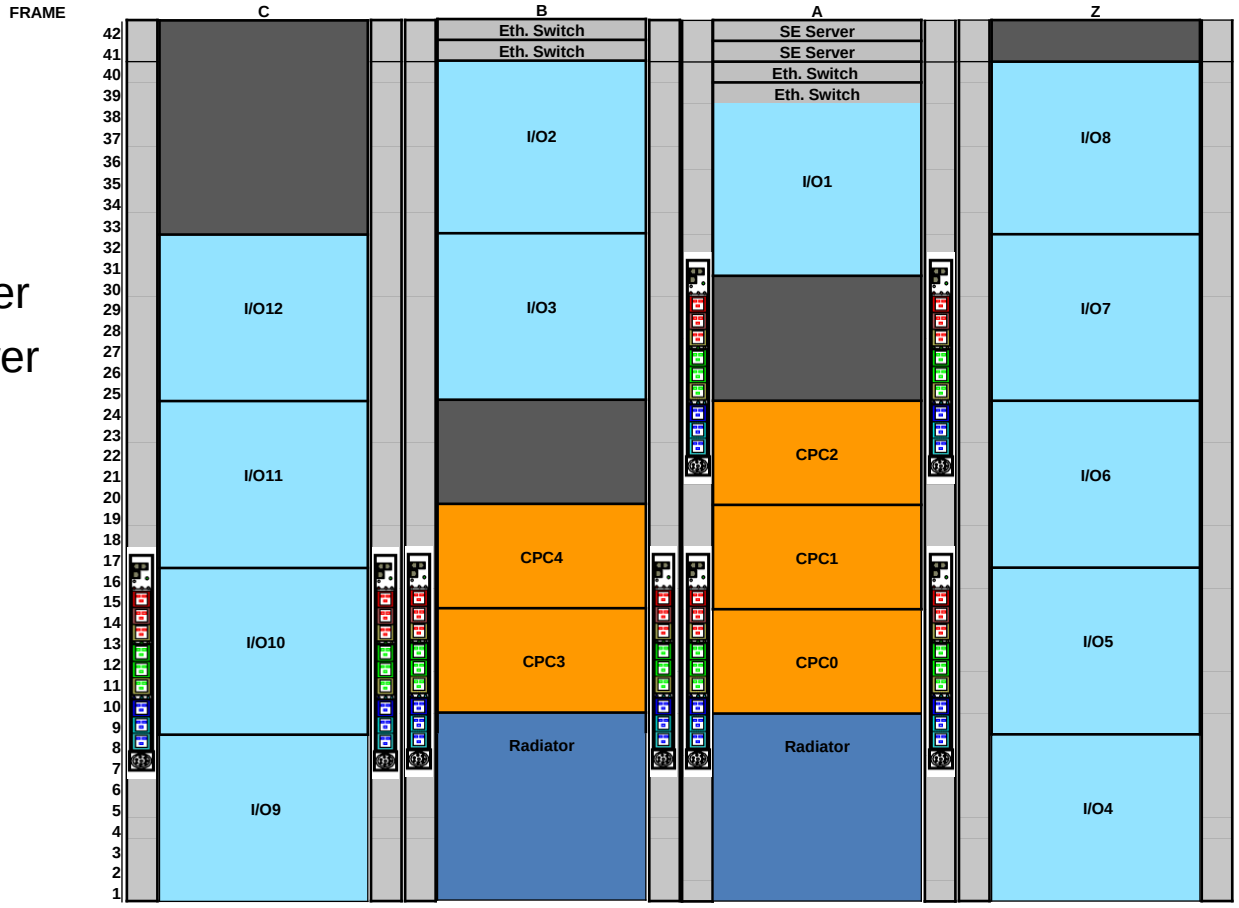
Max65
Up to
48 slots



Bold numbers indicate installation order.

z15 T01 front view (PDU, Four Frames, Z, A, B, C – Max190)

- Max 12 I/O drawer
- Max 5 CPC drawer



DS8910F into z15 Model T02 / LT2

IBM z15 Model T02

~ 500 TB capacity

IBM DS8910F

Delivering an end-to-end solution into a single 19-inch standard rack

IBM LinuxONE III Model LT2

IBM z15 T02 / LT2 – 16U / 8U Reserved Space

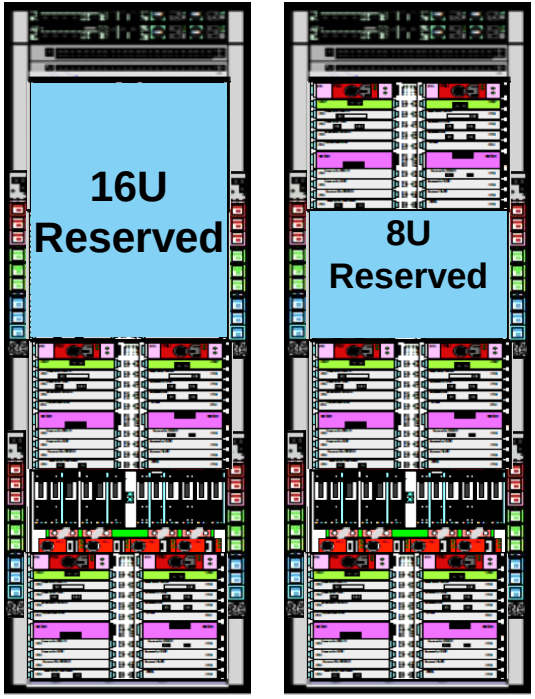
T02 or LT2

- 16U Reserved Space
  - DS8910F Model 993

LT2

- 8U Reserved Space
  - One or Two FS9200 + One or Two 8977-T32 switches
    or
  - One or Two FS7200 + One or Two 8977-T32 switches

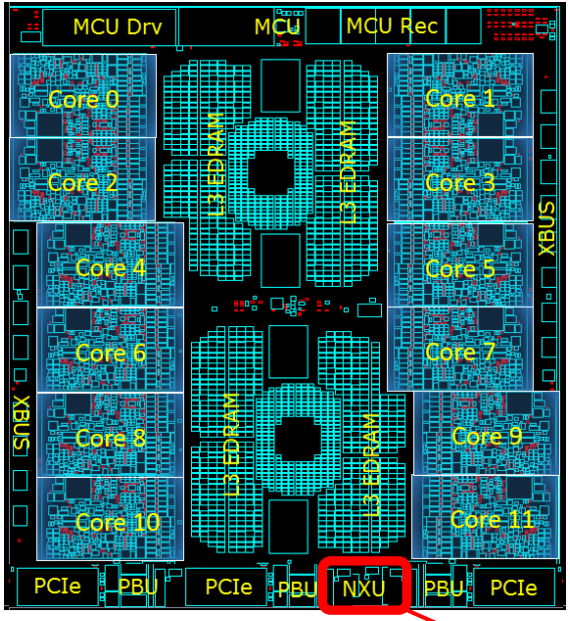
- Both needs single phase power

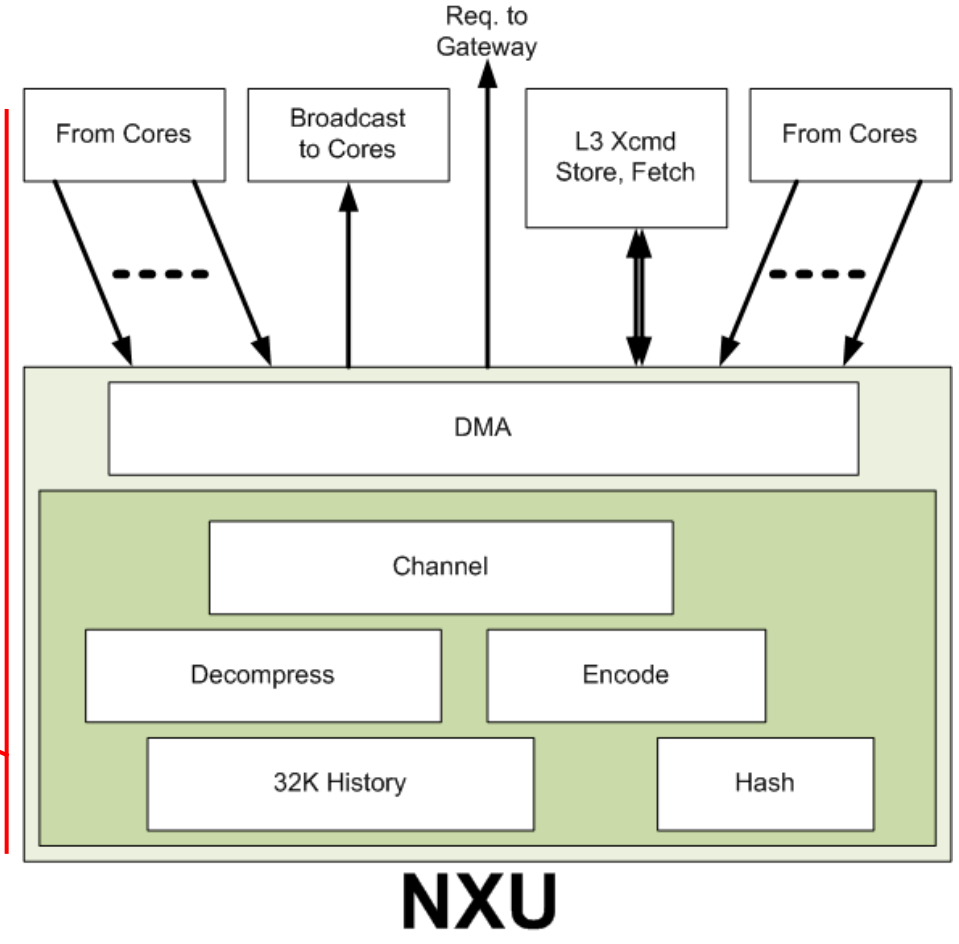


IBM Integrated Accelerator for zEnterprise Data Compression (zEDC)

z15 chip design incorporates a new compression unit
(one per PU SCM) for handling DEFLATE/gzip/zlib operations
This is the zEDC Express PCIe feature replacement

z15 Integrated Accelerator – Design Overview





z/OS Software Feature Exploitation zEnterprise Data Compression

z14

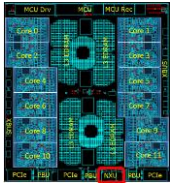
Chargeable: zEDC Hardware I/O feature required.

z/OS software feature required for exploitation of:

- **z/OS SMF Logstream**
- **z/OS QSAM/BSAM**
- **z/OS DFHSM / DFDSS**
- **Db2 for z/OS V12 LOBs**
- **z/FS in V2R3**
- IBM Java
- Cobol
- C
- IBM Content Manager OnDemand
- IBM Encryption Facility
- IBM Sterling Connect:Direct®
- z/OS HTTP Server
- OpenSSH
- IBM MQ for z/OS

z15

No Charge: Integrated Accelerator for zEDC hardware Built-in processor chips.



z/OS software feature required for exploitation of:

- **z/OS SMF Logstream**
- **z/OS QSAM/BSAM**
- **z/OS DFHSM / DFDSS**
- **Db2 for z/OS V12 LOBs**
- **z/FS in V2R3**

No z/OS software feature required for exploitation of:

- IBM Java
- Cobol
- C
- IBM Content Manager OnDemand
- IBM Encryption Facility
- IBM Sterling Connect:Direct®
- z/OS HTTP Server
- OpenSSH
- IBM MQ for z/OS

z15 Linux on Z Compression

Supported with

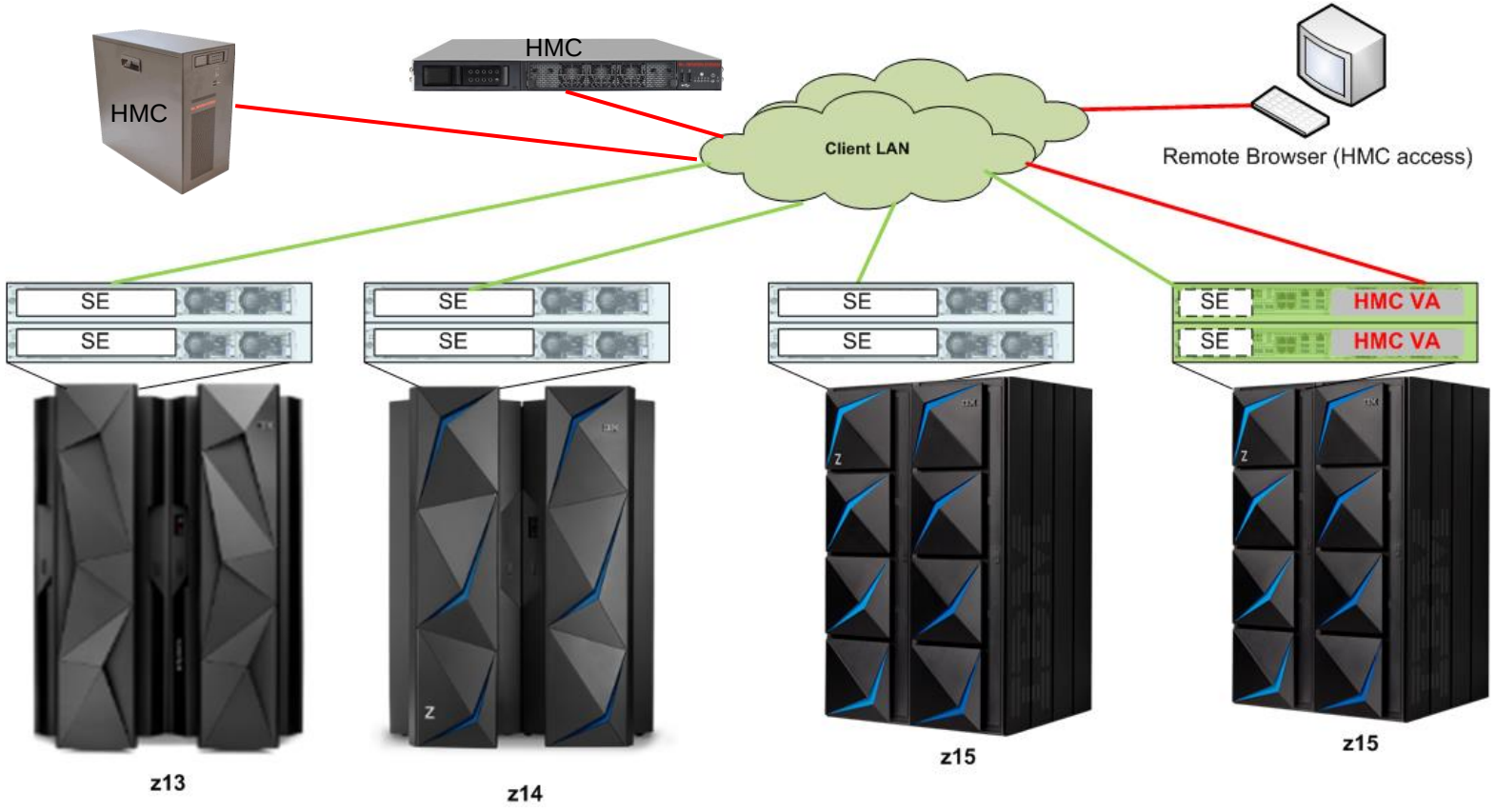
- Red Hat RHEL 8.1
- SUSE SLES 12 SP5
- Ubuntu 20.04

https://linux.mainframe.blog/zlib-acceleration

- On-Chip Compression provides value for existing and new compression users
- Less CPU consumption for compression
- Fully enabled in highly virtualized environments
  - All LPARs and VMs (z/VM & KVM) have 100% access
    - Avoids having to pick and choose which Linux guests may use accelerator
- Most beneficial for:
  - Java (e.g. IBM WebSphere Application Server)
  - Backup (e.g. for DBs)
  - Network traffic (e.g. Apache, NGINX)
  - IBM MQ

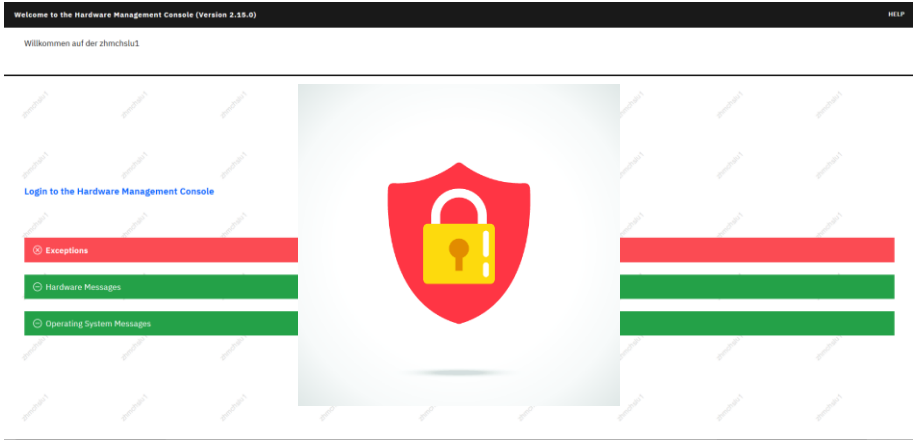
HMC / SE

IBM Z Hardware Management Appliance (HMA)

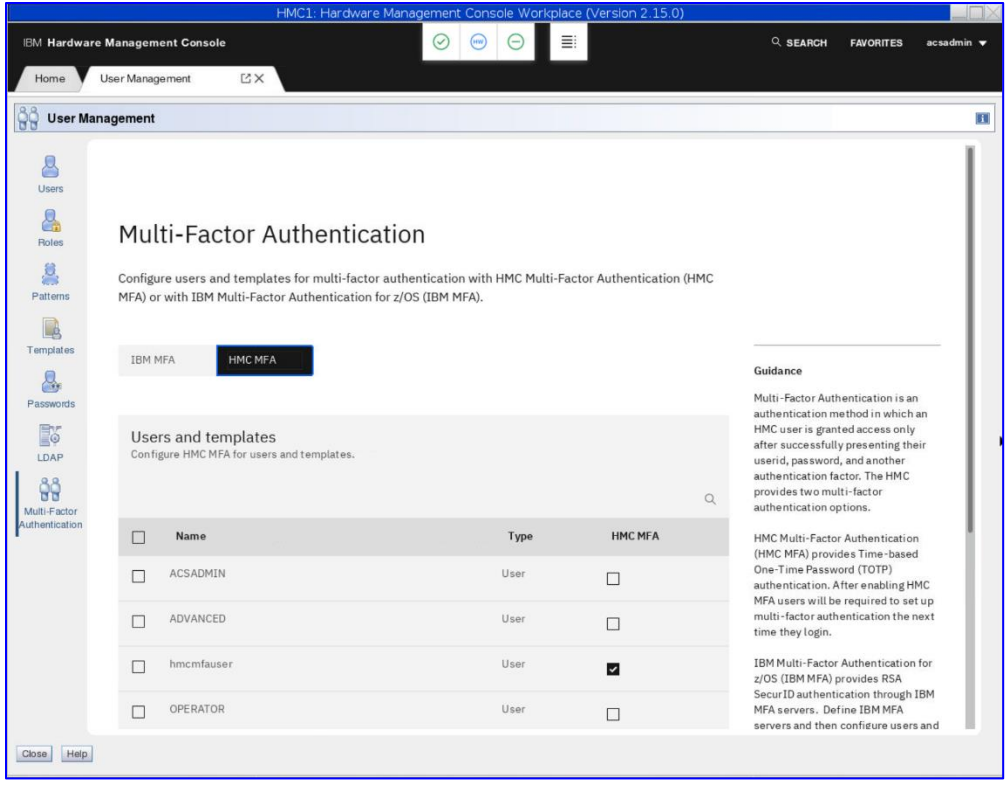


HMC default users

- Change default passwords (SYSPROG, ACSADMIN)
- Password for SERVICE -> change as well, but must be provided to the IBM technician
- Use personalized User IDs
  (just disable, NOT delete default users)
- Enable HMC Data Replication



HMC Multifactor Authentication – MFA



User Management Multi-Factor Authentication tab updated to support both

- HMC MFA
  Time-based One-time Password (TOTP)

IBM Security Verify

Google Authenticator

- IBM MFA for z/OS

Questions?

End of Section

Trademarks

FICON*	IBM Cloud Paks	Parallel Sysplex*	z/VM*
GDPS*	ibm.com*	z14	z/VSE*
HyperLink	IBM logo*	z15	
IBM*	IBM Z*	z/OS*	

Notes:
Performance is in Internal Throughput Rate (ITR) ratio based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed. Therefore, no assurance can be given that an individual user will achieve throughput improvements equivalent to the performance ratios stated here.
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