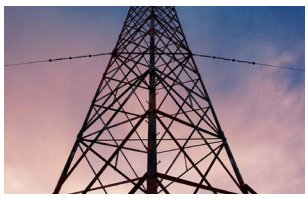
WIRELESS
Radio Solutions




Design Challenges

- Meeting the demand for high transmission efficiency
- Designing flexible, low-cost multi-mode radio solutions that support multiple connectivity standards
- Accommodating low power and thermal efficiency constraints
- Scaling designs to support heterogeneous networks
- Driving down BOM costs and driving up reliability

Xilinx Radio Solutions

- Highest level of integration, implementation for lower power and cost with higher reliability
- Xilinx CFR and DPD IP, providing more than 40% PA efficiency
- JESD204A/B, CPRI and OBSAI IP cores with serial transceivers to speed time to market
- Highly parameterizable IP to meet scalability and performance needs of heterogeneous networks
- Standardized interfacing for ease of integration
- Class-leading evaluation and development boards from Tektelic, Analog Devices, and Texas Instruments

XILINX
ALL PROGRAMMABLE™

INCREASING BANDWIDTH, SCALABILITY AND INTEGRATION FOR REDUCED INFRASTRUCTURE CAPEX AND OPEX

ALL PROGRAMMABLE MULTI-MODE RADIO Meeting Multi-Standard, Multi-Band, and Multi-Antenna Needs with Fewer Components

The demand for increasing coverage and capacity is driving the rapid expansion in heterogeneous networks encompassing femtocells, picocells, microcells, macrocells, and active antenna systems. Furthermore, in addition to the increasing number of form factors, complexity increases when considering the increasing number of frequency bands, air interface standards, growth in signal bandwidth and the demand for multi-antenna MIMO systems. The Xilinx Radio portfolio—spanning All Programmable FPGAs and SoCs, IP building blocks, design tools, reference designs, and development boards— is ideally suited for meeting the current needs of high-throughput radio systems. As a result, Xilinx digital radio solutions are fully flexible and can scale to support multiple standards, wider bandwidths, and varying performance needs of heterogeneous networks. In addition, these solutions also drastically reduce development time, providing increased system integration and flexibility to enable manufacturers to respond quickly to the demands of network providers.

CapEx and OpEx Reduction Through High Transmission Efficiency

Typical transmission efficiencies with 3G air interfaces on LDMOS* power amplifiers are in the range of 8 to 15%. Using advanced digital algorithms, efficiencies of up to 50% (LDMOS*) and 55%+ (GaN**) can be achieved with the latest-generation power amplifiers and Xilinx Crest Factor Reduction (CFR) and Digital Pre-Distortion (DPD) LogiCORE™ IP. This translates to significant savings per year in operational expenditure (OpEx). Capital expenditure (CapEx) is also reduced by enabling the use of smaller transistors in the power amplifiers, to deliver the same transmission power rating at the mast.

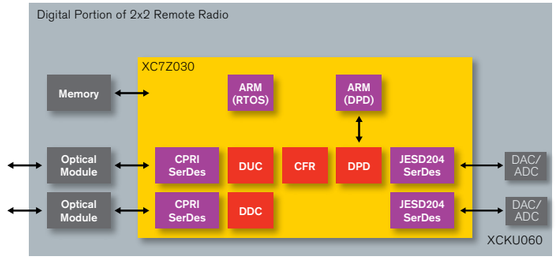
Integration is Key to Low Power, Low Cost and High Reliability

Replacing multiple ASSPs with a single Xilinx All Programmable FPGA or SoC results in the smallest digital PCB footprint. Xilinx devices combine a rich mix of high-performance DSP and logic resources for efficient implementation of digital up conversion (DUC), digital down conversion (DDC), CFR, and DPD algorithms with multi-gigabit transceivers (MGTs) capable of implementing CPRI , OBSAI, or JESD204B connections. Xilinx All Programmable SoCs' on-chip ARM processors and peripherals allow the further removal of external control processors for a single-chip radio implementation. Integrating all elements of radio processing in an All Programmable SoC allows the smallest, lightest, lowest-power and lowest overall cost radio equipment.

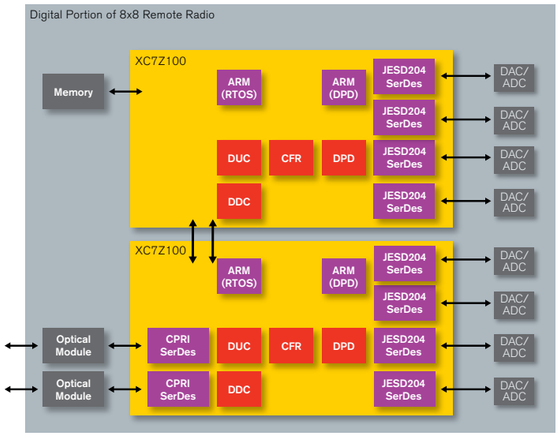
*Laterally Diffused Metal Oxide Semiconductor

**Gallium Nitride

ZYNQ®-BASED DESIGN EXAMPLE FOR 2X20MHZ (40MHZ) 2X2 LTE RADIO



ZYNQ-BASE D DESIG N EXAMPLE FOR 5X20MHZ (100MHZ) 8X8 TD-LTE RADIO



RESOURCE REQUIREMENTS RUNNING 368MHZ

FUNCTION	SOURCE	LUT	DSP	RAM
DUC: 2 Carrier 20MHz (2Tx)	Xilinx	2,087	23	1
DDC: 2 Carrier 20MHz (2Rx)	Xilinx	2,498	30	1
CFR: 3 Iteration [6 6 6] (2Tx)	Xilinx	8,549	45	21
DPD: 2Tx 1CPS Datapath 2 H/W accelerators	Xilinx	10,280	207	126
CPRI Master and Slave	Xilinx	6,325	0	5
JESD204B (2 Lane)	Xilinx	3,340	0	2
Total		**33,079**	**305**	**156**

42% LUTs, 76% DSP, 61% BRAM of Z-7030 with estimated total on-chip power: <10W.

RESOURCE REQUIREMENTS RUNNING 245/368MHZ

FUNCTION	SOURCE	LUT	DSP	BRAM
DUC: 5x20MHz (100M) (4 Tx)	Xilinx	21,930	272	2
DDC: 5x20MHz (100M) (4 Rx)	Xilinx	32,485	280	0
CFR: 4 Iteration [6,6,4,4] (4 Tx)	Xilinx	35,691	80	212
DPD: 4Tx 1CPS Datapath w/ 2 HW Accelerators	Xilinx	36,848	541	283
CPRI Master and Slave	Xilinx	4,280	0	8
JESD204B (4A 8 Lane)	Xilinx	4,512	0	4
Total			**1,173**	**509**

9% LUTs, 58% DSP, 67% BRAM of 7-Z100 with estimated on-chip power: <17W.

XILINX RADIO SOLUTIONS IP

PRODUCT	FAMILY SUPPORT	FEATURE HIGHLIGHTS
JESD204B	6 series 7 series Zynq-7000 AP SoC	▪ 1, 2, 3, 4, 5, 6, 7, or 8 lanes ▪ Scrambling and lane align ▪ Physical and data-link layers ▪ High-speed connection to MGTs at line rates up to 12.5Gbps
CPRI	6 series 7 series Zynq-7000 AP SoC	▪ Designed to CPRI V6.0 ▪ Supported line rates: 614Mbps to 10.1Gbps ▪ Auto-negotiation ▪ Master/Slave PHYs leveraging low-power MGTs ▪ 1 to 32 antenna-carriers per core
DUC/DDC Compiler	6 series 7 series Zynq-7000 AP SoC	▪ LTE (FD/TD-LTE), WCDMA or TD-SCDMA support ▪ 1-30 carriers per antenna ▪ 1-8 antennas ▪ Selectable IO sample rates
PC-CFR	6 series 7 series Zynq-7000 AP SoC	▪ LTE (FD/TD-LTE), CDMA2000, WCDMA, TD-SCDMA, WiMAX or MC-GSM (including frequency hopping) and multi-RAT ▪ Support for up to 100MHz BW in single-RAT and up to 80 MHZ in multi-RAT configurations ▪ 1-8 antennas ▪ Programmable latency ▪ 1-8 iterations ▪ Output peak to average power ratio (PAPR) of ~ 7dB at <4% error vector magnitude (EVM) ▪ >70dB adjacent channel leakage ratio (ACLR)
DPD	6 series 7 series Zynq-7000 AP SoC	▪ LTE (FD/TD-LTE), CDMA2000, WCDMA, TD-SCDMA, WiMAX or MC-GSM (including frequency hopping) and multi-RAT ▪ 1-8 antennas ▪ Optional QMC ▪ Optional hardware acceleration engines to improve update/convergence time (1A update rate ~50ms) ▪ Up to 40dB ACLR correction ▪ Support for 100MHz+ BW ▪ Up to 55% PA efficiency (GaN)

- Seamless scalability, supporting typical antenna array combinations such as 2T2R, 2R4R, 4T4R, and 8T8R.
- Dedicated peripherals for memory controllers and connectivity using All Programmable SoC processing sub-system (PSS), such as DDR2/3, UARTS, Gigabit Ethernet, SPI, I2C etc.

Heterogeneous Network Solution Scalability

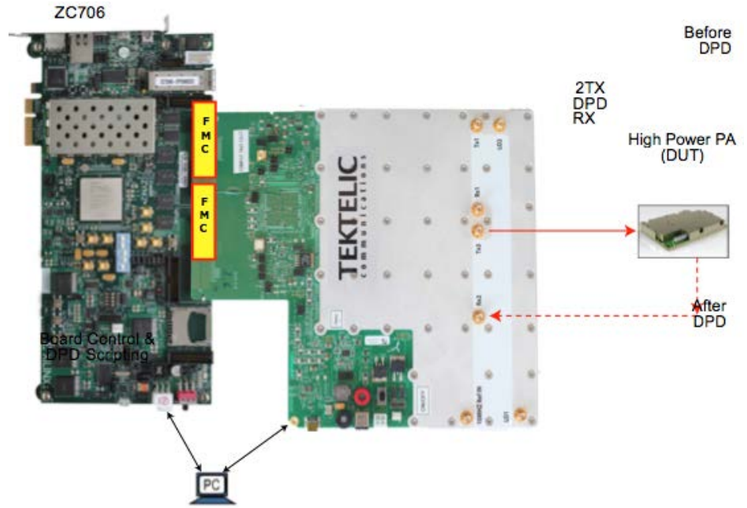
As OEMs develop solutions for heterogeneous networks, it is quickly realized that one size does not fit all. A choice of Xilinx devices and radio IP allows designers to smoothly scale from a low-complexity implementation such as a picocell to a high-end installation such as a wide-bandwidth multi-antenna macrocell. ASICs and ASSPs cannot match this scalability, and instead result in solutions that are limited to a fixed set of criteria and a narrow range of equipment. Xilinx All Programmable FPGAs and SoCs, combined with leading radio IP, allow customers to meet the needs of heterogeneous networks while maximizing cost efficiency, shortening time to market, and retaining full hardware and software flexibility.

	Small Cell	AAS/AIR	Mid Range RRU	High End RRU
	Low	Processing Complexity		High
Sample Specification	**2x2 20MHz** DUC/DDC CFR, DPD JESD204B **3G/4G**	**4x4 40MHz** DUC/DDC CFR, DPD JESD204B (CPRI/Beam Forming in separate device) **3G/4G**	**4x4 60MHz** DUC/DDC CFR, DPD JESD204B CPRI Master/Slave **2G/3G/4G**	**8x8 100MHz** DUC/DDC CFR, DPD JESD204B CPRI Master/Slave **4G**
Power	**<3W**	**<10W**	**<18W**	**<35W**
Cost	**$**	**$$**	**$$$**	**$$$$**
Device	**7Z020**	**7Z035/ 7Z045**	**7Z100**	**2x 7Z100**

Multi-Mode Radio Demonstration & Evaluation Platforms

Wireless radio subsystems must be designed with consideration for their environment. This is especially true of complex algorithms such as digital pre-distortion, where analog effects such as thermal, reactive transistor memory and analog signal chain behavior are not easily modeled. Xilinx has collaborated with the leading board vendors and data converter manufacturers to create a high-performance multi- mode radio demonstration platform showcasing DPD solutions with third-party power amplifiers at various frequencies and any air interface.

HIGH PERFORMANCE RADIO DEVELOPMENT BOARDS FEATURING TEKTELIC



Features

Xilinx Zynq AP SoC ZC706 Board

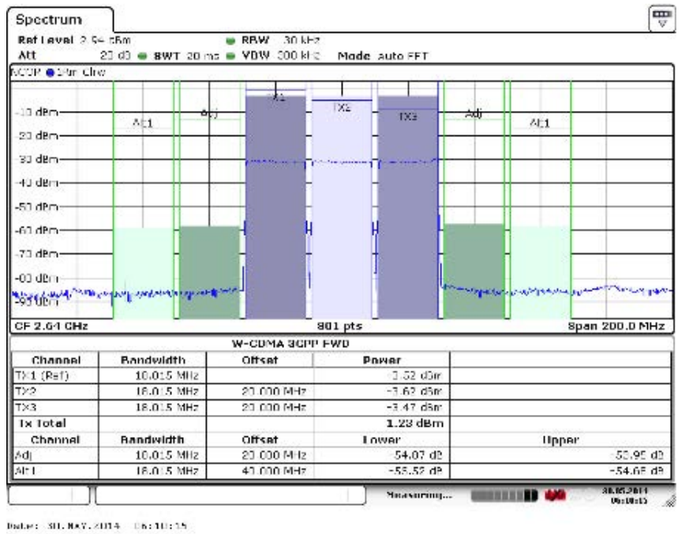
- SFP connector supports connectivity requirements of OBSAI and CPRI
- Zynq AP SoC enables development of complex DUC /DDC, CFR, and DPD algorithms for any waveform
- For full specification, visit: http://www.xilinx.com/products/boards-and-kits/ EK-Z7-ZC706-G.htm

Tektelic MSR Board

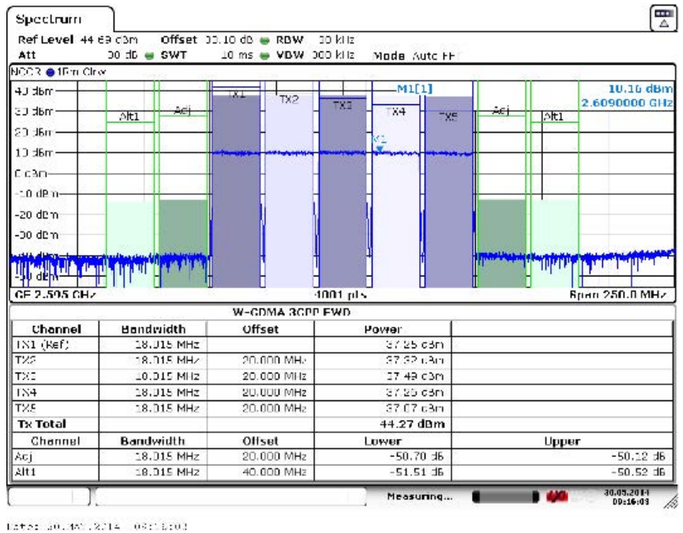
- Support for 100MH z+ transmission bandwidth
- Configurable at assembly for RF frequencies over 700MH z - 2.7GHz
- Meets stringent MC-GSM performance requirements
  - 2Tx, 2 DPD Rx (MIMO, Digital Doherty etc)
  - -170MHz Tx BW, High dynamic range (MC-GSM)

Example Performance Plots

- NXP pallet: BLC6G27-10G driver + BLC9G27LS-150AV final stage
- Test condition: TM3.1
- Note: Tests carried out with Tektelic MSR board



Plot 1: 3 LTE20-FDD carriers in 60MHz



Plot 2: 5 LTE20-TDD carriers in 100MHz

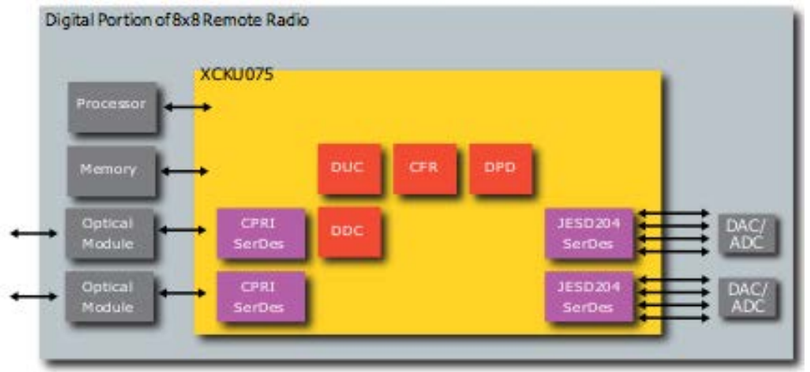
For more information on the Tektelic board for Xilinx, please visit http://www.tektelic.com

UltraScale Architecture for Next-Generation High-Speed Wideband Radio Designs

Xilinx has introduced its 20nm UltraScale™ devices and Vivado® Design Suite to enable the development of next-generation, high-performance systems. The UltraScale devices deliver ASIC-class, system-level performance for the most demanding next-generation applications that requires massive logic resource, massive I/O and massive DSP and packet-processing performance at the highest level of utilization without degradation in performance. The growth driver for UltraScale devices in radio designs is for high-end wireless applications evolving to high-order MIMO architecture and to wideband operation with multiple bands and bandwidths. This means simultaneous use of non-contiguous channels in aggregate bandwidth of over 100MHz. This shift is driven by the next generation of LTE and LTE-Advanced, where peak rates are defined as over 1Gbps at low mobility.

The UltraScale architecture significantly reduces power consumption over 28nm devices, allowing high-order MIMO and wideband radios to be designed to meet thermal constraints (e.g. 100MHz 8x8 radio). UltraScale devices can meet the corresponding connectivity needs by supporting 10.1Gbps CPRI line rates in addition to 12.5Gbps SERDES for JESD204. Furthermore, the UltraScale architecture has been designed in conjunction with the Vivado Design Suite to operate with high resource utilization (>80%) while operating at 491MHz system performance at the slowest speed grade. Although UltraScale architecture does not directly reduce cost over 28nm devices, the additional SERDES performance, power reduction, higher DSP density and high-speed operation means that UltraScale devices can offer total BOM cost reduction over multi-chip designs.

ULTRASCALE-BASED DESIGN EXAMPLE FOR 5X20MHZ (100MHZ) 8X8 TD-LTE RADIO



RESOURCE REQUIREMENTS RUNNING 245/368MHZ

FUNCTION	SOURCE	LUT	DSP	BRAM
DUC: 5x20MHz (100M) (8 Tx)	Xilinx	43,860	544	4
DDC: 5x20MHz (100M) (8 Rx)	Xilinx	64,971	560	0
CFR: 4 Iteration [6,6,4,4] (8 Tx)	Xilinx	71,382	160	424
DPD: 8 Tx HWA (1x)	Xilinx	75,311	1021	599
CPRI x4	Xilinx	8,560	0	16
JESD204B (8A 16 Lane)	Xilinx	9,024	8	0

79% LUTs, 72% DSP, 88% BRAM of XKU075 with estimated total on-chip power: <22W
*DPD V7.0 estimates based on using Microblaze and Hardware Accelerators.

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