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PAM4 Signaling for 56G Serial Link Applications – A Tutorial

Hongtao Zhang, Brandon Jiao, Yu Liao, and Geoff Zhang

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SPEAKERS

Geoff Zhang, SerDes Technology Group, Xilinx Inc.

geoff.zhang@xilinx.com

Geoff Zhang received his Ph.D. in 1997 in microwave engineering and signal processing from Iowa State University, Ames, Iowa. He joined Xilinx Inc. in 2013 as director of architecture and modeling in the SerDes Technology Group. Prior to joining Xilinx he has employment experiences with HiSilicon, Huawei Technologies, LSI, Agere Systems, Lucent Technologies, and Texas Instruments. His current interest is in transceiver architecture modeling and system level end-to-end simulation, both electrical and optical.

Outline

- **An overview of current status of 56G standards**
  - Early pioneers in PAM4 SerDes over a decade ago
  - From IEEE P802.3bj KP4 to OIF CEI-56G-PAM4 and IEEE P802.3bs
- **A brief review of high speed serial link using NRZ signaling**
  - High speed link system composition, signal integrity degradation
  - Nyquist frequency, signal PSD, frequency- and time- domain link analysis
  - Channel ISI and common equalization schemes: TX FIR, RX CTLE, RX DFE
  - Channel impedance mismatches, reflections, and system crosstalk impact
- **A tutorial on PAM4 signaling for high speed serial communications**
  - PAM4 basics, coding schemes and level mapping
  - Signal PDF, SNR degradations from NRZ to PAM4
  - Situations in which PAM4 has advantages over NRZ
  - PAM4 signaling slicer naming definitions and usages
  - Eye diagram anatomy – the difficulty for PAM4 signaling
  - Impact from various sources of impairments on PAM4 signaling

Outline (Con't)

- **A tutorial on PAM4 signaling for high speed serial links (Con't)**
  - Timing recovery: transition densities, 2x oversampled vs. baud-rate CDR
  - Transmitter FIR implementation and TX de-emphasis example
  - Receiver CTLE example in reducing channel ISI and opening up the eye
  - Analog-based RX architecture: CTLE/AGC, analog FFE, FIR-DFE, and IIR-DFE
  - ADC-based RX architecture: CTLE/AGC, analog FFE, ADC, DSP (FFE, DFE, …)
  - Equalizer coefficient adaptations and convergence example
  - On-die eye monitor, sampled eyes, and SER/BER computations
  - 1/(1+D) precoding to reduce DFE induced burst errors
  - FEC to help link system to achieve the desired BER (<1e-15)
  - Channel operating margin (COM) for PAM4 signaling
  - IBIS-AMI modeling and link simulations for PAM4 signaling
  - Test and measurement of PAM4 signaling – pattern definitions
- **Glossaries and References**

56G Standards Overview

Early Pioneers in PAM4 SerDes

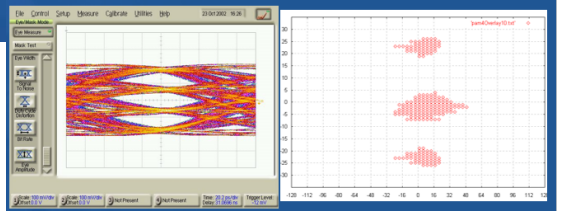
- About a dozen years ago there were two PAM4 SerDes designs out there, by *Rambus* and *Accelerant*, respectively, targeting 6-10Gbps applications

Equalization & Clock Recovery for a 2.5-10 Gb/s 2PAM/4PAM Backplane Transceiver Cell

May 2, 2003
Fred Chen
Sr. Member of Technical Staff
Rambus Inc.

Rambus

10G Eyes & System Margin Shmoos



- 3"/20"/3" = 26" Trace + 2 Connectors
- Tested to BER < 10^{-15}

UC Berkeley BWRC Seminar — Rambus

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Upgrade backplanes to 10 Gbps with 0% coding overhead.(leading edge)(Accelerant Networks AN6420)

EDN

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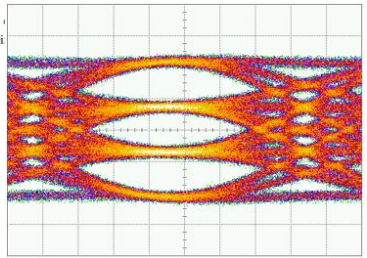
TRANSFERRING PAYLOADS as fast as 10 Gbps per differential pair with 0% coding overhead, the AN6420 quad high-speed backplane SERDES (serializer/deserializer) transceiver from Accelerant Networks operates at 6.25 to 10 Gbps using PAM4 (passband-amplitude-modulation) multilevel signaling. The device also interoperates with SERDES devices that operate as fast as 5 Gbps with DFE (decision-feedback equalization) in binary mode. You can use DFE to open eyes as small as 5 mV to guarantee signal integrity.

Coding schemes, such as 8B/10B or turbo coding, traditionally improve the robustness of a link by providing an error-correction mechanism—usually, an embedded pattern—within the raw bandwidth of the link, which may enable limited repair of corrupted data, thus increasing the BER (bit error rate). ...

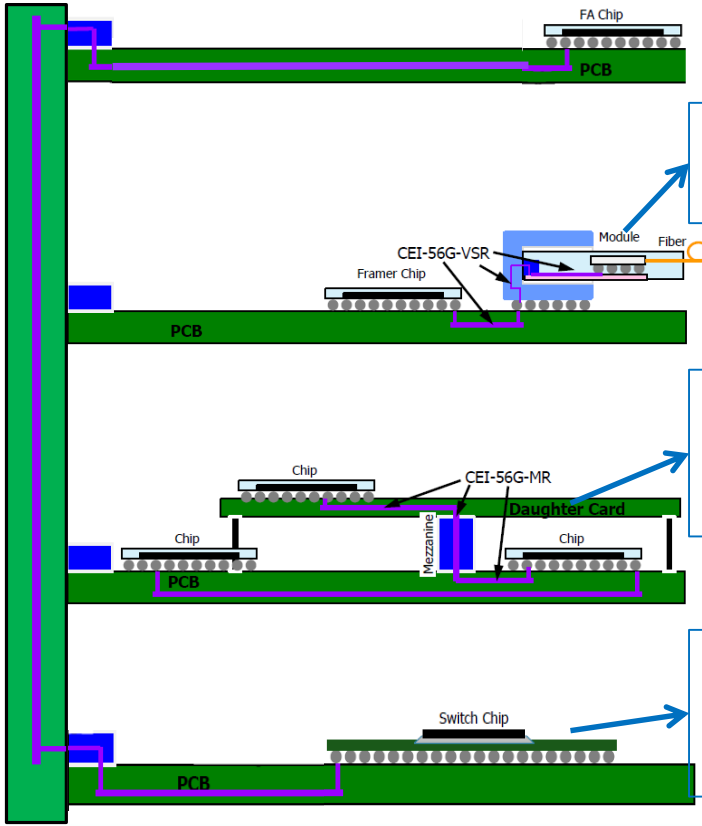
ACCELERANT NETWORKS



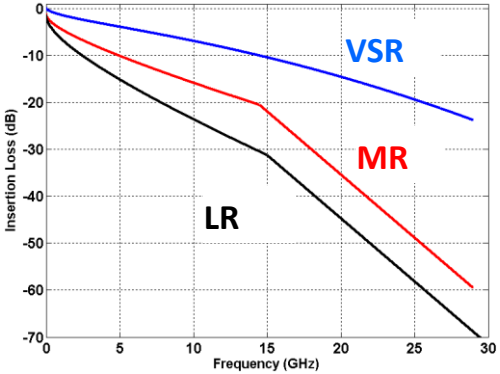
Starting from IEEE P802.3bj KP4

- The “Two-PHY” Solutions
  - 100GBASE-KR4: NRZ for 25.78Gbps NRZ (Clause 93)
    - 35dB at 13GHz with KR4 FEC or ≤ 30dB without FEC
  - 100GBASE-KP4: PAM4 for 28Gbps PAM4 (Clause 94)
    - 33dB at 7GHz with KP4 FEC
- KP4 the earliest PAM4 standard
  - Limited applications adopting it
- Moving to 56G using PAM4
  - IEEE P802.3bs and OIF CEI-56G-PAM4
  - Baseline specs are in a state of flux
  - Both standards leveraged a lot from the KP4 spec

CEI-56G-PAM4-VSR/MR/LR Baseline Specs

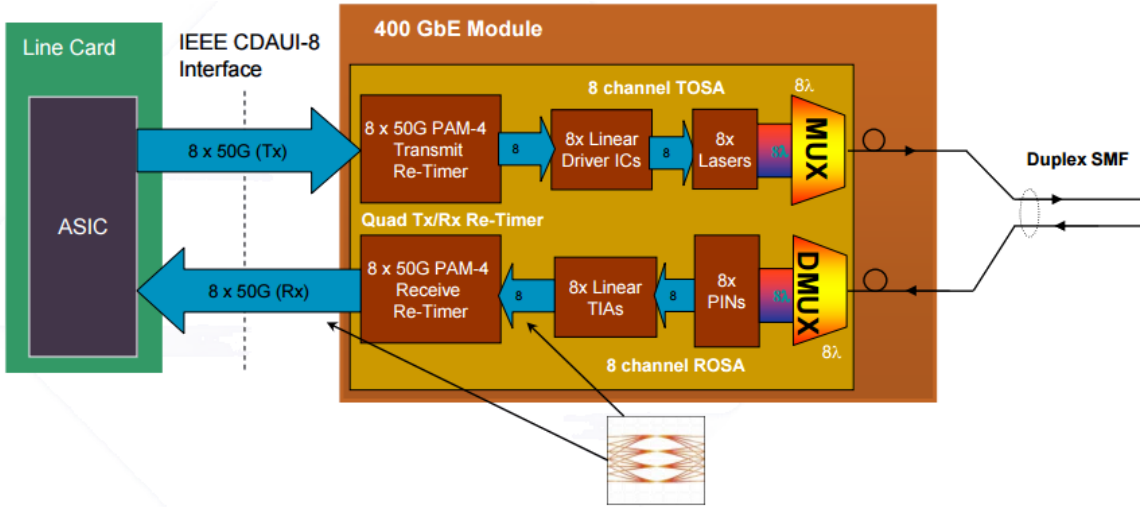


- **VSR: C2M, < 10cm, one connector**
  - **up to 10dB; raw BER < 1e-6**
- **MR: C2C for midrange backplanes, < 50cm, one connector**
  - **up to 21dB; raw BER < 1e-6**
- **LR: backplanes or copper cables, two connectors**
  - **up to 31dB; raw BER < 3e-4**



IEEE P802.3bs CDAUI-8

- The 400GbE task force (802.3bs) in March 2015 adopted
  - PAM4 for CDAUI-8 interfaces for C2C and C2M
  - RS(544, 514, 15, 10) FEC, the “KP4 FEC”



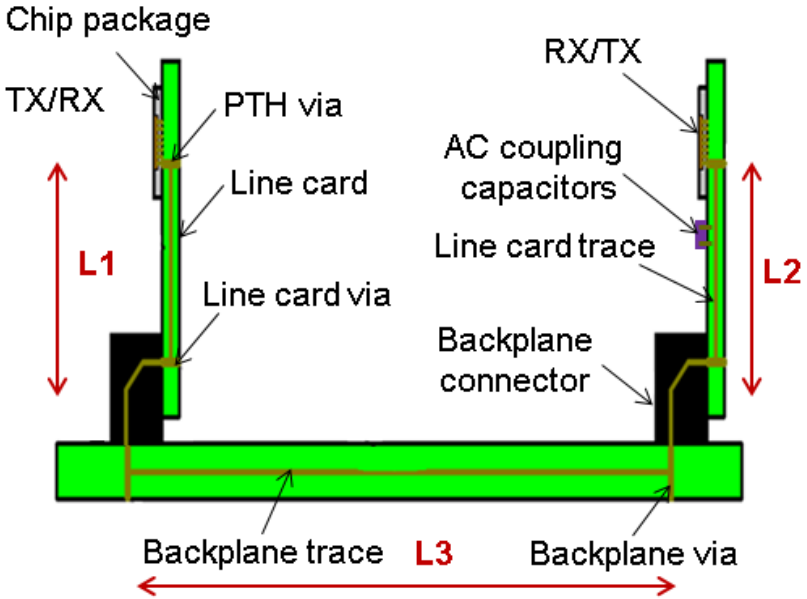
8 x 53.125Gbps

- PCS encoding ratio = 257/256
- KP4 FEC ratio = 544/514
- Thus, 544/514*257/256*50 = 53.125Gbps

A Brief Review of Serial Link using NRZ

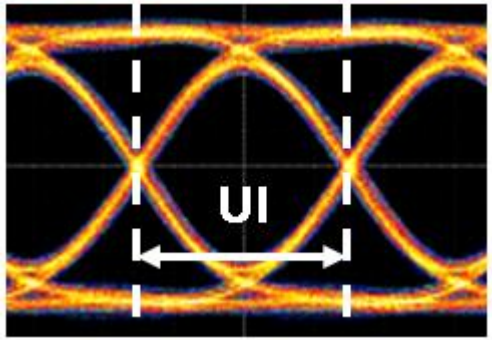
A Typical High Speed Serial Link

- Data is transmitted from TX to RX through a channel composed of various components
- The channel length can be as long as 1m for backplane channels and 5m for copper cable channels
- Signal integrity suffers along the path due to many impairments
  - Jitter, noise, intra-pair skews, frequency-dependent attenuation (ISI), reflections, crosstalk, etc.
- System margin depends on both passive and active components



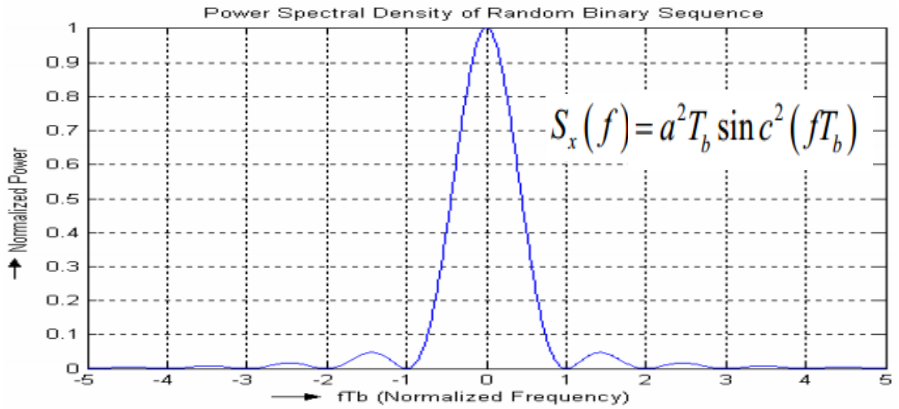
Non-Return to Zero (NRZ) Modulation

- NRZ (a.k.a. PAM2) is characterized by the following
  - Two variant voltage levels are used to represent a 0 and a 1
  - The voltage level remains constant throughout the bit interval
  - Symbol = Bit. There is one eye in each UI (unit interval)



- Example: for serial data at R_s = 56Gbps
  - UI (or T_b) = 1/56e9 = 17.857 ps < 18 ps
  - Nyquist frequency = R_s / 2 = 28 GHz

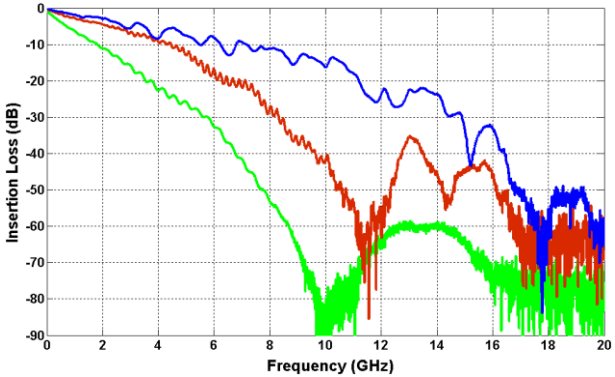
- Power spectrum density (PSD) follows ***sinc²()*** function
  - At R_s and its integer multiples, PSD is 0



Time-Frequency Domain Views and Conversion

Frequency domain (Insertion loss)

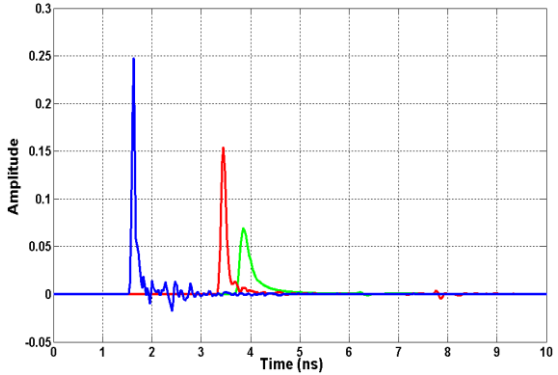
Loss, nulls, smooth/bumpiness, …



$$S_{21}(f) \Leftrightarrow h_{21}(t)$$

Time domain (Impulse response)

Delay, attenuation, spreading, ripples, …

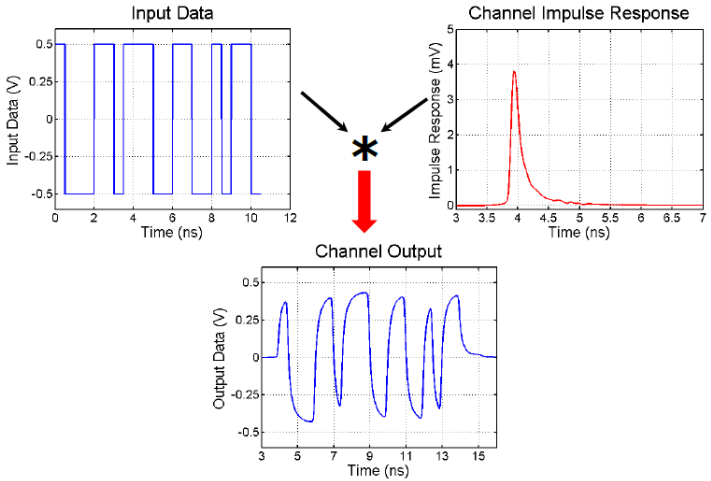


- Note that the more accurate transfer function can be derived as

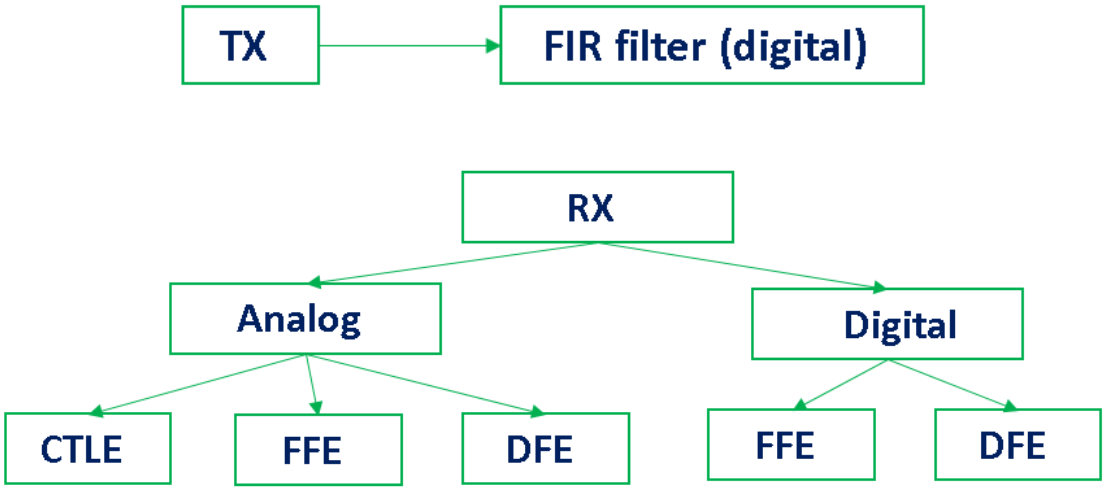
$$H(s) = \frac{V_2(S)}{V_S(S)} = \frac{S_{21}}{2}\left[\frac{(1-\Gamma_s)(1+\Gamma_L)}{(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L) - S_{12}S_{21}(\Gamma_S\Gamma_L)}\right]$$

Chanel ISI and Equalization Techniques

- Inter-Symbol Interference (ISI) depicts the phenomenon in which energy in one bit leaks into neighboring bits, on both sides

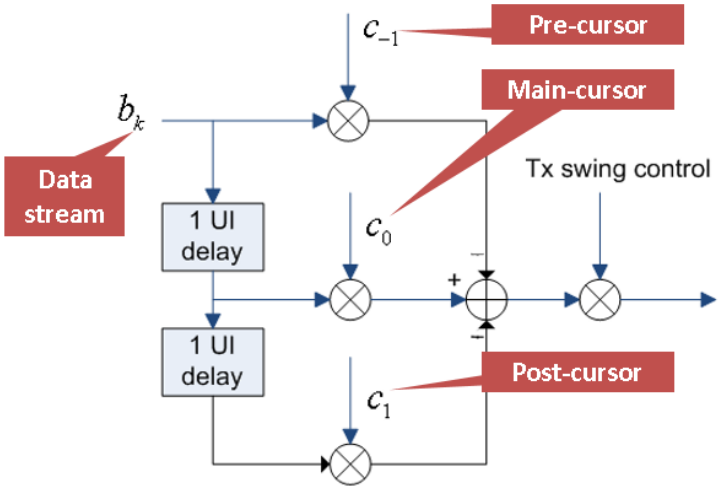


- Two commonly used techniques to mitigate ISI
  - *Equalization* is the most powerful and efficient
  - *Signal modulation* is another optional solution

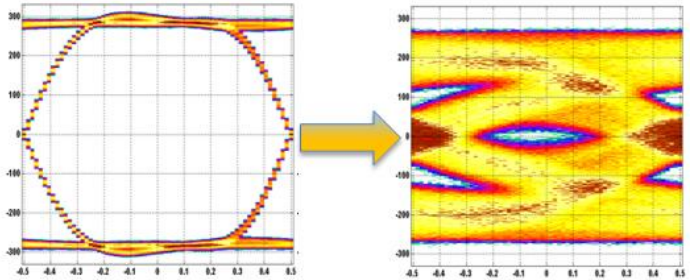


TX De-Emphasis via FIR Filtering

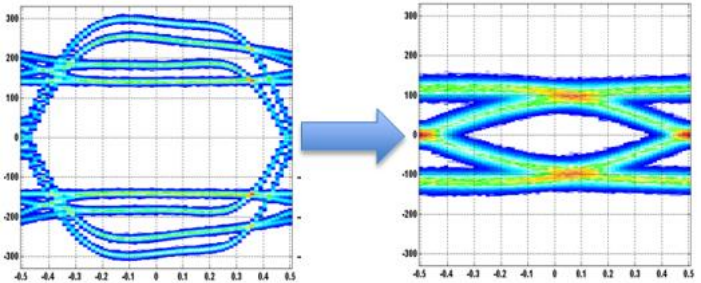
- 3-tap FIR example
- FIR coefficients typically satisfy
  - $C_{-1} + C_0 + C_1 = 1$
  - $C_0 - C_{-1} - C_1 > 0$



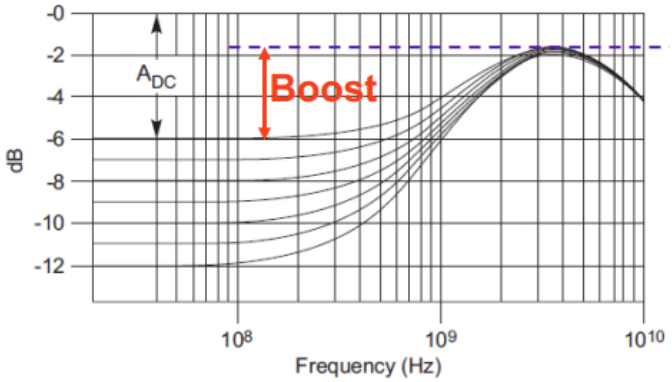
- $C_{-1}=0$, $C_0=1$, $C_1=0$ → 0dB de-emphasis



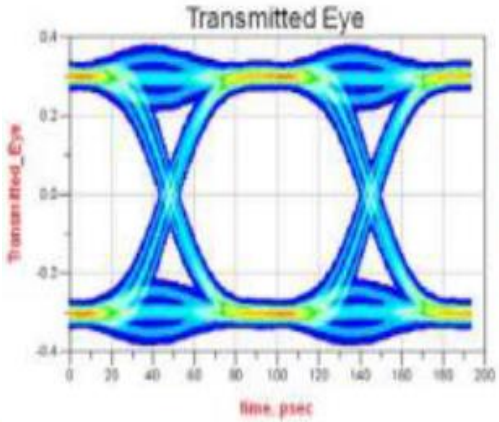
- $C_{-1}=0.075$, $C_0=0.75$, $C_1=0.175$ → 6dB de-emphasis

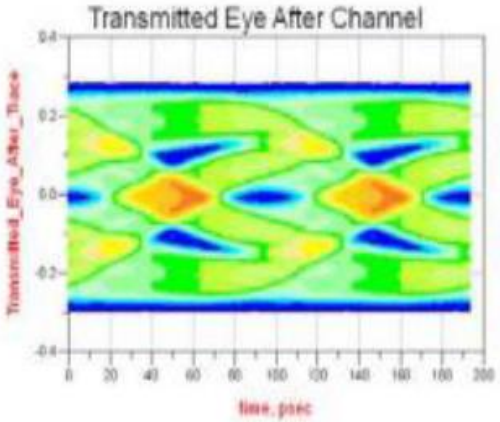


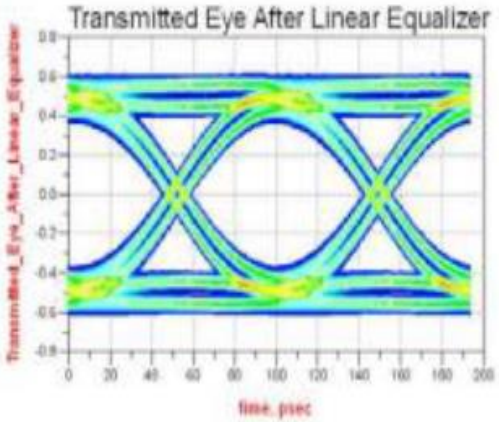
RX CTLE Equalization



- The CTLE filters RX input signal by either boosting high frequency content attenuated in the channel or relatively attenuating low frequency content
  - It introduces zeros to offset the freq-dependent loss
  - CTLE will have the same effect on noise
- The CTLE is generally preceded/followed by AGC

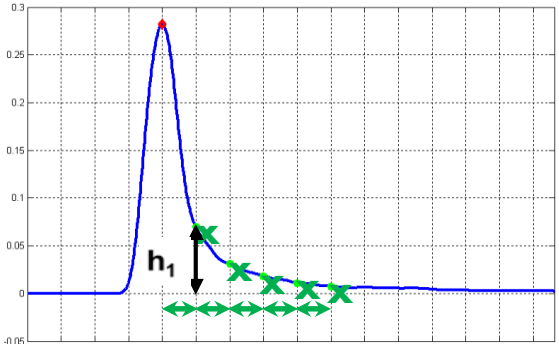


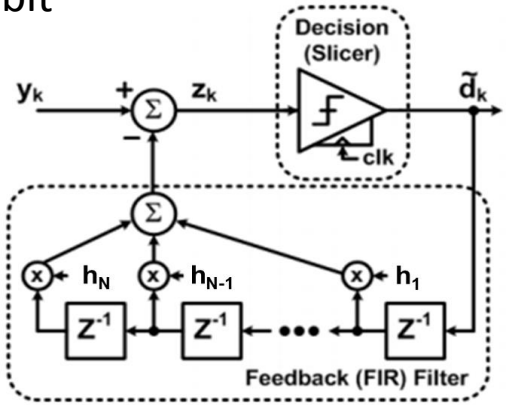


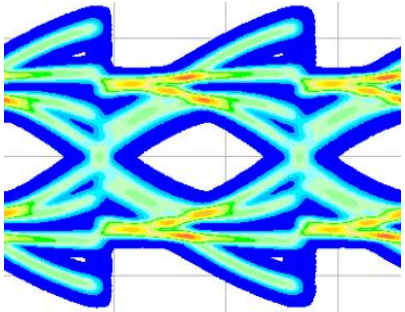


RX DFE for Removing Post-Cursor ISI

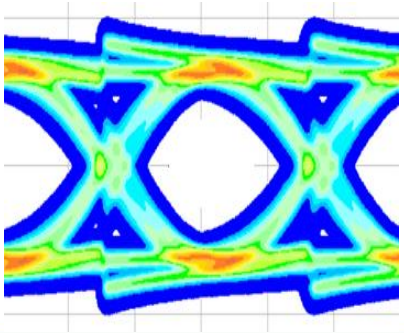
- DFE subtracts out channel impulse responses from the previous data bits so as to zero out post-cursor ISI contributions on the current bit







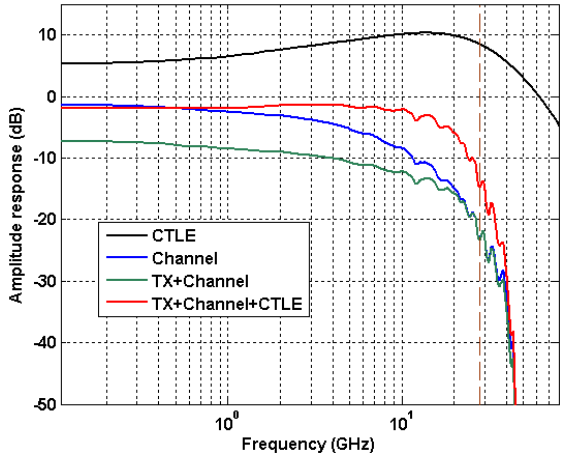
DFE tries to remove dominant positive ISI to open up the eye

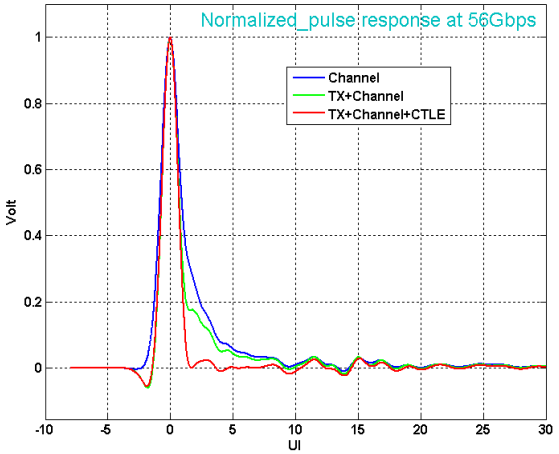


DFE needs to counteract dominant negative ISI to open up the eye

Channel Equalization Goals

- The preliminary goal of channel equalization can be viewed as
  - In f-domain: to flatten the response within the frequency of interest
  - In t-domain: to remove pre- & post- cursor ISI and restrict energy

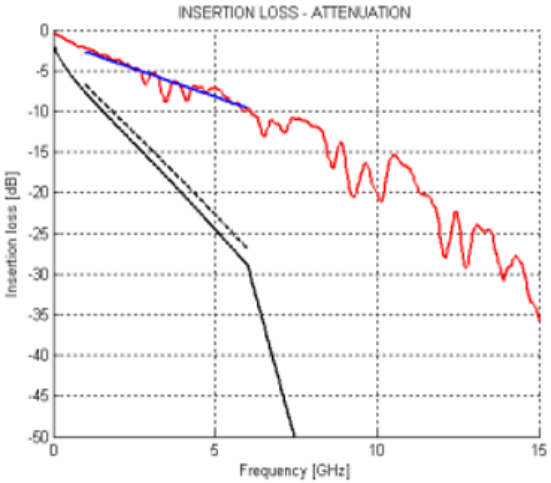


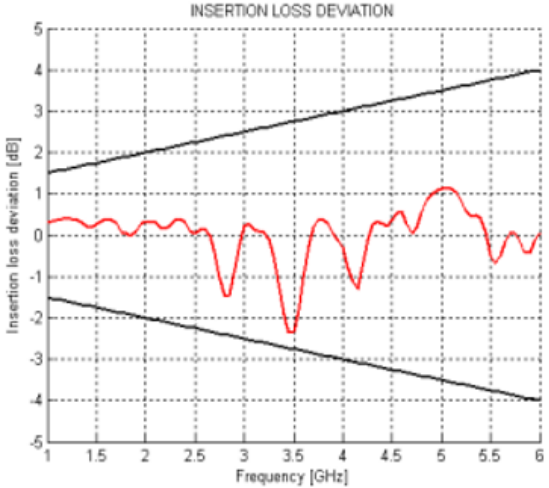


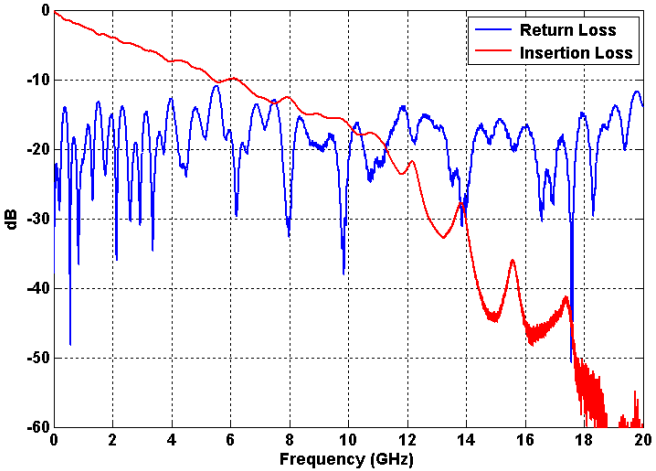
- Non-linear equalizers, such as DFE, do not directly fit into the above picture
- The ultimate goal is to ensure the system works within the BER target

Reflections Could be More Harmful Than Loss

- Reflections, due to channel impedance mismatches, could be even more harmful than channel insertion loss in certain link setups
- Insertion loss deviation (ILD, defined as ILD = IL – fitted attenuation) is used to characterize channel smoothness

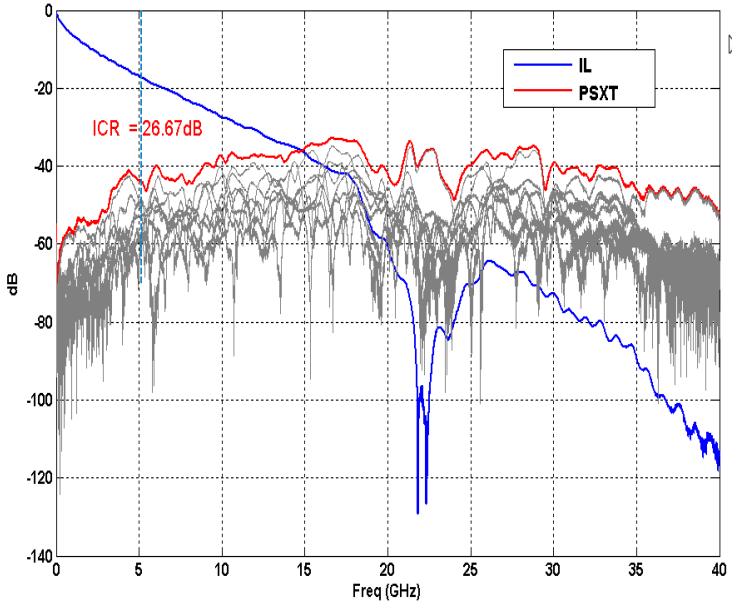






Crosstalk Could be More Harmful Than Loss

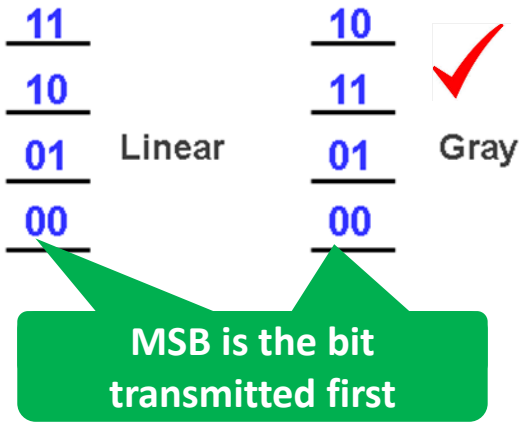
- Crosstalk (noise coupled through vias, connectors, packages, etc.) could be more harmful than channel insertion loss in link setups
- Several different concepts are used to assess the strength of crosstalk, evolved as data rate increases
  - **PSXT**: power sum of crosstalk
    - PSNEXT – power sum of NEXT
    - PSFEXT – power sum of FEXT
  - **ICR**: insertion loss to crosstalk ratio, defined as *IL - PSXT*
  - **ICN**: integrated crosstalk noise
  - **COM**: channel operating margin



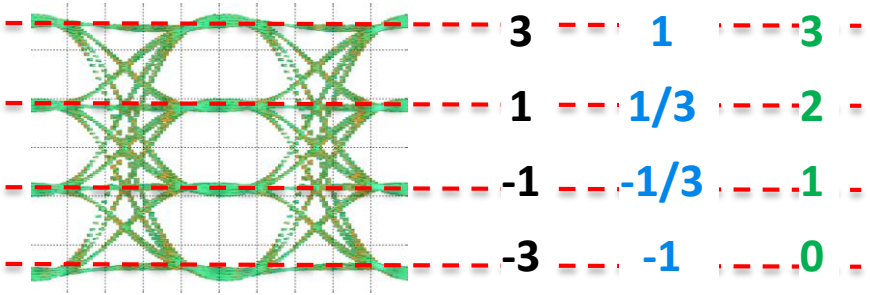
A Tutorial on PAM4 for Serial Link

PAM4 – 4-Level Pulse Amplitude Modulation

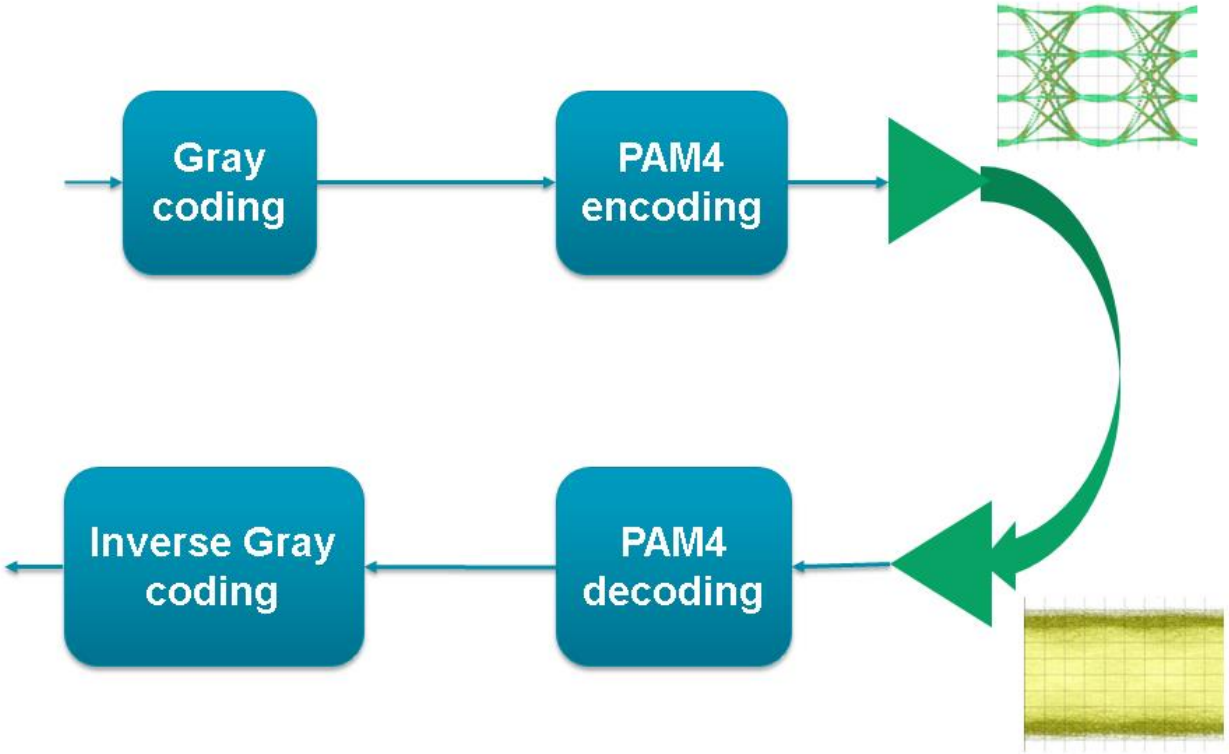
- Every 2 bits are mapped to one symbol
- 2-bits has 4 unique combinations, thus 4 signal levels
- The mapping can be “Linear” or “Gray”
  - Gray coding
    - Only one bit error per symbol is made for incorrect decisions
    - Support dual-mode with PAM2, by grounding the LSB
    - This is the coding adopted in all the PAM4 standards



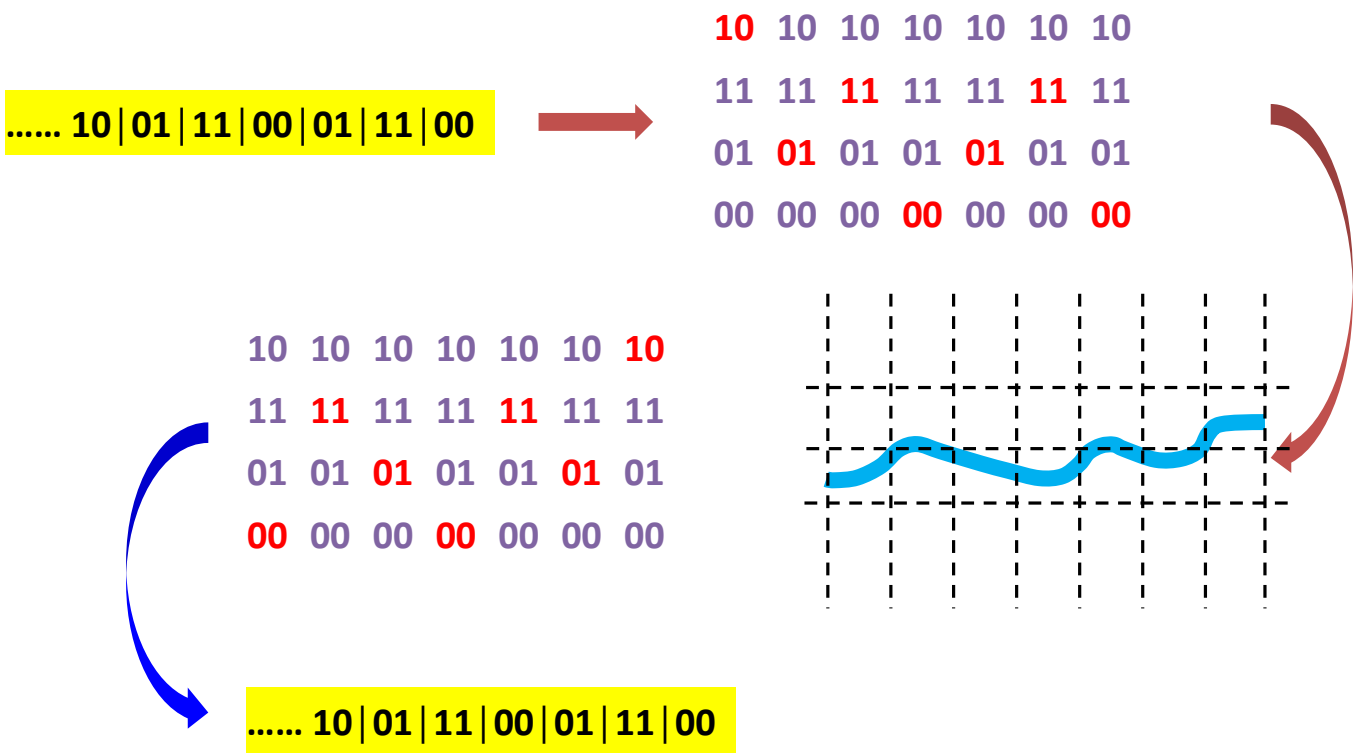
- Three common naming conventions for PAM4 signal levels
  - They might be used interchangeably in this presentation



TX and RX Signaling Process – 1

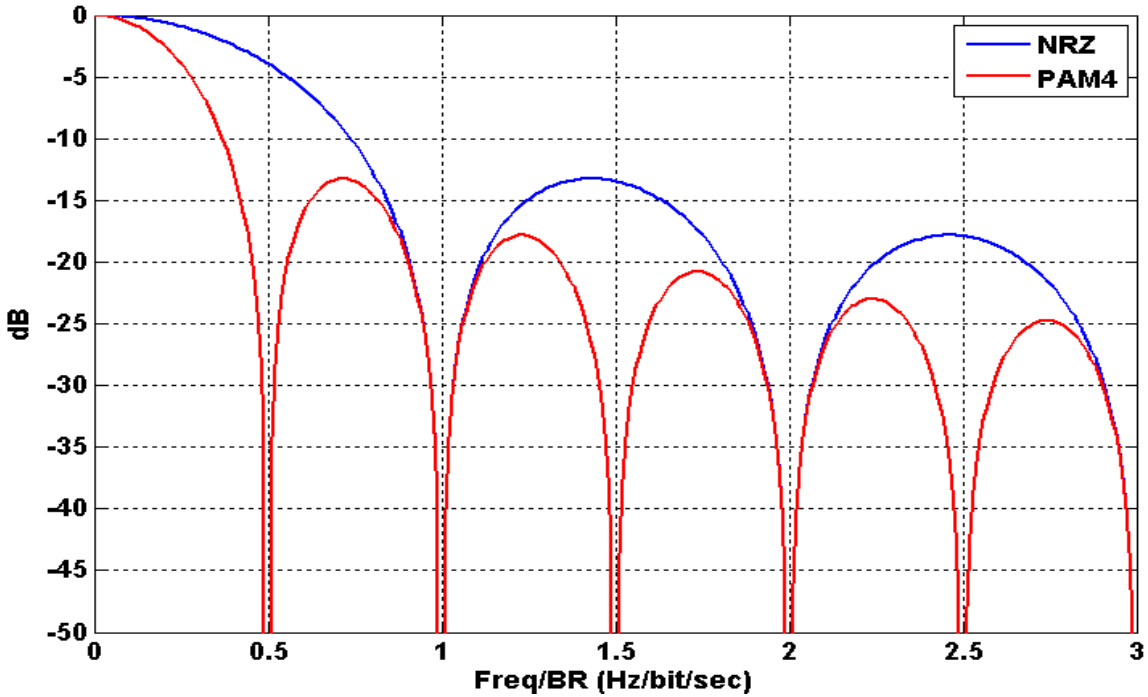


Binary to PAM4 and Back to Binary Example

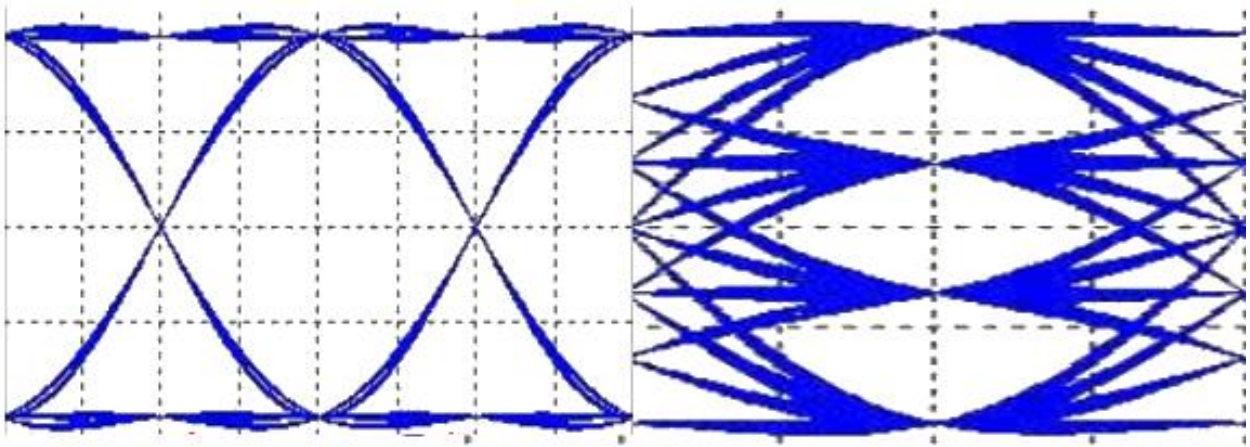


PAM4 Power Spectrum Density

- PAM4 only requires half of the bandwidth of that of NRZ, as can be seen from its PSD (red), in comparison with the PSD for PAM2 (blue)
- For the same throughput, if NRZ is 56Gbps, then PAM4 is running at 56Gbps or 28Gsym (per second) or 28GBd (per second)
  - The Nyquist frequency for PAM4 is 56/4 = 14GHz
  - The Nyquist frequency for PAM2 is 56/2 = 28GHz

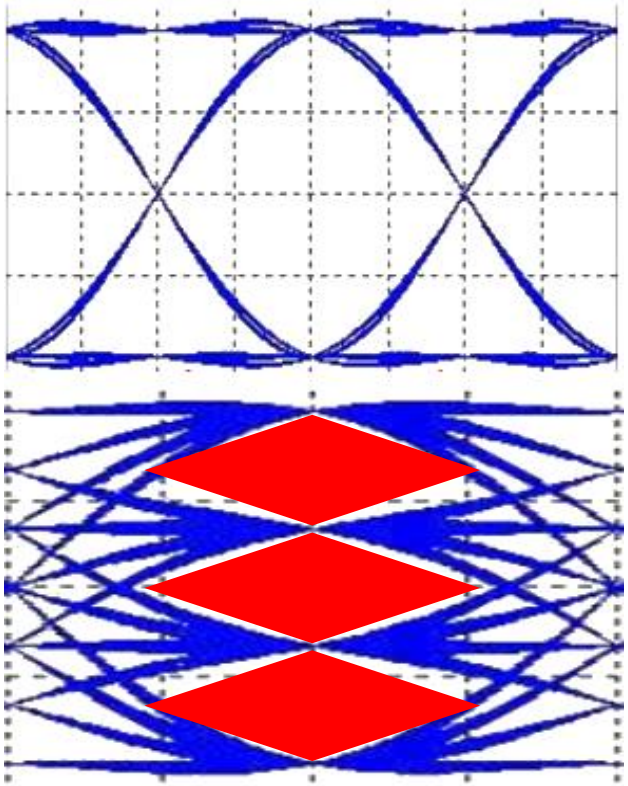


Eye Height Comparison between PAM2 & PAM4



- Eye height for PAM4 is 1/3 of that of PAM2, thus
  - SNR loss = $\mathbf{20 * log10\left(\frac{1}{3}\right) \sim 9.5dB}$
- In practice, there is further degradation due to nonlinearity
  - Together one should consider >*11 dB* SNR penalty

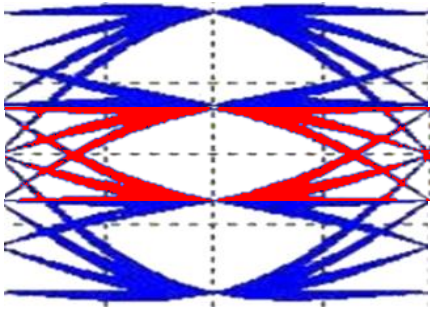
Eye Width Comparison between PAM2 & PAM4

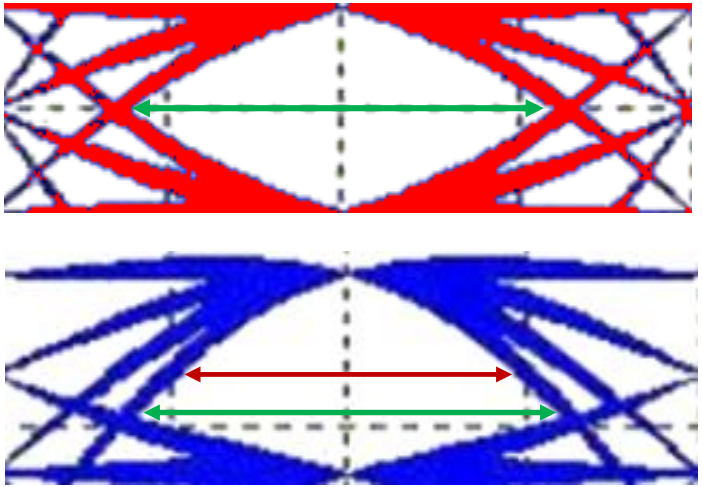


- The illustration is based on raised cosine channel with $\beta = 1$
- Although the Nyquist frequency is half for PAM4 than for PAM2, in reality the real eye width is only between 1/2UI and 2/3UI, far less than 2x of NRZ eye width
- The 3 vertical eyes are not symmetrical
  - Because PAM4 has four voltage levels, there are transitions between non-adjacent signal levels, which take longer time than required for transitions between adjacent levels, thereby narrowing the eye

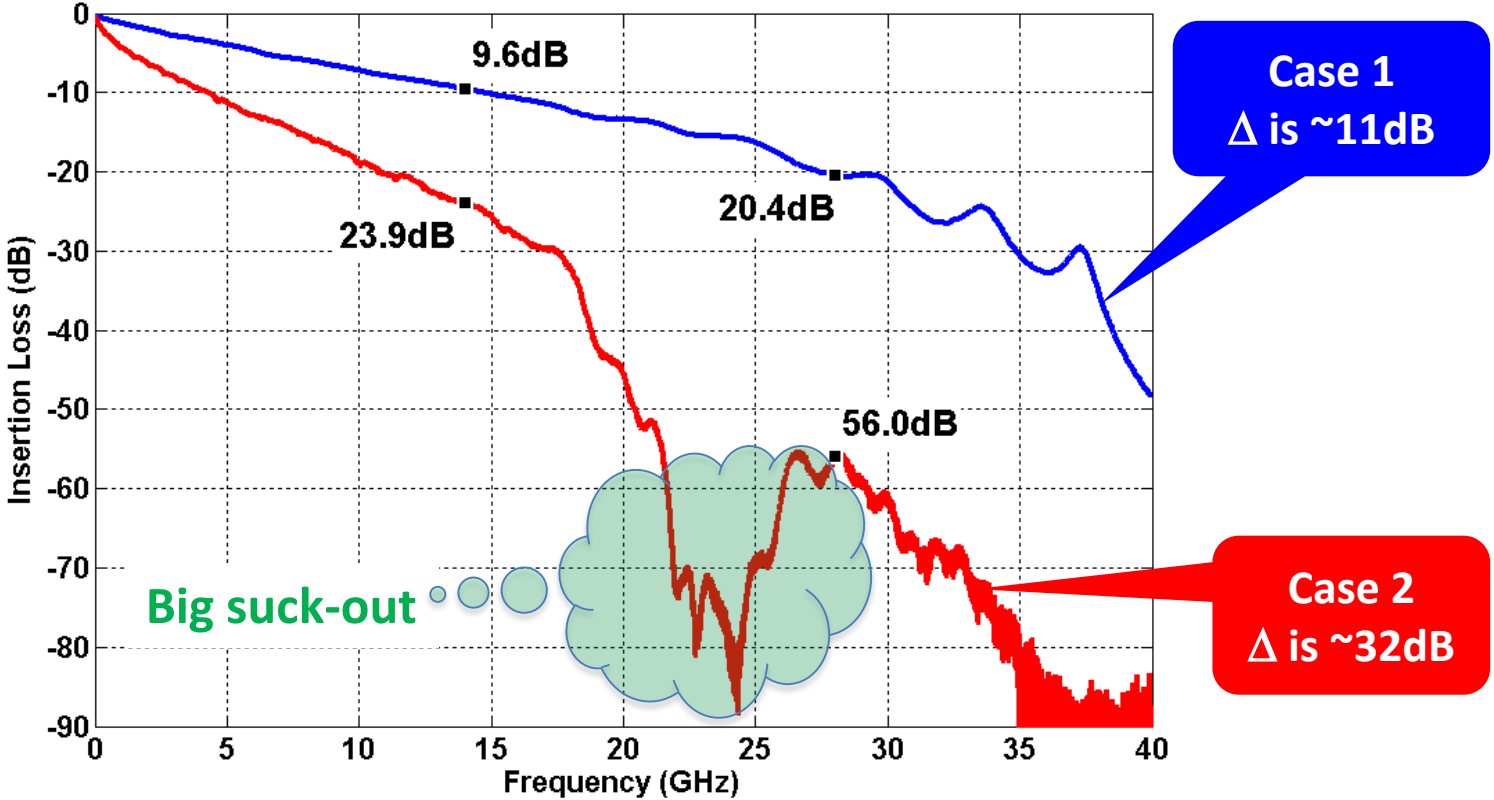
More on Eye Height and Eye Width

- The middle eye (in red) is most symmetrical vertically
- The top and bottom eyes (in blue) are not vertically symmetrical
  - The largest eye width ($EW_{largest}$) doesn't correspond to the largest eye height, where the eye width is EW
  - In this example, $EW_{largest}$ = EW = ~60% UI for the middle eye
  - $EW_{largest}$ is ~60% UI, while EW is ~48% UI for the top and bottom eye



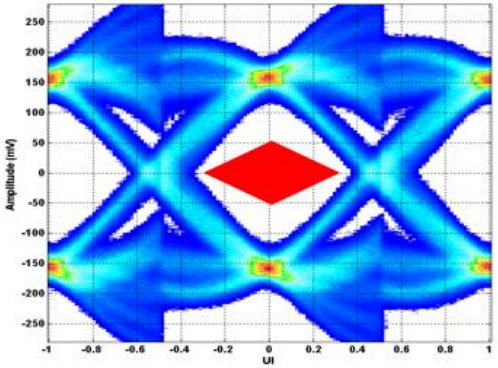


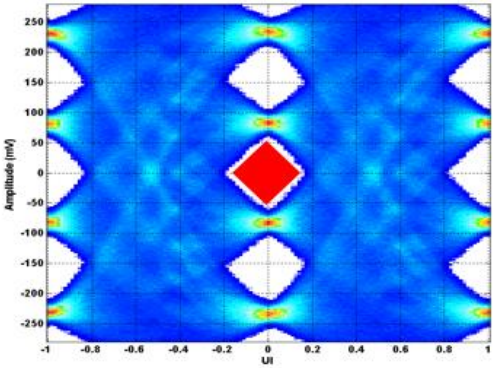
When PAM4 Might be More Advantageous



When PAM4 Might be More Advantageous (Con't)

Case 1

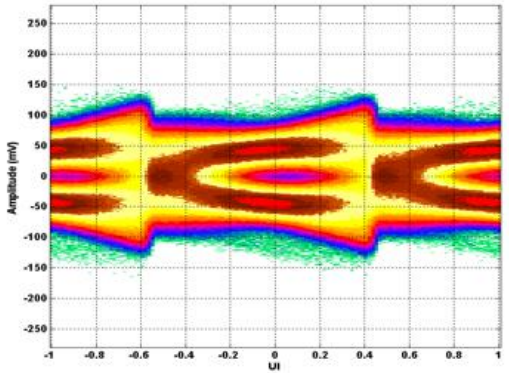


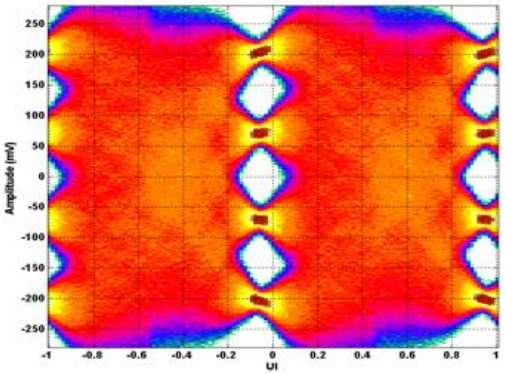


- 20dB for NRZ is reasonable
- The Δ is about 11dB
  - Clearly, the 9.5dB does not directly apply

Note: The two eye masks have the same height (in mV) and same width (in ps)

Case 2



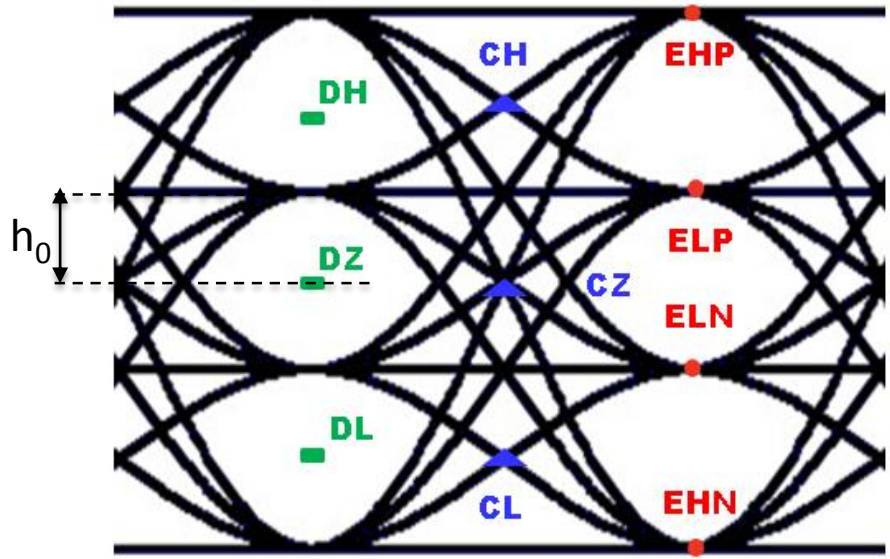


- 56dB is too much for PAM2
- Δ is more than 30dB
  - The suck-out does not affect PAM4 as much as affect PAM2

Note: eye masks are not listed since the PAM2 is totally closed

Suggested Latches/Slicers Naming Conventions

- The following naming conventions are suggested
  - "data latches" – **DH, DZ**, and **DL**
  - "error latches" – **EHP, ELP, ELN,** and **EHN**
  - "crossing latches" – **CH, CZ,** and **CL**
- If vertical symmetry is assumed
  - DL = -DH, EHN = -EHP, ELN = -ELP (= h_0)
- If linearity is assumed
  - DH = 2*ELP (= 2*h_0), EHP = 3*ELP (= 3*h_0)
  - DL = 2*ELN (= -2*h_0), EHN = 3*ELN (= -3*h_0)
- Nonlinearity effect
  - To assume EHP =3*h_0 and DH=2*h_0 , ELP=h_0 , etc. is not always a good practice
  - A good approach is to adapt them separately



Eye Diagram Anatomy

- NRZ only has 8 trace combinations for 3 consecutive bits
- PAM4 has 64 trace combinations for 3 consecutive symbols
- There are 6 combinations (40 unique traces) in PAM4 that are NRZ-like
  - The rest are much less well-behaved
  - Even the well-behaved traces form completely closed eyes

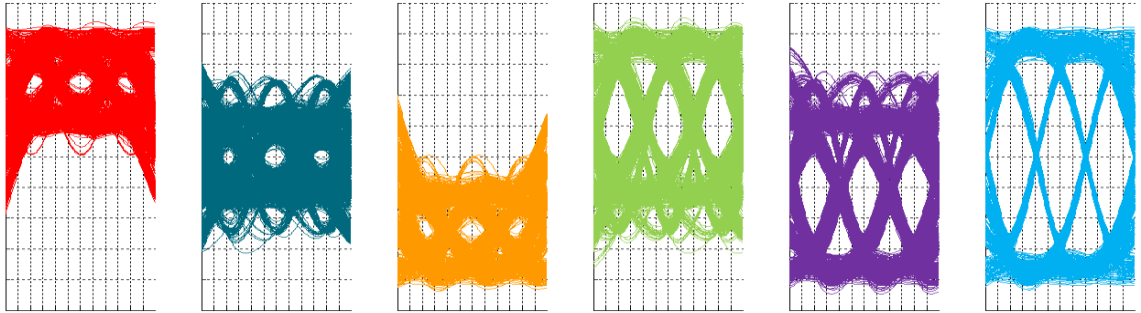
d_{k-1} d_k d_{k+1}

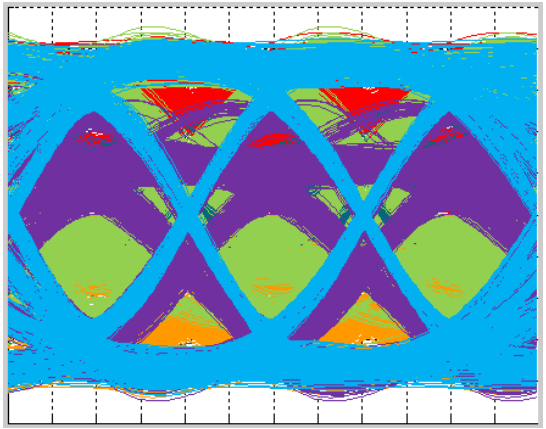
3 3

1 $\{3 \quad 1 \quad -1 \quad -3\}$ 1

-1 -1

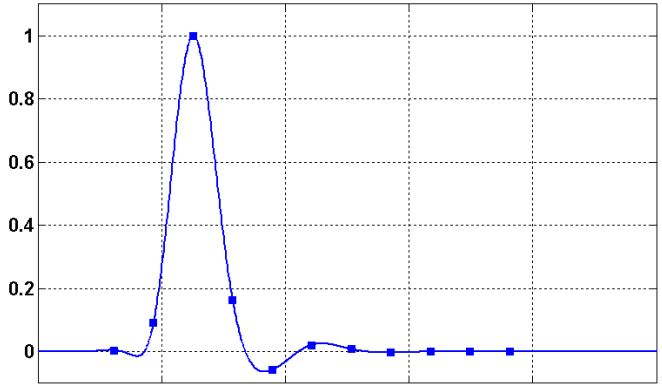
-3 -3

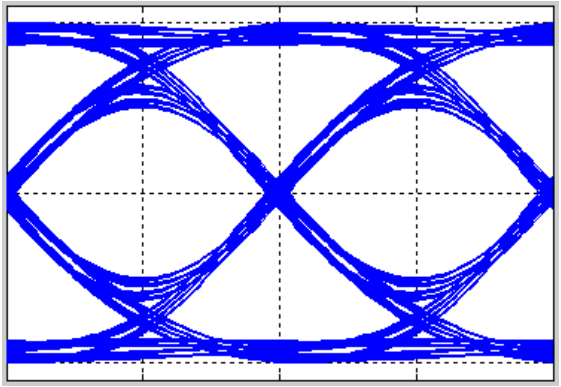


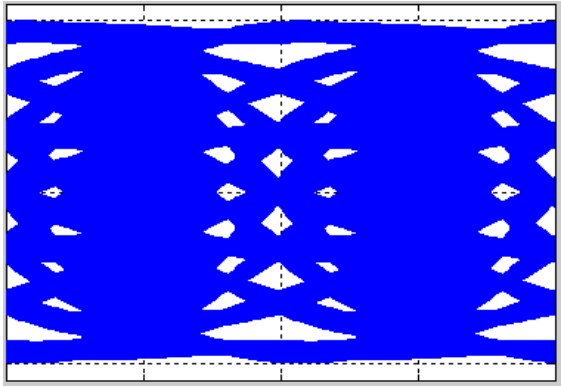


ISI Impact Example

- The combined channel has the single bit response with cursors marked
- A PAM2 and PAM4 coded pattern transmits through the channel
  - No equalization is applied
- The PAM2 eye is pretty open
- The PAM4 eye is completely closed

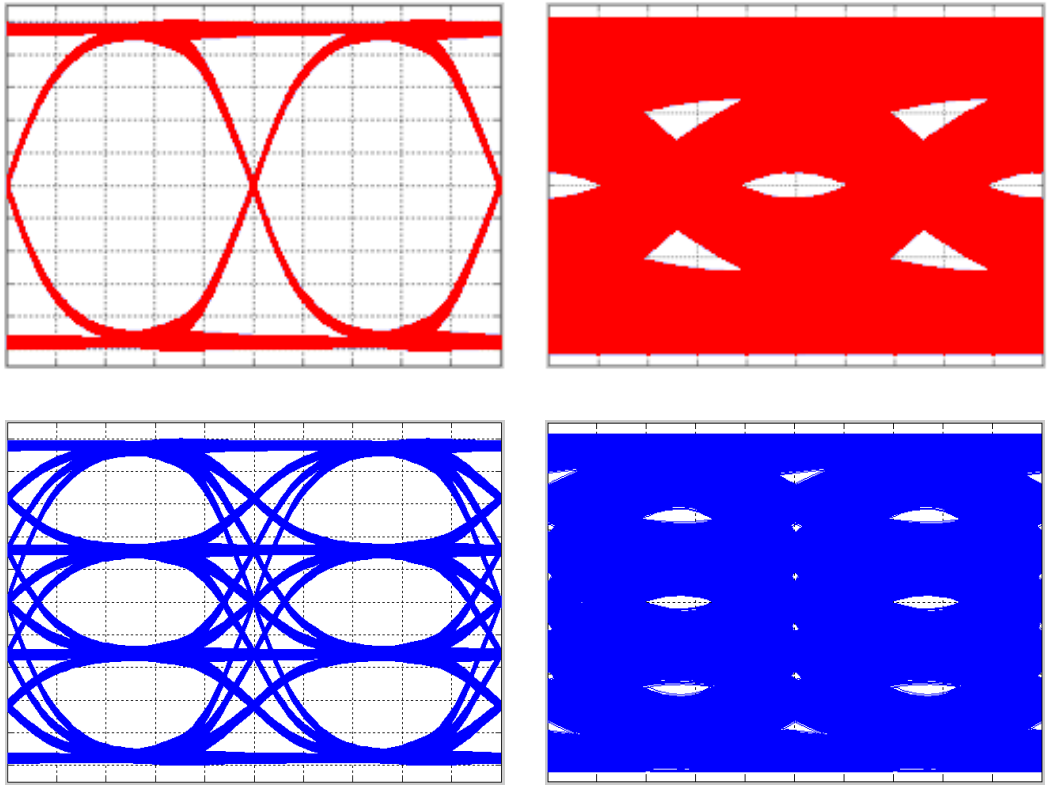






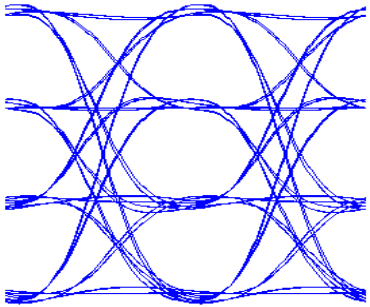
Rule of Thumb for Eye Closures

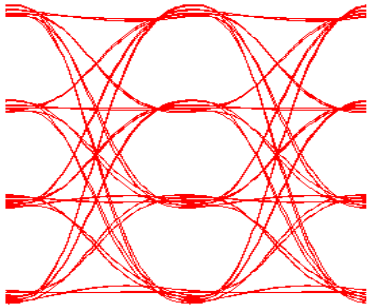
- With Reasonable TX design and package design, it is estimated that, absent of noise,
  - PAM2 eye starts to close at ~10dB
  - PAM4 eye starts to close at ~4.5dB
- In time domain, ISI should be controlled to be 1/3rd for PAM4 than for PAM2
- Channel loss profile also matters

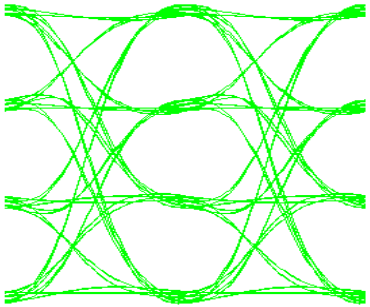


Clock Skew Impact on TX Output Eye

- If the PAM4 signaling is formed such that the MSB and LSB are summed up, clock skew could make the eye misaligned horizontally
- The signal quality will further deteriorate after a channel
- An example is given for clock skew between MSB and LSB
  - Case 1: MSB is early w.r.t. LSB by 1/8th UI (blue)
  - Case 2: There is no skew between MSB and LSB (red)
  - Case 3: MSB is late w.r.t. LSB by 1/8th UI (green)

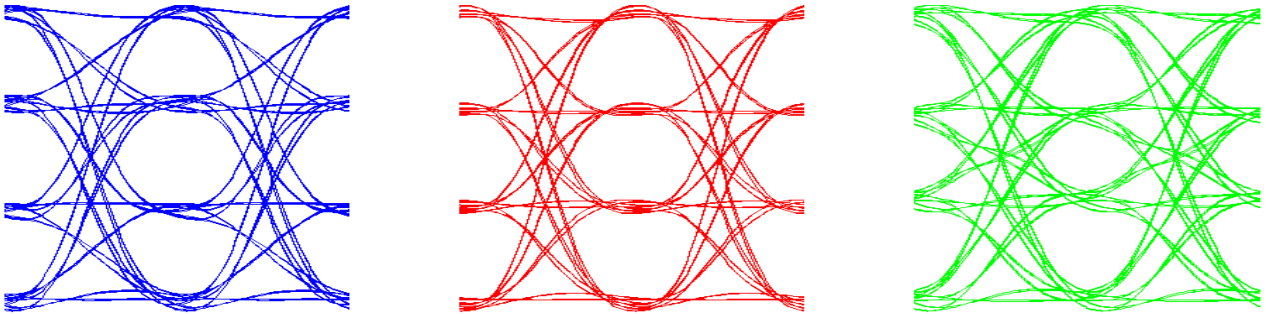






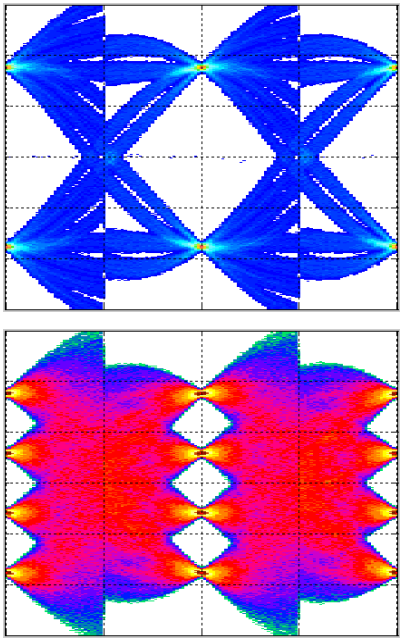
TX Driver Strength Impact on TX Output Eye

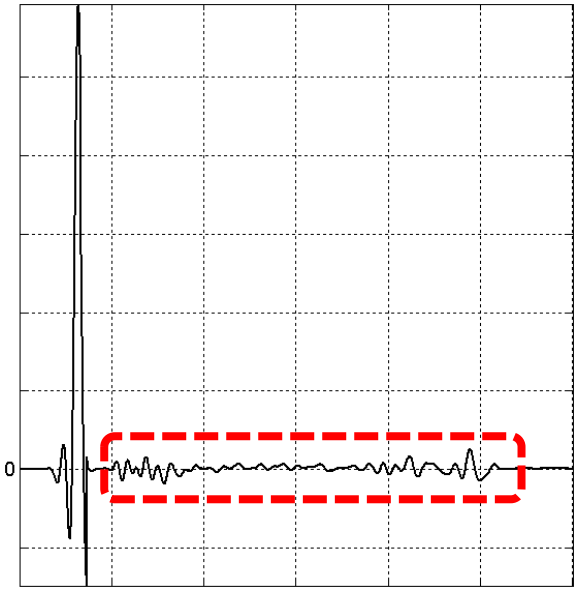
- If the PAM4 signaling is formed such that the MSB and LSB are summed up, driver mismatch could make the eye misaligned vertically
- The signal quality will further deteriorate after a channel
- An example is given for different driver rise/fall times
  - Case 1: MSB driver has faster rise/fall times (blue)
  - Case 2: MSB and LSB drivers are matched (red)
  - Case 3: MSB driver has slower rise/fall times (green)

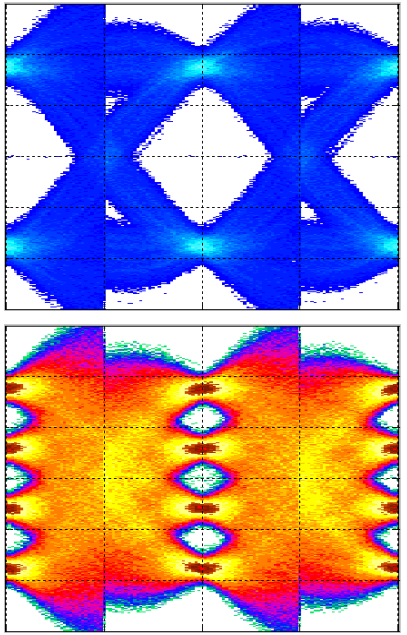


Reflection Impact on PAM4 Signal

- The impact of reflections on PAM4 could be 3x worse in magnitude than on PAM2
  - The LHS eyes are constructed without considering the reflections circled in red
  - The RHS eyes are simulated with all the reflections – PAM4 degrades much faster

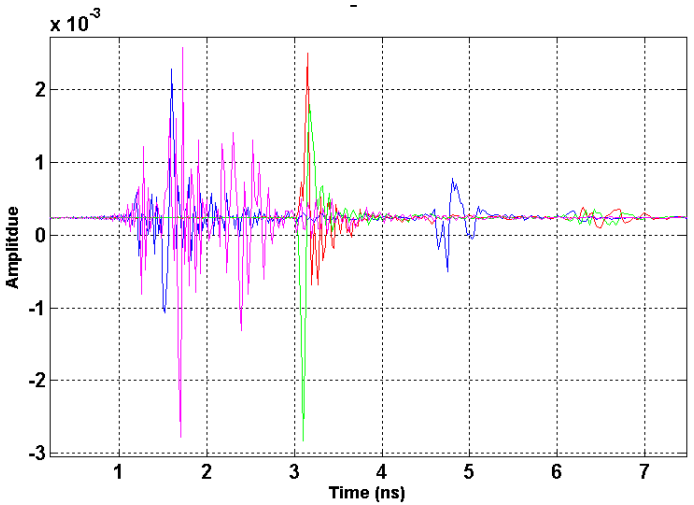


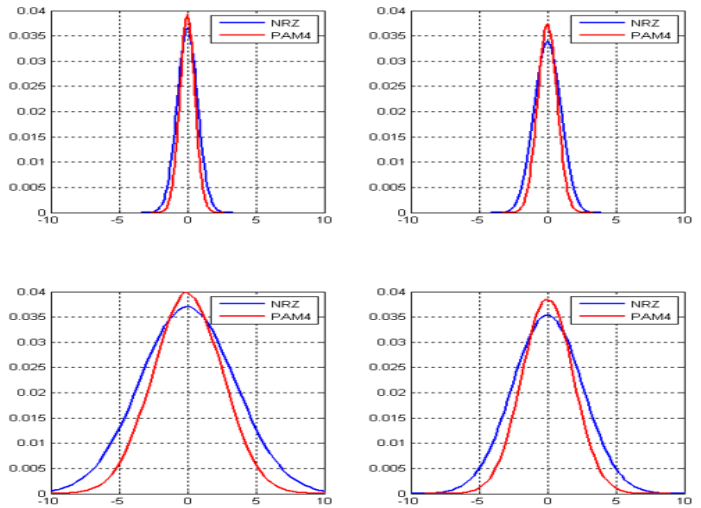




Crosstalk Impact on PAM4 Signal

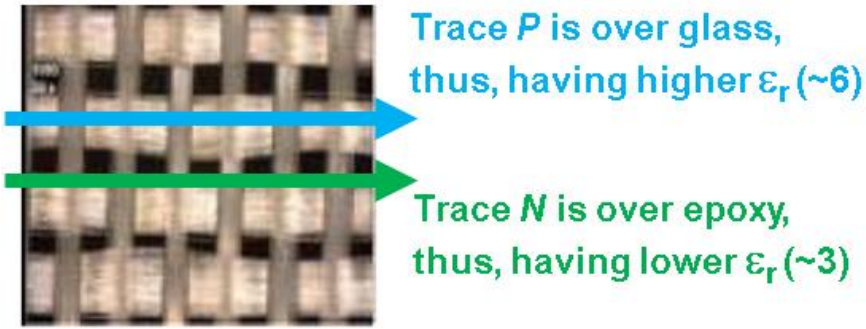
- Crosstalk noise hurts link margin more with the peak-peak value, rather than the RMS value
- When aggressor number is > 3, the crosstalk noise is approaching bounded Gaussian, with peak-peak/RMS up to 11 based on empirical data
- PAM4 aggressors tend to have slightly smaller RMS, but similar peak-peak as for PAM2
- The impact of crosstalk noise on PAM4 signaling is approximately 3x worse than that on PAM2

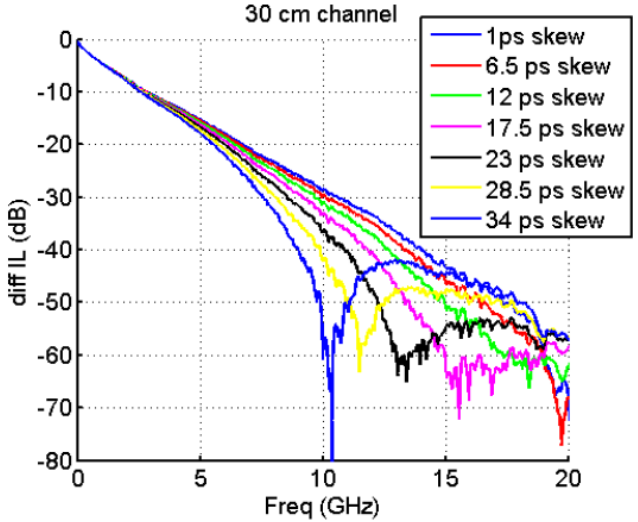




Intra-pair Skew Impact on PAM4 Signal

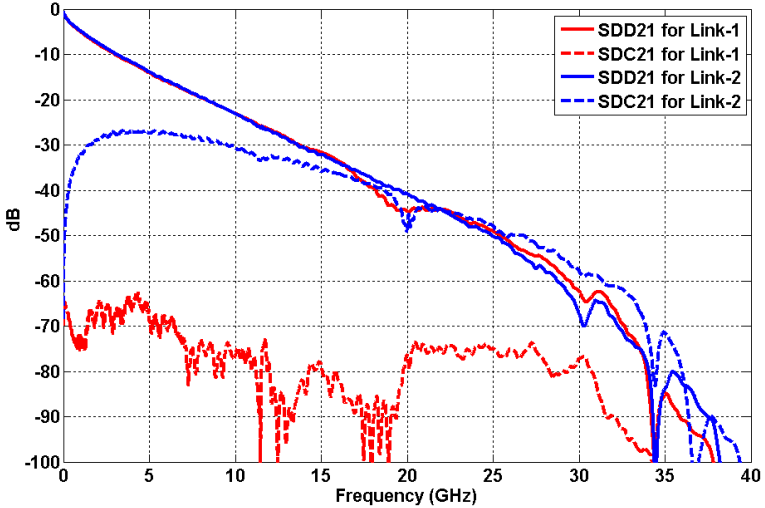
- Intra-pair skew can be due to various sources
  - Different routing lengths, connector fan out, fiber weave effect, etc.
- Intra-pair skew tends to impacts PAM4 much more than PAM2, for the same baud-rate
- In addition to extra loss, mode conversion also needs to be taken into account
  - An example on mode conversion on next page



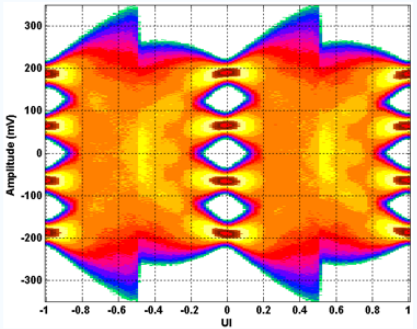


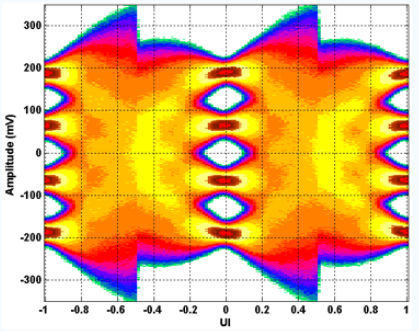
Mode Conversion Impact Example

- Link-1 has 0 ps skew, while Link-2 has 15 ps skew between P&N
- SDC increased by more than 30dB for the skewed pair
- If simulation had SDC21 ignored, the system performance would be optimistic



Link-2 SDC21 is not considered	Link-2 SDC21 is included
MSE based BER ~ 1.3e-9	MSE based BER ~ 5.4e-8

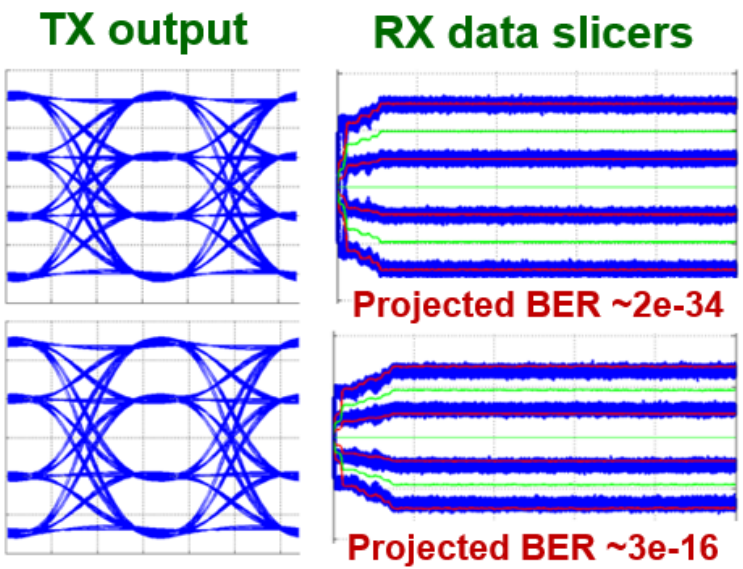




Nonlinearity Impact on PAM4 Signal

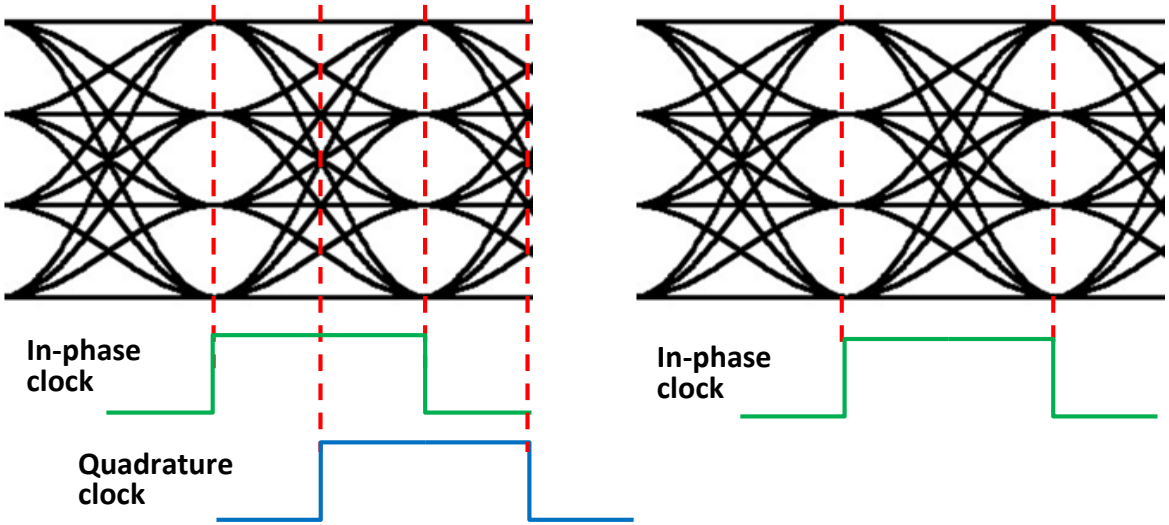
- PAM4 has three vertical eyes, but system margin bottleneck lies with the worst eye
- Nonlinearity plays a much bigger role in PAM4 than in NRZ
- Nonlinearity starts right at TX output (see R_{LM})
- Each active block could add more nonlinearity
- The larger the signal, the more nonlinearity
  - PAM4 needs more dynamic range
  - DFE assumes linear system to work optimally
  - If ADC is used, the full-scale range applies
- Adopting nonsymmetrical data and error slicers can help, but only to a certain extent

(More on nonlinearity later)



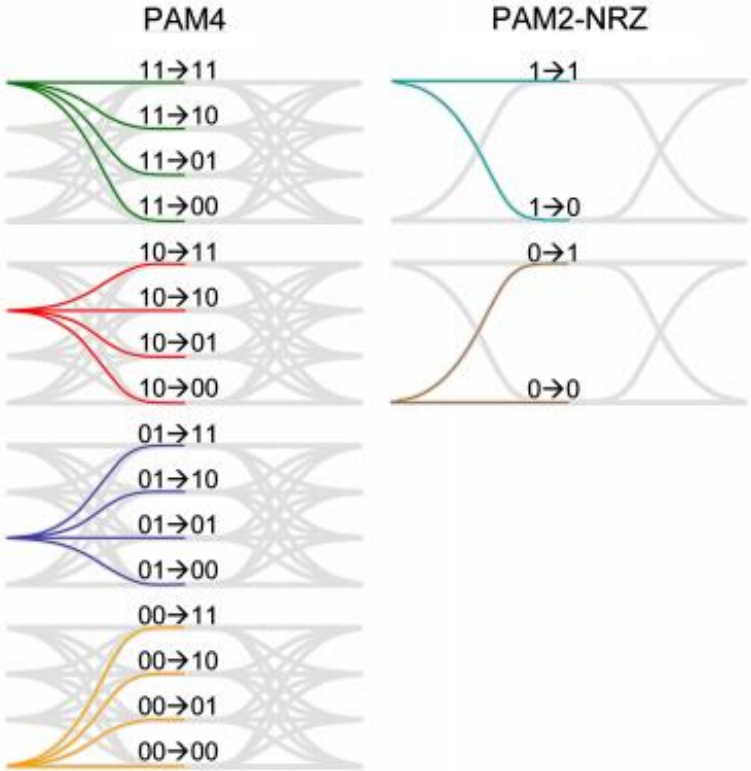
2x Oversampling Vs. Baud-Rate CDR

- Compared with the commonly used 2x oversampling Bang-Bang CDR, baud-rate CDR does not guarantee the sampling phase around the center of the symbol
- Baud rate CDR has less power consumption due to only one phase clock needed vs. two phase clocks for 2x oversampled CDR



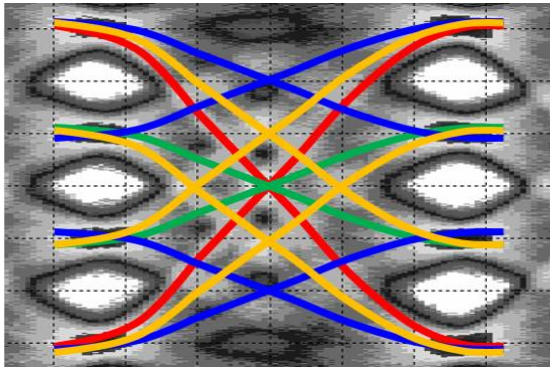
PAM4 Time Recovery – Transition Density

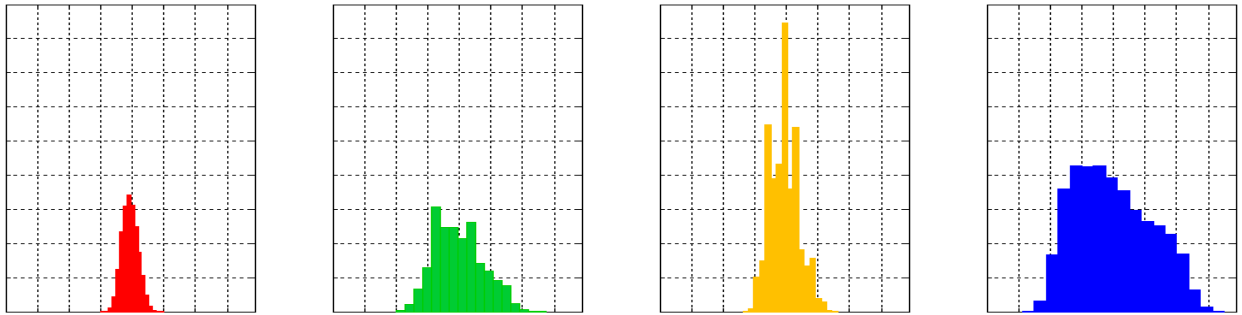
- Transition Density (TD) is illustrated for linear coding
  - 16 traces between 2 symbols
  - 4 are between the same levels
  - 16 - 4 = 12 are level transitions
  - Average TD = 75% (=12/16)
- For PAM2, the average TD is 50%



PAM4 Time Recovery – Selected Crossings

- The narrower the distribution, the less the timing jitter
  - The major transition (red) has the tightest distribution
  - +3 ↔ +1 and -3 ↔ -1 depends on timing slicer level placement
- One can conditionally select transitions for timing recovery
  - This will reduce TD, thus affecting CDR bandwidth

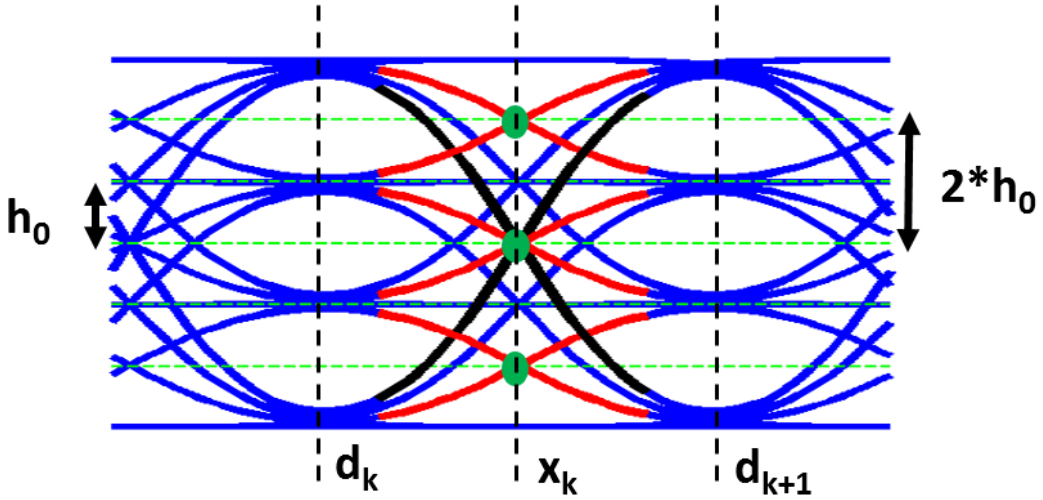




2x Oversampled Timing Recovery Example

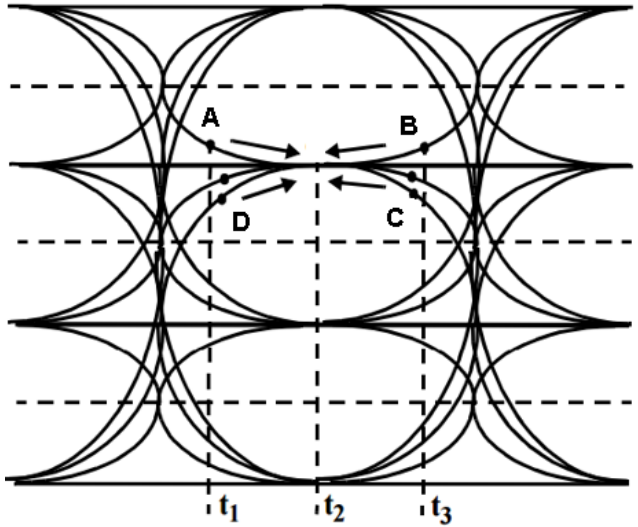
- The transitions between level 3 and level 2 has the following logic

```
if  d(k)>2*h0 && d(k+1)>0 && d(k+1)<2*h0
    if x(k)>2*h0, CDR too early
    else if x(k)<2*h0, CDR too late
    endif
endif
```



MMSE Baud-Rate CDR

- MMSE timing recovery optimizes the sampling phase by minimizing the expected value of the squared error
- Practical high-speed adaptation algorithms often use only 1-bit representations of the sign of the error and the gradient signals, the Sign-Sign MMSE, or SSMMSE



Sampling	Error	Slope	Decision
A	1	-1	Early
B	1	1	Late
C	-1	-1	Late
D	-1	1	Early

Mueller-Muller (MM) Baud-Rate CDR

- The purpose of MM timing recovery is to infer the channel response from baud-rate samples of the received data and then to align the sampling clock so that the precursor ISI equals the post-cursor ISI

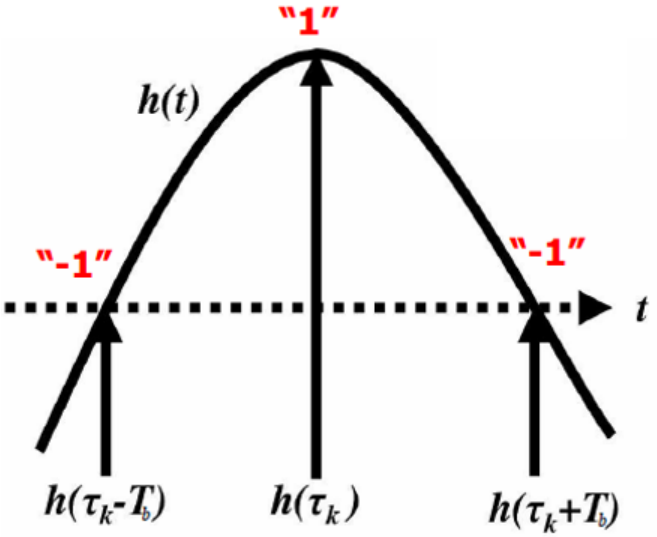
- CDR phase updating is based on

if $h(t_k - T_b) < h(t_k + T_b)$

CDR is too early

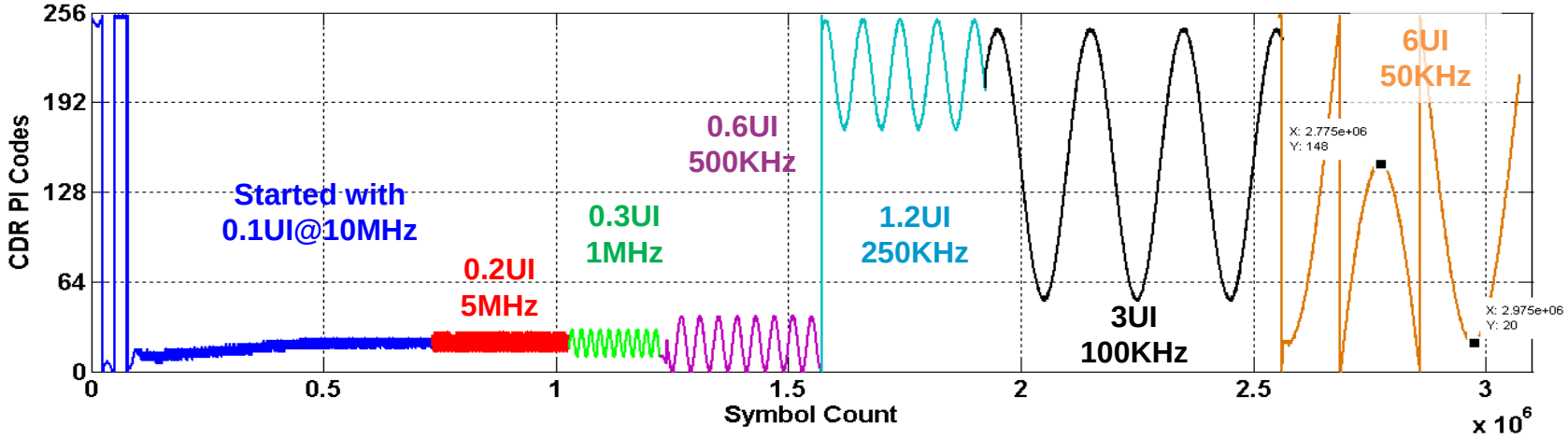
else if $h(t_k - T_b) > h(t_k + T_b)$

CDR is too late



MM Baud-Rate CDR Tracking Example

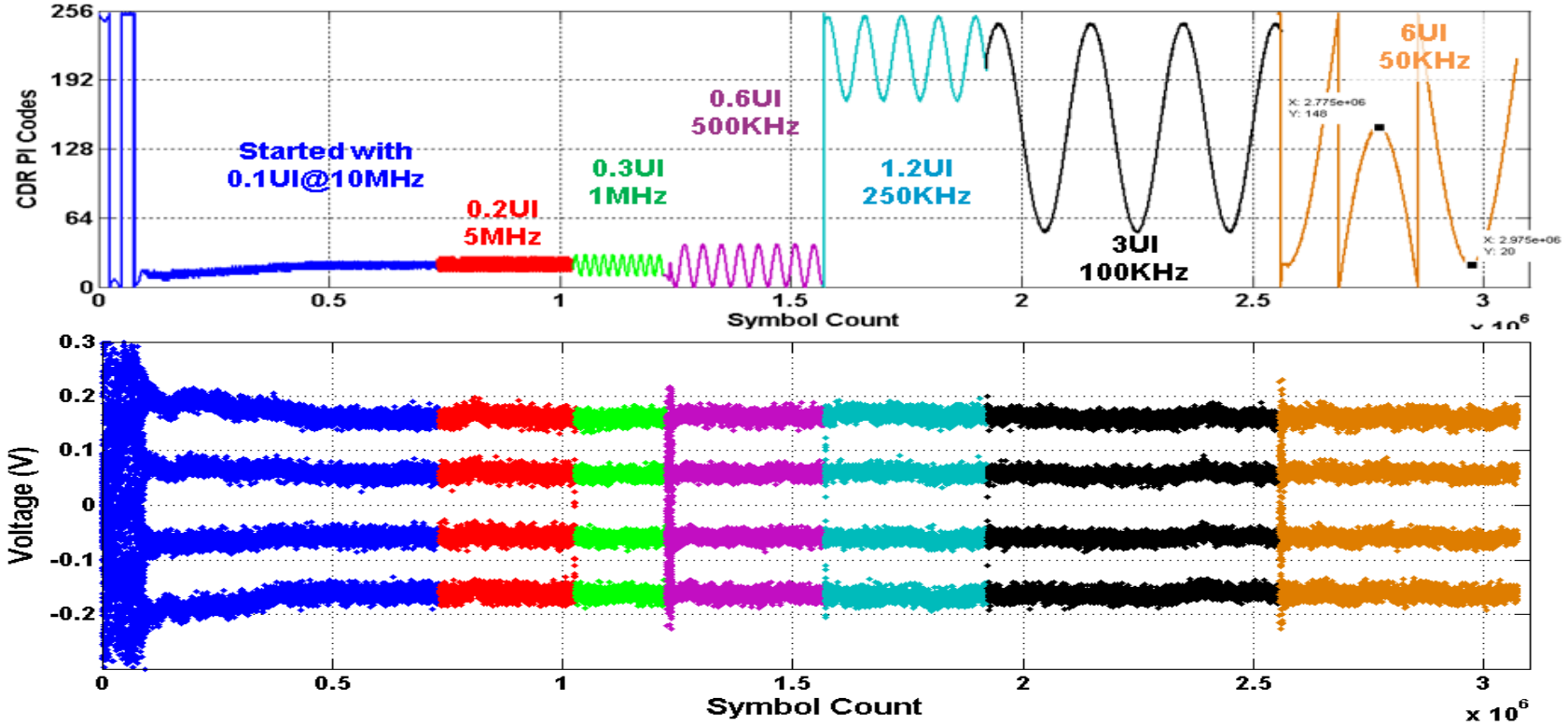
- For an MR channel at 40Gbps, in a quarter-rate clocking system, with 64 codes/symbol
- Single tone SJ, amplitude and frequency, was altered dynamically during simulations



- For the last SJ, we only see settled half a cycle: the duration, each UI=50ps, is (2.975M-2.775M)*50ps = 10µs. So a full cycle is 20µs, or 50KHz
- The first mark is up by 148, and the second down by 256-20=236. So the total swing is 148+236=384, or 389/64 = 6UI

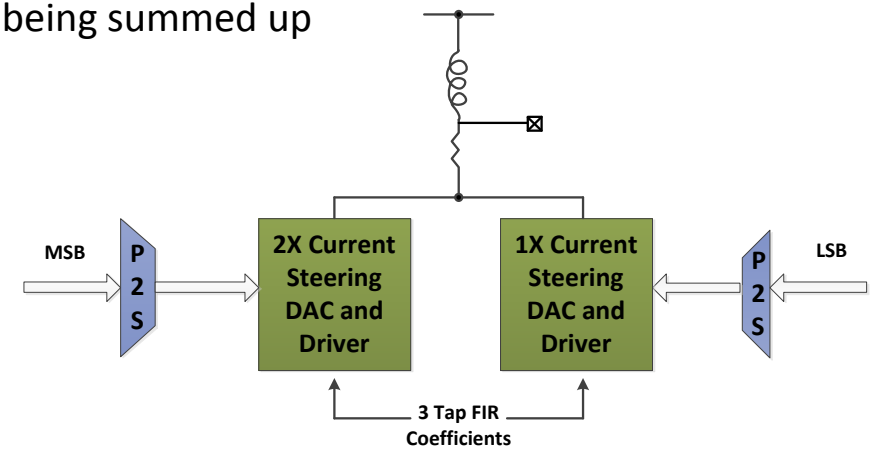
MM Baud-Rate CDR Tracking Example – Con't

- To assure that the CDR is indeed in tracking, the sampled eyes are plotted



TX FIR Implementation Example

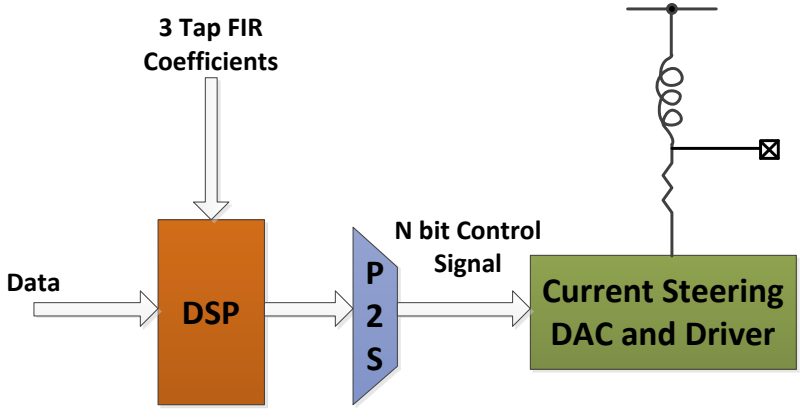
- MSB and LSB are filtered separately, before being summed up



$$d'_{LSB}(k) = -c(1)*d_{LSB}(k+1) + c(0)*d_{LSB}(k) - c(-1)*d_{LSB}(k-1)$$

$$d'_{MSB}(k) = -c(1)*d_{MSB}(k+1) + c(0)*d_{MSB}(k) - c(-1)*d_{MSB}(k-1)$$

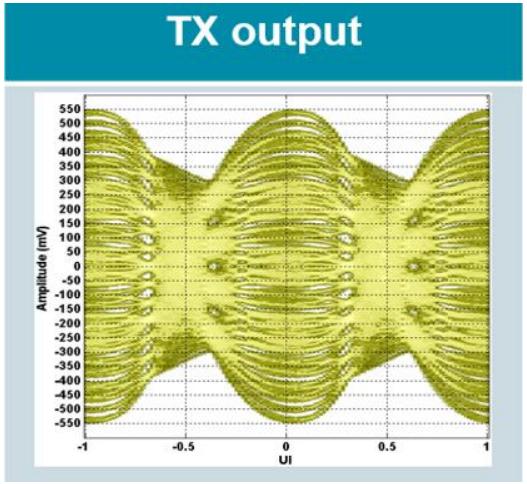
- MSB and LSB are coded and mapped to PAM4 levels first before passing through the FIR filter



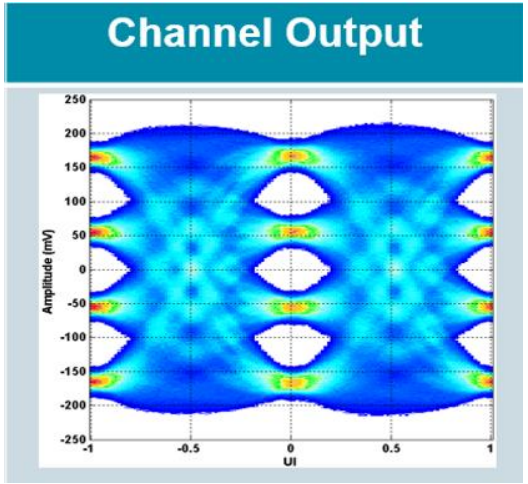
$$d_{PAM4}(k) = -c(1)*d'(k+1) + c(0)*d'(k) - c(-1)*d'(k-1)$$

Transmitter De-Emphasis Example

- Typically, a 3-tap FIR (pre + main + post) TX de-emphasis is used
- 3-tap FIR results in 4^3 = 64 possible distinct signal levels
- An example for a 10dB link
  - {C(-1), C(0), C(1)} = {-0.1, 0.675, -0.225}
  - The TX output eye is totally distorted, while the eye after the channel is open

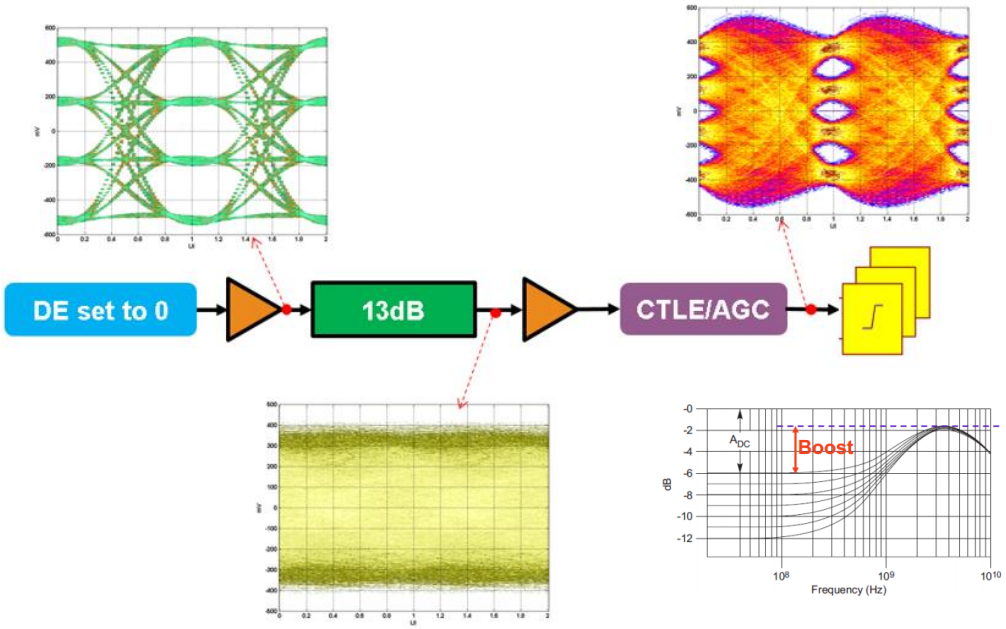


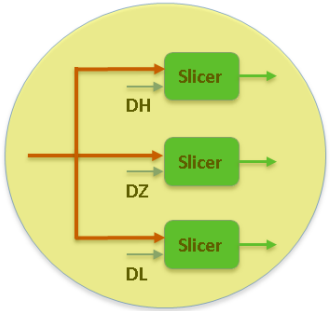
Channel



Channel Equalization with CTLE Example

- The CTLE works the same for PAM4 as for NRZ signaling
- The CTLE is usually followed and/or preceded by AGC



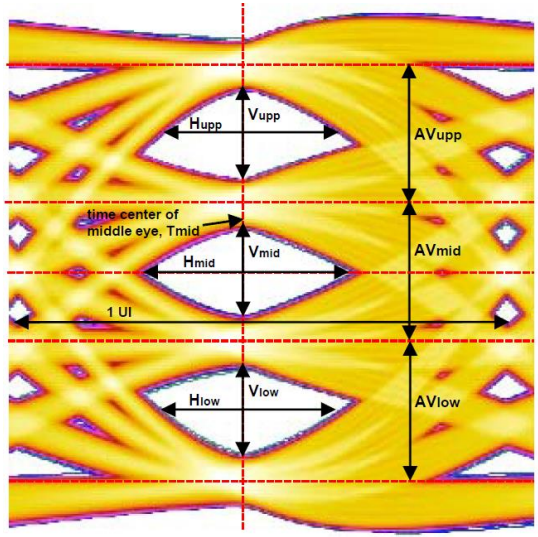


EH6 and EW6

- Since PAM4 is essentially a non-error-free system, eye metrics are defined in the VSR sped at BER = 1e-6
  - EH6 is the vertical distance across the BER = 1e-6 contour
  - EW6 is the horizontal distance across the BER = 1e-6 contour
- Vertical Eye Closure (VEC)

$$VEC = 20 \cdot LOG\left(Min\left(\left(\frac{AVupp}{Vupp}\right), \left(\frac{AVmid}{Vmid}\right), \left(\frac{AVlow}{Vlow}\right)\right)\right)$$

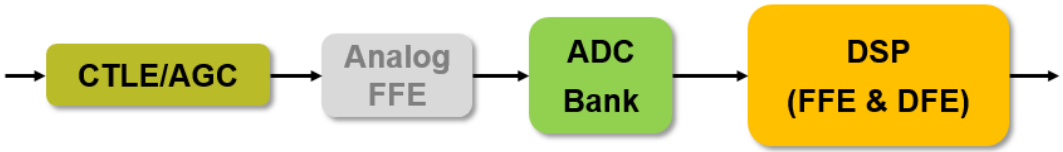
- To support raw BER<1e-6, instead of raw BER<-15
  - The BER is still dominantly affected by deterministic jitter and noise
  - May require redefining link budget to make trade-offs between performance, power consumption, and implementation cost



Analog- vs. Digital- Based Receiver

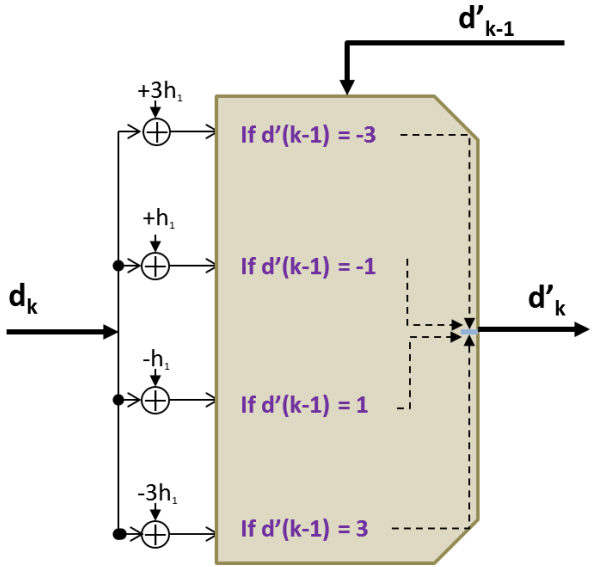
- A lot of experience and circuits can be leveraged from decades' design of NRZ receivers
  - Power is still an advantage over digital-based receiver architecture
  - As link margin gets smaller, each block needs to be fine-tuned

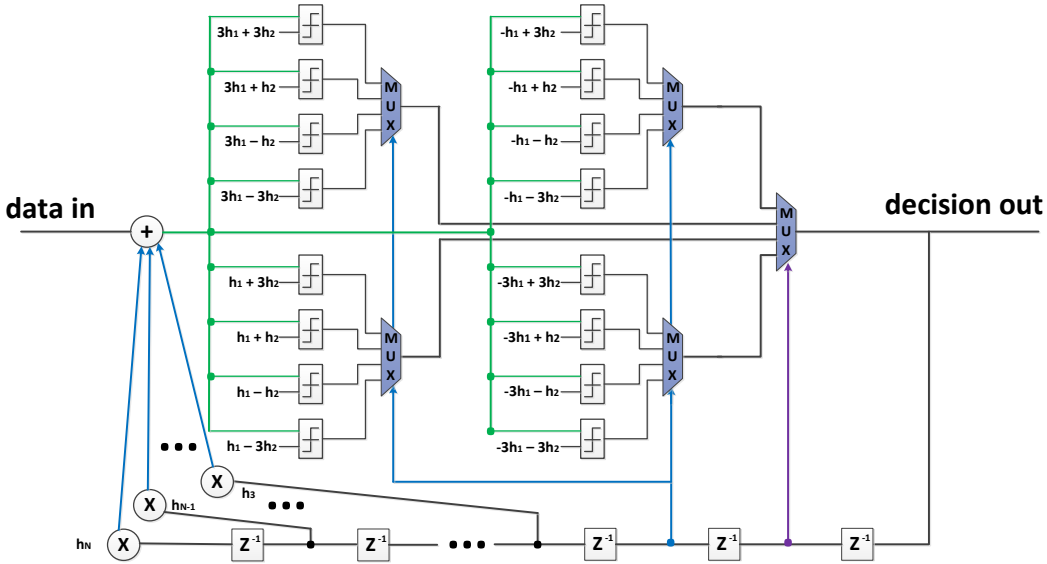
- A common trend has been the increasing use of DSP
  - Benefits: greater flexibility and more powerful signal processing techniques
  - Challenges: architecture complexity and large power dissipation



Tap-Unrolling DFE Example

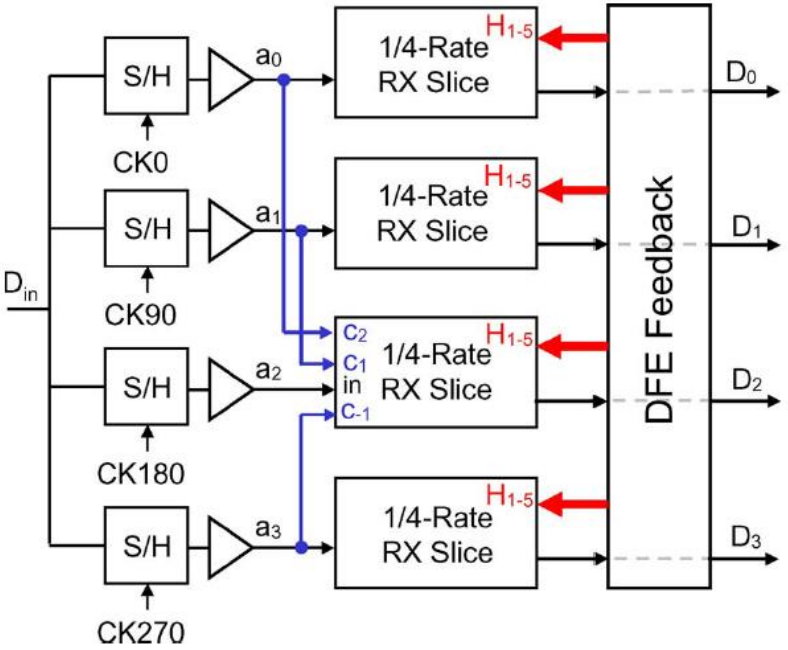
- 4 data slicers are needed for one symbol tap DFE unrolling in full-rate clocking mode
  - For half-rate clocking mode 8 data slicers are required
- For two symbol tap unrolling DFE, the illustration requires 4^2 = 16 slicers is for the full-rate clock scheme, and 32 slicers for the half-rate clocking scheme





FFE+DFE Example in Analog Receiver

- A simplified block diagram of a 4-tap FFE and 5-tap DFE is shown
  - The data path includes a bank of 4 S/H, source follower buffers to drive the sampled data to four parallel RX slices, and DFE feedback logic
  - A quarter-rate architecture is chosen for the receiver to establish data signals for a 4-tap FFE
- Analog FFE can also be implemented using delay lines



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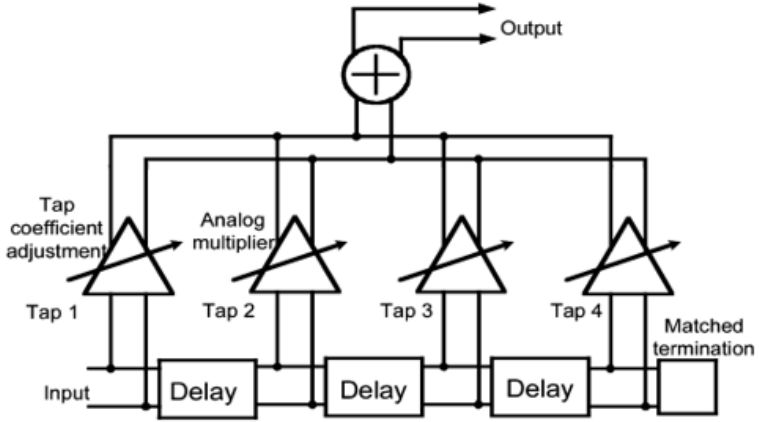
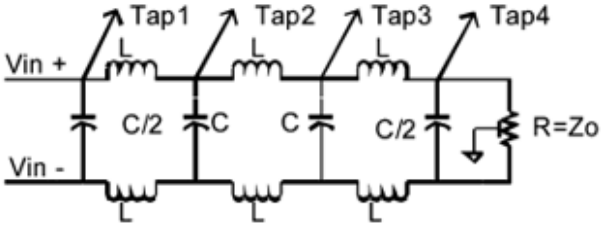
A 19-Gb/s Serial Link Receiver With Both 4-Tap FFE and 5-Tap DFE Functions in 45-nm SOI CMOS

Ankur Agrawal, *Member, IEEE*, John F. Bulzacchelli, *Member, IEEE*, Timothy O. Dickson, *Member, IEEE*, Yong Liu, *Member, IEEE*, Jose A. Tierno, *Member, IEEE*, and Daniel J. Friedman, *Member, IEEE*

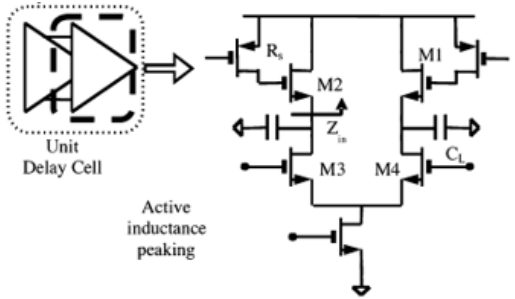
Analog FFE based on Delay Line Design Example



Passive delay element

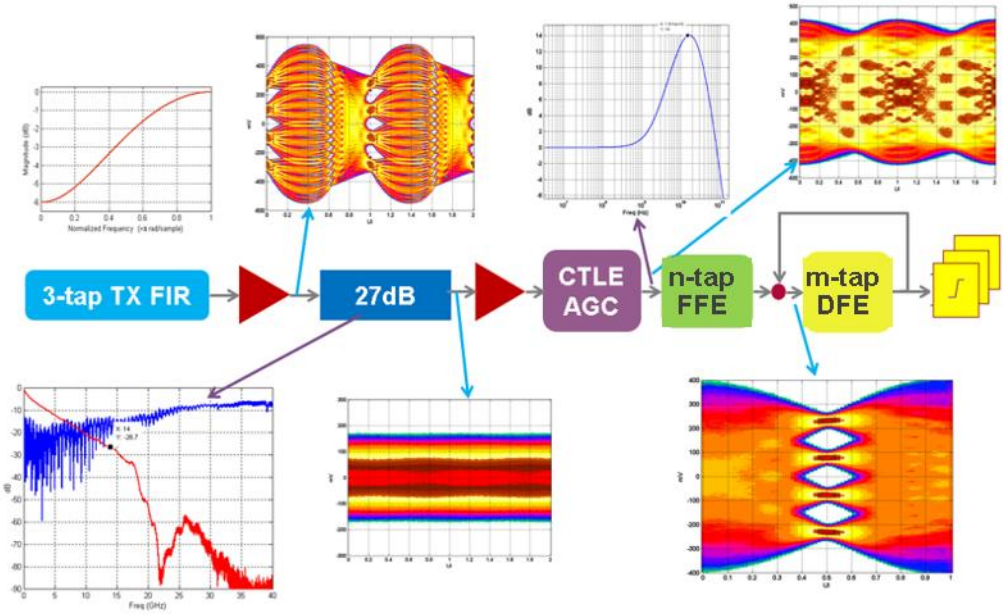


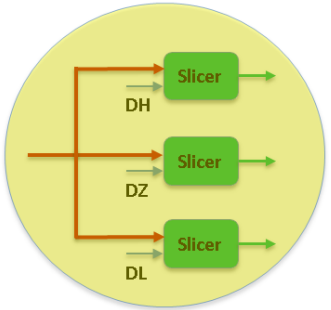
Active delay element



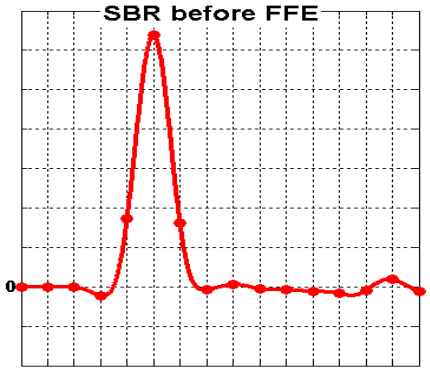
Analog-based Equalization

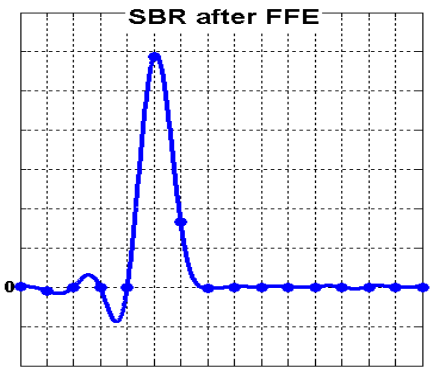
- Besides TX FIR, the RX side usually contains CTLE/AGC and DFE
- Analog FFE is also a choice targeting channels beyond VSR
- An example is illustrated with eyes at different nodes

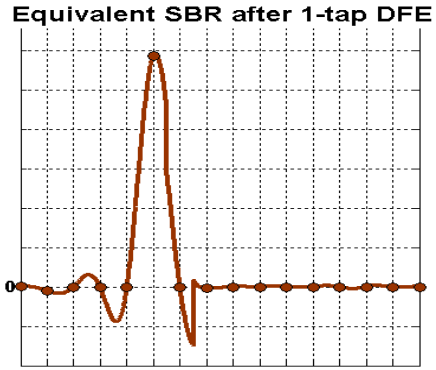


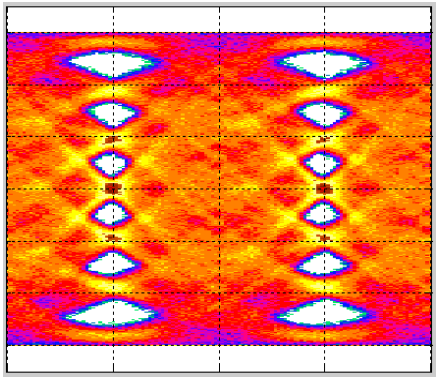


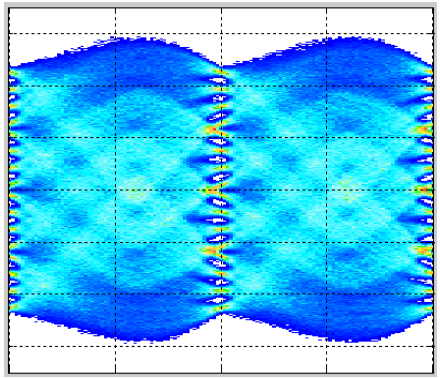
A 20-tap FFE and 1-tap DFE Example

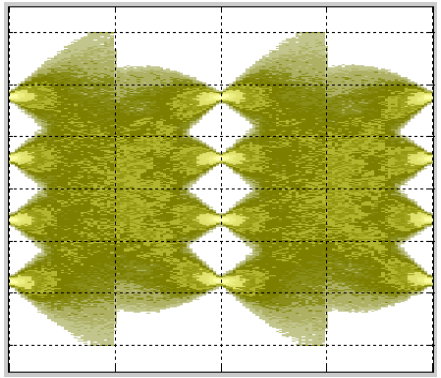






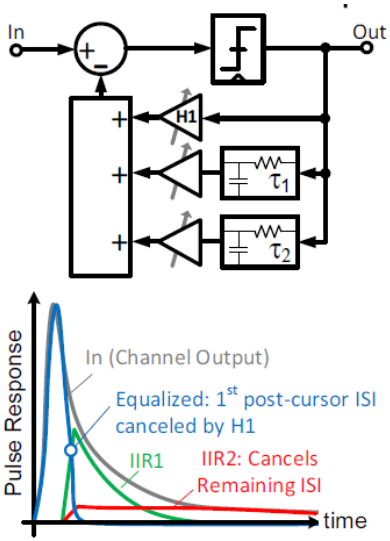


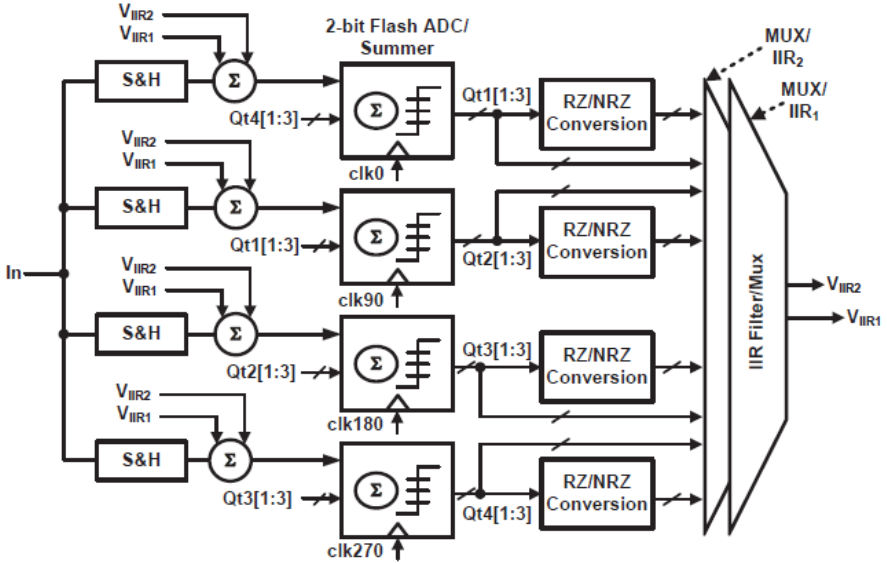




Infinite Impulse Response (IIR) for DFE

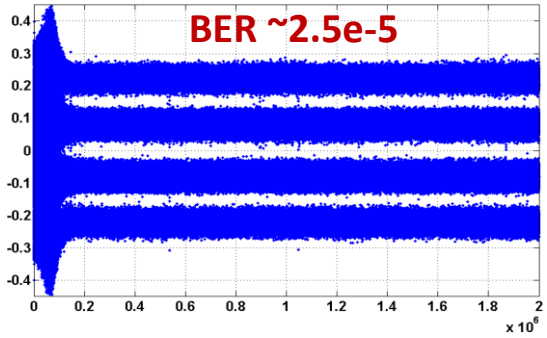
- DFE with the addition of IIR filtering can efficiently cancel many post-cursor ISI terms
  - The CTLE with well placed poles and zeros (low to mid frequency peaking) can mitigate long-tail ISI. However, it may also amplify noise and crosstalk
  - The FIR tap DFE can also do the job but may need many taps, thus increasing implementation complexity and SerDes power consumption

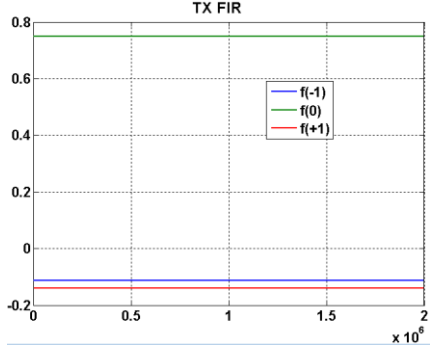


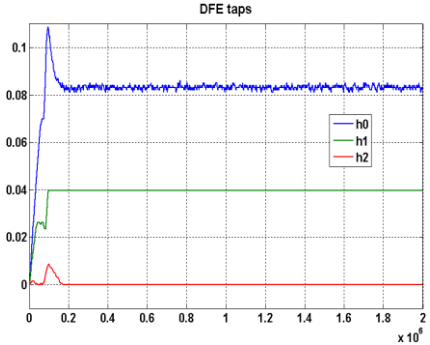


TX IIR for a 25dB Channel Example

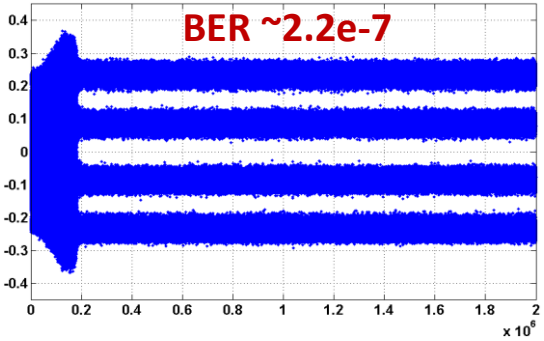
- 3-tap TX FIR + RX CTLE + 2-tap DFE

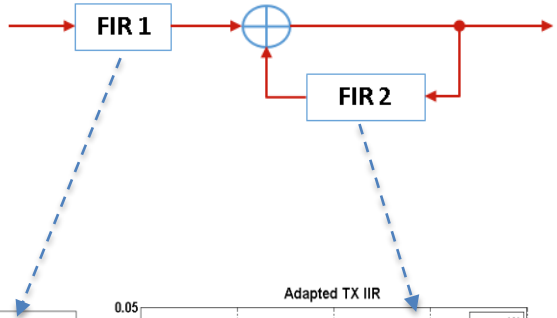


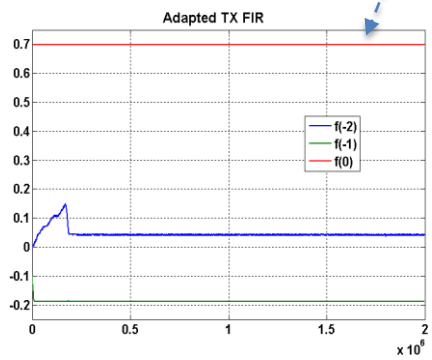


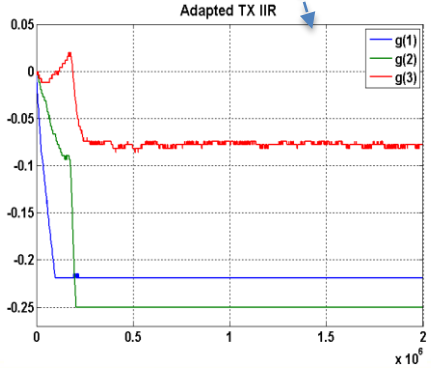


- 3-tap TX FIR + 3-tap TX IIR + RX CTLE



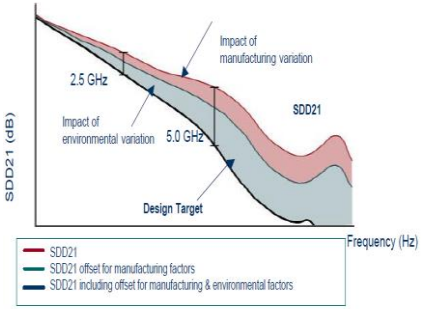




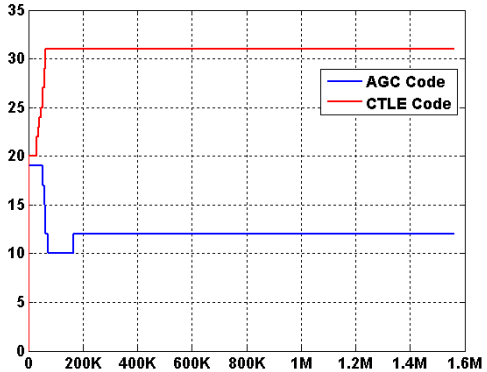


Necessity for Equalizer Adaptations

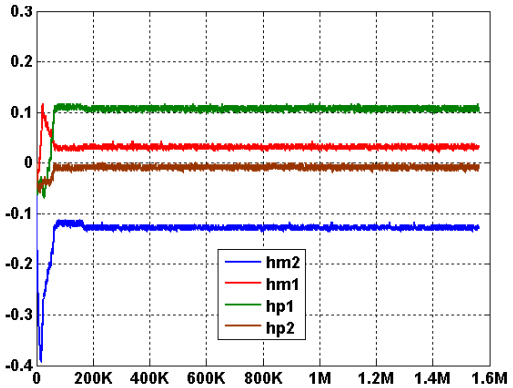
- Equalizer adaptation is important
  - It relieves the burden of relying on manually searching for optimal settings
  - For complicated equalizers it is impossible to tune the parameters manually
  - Most valuably, adaptation can compensate for link characteristic change due to environmental impact, such as temperature



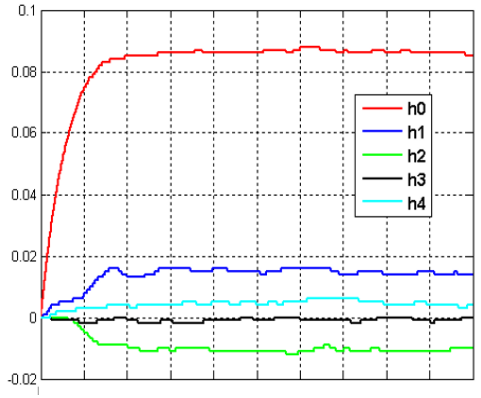
AGC and CTLE convergence



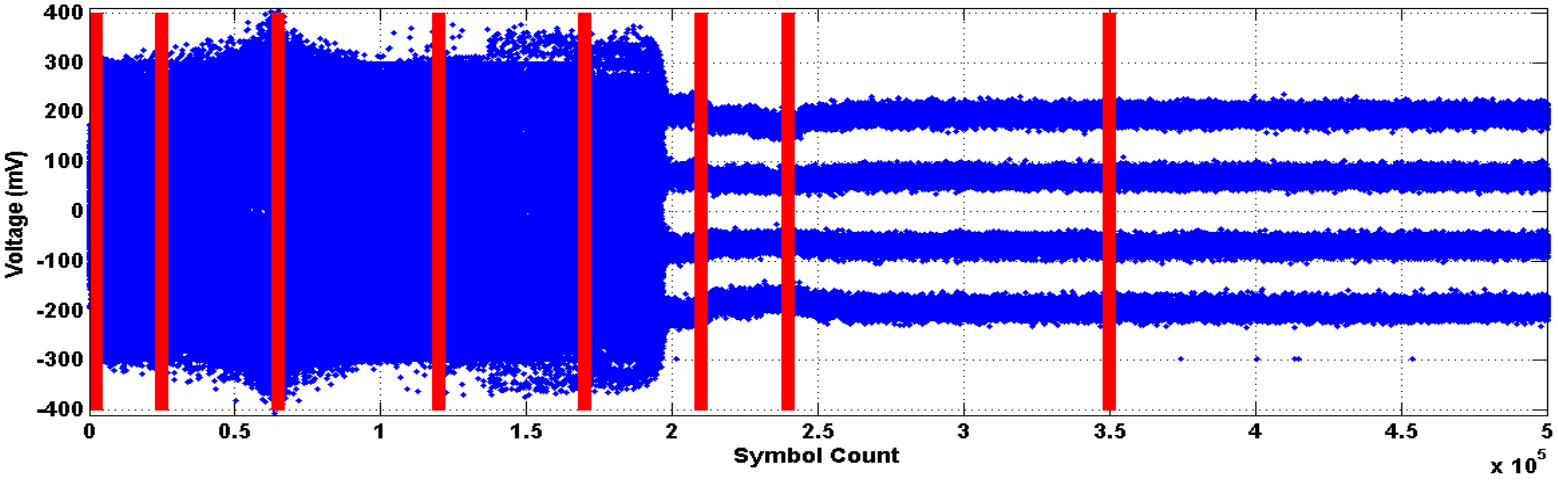
5-tap FFE coefficient convergence

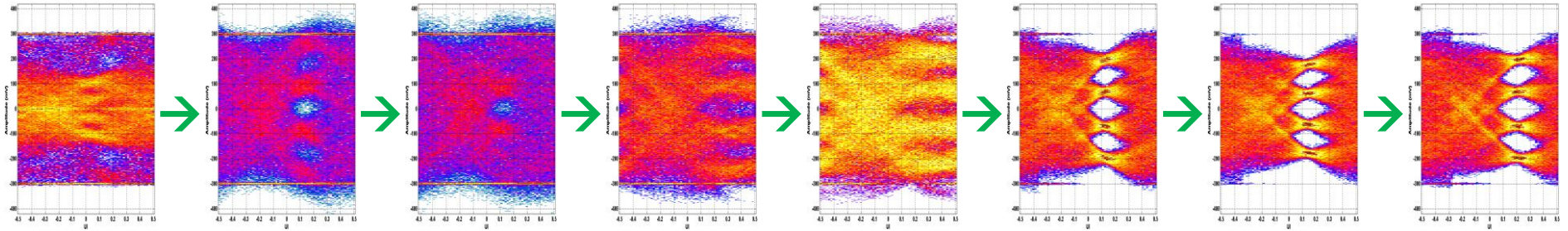


5-tap DFE coefficient convergence



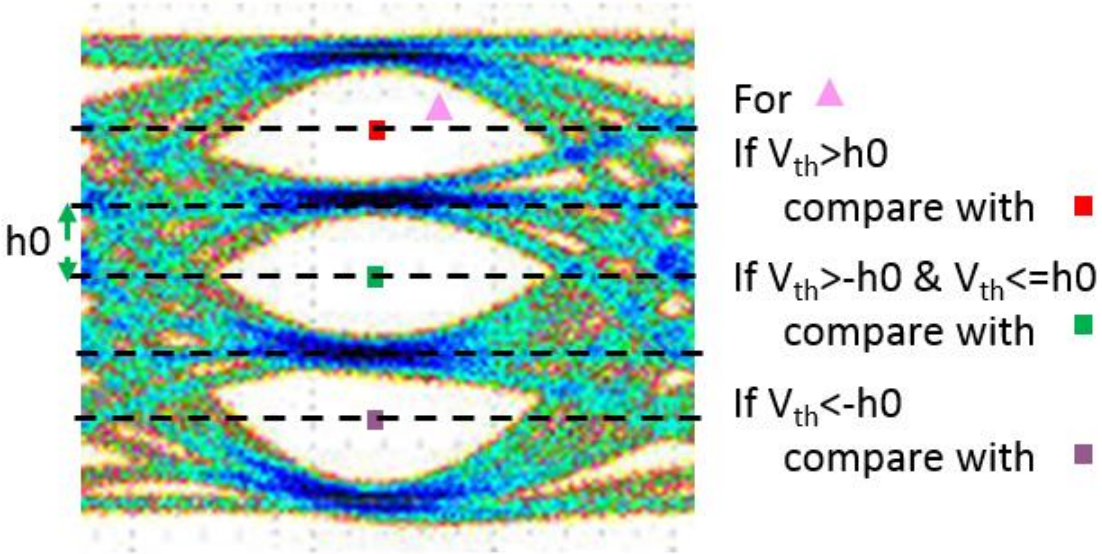
Visualization of Eye Convergence

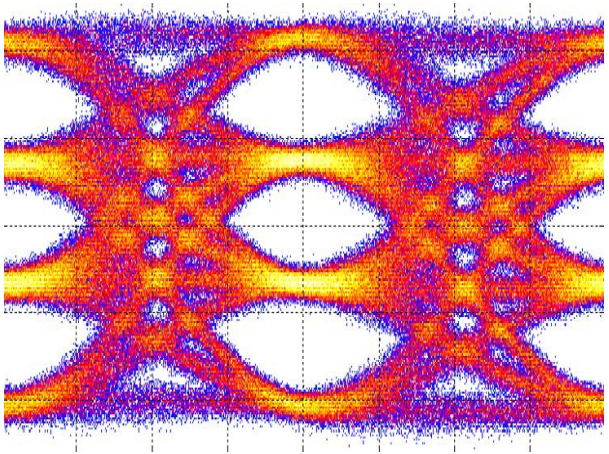




On-Die Eye Monitors

- For analog-based receiver, the familiar eye monitor (a.k.a., eye scope, eye scan, etc.) concept still applies
- An example is given below

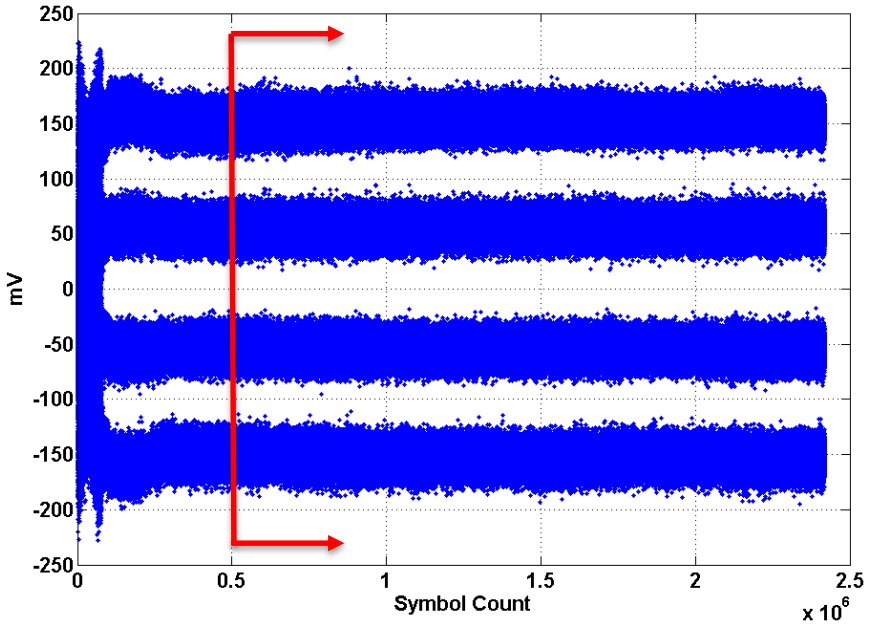


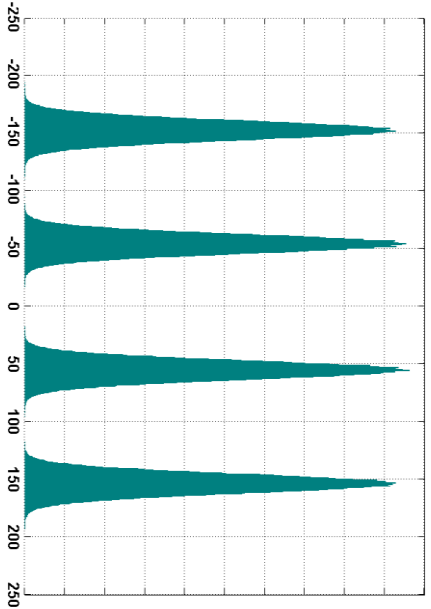


On-die captured eye

Sampled Eyes

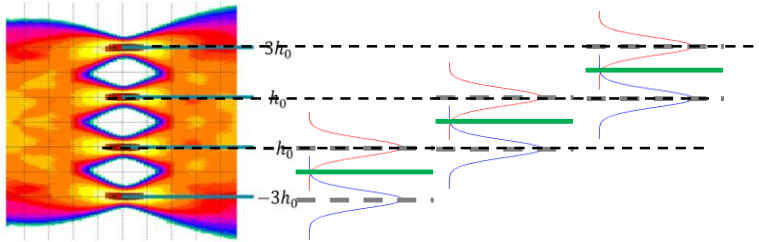
- For ADC-based architecture, with reasonable amount of power and area, only one sample per symbol is available. Thus, we can only get the so-called sampled eye





SER and BER Calculations

- For PAM4 (M=4) BER calculations, assuming that all M symbols are equiprobable, SER (symbol error ratio) becomes



$$\mathrm{SER} = \frac{1}{M}\sum_{i=0}^{M-1}\sum_{j=0,j\neq i}^{M-1} P_{ij}$$

P_{ij} is the probability of receiving symbol j when symbol i was transmitted.

- The BER is dependent on the coding scheme of the symbols, where the d_{ij} is the Hamming distance between the labels of symbols i and j .
  - The BER can be approximated as

$$\mathrm{BER} = \frac{1}{M}\sum_{i=0}^{M-1}\sum_{j=0,j\neq i}^{M-1} \frac{d_{ij}}{\log_2(M)} P_{ij}$$

$$\mathrm{BER}_{\mathrm{approx}} \approx d_{\mathrm{avg}} \frac{\mathrm{SER}}{\log_2(M)}$$

Avg Hamming Distance	Gray Coding	Linear Coding
d_{avg}	1	$2-\frac{\log_2(M)}{M-1}$

BER Estimations

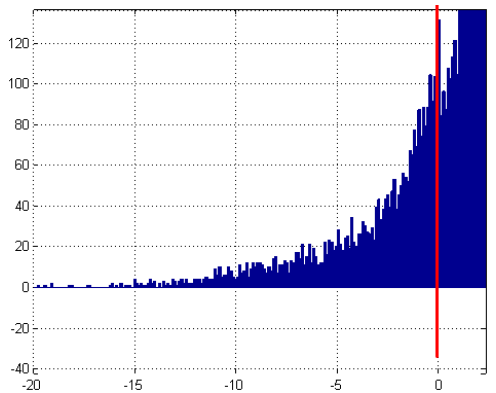
- For analog based receiver, the margin can be derived using vertical and horizontal bathtub curves, very similar to the case in NRZ
- For ADC-based receiver architecture, MSE-based BER is often used

$$\sigma^2 = MSE = \frac{\sum_1^N (x_k - \bar{x})^2}{N}$$

$$\bar{x} = \{\pm h_0, \pm 3h_0\}$$

$$BER = \frac{M-1}{2M}\operatorname{erfc}\left(\frac{h_0}{\sqrt{2}\sigma}\right) = \frac{3}{8}\operatorname{erfc}\left(\frac{h_0}{\sqrt{2}\sigma}\right)$$

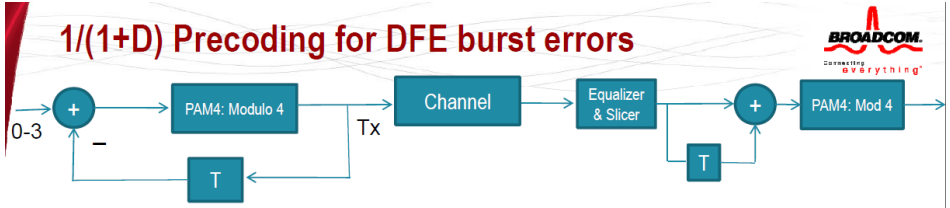
- When BER is high (>1e-6), even in a simulation with a couple of million of symbols, there would be decision errors. Thus, the statistical method introduced above needs to be modified
  - This is true because cross data slicer samples need to be identified and treated differently
  - An example here shows that there are quite a few cross-boundary samples. They are registered on the negative side



Precoding to Reduce DFE Burst Errors

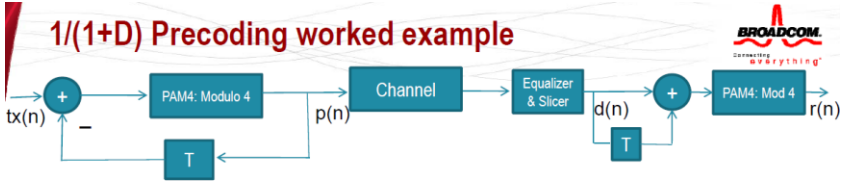
- A good tutorial on this subject can be found in in “Precoding proposal for PAM4 modulation”, 100Gb/s Backplane and Cable Task Force, IEEE 802.3, September 2011
- A highlight is duplicated below

1/(1+D) Precoding for DFE burst errors



- **The burst error length of the DFE error events for PAM4 can be reduced by using precoding**
- **PAM4 Tx precoding uses a 1/(1+D) mod 4**
  - See bliss_01_0311, “**Signaling Terminology; PAM-M and Partial Response Precoders**”
  - Multilevel version of the duo-binary precoder
  - Rx uses a (1+D) mod 4 after slicing
- **Simple to implement**
- **Very low Complexity**
- **Reduces 1 tap DFE burst error runs into 2 errors per error event**
  - One error at the entry, one error at the exit

1/(1+D) Precoding worked example



- **Precoder Input : tx(n)**
  - – 2 2 2 2 0 3 2 0 1 3 3 0 0 0 0 2 3 0 3
- **Precoder Output : p(n)**
  - – 0 2 0 2 2 1 1 3 2 1 2 2 2 2 2 0 3 1 2
- **DFE, Slicer Output : d(n)**
  - – 0 1 1 1 3 0 2 2 3 0 3 1 3 1 3 0 3 1 2
- **Error Event : p(n) – d(n)**
  - – 0 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 0 0 0 0
- **Decoder Output after 1+D at Rx : r(n)**
  - – 2 1 2 2 0 3 2 0 1 3 3 0 0 0 0 3 3 0 3

Entry Error

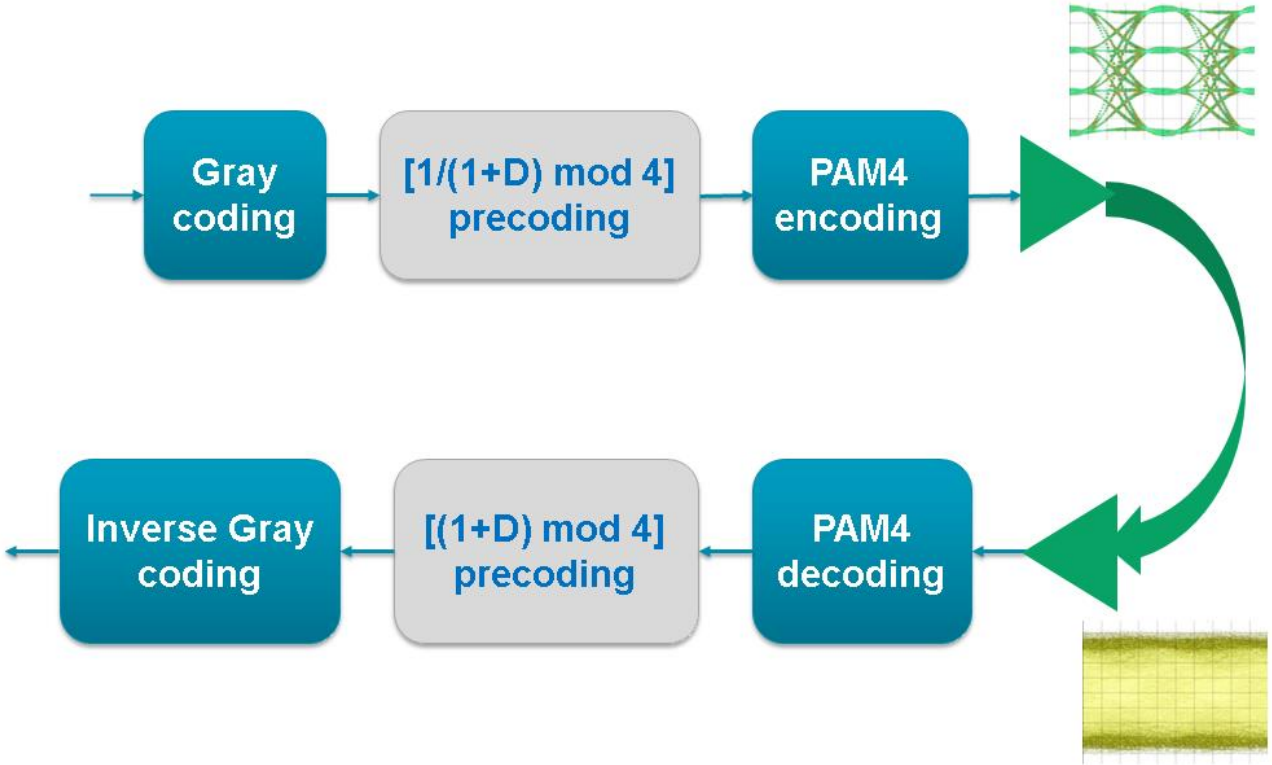
Exit Error

Precoding Benefit Example

Enable Precoding		Off	On
MSE SER		4.28e-4	4.06e-4
Number of SE		2084	1693
True SER		1.04e-3	8.47e-4
Skip Code Errors	1	0	0
	2	0	402
Tally of symbol errors as a function of burst error length	1	231	1187
	2	215	253
	3	240	0
	4	86	0
	5	40	0
	6	10	0
	7	9	0
	8	2	0
	9	1	0
	10	0	0
	11	1	0

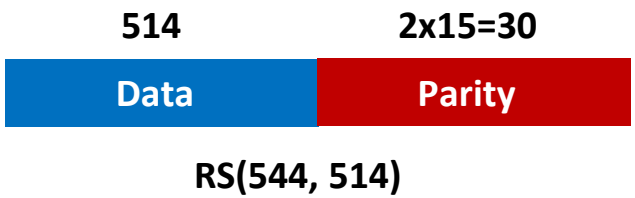
- A challenging link is used as an example such that we will encounter many errors
- The RX equalizer includes a 1-tap DFE
- 3M symbols are simulated and the last 2M are used for analysis
- It is seen that when precoding is not enabled (Off), we experienced symbol error run-length as large as 11
- When precoding is enabled (On), the symbol error run-length is no more than 2
  - Burst error run length of only up to 2 for 1-tap DFE is not always guaranteed

TX and RX Signaling Process with Precoding – 2



FEC Adopted in IEEE P802.3bj and P802.3bs

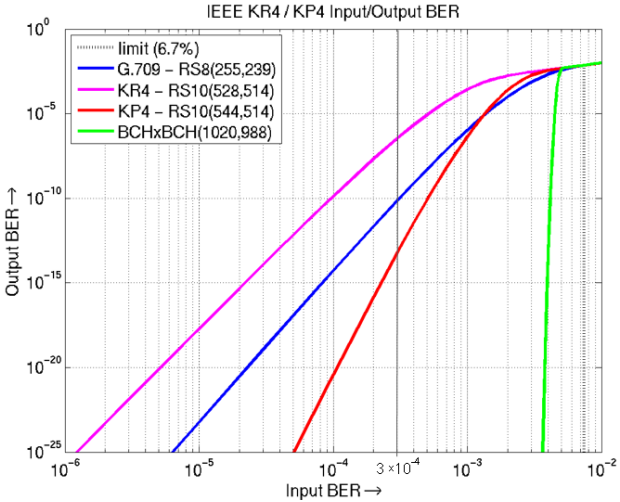
- FEC encoding introduces redundancy into the codeword
  - A block of k data symbols becomes a codeword of n symbols, (n, k)
  - The FEC decoding finds the decoded codeword that is closest to the received codeword
- The FEC decoding is guaranteed to correct T erred symbols in a received codeword. Reed-Solomon FEC coding (RS-FEC) examples
  - RS(528, 514, T=7, M=10), is proposed in IEEE P802.3bj for 25G NRZ
  - RS(544, 514, T=15, M=10), is proposed in IEEE P802.3bj for 28G PAM4
  - RS(544, 514, T=15, M=10), is proposed in IEEE P802.3bs for 56G PAM4
- KP4 FEC Example



  - At its most effective, KP4-FEC can correct as many as 150 bit errors in 5440 bits
  - At the other extreme, KP4-FEC can correct no more than 15 bit errors in 5440 bits
    - If 16 bit errors are distributed across 16 different 10-bit symbols, KP4 FEC simply cannot correct them

FEC Error Correction Capability – Coding Gain

- The coding gain is the reduction in SNR (dB) that can be accommodated while still achieving the desired BER. Under normal link operation conditions, test from system houses showed that
  - RS(528, 514) (KR4 FEC) presents about 5 – 6 dB coding gain
  - RS(544, 514) (KP4 FEC) presents about 7 – 8 dB coding gain



The plot assumes normal, uniform random distribution (Additive White Gaussian Noise)

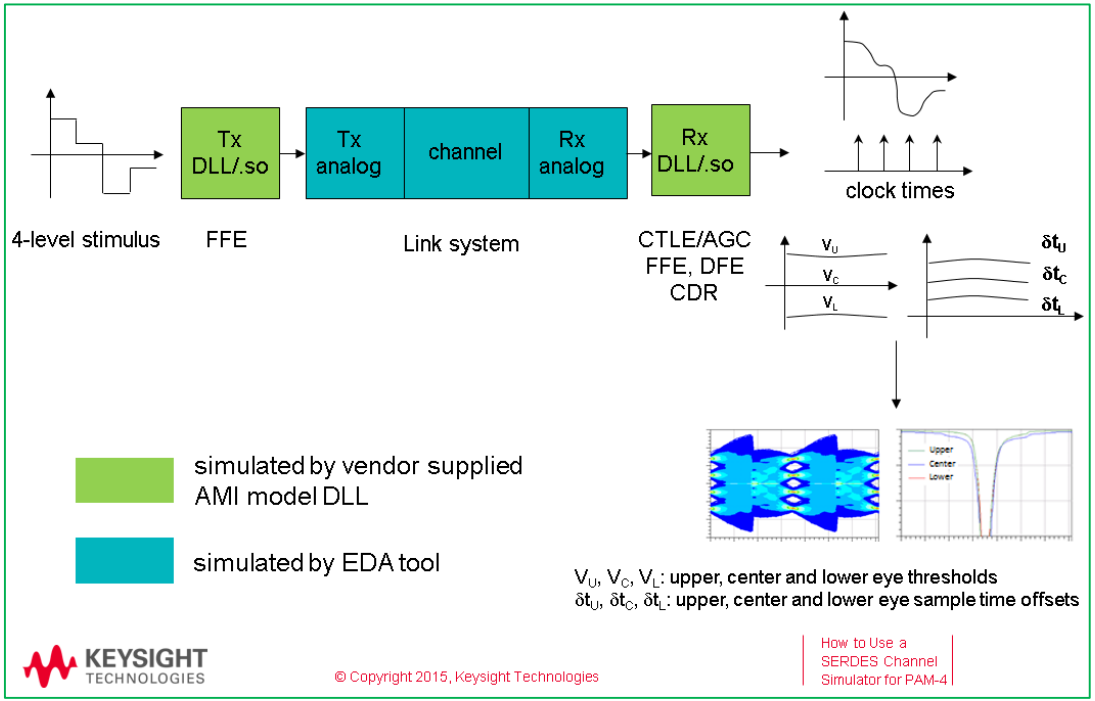
- Example of Input vs Output BER for several well known FEC codes:
  - G.709: RS8 (255,239) 6.7%
  - IEEE KR4: RS10 (528,514) 3.5%
  - IEEE KP4: RS10 (544, 514) 5.8%
  - BCH-BCH (I.9, G.975.1) : 6.7%
  - Shannon limit for 6.7% OH (G.709 rate)
- Need to keep in mind the over-clocking induced SNR loss when using FEC

Channel Operating Margin (COM) for PAM4

- COM is a FOM for a passive electrical channel, based on data eye formalization
- COM has assumed a practical TX and RX equalization capability. COM has defined detailed calculation of crosstalk and ISI distributions, rather than simply treating them as Gaussian distribution. COM does not consider CDR timing, but allows some margin in computed result
- COM reference code can be found at http://www.ieee802.org/3/bj/public/tools/ran_com_3bj_3bm_01_1114.zip
- There have proposals to modify the current COM parameters or to modify parameters ranges or to add new parameters to better represent 56G-PAM4, MR and LR, designs
- One needs to understand advantages and disadvantages of the COM approach before using it to assess the link channel
- Time domain simulations using hardware correlated models are a more sophisticated approach

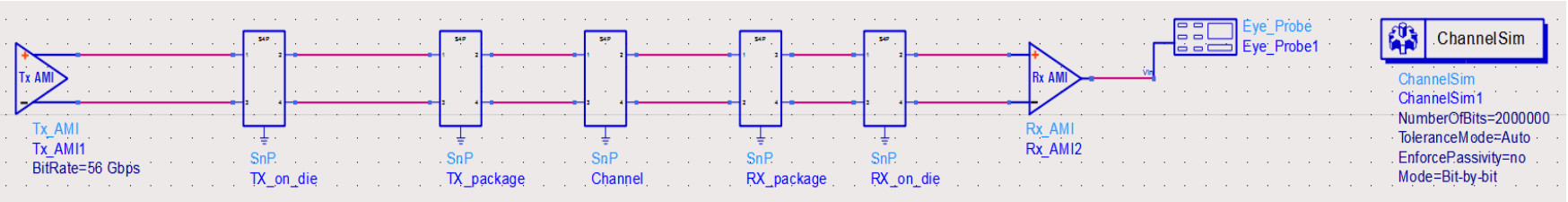
IBIS-AMI Modeling for PAM4 Signaling

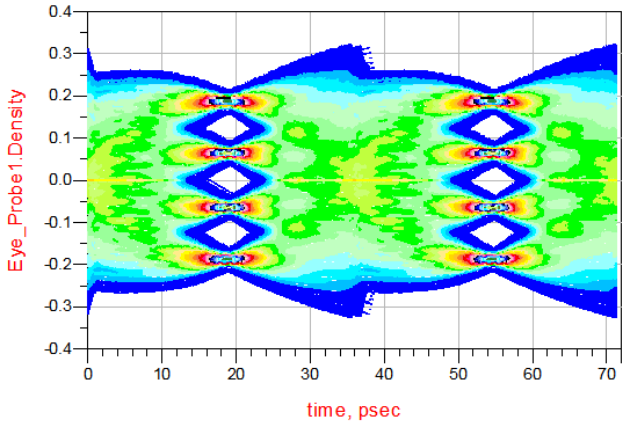
- IBIS-AMI modeling for NRZ signaling is widely accepted in the industry
- IBIS-AMI modeling for PAM4 signaling is still new, but both silicon makers and EDA tool developers are working toward this goal
- An example is provided here, based on Keysight ADS system, to show the simulation flow

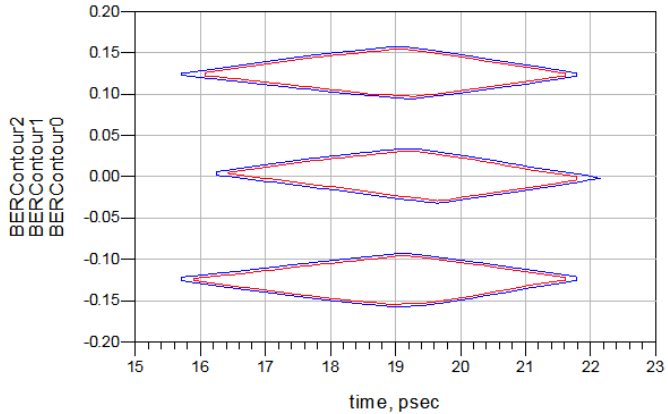


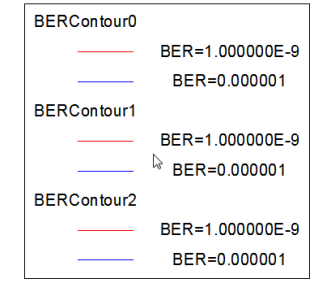
PAM4 IBIS-AMI Simulation Example

- An AMI model, for a 16nm design, was run for an MR channel at 56Gbps in ADS
- The eye diagram and BER contours for the 3 separate eyes are plotted below
- The post-processed statistical BER is 4.95e-10





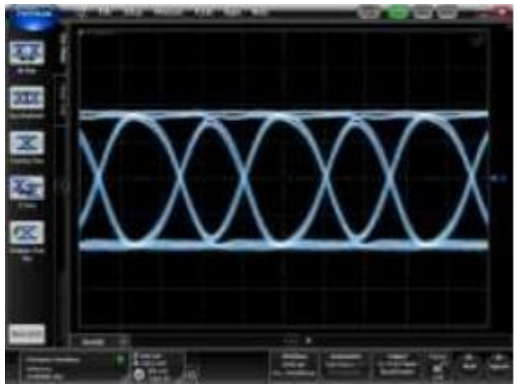


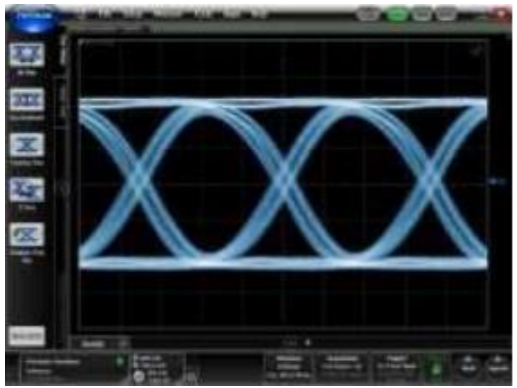


Test Patterns: JP03A and JP03B

- JP03A test pattern
  - It is a repeating {0, 3} pattern for measuring RJ and deterministic clock jitter
- JP03B test pattern
  - It is a repeating sequence of 15x {0, 3} followed by 16x{3,0}

    030303030303030303030303030**0330**30303030303030303030303030303030
  - JP03B is an ideal pattern to measure (1) random Jitter (RJ), periodic Jitter (PJ), (3) Even-Odd (F/2) Jitter (EOJ)





Transmitter Even-Odd Jitter (EOJ)

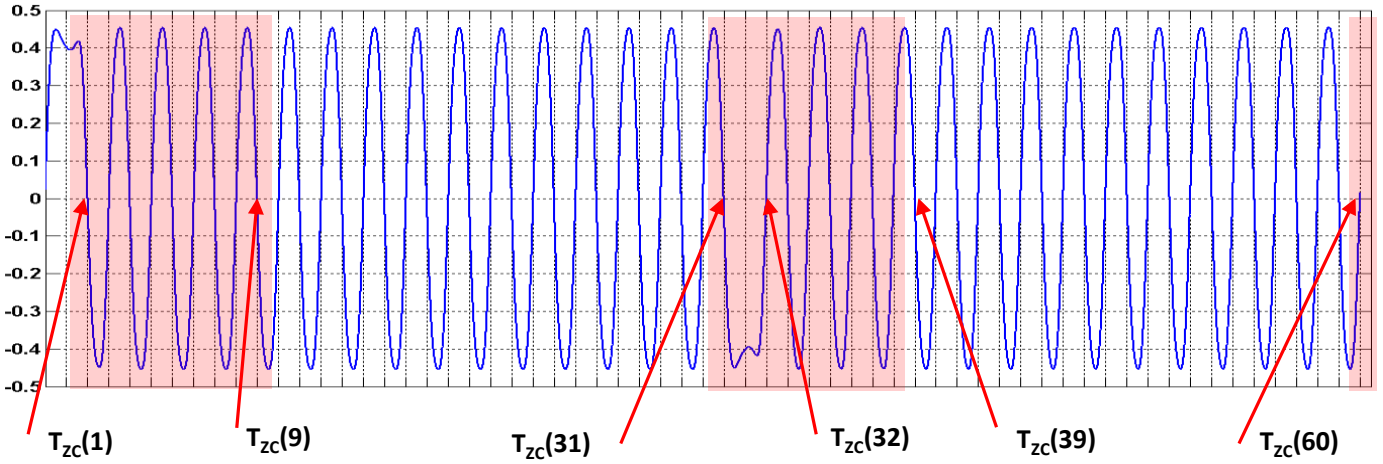
- EOJ is determined using the following procedure:
  - Use the **JP03B** test pattern
  - Capture the time for each of the 60 transitions. (Averaging of the vertical waveform or of each zero-crossing time is recommended to mitigate the contribution of uncorrelated noise and jitter.)
  - Denote the averaged zero-crossing times as $T_{ZC}(i)$, where i = {1,2,...60} and where i = 1 designates the transition from 3 to 0 after the consecutive symbols 3 and 3
  - The set of 40 pulse widths, ΔT(j), isolated from the double-width pulses are determined using the relationship:

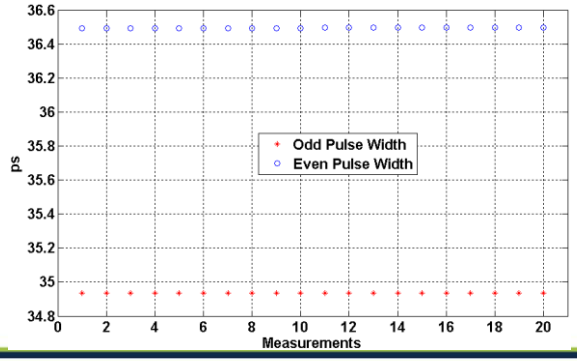
$$\Delta T(j) = \begin{Bmatrix} T_{ZC}(j+10) - T_{ZC}(j+9) & 1 \le j \le 20 \\ T_{ZC}(j+19) - T_{ZC}(j+18) & 21 \le j \le 40 \end{Bmatrix}$$

  - EOJ is calculated as

$$EOJ = \frac{\left| \sum_{j=1}^{20} \Delta T(2 \cdot j) - \sum_{j=1}^{20} \Delta T(2 \cdot j - 1) \right|}{40}$$

Transmitter EOJ Computation Example

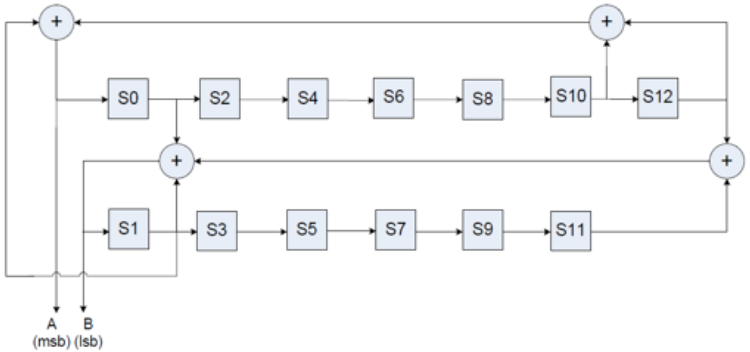


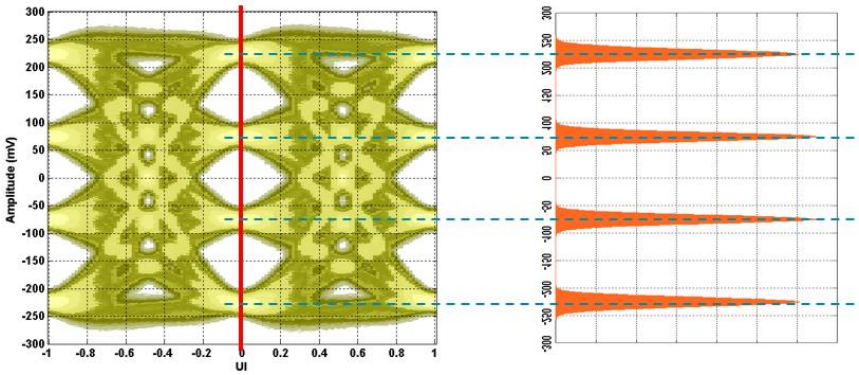


- Computed EOJ = 1.56/2 = 0.78 ps
- This is 2.18% UI

Potential Test Pattern 1 – QPRBS13

- A short while spectrally rich and statistically well-behaved pattern is important for eye metric test, such as signal levels, the mean “thickness” and distributions, and eye vertical alignment, etc.
- Quaternary PRBS13 (QPRBS13) pattern is potentially a good candidate
  - The QPRBS13 test pattern is a repeating 8191-symbol sequence
  - Each test pattern is encoded as a digital input from a PRBS13 generator
  - Two full cycles of 8191 bits are concatenated to form the 16382 bit sequence, R(1:16382)
    - Bits in the first cycle, R(1:8191) are non-inverted
    - Bits in the second cycle, R(8192:16382), are inverted

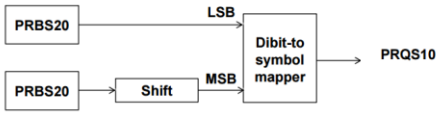




Potential Test Pattern 2 – PRQS10

- Another good candidate is PRQS (Pseudo Random Quaternary Sequence) pattern
- It is a natural generalization of PRBS to quaternary sequences for PAM4
- PRQS patterns can be generated algorithmically using either GF(4) arithmetic based LFSRs or by multiplexing 2 appropriate PRBS patterns
- The proposed PRQS10 has desirable statistical properties for emulating random PAM4 data, provides good baseline wander characteristics, and has modest length ~ 1M symbols

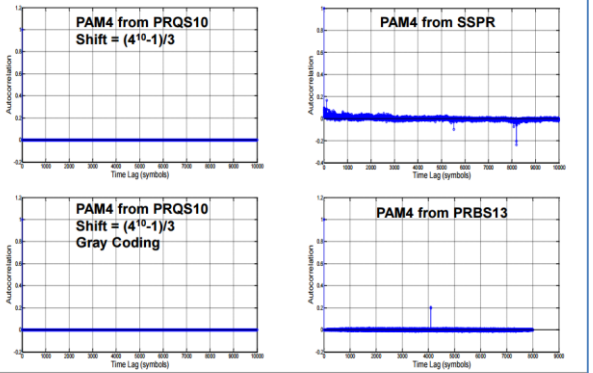
Proposed PAM4 Test Pattern: PRQS10



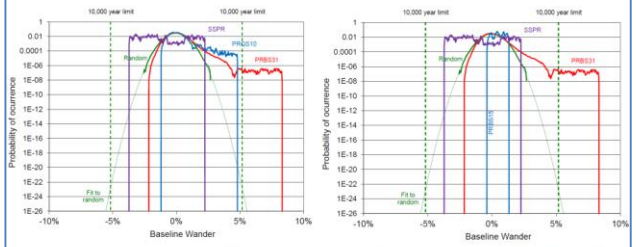
- Algorithmically generated based on multiplexing two PRBS20 patterns
- True maximum length quaternary sequence, i.e. contains all 10 length symbol patterns with equal probability (except for all 10 zeros)
- Pattern length = 4^{10}-1 = 1,048,575 ~ 1 M (short enough for DCAs to support)
- Good "random" statistical properties (see also next slide):

	P0	P1	P2	P3	Transition Density
PRQS10	**0.2500**	**0.2500**	**0.2500**	**0.2500**	**0.7500**
SSPR	0.2573	0.2279	0.2575	0.2573	0.7101
PRBS13	0.2499	0.2500	0.2500	0.2500	0.7501

Simulated Autocorrelation



Baseline Wander Characteristics

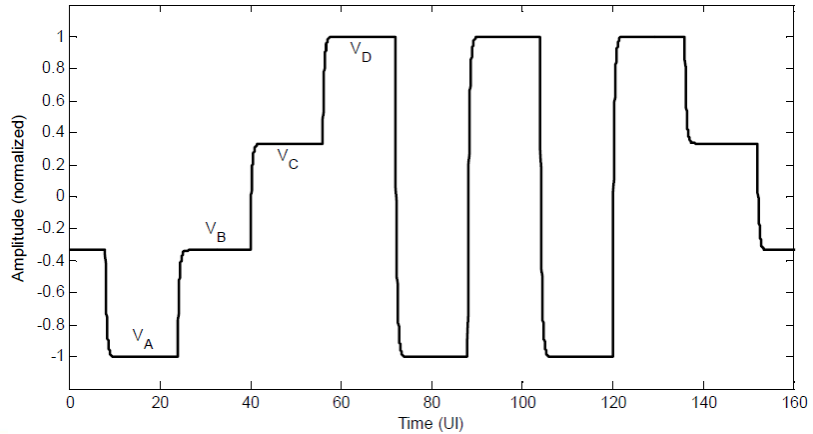


Source: anslow_01_0915_smf

Source: anslow_3bs_03_0714

Transmitter Nonlinearity – Level Mismatch R_{LM}

- The level separation mismatch ratio, R_{LM}, is specified as >= 0.95 for MR and LR, based on CEI-56G-PAM4 baseline specs
- Transmitter linearity test pattern
  - It is a repeating 160-symbol pattern with a sequence of 10 symbol values each 16 UI in duration
  - The 10 values are {-1,–1/3,+1/3,+1,–1,+1,–1,+1,+1/3,–1/3}



$$S_{min} = \frac{min(V_D - V_C, V_C - V_B, V_B - V_A)}{2}$$

$$V_{avg} = \frac{V_A + V_B + V_C + V_D}{4}$$

$$ES_1 = \frac{V_B - V_{avg}}{V_A - V_{avg}}$$

$$ES_2 = \frac{V_C - V_{avg}}{V_D - V_{avg}}$$

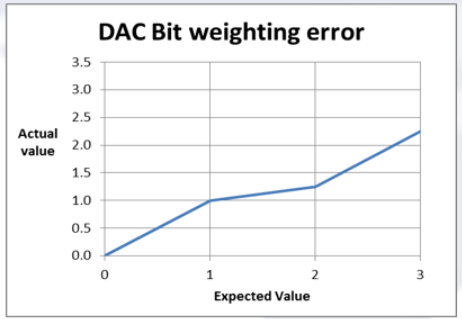
$$R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A}$$

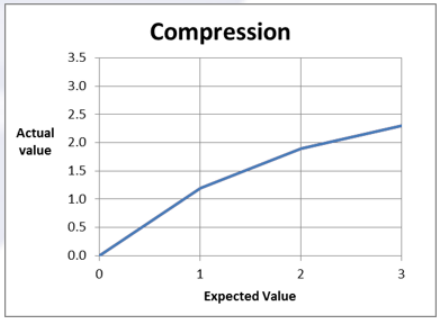
Modeling R_{LM}

- This is a proposal at OIF, October, 2015, Shanghai, by Keysight

'Designing' the stress

- The linearity stress should emulate impairments likely to occur in the link
- Assume majority of non-linearity is introduced by the transmitter and not the channel
- Possible mechanisms:
  - DAC bit weighting error
  - Compression/expansion in Output driver





3

OIF OPTICAL INTERNETWORKING FORUM

R_{LM} Impact Example

- Once R_{LM} profile is defined, its impact on link margin can be simulated
- An example is shown here of 3 different values of R_{LM} whose profile is defined below

$$v_{mapped} = (R_{LM} - 1) \cdot v_{ideal}^2 + (4 - 3 \cdot R_{LM}) \cdot v_{ideal}$$

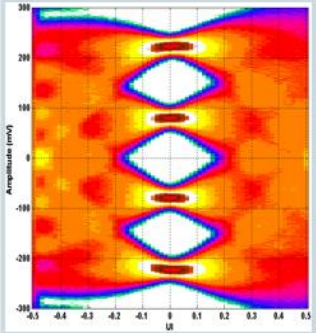
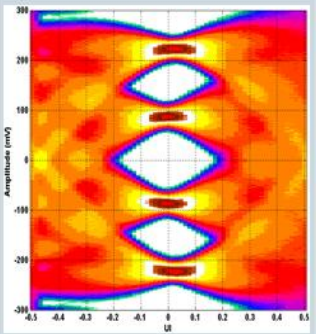
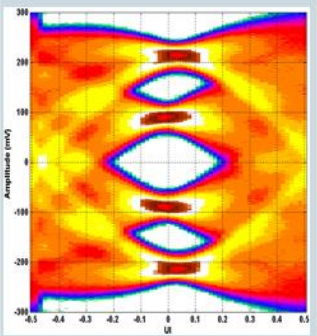
For $0 \le v_{ideal} \le 3$

$$v_{mapped} = -(R_{LM} - 1) \cdot v_{ideal}^2 + (4 - 3 \cdot R_{LM}) \cdot v_{ideal}$$

For $-3 \le v_{ideal} < 0$

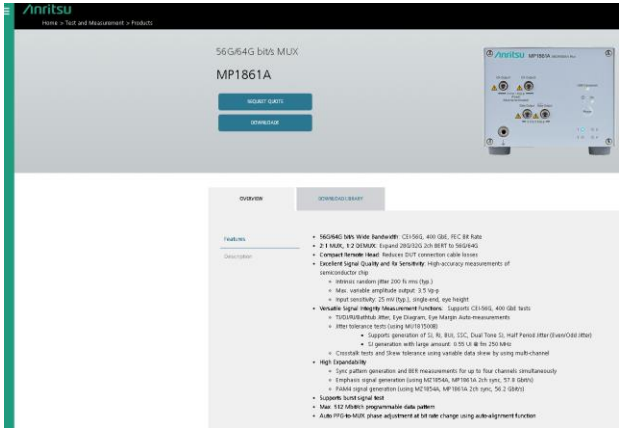
$$v_{out} = \left(\frac{v_{mapped}}{3}\right) \cdot v_{swing}$$

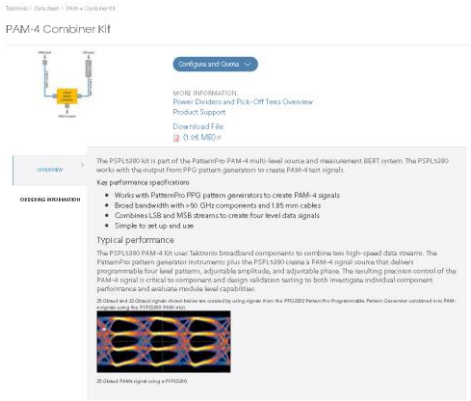
v_{swing} is defined diff zero peak

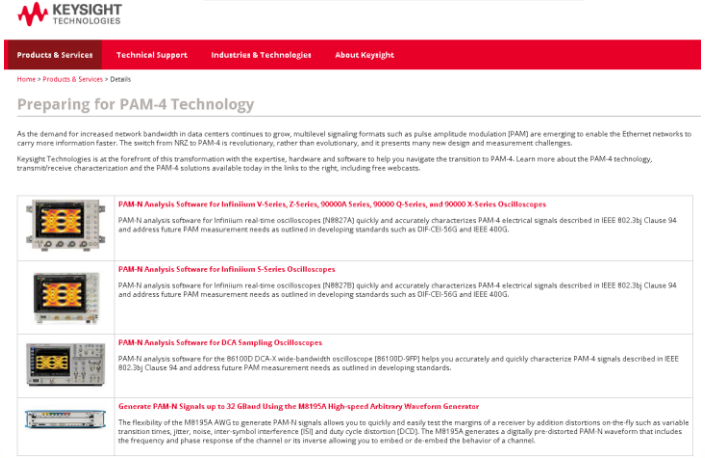
R_{LM}	0.99	0.92	0.85
Eye Diagram			
BER	2.11e-22	1.17e-14	3.67e-8

Test Equipment for 56G PAM4

- As always, test equipment companies are working proactively to provided all kinds of equipment for 56G PAM4 signaling test and measurement, both electrical and optical
- A few examples are listed below. For details please contact your instrument vendors







Glossaries

- ADC – Analog-to-Digital Converter
- AGC – Automatic Gain Control
- AMI – Algorithmic Modeling Interface
- BER – Bit Error Ratio
- CEI – Common Electrical Interface
- COM – Channel Operating Margin
- CTLE – Continuous Time Linear Equalizer
- C2C – Chip-to-Chip
- C2M – Chip-to-Module
- DFE – Decision Feedback Equalization
- DSP – Digital Signal Processor
- EDA – Electronic Design Automation
- EOJ – Even-Odd Jitter
- EP – Error Propagation
- EQ – Equalization
- FEC – Forward Error Correction
- FEXT – Far End Crosstalk
- FFE – Feed-Forward Equalization
- FIR – Finite Impulse Response
- FOM – Figure Of Merit
- IBIS – Input/output Buffer Information Specification
- ICR – Insertion Loss to Crosstalk Ratio
- ICN – Integrated Crosstalk Noise
- ILD – Insertion Loss Deviation
- IIR – Infinite Impulse Response
- IPR – Impulse Response
- ISI – Inter Symbol Interference
- LR – Long Reach
- LSB – Least Significant Bit
- MR – Medium Reach
- MM – Mueller-Muller
- MMSE – Minimum Mean Square Error
- MSB – Most Significant Bit
- MSE – Mean Square Error
- NEXT – Near End Crosstalk
- NRZ – Non-Return-to-Zero
- OIF – Optical Internetworking Forum
- PAM – Pulse Amplitude Modulation
- PHY – Physical Layer
- PRBS – Pseudo Random Binary Sequence
- PRQS – Pseudo Random quaternary Sequence
- PSFEXT – Power Sum of FEXT
- PSD – Power Spectral Density
- PSNEXT – Power Sum of NEXT
- PSXT – Power Sum of Crosstalk
- QPRBS – Quaternary PRBS
- RMS – Root Mean Square
- SBR – Single Bit Response
- SER – Symbol Error Ratio
- SNR – Signal-to-Noise Ratio
- TD – Transition Density
- VEC – Vertical Eye Closure
- VSR - Very Short Reach

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Thank You!

QUESTIONS?