

# Xilinx T1 Telco Accelerator Card

## 5G Virtual BBU, O-DU, and O-CU Acceleration

### OVERVIEW

Xilinx T1 Telco Accelerator card provides high performance, low latency, and power efficiency needed for 5G O-DU deployments. The turnkey solution enables operators, system integrators, and OEMs to get to market quickly and to simplify the deployment of services at the edge.

T1 card uses 16nm Zynq® UltraScale+™ MPSoC and Zynq UltraScale+ RFSoc devices to accelerate fronthaul and real-time baseband (L1) lookaside processing.

- > ZU19EG MPSoC provides the 3GPP O-RAN 7.2 split fronthaul traffic termination for 5G eCPRI/RoE/SyncE protocols. The Zynq UltraScale+ MPSoC also implements IEEE Std 1588 timing functionality with onboard reference clock timing circuit.
- > ZU21DR RFSoc includes 4G/5G encode and decode acceleration along with wrapper functions such as rate matching and CRC logic. Zynq UltraScale+ RFSoc has hardened soft-decision forward error correction (SD-FEC), which can perform high-performance encode and decode with low latency and low power.



The T1 card's PCIe® Gen3 x16 connector is bifurcated into dual PCIe Gen3 x8 interfaces, giving each device independent access to the host. The board is a single slot full height, half length (FHHL) form factor with two SFP28 optical interface connectors.

### TARGET APPLICATIONS

- > 5G ORAN-7.2 Fronthaul termination
- > 5G L1 baseband acceleration
- > 5G Fronthaul with Low-PHY (optional) functions

### PERFORMANCE

Virtualization requires significant acceleration of latency-sensitive and compute-intensive functions. The T1 card performance metrics below are based on in-lab measurements of the card reference design. Watch the launch video at: [www.xilinx.com/T1](http://www.xilinx.com/T1).

#### Fronthaul Performance

Fronthaul Configuration <sup>(1)</sup>	Performance	Notes
ACTIVE-STANDBY with O-RAN Processing on T1	<ul style="list-style-type: none"> <li>&gt; 25Gb/s Active (2 sectors of 4T4R 100MHz)</li> <li>&gt; 25Gb/s Standby (If Active link fails)</li> </ul>	For high-reliability deployments
ACTIVE with O-RAN Processing on T1	<ul style="list-style-type: none"> <li>&gt; 25Gb/s Active (1 sector of 4T4R 100MHz)</li> <li>&gt; 25Gb/s Active (1 sector of 4T4R 100MHz)</li> </ul>	For deployments utilizing fronthaul gateways
ACTIVE With O-RAN in software	<ul style="list-style-type: none"> <li>&gt; 50Gb/s (4 sectors of 4T4R 100MHz with 4 layers each)</li> </ul>	For high-density deployments

(1) Other configurations for fronthaul are possible

#### L1 (Baseband) Acceleration Performance

	Performance	Latency
LDPC Encode	17.8Gb/s	14µs
LDPC Decode	8.1Gb/s	16µs

SoCs	Xilinx   Zynq UltraScale Plus RFSoc   XCZU21DR	
	Xilinx   Zynq UltraScale+ MPSoc   XCZU19EG	
SoC Resources	<b>XCZU21DR</b>	<b>XCZU19EG</b>
	<ul style="list-style-type: none"> <li>&gt; System Logic cells - 930K</li> <li>&gt; CLB LUT - 425K</li> <li>&gt; SDFEC -8</li> <li>&gt; DSP Slices - 4,272</li> <li>&gt; BRAM - 38.0Mb</li> <li>&gt; URAM - 22.5Mb</li> </ul>	<ul style="list-style-type: none"> <li>&gt; System Logic cells - 1,143K</li> <li>&gt; CLB LUT - 523K</li> <li>&gt; CLB Flip-Flops -1,045K</li> <li>&gt; DSP Slices - 1,968</li> <li>&gt; BRAM - 34.6Mb</li> <li>&gt; URAM - 36.0Mb</li> </ul>
Form Factor	<ul style="list-style-type: none"> <li>&gt; Full-height, half-length (FHHL)</li> <li>&gt; x16 PCIe form factor</li> <li>&gt; Width: 167.65mm</li> <li>&gt; Height: 111.15mm</li> <li>&gt; Depth: 34.8mm</li> </ul>	
PCIe Interface	PCIe Gen3 x16 interface bifurcated to two PCIe Gen3 x8	
Onboard Memory	<b>XCZU21DR</b>	<b>XCZU19EG</b>
	<ul style="list-style-type: none"> <li>&gt; 1x Banks of 4GB x72 (64 bit +8bit ECC) - PL</li> <li>&gt; 1x Banks of 2GB x 40 (32 bit +8bit ECC) - PS</li> <li>&gt; Total Capacity 4GB in PL</li> <li>&gt; Total Capacity 2GB in PS</li> </ul>	<ul style="list-style-type: none"> <li>&gt; 1x Banks of 4GB x72 (64 bit +8bit ECC) - PL</li> <li>&gt; 1x Banks of 2GB x 40 (32 bit +8bit ECC) - PS</li> <li>&gt; Total Capacity 4GB in PL</li> <li>&gt; Total Capacity 2GB in PS</li> </ul>
In System Upgrade	Standard Xilinx tandem and partial reconfiguration support for both devices	
Programming	<ul style="list-style-type: none"> <li>&gt; 1x 2Gb QSPI NOR Flash for FPGA configuration for ZU19EG</li> <li>&gt; 1x 2Gb QSPI NOR Flash for FPGA configuration for ZU21DR</li> </ul>	
Network Interface(s)	<ul style="list-style-type: none"> <li>&gt; 2xSFP28 optical interfaces to XCZU19EG</li> <li>(User Configurable, includes 10/25 Ethernet)</li> </ul>	
Other External Interface(s)	Micro USB for JTAG support (FPGA programming and debug) and access to BMC	
Reference Design	Vivado® design (diagnostic bit file) and commands for testing all datapath interfaces available for diagnostic bit files for both FPGAs	
Cooling	Passive cooling, custom heat sink	
Board Management Controller	<ul style="list-style-type: none"> <li>&gt; Power sequencing and reset</li> <li>&gt; Field upgrades</li> <li>&gt; FPGA configuration and control</li> </ul>	
Operating Temperature	<ul style="list-style-type: none"> <li>&gt; Clock configuration</li> <li>&gt; Temperature monitoring</li> <li>&gt; USB 2.0</li> </ul>	
Power	0–100°C (up to 110°C for NEBS excursion)	
Power	< 75W typical	
Clocking Options	<ul style="list-style-type: none"> <li>&gt; Low-Jitter, configurable clock ranging from 10MHz to 750 MHz</li> <li>&gt; Capable of ITU-T G8273.2</li> <li>&gt; 1 PPS input and output mode support</li> <li>&gt; Have assembly option for OCXO and/or TCXO for Master and slave mode operation</li> </ul>	

1. Timing Circuitry

- > TCXO/OCXO with PPS in and out.
- > PS (A53) for 1588 protocol stack

2. Fronthaul Termination

- > 2x25G eCPRI w/TSN + RS-FEC & 1588
- > Aggregation Logic
- > Buffer memory
- > Packet Classification

3. L1 Offload

- > LDPC/TURBO codecs
- > Polar codecs
- > HARQ management
- > Codec Surrounding/Wrapper logic
  - CRC logic
  - Rate Matching/De-Matching

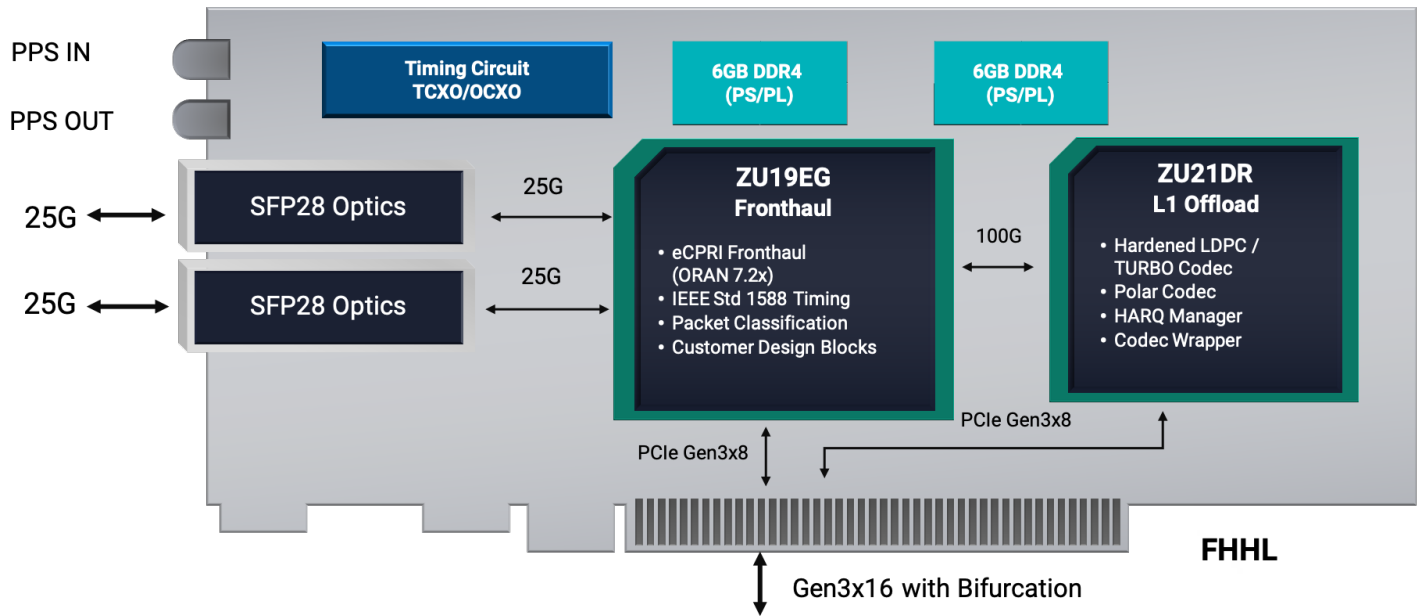


Figure 1: Xilinx T1 Block Diagram

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