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JUNE 1987 £1.95

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Image sensing algorithms

Recharging lithium cells

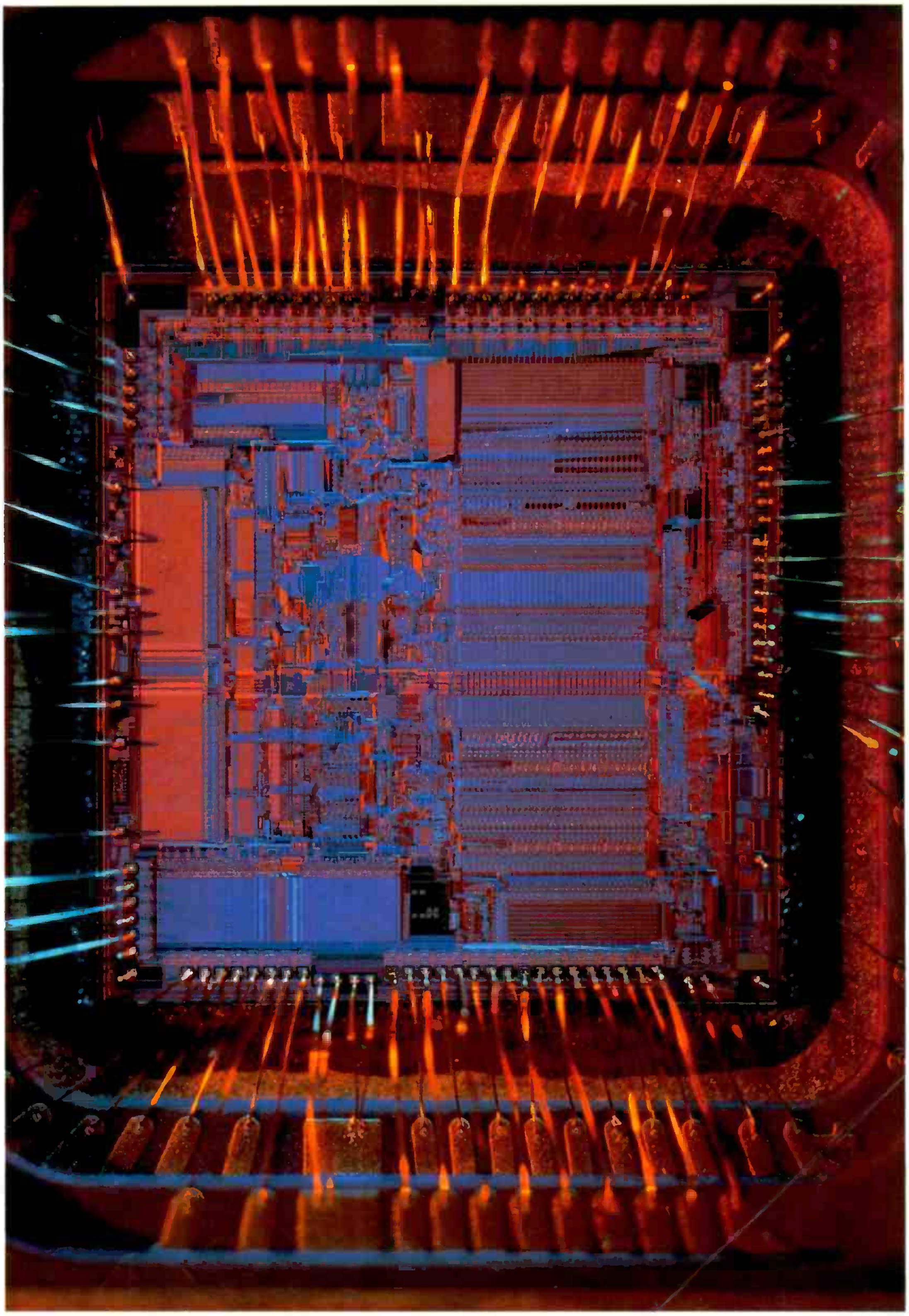
Coprocessor interfacing

Serial eprom programmer

Noise figure vs noise factor

High res graphics chip

Kelvin's dictum



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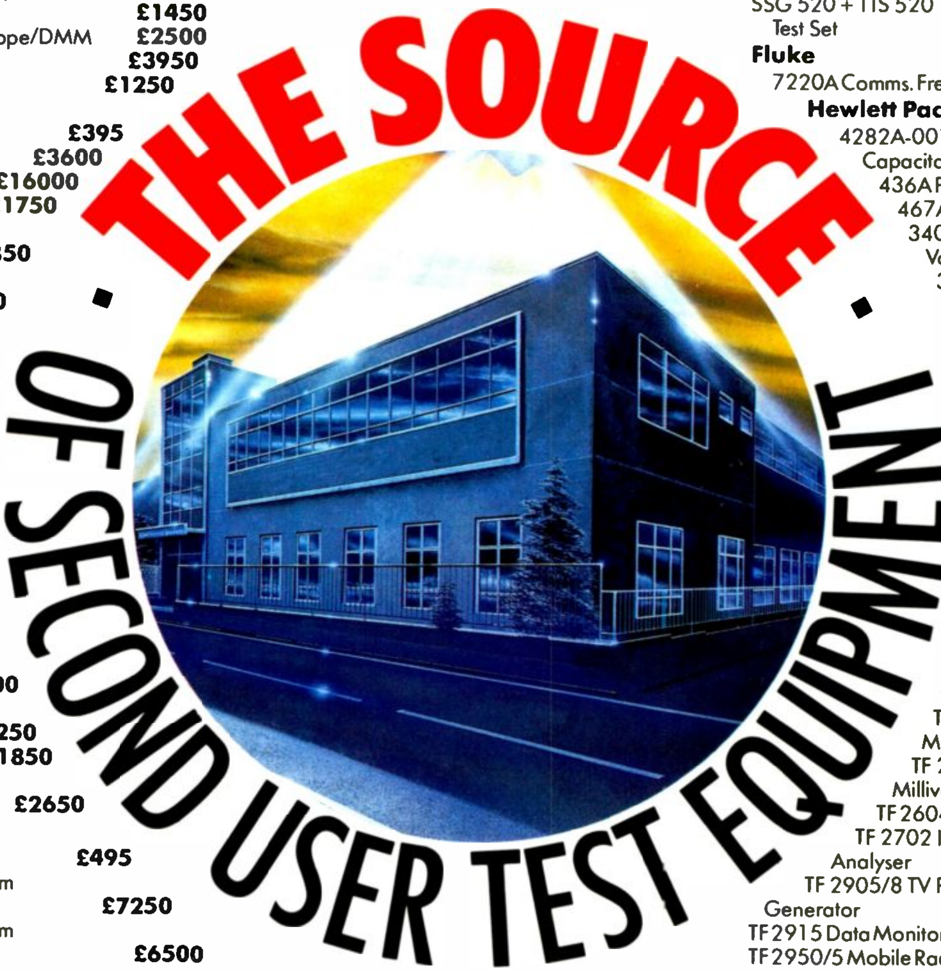

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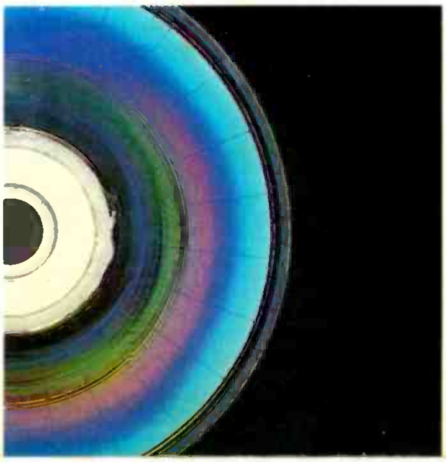

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British r & d – the light under the bushel

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Reactions to the news that a second British airborne defence radar is likely to be abandoned as was Nimrod vary between the weakly humorous "British airborne radar – the lost horizon" through the incredulous "No, not again" to the fatalistic "Just one more example of the British inability to develop anything". Obviously there is an element of truth in all these; the last as a generality has become increasingly popular over the years and superficially at least has a significant bearing on this matter.

At the same time there is another side to this story, which can be put in terms of the experience that is still available in the UK. Project troubles of this magnitude have been cured in the past, even in radar, but this doesn't mean that a complete formula has been found, especially when subjected to ever-increasing demands for results within a shrinking time schedule. But experience of such situations suggests there are certain fundamental principles that have been pushed into the background, quite understandably in the all-pervading computer context.

The information that has been released in both cases does more than indicate that two main areas of difficulty are involved. One is the computer, and the virtual impossibility of providing anything like sufficient software for Nimrod. The other is the antenna system, and though less obvious it could well provide more than one key answer to the overall problem, remembering that in such complex systems failure is often found to lie with a comparatively simple but isolated and difficult-to-detect fault. Therein lies the weakness of the computer. Obscure physical faults are not shown up by it – they are 'lost in the computer'.

A highly relevant example of this can almost certainly be found in the antenna system's radome. Clearly it cannot be said that in these two cases the radome is more than a suspect element. Nevertheless, a poorly designed or constructed radome can be responsible for generating spurious side lobes and squint, and for reflection-back of r.f. power with all that this implies.

This is only the tip of the iceberg, but it does highlight the difficulties facing an r & d team in isolating the factors making up a fault condition. A master watchword in radar, or any other form of technological development for that matter, is to alter only one thing at a time, and it is a 'crashing glimpse of the obvious' that there is just not enough time to adopt the step by step approach thus implied.

However, at the risk of over-simplification, it is suggested that with pockets of know-how still to be found in the UK, existing equipment could be adapted to be used as tried steps in such programmes *provided that* human intervention could be brought into service to fill in the gaps of knowledge that are inevitable when starting from scratch.

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2 × 50 way (S100conn)	600p	—

AMPHENOL CONNECTORS

36 way plug Centronics (solder 500p (IDC) 475p
36 way skt Centronics (solder) 550p (IDC) 500p
24 way plug IEEE (solder) 475p (IDC) 475p
24 way skt IEEE (solder) 500p (IDC) 500p
PCB Mtg Skt Ang Pin
24 way 700p 36 way 750p

RIBBON CABLE

(grey/metre)

10-way	40p	34-way	160p
16-way	60p	40-way	180p
20-way	85p	50-way	200p
26-way	120p	64-way	280p

DIL HEADERS

	Solder	IDC
14 pin	40p	100p
16 pin	50p	110p
18 pin	60p	—
20 pin	75p	—
24 pin	100p	150p
28 pin	160p	200p
40 pin	200p	225p

D CONNECTORS

No of Ways

	9	15	25	37
MALE:				
Ang Pins	120	180	230	350
Solder	60	85	125	170
IDC	175	275	325	—
FEMALE:				
St Pin	100	140	210	380
Ang Pins	160	210	275	440
Solder	90	130	195	290
IDC	195	325	375	—
St Hood	90	95	100	120
Screw Lock	130	150	175	—

EURO CONNECTORS

DIN 41612	Plug	Skt
2 × 32 way St Pin	230p	275p
2 × 32 way Ang Pin	275p	320p
3 × 32 way St Pin	260p	300p
3 × 32 way Ang Pin	375p	400p
IDC Skt A + B	400p	
IDC Skt A + C	400p	

For 2 × 32 way please specify spacing (A + B, A + C).

GENDER CHANGERS

25 way D type

Male to Male £10
Male to Female £10
Female to Female £10

RS 232 JUMPERS

(25 way D)

24" Single end Male £5.00
24" Single end Female £5.25
24" Female Female £10.00
24" Male Male £9.50
24" Male Female £9.50

SOFTY II

This low cost intelligent eprom programmer can program 2716, 2516, 2532, 2732, and with an adaptor, 2564 and 2764. Displays 512 byte page on TV — has a serial and parallel I/O routines. Can be used as an emulator, cassette interface.
Softy II ...... £195.00(b)
Adaptor for 2764/2564 ...... £25.00

SPECIAL OFFER

2764-25 £2.50 (d);
27128-25 £2.75 (d);
6264 LP-15 £2.80 (d);

TEXTOOL ZIF

SOCKETS 24-pin £7.50
28-pin £9.10 40 pin £12.10

MISC CONNS

21 pin Scart Connector 200p
8 pin Video Connector 200p

DIL SWITCHES

4-way 90p 6-way 105p
8-way 120p 10-way 150p

ATTENTION

All prices in this double page advertisement are subject to change without notice.
ALL PRICES EXCLUDE VAT
Please add carriage 50p unless indicated as follows:
(a) £8 (b) £2.50 (c) £1.50 (d) £1.00

TECHNOLINE VIEWDATA SYSTEM. TEL: 01-450 9764

Using 'Prestel' type protocols. For information and orders — 24 hour service, 7 days a week

74 SERIES

74 SERIES	
7400	0.30
7401	0.30
7402	0.30
7403	0.30
7404	0.36
7405	0.30
7406	0.40
7407	0.40
7408	0.30
7409	0.30
7410	0.30
7411	0.30
7412	0.30
7413	0.50
7414	0.70
7416	0.36
7417	0.40
7420	0.30
7421	0.60
7422	0.36
7423	0.36
7425	0.40
7426	0.40
7427	0.32
7428	0.43
7430	0.30
7432	0.36
7433	0.30
7437	0.30
7438	0.40
7439	0.40
7440	0.40
7441	0.90
7442A	0.70
7443A	1.00
7444	1.10
7445	0.70
7446A	1.00
7447A	1.00
7448	1.00
7450	0.36
7451	0.35
7453	0.38
7454	0.38
7460	0.55
7470	0.50
7472	0.45
7473	0.45
7474	0.50
7475	0.60
7476	0.45
7480	0.65
7481	1.80
7483A	1.05
7484A	1.25
7485	1.10
7486	0.42
7489	2.10
7490A	0.55
7491	0.70
7492A	0.70
7493A	0.55
7494	1.10
7495A	0.60
7496	0.80
7497	2.90
74100	1.90
74107	0.50
74109	0.75
74110	0.75
74111	0.55
74116	1.70
74118	1.10
74119	1.70
74120	1.00
74121	0.55
74122	0.70
74123	0.80
74125	0.65
74126	0.55
74128	0.55
74132	0.75
74136	0.70
74141	0.90
74142	2.50
74143	1.30
74144	2.70
74145	1.10
74147	1.70
74148	1.40
74150	1.75
74151A	0.70
74153	0.80
74154	1.40
74155	0.80
74156	0.90
74157	0.80
74159	2.25
74160	1.10
74161	0.80
74162	1.10
74163	1.10
74164	1.20
74165	1.10
74166	1.40
74167	4.00
74170	2.00
74172	4.20
74173	1.40
74174	1.10
74175	1.05
74176	1.00
74178	1.50
74179	1.50
74180	1.00
74181	3.40
74182	1.40
74184	1.80
74185A	1.80
74190	1.30
74191	1.30
74192	1.10
74193	1.15
74194	1.10
74195	0.80
74196	1.30
74197	1.10
74198	2.20
74199	2.20
74221	1.10
74251	1.00
74259	1.50
74265	0.80
74273	2.00
74276	1.40
74278	1.70
74279	0.90
74283	1.05
74742	3.20
74290	0.90
74293	0.90
74298	1.80
74351	2.00
74365A	0.80
74366A	0.80
74367A	0.80
74376	1.60
74390	1.10
74393	1.20
74490	1.40

74LS SERIES

74LS SERIES	
74LS00	0.24
74LS01	0.24
74LS02	0.24
74LS03	0.24
74LS04	0.24
74LS05	0.24
74LS08	0.24
74LS09	0.24
74LS10	0.24
74LS11	0.24
74LS13	0.34
74LS14	0.50
74LS15	0.24
74LS20	0.24
74LS21	0.24
74LS22	0.24
74LS24	0.50
74LS26	0.26
74LS27	0.24
74LS28	0.24
74LS30	0.24
74LS32	0.24
74LS32	0.24
74LS33	0.24
74LS37	0.24
74LS38	0.24
74LS40	0.24
74LS42	0.50
74LS43	1.50
74LS47	0.90
74LS49	1.00
74LS51	0.24
74LS54	0.24
74LS55	0.24
74LS73A	0.30
74LS74A	0.35
74LS75	0.45
74LS76A	0.36
74LS78	0.42
74LS83A	0.70
74LS85	0.75
74LS86	0.35
74LS90	0.48
74LS91	0.90
74LS92	0.35
74LS93	0.54
74LS95B	0.75
74LS96	0.90
74LS107	0.40
74LS109	0.40
74LS112	0.45
74LS113	0.45
74LS114	0.45
74LS122	0.70
74LS123	0.80
74LS125	0.50
74LS126	0.50
74LS132	0.65
74LS133	0.55
74LS136	0.45
74LS138	0.55
74LS139	0.55
74LS145	0.95
74LS147	1.75
74LS148	1.40
74LS151	0.65
74LS152	2.00
74LS153	0.65
74LS154	1.60
74LS155	0.65
74LS156	0.65
74LS157	0.50
74LS158	0.65
74LS160A	0.65
74LS161A	0.75
74LS162A	0.75
74LS163A	0.75
74LS164	0.75
74LS165A	1.10
74LS166A	1.50
74LS168	1.30
74LS169	1.00
74LS170	1.40
74LS173A	1.00
74LS174	0.75
74LS175	0.75
74LS181	2.00
74LS183	1.90
74LS190	0.75
74LS191	0.75
74LS192	0.80
74LS194A	0.75
74LS195A	0.75
74LS196	0.80
74LS197	0.80
74LS221	0.90
74LS240	0.80
74LS241	0.80
74LS242	0.90
74LS243	0.90
74LS244	0.70
74LS245	0.90
74LS247	1.10
74LS248	1.10
74LS249	1.10
74LS251	0.75
74LS253	0.75
74LS256	0.90
74LS2457A	0.70
74LS258A	0.70
74LS259	1.20
74LS260	0.75
74LS266	0.60
74LS273	1.25
74LS279	0.70
74LS280	1.90
74LS283	0.80
74LS290	0.80
74LS292	14.00
74LS293	0.80
74LS295	1.40
74LS297	14.00
74LS298	1.00
74LS299	2.20
74LS321	3.70
74LS322A	3.90
74LS323	3.00
74LS324	3.20
74LS348	2.00
74LS352	1.20
74LS353	1.20
74LS356	2.10
74LS363	1.80
74LS364	1.80
74LS365	0.50
74LS366	0.50
74LS367	0.52
74LS368	0.50
74LS373	0.70
74LS374	0.70
74LS375	0.75
74LS377	1.30
74LS378	0.95
74LS379	1.30
74LS381	4.50
74LS385	3.25
74LS390	0.60
74LS393	1.00
74LS395A	1.00
74LS399	1.40
74LS445	1.80
74LS465	1.20
74LS467	1.20
74LS490	1.50
74LS540	1.00
74LS541	1.00
74LS608	7.00
74LS610	25.00
74LS612	25.00
74LS624	3.50
74LS626	2.25
74LS628	2.25
74LS629	1.25
74LS640	2.00
74LS640-1	3.00
74LS641	1.50
74LS642	2.50
74LS642-1	3.00
74LS643	2.50
74LS643-1	3.00
74LS644	3.50
74LS645	2.00
74LS645-1	4.00
74LS668	0.90
74LS669	0.90
74LS670	1.70
74LS682	2.50
74LS683	3.00
74LS684	3.50
74LS687	3.50
74LS688	3.50
74LS783	16.00

74S SERIES

74S SERIES	
74S00	0.50
74S02	0.50
74S04	0.50
74S05	0.50
74S08	0.50
74S10	0.50
74S11	0.75
74S20	0.50
74S22	0.50
74S30	0.50
74S32	0.60
74S37	0.60
74S38	0.60
74S40	0.50
74S51	0.60
74S64	0.45
74S74	0.70
74S85	5.50
74S86	1.00
74S112	1.50
74S113	1.20
74S114	1.20
74S124	3.00
74S132	1.00
74S133	0.60
74S138	1.80
74S139	1.80
74S140	1.00
74S151	1.50
74S153	1.50
74S157	2.00
74S158	2.00
74S163	3.00
74S169	5.50
74S174	3.00
74S175	3.20
74S188	1.80
74S189	1.80
74S194	3.00
74S195	3.00
74S196	3.50
74S200	4.50
74S201	3.20
74S225	5.20
74S240	4.00
74S241	4.00
74S251	2.50
74S253	2.50
74S258	2.50
74S260	1.00
74S261	3.00
74S283	2.70
74S287	2.25
74S288	2.00
74S289	2.25
74S299	4.50
74S373	4.00
74S374	4.00
74S387	2.25

74C SERIES

74C SERIES	
74C00	0.70
74C04	0.50
74C08	0.70
74C10	0.70
74C14	0.50
74C20	0.70
74C32	1.00
74C42	1.50
74C48	1.50
74C73	1.00
74C74	1.20
74C76	1.00
74C83	2.00
74C85	2.25
74C86	0.50
74C90	1.90
74C93	1.50
74C95	1.60
74C107	1.00
74C150	5.00
74C151	2.00
74C157	2.50
74C160	1.80
74C161	1.80
74C162	1.80
74C163	.80
74C173	1.00
74C174	1.50
74C175	1.50
74C193	1.50
74C194	1.50
74C195	1.50
74C221	2.50
74C244	2.00
74C245	2.25
74C373	2.25
74C374	2.25
74C902	1.20
74C911	9.00
74C912	4.50
74C922	6.00
74C923	6.50
74C925	6.50
74C926	7.50

74ALS SERIES

74ALS SERIES	
74ALS00	0.45
74ALS02	0.45
74ALS04	0.50
74ALS08	0.50
74ALS10	0.45
74ALS20	0.45
74ALS32	0.45
74ALS74	0.70
74ALS138	1.50
74ALS139	1.50
74ALS244	4.00
74ALS245	4.75
74ALS573	2.60
74ALS574	4.50
74ALS580	2.60

4000 SERIES

4000 SERIES	
4000	0.20
4001	0.24
4002	0.25
4006	0.70
4007	0.25
4008	0.60
4009	0.45
4010	0.50
4011	0.24
4012	0.25
4013	0.36
4014	0.60
4015	0.70
4016	0.36
4017	0.55
4018	0.60
4019	0.60
4020	0.80
4021	0.60
4022	0.70
4023	0.30
4024	0.48
4025	0.24
4026	0.90
4027	0.40
4028	0.60
4029	0.75
4030	0.35
4031	1.25
4032	1.00
4033	1.25
4034	2.50
4035	0.70
4036	2.50
4037	1.10
4038	1.00
4040	0.60
4041	0.55
4042	0.50
4043	0.60
4044	0.60
4045	1.00
4046	0.60
4047	0.60
4048	0.55
4049	0.36
4050	0.35
4051	0.65
4052	0.60
4053	0.60
4054	0.80
4055	0.80
4056	0.85
4060	0.70
4063	0.85
4066	0.40
4067	2.30
4068	0.25
4069	0.24
4070	0.24
4071	0.24
4072	0.24
4073	0.24
4075	0.24
4076	0.65
4077	0.25
4078	0.25
4081	0.24
4082	0.25
4085	0.60
4086	0.75
4089	1.20
4093	0.35
4094	0.90
4095	0.95
4096	0.90
4097	2.70
4098	0.75
4099	0.99
4501	0.36
4502	0.55
4503	0.36
4504	0.95
4505	3.60
4506	0.90
4507	0.35
4508	1.20
4510	0.55
4511	0.55
4512	0.55
4513	1.50
4514	1.10
4515	1.10
4516	0.55
4517	2.20
4518	0.48
4519	0.32
4520	0.60
4521	1.15
4522	0.80
4526	0.70
4527	0.80
4528	0.65
4529	1.00
4531	0.75
4532	0.65
4534	3.80
4536	2.50
4538	0.75
4539	0.75
4541	0.90
4543	0.70
4551	1.00
4553	2.40
4555	0.36
4556	0.50
4557	2.40
4560	1.40
4566	1.40
4568	2.40
4569	1.70
4572	0.45
4583	0.90
4584	0.48
4585	0.60
4724	1.50
14411	7.50
14412	7.50
14416	3.00
14419	2.60
14490	4.20
14495	4.50
145000	6.50
14599	2.00
22100	3.50
22101	7.00
22102	7.00
40014	0.48
40085	1.20
40097	0.36
40098	0.40
40100	1.50
40101	1.25
40102	1.30
40103	2.00
40104	1.20
40105	1.50
40106	0.48
40107	0.55
40108	3.20
40109	0.80
40110	2.25
40114	2.25
40147	2.80
40163	1.00
40173	1.20
40174	1.00
40175	1.00
40192	1.00
40193	1.00
40194	1.00
40244	1.50
40245	1.50
40257	1.80
40373	1.80
40374	1.80
80C95	0.75
80C97	0.75
80C98	0.75

LINEAR ICs

AD7581	12.00
ADC0808	11.90
AM7910DC	25.00
AN103	2.00
AN-1-5050	1.00
AY-3-1350	3.50
AY-3-8910	4.90
AY-3-8912	5.00
CA3019A	1.00
CA3020	3.50
CA3028A	1.10
CA3046	0.70
CA3059	3.25
CA3060	3.50
CA3080E	0.70
CA3085	1.50
CA3086	0.60
CA3089E	2.50
CA3090AQ	3.75
CA3130E	0.90
CA3130T	1.30
CA3140E	0.45
CA3140T	1.00
CA3146	2.25
CA3160E	1.50
CA3161E	2.00
CA3162E	6.00
CA3189E	2.70
CA3240E	1.50
CA3280G	3.00
D7002	6.00
DAC1408-8	3.00
DAC0800	3.00
DAC0808	3.00
DG308	3.00
HA1366	1.90
ICL7106	6.75
ICL7611	0.95
ICL7650	4.00
ICL7660	2.50
ICL8038	4.00
ICM7555	0.90
ICM7556	1.40
LC7120	3.00
LC7130	3.00
LC7131	3.50
LC7137	3.50
LF347	1.20
LF351	0.60
LF353	0.90
LF355	0.90
LF356N	1.10
LF357	1.00
LF398	4.00
LM10CLH	4.50
LM301A	0.30
LM307	0.45
LM308CN	0.75
LM310	2.25
LM311	0.60
LM318	1.50
LM319	1.80
LM324	0.45
LM334Z	1.15
LM335Z	1.30
LM336	1.60
LM339	0.40
LM348	0.60
LM358P	0.50
LM377	3.00
LM380N-8	1.50
LM380N	1.50
LM381AN	1.70
LM381N	3.00
LM383	3.25
LM384	2.20
LM386N-1	1.00
LM387	2.70
LM391	1.80
LM392N	1.10
LM393	0.85
LM394CH	4.00
LM709	0.35
LM710	0.48
LM711	1.00
LM723	0.60
LM725CN	3.00
LM733	0.65
LM741	0.22
LM7747	0.70
LM748	0.30
LM1011	4.80
LM1014	1.50
LM1801	3.00
LM1830	2.50
LM1871	3.00
LM1872	3.00
LM1886	6.00
LM1889	4.50
LM2917	3.00
LM3302	0.90
LM3900	0.80
LM3909	1.00
LM3911	1.80
LM3914	3.50
LM3915	3.40
LM3916	3.40
LM13600	1.50
M51513L	2.30
M51516L	4.50
MB3712	2.00
MC1310P	1.50
1413	0.75
MC1458	0.45
MC1495	3.00
MC1496	0.70
MC3340P	2.00
MC3401	0.70
MC3403	0.65
MF10CN	4.10
MK50240	9.00
ML902	5.00
ML922	4.00
MM6221A	3.00
NE529	2.20
NE531	1.20
NE544	1.90
NE555	0.22
NE556	0.60
NE564	4.00
NE565	1.20
NE566	1.50
NE567	1.25
NE570	4.00
NE571	3.00
NE592	0.90
NE5532P	1.50
NE5533P	1.60
NE5534P	1.20
NE5534AP	1.50
OP-07EP	3.50
PLL02A	5.00
RC4136	0.55
RC4151	2.00
RC4195	1.50
RC4558	0.55
S50240	9.00
SAA1900	16.00
SFF96364	8.00
SL490	3.00
SN76013N	3.00
SN76023N	3.00
SN76033N	3.00
SN76115N	2.15
SN76489	4.00
SN76495	4.00
SN76660	1.20
SPO256AL2	7.00
SP8515	7.50
TA7120	1.20
TA7130	1.40
TA7204	1.50
TA7205	0.90
TA7222	1.50
TA7310	1.50
TBA231	1.20
TBA800	0.80
TBA810	0.90
TBA20	0.80
TBA820M	0.75
TBA920	2.00
TBA950	2.25
TC9109	5.00
TCA210	3.50
TCA220	3.50
TCA270	3.50
TCA940	1.75
TDA1004A	5.00
TDA1010	2.25
TDA1022	4.50
TDA1024	1.10
TDA1170S	3.00
TDA2002	3.25
TDA2003	1.90
TDA2004	2.40
TDA2006	3.20
TDA2020	3.20
TDA2030	2.50
TDA2593	5.00
TDA2653	7.00
TDA3560	7.50
TDA3810	7.50
TDA7000	3.50
TEA1002	7.00
TL061CP	0.40
TL062	0.60
TL064	0.90
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The lithium cell users guide

The lithium cell used today has done almost as much to change the nature of electronics as did the advent of the point contact transistor.

by N. HOUSLIP

In the last decade lithium cells have matured from a crude, potentially hazardous device with no history of reliable operation, except under rather unrealistic laboratory conditions. Indeed, there were a number of rather frightening events that led indirectly to a ban, still in effect today, on cells with a lithium content greater than 0.5gram being carried on passenger aircraft. This size cell nevertheless does have a theoretical capacity of approximately 1.5Ah and is capable of supporting almost any reasonable amount of low power memory.

The would-be user of a lithium cell is faced with a bewildering choice of couples, so first a word about how to choose the correct cell. There are four important factors that must be known before the search for the cell can begin:

- magnitude and nature of the discharge current
- duration of the current
- maximum voltage that the circuit can withstand
- minimum voltage at which the circuit will work reliably.

If the discharge current is simple, for example an unchanging resistive load, the cell choice is easier than if it were a complex load with long periods of quiescent current and intermittent high peaks. Except for rough battery size determination, it is of no use whatever to calculate average current. The effect of peak currents that exceed the normal continuous rating of the cell can only be calculated by working out the relative discharges at each current level and the amount of time it is on for.

It is sound practice to consult the manufacturer as soon as possible in the design cycle. This will invariably lead to the nearest suitable cell size being specified, thus preventing the embarrassing condition in which some designers find themselves, i.e. of having only about 60% of the space needed for the battery available. Many have found that a quart of battery will not fit into a pint-size battery compartment.

It is wise to examine the discharge current to see if it necessitates the use of parallel

THE LITHIUM COUPLES

1. Solid Cathode:	low rate, 5+ year shelf life
manganese dioxide	3.0V nom.
polycarbon monofluoride	3.0V nom.
iodine	2.8V nom.
chromdioxide	3.0V nom.
2. Liquid cathode:	medium rate unless wound type
thionyl chloride	3.6V nom.
3. Gaseous cathode:	high rate, 10-year shelf life
sulphur dioxide	2.8V nom.
4. Liquid cathode:	highest rate, wound electrode
sulphuryl chloride	3.9V nom.

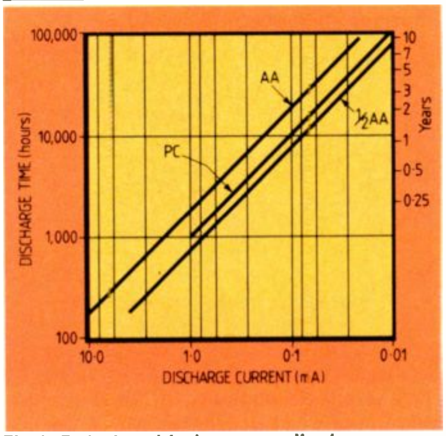


Fig.1. Relationship between discharge current and discharge time is not simple: the self-discharge component is varible adn related to discharge current.

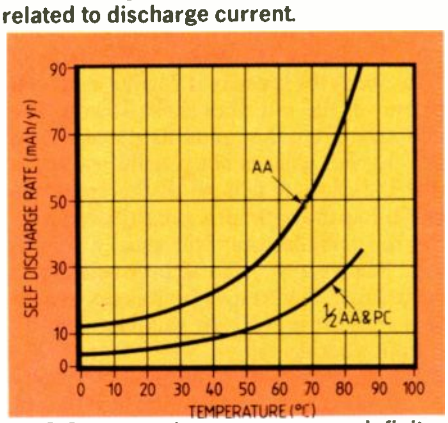


Fig.2. Storage at low temperatures definitely improves shelf life. Keeping cells under refrigeration, for instance, can reduce self-discharge by 20% of the room-temperature rate.

cells. This arrangement should always include protection diodes to prevent circulating currents should one cell in a string fail. The cell manufacturer will always advise on this. Consideration of the voltage levels is needed too. All cells state a nominal voltage but the actual level under load may be as much as 10% lower.

The cell type choice will be from one of two major groups, with either solid or liquid cathode. The solid kind generally contains only low current types that are usually only closed with a crimped elastomer seal that is probably the major limiting factor to life in memory back-up applications. This limitation is brought about by the loss of components of the electrolyte through the seal and the ingress of poisons that interfere with cell action. The most important use of the solid cathode type is in heart pacemaker cells, but this always utilises a glass-to-metal seal for utmost reliability.

For medium-rate duty the liquid or gaseous cathode bobbin type are extremely popular but become very limited by their internal resistance above this. For high rates, such as would be demanded by a portable mobile radio on transmit for instance, the choice is confined to the liquid or gaseous cathode with spirally wound electrodes. These cells always have fully hermetic construction with glass-to-metal seals at the terminals and often laser-welded seams. The mechanism that gives all lithium cells their ability to stand unused for many years is an anode passivation process that causes an insulating layer to build up on the lithium surface. This prevents the spurious chemical action that depletes the cell's capacity. Fig.1 shows the relationship between useful discharge current and time, while Fig.2 shows how the self-discharge is related to temperature. The loss of capacity, albeit small, manifests itself as an inability to deliver current to the load and is for the most part caused by the spurious electrochemical action in the cell that is not stopped by the passivation layer and is strongly temperature dependent. It follows that as the amount of self-discharge is approximately doubled for every 20°C rise, storage at low temperatures will prolong the life of the cell.

In some cells this passivation can cause a temporary depression in terminal voltage at the moment of demand of anything but small currents. To overcome this, cells with a large lithium surface area must be used for these applications. Note that as the rate capability goes up the shelf life limitation is more severe due to the larger available site for the spurious action and room temperature storage without severe loss of capacity is seldom possible for more than two to three years. Low temperature storage is an absolute necessity to ensure long operational life after prolonged storage. This action affects all primary and secondary cells to a greater or lesser extent. A useful tip for those of us who purchase batteries for home and personal equipment is to keep them in the refrigerator in sealed bags, this will ensure that there will be minimal loss of capacity, not always the case in the shop, especially if the sun shines on the stock!

Always follow the manufacturer's recommendations as to use and storage. The range of operational temperatures vary with the chemistry and are by no means standard. Upper limits can be from 72 to 150°C; be wary of operation above the recommended temperature for the particular cell as its internal pressure characteristic may not be suitable. The ultimate limit is the melting point of lithium at 186°C. The molten lithium will then combine with cell constituents and an explosion is inevitable.

CONDITIONS TO AVOID

In normal use, within the design parameters of the cell no hazard is present, but there are certain conditions that must be avoided: short circuits, recharging of primary cells, and disposal by incineration. The most likely problem area is reverse charging of a cell or cells caused by the failure of protection diodes in a memory back-up application. The normal mode of failure is for the diode to fail and short circuit imposing a higher reverse current on the cell. It is good practice to include a series resistor to limit the current under this condition to not more than 1μA per milliampere of cell capacity. An alternative scheme, suggested by Underwriters Laboratories, is to include a second diode in the series network, but this can sometimes result in a greater than desired voltage drop in the circuit.

The result of such abuse is leakage or rupture of the cell if the current is high enough. In most of these cases the cell is contained in the equipment and damage to the p.c.b. and its associated components is the usual outcome. Cells of the high-rate capability type must be handled with great care: inadvertent short circuit can cause trouble even if only the rupture of internal fuses, rendering the cell useless. An earthed soldering iron and a conductive bench top have been known to cause mysterious cell fuse failure. Antistatic mats and packing used for the protection of cmos integrated circuits can significantly reduce capacity too, especially if the cell terminations are inserted into the conductive foam for any length of time.

Rate dependency is a source of some

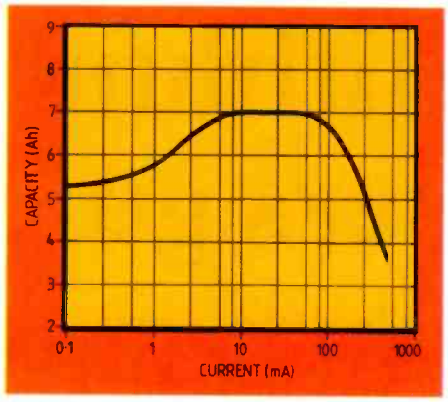


Fig.3. Capacity delivered to load is infuenced by discharge current in this C-size cell. Drain rate's above and below optimum will lead to inefficient use of cells.

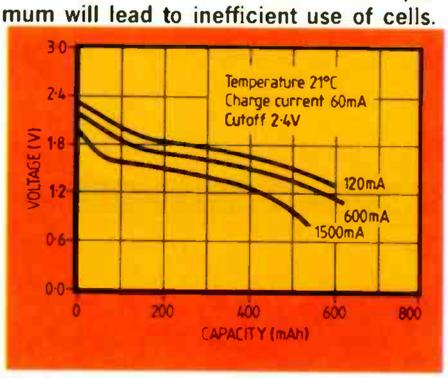


Fig.4. Determination of available capacity is possible from the rechargeable lithum molecell by monitoring its terminal voltage. (Molicell AA size, recommended charging current 60mA to 2.4V cut off).

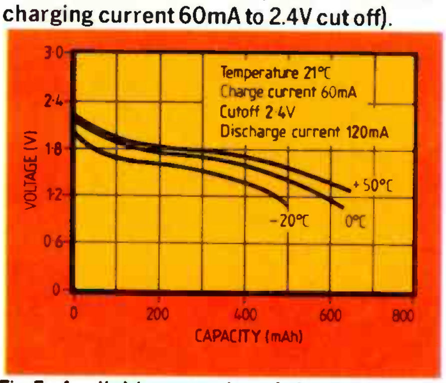


Fig.5. Available capacity of the rechargeable lithium cell decreases with lowering of operating temperature (Molicell AA).

confusion. A study of Fig.3 will show that the returned capacity to the load varies greatly with the discharge current. At the limits of 10 to 50mA the capacity is 7Ah but it falls off sharply as the rate goes above 100mA. The optimization of the cell to its stated duty is evident, but what is not usually realised is that the capacity falls off as the drain rate falls below the optimum. Consultation with the cell manufacturer will usually resolve this. Beware any manufacturer who has a cell claimed to be universal: it is unlikely to be a success, unless you stumble upon its optimum accidentally.

It is also necessary to derate cell capacity by certain factors for operation at extremes of temperature and after storage at temperatures above 20°C. For example, storage at 50°C for a year (see Fig.4) will require derating to 85% of the rate-adjusted capacity. If it is now required to operate the cell at −10°C further derating to 75% of that capacity is required. For a cell of 7Ah discharged at its optimum of 50mA then it is necessary to derate 7Ah to 85% then 75% or 4.46Ah.

These deratings are necessary for all lithium cells; all makes need to be so considered despite any claims to the contrary.

THE FUTURE

With the ever-decreasing current demand of cmos devices the trend is to ever smaller cells with usable capacities of less than 200mAh capable of supporting 8×8K of pure static for more than five years. These are finding popular application in such diverse applications as memory diallers, electricity metering, and data storage of the type that might be encountered in point-of-sale and banking terminals.

Rechargeable cells are now available, the most interesting couple being the lithium molybdenum disulphide cell which offers 600mAh capacity at 600mA discharge with good cycle life. As this cell has a sloping discharge voltage characteristic (Fig.4) it opens up the possibility of easy determination of the remaining capacity with a simple circuit. The first application of this cell in the consumer field will be a photoflash gun with a push-to-test function that indicates the number of flashes remaining before recharge is needed on a bank of leds. Figure 5 shows the relationship between capacity and discharge rate.

A rechargeable lithium carbon cell is just becoming available but is characterised for low current memory back-up applications with very shallow discharge. The cell has a capacity of 1mAh with life of more than 2000 cycles and is ideally suited to consumer applications such as solar powered clocks, calculators, toys and display devices.

There are devices appearing on the market which are the next generation of combination of silicon and lithium in the same package. The non-volatile memory using low power cmos and a shirt-button-size cell is familiar to all but what of a completely non-volatile microprocessor that saves all of its register contents, data and program memories in the event of power failure, and can continue where it left off when powered up? These and many other similar devices that may challenge even the traditional mass-memory storage devices in use today are promised by manufacturers of embedded lithium technology.

Research into lithium cells of sufficient capacity that could be printed onto circuit boards is under way, thus the self-powered integrated circuit may only be just around the corner. Imagine the impact of this technology on small personal computers and other instruments. The use of this type of energy source together with liquid crystal displays driven by ultra low power cmos devices will open up a whole new vista for personal data and communications devices.

Nic Houslip is a director of Suvicon Ltd, who represent four overseas makers of lithium cells, and European sales manager for Dallas Semiconductor.

New cathode material for high energy lithium batteries

Recent research shows that nickel phosphorus trisulphide could aid the commercial development of small rechargeable lithium cells.

by B.A. NEVETT

Over the last ten years we have carried out research aimed at the development of a rechargeable (secondary) lithium cell. Recent successes by various research groups have alleviated problems associated with repeated charge/discharge cycling of the lithium anode and make our work particularly timely.

The variety of materials that are potentially suitable for use as lithium cell cathodes is large. In practice, they are usually limited to metal oxides, metal sulphides or related substances. An important feature which the useful metal oxides and sulphides share is their crystal structure which can be of either two types.

In the first type, the atoms are arranged in a three-dimensional network which provides a series of tunnels through the structure. In the second, the structure is made of layers of atoms grouped together in slabs which are stacked on top of one another. A small gap known as the van der Waals gap separates the adjacent slabs. Both types of material can function as battery cathodes because they allow lithium ions to be inserted into the tunnels or the van der Waals gaps.

Our work at Brighton Polytechnic has concentrated on a series of layer compounds, the metal phosphorus trisulphides, MPS_3, where M can be iron, cobalt nickel, copper or zinc. At present, nickel phosphorus trisulphide shows the best promise for development as a cathode material.

Traditionally, the way of making $NiPS_3$ and the other similar compounds, has involved the prolonged heating of mixtures of reactants at high temperatures. One of our most significant discoveries has been of a quick low temperature method which produces $NiPS_3$ in a form that gives superior electrochemical performance compared with the high temperature product.

The process of discharging the lithium cell is illustrated in the accompanying diagram and can be represented by

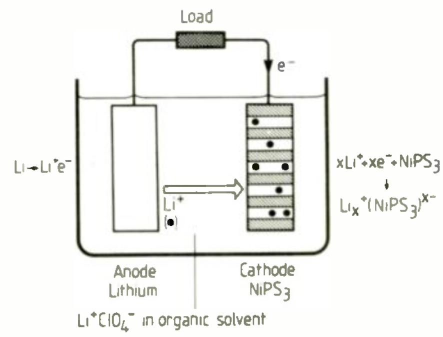
$$xLi^+ + xe^- + NiPS_3 \rightarrow Li^+NiPS_3^{x-}$$

where $0 > x \geq 1.5$. The insertion of lithium ions between the layers of $NiPS_3$ is a reversible process so that the cell can be recharged by simply applying a current in the reverse direction to drive the lithium back out again.

Using a liquid electrolyte of lithium perchlorate, $LiClO_4$, dissolved in an organic solvent of propylene carbonate, this type of cell produces an e.m.f. of >2V over much of its discharge range, with current densities at the cathode ranging from $10\mu Acm^{-2}$ to $1mAcm^{-2}$. We are currently investigating other electrolytes with a view to improving these figures.

The use of a Li_xNiPS_3/Li cell with a solid polymeric electrolyte has recently been demonstrated in collaboration with Dr A. Hooper's research group at AERE, Harwell. This cell operated at 120°C and gave an e.m.f. of about 1.5V with a current density of $10\mu Acm^{-2}$. Other aspects of our work concern studies of the relationship between preparative conditions for $NiPS_3$, a number of its physical properties such as particle size and surface area, and its electrochemical performance. The aim here again is to optimize the performance of the cell.

One of the most interesting features of the $NiPS_3$ cathode material is that there is a negligible change in volume of the electrode during the charge/discharge cycle. This, coupled with the fact that it adheres well to metal foil or gauze with the aid of a suitable binder, suggests that it should be possible to construct cells with very thin electrodes and so produce miniature batteries. Such cells might find use in electronic circuit boards and might even ultimately be printed onto chips as a way of preserving volatile memory devices.



This work is conducted with the financial assistance of the Science and Engineering Research Council and the British Technology Group.

Dr Nevett is in the department of physical sciences at Brighton Polytechnic.

Polymer battery progress

Work on lithium batteries made of synthetic materials began a decade ago when it was discovered that polyacetylen had a similar electrical conductivity to that of metal. Unfortunately, this material proved to be electrically unstable and consequently not suitable for use in a battery made of synthetic material or polymers.

Further development of conductive polymeric materials lead to the discovery of polypryrrol, which remains unchanged in air as well as in many other organic electrolytes. This characteristic, together with the fact that polyprrol can be easily processed into foil, has made it possible to develop a cell which could be mass produced.

Polypyrrol is suitable for positive electrodes; combined with a lithium electrode and an organic electrolyte, a cell system becomes possible which, its makers say, marks "a signficant milestone in polymer battery technology."

Though the polymer battery will never replace the lead acid battery, it could certainly challenge other rechareable battery systems for use in portable electric and electronic equipment.

The first cells from a joint research programme of Varta and BASF represent a big step in the a new battery technology, though Varta admit there is still a long way to go. Much research and development work has still to be carried out before the laboratory samples can be considered viable, but results so far show that a synthetic battery is possible in the future. Rechargeable laboratory cells of the R6/AA size, as well as the flexible flat batteries in postcard size, have already reached energy densities that can be compared favourably with NiCd batteries of similar weight. Under cyclic charge/discharge tests, some 100 cycles have been reached at a 100% depth of discharge, with cells exhibiting an average voltage at the 20h discharge rate of about 3V, varying between 2 and 3.9V.

Much still needs to be done. Energy density has to be improved, as does the number of possible charges and discharges. According to Varta's commercial director, Robin Cloke, such development targets could take several years to achieve.

APPLICATIONS SUMMARY

Video line selector

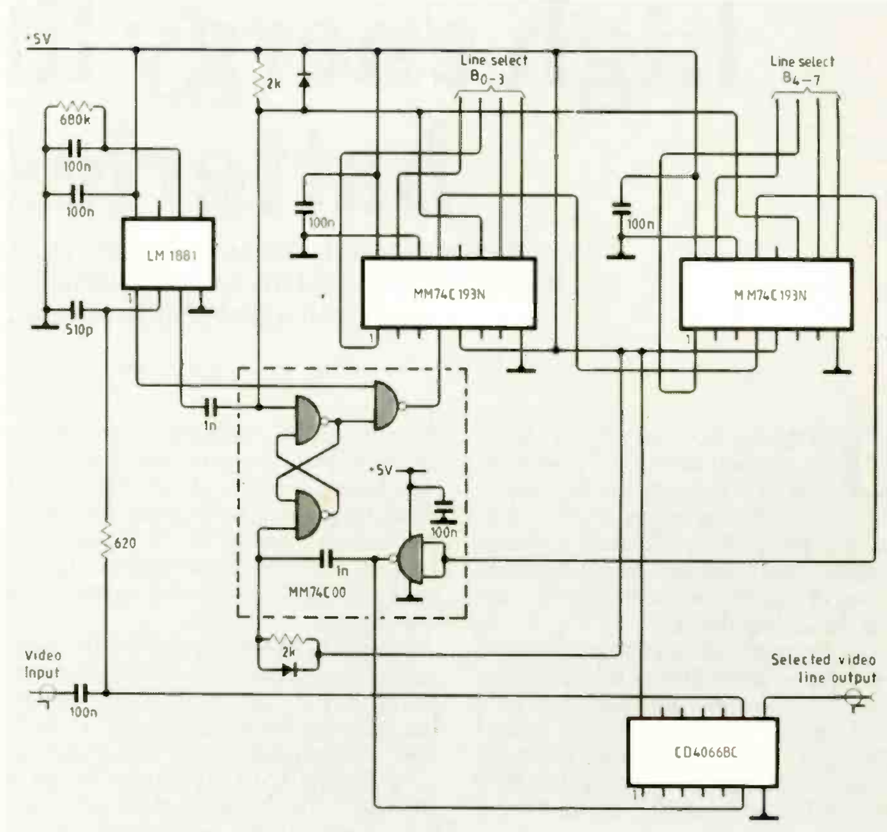
A new sync-separator i.c. is used here as the basis of a circuit for selecting one line from a field or frame of video input. The National Semiconductor LM1881extracts timing information including composite and vertical sync., burst/back-porch timing and odd/even field information from a standard 0.5 to 2V NTSC video signal and provides sync. separation from faster non-standard video signals.

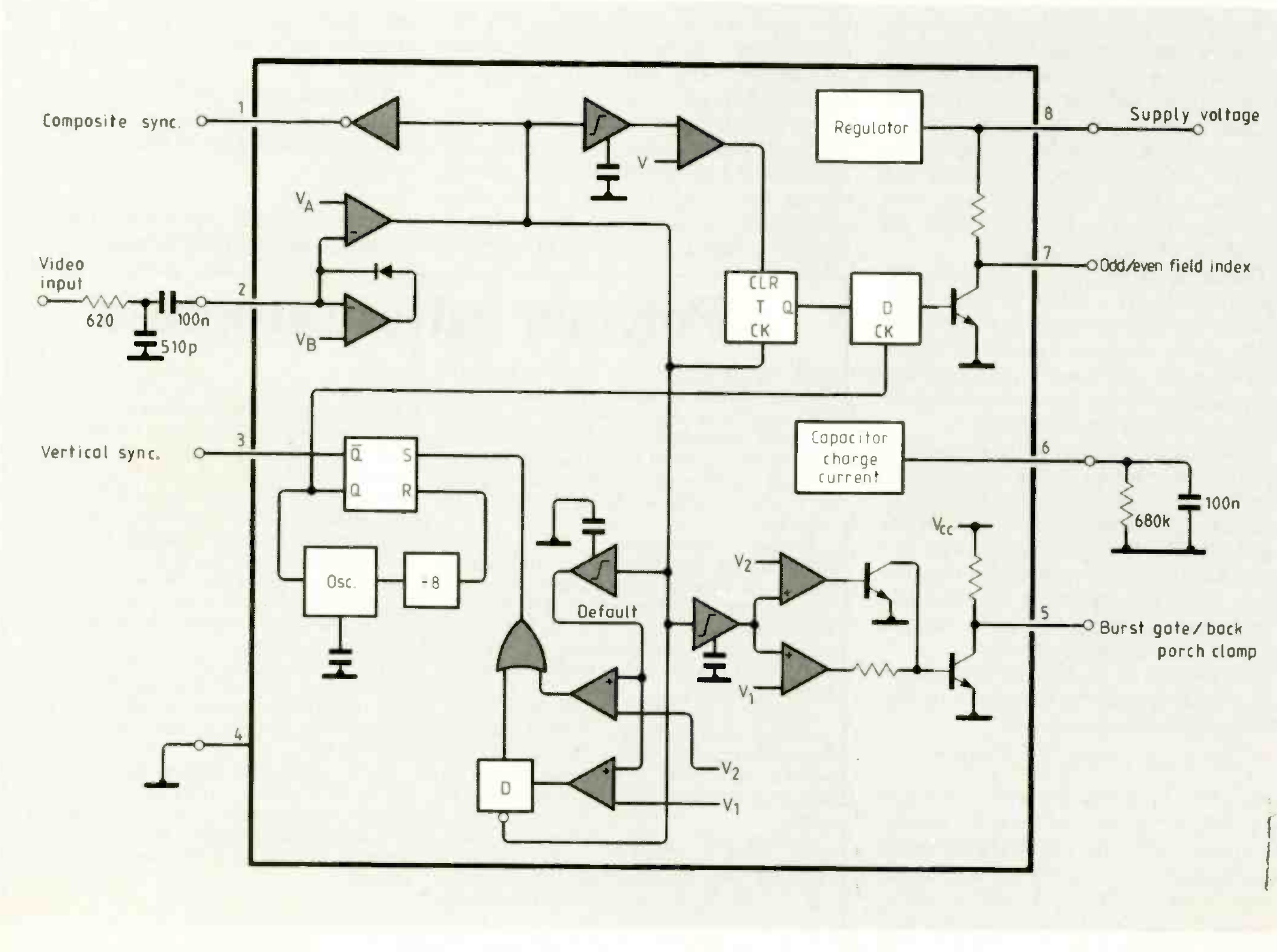
In this line selector circuit, part of the 1881 preliminary data sheet, code for the select imputs is the binary equivalent of the required line minus two. On the falling edge of the 1881 vertical pulse this line-select code is loaded into the 193 counters and the Nand counting latch is started.

Composite sync. transitions are counted using the 193 borrow outputs and the final borrow output pulse turns on the analogue switch during the desired line. Resetting of the start-count latch occurs on the falling edge of the final borrow thereby terminating counting.

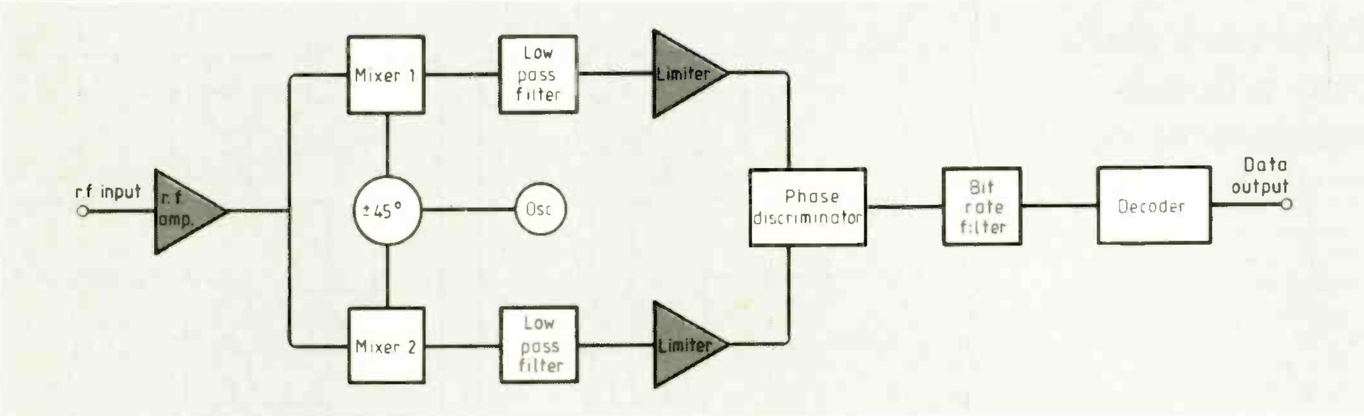
Also included in the data sheet is a circuit for multiple contiguous line selection with black-level restoration.

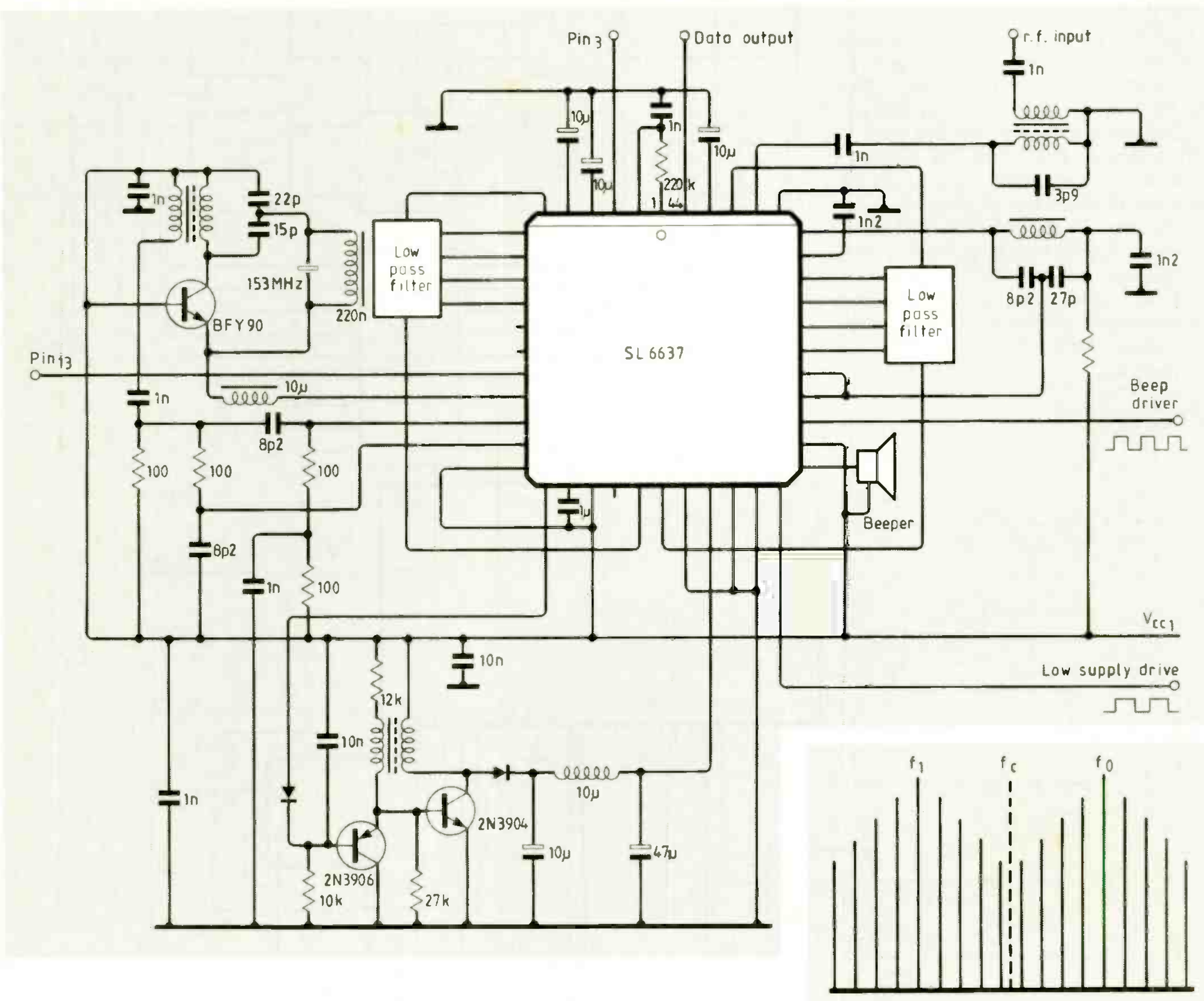
National Semiconductor
The Maple, Kembrey Park, Swindon, Wiltshire SN2 6UT
Tel. 0793 614141





APPLICATIONS SUMMARY





Direct-conversion f.s.k. receiver

Most of the functions required to make a radio pager are contained in the Plessey SL6637 i.c. The low-power device is a direct-conversion f.s.k. receiver capable of 1200 bit/s output and suitable for use in radio-data receivers, ultrasonic direction indicators and security systems as well as radio pagers.

This design from the SL6637 data/ application sheet is a low-power pager. Radio-frequency f.s.k. input is amplified for feeding to the mixers. Phase shift in the quadrature local oscillator is produced using an RC network; frequency of the oscillator is nominally equal to the carrier.

Mixer outputs at baseband pass through active filters which provide selectivity. Theoretically, a receiver using zero i.f. has infinite adjacent-channel rejection.

Audio-frequency filter output is amplified in the two limiters then fed to the detector. Sensitivity is maximized by arranging a number of detectors to provide phase comparison on four pairs of signal edges. Detected output finally passes through a bit-rate filter and second limiter to produce the data output.

Plessey Semiconductors
Cheney Manor, Swindon, Wiltshire SN2 2QW
Tel. 0793 36251

APPLICATIONS SUMMARY

Dual-port static ram reduces component count

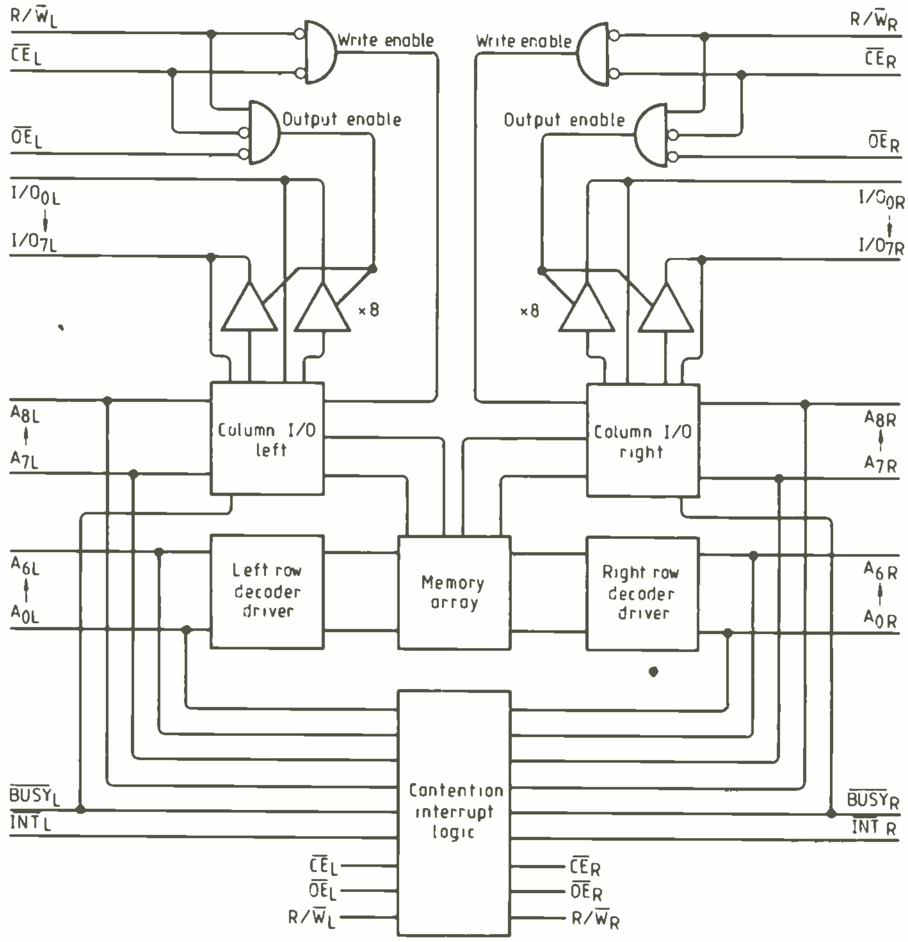
Memory often needs to be accessed by more than one source. In typical 6845 c.r.t. controller circuits for example, screen memory needs to be accessed by both the processor and the c.r.t. controller.

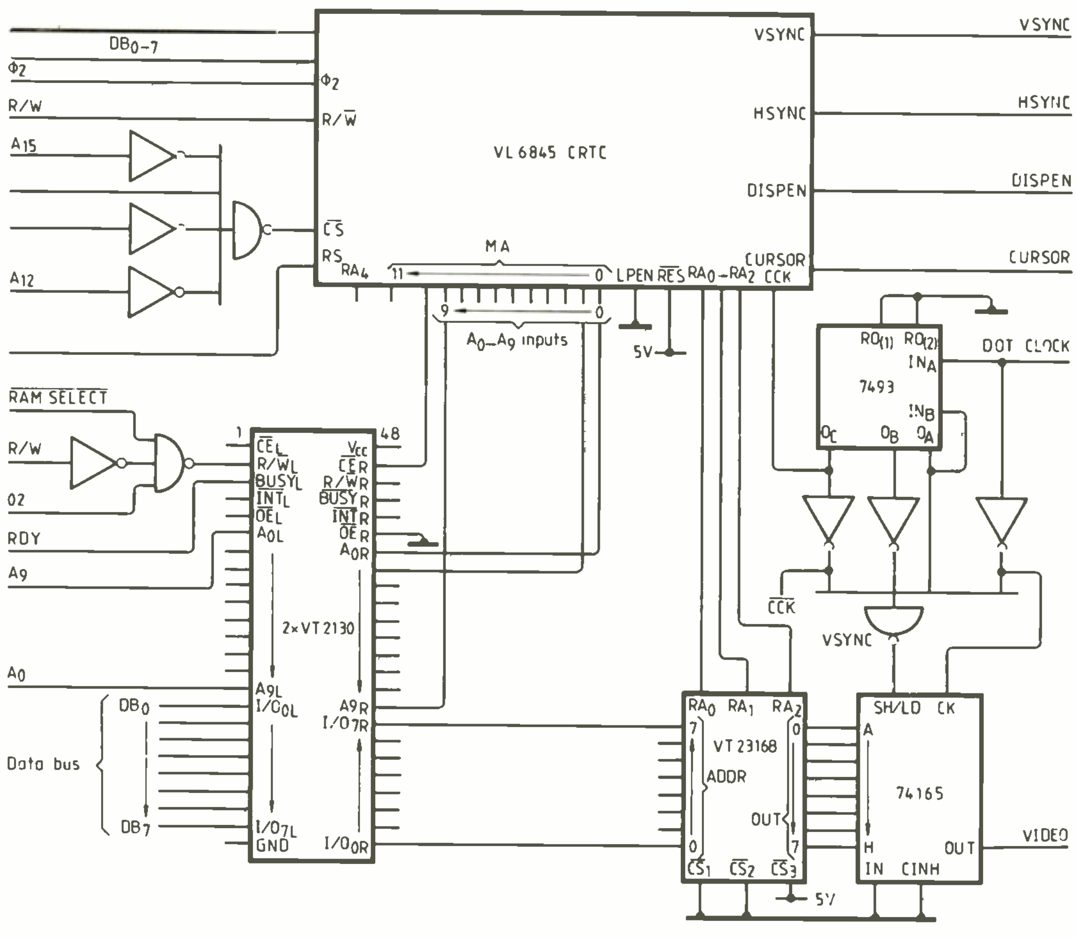
In such situations, multiplexing i.cs are required to switch ram address, data and control buses between the two sources. Logic is also required to make sure that information is not lost if both sources try to access the memory at the same time.

Dual-port rams have two sets of address, data and control lines so the need for external multiplexing i.cs is removed. They also have outputs indicating when the ram is being accessed through the other port.

This design from VLSI Technology's VT2130/2131 application note is a c.r.t. controller in which the microprocessor has priority over the controller for ram accesses. In the 30-page note there is also a block diagram for a similar circuit but with c.r.t. controller priority and there are several microprocessor interfaces. General notes on using dual-port rams are included.

VLSI Technology
Midsummer House, Midsummer Boulevard,
Milton Keynes MK9 3BN
Tel. 0908 670027





THE JOURNAL FOR PROFESSIONAL ENGINEERS

ELECTRONICS & WIRELESS WORLD

Editorial Feature List

JULY 1987

Computer-aided design. There is a great deal of hardware and software dedicated to the design of electronic equipment, from printed circuit boards to integrated circuits. We examine what is now available.

AUGUST 1987

Short-haul optical-fibre data communication is an essential part of modern communications systems. This feature presents an overview of the techniques employed and the hardware available.

SEPTEMBER 1987

Microwave semiconductor devices. These specialised components retain an air of mystery for many engineers. We present a feature on the physics of these devices and characterize the types now in use.

OCTOBER 1987

R.f signal generators. The modern sig.gen is a far cry from those in use even ten years ago. This feature examines new design techniques, facilities available, and the characteristics of a wide range of instruments, from a few hundred kilo hertz to the gigahertz end of the r.f. spectrum.

For further advertising details please ring Martin Perry on: 661 8641

Does your coupling coefficient matter?

Making inductively-coupled energy less sensitive to coil separation.

TOM IVALL

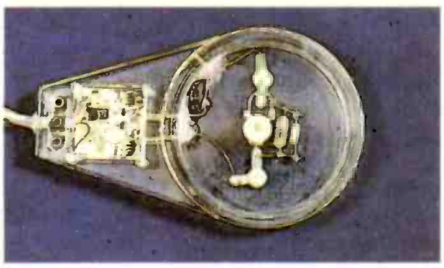
A little-known possibly hitherto unknown, fundamental property of inductively coupled oscillating circuits is being investigated by the Medical Research Council. It is being utilized to improve the operational flexibility of surgically implanted nerve stimulators. At the MRC's Neurological Prostheses Unit in South London these microelectronic implanted stimulators are used to activate nerve fibres which, as a result of some disease or injury, are no longer in use. They give back the patient some degree of voluntary control over limbs or organs which have become paralysed.

The MRC implanted stimulators are energized by electromagnetic induction. Of course, the idea is to avoid the obvious inconvenience and health hazards of making direct electrical connections by wires passing through the skin. Typically, a receiver coil is implanted permanently under the patient's skin by surgery, while an external, manipulable transmitter coil is placed on the patient's body, or attached to it, as close as possible to the subcutaneous receiver[1,2]. Radio frequencies are used for energy transmission (in the region of 3MHz) to allow the coils to have low inductances and therefore only a few turns, so that they can be made conveniently small, light and robust and reliable in operation.

This kind of system – and probably inductive links in other applications outside of medicine – should be operationally flexible in tolerating some uncertainty in the working distance between the two coils. More precisely, variations in the working distance, and therefore coupling coefficient, between the two coils should not affect the amount of electromagnetic energy coupled into the receiver too drastically. P.E.K. Donaldson, of the MRC Unit, has found both analytically and experimentally a new way of achieving such insensitivity to coil separation in certain conditions[3].

The particular 'separation-insensitive link' Donaldson has designed is a combination of self-oscillating series-resonant transmitter and series-resonant receiver. He has discovered that the energy transferred to the receiver is independent of the mutual induction coupling coefficient, k, over a useful range from $k=1/Q_R$ (where Q_R is the Q-factor of the receiver resonant circuit) up to the theoretically perfect coupling of $k=1$.

To give some experimental results first, Fig 1 shows equipotential curves in terms of



Pulsed series oscillator. Coil diameter is 70mm. The negative resistance/voltage limiter is built as a thick-film hybrid microcircuit on a substrate measuring 25mm square.

Implantable receiver, also in thick-film before encapsulation in silicone rubber. Diameter is 43mm. Used with the oscillator shown left, the receiver delivers 30V into 390 ohms.

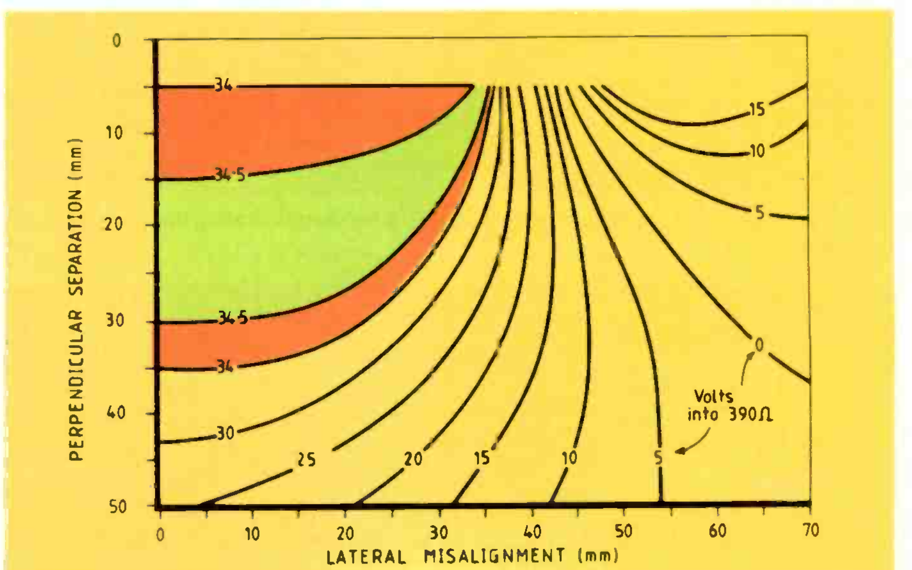


Fig.1. Results from a separation-insensitive link. The curves are plots of constant voltage across the receiver load. Highlighted area at 34V shows the operating region for maximum separation and misalignment.

volts across a 390Ω load in the receiver. Measurements were made using a 70mm diameter transmitter coil and a 35mm diameter receiver coil. As mentioned above, both coils are in series-resonant LC tuned circuits, and the transmitter is a self-oscillating arrangement. Each curve is a plot of constant voltage across the load for different combinations of lateral and perpendicular (coaxial) separation between the coils. Each combination, of course, can represent a particular position in space of a movable transmitter coil relative to a fixed receiver coil or vice versa.

It can be seen from the shaded areas in Fig.1 that a receiver output voltage of 34V can be maintained when one coil is moved around within a substantial volume of space relative to the other. In fact the volume inside which the output voltage is constant within 1% is as large as 90 cm^3 (for example, a cube of 4.5cm sides). In obtaining the separation-insensitivity conditions shown by the shaded areas the coupling coefficient k varies over the range 0.03 to 0.12.

Intuitively, one can picture the mechanism responsible for this effect as something resulting from oscillator pulling. Imagine the two coils being gradually moved towards each other. If the transmitter oscillator were not pulled by the presence of the coupled receiver and remained oscillating at a constant frequency, the output of the receiver would simply continue to rise as the two coils came closer and closer together. But the increasing proximity of the receiver circuit does make the transmitter frequency change, so that the receiver resonant circuit becomes progressively de-tuned relative to this frequency. With Donaldson's series-resonant circuitry this happens at a certain rate at which the receiver's falling response, due to the de-tuning, just compensates for its otherwise rising response due to the increasing coupling. As a result of this compensatory process the receiver output remains constant, and thus independent of k, over a certain range of coupling variation.

A full theoretical analysis of the circuit conditions giving receiver output voltages independent of k has recently been published by Donaldson in a formal paper[4]. The present article will therefore simply outline the circuit property discovered – or perhaps, to be cautious, re-discovered – through a description of the inductive link circuitry and a summary of the mathematical analysis.

INDUCTIVE LINK CIRCUIT ANALYSIS

Figure 2 shows one practical circuit which demonstrates the insensitivity to coil separation. Other arrangements, with received powers ranging from 200mW to 10W, have been built by the MRC Unit. As can be seen, the transmitter is a series-resonant oscillator circuit with gain from two inverter amplifiers. Positive feedback is provided by the 1Ω resistor in series with the LC tuned circuit: the voltage developed across this from the high current at resonance is fed back to the input of the first amplifier. The coil of the series-resonant circuit is inductively coupled to another series-resonant tuned circuit in the receiver. The reason for using a 3t:10t transformer in the receiver will be explained later.

An analytical version of the two inductively coupled tuned circuits is given in Fig.3. On the left is a block representing the negative resistance provided by the amplifier and positive feedback arrangement. For both transmitter and receiver circuits to tune separately at the same resonant frequency, ω_0, then $L_1C_1=L_2C_2$. Resistances R_1 and R_2 are the resistances of the transmitter and receiver circuits respectively.

Readers without a textbook of a.c. theory handy may need a reminder on k, the coupling coefficient dependent on the mutual inductance M shared between L_1 and L_2. This is a number measuring the extent to which the magnetic fluxes of the two coils

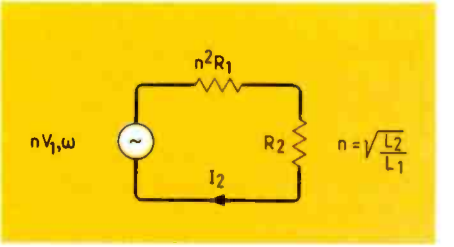


Fig.4. The analytical circuit in Fig.3 reduces to this simple equivalent circuit when coupling coefficient k is greater than $1/Q_2$.

link with the turns of the opposite coils. The coefficient is given by $k=M/\sqrt{L_1L_2}$. Thus perfect coupling, with complete linkage and all the inductance mutual, means that k = 1, while anything less makes k a number between 0 and 1.

The mathematical analysis in reference 4 starts by examining the effects of coupling coefficient on the frequency of oscillation, ω. After setting out the circuit equations in terms of L, M, C, R, Q and Z, and remembering that the uncoupled resonance frequency is ω_0, the analysis shows than when k is less than $1/Q_2$ the oscillation frequency is the same as the resonance frequency, $\omega=\omega_0$. But when the coupling is increased and $k>1/Q_2$ the oscillation frequency starts to change and departs from ω_0. The analysis shows that when $k>1/Q_2$

$$\left(\frac{\omega_0}{\omega}\right)^2=1\pm\sqrt{\frac{Q_2^2k^2-1}{Q_2^2}}.$$

If the term $Q_2^2K^2$ in this is much greater than 1, the expression reduces to a simpler one of $\omega=\omega_0\sqrt{1\pm k}$. In both of these expressions the '±' indicates that there are two possible stable values for ω.

Incidentally, the author relates this behavior to the familiar 'double humping' or twin peaks given by an overcoupled transformer to achieve, for example, a bandpass filter characteristic in i.f. amplifiers. He draws attention to the fact that the twin peaks remain quite constant in height despite variations in the degree of overcoupling, but says he is not aware that this has ever been exploited in self-oscillating systems. Poulsen with his tuned arc c.w. transmitter of 1903 might well have hit upon it, especially as he was struggling with problems of frequency and amplitude instability, but apparently did not do so.

After dealing with frequency, the analysis of Fig.3 continues by formulating the gain of the inductive link for different coupling

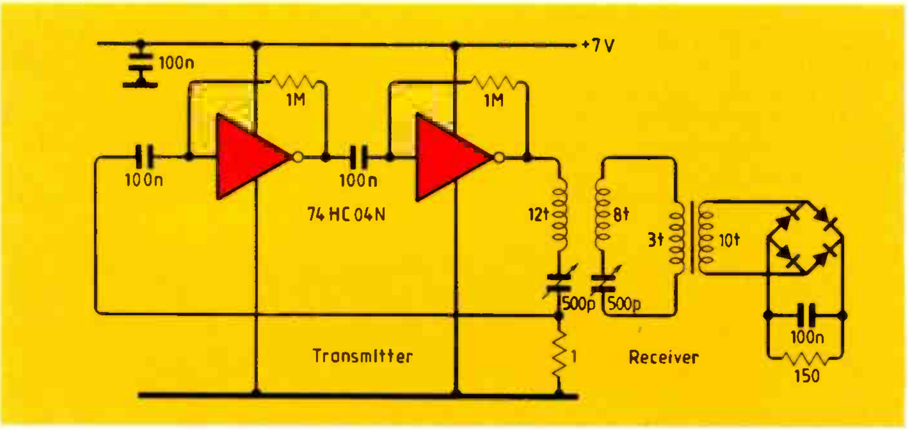


Fig.2. Practical circuit of continuously-running link for demonstrating insensitivity to coil separation.

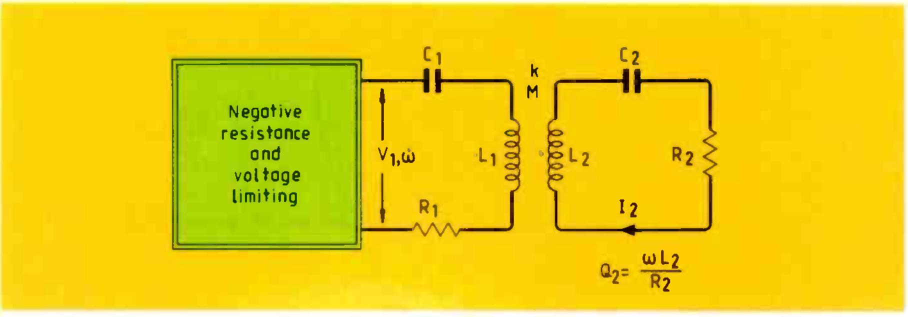


Fig.3. Analytical circuit, related to Fig.2, of a pair of series-resonant circuits with inductive coupling between them.

coefficients. First, when $k>1/Q_2$, the primary circuit impedance is shown to be $Z_1=R_1+(L_1/L_2)R_2$. In other words, although k has been used in the calculation it cancels out so that Z_1 becomes independent of k. From here, the analysis demonstrates that in this condition the transconductance of the link, I_2/V_1, is also independent of k. In general, with k anywhere between the values $1/Q_2$ and 1, the current in the receiver circuit, I_2, is independent of k and equal to

$$\frac{V_1\sqrt{L_2/L_1}}{R_2+R_1L_2/L_1} \qquad (1)$$

In other words, the system behaves as if L_1 and L_2 were acting as a perfect transformer of turns ratio $n = \sqrt{L_2/L_1}$. Thus the e.m.f. in the receiver circuit is V_1 stepped up by the notional turns ratio n. The transmitter circuit resistance R_1 reflects into the receiver circuit as n^2R_1, and this gives the simple equivalent circuit of Fig.4, again independent of k.

A NEAR MISS?

Donaldson has not found any textbooks which discuss this interesting property and its possible uses. The nearest approach seems to be in an analysis of coupled circuits by G.R. Noakes in the *Services' Textbook of Radio.*[5] After stating that I_2 in the secondary circuit (receiver in Fig.3) is given by $V_2/Z_2=-j\omega MI_1/Z_2$, this author examines the condition in which R_2 is small relative to the reactance in the secondary circuit, X_2. (R_2 small implies $k>1/Q_2$, satisfying the working condition in the MRC implant receiver.) He points out that with R_2 ignored the expression for I_2 given above reduces to $I_2=-I_1\omega M/X_2$, and after manipulation this comes to $-I_1M/\pm kL_1$. But from the definition of coupling coefficient (see above) $M=k\sqrt{L_1L_2}$, and if this is substituted for M in the expression for I_2 the k quantities in numerator and denominator cancel out and we are left with $I_2=\pm I_1\sqrt{L_1/L_2}$, which is independent of k. But Noakes heads this result 'Tight Coupling', whereas in fact its relevance is significantly wider.

RECEIVER TRANSFORMER

In the receiver part of Fig.2, the small transformer of 3t : 10t on a ferrite ring core is introduced as a current transformer to measure the series resonance current I_2, as this is the quantity which is being stabilised in the k-tolerant system. If a simpler, classical diode detector circuit were used the connections would be such that the detector would be responding to a p.d. across either L_2 or C_2 (or part of one of these reactive elements).

In the chosen condition of $k>1/Q_2$, the frequency ω varies with k as described above, so that the reactance of L_2 or C_2 varies correspondingly and thus changes the voltage across the component. Measurements, of course, confirm that the output voltage of a simple diode detector would vary with k. By the use of the current transformer, however, the series resonance current I_2 is measured and converted by the bridge rectifier into a proportional voltage across the 150Ω load.

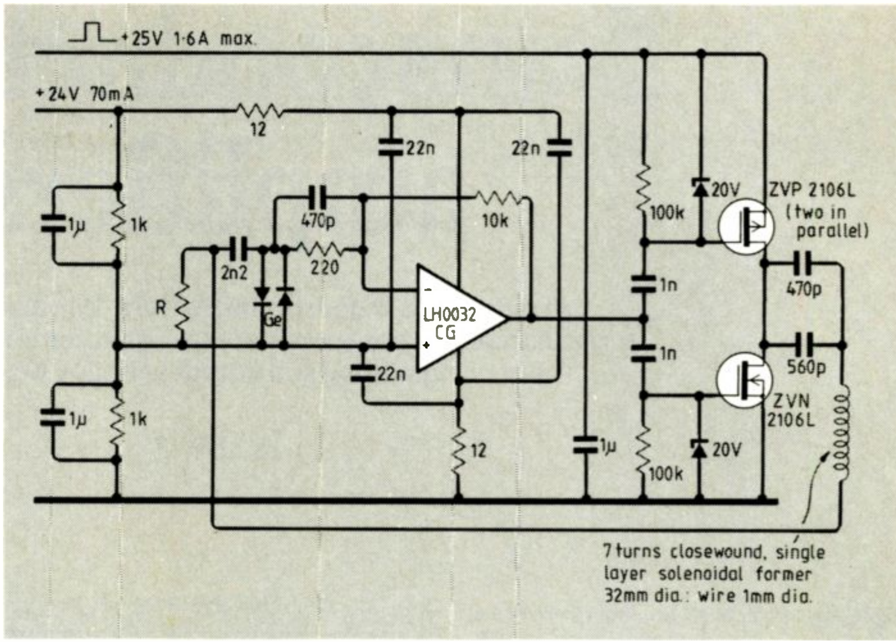


Fig.5. Practical pulsable transmitter circuit operating at 3.5MHz and capable of transferring over 9 watts into the output load of an implanted receiver.

PRACTICAL LINK CIRCUITS

Figure 2 is a practical circuit but intended only for demonstrating the principle. For energizing actual implants the MRC Unit has developed transmitters which are more powerful and can be pulsed or sine-wave-modulated. An example of a pulsable 3MHz transmitter that will transfer over 9W to a receiver output is shown in Fig.5. It will produce a voltage of 60V across a receiver load of 390Ω.

V-mos transistors are used because their on-state internal resistance is very low – of the order of a few ohms. This means that series resistance R_1 in the Fig.3 analytical circuit is minimized, so reducing dissipation, and the receiver current I_2 is maximized, as indicated by equation 1. These transistors also have a gate-source voltage swing for full turn-on and turn-off of about 7V. It is just about possible (though not done in this example) to drive them from fast c-mos devices.

The op-amp switches the output stage between two saturated states with voltage swings almost equal to the supply voltage (25V). This square-wave drive is chosen, rather than a sinusoidal one, in order to achieve both high efficiency and low series R_1. Of course, the LC resonant circuit acts as a filter which selects the 3MHz sinusoidal fundamental. The LH0032 linear hybrid op-amp will provide an output swing of 20V at 3 MHz, ample to drive the output devices. Its input voltage is obtained from the positive feedback resistor R. To make this sufficiently low in value, copper wire was used – three 4cm lengths of 6/0.0025in connected in parallel. Germanium diodes in the op-amp input circuit provide some measure of stabilization of the input amplitude and so minimize the effect of limited slew-rate.

The receiver operating with this transmitter follows the circuit arrangement in Fig.2, though the load is 390Ω. A basket coil is used to pick up the r.f. energy, as this type of winding gives both high Q and a shape convenient for implantation. The current transformer, wound on two stacked ferrite cores, reflects the 390Ω load back into the primary circuit as a resistance of about 11Ω. This gives the series resonant circuit a Q of approximately 20.

One of the first practical links of this kind for a neurological prosthesis is expected to be used for a paraplegic patient in the second half of 1987.

There are, of course, other ways of obtaining insensitivity to coil separation in inductive energy-transfer systems. These include, for example, frequency or pulse-width modulation, and the use of critical coupling for k in a.m. systems[6]. But such systems can require quite complicated or critical circuitry. The MRC's separation-insensitive link described above seems to offer a relatively simple, robust and therefore inherently reliable alternative.

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Transconductance amplifiers

Introducing a transistor buffer into the standard op-amp realisation of a transconductance amplifier improves current handling and output voltage range.

K. LEWIS

Transconductance amplifiers provide a current output proportional to a voltage input with, ideally, infinite output impedance. The gain — amps out per volt in — is denoted by G. Various circuits exist to implement this function, typically making extensive use of current mirrors, which inevitably introduce some error and should be avoided if precision operation is required.

The standard transconductance amplifier is derived from the differential-mode amplifier shown in Fig. 1. First ignore the broken line connections. With this amplifier, if $R_2'/R_1' = R_2/R_1$ common mode rejection is achieved and the input/output voltage relationship is

$$V_{DC} = -V_{AB}R_2/R_1. \qquad (1)$$

It is important to appreciate that both the output voltage V_{DC} and input voltage V_{AB} can be floating, so that the node C does not have to be the circuit common. By adding a fifth resistor R_3 and a load resistor R_L, as indicated by the broken lines, the basic circuit for a transconductance amplifier is established. If R_3 is small compared to the biasing resistors, the voltage V_{DC} establishes a constant current in R_3 which returns to earth, point E, via the load resistor R_L. The circuit may be completed by earthing either input A or B which results in the non-inverting or inverting amplifier Fig 2.

Ignoring the load resistor R_L, it can be seen that the circuit contains three pairs of resistors R_1, R_2 and R_3, as typically $R_1 = R_1'$, $R_2 = R_2'$ and $R_3 = R_3'$. It is apparent that the original balance condition, required for common mode rejection, has been upset by introducing the resistor R_3. A detailed analysis reveals the output impedance of the revised circuit to be infinite as required: Without this modification the output impedance is equal to the positive feedback resistors $R_1' + R_2'$. In effect, common-mode rejection is achieved for the output current, which is a slightly different condition to that defined above.

The transconductance G of the inverting circuit of Fig.2 with B earthed, is most conveniently calculated when $R_L = 0$. Under

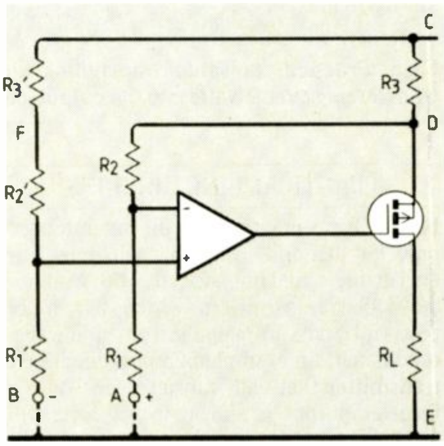

Fig.1. Differential amplifier forms the basic transconductance circuit when R_3 and R_L connected.

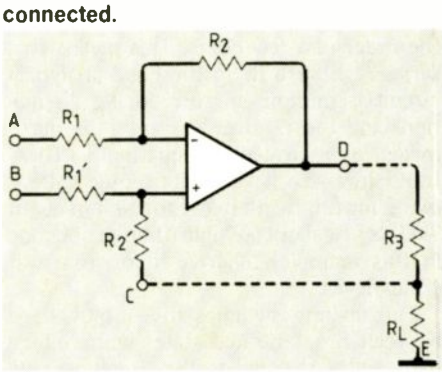

Fig.2. Standard op-amp transconductance amplifier requires R_3' to obtain infinite output impedance. (Either A or B can be earthed).

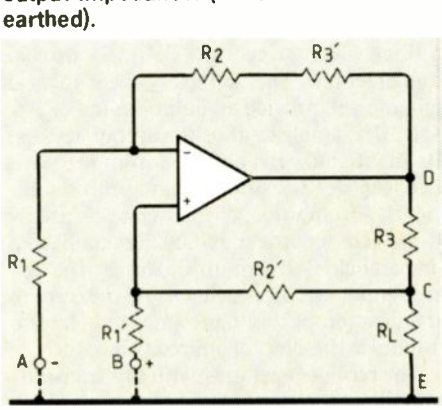

Fig.3. Modified circuit using p-channel, enhancement-mode mosfet.

this condition, the output current is contributed by only R_3 and the op-amp which is effectively connected in its inverting mode has a voltage gain $V_{DE}/V_{AE} = (R_2 + R_3)/R_1$ The transconductance is therefore

$$G = -\frac{R_2+R_3}{R_1R_3}. \qquad (2)$$

This formula, except for the reversal of sign, is also applicable to the non-inverting circuit when input A is earthed.

Since a large amount of positive feedback can exist in this circuit, it is worth considering if unstable operation is possible. The amount of positive feedback is dependent on the load resistance R_L: if R_L is zero, the positive feedback path is eliminated. However, if R_L is open circuit, the fractional feedback to both inverting and non-inverting imputs is equal and is given by $R_1 / (R_2 + R_2 + R_3)$. Unfavourable resistor tolerances could then result in a net positive feedback which, for zero imput voltage, would result in the op-amp output limiting either positively or negatively. In practice, this is not a problem because as soon as a load resistance R_L is connected to the amplifier, the positive feedback fraction is reduced, resulting in correct circuit operation. For optimum performance the three pairs of resistors R_1, R_2 and R_3 should be closely matched and a precision-type op-amp should be used.

The transconductance amplifier described has the capability to both sink and source current, but in practice the current-handling capability is limited by the op-amp output stage and power dissipation. Also, the voltage output range is limited by higher output currents and the voltage drop across R_3, which should be typically one to two volts.

Assume that the amplifier, in its existing form, is modified to include a transistor buffer and is only required to source current. This would suggest employing either an n-p-n emitter follower or a common-emitter p-n-p transistor. The emitter follower would, however, tend to further limit the voltage swing due to the base-emitter voltage drop. On the other hand, a p-n-p transistor would extend the voltage swing capability but has the disadvantage that it would effectively increase the op-amp gain and possibly cause instability.

Since the output impedance of a common-emitter or common-source transistor is inherently high, it is desirable to combine the op-amp with the transistor buffer to take advantage of its high output impedance and achieve a degree of isolation between the load resistance and the op-amp output. If a p-channel mosfet is connected as a source follower buffer to the output of the op-amp, the amplifier can be reconfigured to give a negative output voltage with respect to the positive supply rail, and the current developed in the source resistor is available at the drain as a constant current. This can be achieved in the circuit of Fig.1 by returning node C to the positive supply rail. Again, earthing either input A or B results in the inverting or non-inverting mode amplifier shown in Fig.3.

If the resistor R_3' is shorted, V_{DC}, the voltage developed across the source resistance R_3 is defined by equation 1 and the output impedance at the transistor drain is infinite. However, the current in R_3 is also required to establish the voltage across R_2. This voltage will increase as the supply voltage increases, so that the derived constant-current output is a function of the supply voltage, which is undesirable. By increasing the resistor R_2' to $(R_2'+R_3')$ the voltage V_{DC} slightly increases with the supply voltage to exactly compensate for the increased current demanded by R_2. Power

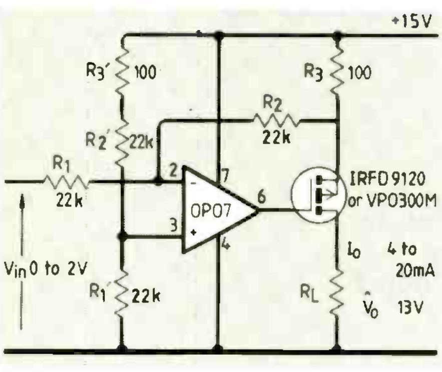

Fig.4. Single-supply transconductance amplifier suitable for use as an industrial 4-20mA interface.

supply rejection of the output current and the transconductance of the amplifier are most easily established using the principle of superposition. Referring to Fig. 3, let both imputs A and B be returned to ground, so that $V_{AB} = 0$. By inspection, the voltage gain from node F to node D is

$$\frac{V_{DC}}{V_{FE}} = \frac{R_1'}{R_1'+R_2'}\,\frac{R_1+R_2}{R_1} = 1. \qquad (3)$$

So that $V_{EF} = V_{DE}$. Now if the op-amp and its buffer are removed, the voltage V_{DE} remains unchanged, demonstrating that a balance condition exists and the fet source current must be zero, independent of the supply voltage.

Now let a voltage V_{AE} be introduced and let the supply voltage be replaced by a short circuit, ignoring the fact that this normally

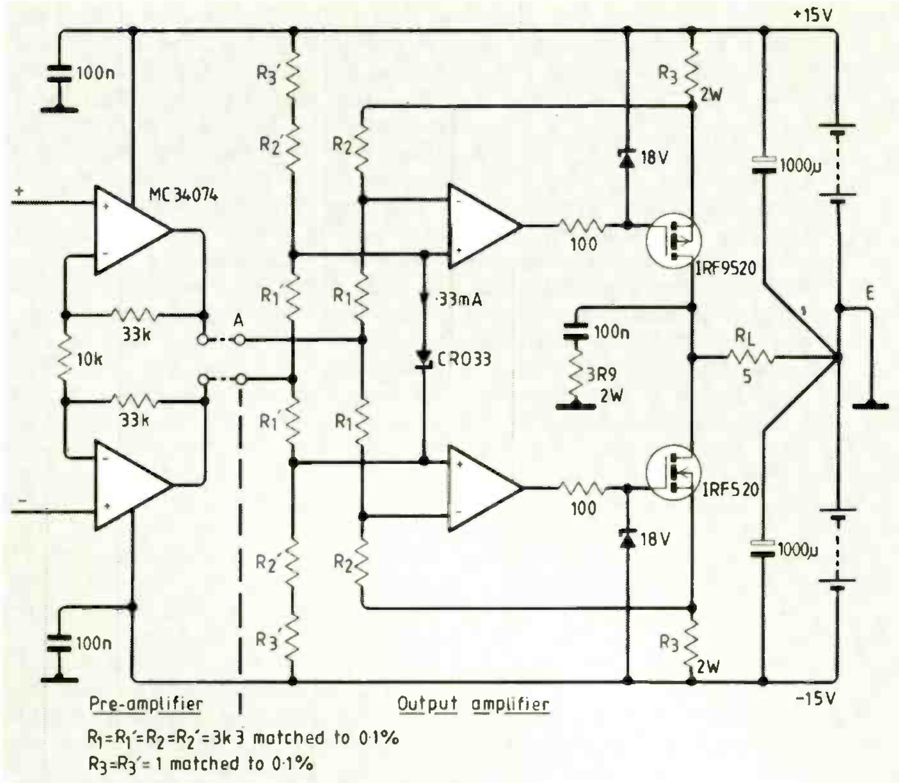

Fig.5. Class-A 10W transconductance amplifier.

supplies the op-amp. The inverting mode voltage gain is

$$\frac{V_{DE}}{V_{FE}} = -\frac{R_2}{R_1}. \qquad (4)$$

The load resistance seen by the fet source is effectively R_3 in parallel with R_2, which therefore results in a fet source current

$$I_s = V_{DE}\frac{R_2+R_3}{R_2R_3} \qquad (5)$$

Substituting for V_{DE},

$$I_s = -V_{AE}\frac{R_2}{R_1}\,\frac{R_2+R_3}{R_2R_3}. \qquad (6)$$

The fet gate current is negligible, so that I_s is equal to the output current. The transconductance is therefore

$$G = \frac{R_2+R_3}{R_1R_3} \qquad (7)$$

G is positive, as the fet introduces a second inverting stage, but is inverted with respect to input B. Note that equations 7 and 2 are indentical!

A number of attractive features are provided by the circuit in Fig. 3. Using an enhancement-mode p-channel mosfet, the gate current is negligible and can be directly connected to the op-amp output. The performance and accuracy of the amplifier is only limited by resistor tolerances and op-amp limitationd, so that precision operation is obtainable. Negative feedback is isolated from the load so that improved dynamic performance is achieved. Normal, unity-gain, stable op-amps can be expected to be stable, as the feedback is taken via a source follower. The positive feedback path present in the basic op-amp circuit is eliminated. By employing power mosfets the current-drive capability can be considerable. The voltage output swing is limited only by the supply voltage and the voltage drop across R_3, as the mosfet typically has a very low on resistance. The common-mode voltage of the op-amp is typically well above the 0V rail, which therefore allows single supply operation. Lastly, an extremely high output impedance is achieved, which is independent of resistor matching.

Figure 4 illustrates a practical single-supply circuit which may be used in industrial signal processing to generate the standard 4 to 20 mA interface. Resistor pairs should ideally be matched to at least 0.1% to avoid offsets and to achieve supply rejection. In my experience, metal-film type 1% resistors, when obtained from the same batch, are typically matched to at least 0.1%. Alternatively, thick or thin-film, isolated resistor arrays can be used. The illustrated circuit has a transconductance of approximately 10mA/V. The 4mA offset must be derived via a suitable voltage (or current) reference and summed appropriately with the signal voltage. If, however the supply itself is an adequate reference of say 15V, increasing R_3' to 1.31kΩ will set up the required 4mA offset without influencing the transconductance of the amplifier.

Figure 5 shows the final circuit. This is a high-performance, class-A transconductance amplifier, which is a symmetrical combination of the p-channel circuit described and its n-channel compliment. It has the ability to both sink and source current and, as there are two complimentary amplifiers, the transconductance gain is doubled. The potential problem of defining the output quiescent current without upsetting the balance condition is nicely solved by introducing the constant-current diode. This will introduce an equivalent dc voltage on the inputs of both halves of the amplifier equal to I_dR_1, where I_d is the diode current. It therefore follows from equation 7 that the quiescent current I_q will be defined by

$$I_q=\frac{R_2+R_3}{R_3}I_d \qquad (8)$$

The differentially configured output stage is extremely flexible and the design can be readily adapted to suit the user's requirements. Correct dc conditions are established without earthing either input A or B, so that the amplifier may be used in its differential mode. An isolated signal source may be connected source has finite inpedance.. However, if either A or B is reuturned to node E, then supply rejection is achieved only if the signal-source impedance is zero. Since many signal sources are not isolated and do not have a low imdedance, an additional preamplifier may be required: a single op-amp could serve this purpose. However, the two-op-amp solution shown provides imput flexibility, since the signal source may be either isolated, balanced or unbalanced.

The 0.33mA constant-current diode, from equation 8, establishes an output quiescent current of 1.09A. The amplifier can therefore be expected to deliver at least ±2 amps into the load R_L for an input voltage V_{AB} equal to ±1V, corresponding to output-stage transconductasnce of 2 amps per volt. The preamplifier increases the gain to provide an input sensitivity of 100mV r.m.s. for 10W out into a 5 ohm load with a sinusoidal source.

Four OP07 op-amps could be used for precision low-frequency performance. However, the quad op-amp type MC34074 provides a more impressive dynamic performance. The series RC circuit connected to the output of the amplifier, although a compromise in a transconductance amplifier is necessary to provide correct output damping: without this network, instability may result with inductive loads. In practice, this network will have a much higher impedance compared to the load resistor R_L. The two 18V zener diodes limit the gate-source voltage below its maximum rating, which could otherwise be exceeded if the amplifier is overdriven or during transients.

Amplifier distortion can only be indirectlly measured by converting the output current into an output voltage, using a suitable resistive load. Some difficulty was experienced by the author with this measurement due to loads which appeared to be non-linear. Distortion measured was mostly third harmonic which, at 1kHz and 10W output into a 5 Ohm load was 0.007%. This figure reduces quite rapidly with output level, which may be expected as the outpout transistors no longer enter their saturation region. The total harmonic distortion is approximately proportional to the frequency, probably accounted for by the associated reduction in open-loop gain of each of the output op-amps. The 3dB cut-off frequency is 600kHz.

The two output transistors together dissipate in excess of 30W and therefore require a considerable heat sink.

In conclusion, the basic transconductance amplifier described, shown in Fig. 3, is simple and flexible and can replace more complex circuits which may use current mirrors. Precision operation is achieved if matched resistors and a good op-amp are used.

Mr Lewis is a group leader at Grinaker Electronics, South Africa.

Noise factor or noise figure?

You can use factors or figures, but watch the noise temperature. Here's why h.f. operation is 'environment-limited' and v.h.f. 'equipment-limited'.

'JOULES WATT'

Ever since H.T. Friis[1] proposed the idea of *noise factor*, F_N, to characterise radio receivers, useful though it is, trouble and confusion still arises. People forget that F_N is a ratio, in other words, that it is referred to some standard. The IRE (now IEEE) established 290K as the reference temperature[2] some time ago; for a detailed discussion of the connection between noise and temperature see the 1975 *Wireless World* treatment[3].

Another slight confusion arises when *noise figure* F, is used. I have seen articles where factor and figure appeared at random in the text! Pity the poor student, because F and F_N are not the same thing. Noise figure F is $10\log_{10}F_N$, i.e. the noise factor ratio converted to decibels.

The use of F is fine at around room temperature, since few problems arise. But at widely different equivalent temperatures care has to be exercised. U.h.f. systems looking out at the sky see the cold depths of space, which means that radio astronomy or satellite communications systems, for example, operate at effective noise temperatures well below 290K. On the other hand, h.f. receivers operate in a man-made, atmospheric and galactic jumble of noise, equivalent to hundreds of thousands of kelvins – Fig. 1. The definition of F is

$$\frac{S_i/N_i}{S_o/N_o} \qquad (1)$$

where the input and output ratios apply to a two-port stage in a system, Fig. 2.

The available noise power at T_0 in a bandwidth B is kT_0B, where k is Boltzmann's constant. Putting T_0 = 290K gives the standard available noise power input N_i accompanying the signal to satisfy the definition of F_N. Thus if G is the available gain of the amplifier or stage, then

$$F_N=\frac{S_i}{kT_oB}\cdot\frac{N_o}{GS_i}=\frac{N_o}{GkT_oB} \qquad (2a)$$

is the noise factor for it. N_0 is the total output noise power. Dividing it by the gain G gives the equivalent total input noise power N_{in}. This is made up of N_i coming in at 290K with the signal and N_e, the equivalent noise at the input from the amplifier alone.

$$\therefore\quad F_N=\frac{N_{in}}{kT_0B}\cdot\frac{N_i+N_e}{kT_oB} \qquad (2b)$$

These noise powers appear to come from sources at temperatures T_0 and T_e, related in the usual way by $N_i=kT_oB$ and $N_e=kT_eB$, (also by a similar argument, $N_{in}=kT_{in}B$). Therefore we can write equation 2 as

$$F_N=\frac{T_{in}}{T_o}=1+\frac{T_e}{T_o} \qquad (3)$$

T_e is the *excess* equivalent noise temperature of the stage (how much above 290K it appears to contribute), whereas T_{in} is the *total* equivalent noise temperature.

If you work with a real system, your interest is in the actual signal-to-noise ratio that is achievable, not directly in F (or F_N...). At high noise levels ($T_{SYSTEM} \gg$ 290K) F hardly matters. In this sense, carefully designing a low-noise front end for an h.f. receiver is misplaced effort. Other criteria become important instead, such as a wide dynamic range. On the other hand, if $T_{SYSTEM} \ll$ 290K, you might predict a much worse s/n than that which can be achieved with a low-noise design.

This can be seen from equation 2 in decibel form

$$\left.\begin{aligned} N_{in} &= 10\log kT_o + 10\log B + F \\ \text{or} \quad N_{in} &= (-144+F)\text{dBm kHz}^{-1} \end{aligned}\right\} \quad (4)$$

This means N_{in} is now the noise power relative to a milliwatt in a 1kHz bandwidth. A plot of this relation gives curve A on Fig.3. The best we can do (apparently!) even with a perfect amplifier, F = 0dB, is resolve a signal at −144dBm for an s/n of unity. Yet satellite receivers must be and are designed to do much better than that.

The error is to remain hung up on the 290K. From equation 2, rearranged

$$N_e = kT_oB\,(F_N-1)$$

or in dB

$$N_e = 10\log kT_o + 10\log B + 10\log(F_N-1)$$

or

$$N_e = [-144+10\log(F_N-1)]\text{dBm} \quad \text{kHz}^{-1}.$$

Plotting this gives curve B on Fig.3. As F_N tends to 1 (perfection!) there is no limit to how small the input signal can be for detection.

Yet all receivers and aerials generate or pick up some noise. The final equation, derivable from (5), takes account of this

$$N_e + N_A = kT_oB(F_N-1) + N_A$$

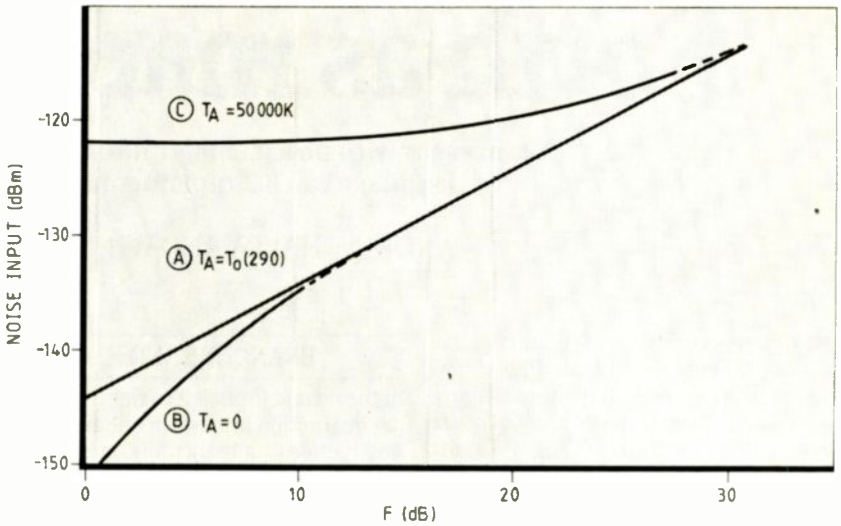

Fig.3. Curves show variations in the noise power input to a receiver (per kHz bandwidth) as the noise figure varies, with aerial temperature T_A as a parameter. The plots are derived from noise input = −144+10log$_{10}$(F_N+T_A/T_o-1) for the various temperatures.

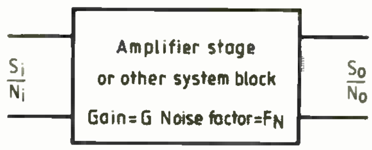

Fig.2. Noise factor, or its decibel equivalent the noise figure, is a parameter that applies to a two-port stage, which can be an amplifier, a mixer, attenuator or, as indicated in Fig.1, an aerial.

where N_A is noise picked up by the aerial. As before, we can write $N_A=kT_AB$, which defines *aerial temperature* T_A.

$$\therefore N_e + N_A = kT_oB\left(F_N + \frac{T_A}{T_o} - 1\right)$$

This is what a designer requires to relate actual noise N_e+N_A present to the signal and therefore arrive at the sensitivity of the system.

Taking logs of this last equation and plotting for a typical aerial temperature of, say, 50 000K in the h.f. band, gives curve C on Fig.3. This shows that you hardly gain any improvement in signal-to-noise ratio by designing for noise figures better than ~20dB in h.f.-band receivers. However, it is worth keeping a weather eye on F when receiving signals approaching 30MHz; essential when working at 144MHz and even more so at 430MHz.

The discussion has highlighted a number of points. One is that although F is independent of bandwidth, the s/n is not. This means that c.w. signals in a few tens or hundreds of hertz are receivable well below the input power level required at the receiver terminals for a.m. speech or even s.s.b. This is especially true when you realise that the physiologists have found that our ears effectively act as narrow-band filters – when we want them to. An experienced c.w. operator 'filters' the wanted signal from all the others, even in a wide bandwidth and can resolve a message that would be lost in the noise, according to the above analysis.

Another point is that h.f. and m.w. equipment is 'environment limited' regarding the signal-to-noise ratio. This explains why the simple one-stage receivers and inefficient aerials of yesteryear worked so well. It also explains why Oliver Lodge failed to detect the Sun at medium wavelengths when he looked for it with coherer apparatus at the end of the last century... Very and ultra-high frequency radio, on the other hand, is 'equipment limited' and all the low-noise techniques and efficient aerial design that we can muster are required for best results.

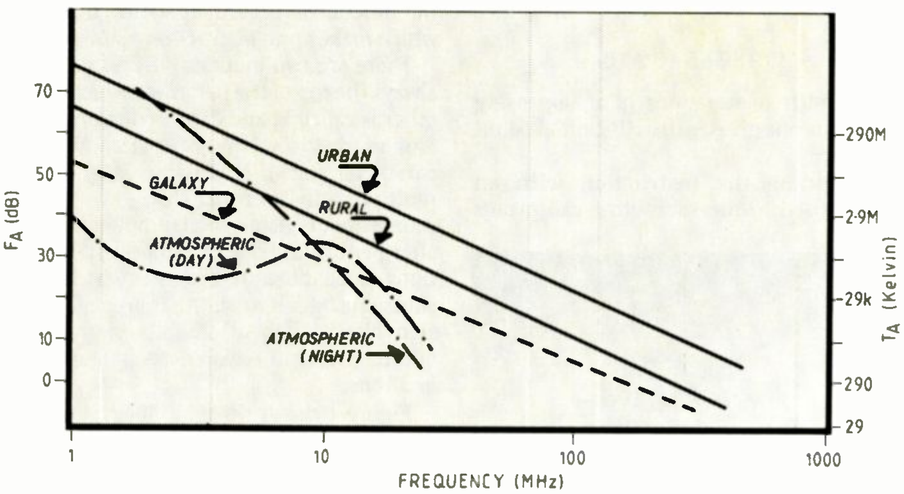

Fig.1 Background noise from the galaxy, the atmosphere and from the man-made environment has an operating noise figure higher than even poor front ends of h.f. band receivers. At frequencies above 100 MHz the effective temperature rapidly falls well below 'room temperature', even in urban areas.

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Forth as machine code

A processor with no assembler illustrates how a high-level language can be implemented in hardware.

ANDREW HALEY AND WILLIAM WATSON

Forth execution is fast using the NC4000 but an understanding of how the language operates within the processor produces even faster code. There are currently three versions of Forth for the NC4000. Although they are separate and distinct Forth environments, they all use the same Forth primitives provided by the NC4000 chip and this is where our description of the software begins.

FORTH OPCODES

Our description of how Forth works on the NC4000 follows the order of the bits that comprise an NC4000 opcode, starting at the most-significant bit and working down.

At the end of every instruction, a single cell* pointed to by the program counter, P, is fetched from memory and latched into the instruction register. As explained in the February issue, if the most-significant bit of the opcode is zero, the instruction is a subroutine call and the lower 15 bits of the opcode are used to load the program counter before fetching the next instruction. At the same time, the previous program counter content is pushed to the return stack.

Execution proceeds until an opcode is found with its "return-from-subroutine" bit set, whereupon the program counter is popped from the return stack and execution continues from the point where the subroutine was called.

Only 15 bits are used for a subroutine address so all subroutines, and therefore programs, must reside in the lower 32K memory cells. This is, if you like, a single-bit instruction which executes in only one clock cycle – the smallest unit of processing time.

If the most-significant bit of the opcode is one, the instruction is not a subroutine call and must be executed. The action of an instruction depends on several three-bit fields in the opcode. This leads naturally to the use of octal notation to describe opcodes.

Since the NC4000 compiler translates high-level Forth source code directly into the required opcodes, it is not necessary to know the details of the bits within each opcode. However, a knowledge of the principles is useful, as it allows the programmer to optimize programs for the chip.

Three bits immediately next to the most-significant bit determine the class of Forth instruction. There are three basic classes – branches and jumps, a.l.u. and stack operations, and i/o and memory instructions.

* Novix is a 16-bit processor. Usually, 16-bit data is described as a data word but where Forth is concerned, the term cell is preferred to avoid confusion with the Forth word.

BRANCHES AND JUMPS

If the second (from left to right) octal digit of an instruction is between one and three, the instruction is a branch of some kind; if the branch is taken, the least-significant 12 opcode bits replace the least-significant 12 bits of the program counter and the upper four bits of the program counter remain unchanged.

This implies that branches can only be within the same 4K-cell destination page. Since Forth definitions (subroutines) are usually very small, and Forth convention is not to jump one definition into another, this is rarely a problem.

The type of branch instruction is indicated by the opcode's second octal digit. Opcode $13xxxx_8$ is an unconditional branch; the 12 bits $xxxx_8$ are used to reload the bottom 12 bits of the program counter. Conditional branches are performed using $11xxxx_8$: if the top item on the parameter stack is zero the branch is taken, but if it is non-zero, the processor continues with the next instruction. In either case the top item is removed from the parameter stack.

Instruction NEXT, represented by $12xxxx_8$, performs hardware looping. If the top item on the return stack is non-zero, it is decremented and the branch is taken. If the top item is zero, the return stack is popped and the top item discarded. This accommodates a count-down looping structure, where register I, the top of the return stack, contains the loop count. Forth word FOR places the initial value in register I. For example the word TEST, defined as

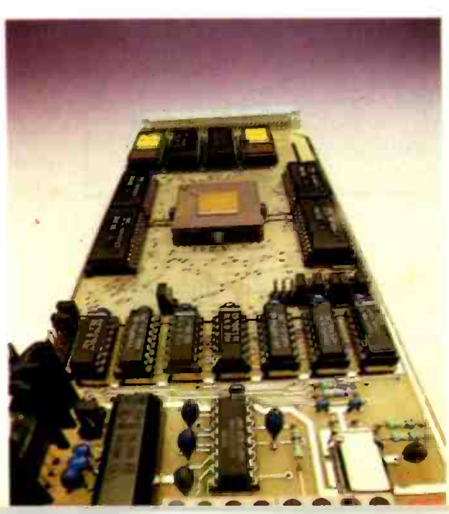
```
: TEST 10 FOR I . NEXT ;
```

produces

```
10 9 8 7 6 5 4 3 2 1 0.
```

The number of iterations of a loop using FOR...NEXT is one greater than the initial count supplied.

Combining the instruction with an address used in the subroutine call means that all jumps are executed in a single cycle. It is worth comparing the FOR...NEXT loop with Forth's universal DO...LOOP which increments the starting value for each pass round the loop and compares it with the terminating value. With the NC4000, the DO...LOOP takes 11 to 13 clock cycles, which is about equivalent to the PDP11-73's SOB instruction or the 68000's DBRA. However, there are innumerable instances in Forth programs where the code is of the form 100 0 DO...LOOP which can be replaced with the phrase 99 FOR...NEXT. This results in a saving of 100×11=1100 clock cycles or 137μs at 8MHz and illustrates how an understanding of the NC4000's operation can produce even faster code.



The NC4000 has an unusual instruction called TIMES which takes a number from the parameter stack and places it in the I register. It also sets the processor's 'streaming' mode, in which the instruction immediately following the TIMES instruction is latched into the instruction register. In each following cycle the instruction is re-executed, decrementing I until it becomes zero, at which point the I register is popped and execution continues with the next instruction. This means that an instruction can be re-executed on every clock cycle without having to be re-fetched. In the next two sections we will show how streaming mode can be useful for arithmetic functions and for moving data blocks.

ALU AND STACK OPERATIONS

An opcode of the form $10xxxx_8$ is an arithmetic and logic unit (a.l.u.) instruction. Instructions in this class form all the stack-manipulation primitives, as well as arithmetic functions. Figure 1 shows the fields which make up an instruction of this kind.

There are two inputs to the a.l.u.; one is always the top of the parameter stack T. The other is called Y, and can be from one of the four sources: the N register (second on the parameter stack), N plus the carry bit, the multiplier-division register, MD, or the square-root register, SR. Output of the a.l.u. after performing one of eight possible functions, is fed into a shift register which either shifts one bit left or right, or propagates the sign bit through all 16 bits of the a.l.u. output. The shift register can shift either 16 or 32 bits.

Figure 1 shows the a.l.u. functions. Note that T–Y and Y–T are provided so both the word – and the phrase SWAP – are possible NC4000 instructions. The simplest a.l.u. instruction is NOP with an opcode of 100000. This causes the T register to be routed through the a.l.u. untouched, back into the T register.

Stack-manipulation instructions are performed using a.l.u. instructions. For example, 107100_8 exchanges T and N, corresponding to the Forth word SWAP. Input Y of the a.l.u. is selected to be the N register and the opcode TN bit is set. The a.l.u. operation selected is seven (pass Y) so N passes via the a.l.u. into T.

Another example is opcode 100120_8, corresponding to Forth word DUP, which duplicates the top of the stack. This time the a.l.u. function is zero (pass T) and the stack-active bit is set, causing register N to be copied out to external ram. Bit TN is also set, which causes T to be copied into N. Words OVER.DROP and SWAP-DROP can be produced by similar means.

Several Forth words can be combined to form one instruction. For example, an instruction corresponding to + 2 * (add T and N, multiply the result by two and leave it in T) is 104022_8. Here the a.l.u. function is +, the stack activate bit is set to pop N from external ram, and the shift-left bit is selected.

Several special instructions are selected by the highest bit of the Y-input field in the opcode. These correspond to multiply, divide and square-root steps. Each 'mathematical step' instruction performs part of a specified function, and is usually 'streamed' a number of times to produce a complete result. For example, executing the divide-step instruction /' fifteen times followed by the last divide step /'' divides the 32-bit concatenation of T and N by the contents of the MD register. The quotient is returned in N and the remainder in T. This means that a full 32-by-16-bit divide takes only 21 cycles or just over 4µs at 5MHz.

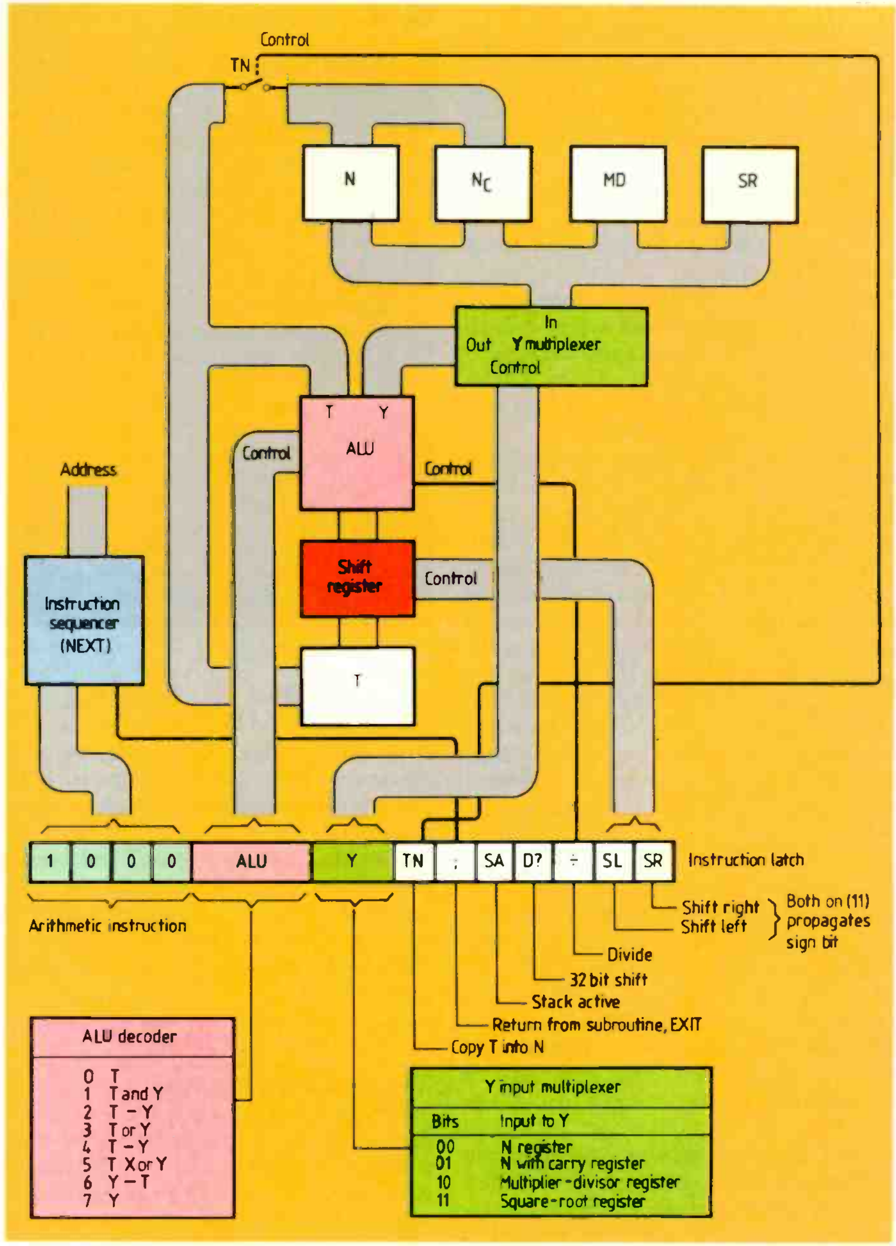


Fig.1. Each of the Forth processor's instructions consists of a 16bit opcode compiled from one or more Forth words. The first four bits define the instruction type and the remaining twelve directly control the a.l.u. and registers.

I/O AND MEMORY INSTRUCTIONS

Instructions where one of the operands is not on the stack form the i/o class. The NC4000 has an array of 16 internal registers. Some, like the program counter and stack pointers, are used to control the processor and some are used to communicate with the outside world. These are listed in the register table.

Instructions internal fetch I@ and internal, I! are not found in conventional Forth implementations and are special instructions used to access the registers within the NC4000. Internal fetch I@ takes the address of an internal register (part of the opcode) and returns the value in that register to the stack. Instruction I! takes a value from the stack and places it into a register.

Internal register addressing gives the programmer access to the NC4000 X and Bports. Each port has four associated registers called data, mask, direction, and tristate control. Each bit in these registers controls the function of its corresponding bit in the port, making every i/o bit independently programmable.

Writing to a port's data register updates that register and causes the data to be output on the pins if the appropriate bit in the direction register is set to one.

Reading from a port returns the exclusive or of each pin's state and the contents of the data register. Therefore, to test for a particular pattern on a port, it is only necessary to set the port for input, write the test pattern into the data register and read the data port. If the data register is zero, the port input matches the desired pattern. This is much faster than having to make an explicit comparison in software. The mask bit for a particular i/o line disables writing to that bit in the data register, but the data still goes to the pins.

Normally, tristate mode causes a pin to be set at high impedance but when the data register is written to, the data is output to the pins for the duration of the current cycle. Fetches in this mode return the contents of the data register. Whenever data is output from the Bport the $\overline{\text{WEB}}$ signal is asserted so data output can be latched on the rising clock edge.

There are other main registers. The '−1' register is permanently wired to all ones; fetching from it allows −1 to be placed on the top of the stack in one clock cycle. This also means that operations such as exclusive oring with −1, to invert all bits of the item currently on top of the stack, can also take place in one clock cycle. Register JK contains both stack pointers, and can be read from or written to. Square root and multiplier-divisor register SR and MD can also be used to store temporary values whenever their associated arithmetic operations are not being used.

All operations on internal registers can be combined with an a.l.u. operation. For example, Bport I@ OVER + takes an input and adds to its a value from the stack, leaving the result of the addition and the original value on the stack underneath – all in one clock cycle.

There are two forms of literal instructions, perhaps more familiar as 'load immediate' on conventional microprocessors. Any value between 0 and 31 (decimal) can be pushed onto the stack in one clock cycle; other 16bit values take two.

To access external memory, fetch (@) and store (!) instuctions with several variants are provided. If the operand is in the first 32 cells of memory, the address can be contained in the opcode, and thus does not need to be placed on the stack by another instruction. This means that there are 32 variables which can be accessed almost as quickly as registers. In a multi tasking system, the pointer to the current task is usually held in one of these fast variables.

Conventional fetches and stores above location 40_8 take two clock cycles. A fetch takes an address from the stack and returns the data in the cell at that address. A store takes an address on top and stores the data underneath at that address.

If the fetch instruction is streamed wih the TIMES feature, a fetch can occur on every clock cycle because the buses are not tied up with fetching new instructions. As a result, data can be fetched to the stack at 16 bits per clock cycle. There is a special incrementing fetch instruction to do this, called @+. It takes its address from the stack, fetches the data and places it under the address, and then adds an increment between 0 and 31 to the address. At the end of its operation, @+ leaves the address on top of the stack, allowing the instruction to be repeated. Normally in Forth this would be written

DUP @ SWAP n +

There are also decrementing versions of this, with corresponding store instructions. With such instructions, data can be moved into NC4000 memory at very nearly bus bandwidth without the need for a direct memory access controller. In fact d.m.a. can be of little help to the NC4000 since it is accessing its buses every clock cycle, with no free cycles during which the d.m.a. could take place.

Here is an example of how repeating instructions might be used to read 128 samples from an analogue-to-digital converter. One TIMES instruction would be used to take 128 samples from the Bport, and another TIMES instruction would store them into a buffer area at full d.m.a. speed. This would be written.

126 TIMES Bport 1@
BUFFER 126 TIMES 1 !+

It is also possible to perform any a.l.u. operation while reading a data port, for example performing And or Or operations to mask bits.

With the exception of call and branch instructions, any of the instructions so far described can have its subroutine-return bit set so that the return from subroutine is executed in parallel with the instruction execution.

NOVIX COMPILERS

We have discussed how Forth operates on the NC4000 at a hardware level, but how is the source of an application generated, compiled and tested in the first place? A standard Forth implementation would provide all these functions for a conventional microprocessor and the various implementations of Forth available for the NC4000 are no different, although the actual hardware support (terminals, discs etc.) varies considerably from system to system.

All currently available systems have the following common features. Source code is stored in 1K blocks and may be edited, listed indexed etc. Compilation of the source code is done by the NC4000 chip itself, if necessary on the Novix board under development. As far as we are aware, no cross compilers† are currently available. All the compilers are capable of code optimization and, broadly speaking, the more expensive the compiler, the better the optimization. Even cmForth (see panel), which is supplied free with the NX4 board, can achieve some degree of optimization.

All available Forths of the NC4000 include a keyboard interpreter – the last essential component of a development environment – so that complied code can be tested on the NC4000 in real time.

Beyond these common features, currently available systems differ widely in imple-

† Compiler describes software for producing object code. A cross compiler produces code for a microprocessor system other than the one on which it is running.

cmForth

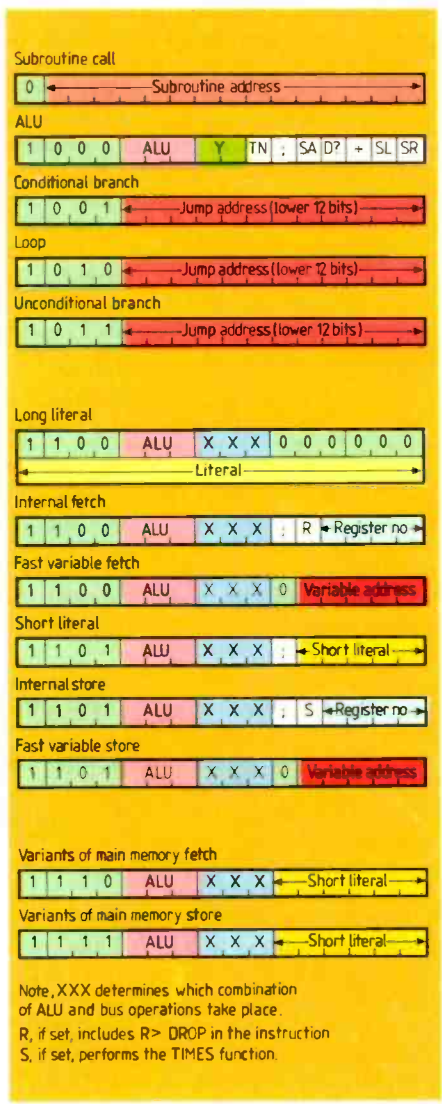
cmForth is an implementation of Forth for the NC4000 microprocessor. It was written by Chuck Moore, inventor of Forth and co-designer of the NC4000. This software is in the public domain, so it can be reproduced and resold without any royalities being payable.

The primary goal for cmForth was to build a Forth system small enough to fit in 2K words of memory (4Kbytes), yet powerful enough to recompile itself. It is therefore extremely compact. As a result the Forth kernel has been changed somewhat from the Forth known to most users. Many of the standard Forth words are not included in cmForth but alternatives are usually provided.

In cmForth, a 'serial-disc' link to the host computer is used to access mass storage. Whenever the NC4000 requires a block from the disc, a request is passed to the host and the appropriate data is transferred. This is slower than would be the case if the NC4000 had its own disc drive but at 38.4-kbaud the speed of loading programs is adequate.

Although editing could, in theory, be done on the NC4000 system, usual practice is to edit on the host and download to the NC4000 to test. The protocol used to communciate with the NC4000 system is very simple, and can be implemented easily on any computer with an RS232 link. The NX4 will run at almost any data rate. We have not found a computer which will transmit data faster than the NC4000 can receive it, so the maximum data transmission speed is always imposed by the host. On power up, cmForth automatically sets its data rate.

Software supplied with the NX4 runs on an IBM-PC or hardware equivalent and includes a full editor. In order to allow the exchange of programs with other systems, we have supplied some additional Forth words to bring the system Into closer compliance with the popular Forth-83 standard. These additions are optional, and will not usually be needed unless programs written for other systems are transferred to the NC4000.



Bit fields within an NC4000 instruction. Most kinds of NC400 code combine high-order bits of instruction with low order bits of data or address, except for a.l.u. operations where all 16 bits are used in the instruction.

Special offer

The NX4 board has been specially designed to accompany this set of articles and is available fully assembled and tested, with circuit diagrams, software and documentation. Availability is subject to stock and you should allow 30 days for delivery. Please send cash or cheque for £286 (fully inclusive) to NX4 offer, Golden River Ltd., Churchill Road, Bicester, Oxfordshire OX6 7XT.

For this offer, Novix has supplied 300 chips at a special price; the one-off price for the NC4000P alone is normally £205. Consequently numbers are limited and only one board can be supplied per order. This offer is available within the UK and Eire. Overseas readers should contact Computer Solutions.

Enquiries about the kit, chip and associated software should be made to Computer Solutions Ltd at Canada Road, Byfleet, Surrey KT14 7HQ.

mentation. The most popular arrangement is to use a serial link between a computer and the NC4000 target board containing its own ram and rom. The computer usually acts as a transparent terminal but when it receives a zero (null) character from the Novix system it is interpreted as a disc request. The Novix system then sends to a two-byte block number, which causes the host to either transmit the block if the number is positive or receive if it is negative. In this way, the Novix system appears to have its own disc drives attached.

This arrangement is cheap and convenient, but suffers from some speed restrictions due to the use of a serial line. These restrictions are due to speed limitations of the host computer rather than the Novix system. Despite the fact that Novix systems often use a software uart, i.e. data is serialized using software, they will sustain much higher data rates than most microcomputers. Even at 38 400 baud, the Novix chip has to perform more than 100 empty FOR... NEXT loops to make the delay between each bit transition.

The NC4000 can be used as the c.p.u. of a complete computer system, with its own disc drives and terminal(s). In such a system, performance of the NC4000 is high enough for multi-user operation.

DEVELOPMENT ENVIRONMENTS

Development software for the NC4000 varies in cost and usefulness. The most popular programming language for the NC4000 is cmForth. It is a basic Forth intended for producing rom-based systems with a minimum of overhead. It consists of 3.5Kbyte of program in eprom and about 30K of source code on disc. The disc contains all the software necessary to regenerate the eproms and allows an application to be added on top of the cmForth nucleus.

This Forth suffers from a few restrictions when compared to a more conventional system. For example, there is no multitasking support in cmForth, and the compiler can only achieve some of the code optimizations possible; users wanting to use very complex multi-word instructions in cmForth will have to construct the opcodes by hand.

So is it possible for a compiler to pick up all multiple word combinations and produce optimally-compiled code? Software used with Novix's development system the Beta Board, provides the answer. It recognizes all but a few of the valid multiple word combinations. The system is supplied with source code accommodating multi-tasking, double, mixed and floating-point arithmetic, trigonometric and logarithmic functions, curve fitting, a data base support package and Forth Incorporated's target compiler which is capable of producing rom-based code. This software and the hard-disc version of the Beta Board provide a formidable development enviroment – the system can recompile itself on disc in just a few seconds.

PROGRAMMING THE NX4

Using the NX4 system is quite straightforward. The host IBM PC or clone runs an MS-DOS program called NX.COM which is a 'sealed' Forth program, though still running a keyboard interpreter with a restricted set of words to enable editing, printing and block and file handling on the host IBM PC.

When communicating with NX4, the word PLUG turns the host computer into a terminal and disc for the NX4. On power up, cmForth on the NX4 does not know what data rate to run at, so after hitting its reset button, the letter B has to be sent from the host computer. The cmForth program responds with 'hi' and the host computer is now the input for the keyboard interpreter.

The cmForth word HI is defined as 1 LOAD, and this block is usually used to load utilities and development code. Definitions can be downloaded from disc or compiled in from the keyboard with equal ease, after which they can be tested by being directly executed from the keyboard.

CONCLUSION

The Novix team has shown that a new processor can be developed at a fraction of the cost of many of the more conventional devices and give superior performance, both in terms of execution speed and ease of programming. Simplicity of the buses and versatility of the i/o ports more than make up for the few extra hardware-stack chips. The NC4000 combination of computing power and flexibility opens up applications considered impossible with other processors, and points the way to new and exciting designs based on this technology.

Novix architecture was detailed in the Februrary issue. A second article in April discussed application of the device using the NX4 evaluation and development board as an illustration.

Andrew Haley and William Watson are with Computer Solutions.

Standard cmForth words

These words may have different parameters from the standard versions, but perform the same function.

```
SWAP DROP OVER DUP ROT >R R< 0= NOT = XOR AND < >
U< * / 2* M/ M* /MOD OR + - MOD */ */MOD @ ! +!
C! C@ 2DROP 0< NEGATE 2DUP MOVE FILL ERASE EXECUTE ?DUP
WITHIN ABS MAX MIN EMIT CR TYPE KEY SPACE SPACES HOLD
EXPECT HERE <# # #S #> SIGN . ? U.R. U. ABORT" ."
BLOCK BUFFER UPDATE FLUSH EMPTY-BUFFERS WORD NUMBER '
INTERRUPT QUIT ABORT DECIMAL HEX OCTAL LOAD ALLOT ,
LITERAL [ ] SMUDGE EXIT : ; CREATE CONSTANT VARIABLE ]
BEGIN UNTIL AGAIN THEN IF WHILE REPEAT ELSE ( EXIT
FORTH
```

Additions to cmForth provided with the NX4 software

```
DO LOOP +LOOP /LOOP I' J .S VLIST COUNT -TRAILING PAD
CMOVE DOES> DEPTH PICK ROLL
```

Fourth 83 standard words not supplied with NX4 software.

```
0> D+ D< DNEGATE SAVE-BUFFERS
DEFINITIONS CURRENT STATE #TIB >BODY FORTH-83 SPAN TIB .( [']
```

NC4000 internal registers.

Address	Read/write	Name	Description
0	Yes	JK	Most-significant byte J is the return-stack pointer and least-significant byte K is the parameter stack pointer. When fetched, JK reflects stack pointer on completion of the operation.
1	Yes	I	Top element of the return stack. Pushes the return stack when stored.
2	Read	P	Program counter. During an instruction's execution, contains the address of the cell following the instruction.
3	Read	−1	Returns all ones.
4	Yes	MD	Multiplier/division.
5	Read	–	Unspecified.
6	Yes	SR	Square root, power of two.
7	Read	–	Unspecified.
8	Yes	Bport	Data register.
9	Yes	Bx	Mask.
10	Yes	By	Direction.
11	Yes	Bz	Tristate mode.
12	Yes	Xport	Data register.
13	Yes	Xx	Mask.
14	Yes	Xy	Direction.
15	Yes	Xz	Tristate mode.

A logic 1 represents disable in the mask registers and sets output direction in the direction registers. For the first two X registers, the bit pattern is 0000 0000 000n nnnn. In Xz, 0000 000i 000n nnnn applies; logic 1 in bit i enables interrupts.

ENTER 38 ON REPLY CARD

ENTER 56 ON REPLY CARD

ENTER 39 ON REPLY CARD

ENTER 51 ON REPLY CARD

Image acquisition system

Creating software routines for a solid-state computer vision interface

G.J. AWCOCK, F.W. STONE AND R. THOMAS

This image acquisition system is based on a low-cost solid-state sensor device, the IS32 optic d-ram by Micron Technology. The IS32 is very suitable for generating the black-or-white binary images widely used in robotics, computer image processing and character recognition. Hardware for this system is described in the April and May 1987 issues.

The main function of the driver software is to obtain image data from the hardware and then to display it on to the screen of the host computer. A suitable screen mode should be chosen so that the image data can be mapped with an aspect ratio matching that of the sensor. Ideally this should be 1.26:1 to correspond with the effective photosite size of $8.6\times6.8\mu m$.

With a BBC computer as host, the best screen modes to use are modes 1 and 4. Mode 4 provides a basic two-colour display whilst using only 10Kbyte of memory; mode 1 gives the opportunity to add colour to screen messages but requires an extra 10Kbyte of ram.

A routine to display a continuously updated image on the computer's screen is shown in Fig.11. First, the initialize procedure sets the computer's serial port characteristics to correspond with the imaging hardware. Sensor quadrant selection is performed by transmitting codes to set or reset the row and column address m.s.bs (Table 2 last month). Finally, control passes to a loop which performs the continuous updating; it starts by transmitting the code to initiate the scan macro-task in the hardware.

It is desirable to employ a display-whilst-scan technique, since this introduces a degree of parallelism which shortens the image update loop as the computer need not wait for the sensor to finish capturing an image. This means that as soon as the sensor scan has been initiated the host begins to plot image data resulting from the previous scan, whilst the hardware is performing its dedicated task.

In the case of the first traverse of this loop after initialization, the resulting image will be quite meaningless, being a display of random memory contents. Also, the displayed image will always be one step behind the image currently being captured by the hardware. But whilst this can be momentarily confusing, it should not present any serious drawbacks in the majority of applications.

On completion of a scan or of the display process, whichever takes the longer, the code to start the read macro-task is transmitted to trigger the transfer of image data from the most recent sensor scan back to the host. When the raw (i.e. packed and partially linearized) image data is received, it is better to buffer it in the computer's main memory, rather than to attempt to de-scramble it fully and plot it directly on the screen. This allows fast hardware-to-host transfer rates to be achieved. The prototype system was run at 19 200 baud with no serial link handshaking, using a BBC computer as host.

To enable the update loop to be terminated, a keyboard scan routine should be included at a suitable point in the cycle. This would allow an interesting image to be frozen by pressing a key and saved to disc for subsequent processing or enhancement.

IMAGE DATA DISPLAY

Plotting the buffered image on to the screen is the most complex task of the image update software. Details of the algorithm will vary for different host machines because of their particular graphic screen memory allocation. Thus, in developing a suitable algorithm for the display task the major factors to be considered are

- the screen memory map of the host: the need for speed prohibits the use of operating system calls which would otherwise allow plotting by means of standard X and Y graphics coordinates.
- the relationship between the orientations of the sensor, the scene and the computer screen, taking account of inversions caused by the optical system employed.

Optical arrangements in the prototype consisted of a modified photographic enlarger with the sensor surface in the film plane. Subject matter could be placed on the baseboard and the image focused on to the front face of the sensor with the normal bellows focusing control and the enlarger head's height control. Since the front face of the sensor is the surface pointing away from the observer, the display automatically compensates for the lateral inversion inherent in the optics. However, optical inversion in the vertical direction must still be corrected and this dictates that the sensor pels along the X-axis (or rows) should be plotted in reverse order on the screen for a correctly oriented image.

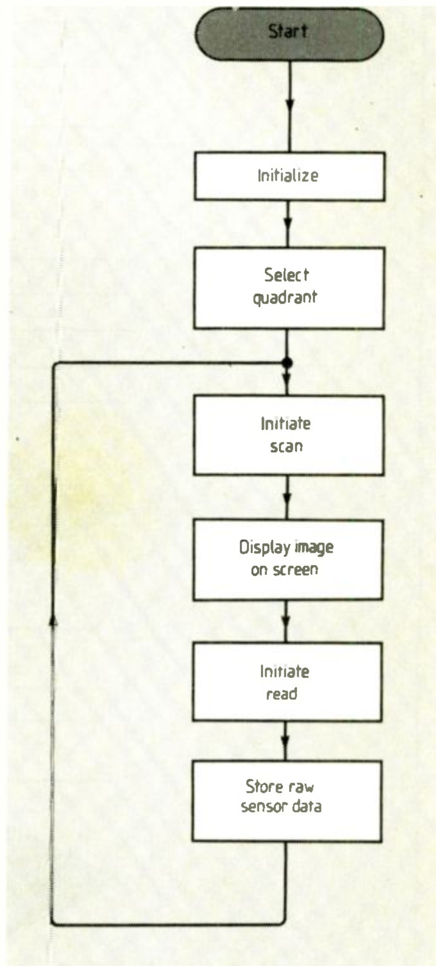
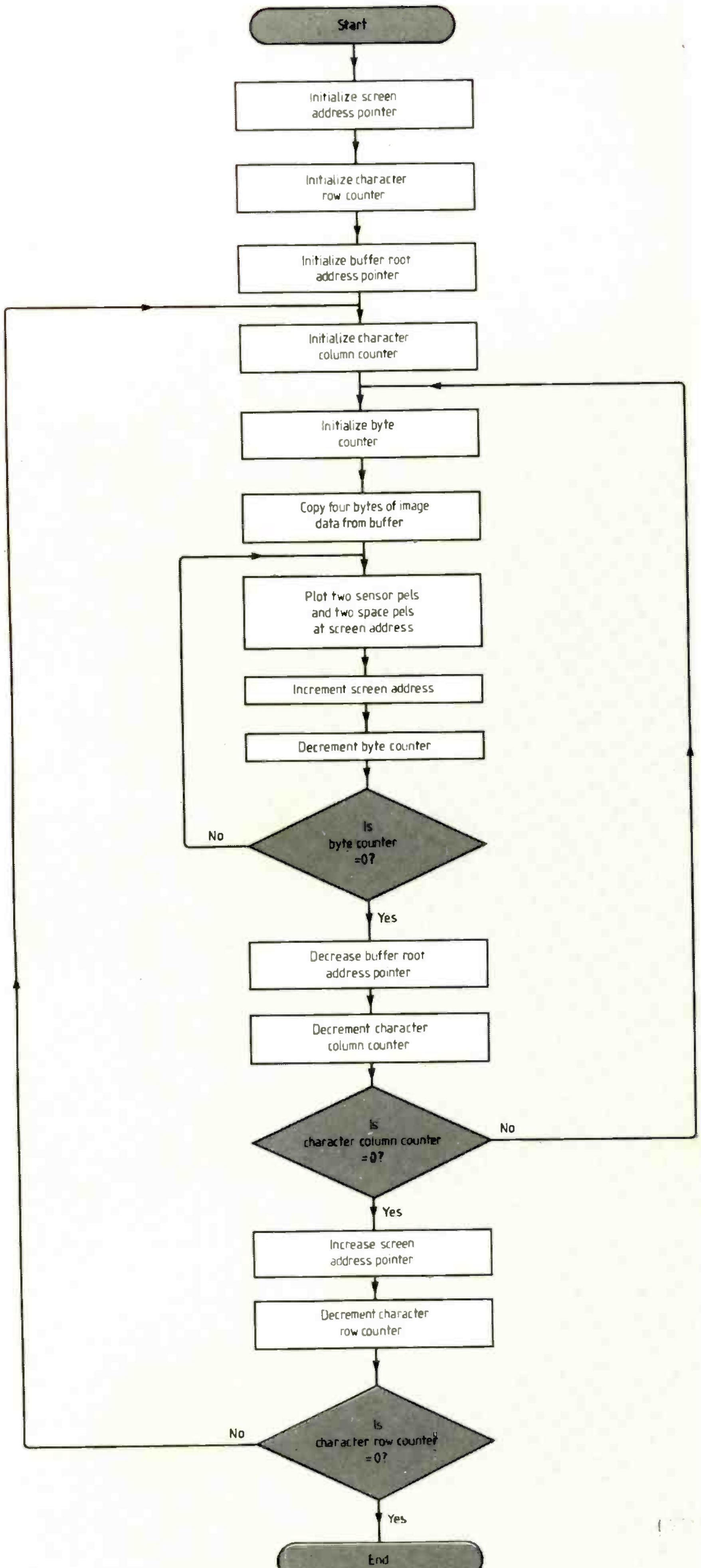


Fig.11. Basic image update routine.

Figure 12 shows an image display routine for mode 1 graphics on the BBC micro, and is inevitably partially specific to that machine. However, it should serve to illustrate the principles of writing software for other computers.

The screen of the BBC micro is controlled by a 6845, which is a textual or 'character'-oriented c.r.t. controller. In effect, it organizes the screen into 'character' rows and 'character' columns, each character cell using eight consecutive bytes of memory (regardless of graphics mode). In mode 1 the



screen is divided into 32 rows of characters, each containing 80 four-pel-wide character columns; each character cell is four pels wide by eight deep. It is necessary to employ an area of screen memory corresponding to 64×16 characters to plot an image of 256×128 pels. Therefore the image plotting routine basically consists of three nested loops, one to count the number of bytes in a character cell, and two more to count the character rows and columns respectively. Each counter should be linearly incremented or decremented to achieve the speediest method of driving the inner loop algorithm around the image plotting area.

The inner loop is repeated eight times under the control of the byte counter, and is responsible for the plotting of two active pels (plus two space pels) in each of the eight consecutive screen addresses comprising a character cell. The middle loop is under the control of the character column counter which causes the inner loop to be repeated 64 times, thereby plotting eight screen lines, each containing 128 active pels and 128 space pels; i.e. a character row. The final, outer, loop is thus controlled by the character row counter and allows 16 character rows of data to be plotted down the screen, yielding a total of 128 screen lines as required. Thus the final image matrix consists of 128 lines each of 256 pels, making a total of 32 768 pels; but it must be remembered that half of these are space pels not supplied by the sensor.

INNER LOOP ALGORITHM

Consideration of the method used by the hardware to pack the data into bytes will reveal that the position of any data bit, indexed by (IS32 column, IS32 row) in the memory buffer may be found by applying the following equations:

Byte address = buffer root address + column×16 + (row DIV 8) (1)

Bit number = 7 − (row MOD 8) (2)

These equations assume that the received image data stream is stored in consecutive bytes from the buffer root address upwards. They return the address in the buffer of the byte containing the desired bit and its bit number within that byte. If, for example, the buffer root address was &2800, then the sensor pels contained at the top of this data table would be as shown in Fig.13.

With the BBC computer in mode 1, each pel can take one of four colours. A screen byte contains only four pels and in this application two of these will be used to represent active photosites whilst the other two will represent space pels and must be left at the chosen background colour. Figure 14 assumes that the image is to be displayed in the top left corner of the screen (screen address pointer initialized to &3000), and shows the relationship between screen memory addresses and IS32 sensor pels required for the first few character cells.

Fig.12. Image display routine for the BBC Micro in mode 1. In this machine screen memory is organized into character-sized cells, a factor which must be taken into account in plotting graphics.

Figure 15 is an enlarged map of the bottom left corner of quadrant 1 on the sensor's 'upper' array (Fig.7, April issue, page 443). This region of the quadrant will be plotted in the top left corner of the screen to compensate for the vertical inversion discussed earlier and so it contains the data to be plotted in the screen memory addresses shown in Fig 14. Highlighted boxes in Fig.13 show where the corresponding pel data is stored in the buffer. Thus for each set of eight consecutive screen addresses, pel data from four widely separated bytes in the buffer is needed. Data highlighted in Fig. 13, 14, 15 reveals a repeating pattern which generates the algorithm for the second stage linearization process, which may be applied to the inner loop of Fig.12.

Before entry to the inner loop, the image data byte pattern containing pels that must be plotted into the character cell will have to be copied from the buffer. This is facilitated by setting up a buffer base-address pointer to locate the bytes that will be used. This pointer is initialized to an address near the top of the buffer, which is where the first data to be plotted may be found. At the end of each pass of the inner loop the pointer is moved to locate the next set of data.

Figure 14 shows that moving from a pel in one character cell to the corresponding pel in the adjacent cell on the same character row requires that the IS32 row numbers remain constant, whilst IS32 column numbers are decremented by two. Similarly, moving from a pel in one character cell to the corresponding pel in the adjacent cell in the same character column requires that the IS32 column numbers remain constant, whilst row numbers are decremented by eight. Using equations 1 and 2 we can deduce the two fixed decrements which are required to move the buffer base-address pointer as the character cell currently being plotted is moved around the screen in increments of one character position. Thus, in the prototype software, a pointer decrement of 32 bytes is required to move one character to the right, whilst a decrement of 1 byte is required to move one character down the screen.

The second-stage linearization algorithm is centred on the inner loop, which is responsible for plotting the sensor data into character cells under control of the byte counter. The byte counter holds the three least significant bits of the screen memory address and thus determines which line of the current character cell receives data. Sensor data to be plotted on even lines of the character cell is contained within one buffer byte (labelled Evendata in Fig.13), whilst data to be plotted on the odd lines is distributed amongst the other three relevant buffer bytes (labelled Odddata1-3 in Fig.13). It is also necessary to determine which two of the four pels described by each screen memory byte receive the photosite data; and this can be achieved by testing the byte counter to see whether it is odd or even. If the counter is even, image data will be found in Evendata and must be mapped into the outer pair of the four pels from a screen memory byte; otherwise, the data will be located in Odddata1-3 and the inner pair of

Memory Address	Bit7							Bit0	Comment
2800	R0 C1	R1 C1	R2 C1	R3 C1	R4 C1	R5 C1	R6 C1	R7 C1	BUFFER ROOT ADDRESS
2FD0 (2FB0)	R0 C125	R1 C125	R2 C125	R3 C125	R4 C125	R5 C125	R6 C125	R7 C125	
2FDE (2FBE)	R112 C125	R113 C125	R114 C125	R115 C125	R116 C125	R117 C125	R118 C125	R119 C125	
2FDF (2FBF)	R120 C125	R121 C125	R122 C125	R123 C125	R124 C125	R125 C125	R126 C125	R127 C125	odddata 1
2FEE (2FCE)	R112 C126	R113 C126	R114 C126	R115 C126	R116 C126	R117 C126	R118 C126	R119 C126	
2FEF (2FCF)	R120 C126	R121 C126	R122 C126	R123 C126	R124 C126	R125 C126	R126 C126	R127 C126	evendata
2FFD (2FDD)	R104 C127	R105 C127	R106 C127	R107 C127	R108 C127	R109 C127	R110 C127	R111 C127	
2FFE (2FDE)	R112 C127	R113 C127	R114 C127	R115 C127	R116 C127	R117 C127	R118 C127	R119 C127	odddata 3
2FFF (2FDF)	R120 C127	R121 C127	R122 C127	R123 C127	R124 C127	R125 C127	R126 C127	R127 C127	odddata 2

Fig.13. Buffer memory contents. R and C denote row and column addresses of the IS32 sensor. Highlighted boxes hold sensor data to be plotted at the extreme top left of the display (Fig.14). Figures in brackets are buffer addresses for the next character cell on the current character row. When one of these addresses is in force, IS32 column numbers must be reduced by 2; and so the last line in the table becomes —

2FDF	R120 C125	R121 C125	R122 C125	R123 C125	R124 C125	R125 C125	R126 C125	R127 C125	odddata 2'

Screen Address	Screen Pel Content 'CHARACTER' COLUMN 0				Screen Address	Screen Pel Content 'CHARACTER' COLUMN 1				
3000	R127 C126			R126 C125	3008	R127 C124			R126 C124	CHARACTER ROW 0
3001		R125 C127	R126 C125		3009		R125 C125	R126 C123		
3002	R125 C126			R124 C126	300A	R125 C124			R124 C124	
3003		R123 C127	R124 C125		300B		R123 C125	R124 C123		
3004	R123 C126			R122 C126	300C	R123 C124			R122 C124	
3005		R121 C127	R122 C125		300D		R121 C125	R122 C123		
3006	R121 C126			R120 C126	300E	R121 C124			R120 C124	
3007		R119 C127	R120 C125		300F		R119 C125	R120 C123		
3280	R119 C126			R118 C126	3288	R119 C124			R118 C124	CHARACTER ROW 1
3281		R117 C127	R118 C125		3289		R117 C125	R118 C123		
3282	R117 C126			R116 C126	328A	R117 C124			R116 C124	
3283		R115 C127	R116 C125		328B		R115 C125	R116 C123		
3284	R115 C126			R114 C126	328C	R115 C124			R114 C124	
3285		R113 C127	R114 C125		328D		R113 C125	R114 C123		
3286	R113 C126			R112 C126	328E	R113 C124			R112 C124	
3287		R111 C127	R112 C125		328F		R111 C125	R112 C123		

Fig.14. Top left-hand corner of the displayed image shows BBC mode 1 screen addresses.

pels must be plotted (Fig.14). This algorithm is summarized by the flowchart of Fig.16 which also indicates the way in which data bits may be extracted from their buffer bytes by right rotation of each byte prior to plotting.

Note that this algorithm assumes that the whole screen has previously been cleared to background colour: this improves speed by removing the necessity to plot the space pels individually.

When the screen memory byte has been written according to the algorithm, the screen address pointer (which was initialized to &3000) is incremented, and the byte counter must be decremented and tested for

Fig.15. Map of the IS32 sensor's surface shows the spatial relationship of photosites at the bottom left of quadrant 1. Row Y128 does not conform to the regular pattern and should not be plotted: this conveniently prevents the plotted image from exceeding 256×128. A similar type of irregularity exists in the columns X0 and X1, not shown here.

X256	X255	X254	X253	X252	X251	X250	X249	X248	X247	X246	X245	X244
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Y112		R111 C127	R112 C125			R111 C125	R112 C123			R111 C123	R112 C121	
Y113	R113 C126			R112 C126	R113 C124			R112 C124	R113 C122			R112 C122
Y114		R113 C127	R114 C125			R113 C125	R114 C123			R113 C123	R114 C121	
Y115	R115 C126			R114 C126	R115 C124			R114 C124	R115 C122			R114 C122
Y116		R115 C127	R116 C125			R115 C125	R116 C123			R115 C123	R116 C121	
Y117	R117 C126			R116 C126	R117 C124			R116 C124	R117 C122			R116 C122
Y118		R117 C127	R118 C125			R117 C125	R118 C123			R117 C123	R118 C121	
Y119	R119 C126			R118 C126	R119 C124			R118 C124	R119 C122			R118 C122
Y120		R119 C127	R120 C125			R119 C125	R120 C123			R119 C123	R120 C121	
Y121	R121 C126			R120 C126	R121 C124			R120 C124	R121 C122			R120 C122
Y122		R121 C127	R122 C125			R121 C125	R122 C123			R121 C123	R122 C121	
Y123	R123 C126			R122 C126	R123 C124			R122 C124	R123 C122			R122 C122
Y124		R123 C127	R124 C125			R123 C125	R124 C123			R123 C123	R124 C121	
Y125	R125 C126			R124 C126	R125 C124			R124 C124	R125 C122			R124 C122
Y126		R125 C127	R126 C125			R125 C125	R126 C123			R125 C123	R126 C121	
Y127	R127 C126			R126 C126	R127 C124			R126 C124	R127 C122			R126 C122
Y128		R127 C127				R127 C125				R127 C123		

an 'end of character cell' condition. If this condition is true, the inner loop is complete; otherwise it must be continued.

On completion of the inner loop it is necessary to perform housekeeping activities to ensure that the plot proceeds in an orderly fashion. Thus the character column counter and the character row counter must be decremented and tested for end-of-row and end-of-plot respectively. The end of row condition causes an offset to be added to the screen address pointer to ensure that the next character row is aligned with the previous one; the end of column condition causes the plotting routine to be terminated (Fig.12).

An enhanced version of the software described in this article is available on disc for the BBC Microcomputer at £7.50 including postage and the cost of the disc, from Bill Stone, 77 St Sampson Road, Broadfield, Crawley, West Sussex RH11 9RP. Please specify either 40 or 80 track disc. The IS32 sensor is distributed by Joseph Electronics, 2 The Square, Broad Street, Birmingham B15 1AP, tel. 021-643 2011.

References

1. Pugh, A.; Second generation robotics and robot vision: *Robotic Technology*, pp. 1-9, Peter Peregrinus Ltd., on behalf of the IEE, 1983.
2. Bray, A., Dickens, A. and Holmes, M. Appendix F – Screen mode layouts; Advanced User Guide for the BBC Microcomputer, pp. 462-471, Cambridge Microcomputer Centre, 1983.
3. Micron Technology: IS32 data sheet.

The IS32 interface hardware and software described in this article have proved to be invaluable tools in investigations into image processing, optical character recognition, industrial inspection and other research applications. Related work has produced a binary image processing software package for the BBC computer which produced the processed images shown in these articles.

Current work at Brighton Polytechnic is directed towards producing interfaces which offer vastly greater image update rates. These should demonstrate the true potential of this versatile image sensor in the field of robotic visual feedback. However, the present system is perfectly adequate to allow investigations into the feasibility of such applications, since it allows the cheapness, small physical size and, more fundamentally, the minimized *computational* expense, offered by the IS32 to be exploited in multiple viewpoint and/or 'eye-in-hand' modes of operation.

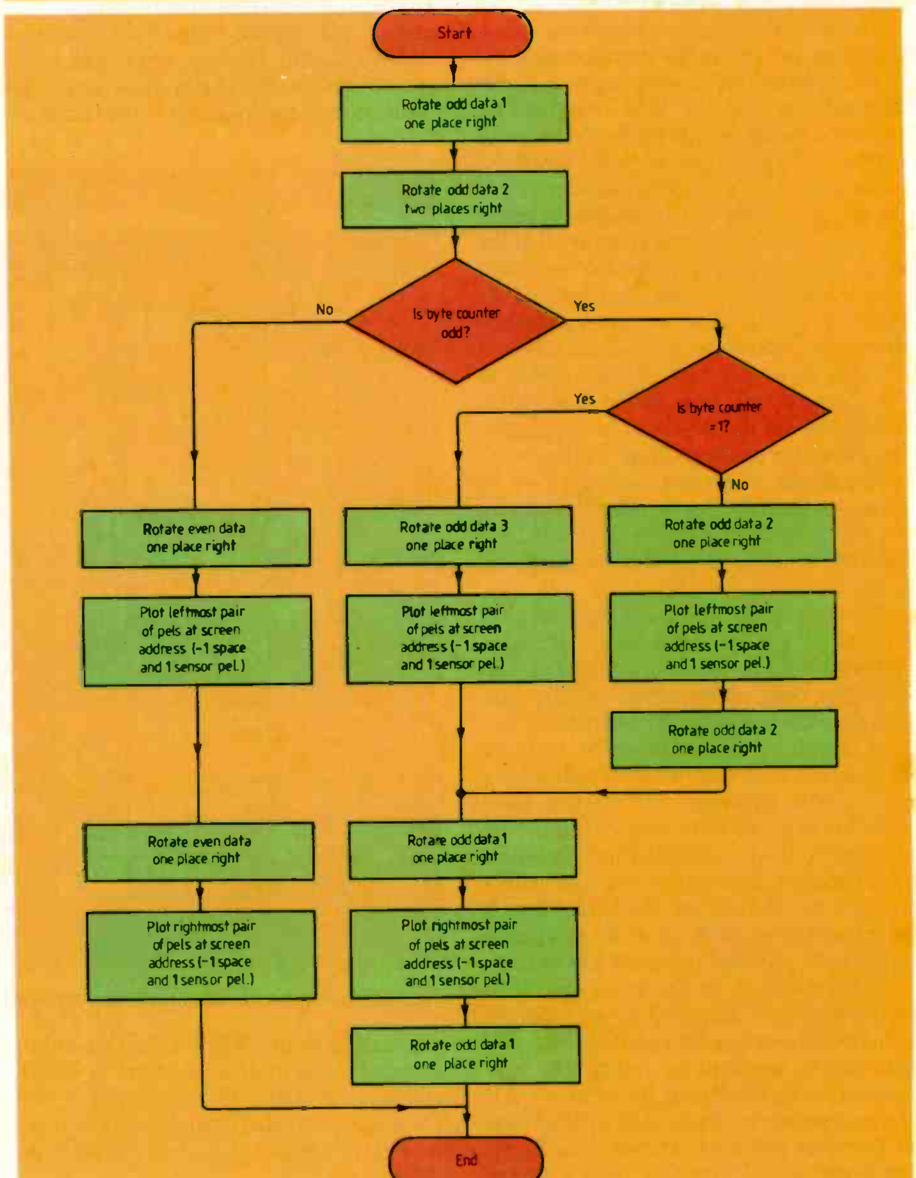


Fig.16. This inner loop flow-chart routine assumes that the screen has previously been cleared to background colour.

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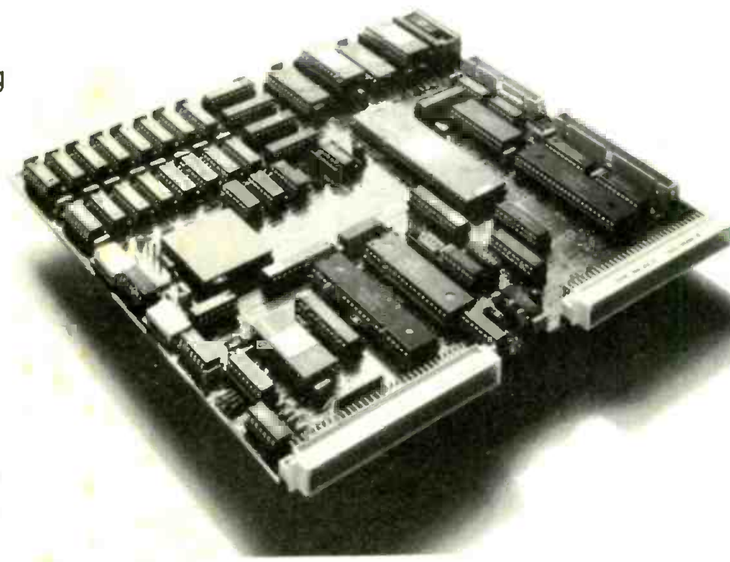

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Supercomputer for science and engineering

The inauguration of a new computer at the SERC Daresbury Laboratories heralds the launch of a programme of research into parallel computer architectures for scientific and engineering computation.

Central to the project is the T20 computer from Floating Point Systems which uses the Inmos Transputer. The fastest available computer systems operate at about 1Gflop* per second, and around 400mips. This rate is only obtained where large ordered sets of data (vectors) can be processed in an optimized assemblyline manner called pipelining. The performance of these supercomputers depends largely on how much of any program can be 'vectorized'.

Problems requiring teraflop speed include simulations of economic importance, such as modelling the flow of air over an aircraft, computing the side effects of drugs and long-term effects of pesticides and herbicides. Although algorithms for solving such problems still exhibit mixtures of vector and scalar operations, the program can often be sub-divided into sections or processes that can proceed independently in parallel. The controller of such a program has to know which processes can proceed in parallel, which must be run in sequence and which need to communicate with others; this is essentially the flow diagram of the program.

The T-series computer exploits this 'coarse-grained' parallelism. It consist of a number of interconnected nodes, where each node consists of a scalar and vector processor with shared memory and input/output channels. The control processor, the Inmos T414-20 Transputer, processes scalar integer code and controls 16 input/output serial channels, executing scalar integer code at between 1 and 10 million instructions per second and can manage four active channels at a time, each transferring at up to 2.5Mbyte/s. When the Transputer encounters a vector instruction of a scalar floating-point instruction it initiates the vector unit which can perform vector arithmetic at up to 16Mflops. The 1Mbyte memory system provides 12 and 64-bit operands to the transputer and vectors of 256 32-bit words or 128 64-bit words to the vector unit. A node occupies one board in the T-series machine.

The Daresbury Laboratory T-series is a T-20 and consists of 16 computational nodes, two system nodes, and a DEC Microvax II local front-end processor. The computational nodes are connected together as the corners of a four-dimensional cube (hypercube of order 4), so that each node uses four of its 16 channels for inter-node links. It can be upgraded by doubling the configuration and connecting the nodes to create a hypercube of the next higher order up to a maximum of 4096 nodes. The T-20 is able to perform arithmetic at speeds up to 256Mflops and 160mips. This is one quarter the performance of the fastest available conventional supercomputer at a cost of less than 5% of such a system, made possible because it is built from standard off-the-shelf components. For the same reason, the T-series requirements for power and cooling are minimal and its support costs are said to be low.

The system runs under Occam, but Fortran and C compilers are to be added. The T-20 will be accessible from Janet, the joint academic network, and the advanced research computing group at Daresbury will be working in collaboration with university groups for the development of software tools: they expect to attract interest from industry for advanced concurrent software. Initial studies are for software on computational chemistry, molecular modelling and surface physics programs.

* 10^9 floating-point operations per second.

OU to get Amstrad PCs

The Open University is to buy up to 4500 computers to form a pool of machines available for hire, or discount purchase, by students. Two suppliers have been selected; Amstrad and Akhter, with the majority of the orders (80%) going to Amstrad. The computers will be used in IT-related courses, and a grant of £2.25M is to be provided by the DTI.

Toward cad standards

A move toward a common software basis for electronic computer-aided design systems has been initiated by a newly formed group of European companies. A coordination of efforts to address the technical areas of persistent data, communications between concurrent cad applications, and man-machine interfaces, could offer a wider choice of hardware and software as well as protecting investments in existing applications, systems and training.

Specifications produced by the group, which includes Bull, CNET, ES2, ICL, Imec, Nixdorf-

EXHIBITIONS & CONFERENCES

4–5 June
Managing complexity in software engineering: International symposium, Freiburg Technology Centre, F.R. Germany. Organized by the European Workshop on Industrial Computer Systems. Details from Richard Mitchell, School of Information Sciences, Hatfield Polytechnic. Tel: 07072 79355.

15–18 June
International ISDN Conference and exhibition. Wembley Conference Centre, London. Online International. Tel: 01-868 4466.

16–18 June
Scottish Technology Week: including the Scottish Electronics Technology Show and Conference; the Scottish Factory Efficiency Show and Conference and OEM Scotland show and conference. Scottish Exhibition Centre, Glasgow. Cahners Exhibitions. Tel: 01-891 5051.

16–18 June
Networks 87. Conference and exhibition. Online International. Tel: 01-868 4466.

18–20 June
Television measurements: Third international IERE conference. Montreux, Switzerland. IERE, Tel: 01-388 3071.

22–26 June
Laser 87 Opto-electronics, microwaves. 8th International congress and exhibition. Munich Trade Fair Centre, F.R. Germany, MMA, Messegelande, Postfach 12 10 09, D-8000 München, FRG.

23–25 June
KBS 87 & Software Tools 87. Knowledge-based systems and software. Wembley Exhibition Centre, London. Online International. Tel: 01-868 4466.

24–26 June
APRS Show, (professional sound recording) Olympia, London.

24–27 June
SMT 87 Berlin: Surface mount technologies. International Congress Centre, Berlin. Details from AMK Berlin, Postfach 19 17 40, Messedamm 22, D-1000, Berlin 19, FRG.

26–30 June
BKSTS 87. 10th international film and tv technology conference and exhibition. Metropole Hotel, Brighton. BKSTS. Tel: 01-242 8400.

28 August – 6 September
International audio and video fair Berlin (incorporating MediaForum). International Congress Centre, Berlin. Details from AMK Berlin.

Cadlab, Olivetti, Sweden's NMP and Philips, would be in the public domain, and participants would implement subsystems based on the common specification for their own platforms or integrated applications. There is no restriction to membership of the group and other participants are expected to join, including third-party software suppliers and start-up companies like Qudos.

Pop video compact discs

The compact disc standard is to be expanded by Philips and Sony to combine video and audio of five minutes duration on a standard-sized disc with an additional 20 minutes of sound which could be played on existing CD players. It is also anticipated that a combination of disc sizes up to the 12in LaserVision disc will be accommodated on a single optical player suitable for both audio and video.

They are also developing the CD equivalent of a 'single' disc, which may become a 3in disc capable of carrying up to 20 minutes of sound audio and compatible with existing CD players by means of an adaptor, though say extensive research and consultation is still necessary before a final specification can be released.

Security in fund transfer

A co-operative marketing agreement, announced by GE Information Services and Racal-Guardata, enables users of GE's worldwide teleprocessing services to combat computer fraud. The first result of the agreement is an upgraded version of GE's money transfer system, incorporating new security features.

The standards for use within security systems for the financial services industry covering message authentication, key management, etc. are being defined and developed through American National Standards Institute (ANSI) and the International Standards Organisation (ISO) in Europe. The GE/Racal solution is a two-tier cryptographically-based system using the data encryption algorithm (DEA), firstly through the ANSI (X9.9 message authentication technique, and secondly by integrating personal authentication and linking the various components, using ANSI X3.92, with message authentication. Together, these two techniques provide a mechanism that ensures end-to-end message authentication and authorization that will identify the originating device as well as the authorizing office. This is a first step in the introduction of 'electronic signature.' The security equipment is tamper-resistant and operates as a peripheral device to the host computer. For a PC, this will be a security card that slots into the computer and for a mainframe will be a fault-tolerant security module. Each authorizing office is issued with a 'Watchword' generator, a hand-held calculator-like, tamper-resistant device used to calculate a digital signature.

Desk-top speech recognition

Computer recognition of human speech has moved dramatically forward in the demonstration of a desk-top system that has a vocabulary of 20,000 words: "97% of all the words likely to be used in business" according to IBM. The system characterizes user's speech in a 20 minute session by reading a prepared document containing 200 key sound patterns. The characterization is retained so the 'training' session is only needed once for each user. Punctuation is added verbally.

The PC-based system uses two high-speed subsystems, each containing an IBM-developed digital signal processor chip. The first subsystem transforms a speaker's words into a string of labels thereby encoding the speech. The second matches those labels against labels of words in the system's vocabulary.

The analysis of 25 million words in IBM office correspondence has provided a context so that the system can determine which is the most likely word to follow the two previous words.

A different approach has been taken by Siemens and Philips in their Spicos system. This allows a user to ask questions or command the computer.

The experimental system provides an automatic question-and-answer service that administers memoranda, letters and similar documents for each user. Its current vocabulary comprises about 1000 words. Commands and interrogative sentences must correspond to certain syntactical patterns culled from 200 typical enquiries. In conjunction with the specified vocabulary, these allow the system to recognize and analyse a total of about 1.5 trillion individual sentences. Recognition is supported by a pronunciation lexicon containing all possible words and a language model which maps the sentences in a network. By comparing the acoustic characteristics of the spoken words with those of reference patterns and applying statistical methods, word and sentence hypotheses are generated and passed on to a linguistic analysis module for further processing. This module constructs grammatically correct structures and transforms them into semantic trees for determining the meaning of the sentences. The subsequent dialogue module establishes the sentence type, interrogates the database and generates a system reply. This reply is converted into a sentence in natural language and then presented either on a screen or fed into a loudspeaker via a screenm synthesis module.

At present, Spicos' dialogue structure does not allow the system to respond dynamically to the user by posing useful replies such as requests to repeat unidentified words or to formulate a question more precisely. Neither does it permit reference to earlier parts of the dialogue. Development for the next phase includes an extension of the vocabulary and dialogue options, improvement of the speech synthesis and reduction of processing times.

SUMMER EVENTS

Further details of the following events from the Secretary Institution of Electrical Engineers, Savoy Place, London WC2, or telephone 01-240 1871 Ext. 330, unless otherwise stated.

2–3 June
UK telecommunications networks – Present and future. First IEE/IERE national conference, Savoy Place.
29 June
Photographic data acquisition: IEE lecture by Dr J.M. Burch in connection with a photographic exhibition at the Institution running from 29 June to 10 July.
5–10 July
Multivariable control for industrial applications: 2nd vacation school at the University of Strathclyde, Glasgow.
10–13 July
History of electrical engineering: 15th weekend school at Trinity College, Dublin.
19–24 July
Computer-aided tools for v.l.s.i. systems: 2nd vaction school at the University of Lancaster.
Transmission for telecommunications: 5th vacation school at the University of Aston.
Radio frequency techniques: vacation school at the University of Bradford.
26–31 July
Satellite communications systems: 3rd vacation school at the University of Surrey.
Software engineering for microprocessor systems: 5th vacational school at the University of Strathclyde, Glasgow.
27–30 July
Gathering the world through microwaves: International microwave symposium in Rio de Janiero, Brazil. Details from Prof A.A. de Salles, Catholic University of Rio, Rua Marques de S. Vincente 225, Gavea, Rio de Janiero, Brazil.
2–4 September
Speech Technology: CEP/IEE conference in Edinburgh. Details from CEP Consultants, 26 Albany Street, Edinburgh EH1 3QH. Tel: 031 557 2478.
6–11 September
Industrial digital control systems: vacation school at Someville College, Oxford.
Data communications and networks: 5th vacation school at the University of Aston.
7–11 September
European microwave conference: 17th MEPL/IEE conference at the Ergife Palace Hotel, Rome. Details from MEPL, Convex House, 43 Dudley Road, Tunbridge Wells, Kent TN1 1LE. Tel: 0892 44027.

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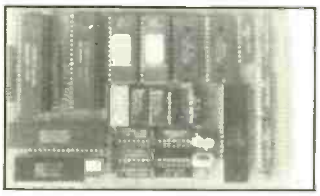

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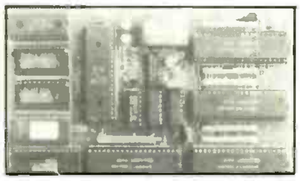

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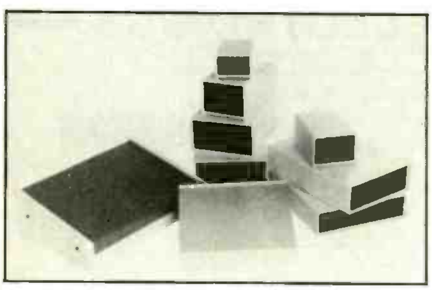

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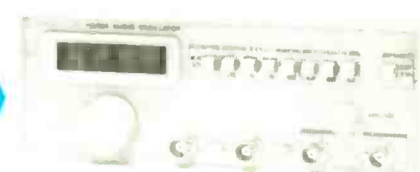

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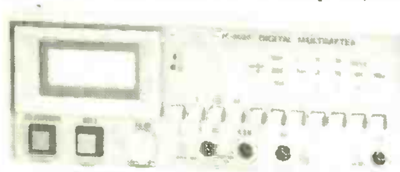

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Pioneers

6. William Thomson, Lord Kelvin (1824-1907): mathematician, scientist and engineer.

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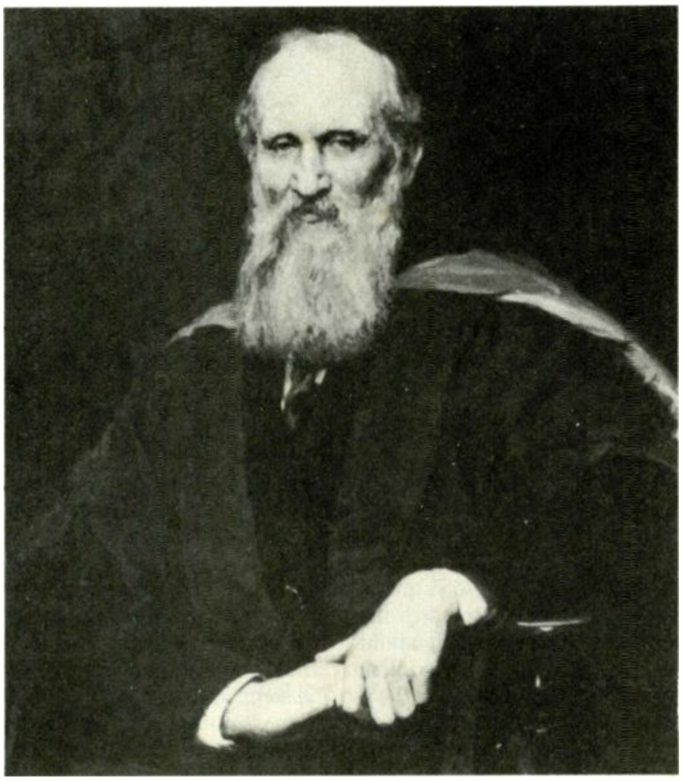


Institution of Electrical Engineers.

If only half of the praise heaped on to the memory of William Thomson is only half true then he was still a truly remarkable man.

Thomson, better known now as Lord Kelvin, was born in Belfast on June 26, 1824 the fourth of seven children of James and Margaret Thomson. His father was an eminent mathematician who, after the early death of his wife, devoted much attention to the personal tuition and encouragement of his children.

When William was seven years old his father was appointed Professor of Mathematics in Glasgow. With his brother James he attended some of his father's mathematics classes, where he displayed his prodigious mind at a tender age. On one occasion when no-one in the class could answer a question, William cried out, "Do, papa, let me answer."

In due course the two brothers became regular students at the university. When William was about 12 years old, a course in natural philosophy drew his attention to electricity; and his father ensured that the book learning was strengthened by practical work, something which was not then the norm. With his brother, William constructed frictional electrical machines and galvanic batteries, building whatever was needed from whatever was available. This 'activity' approach, as it might now be termed, helped develop the original and inventive mind that in later years was to be a driving force in electrical theory and practice.

In his final year at Glasgow, William Thomson's mind was captured by Fourier's theorem. This proved to be a cornerstone of some of his work on the transmission of electricity. He developed a great love for the French mathematicians.

After Glasgow University it was the turn of Cambridge, which he entered as an undergraduate at sixteen. His already-published paper on Fourier's Theorem caused a stir amongst fellow freshmen. He displayed musical talent, rowing skills and a zest for mathematics. One of his lifelong friends later described him at Cambridge as "a most engaging boy, brimful of fun and mischief." Shortage of money was often a problem: on one occasion Thomson wrote home explaining that he had only half-a-crown left.

After graduation in 1845 (he came second) he spent two months in Paris working in Regnault's laboratory, where he received a grounding in scientific research. (It was Regnault who calculated absolute zero to be −273°C.) Thomson met famous French mathematicians and studied Carnot's classic work on the motive power of heat. This helped to set him on the path to his own great work on thermodynamics.

Shortly afterwards he was appointed to the chair of Natural Philosophy at Glasgow, a position he was to retain for 53 years. There were many good candidates for it but the 22-year-old beat them all. His father's joy may be judged by a comment from a close friend: "The first announcement I had on the subject was your father's face as he came out of the hall where the election had been conducted. A countenance more expressive of delight was never witnessed."

For two years father and son held professorships in the same university, a happy situation ended untimely by a cholera outbreak in 1849.

Apparently Thomson was not an outstanding lecturer. His brilliant mind leaping through a problem would often leave his students exasperated. But according to one of them, his influence came from his magnetic personality.

One educational advance he introduced, however, was worth all manner of lecturing technique and that was his student laboratory – the first experimental laboratory for students in Britain. About 1850 he converted a disused wine cellar into a laboratory and there his students learned by doing. Later it became a research unit as he applied his own talents to solving technological problems. These efforts were rewarded by 70 patents, directorships, prestige and wealth. After his death the estate he left was valued at £162 000, a considerable sum in 1907.

Thomson made his mark in several fields of science and engineering. These included thermodynamics, electrical theory, submarine telegraphy, precision instruments, systems of units, and fundamental improvements to the marine compass. In the case of the compass he introduced magnets and soft iron to compensate for the effects of the ship's magnetism.

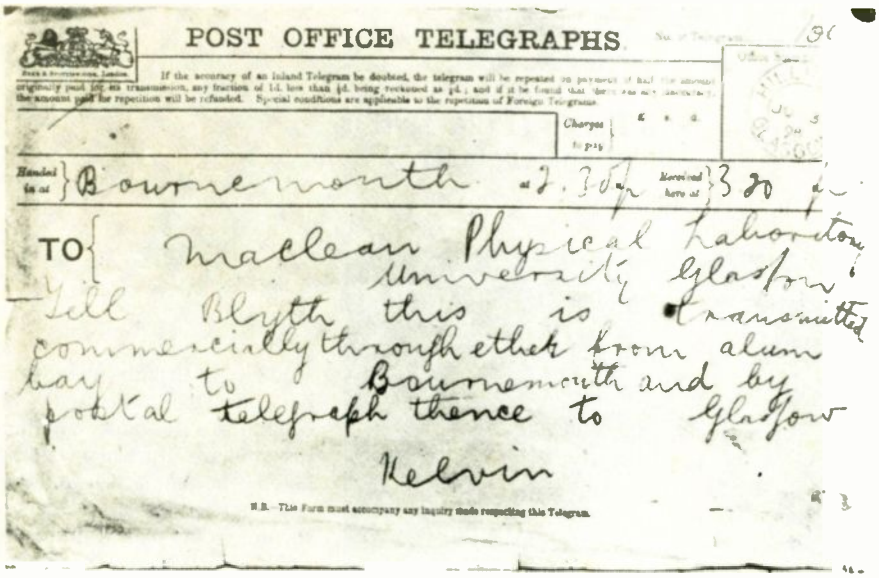
It is said that on seeing an early and crude version of the new compass the Astronomer Royal remarked "It won't do." "So much for the Astronomer Royal's opinion" was Thomson's comment.

Thomson helped establish thermodynamics as a pillar of science and his contributions there alone were enough to secure an honoured place in the history books. He championed J.P. Joule's work on the mechanical equivalent of heat at a time when Joule was finding it difficult to gain a hearing. He suggested the concept of zero energy of motion at −273°C and proposed the absolute temperature scale with zero at −273°C. In 1851 he proposed one of the two original versions of the Second Law of Thermodynamics (the more rigorous version was by R.J.E. Claussius, who gave us the word entropy). Five years later Thomson introduced the term kinetic energy.

THOMSON AND THE TELEGRAPH

But for those of us particularly interested in electrical and electronic engineering, Thomson's fame rests in the realm of electrical theory and practice, and in submarine telegraphy in particular.

By the mid-1850s telegraph engineers had turned their thoughts to spanning the Atlantic. This was to become one of the great engineering feats of the nineteenth century, akin to putting men on the Moon a century later. Thomson was an outstanding contributor to the eventual success of this project,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Handed in at } Bournemouth 2.30 p Received here at } 3.20 p

TO { Maclean Physical Laboratory University Glasgow.

Tell Blyth this is transmitted commercially through ether from alum bay to Bournemouth and by postal telegraph thence to Glasgow

Kelvin

N.B.—This Form must accompany any inquiry made respecting this Telegram.

The first paid radio telegram: Thomson's message from Marconi's experimental station at Alum Bay on the Isle of Wight, 1898 (Marconi Company).

for which he was knighted in 1866.

The first submarine cables had revealed that the speed with which messages could be sent was less for an insulated cable laid in water than for an uninsulated land line of the same length. Siemens and Faraday showed that this was due to the capacitance and resistance of the cable. Sending a pulse into a long submarine cable was seen as rather like charging and discharging a very long capacitor.

Thomson worked out the mathematics and showed that the transmitted pulse took time to grow to its maximum and needed time to decay. Further, the time increased as the square of the cable length. The product of capacitance and resistance (the time constant) was of crucial importance; and one of the first tasks he assumed on becoming a director of the Atlantic Telegraph Company was to reduce both the resistance and capacitance of the cable under preparation. In some cases the copper content of the wire was as low as 50%.

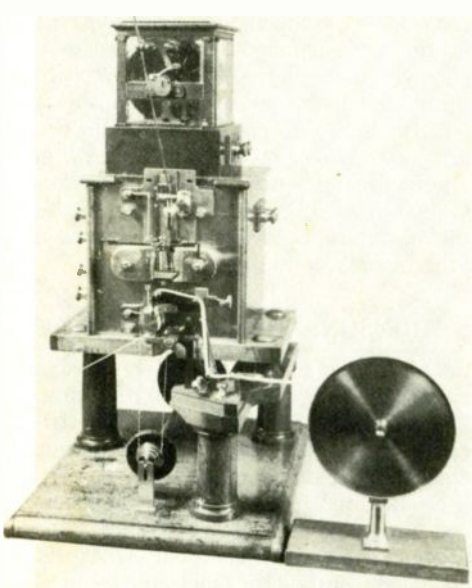
Thomson's mathematical ability enabled him to predict that the operation of the Atlantic cable would be slow but worthwhile. Normal telegraph instruments would be too insensitive for the job and so he devised his very clever (and justly famous) mirror galvanometer. This worked well during the laying of the 1858 cable. However, once the cable was operational, the low voltage transmitter and the mirror galvanometer detector were replaced against Thomson's advice with high voltage induction coils and conventional telegraph detectors. With something in the region of 2kV applied to it, the insulation failed.

This, with the failure of the Red Sea cable, culminated in the setting up of a British Government committee to examine the science and practice of submarine cables. The cable had been the first to be laid across the Atlantic, but was the third attempt at doing so. A lot of money had been lost.

The inquiry, of which Thomson and Wheatstone were members, reported in 1861. Of just over 11 000 miles of submarine cable laid, only about 3000 miles were working. Much was learned about the theory of electrical transmission, the effects of impurities on the conductivity of copper, and the design, manufacturing and handling of cables. With lessons learned, the prospects for a new try seemed good.

An attempt in 1865 failed with only 600 miles to go. The next year a new cable was laid successfully and the 1865 cable recovered, a new piece spliced on, and that cable also completed. Two cables linked Europe and America, as cables have continued to do to this day. Thomson, by the way, had sailed with every expedition.

Thomson invented two famous instruments for submarine telegraphy. They were the mirror galvanometer, mentioned above, and the siphon recorder.



The first ink-jet printer: Thomson's siphon recorder of 1867. Science Museum photograph, Crown copyright.

The first was a moving-iron instrument. A tiny mirror, about a centimetre in diameter, was attached to a fine steel needle. Together they weighed 0.1g. A narrow beam of light reflected from the mirror was focused on to a screen so providing a very long and weightless pointer. A small deflection was easily visible, allowing tiny currents to be detected.

This instrument was so sensitive that Latimer Clark, a well known telegraph engineer of the time, used it to detect a signal sent through the two Atlantic cables in series. His battery was a single tiny cell consisting of a silver thimble, a bit of zinc, and a few drops of sulphuric acid.

The second of Thomson's instruments, the siphon recorder, gave a permanent record of the message and was patented in 1867. Ink in a capillary tube was charged such that it was ejected on to a moving strip of earthed paper. A moving-coil detector drove the capillary tube so that the received signal produced a wavy line on the paper. Thomson was one of the first to employ moving coils rather than moving iron in a meter.

His interest in measurement led him to suggest setting up a British Association committee to propose a system of 'absolute' electrical and magnetic units, continuing the earlier work of Gauss and Weber. The committee was formed in 1861. Various suggestions were lost along the way; 'ohm' for example was originally proposed as 'ohmad', the unit of electrical charge (coulomb) was once the 'weber'. It was Thomson who suggested the term 'mho' for conductance – now replaced by the siemens, which was once a unit of resistance!

Thomson was one of the famous men of the nineteeth century. He was made Baron Kelvin of Largs in 1892. He married twice, but had no children; yet the name Kelvin is perpetuated in our unit of absolute temperature. Many societies elected him as president, including the Royal Society and the Institution of Electrical Engineers. He became a Privy Councillor in 1902.

After his death in 1907 he was buried in Westminster Abbey, close to the remains of Newton. Not many electrical engineers have gained that honour.

Although a scientific revolutionary in his youth he became part of the establishment, so to speak, in his old age. He had doubts about Maxwell's theory of electromagnetism, once calling it "the hiding of ignorance under cover of a formula". He favoured d.c. mains systems to a.c. and once regarded commutators as "frightful". On the other hand he was one of the first to equip his home with the new electric light bulbs. And when visiting Marconi's experiments on the Isle of Wight in 1898 he sent a couple of messages to fellow engineers on the mainland for which he insisted on paying. These according to the Marconi company, were the first radio telegrams to be paid for.

Next in this series of pioneers of electrical communication: Alexander Graham Bell.

Tony Atherton is on the staff of the IBA's engineering training college in Devon.

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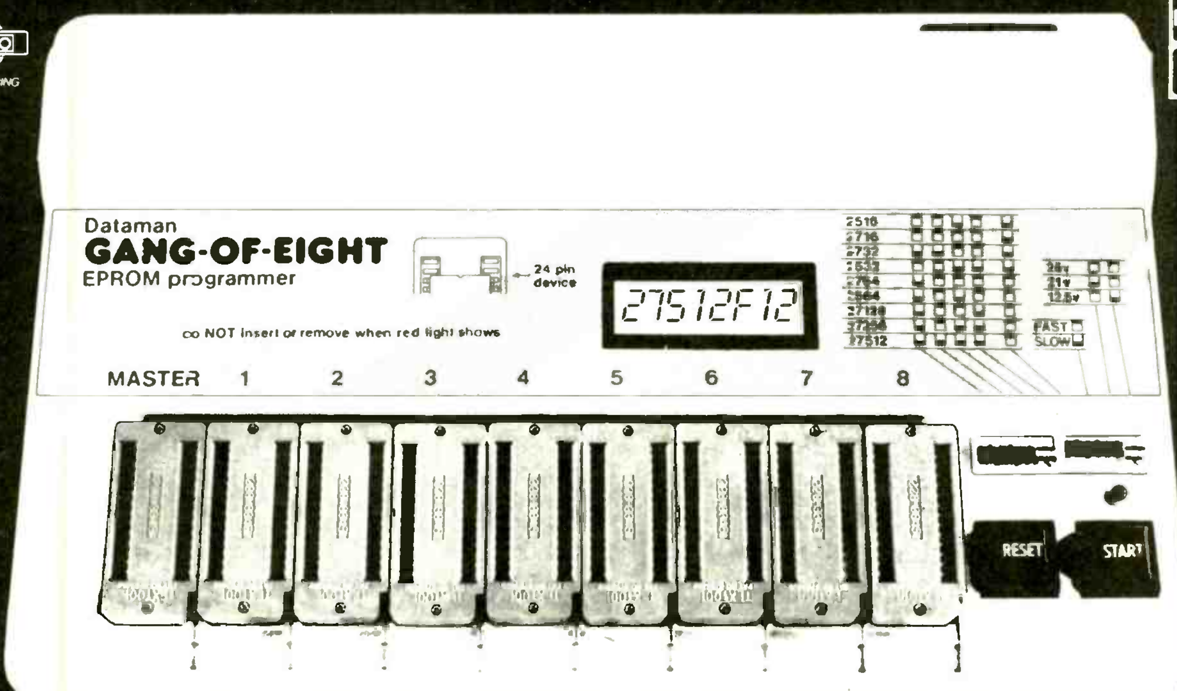

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SATELLITE SYSTEMS

Millimetre-waves for the military

The account of Britain's Skynet-4 military comsat given in the May issue mentioned the use of e.h.f. in the communications payload and promised more details to come. A paper entitled 'The Skynet-4 e.h.f. payload and future developments' was due to be given at an IEE colloquium by two people from Marconi, the payload manufacturers. In the event this paper turned out to be less specific than the title suggests. "Security requirements have obliged us to tone down our presentation to some extent" explained N.F. Kington of Marconi. No doubt the customer, the Ministry of Defence, had become wary of releasing military information after the Zircon affair a few months earlier and had imposed something of a clampdown on Marconi.

Nevertheless Mr Kington was able to discuss and show photos of experimental e.h.f. transponder hardware intended to use in a future Skynet-4 spacecraft. This comprised receiving equipment for the 43.5 to 45.5 GHz military comsat uplink band and transmitting equipment for the corresponding 20.2 to 21.2 GHz downlink band. In addition, M.R. Walbridge of the Royal Signals and Radar Establishment (RSRE) and M.N. Sara of Siemens Ltd described in some detail a millimetre-wave earth terminal built at RSRE, Defford, Worcestershire, for working with the Skynet e.h.f. payload. This terminal is capable of radiating several hundred watts over the band of 2 GHz at 45 GHz from its 6-ft diameter Cassegrain parabolic antenna. It is based on a high-power, water-cooled, coupled-cavity travelling-wave tube which, Mr Sara said, is capable of delivering over 1 kW of r.f. power at 44 GHz.

The Skynet-4 spacecraft originally intended to be launched in 1986 by the space shuttle (see May 1987 issue) is now being held in store by British Aerospace. We have been told that this particular satellite does not carry an e.h.f. payload and that the experimental mm-wave equipment described by Mr Kington will be used for future Skynet spacecraft. Accepting the general air of mystery that inevitably surrounds a military communications project, it is still reasonable to ask why millimetre waves are being used at all, in view of their attenuation problems and the considerable difficulty and cost of engineering e.h.f. radio equipment.

One main answer was given by D.P. Haworth of RSRE at the IEE colloquium – "survivability". This means the ability of the military comsat system to continue operating in the face of jamming and/or interception of signals. Mr Howarth explained that the use of e.h.f. helps in dealing with jamming because there are limitations on the e.i.r.ps achievable from very large jammers at all frequencies, whereas small satcom terminals have e.i.r.ps proportional to the square of the frequency for a given antenna diameter. Furthermore, e.h.f. offers more scope – than, say, s.h.f. – for anti-jamming systems such as nulling antennas and spread-spectrum communication.

Nulling antennas can be interferometers or phased-array structures. The larger the ratio of the antenna baseline to wavelength the finer the spatial discrimination available. Narrow antenna beamwidths at earth terminals help against downlink jamming. And as for spread-spectrum techniques, Mr Haworth said that the wider bandwidth available at e.h.f. (say 2GHz) relative to s.h.f. meant that greater protection against jamming could be obtained because the protection was broadly equal to the ratio of the spread-spectrum bandwidth to the data bandwidth.

Such wide bandwidths called for the frequency-hopping rather than the direct-sequence type of spread-spectrum technique (see May issue). Future military satcom systems, he thought, would have 44-GHz uplinks using frequency hopping over 2 GHz with de-spreading in the spacecraft in order to prevent power capture of the transponder.

On the question of interception, Mr Haworth said that e.h.f. helped because, for a given size of transmitting terminal, the ratio of the terminal's main-lobe to sidelobe gain increased as the wavelength shortened. This would be a disadvantage to an interceptor at the higher frequencies. The use of spread-spectrum over a wide bandwidth would both reduce the need for high power transmission and force an interceptor to widen his pre-detection bandwidth, thus making himself more susceptible to his own front-end thermal noise.

Although gaseous and rain absorption were a problem for satellite communications on millimetre waves, went on Mr Haworth, this would affect the interceptor's signal path to the satellite more than the user's. The interceptor's path would probably lie at a very low angle of elevation compared with that of the comsat user and so would pass through correspondingly more of the water vapour etc. that caused the attenuation.

GOES H observes the environment

The latest contributor of meterological information to the World Weather Watch programme is the GOES H satellite, launched by a Delta rocket in February this year. It is the eighth in a series started in the 1970s and operated by the US National Oceanic and Atmospheric Administration (NOAA). The acronym GOES stands for Geostationary Operational Environmental Satellite. It indicates first that the spacecraft are geostationary – GOES H being stationed at 75°W – as distinct from the many polar orbiting weather satellites with orbital periods in the region of 100 minutes.

Secondly the name indicates that these are more than weather satellites. Environmental satellites not only take weather pictures of the Earth but provide detailed measurements of such things as radiation, temperature, magnetic fields, water vapour concentration and atmospheric pollution surrounding the globe.

GOES H, built by Hughes, replaces and is identical to GOES G, which was destroyed on launch in May 1986 when the Delta rocket carrying it went out of control. From its orbital position at 75°W it has a view of the Atlantic Ocean and will supplement enviromental information from the Pacific Ocean region already supplied by GOES F (also built by Hughes) stationed at 135°W. For a while GOES F was the only satellite of this kind serving the Americas. NOAA moved it temporarily westward from its normal position over the Pacific to a more central point above the Americas, but from here it did not have a very extensive view of the two oceans.

The new spacecraft, like its predecessors, is cylindrical in construction, with a diameter of 2.15m and a height of 3.5m. Solar cells on the cylindrical surface supply more than 300W of power, while nickel cadmium batteries take over during eclipses. The whole structure spins at 100 rev/min to provide gyroscopic stability and thermal equilibrium.

Visible and infra-red images of the Earth and its atmosphere are taken by an elaborate radiometer called a visible/infra-red spin scan radiometer atmospheric sounder (v.a.s.). Built by the Santa Barbara Research Centre of Hughes, it simultaneously produces visible images with a resolution of 950m and infra-red images with a resolution of 6.9km every 30 minutes. These images are built up from a sequence of scans produced by the rotation of the spacecraft. As the satellite spins west-to-east at 100 rev/min a mirror receiving the radiation is stepped 0.01° at each revolution, thus producing scanning lines – actually 8-km wide strips – running from north to south across the Earth's disc.

The v.a.s. is housed in a beryllium cylinder 0.66m in diameter and 1.5m long. The mirror collecting the radiation, mentioned above, is actually part of a Ritchey-Chrétien type of reflecting optical system. This arrangement, common in modern astronomical telescopes, uses hyperboloidal primary and secondary mirrors to avoid the coma and spherical aberration that affect Cassegrain and other classical optical systems. As a result it has a wider field of view than these types.

Altogether the v.a.s. has 26 detectors. Eight are photomultiplier tubes for the visible images, six are solid-state devices for the infra-red pictures, and twelve are filters in the spectral region for atmospheric measurements. Data produced can be used to calculate three-dimensional profiles of several atmospheric parameters including temperature and water vapour.

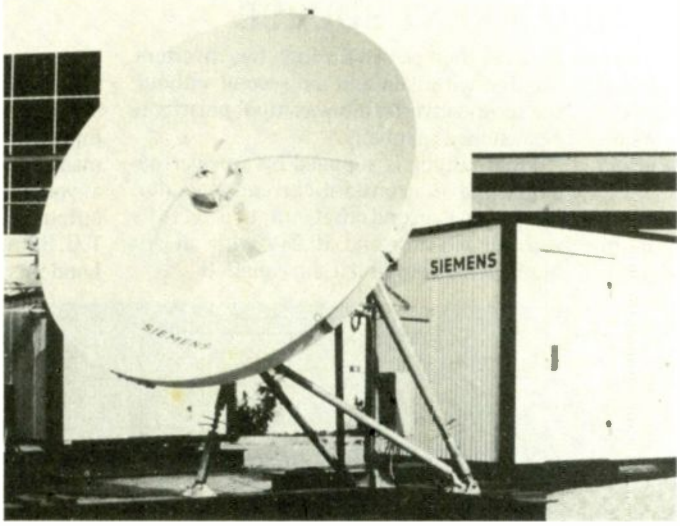
It takes just over 18 minutes for the v.a.s. to run through the 1,821 scan strips necessary to build up a full image of the viewing area (about one-third of the planet). This information is transmitted every 30 minutes in the meterological satellite downlink band (1670 – 1710 MHz) to NOAA earth stations. Here it is processed and re-transmitted through the GOES satellite, used as a comsat, to meteorological receiving stations.

In addition to the v.a.s. imaging detectors, GOES H carries instruments to measure magnetic field strength and direction in the vicinity of the spacecraft and others to measure solar x-ray flux and sense the energetic particles that form the solar wind and radiation belts around the Earth.

A completely new feature of GOES H, compared with previous spacecraft in this series, is that it becomes the first geostationary weather satellite to operate in conjunction with the COSPAS-SARSAT international rescue system (see March issue, p.264). All spacecraft hitherto used in this rescue system have been low-altitude polar orbiting satellites. GOES H carries an experimental 406-MHz receiver to pick up signals from rescue beacons. The idea is that these distress signals will be relayed to the low-altitude satellites and thence into the general COSPAS-SARSAT network.

The two American GOES spacecraft are among a total of five geostationary weather/environmental satellites strung out around the world at roughly 70° intervals. The other three are Europe's Meteosat positioned at 0°, India's INSAT at 74°E and Japan's GMS at 140°E. Together with the polar orbiting satellites mentioned above they contribute to all the other meteorological information given by 9000 land stations, 7000 ships and 850 balloons in the World Weather Watch (WWW) programme. This scheme was set up in 1968 by the World Meteorological Organization, a specialised agency of the United Nations.

Information is processed at three centres, in Melbourne, Moscow and Washington, to provide global weather forecasts, which are finally produced at Bracknell (UK) and Washington (USA). Individual countries participating in the scheme (now about 150) extract information from this world picture to make their own local weather forecasts. Satellites, because of the large areas they observe, have been particularly valuable in constructing the synoptic charts needed by WWW and have also helped to improve the accuracy of forecasting.



The Deutsche Bundespost (West German Post Office) has acquired 15 of these Siemens small earth terminals with 4.2m-diameter antennas for working with the ECS (European Communications Satellite). They will handle traffic for the Satellite Multi-Services (SMS) system, provided by a special ECS transponder, for business communications. The SMS system, intended for major business users, is based on digital channels with data transmission rates of 64kbit/s and above.

Luxembourg's satellite television

British Telecom has signed an agreement with SES (Societe Europeenne des Satellites) of Luxembourg for the use of up to eleven of the transponders in their Astra satellite due to be launched in 1988. The intention is to distribute UK television programmes by satellite into Europe. The transponders would receive feeds from the UK and carry a mixture of English and other language programmes. BT plans to set up a new antenna as its London Teleport to provide an uplink to the Astra satellite.

The geostationary Astra will be one of the well-established Series 4000 spacecraft manufactured in the USA by RCA Astro Electronics. From its orbital slot at 19°E it will provide 16 channels in part of the Ku band (11 GHz), transmitting from 45-W travelling-wave tube amplifiers. The 16 channel frequencies range from 11435.5 MHz, vertically polarized, to 11214.25 MHz, horizontally polarized, with intervals of 14.75 MHz and alternate vertical and horizontal polarization. There will also be six spare channels available. The transponders include GaAs f.e.t. wideband receivers, dual-mode quasi-elliptic input multiplexers, low-loss output multiplexers, limiter amplifiers and t.w.t.a. linearizers.

According to BT, Astra will radiate sufficient power to allow reception with dishes as small as 60cm diameter, in an area bounded by Edinburgh, Stockholm, Milan and Bordeaux.

SES, a Luxembourg-based international company, has a wide European shareholding, including, incidentally, Thames Television in the UK. It is authorized by the Luxembourg government to use the satellite frequencies and orbital position allocated to the country for a television distribution satellite service. The company is the final outcome of several years of politicking, quarrelling and horse-dealing between a variety of interests attempting to set up a European satellite television broadcasting enterprise – though not d.b.s. – as a follow-up to the well known Radio Luxembourg commercial radio station serving Europe. Along the way to SES was a project called Coronet, which, because of a suspicion that it would be bringing more American culture into Europe, was dubbed by the French "the Coca-Cola satellite."

Astra, however, although made in the USA, does not resemble a cylindrical tin can. Structurally it has a rectangular body measuring 2.9×1.6×1m with two solar-cell 'paddles' protruding. This is stabilized in three axes by momentum wheels. The main antenna reflector is not a fixed type as used in earlier RCA satellites. It has two overlapping, orthogonally-grid surfaces fed by horizontally and vertically polarized horn arrays. This arrangement is said to give a high ratio of focal length to diameter, providing higher performance and more precise beam shaping relative to the earlier design. Electrical power storage is given by nickel-hydrogen batteries.

A subsystem for measuring and controlling the attitude of the spacecraft is claimed to give an antenna beam pointing accuracy up to ±0.03°. On station, the roll and yaw information is provided by rate-integrating gyros and the attitude is controlled by pulse modulation of reaction-propulsion thrusters. Any errors in beam pointing, caused by such effects as thermal distortion, can be corrected by adjustments from the ground to a pitch control loop (for east/west) and to the momentum-wheel platform (for north/south). The attitude control system uses a stored program in a microprocessor, and this, in conjunction with observations from the ground, allows diurnal and seasonal beam pointing deviations to be corrected.

A ground control centre for the Astra satellite is being set up in the Chateau de Betzdorf, former country residence of the Grand Duke of Luxembourg. Two uplink earth terminals have been built in the gounds.

Satellite Systems is written by Tom Ivall.

CIRCUIT IDEAS

DIGITALLY-CONTROLLED CURRENT SOURCE

In applications where bandwidth is unimportant this digitally-controlled power source can replace expensive commercial supplies. Output current is programmable in 1mA steps up to 256mA and the power amplifier can dissipate 3W.

While the $\overline{\text{ENABLE}}$ line is high, 8 bit, data is latched within the ZN428 digital-to-analogue converter. Analogue output is buffered then passed through two inverters, the first with gain and the second without; the second inverter allows output polarity to be switched manually.

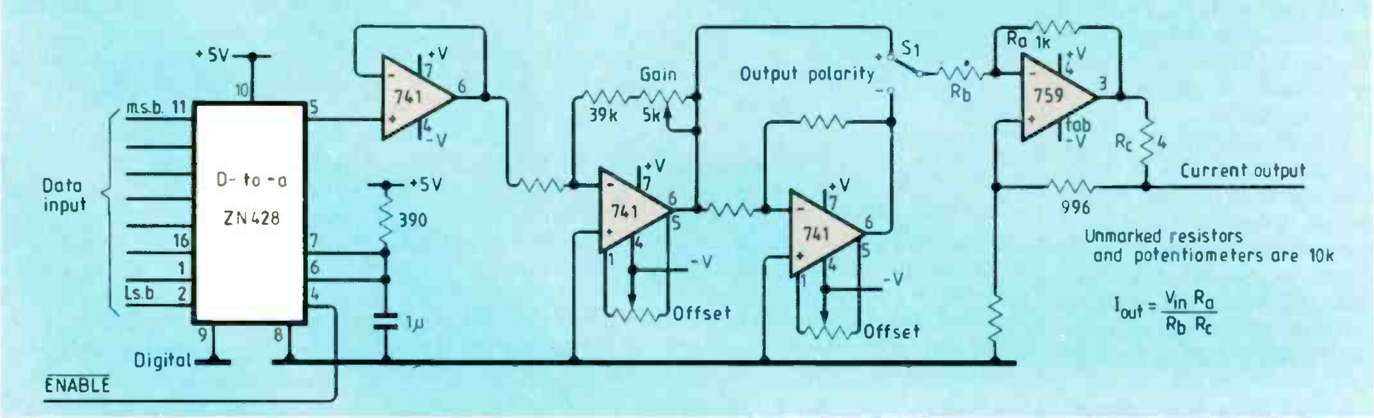
Final output is supplied by a power op-amp wired as a constant-current generator. By varying gain and offset, output is set to 0V with all bits low and 10.24V with all bits high, giving 40mV/bit. Gain equation

$$I_{out}=\frac{V_{in}R_a}{R_bR_c}$$

results in 1mA/bit for the values shown.

By offsetting the first inverter's positive input and adjusting gain, the circuit can be made bipolar. Rewiring the power op-amp as a voltage follower gives constant-voltage output.

T.G. Barnett
London



MEMORY AND I/O ACCESS TRACER

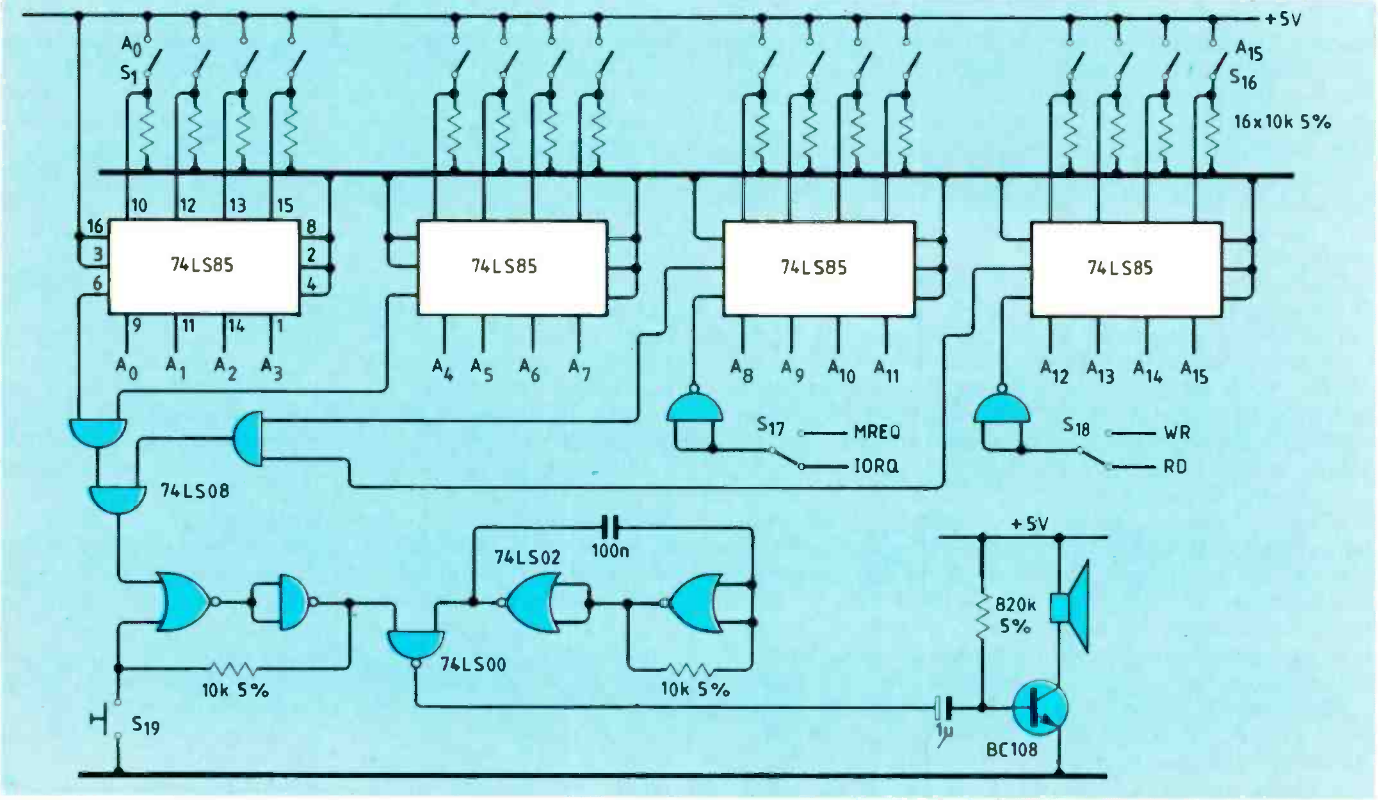
Software debugging can be much easier if you know whether or not a particular memory location or i/o port is being accessed, and whether it is being read from or written to. An audible signal is given by this tracer when a specified address or i/o port is accessed.

Switches S_{1-16} set the trigger address, a closed switch representing binary one. Selection of a memory or i/o port is done using S_{17} while S_{18} determines whether triggering occurs on a read or write operation. Once triggered, the alarm continues until S_{19} is pressed.

To test for stack overflow, the tracer can be set to a memory location several bytes below the stack pointer. The circuit was designed for Z80 systems but it can be used with any eight-bit processor, provided that the address bus is t.t.l. compatible.

Using exclusive-or gates instead of four bit comparators reduces cost at the expense of chip count.

Joseph Duffy
Howth County Dublin



CIRCUIT IDEAS

DYNAMIC-RAM CONTROLLER FOR 68000/08/10

This circuit is cheaper than a TMS4500, and can easily be configured to suit your processor, ram-size, ram-type and refresh requirements. It should be suitable for both eight and sixteen-bit versions of the 68000 microprocessor.

Refreshing is done approximately every 15μs and the refresh cycle is only initiated when the processor is not using the ram. All ram-accesses are delayed until the refresh cycle is finished. One 74LS221 makes a 'precharge delay', which delays any further ram activity for about 100ns.

The circuit is optimized for 150ns d-rams and in this case the clock frequency can be up to 20MHz. If d-rams with other access-times are to be used clock-frequency, the precharge-delay and the REFRAS pulse should also be changed. I have not tried out this circuit idea.

Jesper Udby
Farum
Denmark

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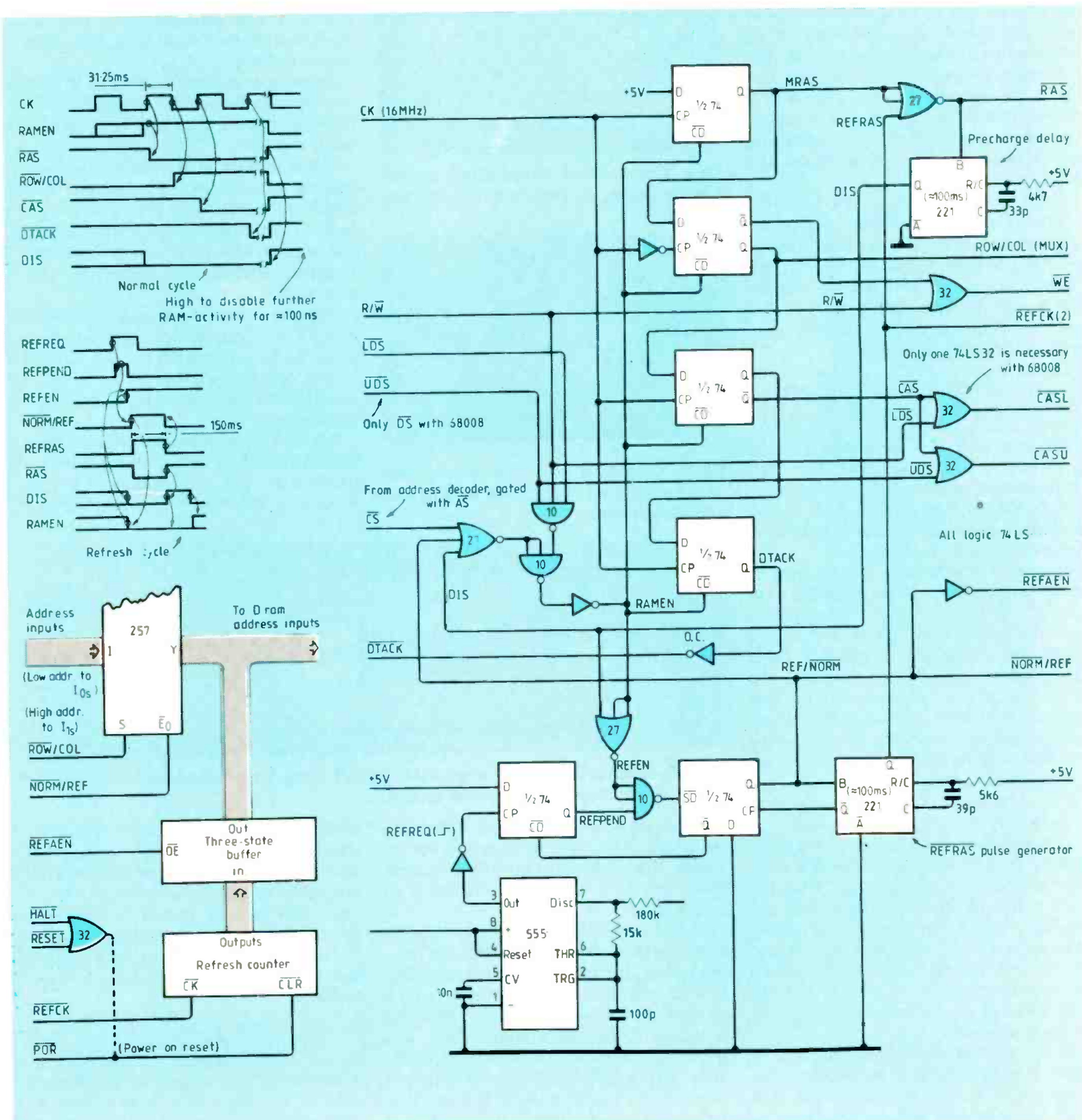

Self-sensing heating elements

A heating element which acts as its own temperature sensor has advantages over the traditional arrangement of separate heater and sensor.

CHARLES H. LANGTON

Whilst carrying out research some time ago into precision temperature control systems employing thermistor sensors, one of the problems encountered was due to the self-heating of the sensor when measuring its resistance. This is because to measure the resistance (and hence the temperature) it is necessary to pass current through the device. The problem was largely overcome by interrogating the thermistor with a very short duration pulse.

From that time, however, the possibility of making use of this self-heating disadvantage remained in the author's mind, it being felt that one single device (thermistor) may be used as sensor and heating element combined. An opportunity to test this approach occurred recently, and this article is an account of the investigation.

ADVANTAGES OF COMBINED ELEMENT-SENSOR

The normal method of thermostatic control is to employ a sensing device such as a thermocouple or thermistor in association with the heating element and there is little doubt that when high accuracy of control is required this is the best method.

In certain applications, however, the presence of the sensor is not desirable. For example, if the rate of production of heat is low, the sensor may absorb too high a proportion of the heat energy. In other cases, where fluid flow is involved, the sensor may present an obstacle in the flow path. In yet another instance, if the surface temperature of the heating element is the criterion, and the sensor is mounted on the heated surface, there will inevitably be a thermal impedance between the surface and the sensor, resulting in possible errors.

The objections indicated above are minimized if the heating element also acts as its own temperature sensor. The following notes relate to an investigation into the viability of such a system. It must, of course, be accepted that if such a self-sensing heater is employed, the one device must perform two functions and either function, or both, may represent a compromise rather than an optimum solution.

It will be appreciated that if a mass of material is to be kept at an accurately *steady* temperature, the sensor must be located close to the heating element. This reduces the time lag between the element changing its temperature, and it detection by the sensor. The ideal situation in this respect must, therefore, be when the heater is its own sensor.

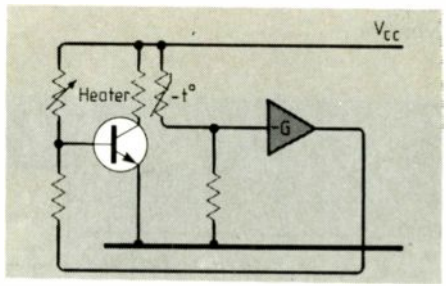

Fig.1. Conventional temperature control system using a separate heater and sensor.

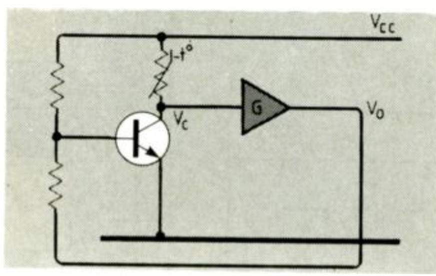

Fig.2. Combined element-sensor, the direct equivalent of Fig.1, will be unstable and will not work.

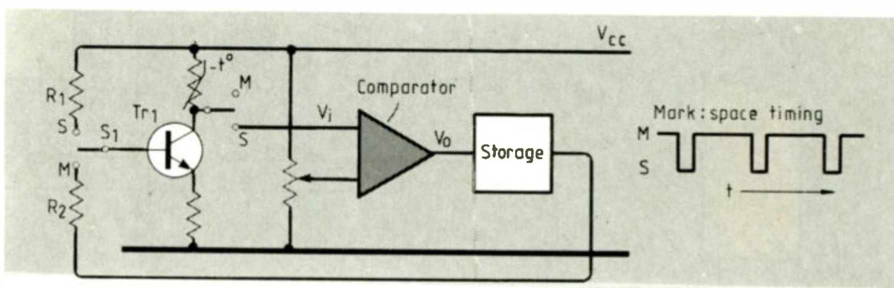

Fig.3. Functional diagram of a workable circuit using a combined sensor and heater based on a time-shared thermistor system.

At this stage, it may be as well to remind ourselves that in any so-called thermal sensing system, the system is really responding to a parameter of the sensing device, which in turn should, we hope, be a repeatable function of the temperature. Thus, if a thermistor is used as the sensor, its resistance R_{TH} at a given temperature θ will have a unique value R_θ, and when it is adjusted to run at this temperature all that happens is that the system maintains the resistance at R_θ, when equilibrium is accepted. If the thermistor resistance R_{TH} changes, then the feedback compensates the control until once again R_{TH} becomes equal to R_θ and equilibrium is restored.

Suppose now a fault occured in the form of a high-resistance joint in series with the thermistor, this dry joint having a constant, small resistance r. The system would now continue to function, but equilibrium will be reached when $R_{TH}+r=R_\theta$. For this to be possible, the thermistor resistance will now be $R_\theta-r$, which means that the temperature will be greater than it should be (assuming a negative temperature-coefficient thermistor).

The above remarks are equally true when using a self-heating element. The system responds to a parameter of the element-sensor, and this we bear in mind. In the investigation the parameter monitored is the resistance.

A typical application is described in which a small quantity of fluid is kept at a constant temperature. The element-sensor being immersed in the fluid must be capable of surviving in this environment. The device should have electrical power rating convenient to produce heat at an adequate rate, and have a temperature coefficient of resistance such that the required sensitivity of detection of temperature change is achieved. It should have a thermal inertia considerably less than that of the fluid mass it is controlling.

CHOICE OF THERMISTOR

A thermistor was chosen as the element-sensor. This was chosen because the high temperature-coefficient of resistance of such devices makes for good sensitivity to temperature change, and they can be (but not all production devices are) reasonably repeatable. Also, it is not difficult to choose a device which has convenient parameters for use as a low-power heater.

The n.t.c. thermistor is subject to runaway when clamped across a fixed voltage source. If used as a heating element in this way, the n.t.c. device is off to a bad start. On the other hand, the temperature of such a device tends to stabilize if driven from a constant-current source. Hence, a n.t.c. thermistor driven in this way presents a much more appealing case right from the outset.

In contrast, a p.t.c. thermistor tends to instability and runaway when supplied with a constant current, but is stable when connected to a constant-voltage source.

Owing to the wider choice of types, a n.t.c. device was employed in the present investigation. This was a rod-type thermistor, approximately equivalent to the Mullard VA1104. N.t.c. thermistors have a high resistance at room temperature, falling exponentially as the temperature rises. This resistance/temperature characteristic is described by the equation

$$R_\theta = R_T \exp\left(\frac{B}{\theta} - \frac{B}{T}\right) \qquad (1)$$

where R_θ is the resistance at θ Kelvins.

In practice, T is usually taken to be 293 Kelvin (20°C), and B lies between 1000 and 5000.

The constant B of the device used in this test was 2000, and the resistance at 20°C was 25 ohms: The broken line in Fig.4 was calculated and drawn from equation 1.

To confirm this characteristic, a practical test was carried out by immersing the thermistor in a pan of vegetable oil and gradually raising the temperature. The resistance of the device was measured at appropriate temperature intervals and plotted as the solid line in Fig.4. This is the curve we shall work with.

As the author had a future application in mind which required a steady temperature of about 50°C it was decided to aim at this temperature in the present investigation.

The larger the thermal mass of the heated body, the easier it is to obtain a steady temperature, at least in the short term. Therefore, the small quantity of oil used in the following tests amounted to an almost "worse case" configuration.

CONTROL CIRCUITRY

When the sensor and element are separate devices, the simple circuit of Fig.1 can be employed. Class A operation is wasteful of power, but the circuit will work.

No such luck for the corresponding circuit in Fig.2, which now employs a self-heating sensor. Assuming the tempeature of the element-sensor to rise above the correct value, R_{TH} will fall, causing V_c to rise. If G has a 180° phase shift, V_O will fall, thereby reducing I_c. Hence V_c will immediately rise still further because the comparatively long thermal time constant of the thermal system will not allow the thermistor to change its resistance value instantly. This will result in instability.

Reducing the frequency response considerably so as to be compatible with the cooling curve of the thermal system may be successful, but this would need to be changed according to the thermal load, and the author has not tried this. Furthermore, making G positive (in phase) will not improve matters. Again, let the temperature rise, so that V_c will rise. V_o will also become more positive, thus driving the transistor into heavier collector current. This may have the desired effect of reducing V_c, but the heavier collector current will heat the element-sensor even more than initially, which is not what we want.

METHOD ADOPTED

Figure 3 is the block diagram which shows the principle of operation of the method. The switches are symbolic and in the actual circuit diode gates were used. The switches are ganged and operated under clock control at about one cycle per second. In the MARK phase, power is supplied to R_{TH}, heating this up. During the very short SPACE phase, the power is removed and a constant current I_{cs} is passed through R_{TH}, due to the normal action of the transistor and its fixed base current I_{BS} which is preset by R_1. Thus, during the SPACE phase the input V_i to the comparator is equal to $(V_{cc}-I_{cs}R_{TH})$. V_i therefore, is a function of R_{TH} and hence the operating temperature.

When operating at the correct temperature, V_i will be equal to the reference voltage V_{REF}, and the comparator output V_o will be zero.

If the operating temperature now falls below the threshold (set by V_{REF}), R_{TH} will have a higher than normal resistance, and V_i will be lower than the reference V_{REF}. This will result in an output V_o from the comparator which turns the transistor on, thereby heating the thermistor during the mark phase until this reaches the threshold temperature, at which V_i will equal V_{REF}, and V_o will hence fall to zero, preventing any further transistor current.

The signal-storage circuit plays a vital part in this. Because the system only looks at R_{TH} for a brief instant during a space, what it sees then must be remembered for the whole of the following mark interval. It is during this interval that the transistor must obey the instruction to turn on or off, as commanded by the voltage comparator during the preceding space phase.

HEATER POWER REQUIRED

Adequate power must be supplied to the heater during the on-period so that a low temperature may be reinstated to nominal as quickly as possible. Too much power will cause excessive overshoot and hunting.

In the trial test, the element was given the task of maintaining the temperature of 100 grams of oil at 50°C. The oil had a specific heat of 0.5 calories per gram and was contained in a glass beaker having no additional thermal insulation. The thermistor was immersed in this.

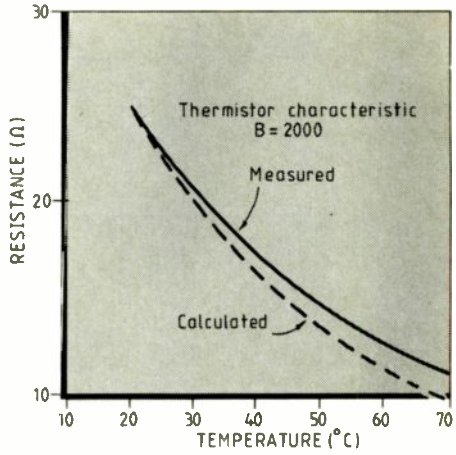

Fig.4. Resistance temperature characteristic of the thermistor employed.

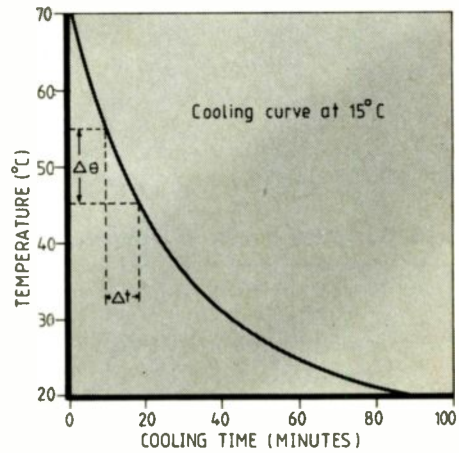

Fig.5. Cooling curve of thermistor and oil bath allows calculation of power.

The beaker and contents were raised to a temperature of 70°C and allowed to cool, the cooling curve being plotted as shown in Fig.5. From this curve, the approximate rate of cooling at 50°C is

$$\frac{\Delta\theta}{\Delta t} = \frac{55-45}{19-10} = 1.11\text{°C/min}$$

Therefore, if the temperature rose 1°C above the threshold, the system would by then have switched off and it would take just over one minute to fall again to 50°C.

Referring again to the rate of fall, it is possible to calculate the minimum power requirements from this. A rate of fall of 1.11°C/minute is equal to 0.019°C/second.

Rate of cooling at 50°C is

$$\frac{\Delta W}{\Delta t} = \text{mass} \times \text{specific heat} \times \frac{\Delta\theta}{\Delta t}$$
$$= 100 \times 0.5 \times 0.019$$
$$= 0.95 \text{ calories per second}$$

or approximately 4 watts This amount of power must be continuously supplied to replace the heat loss at 50°C.

If now the temperature fell by 1°C, say, from 50 to 49°C, an extra amount of heat must be generated by the element in order to restore the temperature to 50°C. The extra amount required is

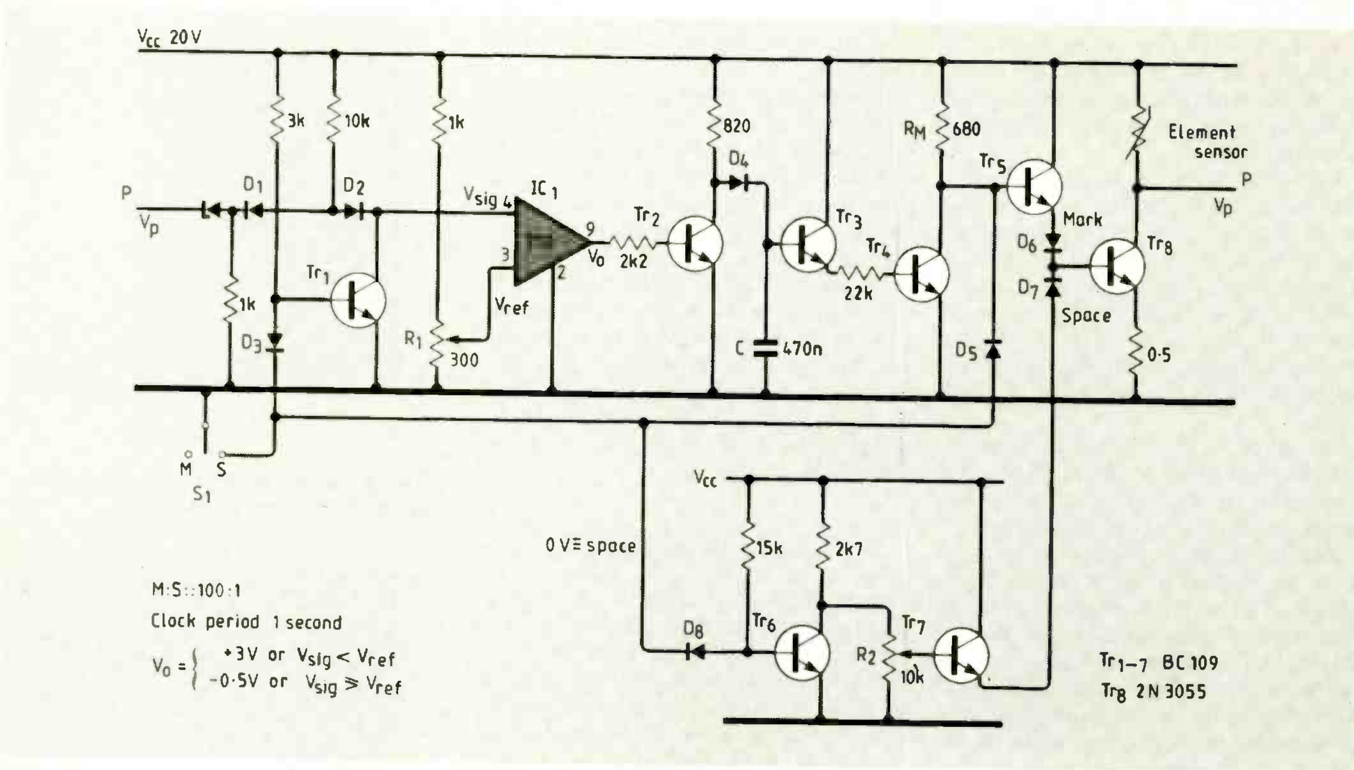

Fig.6. Complete circuit of experimental self-sensing temperature control system.

$$H = \text{Mass} \times \text{sp. ht} \times \triangle\theta$$
$$= 100 \times 0.5 \times 1$$
$$= 50 \text{ calories or } 210 \text{ joules.}$$

If the temperature is to be restored in, say, 10 seconds (10 interrogation periods, in the case of this test), this represents a power of 210/10=21 watts. The total power required, therefore, to guarantee restoring a temperature deficiency of 1°C within 10 seconds is 21+4 = 25 watts.

The resistance of the element-sensor at 50°C can be seen from Fig.4 to be approximately 14.3 ohms. Hence the drive current required to produce a power of 25 watts is

$$I = \sqrt{25/14.3}$$
$$= 1.3 \text{ amperes}$$

During each space interval in Fig.3, the current through R_{TH} was adjusted via R_1 to be 0.5A. This was the reference current used to measure the hot value of R_{TH}. During the mark period, the current through R_{TH} was either zero or 1.3 amperes.

CIRCUIT EMPLOYED

Fig.6 shows the breadboard circuit constructed entirely to satisfy the author as to the validity of using a single thermistor as a combined element-sensor. For more serious precision applications, multi-level control using pulse-width modulation, or proportional control would probably be used, possibly under microprocessor supervision.

Briefly, Tr_8 is the power transistor (2N3055), the collector current of which heats the thermistor R_{TH}. During the space interval, relay contacts Sw_1 close, thus cutting off Tr_6, and turning on emitter follower Tr_7, which drives Tr_8. The collector current I_{cs} of Tr_8 during this time is adjusted by setting R_2.

The constant current I_{cs} passing through R_{TH} during the space interval in a voltage V_P at point P of $(V_{cc} - I_{cs}R_{TH})$ which is coupled to the signal input of IC_1 (voltage comparator 710) via a diode-transistor gate. Transistor Tr_1 shorts out V_{sig} during mark, but during space allows V_{sig} to be compared with V_{ref} at the two inputs of the comparator.

If V_{sig} slightly exceeds V_{ref} (positively), then V_o falls from about +3 volts to −0.5 volts, thus cutting off Tr_2 and allowing capacitor C to charge almost to V_{cc}. The capacitor holds this charge for the duration of the following mark interval, leaking away through the high input resistance of Tr_3, Tr_4.

Had V_{sig} failed to attain the threshold V_{ref}, then V_o would have remained at +3 volts, turning on Tr_2, so that at the end of the space interval the capacitor would have received zero charge.

One final space activity: Tr_5 is switched off, thus preventing any drive current from reaching the base of Tr_8 other than the constant drive from Tr_7. In other words, the diodes D_6 and D_7 act as the changeover switch S_1 in Fig.3.

During the mark interval, Tr_1 switches on, thereby effectively inhibiting IC_1 and turning on Tr_2. If C had been previously charged to V_{cc}, the D_4 isolates C from the collector of Tr_2. If not, it doesn't matter. However, assuming the capacitor had been charged, this would be the result of too high a temperature. Transistors Tr_3 and Tr_4 will be turned on for the whole of the mark interval, and Tr_5 will be turned off, thus removing all base drive from Tr_8, and the thermistor commences to cool.

When sufficiently cool, a sample of V_P during space results in V_o driving Tr_2, and C will not be charged. Hence, during the following mark, Tr_2 and Tr_4 will be off, allowing Tr_5 to fully drive Tr_8 which, in turn, sends the full heating current through R_{TH}. The minimum value of this current has been seen to be 1.3 amperes, and can be adjusted by selecting a suitable value of R_M.

RESULTS

In the experimental circuit the drive current was rounded off to 1.5 amperes. After a settling down period, during which the oil was constantly agitated, the operating temperature was adjusted to exactly 50°C by means of R_1, the threshold control. The temperature of the oil did not vary by more than ±0.5°C during a twelve-hour test run. This was an assessed accuracy, the temperature being measured on a standard mercury-in-glass thermometer having calibration points at one degree intervals.

Further tests involved switching off for long periods, and after switching on the temperature each time returned within the limits 49-51°C. Blowing hot or cold draughts of air on the heated system resulted in recovery to within ±1°C within a few minutes.

Conclusion. The author is not aware of this principle having been applied elsewhere. The tests carried out have been heuristic rather than rigorous, but the results have been encouraging and suggest that further work in this direction could produce a self-sensing heater element system as an alternative to the existing methods. If a demand was shown to exist, then perhaps manufactures would produce a range of special-purpose thermistors, especially larger power devices.

Further reading

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Langton, C.H., "Time shared multipoint temperature controllers", (thesis), Univ. of Bradford, 1974

Thermistors, *Wireless World*, Oct. 1949, p.405

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FEEDBACK

Radioquakes

Regarding Dr Aspden's contribution 'Earthquake' in your February issue, p.230 you might be interested to know of 'The Radioquake Mystery', published by the Home Office in its journal 'Intercom' in 1978, for it outlines how I became troubled by unusual 'static' whilst building a radio station in South America in 1961 and how this led me to the conclusion that radio signals might be employed to provide advance warning of the onset of an earthquake.

The publication of this item brought me no friends in the field of seismology, whilst my peers ostracised be by insisting that it was impossible for such signals to exist, but I'm grateful to Dr Aspden, whose work in the unpopular field of the Ether has for sometime not only offered an explanation of how electromagnetic disturbance deep within the Earth's crust can reach the surface, but has also shown how such signals could have affected the f.m. equipment being used by Markert in Switzerland in 1976. I found it impossible to obtain support for my ideas at government level even though a tiny sum of money withdrawn from our so-often-misappropriated National Overseas Aid Fund to cover research at one of our universities, might well have brought jobs to our factories.

Still friendless, I was fortunate enough whilst spending some months last year in New Zealand to be introduced to Dr Warwick D. Smith of the DSIR's Geophysics division who, having patiently listened to what I had to say, then put his people to work on the literature. Within a week, they had located an article in the September 1982 issue of the *Journal of Geophysical Research* wherein it was reported that a Russian-Japanese research team had located pre-earthquake radio signals. They had also published graphical information relating to three earthquakes which showed how transmissions at 81kHz had been used to produce an 'earthquake imminent' alert up to one hour in advance of the onset of tremors.

As Dr Smith has pointed out, far more study is required to ascertain whether such signals could be used to warn a civilian population, but to this end, he was willing to provide a corner in his laboratory for British research equipment which we could design and construct in this country, but not test. New Zealand is of course located in an active earthquake zone.

Upon hearing this story, my local MP took the matter up some months ago with his ministerial colleagues on behalf of those who suffer throughout the world, but to date, in spite of reminders, the only response has been a stony silence. It would be foolish to expect the automatic acceptance of new ideas, for the chaff has to be separated from the wheat, but more open-mindedness towards them and the work of 'nonconformist' physicists such as Dr Aspden would do our country no harm and possibly a power of good.

Richard E. Hill
Tunbridge Wells

Dr Aspden's claim that a demonstrated correlation between anomalies in radio reception and earthquakes would prove the existence of an ether is a non sequitur. Before Dr Aspden's claim is worth considering – much less publishing – he must at least establish that no other theory of radio wave propagation can explain such a correlation. I think he would find this rather difficult.

Prof. R. A. Waldron
University of Ulster

Don't knock G64

I refer to the article in November's edition of *E&WW*, p.71, entitled "STE standard Eurocard bus", where I feel that the author, Anthony Winter, has sadly been either badly informed or lacking in his research on the subject. His reference to the G-64 bus as being an 8 bit data bus and 64Kbyte addressing is totally wrong.

The G-64 bus was defined and introduced in 1979 by three ex-Motorola employees who created the company Gespac in Geneva. It was even then already ahead of its time as it used the single Euroboard format and the DIN connector giving the reliability and ruggedness required for the harsh industrial environment. More than this it was specified then, and always has been a *16 bit* data bus (please see page 5 of our catalogue enclosed), whereas STD and STE are limited to an 8 bit data bus. Furthermore, from the bus specification, which is in the public domain having been officially published in 1985, it can clearly be seen that the addressing capability is 512Kbytes and not 64Kbytes (32Mbyte on G-96).

Since that time, this bus has become an industrial *de facto* standard along with its compatible extension the G-96 bus, introduced in 1984. Today, Gespac produces more than 4,000 boards per month and has a product range of around 120 different modules dedicated to the industrial world. There are also more than 25 manufacturers throughout Europe and North America dedicated to this bus. Independent figures place Gespac and the G-64 bus as holding 5% of the total European board market in 1985 and from current figures 8% for 1986. Therefore, I hardly think we can be considered as an "also ran" as implied in Winter's article.

Gespac, as an independent manufacturer of board products not aligned to any processor manufacturers, is able to offer a wide range of processor boards on the G-64 and G-96 buses as can be seen from our catalogue with Motorola's 6809, 68000, 68010 and 68020 covered, Intel processors including 8085, 8088, 80286 along with the DEC J11, National Semiconductor's 32 bit 32016 and the Z80.

We are also very competitive in our pricing. For example, our latest board the GESMPU-20 with Motorola's 32 bit processor, 512K eprom, 512K ram, 12/16MHz operation and optional 68881 f.p.u. all on the single Euroboard has a starting price of £800 for one-offs of the 12MHz version, with 256K ram and eprom and without f.p.u.

I do feel, and I think that you would agree, that the least we could expect is a written apology in the next edition of your magazine, or perhaps your staff may wish to write a realistic article on the G-64 and G-96 buses without bias toward other buses which in themselves have very severe limitations, and are already outdated in this world of 16 and 32 bit processors.

R.F. White
Gespac s.a., Geneva

The author replies:

Mr White's letter produced an initial feeling of alarm that I had missed something about G-64; having looked into the *practice* of G-64, as opposed to the *theory*, I feel that my points are justified. My understanding of a bus specification is that manufacturers adhere to it so that their products are compatible; I shall examine Mr White's letter in this light.

He states that "it has always been a 16-bit data bus". It is certainly true that 16 data lines are mentioned on the connector pin-out. Gespac's own literature states, however, that "it is mostly used for the implementation of 8-bit microprocessors". Does this mean, then, that 8-bit microprocessors are required to produce 16 data bits on the bus? Apparently not, because I have a Thomson-EFCIS memory board data sheet which says that the upper eight data lines are not used. Looking more closely, a 16-bit c.p.u. board cannot use this memory board; to quote Gespac again "an 8-bit microprocessor requires that an 8-bit memory is used". When I discussed this point with G-64 users they expressed surprise at the existence of any 16-bit boards on the G-64 (as opposed to G-96) bus. Perhaps we need some user feedback here?

The second point is even more confusing. The specification mentioned by Mr White says there are 16 address lines, one 'memory page' line and 256 Kbytes addressing capability, not the 512K stated by Mr White. Closer examination reveals more puzzles. Firstly, the 256 Kbytes assumes 16-bit data transfers. See my previous comment for a discussion of the likelihood of that. Secondly the memory page line is not used on the c.p.u. or memory boards I have looked at. This brings me back to the 64K.

I'm afraid that my original opinion is reinforced: buses created to use the signals from one processor (the 6809 in the case of G-64) and defined by one manufacturer are always going to look like they've had bits bolted on the side after a few years. Gespac's attempts to upgrade G-64 to G-96 suggest that 16-bit usage with large memory spaces is unlikely to be significant on G-64. In that case it remains what it started out as – a bus for 8-bit c.p.us.

FEEDBACK

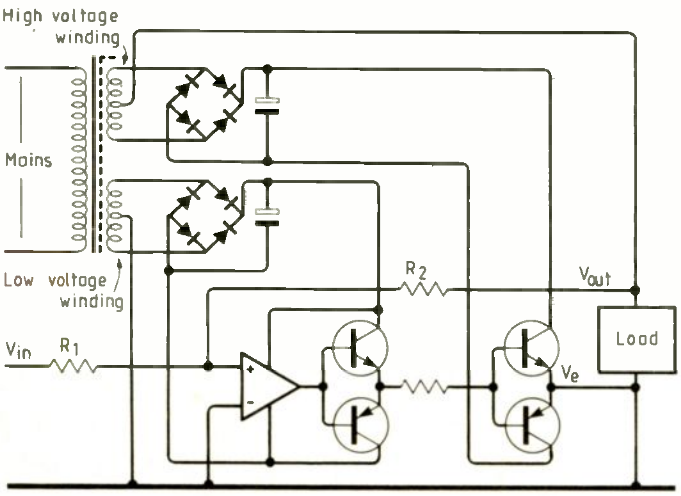
Versatile op-amp

I was interested in the article "Versatile operational amplifier" in the January issue and offer this circuit configuration for interest. The principle of operation relies on the fact that both of the secondaries of the mains transformer are isolated from each other and from ground, although inter-winding capacitance may affect the slew-rate and this may need considering when specifying the transformer.

If the output stage and high voltage winding are considered separately, then the voltage, V_E at the emitters of the complementary pair will vary, with respect to the centre tap of the high-voltage winding, as drive is applied to the bases. However, the high-voltage winding is floating, so the circuit will still work if this common point is connected to 0V. The result of this is that the potential of the whole of the high-voltage winding will move in the opposite direction (i.e. if V_E changes by +100V with respect to the centre-tap changes by −100V with respect to V_E) and hence produce a 180° phase change.

If the centre-tap of the high voltage winding is now treated as V_{out}, then feedback can be taken from there back to the input. Because of inputs of the op-amp are reversed, still giving $V_{out}/V_{in} = -R_2/R_1$ in the traditional way.

If the base drive of the output transistors is too much for the op-amp, then cheap low-voltage complementary transistors running off the low voltage winding can be used as buffers.



This configuration is not practicable with very high voltages due to the restricted choice of high voltage p-n-p transistors but the convenience of using op-amps in an arrangement such as this avoids the need to match components.

John Bonell
Leicester Forest East

Quality Assurance

As a professional Quality man, I must really take exception to the poor quality of the 'Workfile' article on quality assurance in the April edition of your magazine. It contains so many errors and inaccuracies that I shall merely list the more obvious ones.

1. BS5750 was published in 1979, not "three years ago".
2. BS5750 does not "introduce the art of statistical process control", it does not even mention it.
3. Statistical process control does not "indentify flaws so that they can be put right". SPC identifies variations in the process so that flaws can be avoided before they occur.
4. The idea behind BS5750 is not "to put pressure on sub contractors". It is a system of *in-house* quality assurance, with sub contractor control only a very minor part.
5. The old MoD standards are not "0251" but the 05- series, of which 05-21 was just one.
6. MoD Inspectors do not visit approved companies "about four times a year to make sure things are up to scratch". A formal assessment is conducted every three years and between times visits are only made when necessary, in connection with specific contract activities – "No contract-no contact".
7. AQAPS do not "take the skill away from people". They require that skill to be continually assessed against set standards, resulting in a continual upgrading of skills.
8. C&G course 743 does not only "teach quality control techniques to mature people who are often trying to be upgraded to inspector level". Part II of 743 goes well beyond inspection requirements and the course is undertaken by all ages, most particularly by technician apprentices.
9. The "average pay package of £12,000 for a QA engineer" must be the usual South-East distortion. I can assure you that, in the Regions, some QA *managers* are being hired at less than £10,000 in the smaller companies.
10. Surely the initials of "Total Quality Management" are TQM, not "TMQ"-(repeated at least three times).

In closing I would say that, although it is heartening to see somebody flying the QA flag, it would be more reassuring if it was the right colours and not hoisted upside down!

Geoffrey Whitehead
Deputy Quality Manager
Hymatic Engineering Co Ltd

Our correspondent replies

Reporting inaccuracies are unforgivable wherever they occur.

1. BS5750 was indeed published in 1979, guides to parts one two and three were then put out in 1981. The article is referring to increased use of BS5750 over the "last three years".

2. Indeed, Statistical Process Control is not specified in the original 1979 BS5750 publication. It is, I believe, to be mentioned in the forthcoming joint BS5750 and ISO9000 publication.

3-4. As far as I understand, large companies are looking for BS5750 from their suppliers. This does cut down on the amount of Quality Control needed for goods inwards at these companies. Quality Control from top down.

5. The MOD standards before AQAPs were 05 series.

6. Once a company has been AQAPs approved I believe informal visits from inspectors do take place. I believe the number is flexible.

7. This was a direct quote. Mr Aubigne then qualified this statement "that's no bad thing as you can't miss anything this way".

8. Clearly C&G 743 has many facets and purposes. One of its main aims, I believe, is to teach those concerned with QA on a day-to-day basis.

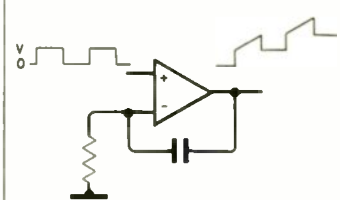
9. £12,000 is a quoted, average figure from a qualified recruitment executive. Obviously managers are hired on £10,000 year and less as the figure I quoted was an average.

10. You're correct Total Quality Management is TQM.

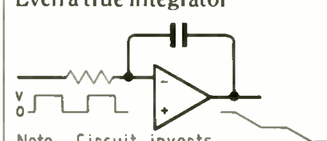
You have pointed to inaccuracies for which I am grateful. The aim of the article was to point to the change in atmosphere in Quality Assurance and the growing importance of the Quality Assurance Engineer with which I hope you would not disagree.

Getting to the root

In "Getting to the root of root-mean-square" Joules Watt does much to clarify and explain the ideas behind r.m.s. measurements, but I am concerned at his choice of integrators in Figs 2 & 3. The circuit that he uses



is not a true integrator but an augmenting integrator and its input signals are superimposed on the result of the integration – which is not what is required in the analogue computations involved in deriving r.m.s. values. Even a true integrator

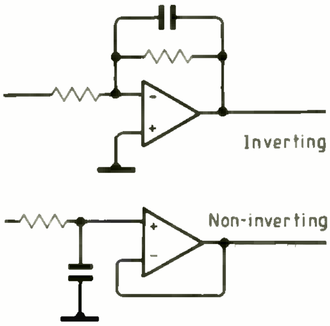


which does not superimpose its input on the integrated output is unsuitable because it integrates its input (including any offset errors) forever. With a unipolar input (which it will receive from

FEEDBACK

a squarer) its output will increase continuously until the amplifier limits.

What is required in the application is a leaky integrator, or averager, with a finite integration time constant of several times the period of the lowest frequency to be handled. I illustrate two suitable circuits:



Joules Watt's text seems to realise this – but the circuit he uses to illustrate the text does not perform the function he describes.

James M. Bryant
European Applications Manager
Analog Devices

Relativity

The explanation M. H. Butterfield ('Feedback', February 1987) asks for concerning flashes of light and the derivation of the Lorentz transformations is given in the reference I quoted in the October 1986 'Feedback'. Surely observations on flashes of light amount to experimental evidence?

Many writers on relativity have claimed that what de Sitter asserted – that the absence of the splitting of spectrum lines of binary stars is in agreement with Einstein's invariance postulate – is the best direct evidence that exists for the postulate. Since such splitting is in fact observed, where does that leave the postulate? Again, if Butterfield wants to understand the point better, let him look up the reference I quoted.

Prof. R. A. Waldron
University of Ulster

I think my old friend Alan Watson must have been teasing when he said that in the timekeeping equation for terrestrial clocks the "acceleration-potential" (GTR) term and the Lorentz-velocity (STR) term are indentical, so that only one of them is required! (*Feedback*, April 1987).

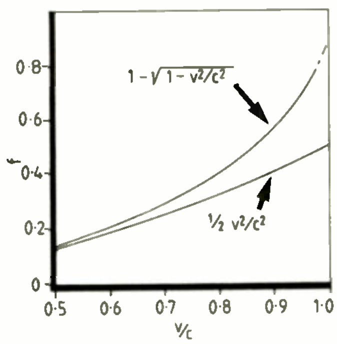
Mr Watson correctly derives the former term in his letter, showing it to provide the proportional slowing

$$(\Delta t/t)_a = \tfrac{1}{2}v^2/c^2 \text{ (exactly)}.$$

where $v = \Omega R$. On the other hand, according to Einstein himself[1] the time-dilation term is

$$(\Delta t/t)_v = 1-\sqrt{1-v^2/c^2},$$

which is not the same thing at all. Their difference becomes pronounced when they are plotted for $v \geq \tfrac{1}{2}c$, as in the diagram.



At low velocities, of course, $\tfrac{1}{2}v^2/c^2$ is a good approximation to $(\Delta t/t)_v$; but the whole point of the relativity theory is that it is said to predict the correct answers even when $v \rightarrow c$. The terms differ by over 50% at $v = 0.95c$, so that it would seem wrong to assert their identity. The same problem arises, and the same mistake is regularly made, when discussing the well-known ultracentrifuge experiment (Mossbauer effect).

In the context of the clocks discussion I might add that experimental evidence seems to exist, to the effect that ideal clocks on the earth's surface do not "keep the same relativistic time independently of latitude differences" (to quote Hafele & Keating). Dr Harold Aspden was king enough to draw my attention to two interesting papers by the Italian time specialists Briatore and Leschiutta, [2], whose results may take quite a lot of explaining away. Watch this space!

In the same (April) *Feedback*, H. Pursey of New Malden takes your correspondent Lee Coe (January 1987) to task, for "not being aware of the relativistic doppler effect, the theory of which may be found in any undergraduate physics textbook". I believe Mr Pursey may have missed the point.

Mr Coe had explained carefully that the radar echo from a moving target (car) travelled at velocity c relative to that car, and also (according to relativity theory) *at the same time* at velocity c relative to the stationary police vehicle. Anti-relativists, he said, would not agree: rightly or wrongly, they would probably suggest its velocity was c + v.

The point would seem to be this. Mr Coe quoted from the *Scientific American* article on the new Stanford accelerator, which said

> "... the accelerating [electromagnetic] field must travel at a velocity close to that of the particles. Some slippage between the two is allowable, so long as the particles stay near the wave-crests."

Here the particles are claimed to be travelling at the velocity 0.9999999997c relative to the accelerator, so the wave velocity must be slowed down slightly to match it. The engineers have built a 'slow-wave' structure to make this happen; it is a standard waveguide technique.

But now: what is the velocity of this wave (a light wave) *relative to the particles?* (It needs to be substantially zero, so that the particles can as it were surfboard along on the waves, continuously gaining energy from them.) But, like the velocity of that radar wave, c relative to both the moving car and the stationary car, should it not be (very nearly) c relative to the particles in this case also? How do the particles differ from moving motor cars, according to relativity theory? And if the wave velocity *is* c relative to the particles, how can "the particles stay near the wave-crests" – and how does this big accelerator work, please?

Mr Coe's point is a little deeper than is normally "found in any undergraduate physics textbook". It is one of those which are not willingly discussed by relativists at any level.

W. A. Scott Murray
Kippford
Galloway

1. Einstein, A. On the Electrodynamics of Moving Bodies; trans. in *The Principle of Relativity*. Methuen, 1923, Dover, 1952, p.49.
2. Briatore, L and Leschiutta, S. Verifying the gravitational shift due to the earth's rotation: *Lettere al Nuovo Cimento*, vol. 15, 1976 pp. 203-207 (In English). Correction: vol. 17, 1976 p.328.

In the Feb. issue Prof Butterfield states "It is not helpful to look for every opportunity to knock the theory that provides an explanation without any vetige of something to replace it".

Having 'knocked' the theory *and* provided an alternative based on the sound rule of *no presupposition*, I invite Prof Butterfield to read the subscribed references and provide a reasoned refutation, again without presupposition. If refutation is not possible then will he admit that Einstein dropped a clanger?

Alex Jones
Alderney

Letters from Alex Jones:
Twins paradox, *Wireless World*, May 1982.
E. M. Doppler, *Wireless World*, November 1983.
Light, distance and time. *Electronic & Wireless World*, September 1985.

Multi element transform

Pull the other one! "Multi to single element transform", my Aunt Gertie, God rest her. What J. C. Belcher's article boils down to might be summarised as:

* Integration of inverse-square vectors over two or three dimensions is difficult
* his transform is easier
* but it is just complex enough that until you read the article you don't see
* that it gives the wrong results (his words are "comes into dispute with contemporary theory").
* so he is going to go on using it anyway.

Nowhere is the faintest effort made to justify use of the so-called "transform". I suppose we should not be surprised: any such attempt would reveal that the article is a candy-floss of nonsense though I failed to find in the name of the author or in the title of the article any anagrams of, for instance, April Fool. Bearing in mind the price of the generally excellent magazine, I would nevertheless appreciate if next year you used less valuable space on jokery.

Alex D. Wilding
Redditch

68020 coprocessors

Using tree-structured memory management tables saves large amounts of memory

DAVID BURNS and DAVID JONES

In paged memory-management systems a description of how a logical address is transferred into a physical address needs to be stored in memory. This description is usually placed in a descriptor table containing information about where the physical address is in memory and other information pertinent to the requirements of a modern virtual-memory operating system.

Linear tables, which contain a single contiguous table with an individual entry for each logical page, are by far the simplest. For logical to physical translations the logical address is simply used to index a large linear table containing the physical address.

With linear tables however, a large portion of the table must reside in memory. Pages as small as 256 bytes are sometimes used; a 68020 system with this type of management and 4 Gbyte addressing would need many megabytes of memory to accommodate several million pages.

An alternative is to translate addresses in a tree structure, Fig.1. With this method only a portion of the logical address space is mapped at each level. At the highest level of the tree, logical address space is subdivided into relatively large blocks; each stage of the tree further subdivides the address space until the page address emerges at the bottom. The M68851 manages memory in this way, accommodating pages as small as 256 bytes.

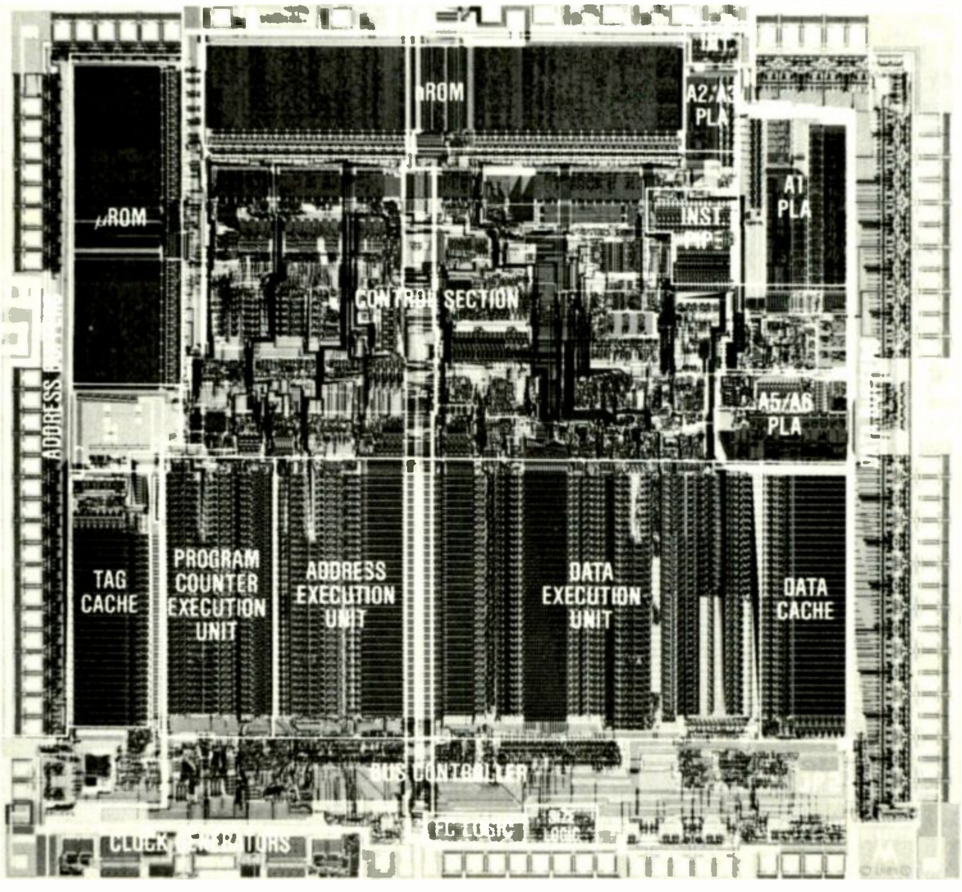
Tree structures allow large portions of logical address space to be allocated to a single entry at a higher level of the tree. In addition, portions of the tree itself may reside on secondary-storage devices, or may not exist at all, until they are required by the processor. As a result, more system memory is available to the user.

Being more complex than linear tables, tree structure translation tables may require several table searches to locate a translation descriptor. In the 68851, a fully-associative address-translation cache with 64 entries and an efficient bus overcome this disadvantage (the translation cache has a hit rate of less than 95%). When a physical map is found, an entry is made in the translation cache. On each subsequent access of this physical page the translation cache responds, making external table searching unnecessary.

TREE STRUCTURE TABLES

Translation tables in the tree structure are indexed from a particular section of the logical address input. How the logical address is divided depends on the contents of the translation-control register.

Within the control register the size and level of the table tree can be defined. This register also defines initial shift, page size, supervisor translations and function-code look-up. Figure 2 shows how these indices are used as index pointers to different levels of table within the structure.



Two types of tables exist within this process – descriptor tables and page tables. Descriptor tables indicate addresses of the next level of tables beneath the present one and page tables point to the base address of the translated page. During normal address translation, the memory-management unit steps down through several levels of descriptor tables before it reaches the page-table reference at the bottom of the tree. At this level the page pointer can also be used as an indirect pointer to the final page address so there is the potential for five levels of table within the translation process.

Table entries can be in either long or short form. Table descriptors contain the base address of the next table (descriptor or page) and status information relating to write protection, user and descriptor type. Long-form descriptors have a limit field to restrict the size of a particular table and additional information to accommodate accéss levels. Page descriptors hold the base address of the physical page in memory, i.e. the translated logical address. In Fig.3, the complete translation process using all four levels of tables is shown.

Table structures of this type increase flexibility. By using different translation paths down through the tree structure it is possible to end up at the same physical address translation. This feature can be used in multi-tasking to give different tasks different access rights to a particular physical page. By mapping different tasks down through different descriptor tables it is possible to assign read/write protection to the lower levels of tables. One task may be allowed to read and write to the page whereas the other task may only be allowed to read from it simply by manipulating the write-protect bit within the relevant table descriptor.

68851 PROGRAMMERS' MODEL

Being designed as a coprocessor for the 68020, the 68851 follows the concepts of the floating-point arithmetic processors described last month. These coprocessors work

Table 1. In 68020 assembly language, memory-management instructions for the 68857 are preceded by P.

Mnemonic	Operation
PMOVE	Move data to or from the 68851 registers using the addressing modes of the processor.
PVALID	Test access level permission of a calling module.
PTEST	Search a table using specified address and function code values. Results of the search are recorded in the PSR. Optionally, the physical address of the last descriptor fetched may be returned.
PLOAD	Performs a search as PTEST but loads an entry into ATC.
PFLUST/PFLUSHS	Invalidate an entry in the ATC; PFLUSHS invalidates only share global entry in ATC.
PFLUSHR	Invalidate an entry in root-pointer table.
PFLUSHA	Invalidates all ATC entries.
PBcc, PDBcc, PSCC, PTRAPcc	These instructions operate in the same manner as the 68020 conditional instructions except they operate on the 68851 status register.
PSAVE	Save entire machine state information on the supervisor stack.
PRESTORE	Restore all machine-state information in the 68851 register.

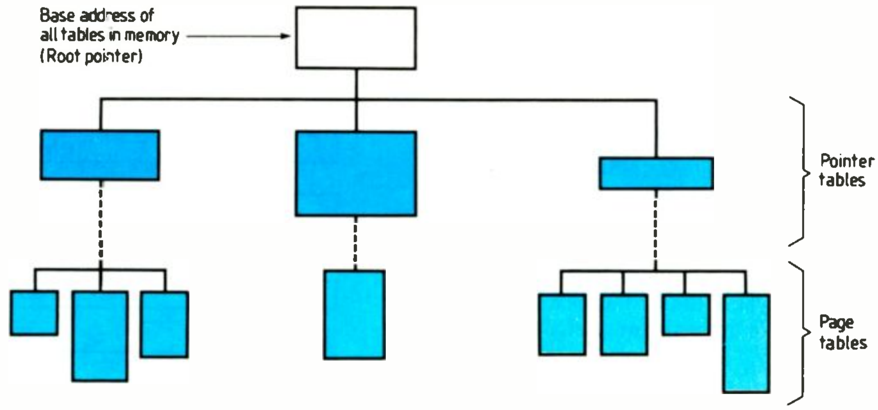


Fig.1. Translation mechanism of the 68851 uses a tree structure to find physical mapping of the logical address. Method allows only a portion of the current tree structure to be resident in memory whereas the linear approach requires the whole contiguous table to be stored in memory.

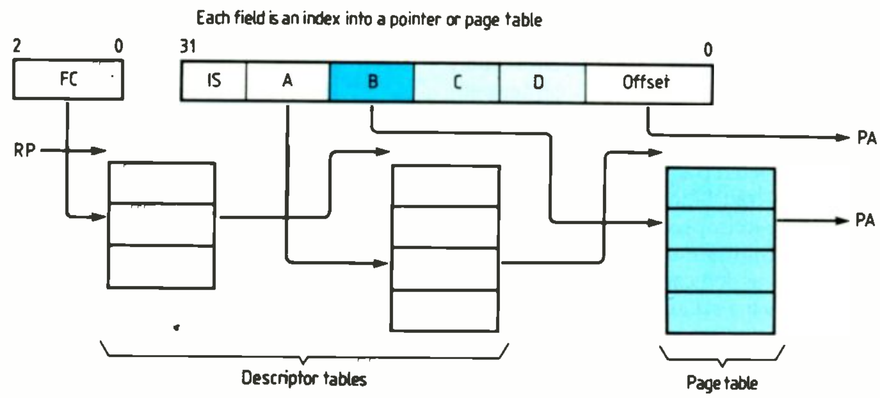


Fig.2. Translation control register, TC, is the main element in the 68851 and controls how all translations in memory are performed, table size and the page size.

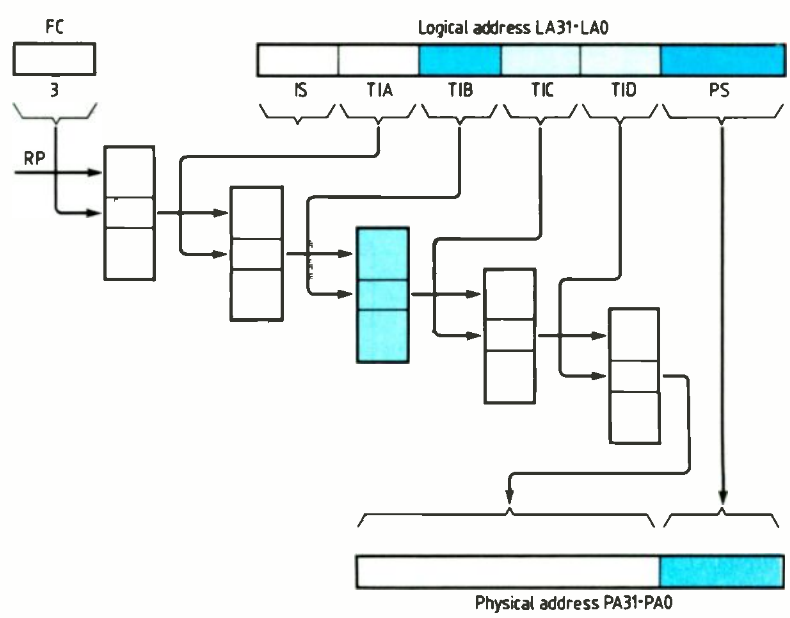


Fig.3. Logical addresses are divided into a number of blocks. At each level there is a table with a reference to another table finally ending in a page descriptor. Page-descriptor information is used by the 68851 to produce the final physical address. This information is loaded into the address translation cache.

so closely with the main processor that the programmer need not be aware that extra hardware has been added; all that the programmer needs to know is that there are extra instructions and registers available. Figure 4 shows the 68851 memory-management unit programmers' model and Table 1 shows the instructions for programming these registers.

Within the 68851 are three root pointers each containing the base address of a set of table and page descriptors for a task, the descriptor type at the next level, a limit field and a bit for implementing shared global memory.

Most translations are performed through the c.p.u. root pointer and each time a new task is executed a new value is written into the root pointer. A record of the eight most recently used root pointers is kept in an on-chip root-pointer table.

The root-pointer table exists so that if a context switch is made, i.e. if the time-slice given to that particular task expires, a new root-pointer value is simply written to the c.p.u. root-pointer register. If this new root pointer also appears in the root pointer table, the task has already run and it is likely that the translation cache will contain entries for it. This being the case the 68851 may not need to perform many, if any, table searches to fetch the pages for this task into the address-translation cache.

If the supervisor root-pointer enable bit is set in the translation control register then all supervisor logical address accesses are translated via a separate root pointer called the supervisor root pointer. This adds flexibility and increases system integrity.

Since the 68851 accommodates both logical and physical bus arbitration the direct memory access root pointer is used to allow translations for other logical bus masters; a disc controller for example can have its own translation mechanism.

How translations occur is controlled by the translation control register. It enables translations to occur once all the table entries have been entered into processor memory or other storage devices. In addition the translation control register can enable a function-code to be taken from the first table pointed to by the root pointer.

Remaining parts of the control register program page size, initial shift and up to four table index fields. How many upper logical-address bits are to be ignored by the 68851 during table search operations is determined by the initial shift field. During a table search operation, the index fields specify the number of bits of the logical address to be used as an index to the translation-table level.

Status information for the translation cache is held in the memory management unit's cache status register, PCSR. This information helps the operating system to maintain the computer system by for example allowing the translation cache to be flushed when the F bit is set. Information in a second status register, PCR, is used by the operating system to determine the cause of faults like bus errors and access-level violation. To simplify fault correction, this status also contains information about the table or

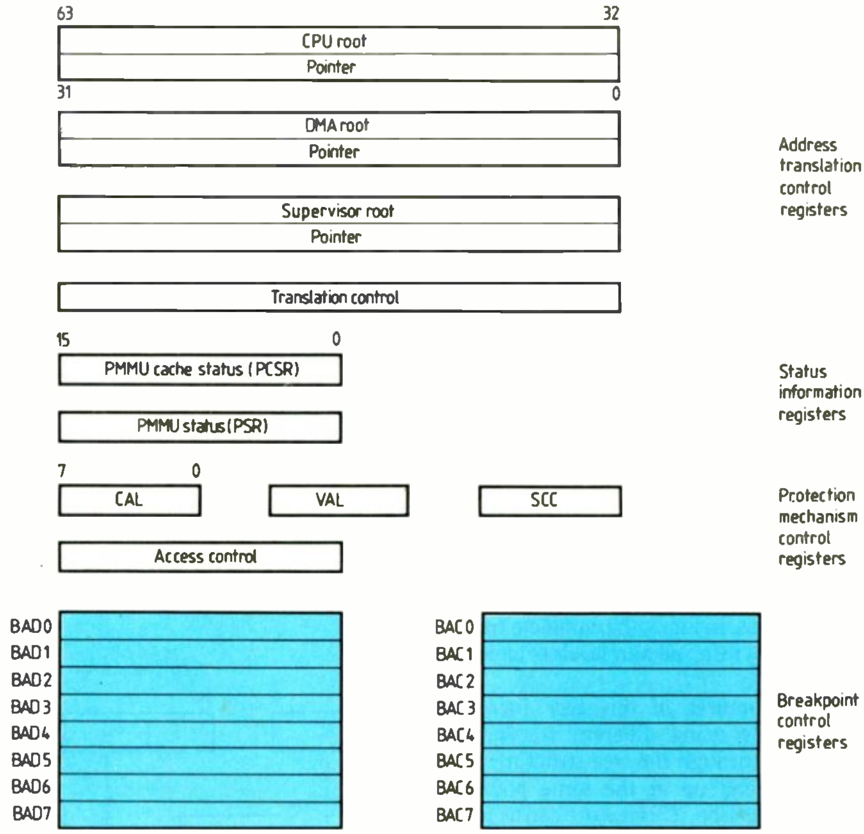


Fig.4. As a 68020 coprocessor, the 68851's internal registers can be considered as extensions to those of the 68020. As far as the user is concerned, executing instructions for the 68851 is no different to executing 68020 instructions.

page descriptor at the time that the fault occurred.

Four protection registers, CAL, VAL, SCC and ACCESS CONTROL are used in conjunction with the 68020 module support facility described in the February issue to implement a hardware and software protection scheme for the memory system.

Registers BAD_{0-7} and BAC_{0-7} are used in conjunction with the 68020 breakpoint instruction BKPT #<data>. Breakpoint-acknowledge data registers BAD_{0-7} hold opcodes displaced by the breakpoint instruction and breakpoint-acknowledge control registers BAC_{0-7} contain enable and count functions for the breakpoint-acknowledge mechanism.

Communication between the 68020 and coprocessor is not apparent to the programmer. All that the programmer needs to know is that there are extra registers and instructions to make the system more flexible. Adding a coprocessor to the 68020 is quite straightforward and once it is in position it can be used as much or as little as is necessary.

David Burns and David Jones are applications engineers at Motorola's East Kilbride plant.

Why have memory management?

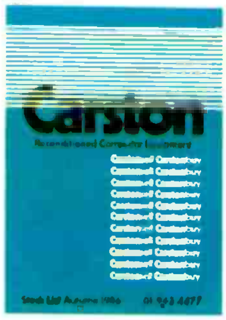
Memory management is needed in most large systems today for several reasons.

- **Multi-tasking operating systems require a degree of inter-task protection. This is to prevent the situation whereby one task may accidentally try and overwrite another task's data area. The provision of a memory management unit will confine a task to permitted areas of memory.**

- **In a virtual memory system of the address space is contained on disc and only the areas that are currently being used are actually resident in main memory. A memory management unit allows the operating system to keep track of memory areas (pages) which are active and those which are on disc.**

• DATABANK •

CARSTON ELECTRONICS



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Minimal eprom programmer

This flexible design is suitable for almost any computer with an RS232 port: it requires no access to the main processor bus.

B. J. SOKOL

Because it gets all its intelligence from the host computer this circuit requires no c.p.u., no firmware and no memory. For some computers, even simpler circuits can program eproms; but such circuits must be plugged into the computer's main processor bus, and that requires opening up the case.

The serial circuit described here gains two great advantages: it does not require any particular type of computer with a specific backplane; and it can stand alone alongside its host with only a cable to plug in. In practical terms the second advantage makes for three great conveniences: whenever it is needed the programmer can be easily connected, used on the tabletop, and put away again with very little effort.

The design requires a separate power supply for the programmer, as sufficient power is not available through an RS232 connection. However neither the power supply nor the hardware need be costly, and indeed the designs offered here use only a few standard components to achieve all required functions.

The reading or writing of one byte of an eprom requires setting up an address for the chip and then reading or writing its data pins with appropriate strobe signals applied to other pins. An RS232 connection can send or receive up to eight bits of data per block, which is sufficient to transmit the data in or out of the eprom, but not sufficient to set addresses or strobes. Multiple byte transmission via RS232, as for example using two bytes of Ascii to represent each hex data byte and using Ascii codes outside the range 0-9 and A-F for control purposes, would obviously allow an RS232 connection to run an eprom programmer. This is what is usually done, but it requires a micro and firmware at the programmer end of the connection to interpret codes, reassemble bytes, construct addresses, etc. But an alternative approach based on a special purpose-designed protocol requires no such hardware complexity.

The protocol requires that the host computer send a byte and then wait for a byte to be sent in return from the programming circuit. Depending on the direction of information transfer, one or the other of these bytes is a dummy used only to signal the receipt of or request for a meaningful byte. In addition, only half the pairs of bytes of this sort convey data information and the other half convey control information.

If the RS232 connection is over a short cable, of say 1.5 metres, there is no problem whatsoever in using 9600 baud signalling. At this rate each byte requires approximately 1 millisecond to be sent, and since four bytes must be exchanged for each eprom byte dealt with, a signalling time of 4ms is required for each byte of eprom. Since programming a single byte takes 50ms, the signalling overhead is relatively small. The overhead is not excessive on read cycles either: the signalling time required to read in the entire contents of a 2764 eprom, for example, is only 32 seconds.

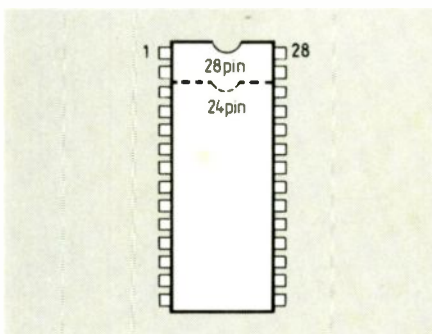
The only complex element in the programming circuit is a uart. This chip signals when a complete byte is received, and then a simple monostable made of a Schmitt gate and a capacitor causes the same chip to send a byte in return. A toggle flip-flop connected to the same circuit causes alternate byte pairs to be treated as data pairs or control pairs. For simplicity the control pairs have essentially only one function, to advance a binary counter string that provides the address information to the eprom. In programming mode one other function is also supplied by this address-advancing signal, and that is to strobe the eprom for programming.

Figure 1 shows how simply this can be realized. Only a few chips generate data, addresses, and strobes, and enable the RS232 handshaking protocol described above. The signals RESET and NOT-READ/READ are generated under user control (rather than processor control), greatly simplifying the demands on the protocol.

Assuming RESET has been strobed briefly, the address presented to the eprom will begin at 0. If READ is then asserted and a dummy byte with no particular meaning is received from the host computer, the uart will set RDA, received data available. After a short delay this will strobe TDS, transmitter data strobe, which will cause the uart to send back to the host computer the byte on the data pins of the eprom. At the same moment RDA will be reset through RDAR. Rising pulses on RDA toggle the 4013 flip-flop. The second RC circuit and the Schmitt input of the 4040 produce a brief delay (this allows the programming pulse to fall before address changes), and the falling edges of the 4013 output advance the 4040 and 4520 counter strings. Thus as even-numbered dummy bytes are received the addresses presented to the eprom will advance through all the possible addresses in turn. On receipt of odd-numbered alternate dummy bytes, data corresponding to the last set address will be sent back to the host. Thus the whole rom can be read.

Table 1. Header connections for the personality modules. Note that 24-pin types must be inserted in the zif socket as illustrated below: pin numbers are therefore correct for the socket and not for the chip.

	Zif socket pins						Resistor
	20	22	23	26	27	1	R_h
2716	PGM1	$\overline{OE}$	V_{pp}	+5V	n.c.	n.c.	none
2764/27128	ground	$\overline{OE}$	A11	A13	PGM2	V_{pp}	12k 1%
27256	PGM3	$\overline{OE}$	A11	A13	A14	V_{pp}	12k (21V types) 1.8k (12.5V types)
27512	PGM3	see Fig.4	A11	A13	A14	A15	1.8k 1%
2732	PGM3	see Fig.4	A11	+5V	n.c.	n.c.	none for 25V type, 12k for 21V (2732A)



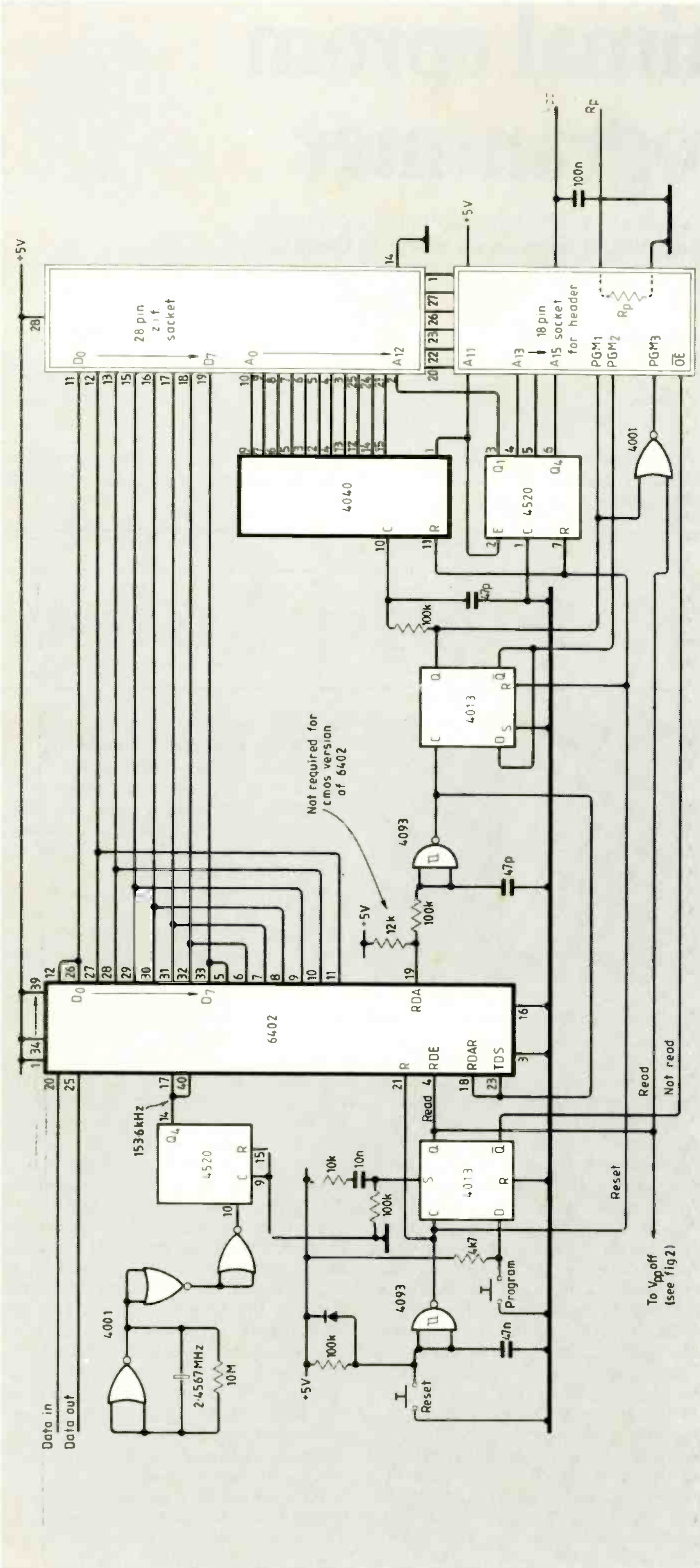


Fig.1. With appropriate links or parts on the 18-pin header, the programmer can handle eproms from 2716 up to 27512. To start the programming sequence, the Reset switch must be closed momentarily whilst Prog is held down.

Writing an eprom is similar except that NOT-READ is asserted rather than READ, which makes the uart output data to the eprom rather than input from it. So the host computer must send the data to be written to the eprom rather than just dummy bytes to advance addresses. On the other hand, during programming the data sent back from the uart to the host has no meaning except as an acknowledgement of receipt of a byte. The 4013 toggle flip-flop not only advances the address counters but also controls the program-enable pin of the eprom. This pin must be active for 50ms per byte programmed, and this timing is part of the business of the host computer.

The remaining circuitry consists of a bit-rate generator, an interlocking electronic read/program switch, a logic controlled power supply, a line interface, and personality headers to allow many different types of eprom to be programmed. Circuitry is also required to generate three different types of programming pulse to accord with the requirements of various types of eprom. The 2732 and 27512 types use the same pin for programming voltages and enable inputs, and that is achieved by active components on the personality headers, which need not be included if not needed.

The interlocking programming switch uses a spare section of the 4093 and the spare half of the 4013. This system is not absolutely necessary, for just a toggle switch and a push button switch would do the job. The interlock is intended to prevent accidents in three ways. The 4093 and the RC circuit on the set pin of the 4013 assert a power-on reset so that the circuit always powers up ready to read, and not program. Thus eproms will not be damaged if they are plugged in at turn-on time. Secondly, to change over to the program mode a two finger operation is necessary. This requires some thought, and should diminish the chance of accidental damage. Thirdly, momentary push-to-make switches are cheap and simple, and since the power supply provides a warning light, malfunction is unlikely and cannot be disguised as it might be with a toggle switch.

The power supply shown in Fig. 2 is somewhat unusual. It uses a single transformer winding to provide a variable programmable supply adjustable between 5 and 25V, and a fixed supply providing 5V. This simplifies the choice of transformer and allows it to be kept remote and safely insulated (mine is inside a plastic mains plug body). The two wires from the transformer supply 12V a.c. and so a common 6-0-6 unit is suitable.

The circuit around the 317L needs some explanation. The 3360Ω resistor, which can be made up of two units in series, allows standard resistor values for R_p (in the personality header) to set the usual programming voltages, 25, 21 and 12.5V. Re-

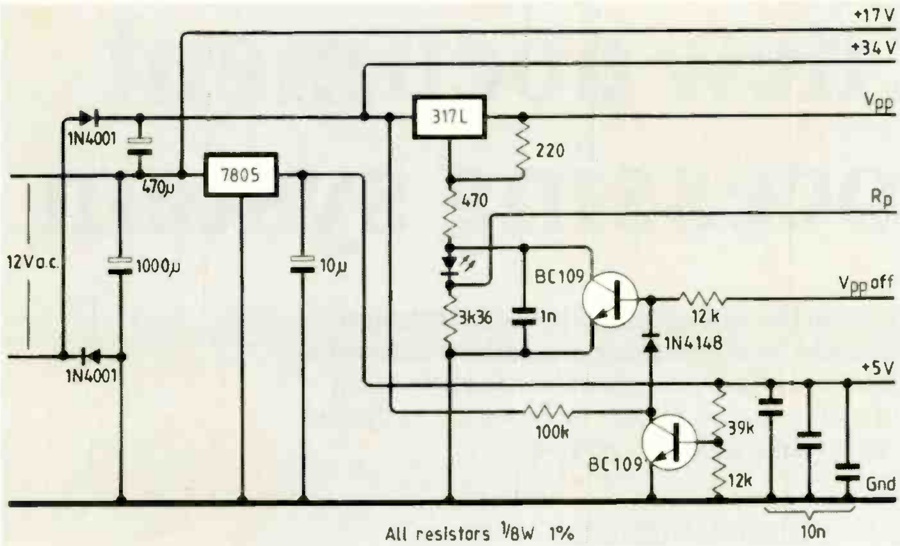


Fig.2. Power supply for the programmer. An unusual feature is that the 317L regulator helps identify faulty eproms: if excessive programming current is drawn, it overheats cyclically and flashes the led.

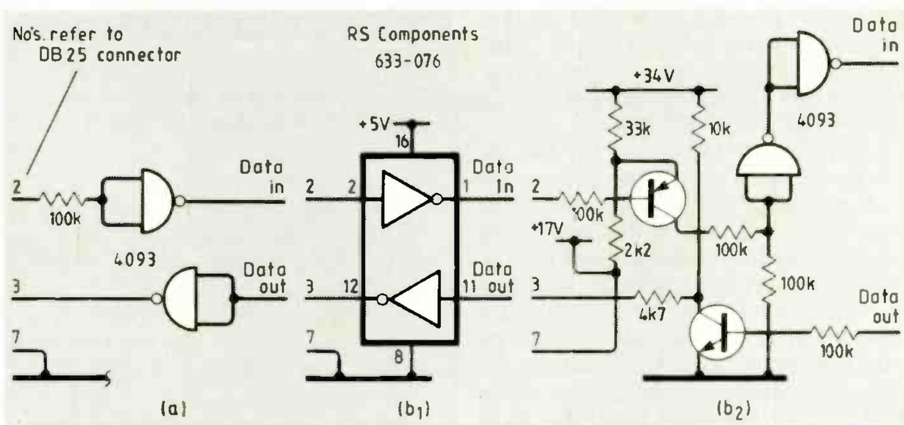


Fig.3. Line interfaces for the serial connection. The simplest version (a) provides only a 0-5V swing; if the host computer requires a negative swing at its RS232 input, versions (b_1) or (b_2) should be substituted. Version (b_2) is the cheaper.

gardless of the R_p value the led carries a constant current given by 1.2V ÷ 220Ω, or 5.45mA, whenever $V_{pp\ off}$ is low. Thus its brightness does not depend on the type of eprom being programmed. The transistor controlled by $V_{pp\ off}$ switches off the led and reduces V_{pp} to the t.t.l. high level set by the 470Ω resistor, as required by most eproms when they are read. The purpose of the additional transistor controlled by the 5V supply is to ensure that V_{pp} is at the lower level whenever the 5V supply goes off: this protects eproms from potential destruction.

There is in addition one serendipitous feature of the V_{pp} supply: the 317L chip will cyclically overheat if a programming current of more than 30-35mA is drawn, and that flashes the led so that faulty eproms are detected as they are programmed.

The line interface indicated in Fig. 3 is simple but non-standard. It provides only a 0 to 5V swing on the serial output, which will not work with some rare RS232 interfaces that require the full legal swing down to –3V or less. Figure 3b shows a solution for this problem if it arises. In either case the experienced will note with gratitude that only two active lines are used in the RS232 connection, data in and data out, which are always on pins 2 and 3 of a 25-way D connector. They might be either way around (IBM PCs use 2 for data in), but that's the worst it can get. Pin 7 is *always* data ground.

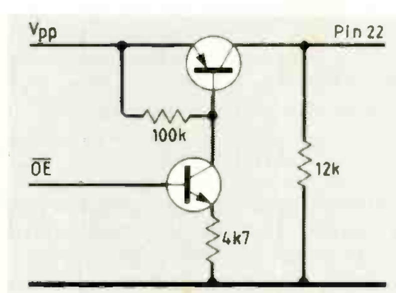


Fig.4. Special parts for personality modules for programming 2732 and 27512 devices.

Personality header connections for a range of eproms are indicated in Table 1. Figure 4 shows the special personality header required for 27512, 2732 or 2732A type eproms.

To be continued.

BOOKS

World Radio TV Handbook, edited by Jens M. Frost. Billboard Publications, 575 pages, soft covers (available in the UK from Pitman Publishing at £17.95). The 1987 edition of this all-embracing directory of the world's broadcasting follows the same format as before, though with minor additions such as a list of European satellite tv stations. In the features section are articles on the BBC Monitoring Service and clandestine radio stations, plus a useful review of portable h.f. receivers for the traveller.

Oliver Heaviside, the man by G.F.C. Searle, CAM Publishing, hard cover, 80 pages, £12. At the time when the somewhat eccentric Heaviside made his outlandish statements about e-m theory, the tightly-knit scientific establishment was rigid in its views. As a result, his work was dismissed and all but forgotten.

But recent advances, particularly in digital electronics, have indicated that there might be holes in traditional e-m theory; and interest in Heaviside and his work is being revived.

Luckily, the opinion that Heaviside was an eccentric is no longer so important. In fact, by today's standards he would probably not even be considered eccentric. This book, written by Heaviside's close friend Dr G.F.C. Searle and said to be the only published biography, will allow you to judge for yourself.

Reading about Heaviside's private life will neither confirm nor abrogate what he said publicly, but it might inspire you to take a close look at his ideas and to give you an insight into the scientific establishment of Heaviside's time. M.E.E.

A selection of technical books on broadcasting is among a wide variety of more general publications on radio and television available to callers at the BBC World Shop in London. Subjects include engineering practice in radio, tv and film work. Special emphasis is placed on h.f. radio. The shop, now refitted after an unexpected dousing during January's cold snap, is at the BBC External Services' headquarters at Bush House in the Strand.

A 32-page catalogue from the Institution of Electrical Engineers describes the IEE's extensive range of books, bibliographies, conference proceedings, colloquium digests and journals, including many new titles to be released during the year. Main subject headings include telecommunications, electromagnetic waves, computing, materials and devices, energy, power, management, history of technology. The 1987 Publications Catalogue is available from the Books Administrator, IEE, P.O. Box 8, Southgate House, Stevenage, Hertfordshire SG1 1HC, tel. 0438-313311.

Reos – a new document image processing system

New technology and the emergence of powerful standard operating systems and local area communications networks makes it feasible to produce document image processing systems that will have as much impact on business as did the mainframe on office systems.

RICHARD KREUZER

Despite decades of computerization, low-cost word processors and office micros, the vision of the paperless office still does not equate with the reality of today's office. It's not surprising; paper is cheap, portable, user-friendly and readily available. Far from becoming obsolete paper usage is growing, and conventional filing is growing at 20% every year.

The cost to industry in terms of space lost to filing cabinets, lost documents, extensive time to find documents and photocopying charges is enormous. In addition, paper is routed through organisation and is used to sequence people's activities and to record their decisions.

There is thus a pressing need for electronic systems that allow departments to capture all their incoming documents, index them, store them digitally and provide multiple users with fast access to images of those documents via high resolution terminals and print-outs. In addition, such a system must be able to be integrated with existing sources of information, particularly mainframe databases and PC-based databases.

Until recently the technology to provide this range of capabilities was not available, but with the advent of high capacity optical discs, powerful high-resolution workstations, laser printers and image processing chips, it is now possible to meet departmental needs.

BACKGROUND

Optical disc technology was originally developed for document image storage in the Japanese environment where 98% of business documents in Japan are handwritten. The first systems therefore were primarily facsimile-forwarding systems using optical storage media and PC-based filing and retrieval software. There are nearly 3,000 of these type of systems installed in Japan today and they are single-user systems; indeed one might equate them to the private filing cabinet. Networking and operational systems software is either extremely limited or non-existent. To add further users requires purchasing another complete system. These systems are available outside of Japan marketed by Sony, 3M and Hitachi and range in price from $35,000 to $85,000.

Systems integrators in the UK and the USA have taken a wider multi-user view of the use of optical technology for document image processing and in this respect the prime participants are Filenet and Prodigy and in Europe, Philips and Racal. In the case of Filenet and Philips these systems are presented in a closed systems environment using proprietary hardware and software and entry-level systems are available from circa $250,000. On the other hand, the Racal system has been built on open system architecture using standard protocols and interfaces and proven hardware system suppliers, for example Sun and Canon. Racal themselves have developed the operational software, a selection of hardware boards and a fourth generation customization language. The entry-level system price for a fully functional system is circa $130,000.

THE NEED

The primary need for digital image processing systems is in clerical environments which routinely deal with large amounts of paperwork. This paperwork almost always has some handwriting on it and is thus not suitable for existing computer systems. An electronic document image processing system for such clerical use must fulfil three basic needs.

● **Queries** – where the users respond to customer queries, generally over the phone. The principal need here is for fast access to data, for example the ability to retrieve a customer letter from a third of a million similar letters in under 20 seconds. Often complementary information exists on the corporate database and the ability to access this data via a window on the workstation screen is a secondary need.

● **Document processing** – where the user adds to or otherwise uses the information contained in the document, typically adding

OUTLINE OF REOS FACILITIES

Reos is a multitasking, multiuser, image processing system which allows the user to initiate a new task before the system has completed the last.

Image processing

Image capture for originals up to A3. Template/partial scanning 200/400 dots per inch resolution. Automatic sheet feeding.

Image display providing zoom/shrink, pan and scroll. Multiwindowing. Image cut and paste: Image annotation via handwriting and/or typing.

Document image storage within work station to allow rapid page browsing.

Document printing at up to 400 dot/in of the original image plus annotations on paper of up to A3 size, blank or logo paper. Alternatively Reos can print the logos.

Document processing

Document mailing manually or automatically to other Reos users.

Document may be associated with 'bring-up' dates to provide automatic prompting.

Documents automatically dated, time stamped and numbered when captured.

Man-machine interface

The system can be driven via menus, dedicated function keys and/or icons and a mouse/bit-pad. This is a customer option. Screen layout and "macro" functions may also be custom designed.

External communication

Ethernet using Transport Control/Internet protocols

BSC RJE*

SNA*

PC-DOS support

IBM PC programs can be supported via a PC window. The program may execute at the workstation on a dedicated PC/AT emulation card or on a shared PC/AT card in the core

* Abbreviations for IBM's Binary Synchronous Communications – Remote Job Entry, and System Network Architecture.

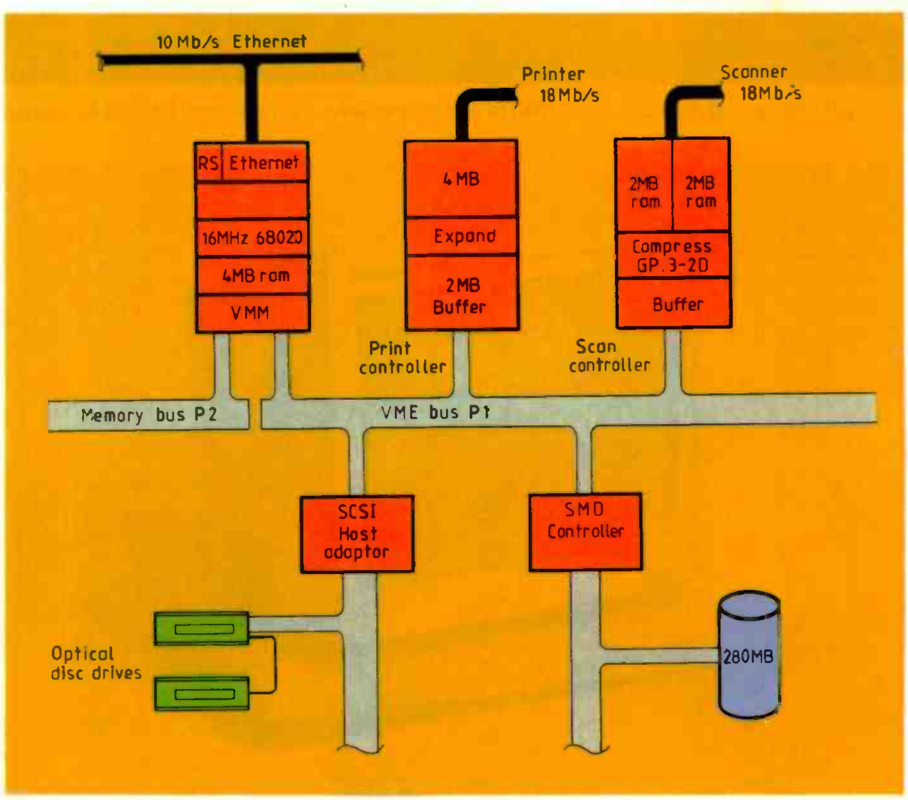
'official' information into the appropriate boxes,signing the document off, and perhaps updating the corporate database. Thus the workstation must also offer a facility to handwrite and type onto the document and maintain an audit trail of these annotations, plus an ability to mail the document to the next processing clerk. Such departments typically store one third of a million active letters.

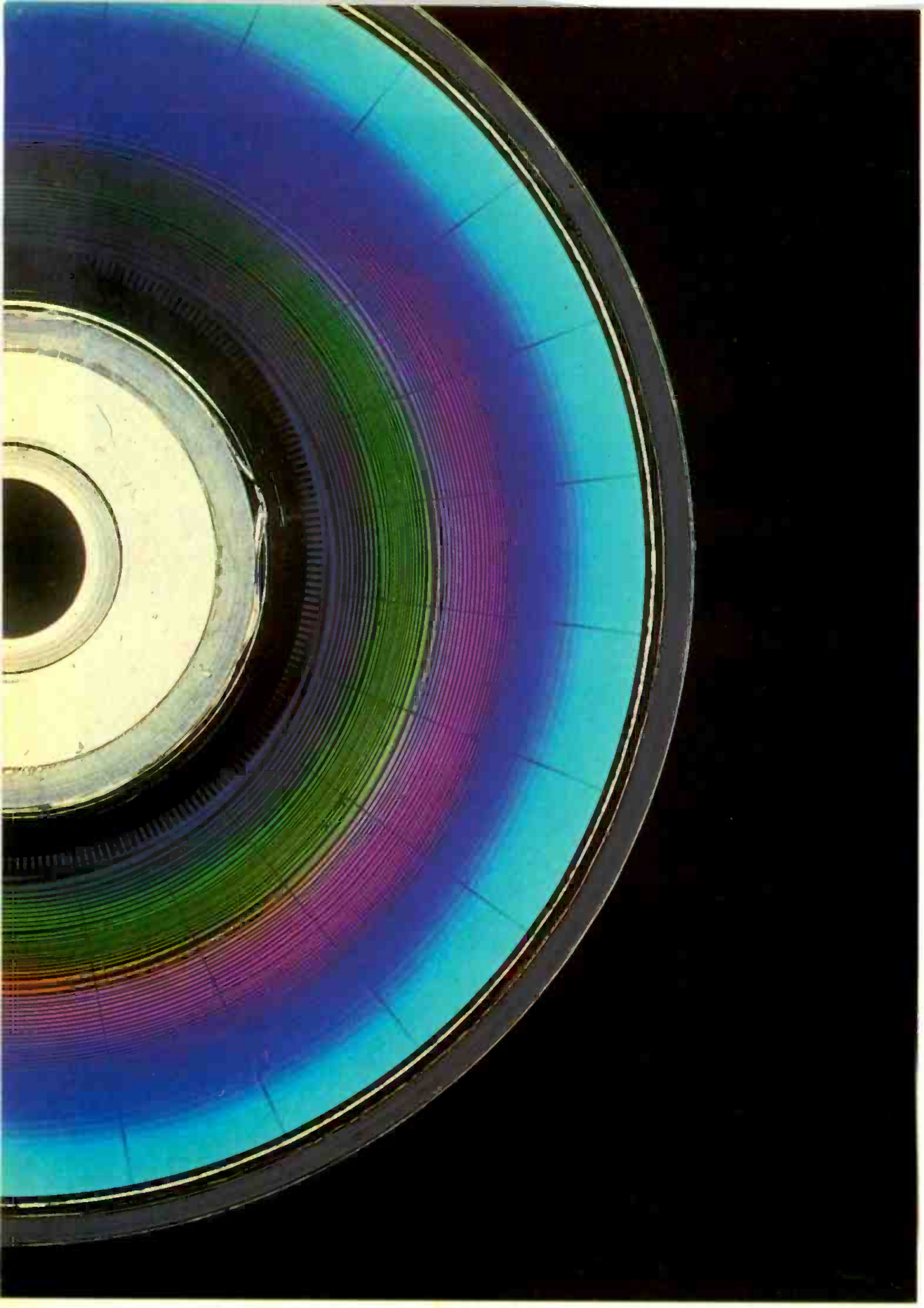
● **Archival storage** – characterised by the need for very large document storage capacities – greater than 1 million A4 pages – with comprehensive cross-reference retrieval capabilities.

In addition, there is also a need to access other information systems such as IBM's SNA and PC-DOS programs.

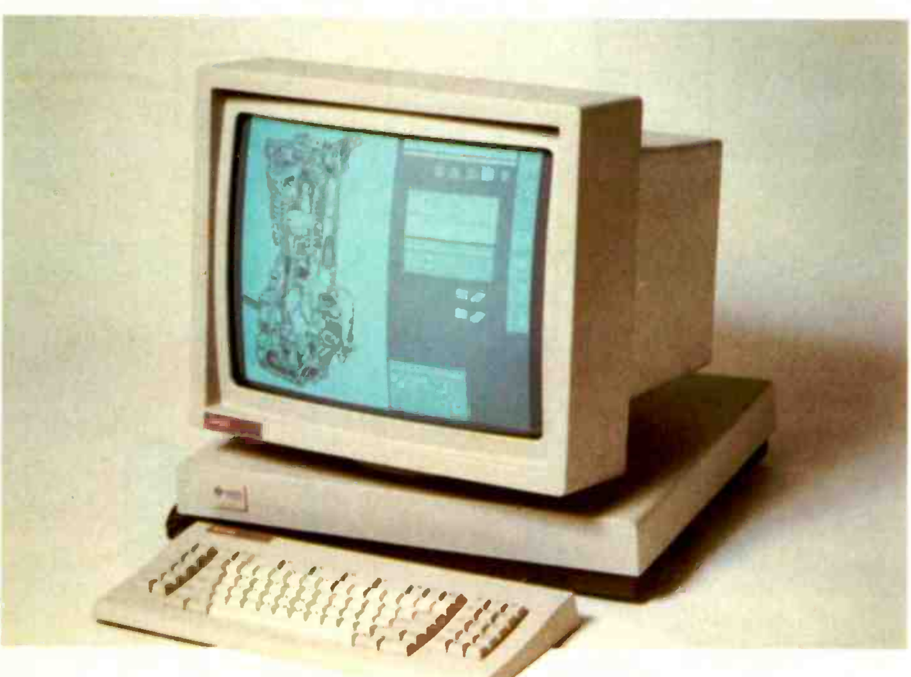
Racal new document imaging system pro-

A typical core configuration consists of a 16MHz 68020 4Mbyte computer running Berkeley Unix; 280Mbytes of Winchester store for the card index relational database and temporary storage of images; two or more optical disc drives; and also the printer and scanner controller/ compressor boards. A further seven slots are available for expansion and options.





One 12 inch optical disc can store 1Gbyte of data per side, equivalent to 30,000 A4 pages.



Images are viewed on Sun Microsystems' 19in high resolution workstations capable of displaying two A4 documents, and providing document handling, editing and local image manipulation.

vides a unique example of the commercial realisation of system that meets these needs.

THE REOS SYSTEM

A Reos* system consists of four principal components: one or more document scanners, one or more laser printers, a document server, and one or more document workstations linked to the server through an ethernet local area network. The server drives up to 16 optical disc drives which use use write-once 12in discs capable of storing 1.2Gbyte of data per side. The server also contains magnetic disc storage with a capacity of up to 1Gbyte.

Figure 1 shows a block diagram of the Racal system. The peripherals and workstations are connected to a central core server which controls access to, and the permanent storage of, the information. Workstations manipulate images and data via windows and editors. These images are temporarily stored within the terminal. Images and data are transmitted to and from workstations and the core via the ethernet link. The scanner and printer connect to the core via proprietary high speed links (18Mbit/s). The optical and winchester drives use industry-standard SÇSI and SMD interfaces.

A Reos core can accommodate expansion options:

up to 4 scanners
up to 16 optical disc drives
up to 1.2Gbytes of hard disc storage
up to 16Mbyte of random access memory
an SNA front-end coprocessor board, and
PC AT coprocessor board.

Although it is generally recommended that a core should serve no more than 16 workstations the actual number used depends on the throughput they impose on the magnetic optical disc drives. If users spend most of the time reading the image documents then the actual system throughput can be low enough to permit many more workstations.

HARDWARE AND SOFTWARE

Based on Sun Microsystem's 3/160 computer system, the core contains a 32-bit VME bus and 16MHz 68020 c.p.u. Memory operating over a 15Mbyte/s bus, can be expanded to 16Mbyte in increments of 4Mbytes. The VME (P1) bus, running at 5Mbyte/s, is used by the input output peripheral controllers. The c.p.u. supports multiple processes by means of a high-speed, 270ns-access memory management unit which allows the operating system virtual memory facilities. The core operating system is the Berkeley '4.2 BSD' version of Unix.

Image compression or decompression is achieved using industry-standard circuits housed in Racal Imaging's image controller subsystems. Each scanner controller, print controller and image converter board incorporates one of these subsystems. In addition the image converter and printer boards contain hardware to perform image resolution conversion. All the boards contain sufficient buffer memory to ensure that conversion, compression and decompression occurs at the fastest possible rate.

Reos is a true multi-tasking real-time system, as shown in the block diagram of the basic system software on page 000. The core modules synchronize their activities by means of messages which they exchange with one another via the executive real-time dialogue handler. Because of this the modules are portable and can be relocated from core to terminal and vice versa to optimize configuration and performance.

The particular facilities that are made available to users and the manner in which these are presented is determined by the 'syntax trees'. These are constructed off-line by Racal Imaging Systems to enable systems to be customized.

Application programs are written in the C programming language.

SYSTEM OPERATION

Reos captures images of documents via the scanner. Paper is fed automatically or manually placed on the scanner platen and pre-scanned to determine the paper size, position and print density. A mirror system and a 4688-element c.c.d. array then scan a default resolution of 200 picture elements per inch, producing about 3.8 million picture elements for an A4 page. For pages with fine print the scanner can be set to scan at a resolution of 400 picture elements per inch. Photographic originals are converted into half tones giving the ability to produce up to 64 graduations of tone. The resulting bit image stream is transmitted from the scanner to the scanner controller board located in the server at about 18b/s, which buffers this data prior to compressing it.

Compression

Standards for the compression of image data agreed by the CCITT define the document representation, coding alternatives, encoding algorithms, and transmission requirements for facsimile operation. The system compresses images in conformance with the group two – dimensional encoding standard which takes advantage of the fact that many images, particularly text and line drawings, exhibit a strong vertical correlation from scan line to scan line. About 50% of all the transitions from black to white or vice versa are directly underneath a transition on the line above it; about 25% differ by only one picture element. This encoding standard provides an as verage compression factor of 15, and the original 3.8Mbits are compressed to 32Kbytes.

The scanner controller board contains two input buffers enabling one page to be compressed whilst the other is being received from the scanner. Documents from the scanner are sent to the recipients 'scanner in-tray', selected by the scanner operator who keys in the necessary identifying name.

* Reos is classical Greek for fast flow.

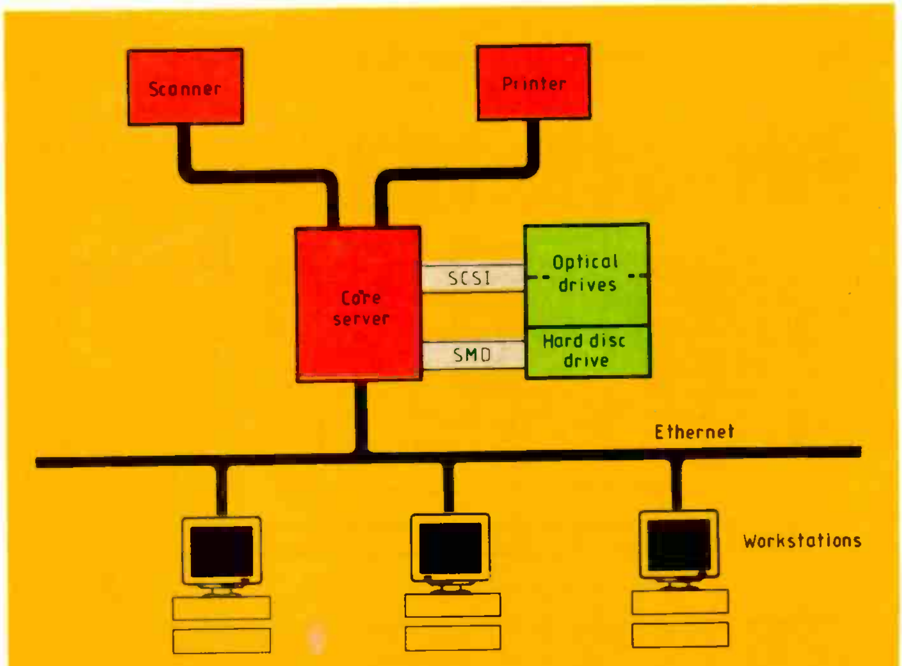
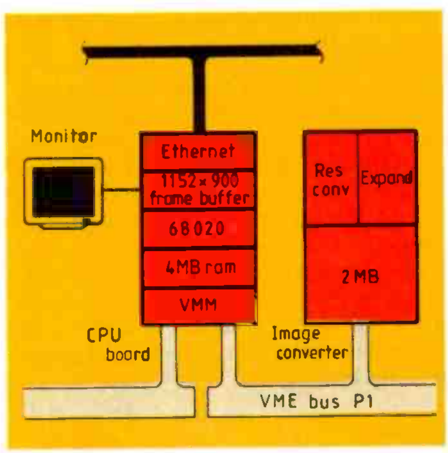


Table 1 System components

Scanner	– Canon 9030 S
Printer	– Canon 9030 P laser
Core server	– Sun Microsystems 3/160-4S plus scanner controller and printer controller boards
Optical drives	– Hitachi optical disc and formatter
Terminals	– Sun Microsystems 3/75 M plus Racal image converter board

A typical small department entry-level document processing system. Such a system could be expanded with more workstations and a small juke box to allow access to up to two million A4 pages.



The workstation has the same 68020 4Mbyte computer board as the core, running Berkeley Unix. Additionally it contains an image processor board which decompresses images and scales them for zoom/shrink operations. The workstation can support many simultaneous operations, allowing the user to interact with them via screen windows.

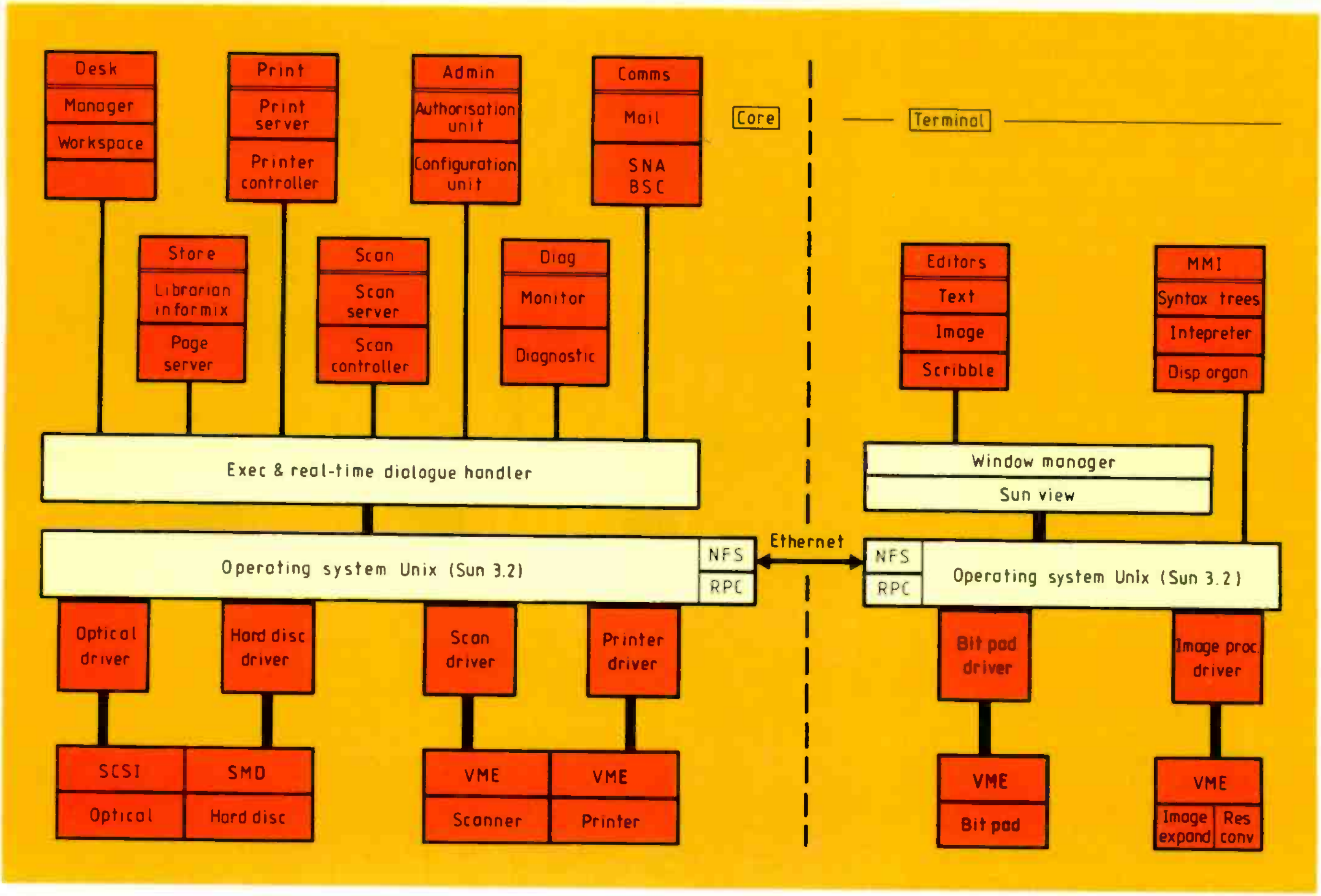
The compressed pages are actually held on magnetic disc in the document server.

Indexing

Before documents can be stored on optical disc they must be indexed with their filing/retrieval parameters. Selecting the Indexing function splits the screen into three windows 1 displays the document page images 2 displays an index card proforma, and window 3 displays the 'scanner in-tray' contents to show the number and type of documents and the number of pages in each. The operator can read the image pages which can be enlarged using the zoom button, panned and scrolled, browsing through them using 'next and previous' page buttons.

These effects are achieved by pulling the compressed pages off the magnetic disc and transmitting them to the document workstations via the Ethernet. The compressed images are decompressed in the workstation's image converter board to their original 200 or 400 element format. This image is then resolution-converted to the number of elements needed to fit the image into the display windows. For example, a display with a resolution of 1150h by 900v which used approximately half the screen to display an A4 image would have an effective resolution of 80 elements per inch. The converter would therefore apply a scaling factor of 2.5.

The image converter board uses special hardware to accomplish this conversion. The converter calculates a weighted sum of an array of 4-by-4 picture elements. The weighting emphasizes closely grouped black dots over dispersed dots, i.e. the detail. The array is stepped across the entire image to produce a new image with fewer picture elements. Similarly, zoom/shrink is



Reos is a distributed computer system. The applications programs running on the system synchronize their actions by exchanging messages via a real-time nucleus containing the Berkeley Unix operating system.

achieved by overscaling or underscaling the image with respect to the window.

Parameters keyed into the index card proforma can have a variety of checks performed on their range, type, pattern, etc. The card can contain up to 16 fields of 32 characters, the contents of which may be chosen to suit the application. The system can automatically insert parameters such as time/date, document type and a serial number. When the index card is completed the reference to the document in the scanner in-tray window disappears and is now in the 'out tray' ready for storage or mailing.

Storage

A document is stored with three actions. Data from the index card are written to a relational database on the server magnetic disc; compressed document images plus index data are written to the optical disc; and a unique reference indentifying the document and its location is written both to the relational database and to the optical image file.

Two regimes are available. One mode writes each image file out serially to one optical disc. The other mode associates a document with a folder. A set of folders can be allocated across a range of discs and they contain free space for additional documents and annotations. In both modes image files are written sequentially onto the disc in a similar way to tape: there is no explicit directory.

Because of the general lack of standardization of optical discs and drives, the system can use disc drives from either Hitachi, Optimem, or CDC/OSI. The optical discs store 1.2Gbytes per side, the equivalent of about 30,000 A4 pages, and the server drives up to 16 optical drives—on-line access to the equivalent of around 480,000 pages. An alternative to a number of drives is the juke box: a robot picker mechanism that can load, unload or turnover optical discs from drives as instructed by the server. A 32-disc juke box provides access to approximately two million A4 pages.

Retrieval

Wild card and wild string characters can be used when a document is to be retrieved. The operator fills in a retrieval proforma listing the document parameters that are to be used to search the card index database on the server magnetic disc. A list of matches is displayed in a selection window after a few seconds showing a customised subset of the index card parameters.

On selection of a document the first page or all pages are read from the optical disc on to the server magnetic disc. From there the first page is transmitted to the workstation via the Ethernet. As in the indexing case, the image is expanded, resolution-converted and displayed in a window. As the operator browses through the document by selecting next page, images are transmitted from the magnetic disc to the workstation memory. Subsequent browsing through these pages is faster when they are held in the workstation. For comparison, a second document can be selected from the selection list window, the pages of which will be displayed in a window next to the first image window.

Annotation & print

Page images can be annotated by typing or 'handwriting'. When annotation is selected an editor capable of handling the appropriate data type is activated–ASCII characters for type, and vectors for handwriting derived from a bit pad and pen connected to the image converter board.

Each editing session generates a page layer that is written to the optical disc. A layer can be thought of as a transparent sheet laid over the image, containing the annotations. Each layer can have visibility privileges and is date/time and user ID stamped so that annotations can be audited and operators lacking visibility privileges will be unable to view sensitive information.

Any image with its annotations can be produced in hard-copy form by the printer at 400 dots per inch on either A4 or A3 pages. The printer controller board located in the document server converts the page layers into a composite image. Image data is transmitted at 18Mbit/s to the printer, buffered and then used to modulate a laser diode producing an image on the printer's amorphous silicon drum. Sending to other Reos users is by filling in a simple envelope with the recipients log-in name.

Richard Kreuzer is product manager with the recently formed Fleet-based Racal Imaging Systems Ltd.

RESEARCH NOTES

New crystal cut

A recent paper in *Electronics Letters* vol.23 no.4 from the Bulgarian Academy of Sciences describes a new cut of quartz resonator with a very precise and linear relationship between frequency and temperature. Crystals with this property aren't unique, but others require cuts to be made with a precision of 30 arc sec and are hence very difficult to reproduce reliably.

The new Bulgarian resonator claims to be easily reproducible – no more difficult in fact than AT or BT cuts. Unlike these last cuts, however, the second and third-order temperature coefficients of the new crystal are so small that the change of frequency with temperature is virtually linear.

A practical crystal was constructed to operate on the third overtone at a frequency of 26.5 MHz at 0°C. In this mode the frequency change with temperature was 1kHz/°C, over a practical range of −60 to +280°C. Maximum non-linearity at any point was ± 0.9°C.

The paper points out that, with a basic stability of one part in 10^8 and an ability to measure increments of 0.0001°C, this new crystal cut should be especially valuable for meteorological applications and for a variety of scientific research purposes where accuracy and high resolution are vital.

Oscillating to a chemical beat

To those of us used to oscillators that are either mechanical or electrical, it might come as a surprise to hear that chemicals can oscillate too. According to Miklós Orbán of the L. Eötvös University of Budapest, if you take an alkaline solution of potassium thiocyanate and add some hydrogen peroxide and a pinch of copper sulphate, the resulting solution will oscillate periodically between a dark yellow tint and colourless.

This isn't the first known oscillating chemical reaction but up till now they've all required a pumped flow to keep them oscillating. This one apparently requires nothing more than an occasional stir. It's also unique in that it will exhibit bistability under certain conditions. If the chemicals are fed into a reaction chamber from separate tubes the resulting solution will take on some of the two steady state conditions, either yellow or colourless. But any slight perturbation or other energy input may cause it to flip into the opposite state.

As far as is known, there are no plans afoot to build a chemical computer, but the work is of fundamental interest beause of the insight chemical oscillators may provide into the biochemistry of circadian rhythms, heartbeats and other rhythmic processes in nature.

How to handle one atom

A team from AT&T Laboratories, Murray Hill, New Jersey, has demonstrated its ability to manipulate what amounts to a few chosen atoms on the surface of a crystal of germanium. This work is a development of a technique known as tunnelling electron microscopy (t.e.m.) which is normally used to build up a picture of the topology of a solid surface. The tunnelling electron microscope consists of a fine needle made from tungsten which is manipulated by means of piezo-electric transducers to within a few atoms distance of the surface being investigated.

At this distance, a small bias voltage will induce a tunnelling current to flow between the crystal surface and the needle. The value is typically 20pA at 1V. If the tunnelling current is then amplified and fed out-of-phase to the piezo transducers, the needle will be held at a constant distance from the nearest atom in the crystal surface.

By applying a lateral movement to the needle and plotting the vertical error signal against lateral distance, it is then possible to produce an image of the surface of the crystal showing details at the atomic level.

Using a near-perfect crystal of germanium prepared by ultra-high vacuum sputtering techniques, the AT&T researchers proceeded to draw a detailed map of a small (5×6.5 nanometres) area of its surface topology. This surface proved to be near-perfect.

Then they momentarily increased the bias to 4V, which they believe caused an atom-sized piece of germanium, previously picked up by the tungsten needle, to detach itself from the needle and bond itself to the crystal surface beneath. Subsequent t.e.m. scans at the normal 1V bias showed that such a piece of germanium had indeed bonded itself to the underlying crystal lattice.

The AT&T researchers were able to repeat this procedure with a high degree of reliability, demonstrating for the first time the ability to manipulate matter, virtually atom by atom. As yet they aren't precisely clear about the atomic structure of the resulting lattice, but, writing in *Nature* vol.325, the group are clearly excited by the potential of the new technique..."The final rewards may be high-density memories, new devices whose electrical properties are dominated by quantum-size effects, or the modification of a single self-replicating molecule on a surface."

Thin film research

Exeter University's thin film and interface group in the Physics Department has been awarded a grant of over £20,000 by the Science and Engineering Research Council for a preliminary study of the poorly-understood interface between electrodes and electrolytes. The study by Dr Roy Sambles and his colleagues, although highly esoteric at this stage, could have important implications for batteries, capacitors and electrochemistry generally.

At first sight the electrode/electrolyte interface might seem most accessible from the electrolyte side. But the Exeter studies are making use of a novel optical technique in which a ray of laser light is passed through a prism on to the *back* of a thin film electrode, a layer of silver or gold typically a few tens of nanometres thick.

Normally such a layer would simply reflect the incident light, like the silvering of a mirror. But at a certain critical angle the light is completely absorbed by a resonance effect that occurs at the metal/electrolyte interface.

By monitoring this absorption effect, Dr Sambles and his group have an extremely sensitive means of probing the detailed physical structure and charge distribution at the interface. This in turn should help clarify some of the complex electrochemistry on which many of today's charge storage devices depend.

Radar ice probe

A method of measuring the thickness of sea ice using a helicopter has been developed by Exxon Production Research Company and the British based company, Cambridge Consultants Limited. This method is the result of a research and development project, which began in 1981.

The method utilises an impulse radar unit, mounted on a helicopter which flies some three to five metres above the ice surface at a speed of five to ten knots while making thickness measurements. A broad-band, very short pulse of electromagnetic energy is emitted from the transmitting antenna which is mounted on one side of the helicopter. Part of this energy is reflected by the top of the ice, and part is reflected by the interface between the bottom of the ice and sea water. The reflected energy from both of the bottom and top of the ice is detected by the receiving antenna which is located on the other side of the helicopter. By knowing the time delay between the two received signals and the velocity of radar energy in sea it is possible to measure the ice thickness.

The thickness of sea ice is important in the design of oil and gas production facilities for use off the coasts of Alaska, Canada and Norway. Ice thickness determines the forces exerted by ice-floes against structure such as platforms set on the seabed.

In the past, most of the ice thickness data was obtained by drilling a hole through the ice with an auger, a process which is slow, tedious and consequently costly. With impulse radar it is possible to collect more data in thirty minutes than can be obtained by six-man crew drilling for two days. The new system is accurate to within approximately one foot of the drilled ice thickness measurements and

RESEARCH NOTES

can reliably measure ice about thirty feet thick.

Work is continuing to further refine the system so that it can produce more sharply defined images, and also on methods of enhancing the data obtained in the field by using signal processing techniques.

Who pinched Mona's necklace?

Computer analysis of the 450-year old Mona Lisa, Leonardo da Vinci's masterpiece that now hangs in the Louvre, shows that the artist originally painted his subject wearing a necklace. According to research by Dr John Asmus of the University of California in San Diego, there was also a background range of mountains near the face. Even the famous enigmatic smile is claimed to be the result of several overpaintings.

Previous infra-red and X-ray studies have revealed nothing except restoration that is already well documented. But although the picture was sold in 1517 much as we see it today, earlier copies do show a necklace.

Today it's virtually impossible to deduce anything by superficial examination because the painting has been dulled so much by its decaying varnish. What Dr Asmus did was take a good quality print and digitize it into 18 million pixels, each specifying the proportions of the three primary colours. He then obtained a colour profile for old varnish and, with a computer, subtracted this from the values taken from the original print. The result: a bright new-looking Leonardo! But that's not all. The subtraction revealed all the evidence of age cracks and extensive restoration.

The next stage of Dr Asmus's work was to programme the computer to remove obvious artefacts such as cracks by their structure and their lack of relation to other features of the painting. Finally, by means of image processing techniques normally used to enhance satellite pictures, Dr Asmus examined the picture for non-random changes in colour and contrast. This was to distinguish any unusual variations in brush strokes or over-painting.

The result confirms that a necklace was indeed painted out and that the smile has been changed many times since the original. This would suggest that what we see today is not the result of second thoughts by Leonardo, but the work of later restorers.

As yet, there is more research to be done and probably more curiosities to be revealed. So if you're still puzzled by the smile of the Mona Lisa, you're not the only one!

Handle with care

The University of Southampton Control Engineering Research Group have developed one of the most advanced artificial hands in the world which could, in a few year's time, give amputees a new lease of life.

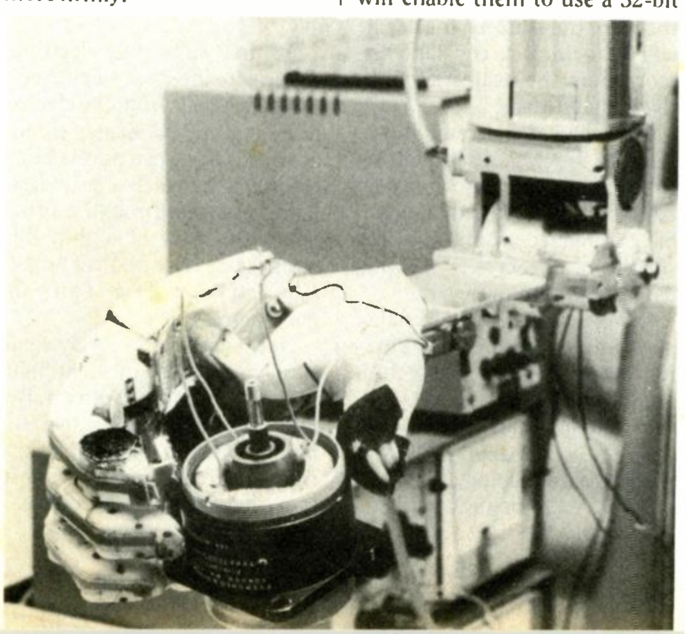
Today's artificial hands have little more than a simple open and close function, triggered by electrical signals from the patient's stump. No sensory feedback is provided, so the wearer must constantly monitor the activities of the hand by eye. Delicate movements are completely impossible.

What the Southampton group, led by Professor Jim Nightingale, have done is to add touch sensors operating under the control of a microprocessor. These allow the artificial hand to judge how much force it needs to apply to hold an object securely without at the same time crushing it. Should the object begin to slip, the hand grasps it more firmly.

Four motors drive the hand, two for the thumb, allowing it to move in two planes, one for the index finger and one for the remaining fingers. As with previous artificial hands, control signals are mostly derived from existing nerves, with only a limited need for conscious input from the user.

Now that a successful working prototype has been demonstrated, the research team intend to miniaturise the electronics to enable all the control systems to fit within the hand itself. Only the battery will need to be mounted elsewhere on the body.

Professor Nightingale is also developing a separate larger model for use as an industrial robot. The ability to pick up delicate glassware in a radioactive environment would be one obvious application for such a hand with sensitive feedback control.



Simulating power cuts

One of the most powerful microwave systems ever built is being developed at Bath University to deal with major breakdowns on the national electricity grid.

The CEGB and the Science and Engineering Research Council have given a joint grant of £86,361 to Mr Richard Daniels and Mr Rod Dunn of the University's School of Electrical Engineering to build a mock-up of the electricity network. The two researchers have been working on a model of the network for six years, using a relatively slow 16-bit processor. The new grant will enable them to use a 32-bit processor, at least seven times more powerful, with a bank of 12 microcomputers operating in parallel. The result will be a dedicated computing system that will enable the team to make a very detailed model of the grid.

CEGB control engineers will be able to use the model, both as a fault predictor and as a simulator to train on.

It will enable them to investigate alternative strategies in dealing with fault conditions or abnormal loads.

Companies get together in a SARI

A Silicon Architectures Research Initiative (SARI) is proposed as the third in a series of National Electronics Research Initiatives, which enable industrial collaborators to work together on pre-competitive research lasting 3-5 years.

A number of UK companies have already shown interest in participating in the SARI hosted by Edinburgh University's Department of Electrical Engineering, which has a considerable reputation in this area. The following organizations have begun discussions to formulate a programme: British Aerospace, Ferranti, Hewlett-Packard, Lattice Logic, Marconi, Mullard Plessey, Racal, STL, Thorn-EMI and Edinburgh University.

There is a significant gap between Britain's capability to develop and model algorithms on general-purpose computers and our ability to map these algorithms into real-time electronic hardware – especially in very-large-scale integrated (v.l.s.i.) form – and deliver competitive electronic systems. The proposed programme will address this problem by automating the algorithm-to-silicon design route. The intention is substantially to enhance UK expertise in design and specification of real-time systems, and in v.l.s.i. architecture and silicon compiler technologies.

The Department of Trade and Industry would like to hear from any other companies or organizations who might wish to participate in the SARI.

Research Notes is written by John Wilson.

TELECOMMS TOPICS

Fair competition in international access

The Office of Telecommunications has issued a Determination which will govern the arrangements that British Telecom and Mercury Communications may make with overseas telecommunications operators for the sending and receiving of international messages. According to Oftel, "this takes the process of liberalization a step further by providing for the introduction of competition in international telecommunications services, where this is likely to be the ultimate benefit of consumers."

This Determination ensures that overseas monopolistic operators cannot use the competition between BT and Mercury to gain an unfair advantage. It rules that BT and Mercury will be obliged to accept exactly the same financial and other terms with overseas operators, other than in exceptional circumstances. This has been called "parallel accounting".

Prof Carsberg, Oftel's Director General, sees the ideal arrangement between BT, Mercury and an overseas operator as one where the overseas operator agrees to give BT and Mercury "proportional return", i.e. the overseas operator will send traffic to each of the UK companies in the same proportion as the traffic it receives from each of them. This arrangement would ensure that if Mercury generates outgoing traffic it will receive its due share of incoming traffic.

Guernsey's repeaterless cable

The world's longest unboosted undersea optical fibre cable will run 135km (84 miles) between the island of Guernsey and Dartmouth. The cable will have six fibre pairs, of which two will be employed immediately the cable comes into service. The system will operate at 140Mbit/s so giving each pair a capacity of 1920 simultaneous calls.

The cable will use the latest single-mode technology operating at 1535nm with much narrower line width than that of earlier designs. This reduces the effect of chromatic dispersion and thus increases repeaterless path lengths. A £5.7million contract for it has been awarded jointly by British Telecom and the Telecommunications Authorities of Guernsey and Jersey to STC Submarine Systems. This award follows the recent order, also to STC Submarine Systems, for a 90km cable to Douglas, Isle of Man.

Government telecoms network

British Telecom is to install the computer system for managing the Government Telecommunications Network (GTN), the UK's largest private voice network. BT's Communications Facilities Management (CFM) unit has won the contract from the Central Computer and Telecommunications Agency (CCTA) under which it will supply its Linesman computer-based system and network management products and services. BT will also act as project manager for the installation of the system. Starting shortly, completion is scheduled by Spring 1988.

The GTN interconnects Government offices in London with regional and local offices around the country. At present it consists of around 460 p.b.xs, serving 170,000 extensions. The p.b.xs are interconnected by a network of tandem (call forwarding) exchanges linked by 2Mbit/s digital private circuits. These exchanges route calls between extensions in different parts of the country.

The Linesman system will run on a central processor at CCTA headquarters in London, linked to microcomputers at each main tandem exchange. These will log calls and provide remote access for configuration changes, alarms and supervision. In addition to its Linesman network management system, BT's CFM unit will supply network diagnostics equipment to check circuits for availability and quality of transmission. Central autodiallers will generate test calls through the night and monitor the performance of the network from responses to the calls provided by local transponders.

Skyphone take-off

In-flight trials of the first worldwide satellite telephone service for air travellers starts this autumn. British Telecom International and the authorities of Norway and Singapore, are to work toward providing global coverage for the service to be launched by BTI on the transatlantic routes next year following the trials.

The cost of calls has not yet been finalised for the Skypnone service which will allow passengers to make their own telephone calls from planes, payment being made by credit card. Initially, it will not be possible to receive incoming calls. The service will also offer telephone and data message facilities for airline operations.

A dedicated earth station is available at Goonhilly Downs in Cornwall for this service and similar new earth station facilities will be provided in Norway and Singapore.

Efficient p.b.x-to-trunk integration

Timeplex, which has transferred its UK headquarters from Leeds to Langley, Slough, has launched its Link 2 Facilities Management System in Europe. Aimed at meeting the needs of the now maturing digital voice and the more established data networking environments, Link 2 provides a more efficient way of integrating a digital p.b.x to 2MBits/s or similar digital trunks. It is essentially a synchronous time division byte-interleaved multiplexer operating at data rates from 4.8Kbit/s to 2.04Mbit/s and supports a wide range of port rates, both asynchronous and synchronous.

Victoria Brown, senior vice president of Timeplex Inc. who was in the UK for the launch, said that the company expects a great demand for the new Link 2 from both new and existing customers, revealing that over 5,000 Link 1 systems have already been installed worldwide. Pointing out that America's standard T1 digital transmission system at 1.544Mbit/s (and therefore 2Mbit/s in Europe) has become "the cornerstone of private networks", she said the most important reason for this was that T1-based private networks provided the opportunity to save "literally millions of pounds in communications costs."

Bryan Gray, VP International of Timeplex, Inc. of New Jersey, previously managing director of Timeplex UK, said "Over the next few months, we will be putting in place a new International Group, based at Langley, which will support the entire Timeplex international organisation and customer base which is outside the North American continent." Among its facilities will be a fully equipped training centre.

Centrex in the UK

Centrex, best described as providing p.b.x facilities from the local exchange, is to be offered by both British Telecom and Mercury Communications. Northern Telecom has completed its programme and claims that "the Mercury Centrex is the first of its kind outside of the US" and a Mercury spokesman said the company has prepared its tariffs, and will disclose them as soon as it is ready to offer the service. Similarly, British Telecom, which is to launch the pilot phase of its Centel 100 service in London in August as the start of a national implementation plan, will publish its charges shortly. They will consist of connection fees plus rentals with the possibility that customers will have the opportunity of spreading their connection payments, thus reducing the initial outlay.

However, as the day draws closer when Centrex services are actually introduced, their likely impact in the marketplace is more widely recognised but not understood.

Oftel has published a consultative document entitled "Centrex: the Regulatory Issues" which outlines a number of issues which Oftel has identified as requiring decisions. It also gives details of the proposed modifications to BT's and Mercury's licences to allow them to provide Centrex services in a way which might otherwise breach the letter (though not the spirit) of the prohibition on simple resale of telecommunications services.

Telecom teach-in

London Business School has launched a new international management programme for senior executives in the telecommunications industry. The two-week residential course, designed to be of relevance to all interests in the telecommunications industry, will consider the major forces for change facing the industry: in particular, national and international deregulation and technological developments.

The strategic implications of these for market opportunities and costs will be examined, and the issues and skills most relevant to senior management's analyses. The topics will include the management of strategic alliances and organisational change; the assessment of market opportunities and risky projects; and marketing and pricing in a competitive environment.

Further information on these courses, the first one to be run from 14 to 26 June, from Kim McCarthy, London Business School, Sussex Place, Regent's Park, London NW1 4SA. Tel: 01-262 5050. Telex: 27461 LBSKOX G.

Exchanges for Arabs

Following a study conducted jointly by UK consultancies British Teleconsult (a division of British Telecom) and KMG Thomson McLintock, a joint programme to develop advanced public telephone exchanges for use within the Arab community has been decided upon by PTT experts, government officials and investors from seven Arab countries. The programme, looking at a potential market worth around $200 million, is the outcome of a study commissioned by the Arab Industrial Investment Company.

Most of the countries involved have yet to install digital equipment in quantity, but once they do, the market will grow rapidly. "Our conservative estimate" says project manager, Andrew Dymond, "is that the annual market for digital equipment will be close to 1.2 million lines by 1990, and that the number of new installations will grow at 6% annually until the end of the century."

In view of the fact that annual sales of 250,000 lines would be needed to make domestic manufacture economically viable, and that demand studies show that four countries in the region currently require over 100,000 lines, the consultants recommend that the Arab countries should set up one or two joint plants before their markets are fragmented by external supply. Egypt has already invited tenders for a factory to meet its own needs. However, it is believed that both GEC and Plessey have been excluded on the grounds that UK's System X has not won appreciable orders in the international marketplace. Front runners are probably Alcatel (now incorporating ITT's System 12), APT (AT&T and Philips Telecommunications) and Ericsson.

Contract news

Plessey Telecommunications Products Ltd has won a national account-call development contract from British Telecom together with orders for national credit card payphone systems from Sweden and Spain.

The BT contract, initially worth £1million, is for the development of two prototype account-call systems. Known as Cashless Services Processor Units (CSPU), these prototypes are expected to be available in mid-1988. Once implemented, the system will allow users of payphones to have the charges logged directly onto their own office or home telephone accounts. Orders for additional systems, said to be worth £7.5million, will follow to give full national coverage. As well as this, Plessey is waiting to receive repeat orders from BT for public payphones, an area where BT is the monopoly supplier, which could be worth as much as £15m.

Televerket, the Swedish PTT, having completed a six-months field trial with credit card payphones is moving to national introduction with 2,100 units being installed in major cities at a cost believed to be around £2 million. This number could grow to 10,000, dependent on user acceptance.

Spain's Telefonica, having worked closely with Plessey to develop a customised cashless calling system for Spain, is running a series of payphone trials comprising joint coin and credit card units in Barcelona and Madrid, and a prepaid card trial in Madrid. The value to Plessey of the contract is approaching £1m, including development charges. In addition, the Finnish PTT has invited Plessey to install a payphone field trial.

East Midland Electricity Board has placed a contract with Newbridge Networks Ltd for the supply of a network of Newbridge 3600 Mainstreet digital network bandwidth managers. The system to be provided is to allow the interconnection of high-speed digital services provided by various carriers, including BT and Mercury, between Board offices and communication sites. The Newbridge systems are for use in 2Mbit/s-based backbone networks and will provide high-speed data interfaces to ISDN standards. Later on this year the system will be upgraded to provide network control and management from a single central location.

Newbridge Networks Ltd, based at Chepstow, Gwent, is the European end of the Ottawa-based company founded by Terry Matthews, former Chairman of Mitel, which is now a subsidiary of British Telecom.

Britain's National Computer Centre has been awarded a contract for the supply of an OSI transport-layer testing system by the US-based Corporation for Open Systems (COS). Worth nearly $1 million, the contract is the first to be awarded by COS following its worldwide call for proposals last September. COS was formed last year with the specific intention of providing credible testing services for OSI-based communications systems. Its membership includes all major US-based vendors of computer communications equipment, as well as a number of influential users, including CCTA in the UK.

Commenting on the award, Dr Tim Wells, responsible for standards and software engineering at NCC said "The award of the contract to NCC means that the same basic technology will be in widespread use for transpor layer testing both in Europe and North America. The effect of this will be that systems tested in different countries are much more likely to interact, and genuine operational OSI will be a step nearer. NCC launched the world's first commercial OSI testing service based on its transport testing system in 1985. The adoption of the system by COS is vindication of the quality of this service and of the risk taken by the NCC two years ago."

Cellnet, one of the two cellular radio network operators have placed orders worth £16 million with Motorola for transceiver (£12m) and switching equipment (£4m) to operate on the new London-area frequencies which will be freed for cellular operation before the end of the year.

Having already invested £22million ($35m) in enhancing its London network by splitting cells into six sectors and increasing the number of available voice channels over a smaller area, Cellnet claims to have increased the possible number of subscribers within the capital by a factor of 2.5.

Development of the technology necessary to implement the new frequencies is already well advanced and the company expects to bring them into operation by the end of the year. In addition to work on the fixed network, cellphone manufacturers are working to introduce the slight modifications necessary to use these extra frequencies in the new ETACS (extended total access communications system) specification.

Cellnet's managing director, Colin Davis, says that Cellnet already has the most advanced cellular system, ensuring that there is no justification to tamper with the frequencies to be held in reserve for the projected European-wide digital system planned for operation in 1991.

More on page 658.

Telecomms Topics is written by Adrian Morant.

Low-cost factory network

Based on the Bitbus remote access and control interface, this manufacturing cell datalink is cheaper to intall than the Manufacturing Automation Protocol yet offers nearly all its facilities, as well as the ability to mix STE, VME and PC systems on the same network.

S. HINTON, N. D. McQUILLON & B. WORTH

Recent developments within factory automation include the recognition that 'islands of automation should not be allowed to remain in glorious isolation. For the larger organizations the way has been led by General Motors with its Manufacturing Automation Protocol, by which the might of GM is persuading computer and control hardware manufacturers to speak their language.

But what about the smaller organization where the high performance and associated high cost of MAP may be impossible to justify? How can the average-size manufacturer integrate both new and existing machines or install inter-machine data exchange media at an affordable price?

Involved for many years in machine control and latterly in manufacturing cell integration, we have identified this need for an efficient and cost effective data transfer vehicle capable of interconnecting a number of independent, possibly isolated, machine or process control systems and operator interface media with a central facility.

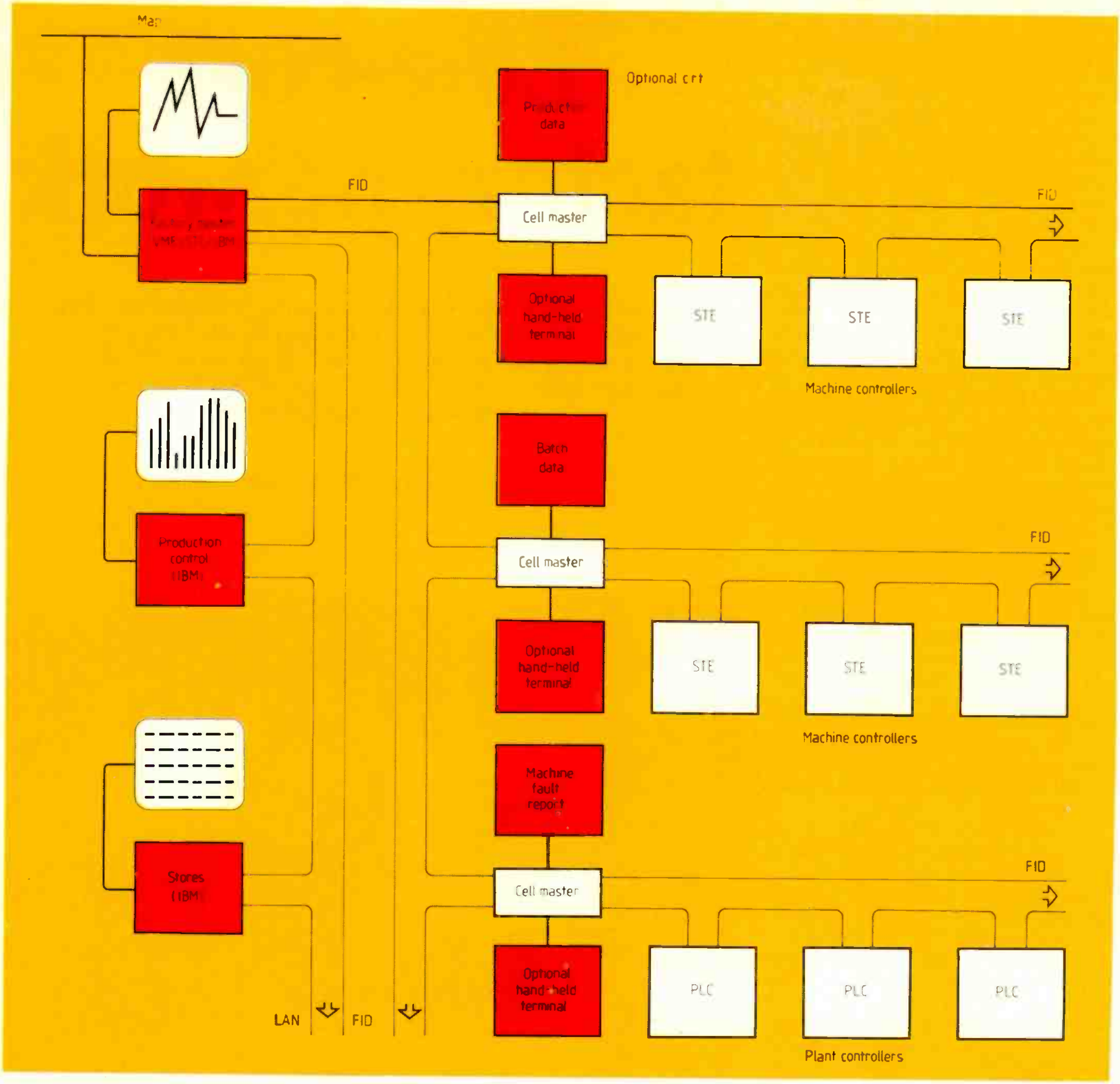
The Factory Information Datalink is based on the RS485 data communications standard, which allows one master station to be connected to a number of slave stations on a multi-drop configuration via low-cost, single twisted-pair cable. Distances up to 1.2km can be achieved without repeaters at rates of 62.5Kbit/s although higher rates are achievable over shorter distances. The Datalink protocol and message formatting are based on Intel's Bitbus which is a subset of IBM's SDLC protocol.

The slave station will typically be an embedded microcomputer system, such as STE or VME-based microcontrollers or industrial IBM PCs, programmable controllers, and factory-floor data entry terminals. The master can be a VME industrial microcomputer, IBM PC or compatible, or an Intel microcomputer. In most organizations, this configuration will be the limit of what will be required for some time to come. But where the factory is large enough to justify a factory-wide MAP scheme either a VME or PC-based master can be provided with a MAP gateway board, making it the master for a manufacturing node. The advantage of this approach is the ability to mix STE, VME and IBM PC systems on the same network at very low cost, providing a link to other administrative lans with their inherent databases associated with production control, stores and maintenance departments.

Other system vendors have recently announced products capable of interfacing with Bitbus, indicating that it has already achieved multi-vendor status with similar commitments from Intel, Honeywell, Toshiba, Dec, British Telecom, Arcom, Analog Devices, GMF Robotics and Westinghouse.

PHYSICAL CHARACTERISTICS

The network consists of a multi-drop configuration with the equipment at each node being 'daisy-chained'. The communications cable is a relatively low-cost, screened twisted-pair cable with a characteristic impedance of 120 ohms. In a simple self-clocked network with no repeaters only one pair is needed in the cable and the cost can be as low as 50p per metre.



Factory Information Datalinks can be cascaded to link manufacturing cells with factory master and associated administrative networks.

The connector and its pin-outs used at each node on the cable is defined by the Bitbus specification. This connector is an inexpensive nine-way sub miniature D-type, which is a smaller version of the connector specified for the ubiquitous RS232 standard. At each node the equipment is provided with a male and female bulkhead connector wired in parallel. To remove a node from the network, the cables can be disconnected from the equipment and the free ends connected together. The network traffic is only interrupted for the short period required to restore the continuity of the cable. This can be carried out whilst the network is live and recovery is automatic. As usual with data communication cables, a terminator is required, which consists simply of a single resistor.

ELECTRICAL CHARACTERISTICS

The electrical characteristics of any data transfer medium comprise two elements, namely the d.c. a.c. parameters of the transmitters, receivers and terminators, and the data encoding technique used to pass data on the medium. The Bitbus specification uses established internationally recognized standards for each.

The d.c./a.c. parameters are defined in the EIA RS485 standard, a multi-drop, master-slave version of the well-known RS422 differential transmit/receive standard. In self-clocked mode, the data encoding technique uses NRZI (non-return to zero inverted with zero-bit insertion-deletion). Synchronous mode employs a return to zero scheme, where a 'one' is represented by a high level and a zero by a low level. The more complex NRZI represents a 'one' by no change in level and a zero by a change in level. Zero insertion/deletion (bit-stuffing) ensures that a level transition by the insertion of a zero after a sequence of five consecutive ones. This maintains the self-clocking, the extra zeros being removed by the receiver.

PERFORMANCE

In synchronous mode, between 500Kbit/s and 2.4Mbit/s can be achieved over 30 metres with 28 nodes. Using self-clocked mode, up to 1200 metres is possible at 62.5Kbit/s, falling to 300 metres at 375Kbit/s. As with all frame-oriented protocols the bits per second rate does not reflect the actual rate of transfer of information. With the FID protocol, an overhead is incurred due to the need to provide comprehensive error checking and packet routeing. To give some idea of information transfer rates, in the self-clocked mode at 62.5Kbit/s, a worst case of about 1000 bytes per second is estimated. This corresponds approximately to the information transfer rate possible with RS232 at 9600baud. However, if the processor at the master and slave is capable of an immediate response, which would be the case if a dedicated communications processor such as the Intel 8044 BEM is used, then it is possible to achieve 10,000 bytes per second at the same bit rate.

The robustness of the network is assured through the error checking carried out at the different protocol levels. From the lowest levels up these are:

- At the end of each frame transferred on the bus there is a check sequence field containing a 16-bit cyclic redundancy check word.
- Sequence counts are maintained by both slaves and master to ensure that no frames are transmitted without an acknowledgement being received. If the sequence counts do become out of step then a mechanism for re-synchronization is automatically invoked.
- If the master does not receive a return frame from a particular slave within 10 ms of transmitting a frame to it, then after a second such failure then the synchronization mechanism is invoked.
- The message format is checked for correct length, message type, and the correct slave address.
- The master receives a reply for each command sent to a slave. This reply has a response field which is used to indicate the acceptance of the command or rejection, indicating the reason for rejection.

All of this error checking concerns automatically recoverable errors. Obviously, if a catastrophic error such as a cable break or slave disconnection or failure, the master will be unable to communicate with the slave. However, when the fault is rectified, the communications will automatically resume without human intervention. A time-out detects this type of fault and the higher application levels of software are signalled with an appropriate error number.

FID SERVICES

One of the tasks supported by FID is reserved for remote access and control, defined as an option in the Bitbus specification, and provides the following facilities:

— reset slave
— read i/o
— write i/o
— update i/o
— upload memory
— download memory
— status read
— status write
— OR i/o
— AND i/o.

The resulting systems interface will permit such activities as:

— remote target system activation
— remote target system i/o monitoring
— remote target system variable editing
— upload/download of volatile memory
— remote target system status monitoring.

FID PRODUCTS

The range of eight-bit (STE) and 16-bit (VME) bus-interface modules and RS232/422 to RS485 convertor modules now on the market are:

STE to Bitbus or FID board

Trebit is a non-intelligent board providing the SDLC usart and RS485 drivers for the FID interface. It does not contain a dedicated communications processor so that communications software is required for the host processor.

Tutil is similar to the Trebit board but with the addition of further system utilities, such as a watchdog, system clock, analogue i/o, system reset switch, two channel incremental encoder input and one RS232 channel.

Tifid contains an Intel 8044 BEM i.c. which implements all the levels of Bitbus with minimum main host processor overheads.

VME A VME board is available which contains an Intel 8044 BEM processor.

Hand-held terminal

Incorporates a four by 40 character back-lit liquid crystal display, 16-way operator key-pad, RS232 serial channel, and an FID interface. Other interface options include bar-code readers, magnetic card readers, and light pen.

RS232 to FID converter

To enable existing systems provided with an RS232 serial port to be connected to FID, a converter module is available.

Software

Intelligent boards such as Tifid and the VME Bitbus board contain all the levels of the Bitbus protocol in firmware within the Intel 8044 BEM processor chip. With the STE Trebit and Tutil boards, and with the Olivetti M24 computer fitted with the 8530 SDLC usart, the data link and message protocol layers, and RAC are implemented in software. This software has been written in C language to provide maximum portability over a range of different hardware configurations. For example the C source has been compiled on the Olivetti M24 using the Microsoft C compiler under MSDOS for execution by the machine's 8086 processor; on a 68008 STE system using the Microware C compiler running OS9 and using Whitesmith's Z80 cross-compiler running under Unix System V for an STE Z80 target system. It should be possible to port the software to other target systems relatively easily.

IBM PCs AND COMPATIBLES

Products are now available to enable the widely used IBM PCs and their clones to be connected to Bitbus. Intel manufacture a Bitbus board that plugs directly into the IBM PC bus. There is also a bus converter which enables Intel's iSBX 344 board to be used in an IBM PC.

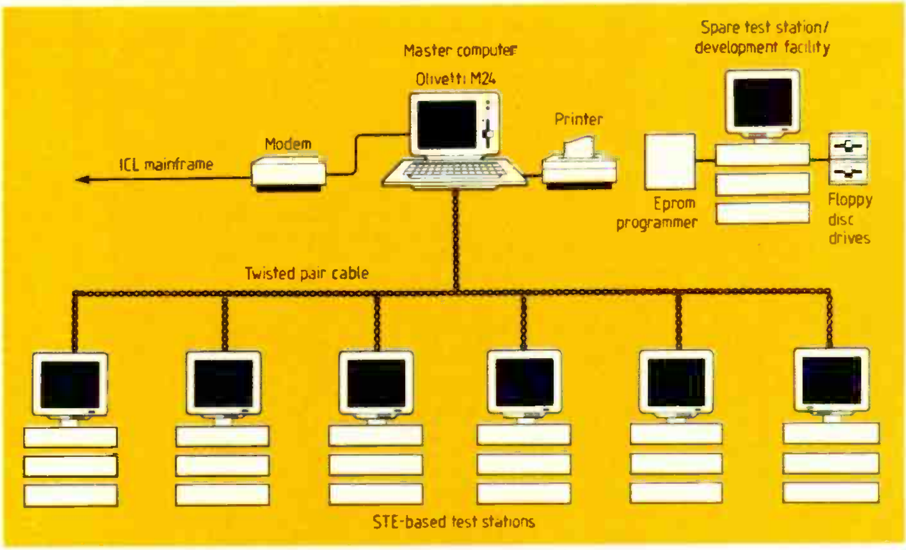
The Olivetti M24 can accept an SLDC usart that enables a Bitbus interface to be configured at relatively low cost. However, whereas the Intel board implements all levels of the protocol directly using the 8044 BEM i.c., this approach requires communications software for the computer host processor running under MSDOS.

TYPICAL APPLICATION

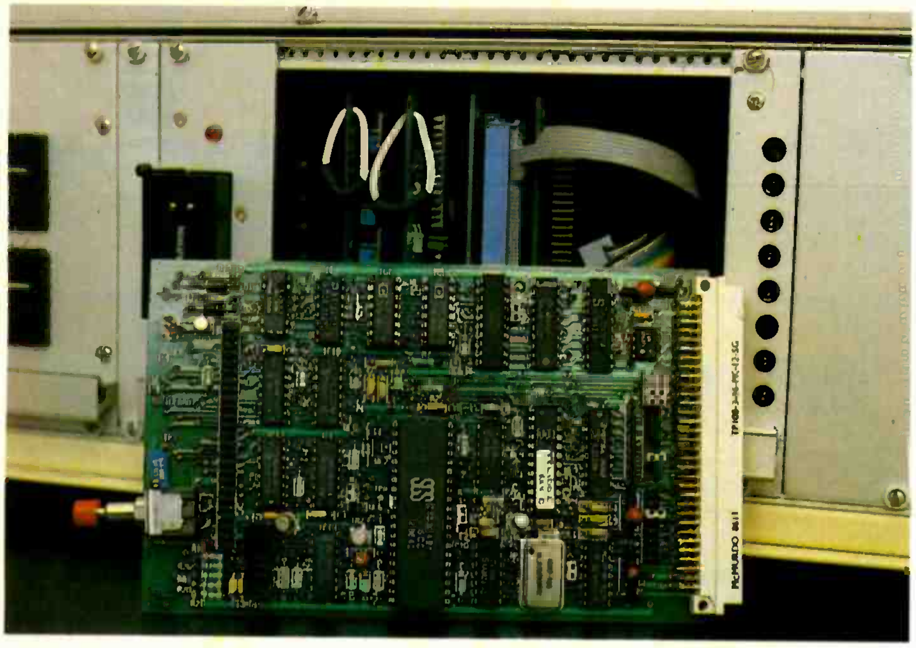
The rather abstract discussion so far can perhaps be better understood in the light of a typical application. Here we describe a recently installed and working implementation of FID. It is representative of a small-scale, low-throughput, low-cost system that is more than able to meet the requirements of the application and still allows plenty of scope for expansion.

The customer is a vehicle manufacturer with a large range of models with many options available on each model. Vehicles are therefore not built in large batches and consequently each vehicle has a unique test requirement. As each vehicle rolls off the production line it is inspected to ensure that it meets the works order and that there are no apparent defects. A thorough functional test takes place, with the tester recording over 100 performance parameters. For safety reasons tests must be performed in a predetermined sequence, with the testing of the vehicle being aborted if a critical safety test is failed: e.g. an earth fault on the vehicle.

A need for computer-assisted testing had already been identified by the customer, who saw it reducing testing time, improving



Schematic illustrating the application of Factory Datalink to a multi-station computer-aided test system.



An FID Development Station supplied to a customer for both software development and 'hot spare' purposes.

accuracy and reducing the chance of errors being made by testers. Originally the customer envisaged a computer-assisted testing station at the end of each of four production lines, with the possibility of another station for use at a further dynamic testing facility and also one at the final inspection site. Without the ability to communicate with other computers, these test stations would have had to be able to store the large amounts of data needed to test several different vehicles. They would also have needed a facility to print test results and to load data manually, possibly via floppy disc, which would have been unsuitable in a factory environment. The cost per slave station would therefore have been fairly large.

After considering the requirements we proposed a solution of a central computer, an Olivetti M24 with 20Mbyte hard disc and printer, connected to the slave test stations via FID. The slave stations would be low-cost, low-power but with enough capacity to hold the data for one vehicle and perform the testing of that vehicle autonomously. A Z80-based STE system was chosen; all the test stations being identical to allow rapid repair by having a single spare system standing by. The spare system had a second function of being able to be easily converted to a software development facility by plugging in floppy disc drives, extra memory, an eprom programmer and a printer. The new approach thus had the following advantages on top of those already acknowledged under the original scheme:

- Lower cost per test station.
- Lower overall cost for the given number of stations despite the overhead of a central computer.
- Ability to test any vehicle at any station, knowing that the testing parameters will be available.
- Possibility of connecting the system to the company mainframe through the Olivetti M24 and obtain the works order as entered by the sales department.
- Storage of data that would otherwise have been discarded.
- Storage of test results for a large number of vehicles other departments on IBM PCs and ATs already available to them. This would allow trends and production problems to be identified and rectified.

The central computer, or master, is based on an Olivetti M24. The M24 can accept on the main p.c.b., a communication i.c. capable of synchronous SDLC data transfer, the basis of Bitbus and FID. With the installation of this usart and the addition of a small board providing the necessary receiver and driver chips and a crystal oscillator the computer was converted to the heart of the FID network. The software needed to implement the Bitbus protocol was written in the C language and interfaced to the application programs, written in GWBASIC, through MSDOS. The application programs for the master and the slaves were written in basic for ease of modification by the customer. The communications software was made transparent to the applications programs and written in C enabling it to be readily transported to other computers. The slaves comprised in STE backplane with Z80 processor board, c.r.t. graphics controller board, additional eprom memory board, i/o board, and the tutil board already described, all of which are off-the-shelf items. Signal conditioning was provided outside of the STE backplane.

When a vehicle is ready for testing it is taken to a test station where its works order number is keyed in to the test computer and sent to the M24 master computer which accesses a works order file for this vehicle. A series of data transfers then take place as the options specified for the vehicle are sent to the test station and verified by the tester. Faults found by the tester are entered as codes and sent to the master. The sequence of tests to be performed for the particular model are then sent to the test station, followed by the parameters that are to be met during those tests. No further transfers take place until the testing of the vehicle has finished, when the results are sent to the master computer which then prints a test result sheet. A vehicle test takes between an hour and an hour and a half, and during this period a test station will not use the FID network for more than a total of 45 seconds; with six test stations in operation at once utilisation of the network is currently below 10%.

IMPROVEMENTS

Since accepting the concept of FID, the customer has seen further areas of improvement that are possible with the present set-up. At the moment the works order information for each truck has to be entered manually at the Olivetti M24 using a dedicated screen editor, although defaults are entered automatically by the computer. As this information is already available on the company ICL mainframe a modification is now to be made to the system to allow it to receive this information via a modem link through the ICL CO3 protocol under the ICL VME operating system.

Whilst certain functional tests are occurring, many readings are taken. If a tester thinks that the vehicle is behaving oddly he can request that performance graphs of the readings relating to the truck be plotted on the test station screen. The proposed modification to the system will allow the tester to send this graphical information to the central computer where it can be stored for later investigation by design engineers.

The Trenan Factory Information Datalink represents a new approach to an old problem using new standards to reduce costs and increase efficiency. The system will be inherently easier and cheaper to install, and can provide nearly all of the advantages of MAP at this level without incurring the cost overheads of full compliance with a specification that, for many installations will be overkill. In particular, broadband MAP requires an expensive r.f. modulator at each node and for each network an even more expensive head-end remodulator. The various FID modules allow the standard to be implemented with the minimum of disruption to existing installations and impose the minimum of restrictions on the design of new equipment to communicate with it.

Stephen Hinton and Brian Worth are founder members of Trenan, formed in 1982. With a grounding in mechanical engineering, Stephen has many years of experience in the application of intelligent instrumentation systems, microcomputer-based data acquisition and control systems. With a degree in electronic engineering Brian is responsible for the technical development of the company and has been a driving force behind the FID project, being experienced in the engineering of both programmable logic and computer-based solutions to real-world problems. Neill McQuillin joined Trenan in 1985 having gained experience working for an international electronics company. Neill has a degree in electronic engineering and has been responsible for much of the development and the first practical implementation of the Datalink.

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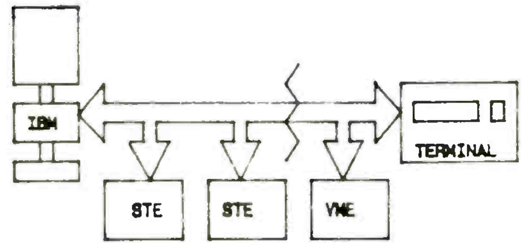

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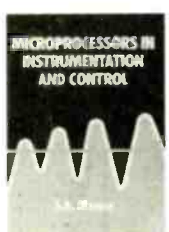
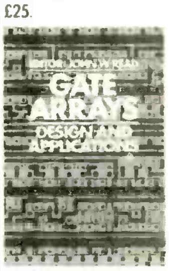
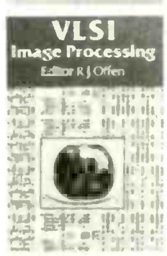
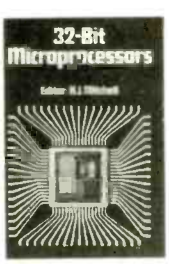




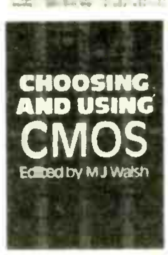
Gate Arrays: design techniques and applications, edited by John Read (of STC Communications Ltd); hard covers, 368 pages. Practical guide, covering hardware technology choices and CAD software for successful systems design. £25.

VLSI Image Processing edited by Raymond J. Offen (of the GEC Hirst Research Centre); hard covers, 336 pages. Authoritative contributions from a variety of specialists covering all aspects of this rapidly developing field. £30.



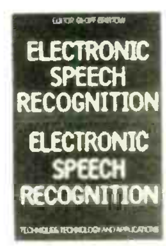


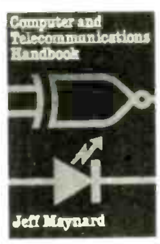
32-bit Microprocessors edited by H.J. Mitchell (of CAP Scientific Ltd); hard covers, approximately 350 pages. Architecture of 32-bit processors, development aids and application areas; offers one of the first comparisons of available 32-bit devices. £30.



Choosing and Using CMOS edited by Mike Walsh (of AMI Microsystems Ltd); hard covers, 312 pages. Theory and applications of analogue and digital c-mos devices, including gate arrays, from industry experts on both sides of the Atlantic. £30.

Electronic Speech Recognition edited by Geoff Bristow (of STC Network Systems); hard covers, 416 pages. Introduction to speech-recognition techniques and technology, with a wide-ranging examination of practical applications. £30.





Computer and Telecommunications Handbook by Jeff Maynard; hard covers, 248 pages. Invaluable miscellany for the engineer; includes telegraph and radio codes and assignments, tables, explanations of symbols, details of relevant BS, ANSI, CCITT and other standards plus much other reference material. £14.95.

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The box loop

Easily constructed indoor loop antenna reduces effect of mains-borne interference for short-wave listening.

G. W. SHORT AND V. SMITH

The aerial described here was designed to help listeners to the BBC External Services short-wave broadcasts. Many such listeners live in flats or houses with no outdoor space for erecting aerials. Mains-borne electrical interference can be a problem, and in some places there is strong co-channel interference, which may take the form of deliberate jamming by a local transmitter.

These circumstances lead naturally to the use of a loop aerial. The relative insensitivity to electrical interference and the directional properties of a loop can give useful protection against mains-borne noise and local co-channel interference. As Schemel showed in a very informative article in this magazine[1] a loop of relatively moderate dimensions can provide enough signal pick-up to swamp atmospheric noise. More recent publications[2,3] have explored the possibilities of making loops from easily obtained materials and adapting them for use with domestic receivers.

COMBINED LOOP & SCREEN

An essential of any directional reception arrangement is some method of preventing the direct entry of signal into the receiver. Direct signals bypass the loop, reducing its null depth, and in general the routes by which these signals reach the receiver also permit the entry of electrical noise from domestic appliances. Mukherjee[2] describes how a reasonably effective screening box can be made by covering an open-fronted cardboard box with aluminium foil and placing the receiver well inside it. An external loop is connected via a feeder which passes through the box and couples to the receiver by a home-made balun. This is a flexible and effective arrangement, but it does still call for rather more constructional ability than can be expected of the average domestic listener.

The aerial scheme described below was prompted by the thought that four of the sides of a foil-covered box themselves form a loop. The screening box itself is thus a potential loop aerial, Fig.1. Since the receiver is located inside the screen, problems of downlead pickup vanish and no balun is needed.

An open-fronted box is, however, a poor loop aerial, because the back shorts the loop. This effect can be reduced to tolerable proportions by cutting narrow slots in the back foil to convert it into a Faraday shield, Fig.2. If the slots are spaced not more than about 20mm apart most of the eddy-current damping of the loop is eliminated. The shield is connected at the bottom and to the foil on the frame of the box by an overlap.

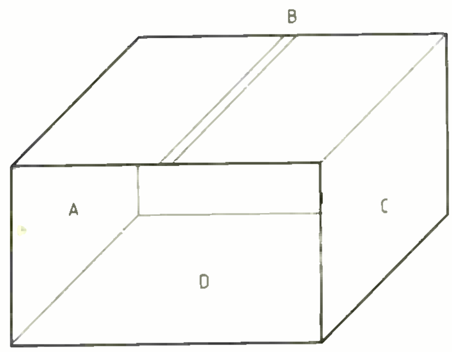


Fig.1.

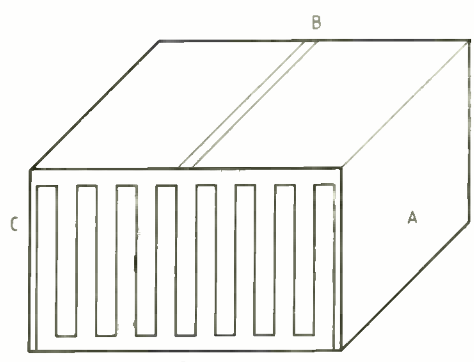


Fig.2.

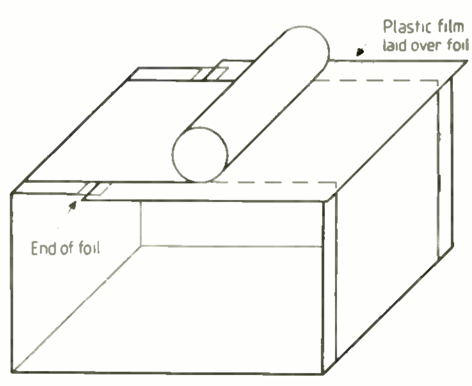


Fig.3.

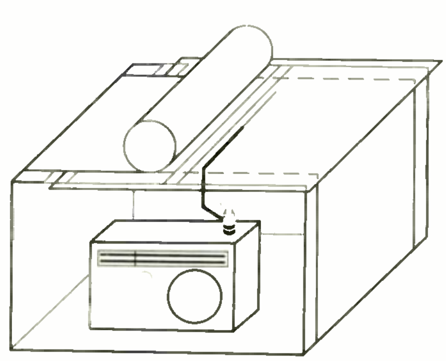


Fig.4.

TUNING THE LOOP

The sensitivity of a loop can be greatly increased by tuning it. The effect is essentially to increase the circulating signal current by a factor of Q. Since the box loop is a broad band of quite pure aluminium, Q can be high, even though the inductance is only of the order of 1μH. Conventional tuning capacitors can be used, but there is a simpler method. The loop foil is made to go round the box for more than a complete turn. Plastics film inserted into the overlapping area provides a dielectric. By adjusting the area of overlap the loop can be tuned. In practice all that is needed is to leave some spare foil on the roll, Fig.3, and unroll it over the film to tune the loop. The capacitor so formed is not very stable, but it is usable.

RECEIVER COUPLING

This can be inductive or capacitive. The simplest method is just to erect the pull-out whip aerial so that its tip is close to one edge of the gap in the loop foil. However, this may not provide enough signal transfer. The loop-to-whip capacitance can be increased by wrapping the insulated end of a wire round the whip and connecting the other end to the foil by baring a length of conductor and slipping it between foil and box, near the gap, Fig.4. The return path for current is provided by the capacitance between the base of the receiver and the foil. In general, however, inductive coupling is better, if only because it dispenses with any mechanical connexion between receiver and loop. The user is then free to remove the set from the box when it is needed elsewhere for local station reception. If the receiver is provided with aerial and earth terminals, signal can be supplied to these by a small secondary loop inside the box loop. The number of turns is best found by trial, but an arrangement likely to work is to wrap two or three turns

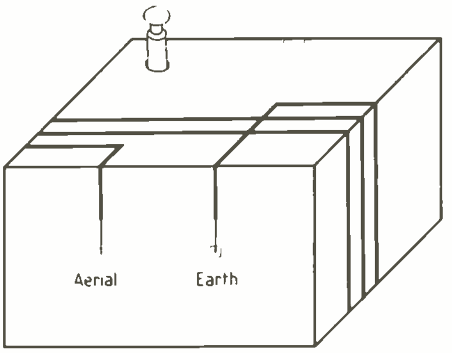


Fig.5.

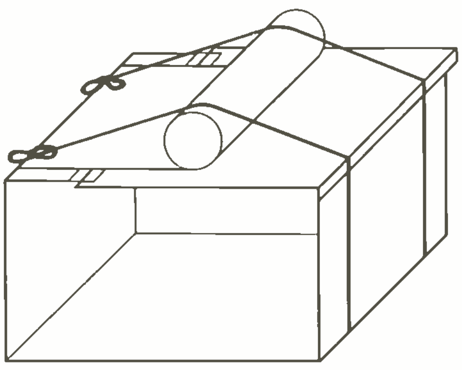


Fig.6.

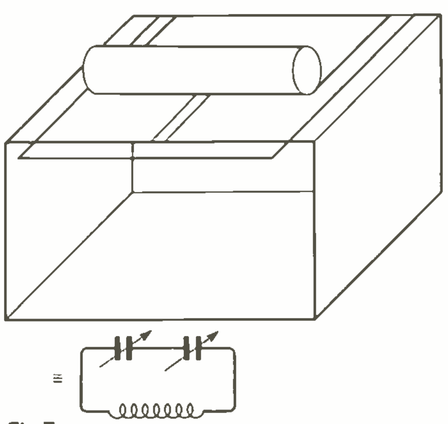


Fig.7.

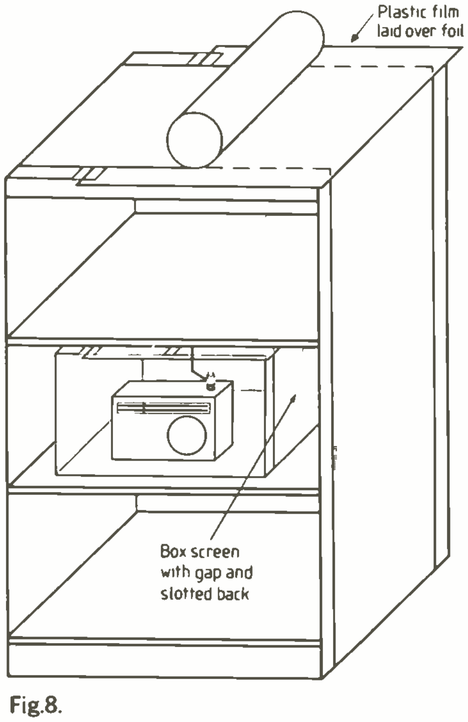


Fig.8.

round the receiver cabinet, Fig.5. A short ferrite rod of medium wave grade may also be used to carry a secondary loop of a few turns. If there are no aerial terminals, one end of a secondary loop can be coupled capacitively to the whip, as above. The other end is connected to a pad of foil which is fixed to the cabinet at a strategic point such as over the battery compartment. If necessary this pad can be slotted to reduce damping.

DIRECTIVITY

Laboratory measurements of the null depth give values in excess of 40dB. This suggests that a box-loop should enable some listeners to reduce interference by local stations to tolerable levels. Loops are, however, of limited effectiveness when the interference comes from a distant transmitter. In this case, the ionosphere is likely to distort the polarization of the wave and produce variations in its apparent direction of origin. This reduces null depth. Even when interference takes the form of the ground wave from a local transmitter some wavefront distortion is likely, as the wave is reflected from metal pipes, rods and wiring inside the house. In this case it may, however, be possible to find an aerial position where such effects are small.

BOX AERIAL CONSTRUCTION

It is important to use a large box, at least 50cm square. Smaller boxes may not pick up enough signal, especially at the lower frequencies. A deep box gives better screening than a shallow one.

In general, the plastics film used as the dielectric for the makeshift tuning capacitor should be as thin as possible, to enable the lower frequencies to be tuned. At the h.f. end, tuning becomes rather fierce. To ease this problem extra thicknesses of film can be inserted to taper the tuning law. In practice it is possible to achieve frequency ratios of three or more. It helps to weight the top foil so that it presses down on the dielectric. One way of doing this is to lay a strip of heavy cloth or some sheets of newspaper over the foil. This is rolled and unrolled with the foil itself. Another useful ploy is to tie strings round the box to hold steady the roll Fig.6. If only high-frequency coverage is needed, the symmetrical arrangement shown in Fig.7 can be used. This has two capacitors in series. The rolling foil may be tapered to improve the ease of tuning at the h.f. end.

If the nulling property of the loop is not required it may be advantageous to install a large fixed loop. To avoid the need for a huge box the loop proper can take the form of a band of foil run round a bookcase or some other convenient object. The receiver, housed in a small untuned box screen, Fig.8, can be coupled to the main loop by means of a small secondary loop, as described.

References

1. Schemel, R.E. The loop aerial revived. *Wireless World* July 1979 p.48.
2. Mukherjie, S. Indoor loop aerial for short waves. *Wireless World* April 1985 p.38.
3. Wareham, G. Short-wave loop aerial. *Electronics & Wireless World* February 1986 p.41.
Jones, R. Indoor Loop Aerial (letter) *Ibid* p.42.

BOOKS

Landmobile and Marine Radio Technical Handbook by Edward M. Noll. Howard W. Sams & Co., 576 pages 183×247mm, soft covers; available in the UK from Pitman Publishing at £20.95. Well-illustrated manual for the technician, covering basic radio and electronics as well as more practical information. Unfortunately, much of the latter is based on US conditions and so lacks relevance to the UK scene.

1987 D.A.T.A. Book: PC Board Connectors, edition 1, D.A.T.A. Inc., 1112 pages approx. A4, soft covers; available in the UK at £105 (two editions) from H.T.I. Ltd, 16–20 Victoria Road, Romford, Essex RM1 2JH, tel. 0708-46447. Comprehensive reference work indexing 5473 types from 100 manufacturers. This volume is one of an extensive series of directories covering electronic components of all types. Many directories are available on disc for use with hard-disc versions of the IBM PC-XT/AT or compatibles, or on computer tapes.

Electronics and Waveguides, Dictionary No. E.O.3. Schnellmann-Verlag (Widnau, Switzerland), 120 pages 150×200mm, paper covers; price £16.50 in the UK. English-German (and vice versa) dictionary for the engineer, giving equivalents of some 2500 technical terms and phrases including some highly specialized ones. Other volumes in this series cover computers, electrical technology, industrial and laboratory chemistry, machinery, construction engineering and plastics. Languages represented are Dutch, French, German and Spanish. The publisher's distributors for English-speaking countries are Grant & Butler Ltd, 55–57 Great Marlborough Street, London W1V 1AY, whose catalogue, including over 50 pages on specialist dictionaries, is free on request.

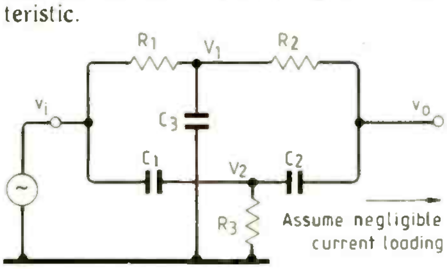
Hy-Q Handbook of Quartz Crystal Devices by David Salt, group engineering manager of Hy-Q International Ltd. Van Nostrand Reinhold (UK), 229 pages, hard covers, £30. Comprehensive guide for the design engineer to a little-understood component which has nevertheless grown greatly in importance. Sections deal with the crystal itself and the various types of resonators, manufacturing processes, circuit characteristics of crystals and design of oscillators and filters. Treatment of the subject is fairly mathematical; circuits given are design illustrations rather than worked examples. The author tackles crystal physics in greater detail in a series of six appendices. Though the book carries a prominent crystal manufacturer's name, commercial pressures penetrate it no further than the cover.

General analysis of twin-T filter – and some bandpass filter theorems

Whilst formulas for the twin-T filter are well documented for the symmetrical case, analysis of the general case isn't.

P. J. RATCLIFFE

The twin-T circuit realized using RC components can have frequency selective characteristics such that in its normal connection it is a notch filter. Alternatively, because the network has only three terminals to its external environment (v_i, v_o and earth which is common to both input and output circuits), then the common earth and v_i can be interchanged to give the complementary bandpass characteristic.



From an analysis of the currents in the branches meeting at the intermediate nodal voltages v_1, v_2, above, and assuming negligible loading current, the relation between v_i and v_o takes the form

$$(a+jb)v_i = v_o(c+jd) \qquad (1)$$

which can be further simplified by noting similarities between the expressions for the real and imaginary parts and writing $c=a+a'$, $d=b+b'$, where

$$a = 1-\omega^2C_1C_2(R_1+R_2)R_3$$

$$a' = -\omega^2C_3R_1R_3\left[C_1+C_2\left(1+\frac{R_2}{R_3}\right)\right]$$

$$b = \omega R_3(C_1+C_2-\omega^2C_1C_2C_3R_1R_2)$$

$$b' = \omega R_1\left[C_2\left(1+\frac{R_2}{R_1}\right)+C_3\right] \qquad (2)$$

There is a unique null in v_o for the simultaneous zeros $a=b=0$. The imaginary part, b, is zero for a frequency

$$\omega_0^2 = \frac{1}{C_3R_1R_2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right) \qquad (3)$$

which is independent of R_3. The real part, a, can be made equal to zero simultaneously at this frequency by suitable choice of component values, where the exact null condition between the component values is

$$\frac{C_3}{R_3} = (C_1+C_2)\left(\frac{1}{R_1}+\frac{1}{R_2}\right) \qquad (4)$$

in which the components on the left-hand side of the equation are in the vertical arms and on the r.h.s. in the horizontal arms of the circuit as shown.

To show these last two equations, determine the notch frequency by the values of C_1, C_2, C_3, R_1, R_2 as in equation 3, then calculate the value of R_3 for an exact null in the notch amplitude using equation 4.

Finally, the complex attenuation factor v_o/v_i can be neatly expressed using the null conditions to simplify a and b in (1), so that

$$a = 1-(\omega/\omega_0)^2$$

$$b = \omega(C_1+C_2)R_3[1-(\omega/\omega_0)^2].$$

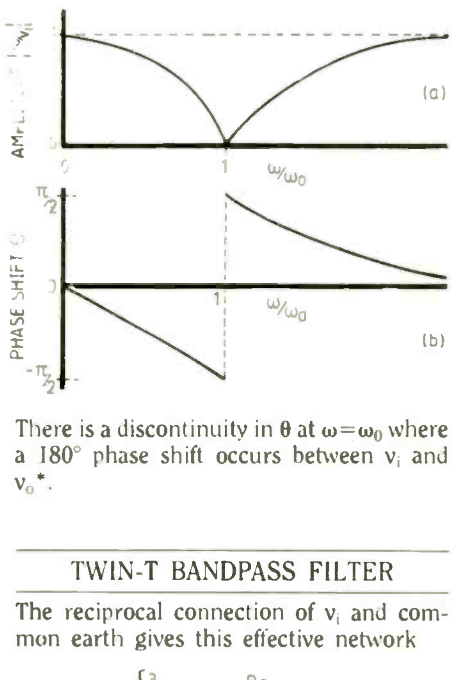
The complex attenuation factor can be written as

$$\frac{v_o}{v_i} = \left[1+\frac{j\omega_0R_1\left[C_2\left(1+\frac{R_2}{R_1}\right)+C_3\right]}{\frac{\omega_0}{\omega}-\frac{\omega}{\omega_0}}\right]^{-1} \qquad (5)$$

assuming that the null condition for the component values is satisfied so that certain terms have simplified out to be zero. From equation 5 the phase shift in v_o/v_i can be written down by inspection as

$$\tan\theta = \frac{-\omega_0R_1\left[C_2\left(1+\frac{R_2}{R_1}\right)+C_3\right]}{\frac{\omega_0}{\omega}-\frac{\omega}{\omega_0}} \qquad (6)$$

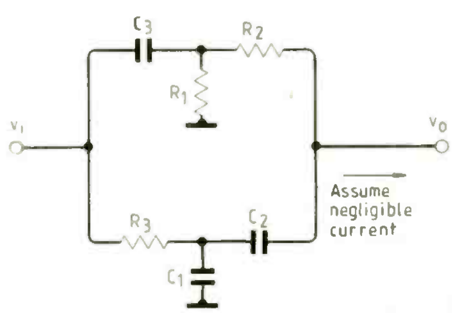
which gives $\theta=\pi/2$ at $\omega=\omega_0$. The characteristic curves for the amplitude $|v_o/v_i|$ and phase shift θ for the exactly balanced notch are of this general form:



There is a discontinuity in θ at $\omega=\omega_0$ where a 180° phase shift occurs between v_i and v_o*.

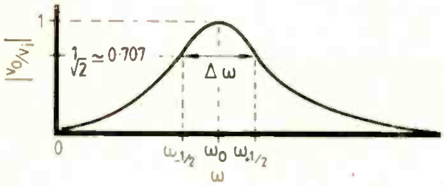
TWIN-T BANDPASS FILTER

The reciprocal connection of v_i and common earth gives this effective network



* This analysis obviously assumes normal a.c. network theory for sinusoidal currents of frequency ω attaining an assymptotic equilibrium of interactions in the network.

This frequency-selective network can be seen as a combination of two complementary phase-shifting potential dividers based upon R and C components respectively. It has a bandpass characteristic that is the reciprocal of the notch shown on the previous page.



The maximum value must be unity, since the notch is zero, assuming negligible loading at the output which would otherwise complicate the interaction of the currents in the network at $\omega=\omega_0$.

The frequency selectivity or Q factor is defined as the ratio of the centre frequency to the bandwidth between the frequencies at the half-power points ($\omega_{\pm 1/2}$)

$$Q = \frac{\omega_0}{\Delta\omega}.$$

The criterion for the half-power frequencies in terms of voltage is

$$\left|\frac{v_o(\omega_{\pm 1/2})}{v_i}\right| = \frac{1}{\sqrt{2}}\left|\frac{v_{o\ max}}{v_i}\right|$$

which also corresponds with the condition that the real part equals the magnitude of the imaginary part in the complex attenuation factor, because the reciprocal attenuation can be written in the form

$$\frac{v_i}{v_0} = a+jb(\omega)$$

where a, b are constants (not arbitrary local variables as before), where a is independent of ω. The proof of this theorem for the half-power frequencies is given in the appendix. Since v_o/v_i can be written in two complex forms

$$\frac{v_i}{v_o} = \frac{1}{a+jb} = \frac{a-jb}{a^2+b^2}$$

real and imaginary parts can be equated in two ways, a=b or a=b that is referring to equation 5 for the values of

$$\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} = \pm\omega_0 R_1[C_2\left(1+\frac{R_2}{R_1}\right)+C_3].$$

This gives a quadratic equation in ω for the two solutions of the half-power points

$$\omega_{\pm 1/2} = \pm \tfrac{1}{2}\omega_0^2 R_1[C_2\left(1+\frac{R_2}{R_1}\right)+C_3] \pm \tfrac{1}{2}\sqrt{\left\{\omega_0^2 R_1(C_2\left(1+\frac{R_2}{R_1}\right)+C_3\right\}^2+4\omega_0^2}$$

where, since the root term is always greater than or equal to the 1st term, we ignore the negative root because negative $\omega_{-1/2}$ is meaningless. Thus the (realistic) solution for the two half-power frequencies is of the form

$$\omega_{\pm 1/2} = \pm A+\sqrt{B}$$

so the bandwidth is

$$\Delta\omega = +A+\sqrt{B}-(-A+\sqrt{B})$$

$$2A = \omega_0^2 R_1[C_2\left(1+\frac{R_2}{R_1}\right)+C_3].$$

and the quality factor or Q can be written in terms of dimensionless ratios of the component values as

$$Q = \frac{1}{1+\frac{R_2}{R_1}+\frac{C_3}{C_2}}\sqrt{\frac{R_2}{R_1}\cdot\frac{C_3}{C_2}\cdot\frac{1}{1+\frac{C_2}{C_3}}} \qquad (7)$$

This has a maximum attainable value of ½ corresponding to infinite attenuation in the ratio $R_2/R_1\rightarrow\infty$, $C_3/C_2\rightarrow\infty$, and $C_1/C_2\rightarrow\infty$.

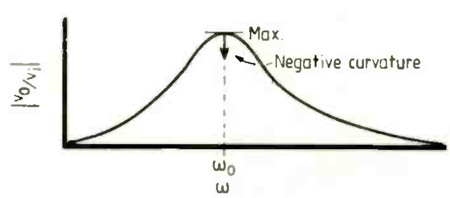
APPENDIX

General theorems for bandpass filters

Suppose that the complex attenuation factor for a bandpass filter can be expressed in the form

$$\frac{v_o(\omega)}{v_i} = A(\omega)+jB(\omega) \qquad (A1)$$

and the amplitude has a graph with a maximum at some frequency $\omega=\omega_0$.



To prove the following theorems we use a lemma (unproven) that the reciprocal of the complex attenuation can be written in the form

$$\frac{v_i}{v_o} = a+jb(\omega) \qquad (A2)$$

where the real part, a, is independent of ω. The lemma (A2) where a is independent of ω is unproved but supported by all empirical data. The reciprocal graph of the amplitude-frequency characteristic will have a corresponding minimum at $\omega=\omega_o$ with positive curvature. Then in terms of a, b the complex attenuation factor in (1) can be written

$$\frac{v_o}{v_i} = \frac{1}{a+jb(\omega)} = \frac{a-jb(\omega)}{a^2+b^2(\omega)}$$

which is of the form of equation with

$$A(\omega) = \frac{a}{a^2+b^2(\omega)} \text{ and } B(\omega) = \frac{-b(\omega)}{a^2+b^2(\omega)}.$$

Theorem 1. Prove that maximum $|v_o/v_i|$ corresponds to zero imaginary part.

Proof. Using the above lemma in supposing that the real part is independent of ω, write the reciprocal amplitude as

$$\left|\frac{v_i}{v_o}\right| = \sqrt{a^2+b^2(\omega)}.$$

This has a minimum when

$$\frac{\partial}{\partial\omega}\left|\frac{v_i}{v_o}\right| = 0 \text{ and } \frac{\partial^2}{\partial\omega^2}\left|\frac{v_i}{v_o}\right| > 0$$

so evaluating these derivatives

$$\frac{\partial}{\partial\omega}\left|\frac{v_i}{v_o}\right| = \frac{\partial(\omega)}{\sqrt{a^2+b^2(\omega)}}\cdot\frac{\partial b(\omega)}{\partial\omega}$$

which is indeed zero at $\omega=\omega_o$ if $b(\omega_o)=0$, and the non-zero terms (for $b(\omega_o)=0$) remaining in the second derivative are

$$\frac{\partial^2}{\partial\omega^2}\left|\frac{v_i}{v_o}\right| = \frac{1}{\sqrt{a^2+b^2(\omega)}}\left(\frac{\partial}{\partial\omega}b(\omega)\right)^2 \geqslant 0$$

which is positive for a minimum at ω_o.

Conversely, the maximum in v_o/v_i corresponds with zero imaginary part, with value

$$\left|\frac{v_{o\ max}}{v_i}\right| = \frac{1}{|a|} \qquad (A3)$$

so the theorem is proved provided that the lemma is true.

Theorem 2. Prove that the frequencies for the half-power points correspond when Re part=Im part of the complex attenuation factor.

Proof. The criterion for the frequencies at half power is

$$\left|\frac{v_o\ (\omega_{\pm 1/2})}{v_i}\right| = \frac{1}{\sqrt{2}}\left|\frac{v_{o\ max}}{v_i}\right| \qquad (A4)$$

and provided that v_o/v_i can be written in the form $1/a+jb(\omega)$ then

$$\frac{1}{\sqrt{a^2+b^2(\omega_{\pm 1/2})}} = \frac{1}{\sqrt{2}}\cdot\frac{1}{|a|}$$

where, by the lemma, a is independent of ω on both sides of the equation

$$a^2+b^2(\omega_{\pm 1/2}) = 2a^2$$

$$\text{or } a = \pm b(\omega_{\pm 1/2}). \qquad (A5)$$

Thus the theorem is proved. Instead of calculating $\omega_{\pm 1/2}$ longhand from the original definition (4), we use this theorem conversely, by equating the real and imaginary parts as in (5) to get a quadratic equation for the two solutions for the half-power points $\omega_{\pm 1/2}$, always provided that the lemma is true.

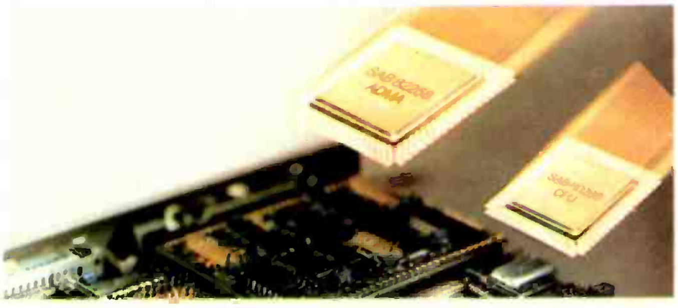
Theorem 3 (an unproven conjecture). Prove that for any passive filter using only RC components, $Q_{max} = ½$.

This theorem is borne out by an analysis of all the facts for RC bandpass filters without amplifying elements, but the intuitive proof is not rigorous enough to elevate the statement from the level of a conjecture to a proven theorem.

NEW PRODUCTS
COMPUTING

Multi-standard modem

Several integrated circuits are mounted onto a single 50-pin dual-in-line package by Texas Instruments to provide a complete modem circuit. MOD3110 is a multi-standard model which meets the requirements of CCITT V22BIS/V22/V21 and Bell 212A/103 standards. It needs only a simple interface for connection to telephone lines, and can be used with automatic dialling (pulse or tone) and automatic answering. The model includes test facilities such as analogue loop-back as required by the standard specifications. The information we have received is in advance of the device becoming available but samples should be arriving between July and September. Further details from Online Distribution Ltd, Melbourne House, Kingsway, Bedford MK42 9AZ. Tel: 0234 217915.



16-bit d.m.a. controller

Designed especially for use with 16-bit processors like the 80286, 8086/88/186/188, the SAB82258 from Siemens has four direct memory-access channels. It can transfer data at up to 8Mbyte/s at 8MHz in a 286 system or 4Mbyte/s at 8MHz in a 8086/186 system. Such a bandwidth enables fast data transfer or the use of a number of peripheral devices at the same time in parallel.

The controller works with all five of the Seimen's 16-bit processors without extra support or interface logic because it has an adaptive bus interface to handle the different signals, functions and timings.

It is configured by software to work with the 8-bit buses of 8088 and 80188 processors. Available through RR Electronics Ltd, St Martins Way, Cambridge Road, Bedford MK42 0LF. Tel: 0234 47211.

Analogue circuit simulator

Linear circuits may be modelled on Miteyspice, an addition to Micro-spice, the in-circuit emulator that runs on the BBC computer. It features a.c. and d.c. analysis, 20-parameter transistor modelling, and component value sweeps.

Non-linear components can be first handled by the d.c. analysis that will establish the operating point for the a.c. program. Thus circuits with non-linear behaviour can be modelled and modifications made by use of the editor program. The results can be viewed graphically on the screen through a post-processor program which incorporates an advanced scaling algorithm. The makers claim that this is particularly useful in filter design. Those Engineers Ltd, 106a Fortune Green Road, London NW6 1DW. Tel: 01-435 2771.

FORTH CORNER · FORTH CORNER · FORTH CORNER

High-level language processor

Readers interested in the articles on the Novix Forth processor (page 00) might like to know about the Metaforth MF1600VME processor which also executes high-level Forth instructions directly. It does this through a processor board which has no single-chip microprocessor; the board itself functions as a distributed processor based on programmable array logic devices. Running at 20MHz, it can execute 6.6 million high-level instructions per second. Over 200 instructions are acted upon and it is possible for the user to add microcoded instructions to further accelerate the timing of programs without the need to rewrite software.

The board can be coupled to a VMEbus board and can offer all the VME facilities, including access to mass memory storage and master/slave arbitration, eight levels of interrupt priority, and communications protocols. A watchdog circuit will isolate the processor from the VMEbus if the application software does not signal its status every 250ms.

The processor board can run completely independently of the VMEbus and includes onboard stack memory, 512K system initialization rom, 128K static ram and sockets for two 28-pin eproms. The real-time clock/timer has a four-year calendar and a resolution of 1ms. Two RS232C serial ports are provided. A completely self-contained unit with disc drives and an eprom programmer is optionally available.

Program development is performed on the board which will run it and thus save considerably in time and cost. Metasys is a full operating system that includes keyboard decoding, integer and fixed-point arithmetic, i/o handling, and a complete operating environment for multitasking and multiprocessing applications. It is provided in software and designed to be resident on the board in eproms. There are also a number of disc-based tools including a screen editor, program compiler, trace and debug utility and an applications profiler that enables the identification of the instructions needed to be designed as microcodes. All these are provided with the system. Optional extras are floating-point arithmetic and Pascal or C compilers. Advanced Processor Design, Newlands High Technology Centre, Inglemire Lane, Hull HU6 7TQ. Tel: 0482 855927.

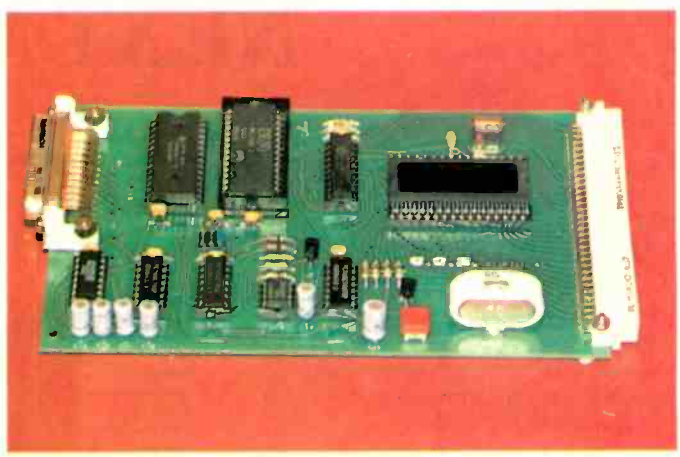
Forth control manual – free

A technical manual describes applications for the Forth control cards from Triangle Digital Services. It describes the use of Forth and multi-tasking, including the use of interrupts in assembler code and in Forth. There are Forth listings of such applications as an l.c.d. driver, a software wart and an interface to serial eeproms.

The manual is free to those who send a blank formatted disc for an IBM PC or compatible. The printed version has some additional application circuit diagrams and photographs and costs £8 (or £10 for a company purchase order).

The TDS900 is a set of p.c.bs for use in test equipment, data collection, and control systems. Versions with additional screen memory are available as development systems for use with a number of personal computers including IBM, BBC and v.d.u. terminals. Each uses Forth and is suitable for building into equipment as an embedded controller or computer.

Triangle Digital Services Ltd, 100A Wood Street, London E17 3HX. Tel: 01-520 0442.



Forth single-board computer

Forty input/output lines gives this single-board computer its name Forth-40. Developed in Warwickshire by Central Control Systems, the board is intended to reduce costs and development time in control, instrumentation and laboratory testing applications. A Forth kernel is held permanently on board and allows programs to be developed using Forth or assembly-code. The 40 lines reduce the need for additional support circuitry and the board acts as its own eprom programmer.

Rom-based software allows the board to be used with a BBC for screen editing, terminal emulation and disc storage. Other computers or terminals can be used in conjunction with the board's battery-backed memory. The board is based around a 2MHz c-mos 6502. It has two counter/timers, and RS232 interface and can be run automatically at switch-on. Central Control Systems Ltd, 42 Woodlands Road, Kenilworth, Warwicks CV8 2FL. Tel: 0926 50732.

High-speed, high-resolution d.s.o.

The use of their own emitter-coupled logic i.c.s has enabled Philips to produce a digital storage oscilloscope (PM3320) with a host of new features. 12-bit a-to-d converters are used to guarantee 10-bit accuracy: claimed to be four times better than rival products. The maximum sampling rate is 250M samples/s (i.e. a minimum sample period of 4ns). The bandwidth of 200MHz allows fast signals to be recorded accurately.

The d.c. offset range means that minor fluctuations on any signal up to 300V can be examined: for instance, with the attenuation set at 50mV/division, distortion as little as 10mV can be picked up on a 50V signal.

The 3320's restart facility enables the user to pick out part of any signal for expansion on the screen, marking the limits with cursors. Independent x and y positioning is possible because the vertical and horizontal components of any signal are stored separately. Comprehensive settings and test sequences to a maximum of 77 steps/set-ups can be stored in memory and recalled by softkey operation. Like other Philips instruments, the oscilloscope is provided with a 'green button', the operation of which will automatically trace the signal and set the instrument to give an optimum display. The instrument has been designed to be easy to use with menus displayed on the screen, outside the signal display area. Cursor measurements are displayed at the top of the screen. An optional interface board provides GPIB and RS232C interfaces with a direct drive to a plotter. Philips Test and Measurement, Pye Unicam Ltd, York Street, Cambridge CB1 2PX. Tel: 0223 358866.

Data recorder with digital filters

A tape recorder for data acquisition is claimed to be the first in the world to use digital anti-aliasing filters. Known as the EDR 8000, it offers high accuracy and resolution, together with a dynamic range 100 times better than conventional analogue tape recorders. The EDR instrument is capable of recording and replaying up to eight analogue input signals. With digital anti-aliasing filters, the EDR 8000 can operate at varying bandwidths and numbers of channels without the need for expensive and cumbersome analogue filters.

The bandwidth available depends on the number of channels selected, up to a maximum of one channel at 2048Hz or eight at 256Hz. Unlike conventional recorders, EDR 8000 gives an increase in the recording time as the selected number of channels decreases. The dynamic range of 96dB covers all the input ranges of traditional recorders without the need for adjusting. During recording, the gain information is embedded within the data sample so that when a tape is replayed the original signal level can be recovered. The instrument is fitted with RS232 and IEEE488 interfaces, allowing full remote control and downloading of data to a computer. It also has a time search facility and automatic time, date and status recording. Earth Data Ltd, Nutsey Lane, Totton, Southampton SO4 3NB. Tel: 0703 869922.

NEXT MONTH

Low noise oscillator design builds on previous articles to explain how practical proglems are tackled when designing v.h.f. voltage-controlled oscillators for low phase noise.

Real time colour palette is an upgrade to the video frame store, described in the series that finished last March, and enables moving television pictures to be colourized in real time.

Mobile radio developments – a report on the annual conference of the Mobile Radio Users' Association, where this year's hot topic was the DTI's newly published report on privatizing the airwaves.

Pioneers. Next in our gallery of pioneers of electrical communications is Alexander Graham Bell, father of the telephone.

Minimal eprom programmer – creating software routines for the programmer described in June's issue. Special protocols allow software in the host to take over all the tasks involved in reading or writing eproms.

Cache memory. As many programs spend much execution time in a few tight loops, the cache offers a means of accessing these loops faster, after the first time round, thus avoiding repetitively accessing slower peripherals.

Vector theory. With the aim of calming troubled waters, 'Joules Watt' brings his professorial talents to bear on displacement current and Maxwell's equations, at the same time removing the mystery from divs, curls and grads for those who missed out on vector theory.

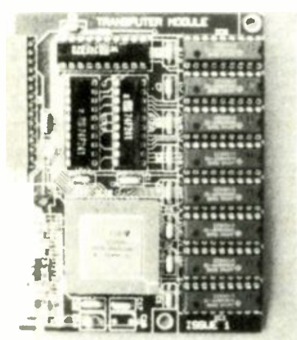
NEW PRODUCTS
COMPUTING

Computer aid to computer-aids

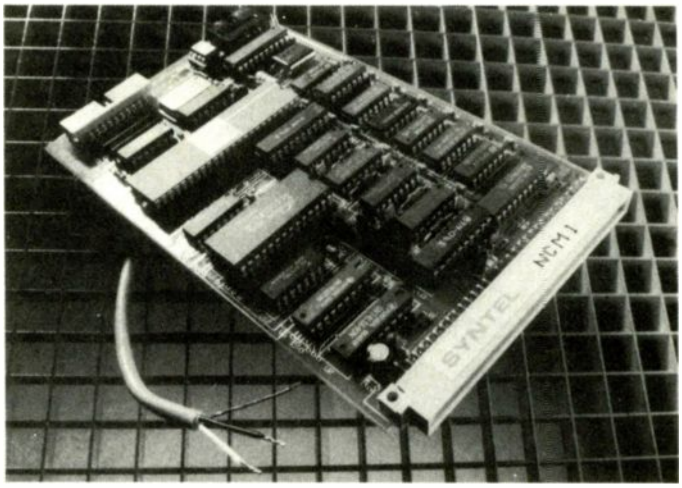
A disc-based database system has been developed to list software, systems and suppliers of computer-aided design, engineering and manufacturing applications. Hunter, as it is called, runs on an IBM PC or near compatible and requires a hard disc, though it is supplied on a number of floppies. The system is available as a single issue or on a subscription basis with regular updates. The initial version contained 500 suppliers of 2000 products and is continually updated. The user can search by keywords and wild cards and there is a useful 'help' system. When an application, a supplier and a system are matched, the system can automatically print a letter asking for further details. Further details of Hunter can be obtained from Cad Source Ltd, Shadwell House, 65 Lower Green Road, Rusthall, Tunbridge Wells, Kent TN4 8TR. Tel: 0892 26476.

Transputer board

An evaluation system has been designed to allow manufacturers and education the chance to use the Inmos T414 transputer for a relatively small outlay. Concurrent Technology's TM1 is a four-layer



p.c.b. on which are mounted a transputer and 256K of high-speed dram. The module mounts on a suitable interface board through a 15-way female connector. A PC interface card will be available soon, as well as a resident assembler. As it stands, the card can operate at up to 7.5mips. However if eight of them are used in parallel, mounted on a single eurocard with support circuitry, they can provide 60mips on a system that can be held in one hand! The board can be fitted with the faster (10mips) T414-20, or the new T800. The latter with on-chip maths co-processor can operate at up to 2.25M floating-point operations/s (Mflops). The board cost £600 for one-off and reduces to £475 each for six or more. Concurrent Technology, 30 Baldslow Road, Hastings, E. Sussex TN34 2EY. Tel: 0424 714790.



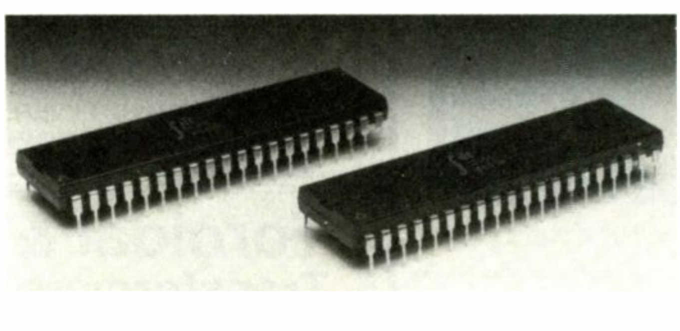
Low-cost computer network

A local-area networking system needs only a two-wire link to provide interconnection to instruments and control applications on the G64 bus.

Sycom uses a multi-drop topology and token-passing protocols. Additional stations can be added to the network through a simple 'T' connector, up to a total of 254 nodes. The transmission rate is 1Mbit/s. The hardware is a single G64 bus Eurocard incorporating a Manchester encoded RS422 interface. Software includes a message delivery service and an OS9 operating system file structure for the communication of management information and other signals between systems. Interfaces for the VME and IBM PC buses are being developed which will allow the network to communicate between systems operating different buses. Syntel Microsystems, Queens Mill Road, Huddersfield, HD1 3PG. Tel: 0484 35101.

CD sound on CD rom

A 'second generation' CD rom optical disc drive has been produced by Hitachi. It is physically smaller than previous models and yet provides more facilities: it offers stereo sound output for combined audio and data output. The two audio channels can also be used for bilingual versions of a presentation. Up to four of the drives can be daisy-chained together to provide a total capacity of 2.2Gbyte. The drives interface through an IBM PC bus or small computer system interface (SCSI) and interface boards are provided with the drives. Hitachi, Hitachi House, Station Road, Hayes, Middlesex UB3 4DR. Tel: 01-848 8787.



Serial and parallel fifo

Two first-in-first-out memory chips are claimed to be the first to offer both serial and parallel operation. The IDT72103 is configured as 2048 by 9-bits while the IDT72104 is organized as 4096 by 9-bits. IDT's Flexishift system allows the user to program word lengths from four bits to any bit width for serial operations without using additional components and still maintaining a high bandwidth. The system lets users run a serial bit stream for any application at 40MHz. The four-port devices feature 50ns parallel port access time and a serial input/output port frequency of 40MHz. The ports permit serial-to-serial and parallel-to-parallel operations. The fifos can expand in depth or width for any mode. Integrated Device Technology, Europe, 5 Bridge Street, Leatherhead, Surrey KT22 8BL. Tel: 0372 377375.

Write-once optical disc memory

Up to 230Mbytes can be stored on a single 5.25in optical disc in a PC-compatible disc drive. It offers an alternative to CD-roms, hard magnetic disc drives and microfiche for archival storage. The drive can be easily installed on a PC and uses Corporate Retriever software, previously available for hard discs. The retrieval system relies on keywords to build up a reference index which provides access to the stored data. It is possible to use the built-in thesaurus to search for keywords and even find words that sound like the required word. The disc cartridge is guaranteed for ten

years against data loss, and the system is claimed to be of lower cost than a hard disc drive. Computer and Aerospace Components Ltd, Fullers Way South, Chessington, Surrey KT9 1HW. Tel: 01-397 5311.

Fortran on a PC

Quin Systems describes their board as a 'high-level language processing engine'. It incorporates a standard Fortran 77 compiler, 680X0 processor, floating point maths chip (optional) and memory, and gives an ordinary PC a floating point maths processing capability approaching that of a DEC VAX 8600.

The main applications for the Fortran processing engine are expected to be in maths intensive engineering and scientific roles. There are five products in the Quin Systems Fortran/LE family, offering a choice of 680X0 chips and clock speeds from 10 to 16MHz. Each board has a processor, 1Mbyte of memory, PC DOS68 system kernel, Absoft Fortran 77 compiler, symbolic Fortran program debugger, Fortran module linker and subprogram profiler.

Main options are up to 4Mbytes of additional memory, and a floating point maths processor with Fortran support library. The board is designed for user installation – it simply plugs into one of the available slots in an IBM PC or compatible. Quin Systems Limited, 35 Broad Street, Wokingham, Berkshire RG11 1AU. Tel: 0734 783114.

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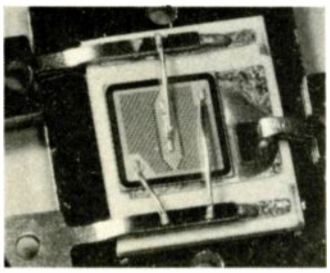
NEW PRODUCTS

Thyristor with built-in protection

A seris of 120A gate turn-off thyristors from Mullard features an anti-parallel diode integrated onto the chip. The BTV60D series is meant for use in high-frequency inverters, power supplies, and in p.w.m. a.c. motor control applications. The devices can switch off a 120A anode current in less than 300ns. Three types offer repetitive peak off-state voltages of 850, 1000 or 1200V. The peak on-state current can go up to 240A, with an average value of up to 25A. Mullard Ltd, Mullard House, Torrington Place, London WC1E 7HD. Tel: 01-580 6633.



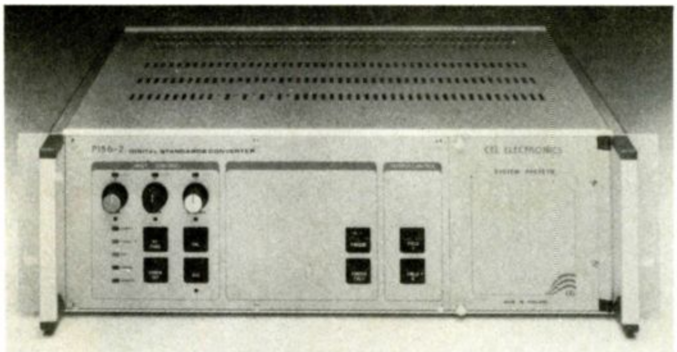
Computer-aided p.c.b. design

Printed circuit boards may be designed, with the artwork printed out on a standard dot-matrix printer, by using Channel Micro's PCB Utility software on a BBC Master Turbo or model B (with second 6502 processor).

The system offer three interlinked programs: a drafting program, one for editing a design, and the third for driving a printer. It is compatible with the Micronova system (by the same author) but offers much higher screen re-draw speed and more facilities such as selectable pad sizes and line thickness, and automatically places d.i.l. or s.i.l. pads. It copes with double-sided p.c.b.s and displays both sides on a coloured monitor in different colours. It is easy to switch between sides and work on either at will. Although the system does not provide auto-routing, it can repeat lines for similar dual-in-line buses.

The editor program enables the contents of a screen box to be deleted, moved, rotated or reflected or even changed to the other side of the board. The box may be saved as a named file separately from the whole design.

The maximum board size can be over 600mm square and the printout can be 1:1 for reference, 2:1 or 4:1 for direct photo-reduction. Printouts can be mirror imaged and solder mask patterns can be produced automatically if required. Plotter drivers for most plotters are also available. Channel Micro Products Ltd, 227 Canterbury Street, Gillingham, Kent ME7 5XB.



Digital tv standards converter

Designed as a self-contained unit, the P156-2 from CEL employs two standards decoders for PAL to Secam or NTSC 3.58 to NTSC 4.43. They may be selected manually or automatically and allow conversion from 625 to 525 lines and vice versa. A transversal filter optimizes the luminance response, and a spatial two-line interpolator corrects the geometry of picture sizes. The converter is aimed at commercial and industrial, educational and corporate video applications and can also operate as a back-up unit for broadcasters. CEL Electronics Ltd, Chroma House, Shire Hill, Saffron Walden, Essex CB11 3AQ. Tel: 0799 23817.

Data communications transceivers

Claimed to be the first devices to comply with EIA standards RS422 (balanced line) and RS423 (unbalanced line), the Motorola MC34050/51 series of bipolar dual data standard transceivers are now available from ITT Multicomponents. The devices have a maximum enable input voltage of 5.5V d.c., a maximum power supply of 7V d.c., and an input common mode voltage (receivers) of ±25V d.c. The typical data input transition time is 50ns, and the maximum propagation delay (data input to output high to low) is 20ns.

Features include 3-state outputs, single +5V operation and short circuit protection. The MC34050 has a driver-enable for both drivers and a receiver-enable for both receivers; the MC34051 has a driver-enable for each driver; the receivers are permanently enabled.

ITT Multicomponents, 346 Edinburgh Avenue, Slough, Berks SL1 4TU. Tel: 0753 824212.

PWM amplifier modules parallel to 30kW output

Copley Control's book-size pulse-width modulation power amplifier modules, develop 1.1kW continuous power output and 1.6kW peak power at 75V for applications requiring precisely controllable four-quadrant energy up to 10kHz. The amplifiers may be paralleled in a master-slave configuration to deliver 30kW continuous output (450A, 75V), or 48kW (600A, 75V) short term. They are protected against overload, short-circuit and excessive temperature rise, and remain stable when driving highly capacitive or highly inductive loads. Based on mosfet bridge output circuits, as described in April's article, the Model 220-10 amplifiers dissipate only 84 watts at full load for 92% efficiency, enabling them to replace bulky and inefficient, heat-producing linear amplifiers in many industrial uses. Typical applications occur in power function generators and ATE systems, pulsing or powering magnetic coils, variable frequency/voltage power sources and line conditioners, and for driving servo motors in 'muscular' robotics and other actuators.

The new Model 220-10 amplifiers operate at 80kHz switching frequency, claimed to be the industry's highest, to achieve 10kHz bandwidth, and less than 1% output ripple at the switching frequency. Distortion is less than 0.05% up to 700Hz, and below 2% at 10kHz. Copley Controls Corp, 375 Elliot Street, Newton, MA 02164, USA.

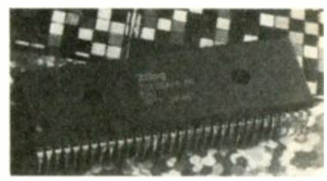
Miniature fans

These d.c. brushless fans are small enough to be easily fitted into equipment cases. Blades and bearings have been designed to offer high efficiency, low-noise and low power consumption. The use of an oil-moisture bearing material allows the fans to be mounted in any position without any increase in wear and providing a long life. RBS Components Ltd, Unit 4, Airport Trading Estate, Biggin Hill, Kent, TN16 3BW. Tel: 0959 76480.

Second source for 64180

Japan's enhanced c-mos Z80 with integrated peripherals, the Hitachi HD64180, is to be second-sourced by Zilog.

The device is completely compatible with Z80 software and includes a memory-management unit for 512Kbyte addressing, two d.m.a. channels, synchronous/asynchronous serial data channels with bit-rate generators, an interrupt controller, two timers and a wite-state generator. These peripherals are controlled using 64 i/o locations that can be moved about within a 256 byte range.



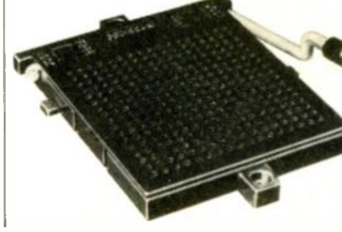
Some of the Z80 instructions require fewer machine cycles. Extra instructions allow eight-bit multiplication, data-block movement from memory to i/o ports and non-destructive data-state tests.

Using two registers for addressing, the 64180 can access 64Kbyte of i/o space (The Z80 accesses 256 bytes). Further instructions are included for more efficient addressing of the first 256 bytes. Finally there is an instruction for putting the device into its low-power mode.

Sadly the Z800 is not now likely to appear. The photograph shows a Zilog 64180 made in Japan by Hitachi but Zilog assures us that their own devices are now coming off the production line. Gothic Crellon Ltd, 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878.

Zif socket for p.g.a. testing

Low profile zero insulation force sockets are designed for burn-in testing of pin grid array devices and are available for up to 144 pins and all the standard pin matrices. The bodies are constructed from polyethersulphone (pes) which can withstand 170°C. Special pin counts can be arranged if required. Radiatron Components Ltd, Cr[illegible] Road, Twickenham, Middlesex TW1 3ET. Tel: 01-891 1221.



NEW PRODUCTS

Electrostatic tester

A hand-held electrostatic discharge simulator has been designed to test the immunity of computers and microprocessor-controlled equipment to electrostatic discharges. The MiniZap is available in two models which run on rechargeable batteries, and cost from £2500. Made by KeyTek in the US, it is available in the UK from Eaton EID, Molly Millars Lane, Wokingham, Berks RG11 2QS. Tel: 0734 794717.

High-voltage power

This power supply from Applied Kilovolts can deliver up to 3kV at 3mA d.c. with noise and ripple figures better than 10mV peak-to-peak at full output. It offers a load regulation of better than 0.1% and a line regulation of 300mV per volt change in the 24V input line. The output voltage can be controlled by the front panel multi-turn control or through an external analogue voltage allowing remote control. It is fully protected against short circuits and arcs. Applied Kilovolts, 54 Bennet Drive, Hove, E. Sussex BN3 6UQ. Tel: 0373 507973.

Processor with 128K of on-chip memory

A single-chip c-mos microcomputer has 16Kbyte of eprom and 256 byte of ram. It is thought to be of special interest to those designing industrial control systems and computer peripherals. The processor includes two timers, one of which has a 16-bit resolution and can be used to generate output waveforms. The eprom can be programmed using the same instrument as for a 27256, and can be protected against external reading. Also includes a serial communications interface with synchronous and asynchronous modes. Dot length, parity and stop-bits are all programmable. The processor runs from a standard 5V supply. The Hitachi HD63701YO is available from Impulse Electronics, Hammond House, Caterham, Surrey CR3 6XG. Tel: 0883 46433.

Digital signal kit

A design kit to exploit the functions of the TI TMS320 family of digital signal processors. Two processors are supplied the TMS32010 and 32020, together with a codec and four pre-programmed proms. Data sheets on all the devices are included along with a 735-page manual covering applications of the processors and four discs of software applications routines. The rooms contain design examples including an adaptive differential pulse-code modulator and fast Fourier transforms. Available from DC Distribution, Hitchin Road, Arlesey, Beds SG15 6SG. Tel: 0462 834444.

Direct control from a PC

A digital interface card allows any IBM-compatible computer to drive relays and solenoids directly. It has 24 opto-isolated output channels, each provided with a Darlington output which allows the direct switching of loads up to 50V at 200mA. The board is port mapped and may be controlled from any computer language. It is part of a range of plug-in cards for data acquisition and control. Blue Chip Technology Ltd, Westbury House, Earle Drive, Parkgate, South Wirral, L64 6RZ. Tel: 0244 520222.

Signal manipulation/ analysis software

Educational software for manipulating and analysing signals can be used to illustrate Fourier series, Fourier transforms convolution, sampling and discrete Fourier transforms.

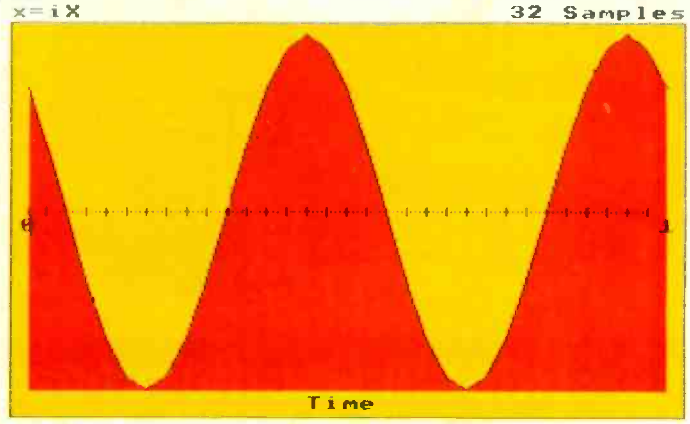
The Sigma package, for BBC computers, allows you to produce many different signals, including noise, and transforms them into the frequency domain. Complex spectra can also be transformed back into the time domain. Depending on the resolution required, more than one signal can be handled at once.

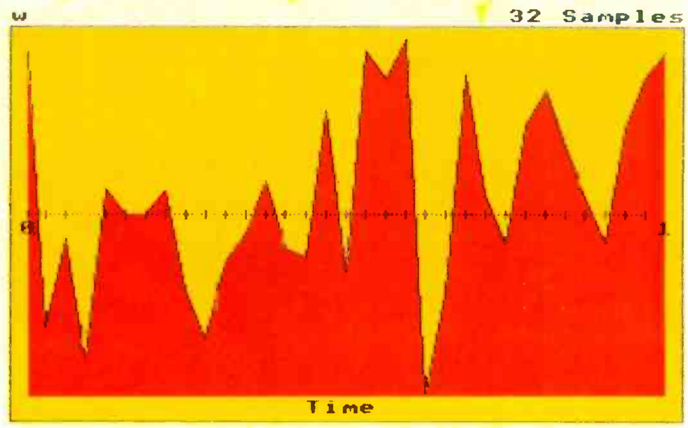
Signals and spectra are given labels reflecting widely used nomenclature: x is an input signal for example, and y is an output signal. Upper-case letters indicate frequency-domain equivalents.

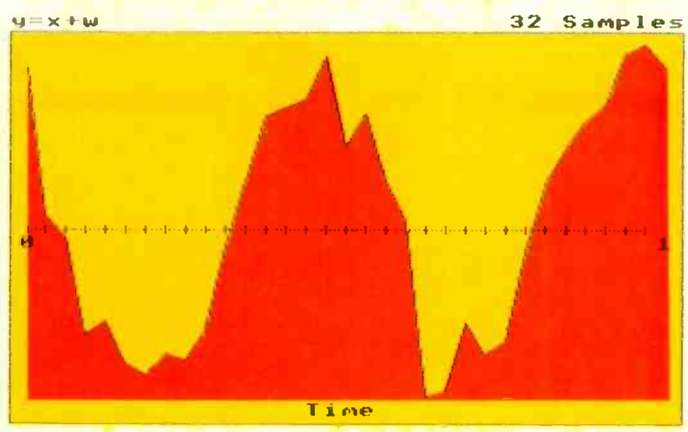
Simple algebraic expressions such as x=yx for multiplying spectra and t=x#y for time-domain convolution are used for manipulation. Standard operations include addition, multiplication and time/frequency-domain convolution. Other functions are used to obtain modulus, argument or conjugate of a spectrum.

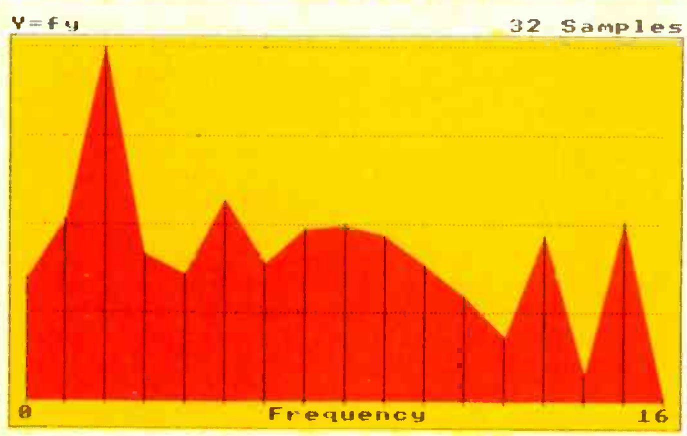
Signals can be passed through user-defined characteristics including non-linearities, difference equations and filters. Quantization and sample-and-hold effects can also be simulated.

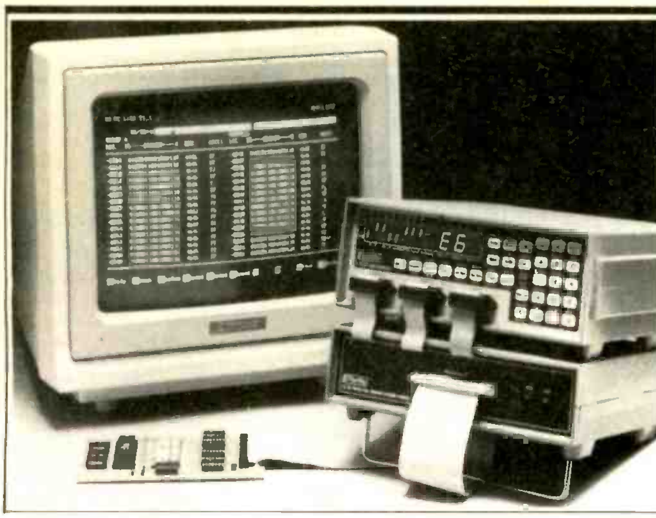
Sigma costs £190 inclusive. A related program for harmonic synthesis called Harm costs £40 or £20 when purchased with Sigma. Software is available for designing and simulating single i/o control systems and for process-control systems. Golten & Verwer Partners, 33 Moseley Road, Cheadle Hulme, Cheshire SK8 5HJ. Tel: 061 485 5435.











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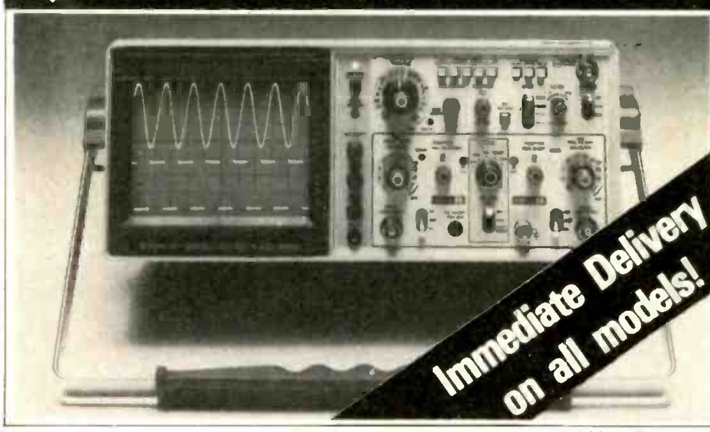

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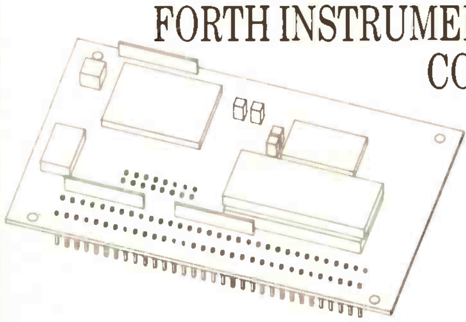

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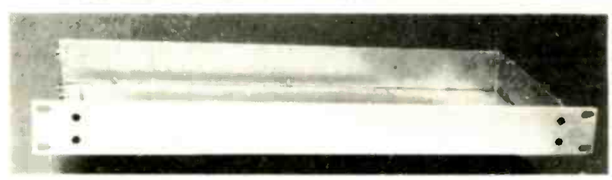

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RADIO BROADCAST

Spectrum privatization

The bulky 230-page CSP International report "Deregulation of the Radio Spectrum in the UK" (HMSO, £9.50), commissioned by the DTI at a cost of £200,000, will need and deserve very careful appraisal. For if its 17 main recommendations are ever implemented they seem bound to have a profound effect on virtually all present and future UK users of the radio spectrum. The authors of the report have avoided the pitfalls of some of the previous suggestions on selling or renting the spectrum and have recognized that the international frequency table cannot be lightly disregarded. Nevertheless, they have come up with a most radical concept in firmly believing that it is possible to quantify the "economic benefit per MHz" of spectrum usage and that it is possible to privatize spectrum management by creating a new 'Spectrum Management Licence' to be issued to 'frequency planning organisations' and 'major users' who would be largely responsible for monitoring and enforcement of their bulk allocations of spectrum which they would then parcel up and sell to anyone willing to pay the asking price. To provide a degree of competitive marketing of the spectrum it is assumed to be necessary to ensure that at least two competing FPOs were in a position to supply suitable channels to any applicant, but in effect the cost to users would be governed by market forces.

One can see that such recommendations could well find favour with a government headed by Prime Minister Thatcher, though possibly not appealing to the civil servants in DTI or the Home Office broadcasting policy unit. With much emphasis placed on the potential growth of mobile and cellular radio, cordless telephones, etc any implementation of all or part of the report is likely to be watched carefully by industry not only in the UK but also overseas – and by regulatory authorities everywhere.

For users, both actual and potential, the $64,000 question is whether a possibly less cluttered and simpler right of access to frequency channels would be more than counterbalanced by the steep rise in the price to the user that seems to be implied in the report. Although the authors point out that in the country as a whole there is not the critical shortage of spectrum space that has often been implied in the past, one could imagine the cost of clear channels in south-east England going through the roof. It is difficult to follow the reasoning whereby it is suggested that in the London area the annual economic benefit of tv broadcasting amounts to £4.3 million per MHz, amounting to £34.4 million for a single 8MHz channel, when one recalls that a year or two back Thames Television were trading at a loss on their domestic operations while using not only the Crystal Palace channel but also some 20 or so low-power relay channels. Similarly, although the report correctly gives the bandwidth of a f.m. broadcast channel as 100kHz it does not mention that the transmission actually occupies almost double that bandwidth, so inhibiting the use of adjacent channels over a wide area. The authors are not in favour of the traditional UK practice of always trying to provide the same number of national network programmes available in all geographical areas, unlike the American system where 60 radio stations may be available in New York or Los Angeles but with few fill-in relays in rural areas.

Worse h.f. crowding?

The failure of the five-week second and final session of the World Administrative Radio Conference for the planning of the broadcasting segments of the h.f. spectrum to accept the elaborate International Frequency Registration Board's computerized frequency-assignment proposals, and instead to sanction "no immediate change" in frequency scheduling procedures, may have been welcome to major h.f. broadcasters but it does mean that the bands seem likely to become even more chaotic than at present.

The IFRB proposals, aimed at satisfying as many as possible of the vast number of requirements listed by delegates (about ten times the number that could be accommodated sensibly), were deemed bound to result in an unacceptable number of daily frequency changes, with some transmitters allotted a specific channel for as little as 30 minutes, would also result in service gaps ("discontinuities") and would not guarantee a satisfactory degree of interference-free reception in the target areas.

Now the IFRB has been charged with devising a modified plan for some future, date-still-to-be-determined, h.f. planning WARC. In the meantime, frequency scheduling for most segments will continue to be left to individual countries, or cooperating groups, acting in consultation with the IFRB as at present.

To salvage something from these two large and hugely expensive ITU conferences, recommendations were approved that the next main WARC intended to redefine the entire radio spectrum for all purposes should be asked to examine the possibility of extending the allocations for h.f. broadcasting (it would almost certainly do this in any case). The conference also agreed that h.f. broadcasting should move progressively towards becoming entirely converted to the s.s.b. mode (a tentative date of 2015 is attached to this recommendation but subject to review in the light of the cost of receivers suitable for s.s.b. and with digital frequency readout). However, anyone wishing to use broadcast s.s.b. can now do so.

Some will see the conference as a victory for the 'have' nations, already occupying enough channels to provide near 24-hour, world-wide services; others may argue that it is absurd for Third World nations to seek to provide comparable external services while they still lack effective internal telecommunications. The chances are that the h.f. broadcast segments will become even more flexible, more crowded and more chaotic than at present.

The old t.r.f. on h.f.

Inspired by a report from shortwave-listener, Alan Radmore, I have been using an ancient, valve t.r.f. (1-v-1 type) regenerative-detector receiver as an h.f. tuner for casual listening on my domestic broadcast set between 5 and 18MHz. Like Alan Radmore I have been surprised how effectively such receivers (he uses a four-stage, 0-v-3, set with two twin valves, ECC81, ECL82) perform even in the present over-crowded broadcast bands. The use of a regenerative-detector rather than the alternative arrangement of balanced-detector/homodyne direct-conversion provides a good audio quality reception of a.m. broadcast transmissions, marred only by the absence of effective a.g.c. It also gives good results from s.s.b. and morse signals in the amateur-radio bands. With electrical bandspread, tuning is reasonably easy. Selectivity when the detector is close to, or just above, the point of oscillation is far better than might be imagined from a set without i.f. transformers. Alan Radmore has shown that the limited dynamic range of a regenerative detector can be largely overcome by fitting a very simple r.f. attenuator ahead of the receiver.

Currently, the interest in building replicas of simple receivers, designed in the 'thirties' or even earlier, has spread worldwide. In New Zealand, Don Sutherland has measured the performance of an old-style "blooper" two-valve receiver replica built by Peter Byam, ZL2JJ. At about 7MHz it was still providing an (s+n)/n ratio of 12dB for an input signal of only 0.12μV (−129dBm). As he puts it: "It is clear that such a receiver of elementary design is able to match closely the performance, in some important areas, of many of the most modern, sophisticated h.f. receivers and amateur-radio transceivers. We see that the claims of excellent performance made on behalf of these simple sets by 'old-timers', based on their recollections of half-a-century ago and more, are fully substantiated. Only in the 'blocking' performance does it leave much to be desired." It should perhaps be added that a simple regenerative-detector cannot provide true single-sideband or single-signal reception but is excellent for broadcast double-sideband a.m.

Radio Broadcast is written by Pat Hawker.

TELEVISION BROADCAST

Better tv sound?

Although broadcast engineers and some viewers have frequently expressed the view that "sound is the poor relation of television", with set-makers often fitting inferior loudspeakers into acoustically-poor cabinets, the situation has steadily improved, with modern sets often providing entirely acceptable audio. Again, for those with long memories, the disappearance of the intrusive 10,125Hz line whistle of the old 405-line standard brought a welcome relief.

The improvement in tv-set audio at least in the top-of-the-line models has come just in time since the increasing use of digital-audio systems during production and post-production, and with digital stereo systems for terrestrial and satellite systems now not far distant, sound is at last becoming an equal partner to vision. It is not that digits are necessarily better than good analogue broadcast transmission, but they seem to represent the start of a new chapter in tv sound.

Sound engineers who have been working with computerized digital audio post-production systems claim the experience to have been an exciting one "with new applications emerging every day that either save time or provide better sound, or both, in comparison with analogue editing techniques, bringing closer that inevitable day when post-production will be an entirely digital process."

The planned introduction of digital stereo into UK terrestrial and satellite tv broadcasting is having the effect of elevating the importance of tv sound generally. Admittedly, there remains the problem that the size and shape of domestic tv screens and sets is not really well suited to stereo. Viewed from, say, the recommended distance of about six times the height of the picture, there is no way in which in-built loudspeakers could be placed to form with the listener the desirable equilateral triangle. With an out-board audio system and well-separated speakers there remain doubts whether such a wide 'sound stage' fits well with the relatively small size of a tv picture at least until we reach the era of the large, wide-screen pictures that are promised for the future era of high-definition television.

The experience in the cinema and in those countries using analogue tv stereo systems indicates that usually dialogue and soloists are best handled as centre-of-picture mono, with only the sound effects and music dubbed in the stereo mode. Mono dialogue helps to overcome the problem of changing camera angles, etc.

Generally, however, it seems the introduction of stereo-tv will mean that more attention will have to be given to producing and transmitting good quality sound. This is not always as easy as it might be supposed. Inter-city links that are not based on p.c.m. digital transmission seldom extend much above 7,500Hz. The large number of people, camera dollys and cranes etc. moving about on the studio floor can also make it advisable to cut severely the low-frequency response.

Academic barriers

Although radio-frequency interference to television and radio reception has long been a problem, particularly for radio amateurs and c.b. enthusiasts using transmitters in residential areas, the ever-widening impact of r.f.i., e.m.i. and e.m.c. has now made this whole area of major importance in many branches of electronics and telecommuncations.

At a recent IEEIE symposium entitled Electromagnetic Interference: practical design and construction techniques, Professor Mike Darnell of the University of Hull warned that the proliferation of sources of e.m.i. would continue for the foreseeable future as more elements of electronic systems become more susceptible to r.f. fields. He made a strong appeal for more academic interest in the problems of e.m.c.

This whole area was largely neglected as an academic discipline he pointed out, by institutions of higher learning. Many advanced electronic engineering courses ignored it completely. He gave three reasons:

- Although e.m.i. and inadequate e.m.c. were now perceived by industry to be areas of concern, their economic and technical significance was not yet appreciated in the academic sphere.
- Electromagnetic compatibility had still not been recognized as a genuine academic discipline requiring a broad range of expertise.
- No specialist e.m.c. engineers were yet being produced in the higher educational system.

There is, he believes, a serious academic barrier to e.m.i./e.m.c. progress.

It could be, indeed has been, argued that many electronic engineering courses have swung too far away from analogue r.f. engineering towards digital electronics, even though it is largely the introduction of high-speed digits and c.m.o.s. microprocessors into consumer electronics that have dramatically increased the problems of r.f.i.

Recently part of the Rover Group, Gaydon Technology, opened an £800,000 test chamber to study the problems of e.m.c. in relation to the increasing amount of automobile electronics. It has been reported that in Federal Germany it has been necessary to install a giant Faraday cage over a stretch of autobahn that passes close to a defence establishment, to screen the vehicles from strong r.f. fields.

Sound balance

Over many years, a small number of viewers have complained to broadcasters that they find the background music in drama and films too obtrusive and make it difficult or impossible to follow the dialogue. It took some time before it was realised that most of those who complained had hearing impairments and, as a result, were frequently troubled by a sound balance that was entirely satisfactory for those with normal hearing.

Now, at last, a working party has been set up to study this problem, including representatives from the BBC, IBA, ITCA, RNID and the British Association of the Hard of Hearing.

The working party will investigate the way in which the audibility of dialogue and speech can be affected by accompanying music, audience responses and sound effects, both for hard-of-hearing and normal-hearing viewers.

A more frequent cause of viewer and listener complaint is the difficult problem of achieving a satisfactory sound balance at the junctions between the different programmes, speech and music, programmes and commercials, etc. Occasionally, such complaints stem from operational errors or the difficulty of achieving similar levels on a random series of commercials made by different production houses, even though these may all be working within the IBA and ITCA guidelines.

But there are also inherent difficulties in achieving sound levels on radio or television broadcasts that satisfy everybody. Listeners' tastes vary enormously. For instance, some people prefer speech to be quieter when it follows music than when it precedes it. Very much depends upon the junction between two different types of music. The loudness of a sound is not determined by its peak levels (which can readily be measured) but the power represented by the sound, difficult to measure and display accurately.

There are also many subjective or psychological factors outside the control of the broadcasters. Young people have a measurable preference towards music louder in respect of speech than older people. A good music/speech junction differs for classical, light and pop music and even between different languages. People living in cities are less critical of balance than those living in the country. Ambient noise affects the balance perceived by a listener. People switching on dialogue tend to set levels higher than they prefer later. Sound engineers tend to monitor programmes at relatively high levels of sound so that their perception of junction balance differs from that of a domestic listener. But the main problem is when an advertisement with pop music follows immediately upon drama where a producer may require a soft level of speech to produce a required dramatic effect.

Television Broadcast is written by Pat Hawker.

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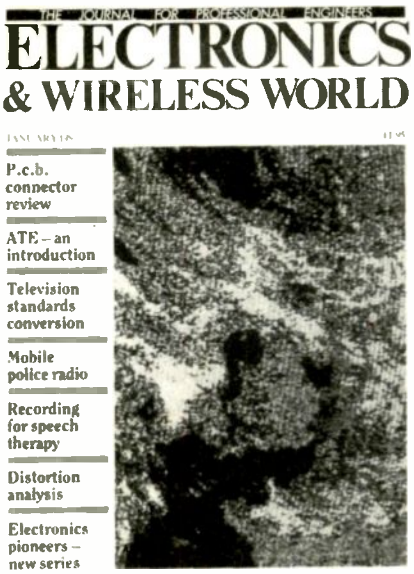

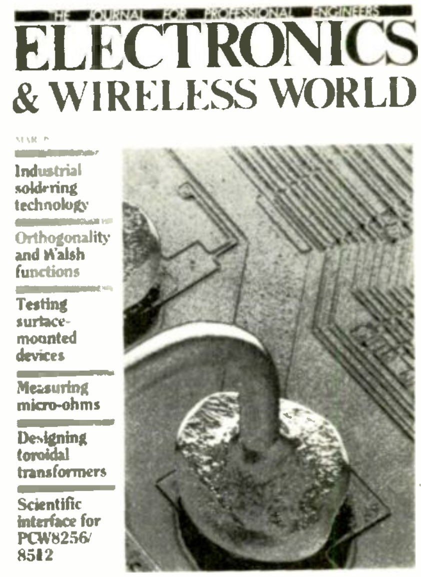

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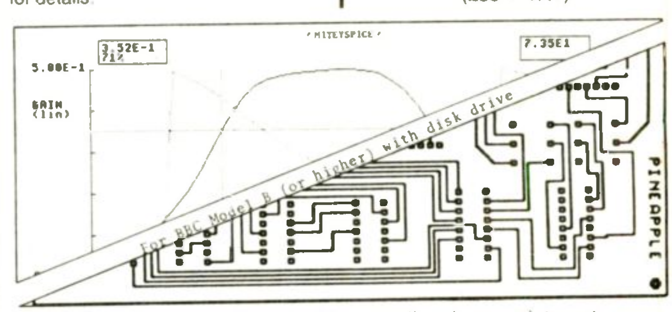

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RADIO COMMUNICATIONS

US privacy law

As noted in this column last month (correcting an earlier misunderstanding), the US Electronic Communications Privacy Act, 1986 was ratified last year and came into force in January. A memorandum circulated by the Washington DC firm of Brown and Schwaniger, a law firm that specializes in representing land mobile and microwave systems and manufacturers of r.f. devices before the FCC, analyses the new Act in detail. From this it is apparent that electronic privacy law in the USA differs substantially from the UK's simple Interception of Communications Act, 1985, in force since April 1986, the main clause of which makes it a criminal offence for any (unauthorized) person to intentionally intercept a communication in the course of its transmission by post or by means of a public telecommunication system. With regard to the interception of radio messages other than as part of a public telecommunication system there are the less harsh penalties of the Wireless Telegraphy Acts.

The new American law is far more detailed. For example, it specifically excludes "the radio portion of a cordless telephone communication that is transmitted between the cordless telephone handset and the base unit" on the grounds that "the user has no reasonable expectation of privacy" (a concept that might surprise many UK users of cordless telephones). It also excludes police, fire and emergency services on the grounds that such transmissions are "readily accessible to the general public".

The Act defines an electronic communication "readily accessible to the general public" as one which is not scrambled or encrypted, transmitted using secret modulation techniques, carried on a subcarrier, transmitted on a common carrier or private microwave system, or a broadcast station's remote pick-up system." The Act thus leaves many radio signals unprotected.

The penalties include substantial fines and up to five years imprisonment. But Brown and Schwaniger suggest that: "Potentially more serious (and far more probable) than the liability to criminal prosecution or suit by the Government for an injunction is the risk of private civil action to which an interceptor is exposed. The Act authorizes any person whose wire, oral or electronic communication is intercepted, disclosed or intentionally used in violation' of the Act may bring a civil action to recover actual or statutory damages, plus attorneys' fees and costs of the suit."

XXXX gets Australian MP the sack

The political career of Australia's former shadow minister of foreign affairs, Mr John Howard, may have been shattered following the publication by a Melbourne newspaper of a mobile-radio conversation he had with a political colleague. In the course of this

he expressed strongly critical views of his party leader, liberally laced with Australian expletives. This was heard and taped by a radio enthusiast who recognized the voices and sent the tape to the newspaper. The result was that John Howard was abruptly dismissed for disloyalty by the Liberal party leader.

When Colossus caught Fish

The dual meetings of the IEE devoted to the development and use of Bletchley Park's two wartime Colossus codebreaking computers – now firmly recognized as "the world's first programmable operational electronics machines" – attracted virtually house-full audiences, with the evening attendance for Professor Sir Harry Hinsley's "Colossus and the German high-grade ciphers" almost filling those little-used balconies at Savoy Place.

During the afternoon session, most of the speakers were members of the original team at the former Post Office Research Station at Dollis Hill, London or those who installed and maintained the electro-mechanical Heath Robinson machines, Colossus Mark 1 (operational from February 1944) and Mark 2, which became operational on exactly its target date of June 1, 1944.

These machines were used only to recover the ten-rotor settings of the German pioneering on-line enciphered radio teleprinter "Geheimschreiber" (secret writer) machines used increasingly from 1942 for the very highest level military traffic (Army Group and above). At BP this became known as Fish traffic.

Mark 1 used 1700 thermionic valves and could process 5000 characters per second. Mark 2 used 2400 valves and processed up to 25,000 characters per second. Both were designed and built at Dollis Hill by a team led by Dr 'Tommy' Flowers (one of the afternoon speakers), advised by BP cryptanalysts Professor Max Newman, Alan Turing and Gordon Welchman.

Although the wartime existence and use of Colossus remained secret for more than 30 years it is now increasingly recognized that this work had an important influence on British post-war work on early digital computers at Cambridge, NPL and Manchester. As Professor B. Randell puts it: "Though Colossus was a more specialized and much slower device, it predated by several years what has usually been assumed to have been the earliest digital electronic computer, the American ENIAC. The Colossus project provided some of Britain's post-war designers with extremely valuable insights and experiences, though for many years their source could not be revealed even to close colleagues. Only recently has it become known that machines such as the early Manchester computer and NPL's 'Pilot Ace' owe their origins partly to Colossus rather than solely to the Eniac/Edvac project in the USA."

Several speakers explained why a machine with over 2000 standard-type valves proved reliable in use, the electronics more so than the mechanical ancilliaries. The valve heaters were *never* turned off, not even during maintenance. The physically large valves such as EF36, 6V6, 807 meant that these were not crowded close together. There were few hot-spots, the valves were de-rated and ran well below maximum ratings.

Characters were read with optical magnification by hard-vacuum photo electric cells. Dr A.C. Lynch told how he first tried using commercially-available gas-filled p.e. cells but their response was too slow. He realized that he needed hard-vacuum cells but as these were extremely rare he expected it to take many months to obtain the numbers he needed. On the off-chance he rang the Ministry of Aircraft Production and, to his surprise, was told to put in an order as they might be able to help. He promptly ordered 1,200. Miraculously, all were delivered within days, free of charge.

Few at Dollis Hill knew what Colossus or the Heath Robinson machines were wanted for. They were told they were working on a new high-speed telegraph system, but soon heard mention of BP. This proved excellent cover since it was taken to mean the RAF headquarters at Bentley Priory.

Even with Colossus, it took a minimum of some four days for BP to decipher the Fish messages which never reached more than about 300 per week, compared with up to more than 20,000 Enigma messages per week.

But those that were read before and after this period were of the highest importance. Sir Harry Hinsley revealed that messages from von Rundstedt's HQ Army West in the period leading up to D-Day (June 6, 1944) showed that the Germans had correctly deduced that the Allied attack would come in Normandy and the Cotentin peninsula with the port of Cherbourg a prime objective. The elaborate Allied deception plans had largely failed, though later successfully re-established when the double-agent w/t messages led to the German's countermanding the removal of crack troops from the Pas de Calais area. Sir Harry revealed that as a result of the Fish breaks, the Allies made last-minute changes to their invasion plans, though he stressed that the Normandy campaign remained in more jeopardy than has generally been appreciated.

Radio Communications is written by Pat Hawker.

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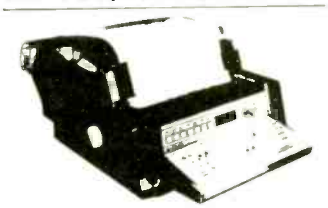

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The European path to digital cellular

A pan-European digital cellular radio system is scheduled for the 1990s. Work is now well under way to select the technology, lay down specifications and forge strategic alliances in this area, which could account for 10 per cent of the telephone market by 1995. Siemens of West Germany and Ericsson Radio Systems of Sweden have already agreed to carry out a joint development.

No single cellular radio system covers the whole of Europe, so even if the PTTs would agree on Europe-wide roaming, system incompatibilities would preclude it. There is the widely-known and used Nordic Mobile Telephone (NMT) system covering Scandinavia, also used in certain other countries such as Switzerland, Net-C in Germany and the UK TACS system. For this reason CEPT (Conference of European Posts and Telecommunications) is keen to promote the development of a common European standard which will, in turn, create a European market. This is expected to provide manufacturing opportunities for European companies and, because of economies of scale, reduce the prices of cellular equipment.

In due course, it will allow the Europe-wide roaming that would be beneficial to the international business traveller. Although the remotest areas are not likely to fall within service areas, the target will be to encompass 90 per cent or more of the populations.

The two UK networks, Cellnet and Vodafone, use TACS, which is arguably the most advanced analogue system. Even though they only started service at the beginning of 1985 they have experienced congestion in London. This has been improved by reducing cell size, and more radio channels have been allocated and will be brought into service next year. But even without the additional facilities that the next generation digital system will bring, especially for data, the expected congestion of the 1990s will make its introduction a necessity.

The CEPT targets are that a draft specification should be issued by the end of this year with the formal specification by the latter part of 1988. This lead time is necessary to enable semiconductor manufacturers to design suitable chip sets. This would allow real network roll-outs to commence by 1990/91 and a national coverage around 1993. While, for example, this time scale would pose no problems in the UK, France is considering an interim system, probably working at 450MHz, because its system is estimated to saturate by 1991.

A meeting of the GSM (Group Speciale Mobile) of CEPT was held in February to consider the results of the competitive field trials held in Paris last year. There were eight potential systems proposed by German, Scandinavian French and Italian companies, within a common overall t.d.m.a. approach, there were two broad-band and six narrow-band contenders which together demonstrated (according to Prof. William Gosling, Technical Director of the Plessey Company) "practically every alternative technical design approach known to the radio community."

Even though considerable mobile development and manufacturing experience exists in the UK, British companies had decided not to originate a system of their own. Consequently, UK specialists were well placed to act in the independent technical assessment of the various proposed systems. Specifically, Plessey has been a member of a consortium carrying out scientific support activities for CEPT via the Cellular Radio Advisory Group (CRAG). This committee brings Britain's manufacturers and operators together in a policy forum. Chaired by the Department of Trade and Industry it includes representatives from British Telecom, GEC, Marconi, Philips, Plessey, Racal and STC. In fact, the recently appointed head of GSM's permanent team in Paris is Bernard Mallinder, who was technical director of Cellnet during its formative stages.

GSM agreed that a digital had substantial advantages over analogue; and, similarly, that time division multiple-access (t.d.m.a.) was preferred to f.d.m.a. Consequently, all the fifteen administrations within CEPT agreed that these techniques should be adopted. In addition, thirteen of them agreed that narrowband t.d.m.a. has substantial advantages over wideband and therefore should be adopted. At that time, France and Germany could not join this agreement as they had expressed a preference for wideband t.d.m.a. Consequently, the GSM requested these two to reconsider their positions and report back. It is believed that they will both follow suit.

The GSM agreed a set of working assumptions that would be adopted for the particular characteristics of a narrowband t.d.m.a. pan-European system. Included in these were that the traffic channel should be 16kbit/s gross bit rate on a full-rate channel and 8kbit/s on a half-rate channel with eight full-rate channels/carrier t.d.m.a. with interleaving and, similarly, 16 half-rate channels being accommmodated within the frame structure.

Similarly, based on tests carried out on two sub-band and two linear predictive coding (l.p.c.) codecs last September in Turin, the speech coding scheme adopted will use the l.p.c. codec developed by Philips Kommunikations Industrie of West Germany with certain features of the French LPC design. Data services will be provided using terminal adaptors via the traffic channel using digital transmission.

Now that the outline parameters have been agreed, even though there is much work to be done in areas such as channel coding and error correction, it is possible for work to proceed towards building a prototype GSM system. In this context, most countries will be proceeding along parallel lines while there will be cooperative groupings within CEPT. For example, the Quadripartite Group of the UK, France, Germany and Italy aim to jointly cooperate. They could well be joined with the Nordic group.

In the UK, CRAG coordinated the Digital Test Bed activities of Racal, BT and Marconi. These were concentrated on coding and t.d.m.a. etc. A separate project was the joint BT/Plessey Digital Cellular Demonstrator where the emphasis was mainly on propagation. In addition, BT and Plessey in conjunction with Southampton University has staged a demonstration of an i.s.d.n. service over digital cellular. Claimed to be a world first, they used a camera in a car near Tower Bridge to transmit slow-scan tv pictures. Signals were sent by a digital cellular radio link into BT's i.s.d.n. centred on a System X exchange.

According to Plessey cellular specialist Donald Cameron, "We are seeing a tremendous growth in the use of cellular telephones and we expect a similar growth of i.s.d.n. services before the end of the decade. The demonstration illustrates what can be achieved by the integration of these two services. And the slow-scan tv shown is but one of the many possible applications, including security surveillance, credit card validation, electronic mail, data transfer and ambulance patient monitoring."

Existing cellular operators will get the licences to operate digital cellular services in due course. In the UK, BT involvement is wide ranging. Not only is much of the research being carried out at its Martlesham Heath laboratories, it is part-owner of the Cellnet network and is also a retailer of mobile communications services and facilities. According to Peter Carpenter, Business Planning Director of British Telecom Mobile Communications, the BT budget for this second generation digital cellular research is £2 million ($3m) in 1988, with the sum increasing by 50 per cent to £3m in both 1989 and 1990. He points out that BT has a down-to-earth approach and watches commercial realities whereas the PTTs tend to overspend.

The stakes are large with cellular expected to achieve 10 per cent of the telephone market by 1995 and the equipment market being worth around £1 billion per annum. But this is only the next stage in the revolution, initial studies are under way for the third generation cellular systems. Operating at around 1.8GHz, these will be the systems for the year 2000. Even more radical approaches will be necessary by then with one of the targets being a "network independent terminal" which, while in the office or home, will act as a cordless phone but will also operate as a cellular phone when out on the road.

–AJM

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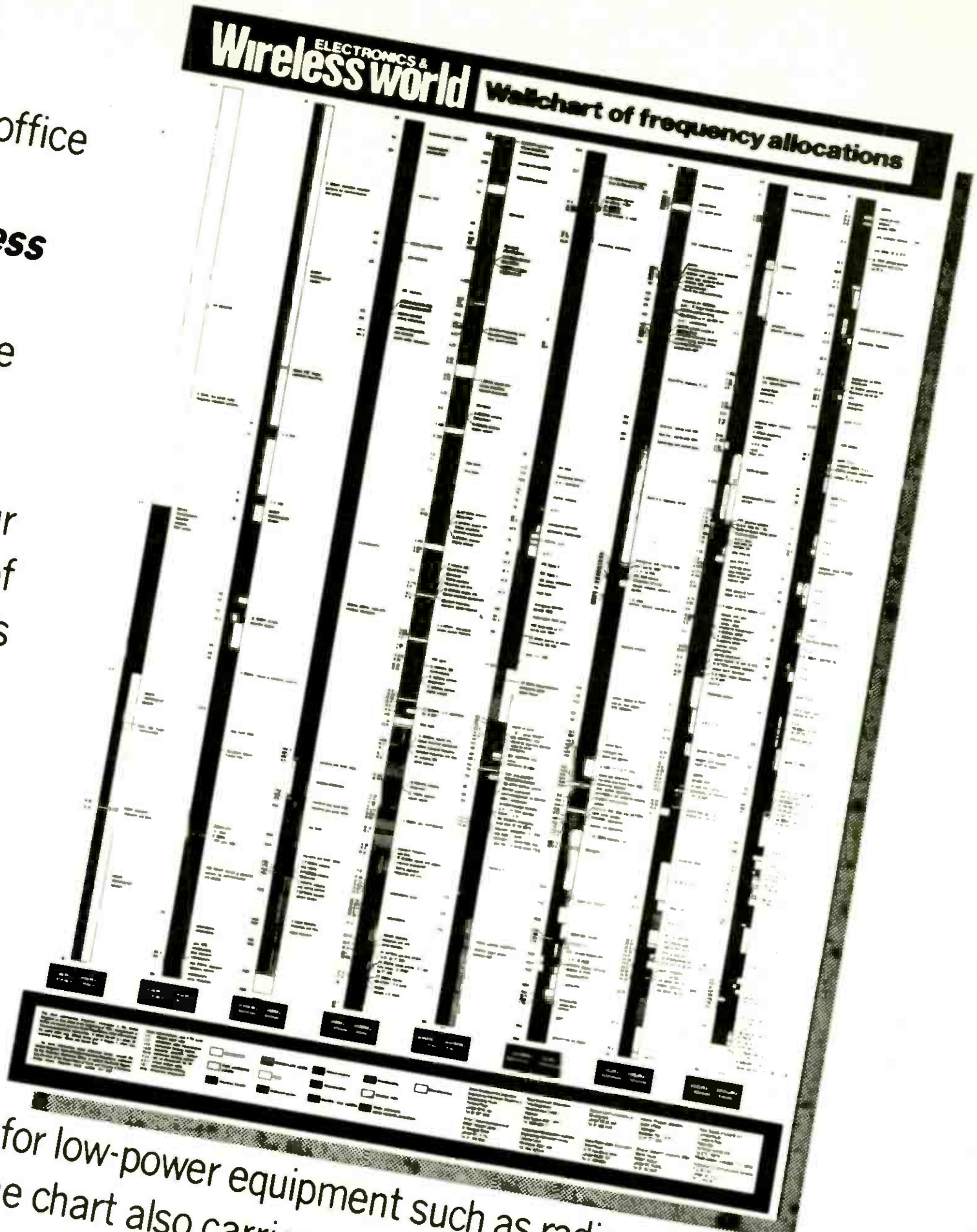

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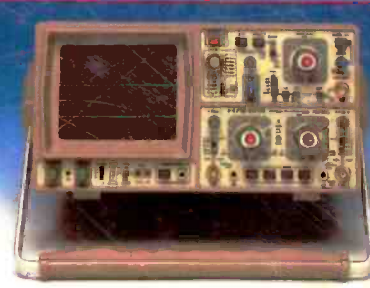

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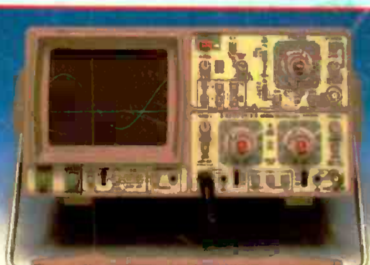

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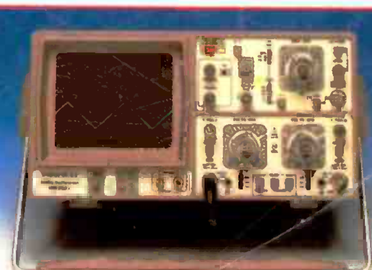

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