THE JOURNAL FOR PROFESSIONAL ENGINEERS

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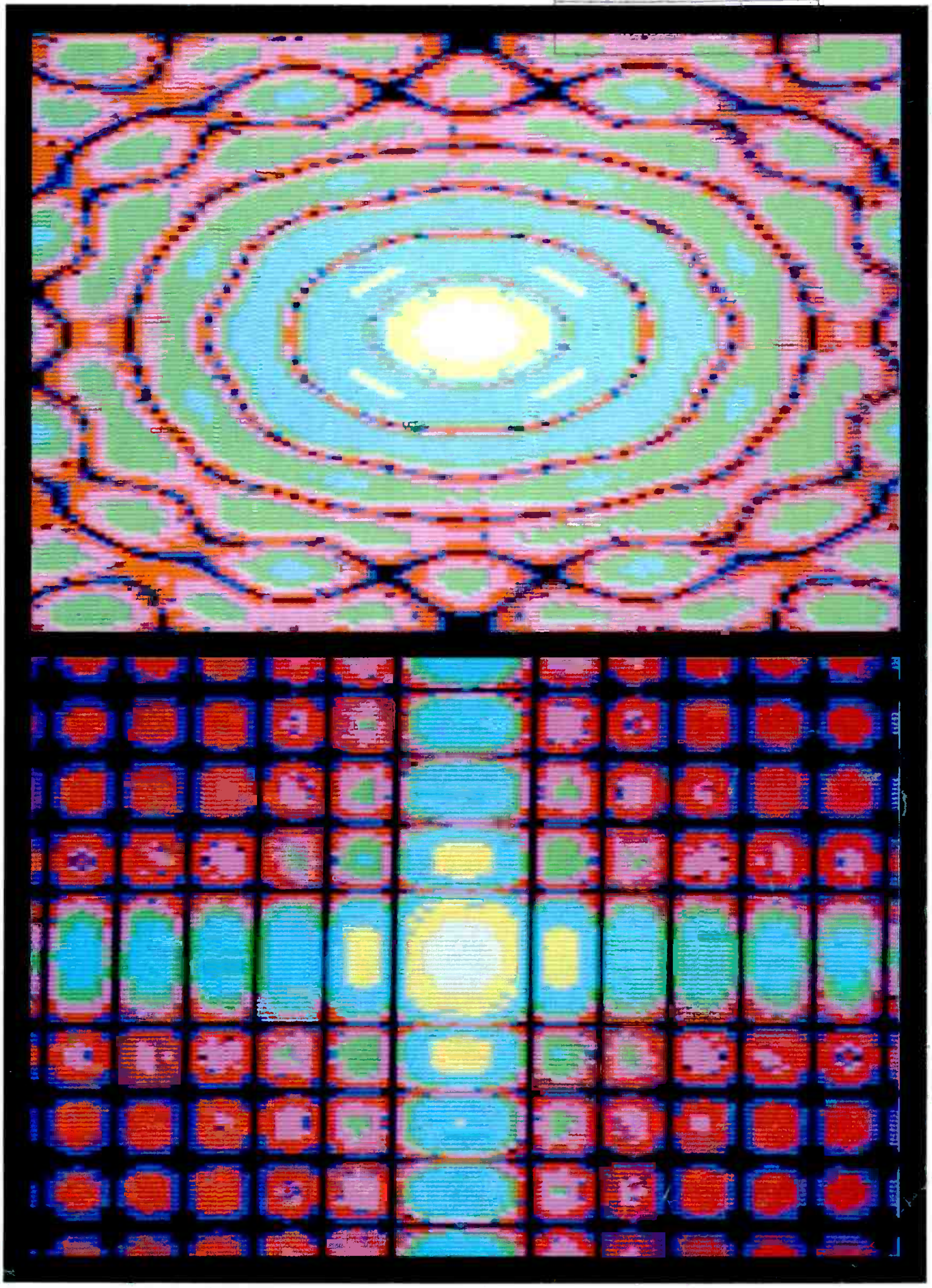

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DECEMBER 1986 VOLUME 92 NUMBER 1610

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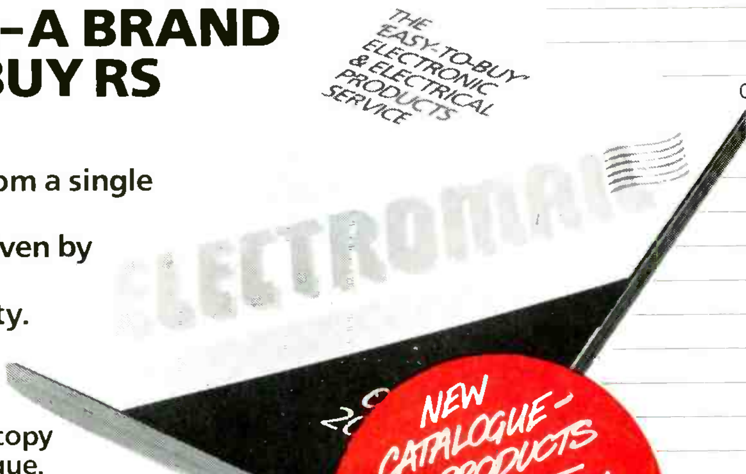

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White-collar engineers

In this issue appears an article in which the author puts forward the view that there is a pressing need for a return to basic thinking in electronic engineering training, the requirement being to produce all-rounders, in the engineering sense.

There appears to be a feeling that a fledgling graduate in electronics or some related discipline needs only to cultivate a relationship with his design-assisting computer, whereupon he can dismiss from his mind almost everything from Ohm's Law to the upper reaches of semiconductor physics and devote himself to broad concepts. The feeling is reinforced in conversations with university lecturers, some of whom express unease at the lack of interest shown by students in the bricks and mortar of electronic engineering. Computing is the spur, it seems, and engineering is beginning to assume once again its traditional greasy image – even the electronic variety.

It can hardly be denied that the computer, in all its forms, is here to stay. But, if education is to consist of almost unalloyed computer programming and application, classical engineering being regarded as superfluous to an engineer's needs, we are surely heading for a disastrous shortage of people who possess an understanding of what is happening behind the technology.

There exists a point of view that engineers do not need the kind of training formerly thought to be essential – the bare bones of circuit design or the physics that lie behind them. Computers are available, they say, which are able to provide fully calculated designs ready to be built: why is the basic theory needed? Faced with a need for, say, an amplifier with a given specification, one can choose from a range of integrated circuits or hybrids, consult the relevant application note and consider the requirement met. And so it is, but who designed the amplifier in the first place?

This is not unsubstantiated fancy. A lecturer of our acquaintance, who asks that his anonymity be protected because his views are unpopular with the university authorities, is outraged at the way in which he is told to teach electronic engineering. Circuit design is for technicians, he is told. All an engineer needs is a standard circuit configuration, a computer to calculate the component values and plot the circuit characteristics and someone else to construct and install it. Even testing is regarded as unnecessary, since the computer indicated that the design was valid.

Taken to a logical conclusion, this view of the needs of a graduate engineer is bound to concentrate the understanding of what is happening in reality, as opposed to what a machine says is happening, in the hands of a very few integrated-circuit designers, so that these few and a host of technicians will know the subject and the 'white-collar' graduates will be interchangeable with any other computer operator.

There is currently a shortage of engineers in some areas of electronics – r.f. design, for example. If the above approach to engineering training is ultimately adopted universally, it is difficult to see how the shortage can be reduced.

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50	235p	200p	390p

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Solder	60	85	125	170
IDC	175	275	325	—
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7428	0.43
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7437	0.30
7438	0.40
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7451	0.35
7453	0.38
7454	0.38
7460	0.55
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7486	0.42
7489	2.10
7490A	0.55
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7492A	0.70
7493A	0.55
7494	1.10
7495A	0.60
7496	0.80
7497	2.90
74100	1.90
74107	0.50
74109	0.75
74110	0.75
74111	0.55
74116	1.70
74118	1.10
74119	1.70
74120	1.00
74121	0.55
74122	0.70
74123	0.80
74125	0.65
74126	0.55
74128	0.55
74132	0.75
74136	0.70
74141	0.90
74142	2.50
74143	1.30
74144	2.70
74145	1.10
74147	1.70
74148	1.40
74150	1.75
74151A	0.70
74153	0.80
74154	1.40
74155	0.80
74156	0.90
74157	0.80
74159	2.25
74160	1.10
74161	0.80
74162	1.10
74163	1.10
74164	1.20
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74173	1.40
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74LS09	0.24
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74LS11	0.24
74LS13	0.34
74LS14	0.50
74LS15	0.24
74LS20	0.24
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74LS38	0.24
74LS40	0.24
74LS42	0.50
74LS43	1.50
74LS48	0.90
74LS49	1.00
74LS51	0.24
74LS54	0.24
74LS55	0.24
74LS73A	0.30
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74LS75	0.45
74LS76A	0.36
74LS78	0.42
74LS83A	0.70
74LS85	0.75
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74LS90	0.48
74LS91	0.90
74LS92	0.35
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74LS95B	0.75
74LS96	0.90
74LS107	0.40
74LS109	0.40
74LS112	0.45
74LS113	0.45
74LS114	0.45
74LS122	0.70
74LS123	0.80
74LS125	0.50
74LS126	0.50
74LS132	0.65
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74LS153	0.65
74LS154	1.60
74LS155	0.65
74LS156	0.65
74LS157	0.50
74LS158	0.65
74LS160A	0.65
74LS161A	0.75
74LS162A	0.75
74LS163A	0.75
74LS164	0.75
74LS165A	1.10
74LS166A	1.50
74LS168	1.30
74LS169	1.00
74LS170	1.40
74LS173A	1.00
74LS174	0.75
74LS175	0.75
74LS181	2.00
74LS183	1.90
74LS190	0.75
74LS191	0.75
74LS192	0.80
74LS194A	0.75
74LS195A	0.75
74LS196	0.80
74LS197	0.80
74LS221	0.90
74LS240	0.80
74LS241	0.80
74LS242	0.90
74LS243	0.90
74LS244	0.70
74LS245	0.90
74LS247	1.10
74LS248	1.10
74LS249	1.10
74LS251	0.75
74LS253	0.75
74LS256	0.90
74LS2457A	0.70
74LS258A	0.70
74LS259	1.20
74LS260	0.75
74LS266	0.60
74LS273	1.25
74LS279	0.70
74LS280	1.90
74LS283	0.80
74LS290	0.80
74LS292	14.00
74LS293	0.80
74LS295	1.40
74LS297	14.00
74LS298	1.00
74LS299	2.20
74LS321	3.70
74LS322A	3.90
74LS323	3.00
74LS324	3.20
74LS348	2.00
74LS352	1.20
74LS353	1.20
74LS356	2.10
74LS363	1.80
74LS364	1.80
74LS365	0.50
74LS366	0.50
74LS367	0.52
74LS368	0.50
74LS373	0.70
74LS374	0.70
74LS375	0.75
74LS377	1.30
74LS378	0.95
74LS379	1.30
74LS381	4.50
74LS385	3.25
74LS390	0.60
74LS393	1.00
74LS395A	1.00
74LS399	1.40
74LS445	1.80
74LS465	1.20
74LS467	1.20
74LS490	1.50
74LS540	1.00
74LS541	1.00
74LS608	7.00
74LS610	25.00
74LS612	25.00
74LS624	3.50
74LS626	2.25
74LS628	2.25
74LS629	1.25
74LS640	2.00
74LS640-1	3.00
74LS641	1.50
74LS642	2.50
74LS642-1	3.00
74LS643	2.50
74LS643-1	3.00
74LS644	3.50
74LS645	2.00
74LS645-1	4.00
74LS668	0.90
74LS669	0.90
74LS670	1.70
74LS682	2.50
74LS683	3.00
74LS684	3.50
74LS687	3.50
74LS688	3.50
74LS783	16.00

[illegible]

74S00	0.50
74S02	0.50
74S04	0.50
74S05	0.50
74S08	0.50
74S10	0.50
74S11	0.75
74S20	0.50
74S22	0.50
74S30	0.50
74S32	0.60
74S37	0.60
74S38	0.60
74S40	0.50
74S51	0.60
74S64	0.45
74S74	0.70
74S85	5.50
74S86	1.00
74S112	1.50
74S113	1.20
74S114	1.20
74S124	3.00
74S132	1.00
74S133	0.60
74S138	1.80
74S139	1.80
74S140	1.00
74S151	1.50
74S153	1.50
74S157	2.00
74S158	2.00
74S163	3.00
74S169	5.50
74S174	3.00
74S175	3.20
74S188	1.80
74S189	1.80
74S194	3.00
74S195	3.00
74S196	3.50
74S200	4.50
74S201	3.20
74S225	5.20
74S240	4.00
74S241	4.00
74S244	4.00
74S251	2.50
74S257	2.50
74S258	2.50
74S260	1.00
74S261	3.00
74S283	2.70
74S287	2.25
74S288	2.00
74S289	2.25
74S299	4.50
74S373	4.00
74S374	4.00
74S387	2.25

74C SERIES

74C00	0.70
74C04	0.50
74C08	0.70
74C10	0.70
74C14	0.50
74C20	0.70
74C32	1.00
74C42	1.50
74C48	1.50
74C73	1.00
74C74	1.20
74C76	1.00
74C83	2.00
74C85	2.25
74C86	0.50
74C90	1.90
74C93	1.50
74C95	1.60
74C107	1.00
74C150	5.00
74C151	2.00
74C157	2.50
74C160	1.80
74C161	1.80
74C162	1.80
74C163	1.80
74C173	1.00
74C174	1.50
74C175	1.50
74C193	1.50
74C194	1.50
74C195	1.50
74C221	2.50
74C244	2.00
74C245	2.25
74C373	2.25
74C374	2.25
74C902	1.20
74C911	9.00
74C912	4.50
74C922	6.00
74C923	6.50
74C925	6.50
74C926	7.50

[illegible]

74ALS00	0.45
74ALS02	0.45
74ALS04	0.50
74ALS08	0.50
74ALS10	0.45
74ALS20	0.45
74ALS32	0.45
74ALS74	0.70
74ALS138	1.50
74ALS139	1.50
74ALS244	4.00
74ALS245	4.75
74ALS573	2.60
74ALS574	4.50
74ALS580	2.60

[illegible]

4000	0.20
4001	0.24
4002	0.25
4006	0.70
4007	0.25
4008	0.60
4009	0.45
4010	0.60
4011	0.24
4012	0.25
4013	0.36
4014	0.60
4015	0.70
4016	0.36
4017	0.55
4018	0.60
4019	0.60
4020	0.80
4021	0.60
4022	0.70
4023	0.30
4024	0.48
4025	0.24
4026	0.90
4027	0.40
4028	0.60
4029	0.75
4030	0.35
4031	1.25
4032	1.00
4033	1.25
4034	2.50
4035	0.70
4036	2.50
4037	1.10
4038	1.00
4040	0.60
4041	0.55
4042	0.50
4043	0.60
4044	0.60
4045	1.00
4046	0.60
4047	0.60
4048	0.55
4049	0.36
4050	0.35
4051	0.65
4052	0.60
4053	0.60
4054	0.80
4055	0.80
4056	0.85
4060	0.70
4063	0.85
4066	0.40
4067	2.30
4068	0.25
4069	0.24
4070	0.24
4071	0.24
4072	0.24
4073	0.24
4075	0.24
4076	0.65
4077	0.25
4078	0.25
4081	0.24
4082	0.25
4085	0.60
4086	0.75
4089	1.20
4093	0.35
4094	0.90
4095	0.95
4096	0.90
4097	2.70
4098	0.75
4099	0.99
4501	0.36
4502	0.55
4503	0.36
4504	0.95
4505	3.60
4506	0.90
4507	0.35
4508	1.20
4510	0.55
4511	0.55
4512	0.55
4513	1.50
4514	1.10
4515	1.10
4516	0.55
4517	2.20
4518	0.48
4519	0.32
4520	0.60
4521	1.15
4522	0.80
4526	0.70
4527	0.80
4528	0.65
4529	1.00
4531	0.75
4532	0.65
4534	3.80
4536	2.50
4538	0.75
4539	0.75
4541	0.90
4543	0.70
4551	1.00
4553	2.40
4555	0.36
4556	0.50
4557	2.40
4560	1.40
4566	1.40
4568	2.40
4569	1.70
4572	0.45
4583	0.90
4584	0.48
4585	0.60
4724	1.50
14411	7.50
14412	7.50
14416	3.00
14419	2.60
14490	4.20
14495	4.50
145000	6.50
14599	2.00
22100	3.50
22101	7.00
22102	7.00
40014	0.48
40085	1.20
40097	0.36
40098	0.40
40100	1.50
40101	1.25
40102	1.30
40103	2.00
40104	1.20
40105	1.50
40106	0.48
40107	0.55
40108	3.20
40109	0.80
40110	2.25
40114	2.25
40147	2.80
40163	1.00
40173	1.20
40174	1.00
40175	1.00
40192	1.00
40193	1.00
40194	1.00
40244	1.50
40245	1.50
40257	1.80
40373	1.80
40374	1.80
80C95	0.75
80C97	0.75
80C98	0.75

LINEAR ICs

AD7581	12.00
ADC0808	11.90
AM7910DC	25.00
AN103	2.00
AN-1-5050	1.00
AY-3-1350	3.50
AY-3-8910	4.90
AY-3-8912	5.00
CA3019A	1.00
CA3020	3.50
CA3028A	1.10
CA3046	0.70
CA3059	3.25
CA3060	3.50
CA3080E	0.70
CA3085	1.50
CA3086	0.60
CA3089E	2.50
CA3090AQ	3.75
CA3130E	0.90
CA3130T	1.30
CA3140E	0.45
CA3140T	1.00
CA3146	2.25
CA3160E	1.50
CA3161E	2.00
CA3162E	6.00
CA3189E	2.70
CA3240E	1.50
CA3280G	3.00
D7002	6.00
DAC1408-8	3.00
DAC0800	3.00
DAC0808	3.00
DG308	3.00
HA1366	1.90
ICL7106	6.75
ICL7611	0.95
ICL7650	4.00
ICL7660	2.50
ICL8038	4.00
ICM7555	0.90
ICM7556	1.40
LC7120	3.00
LC7130	3.50
LC7131	3.50
LC7137	3.50
LF347	1.20
LF351	0.60
LF353	0.90
LF355	0.90
LF356N	1.10
LF357	1.00
LF398	4.00
LM10CLH	4.50
LM301A	0.30
LM307	0.45
LM308CN	0.75
LM310	2.25
LM311	0.60
LM318	1.50
LM319	1.80
LM324	0.45
LM334Z	1.15
LM335Z	1.30
LM336	1.60
LM339	0.40
LM348	0.60
LM358P	0.50
LM377	3.00
LM380N-8	1.50
LM380N	1.50
LM381AN	1.70
LM381N	3.00
LM383	3.25
LM384	2.20
LM386N-1	1.00
LM387	2.70
LM391	1.80
LM392N	1.10
LM393	0.85
LM394CH	4.00
LM709	0.35
LM710	0.48
LM711	1.00
LM723	0.60
LM725CN	3.00
LM733	0.65
LM741	0.22
LM747	0.70
LM748	0.30
LM1011	4.80
LM1014	1.50
LM1801	3.00
LM1830	2.50
LM1871	3.00
LM1872	3.00
LM1886	6.00
LM1889	4.50
LM2917	3.00
LM3302	0.90
LM3900	0.80
LM3909	1.00
LM3911	1.80
LM3914	3.50
LM3915	3.40
LM3916	3.40
LM13600	1.50
M51513L	2.30
M51516L	4.50
MB3712	2.00
MC1310P	1.50
1413	0.75
MC1458	0.45
MC1495	3.00
MC1496	0.70
MC3340P	2.00
MC3401	0.70
MC3403	0.65
MF10CN	4.10
MK50240	9.00
ML902	5.00
ML922	4.00
MM6221A	3.00
NE529	2.20
NE531	1.20
NE544	1.90
NE555	0.22
NE556	0.60
NE564	4.00
NE565	1.20
NE566	1.50
NE567	1.25
NE570	4.00
NE571	3.00
NE592	0.90
NE5532P	1.50
NE5533P	1.60
NE5534P	1.20
NE5534AP	1.50
OP-07EP	3.50
PLL02A	5.00
RC4136	0.55
RC4151	2.00
RC4195	1.50
RC4558	0.55
S50240	9.00
SAA1900	16.00
SFF96364	8.00
SL490	3.00
SN76013N	3.00
SN76023N	3.00
SN76033N	3.00
SN76115N	2.15
SN76489	4.00
SN76495	4.00
SN76660	1.20
SP0256AL2	7.00
SP8515	7.50
TA7120	1.20
TA7130	1.40
TA7204	1.50
TA7205	0.90
TA7222	1.50
TA7310	1.50
TBA231	1.20
TBA800	0.80
TBA810	0.90
TBA20	0.80
TBA820M	0.75
TBA920	2.00
TBA950	2.25
TC9109	5.00
TCA210	3.50
TCA220	3.50
TCA270	3.50
TCA940	1.75
TDA1004A	5.00
TDA1010	2.25
TDA1022	4.50
TDA1024	1.10
TDA1170S	3.00
TDA2002	3.25
TDA2003	1.90
TDA2004	2.40
TDA2006	3.20
TDA2020	3.20
TDA2030	2.50
TDA2593	5.00
TDA2653	7.00
TDA3560	7.50
TDA3810	7.50
TDA7000	3.50
TEA1002	7.00
TL061CP	0.40
TL062	0.60
TL064	0.90
TL071	0.40
TL072	0.70
TL074	1.10
TL081	0.35
TL082	0.55
TL083	0.75
TL084	1.00
TL094	2.00
TL430C	1.20
UA759	3.20
UA2240	1.20
UCN5801A	6.00
ULN2001A	0.75
ULN2002A	0.75
ULN2003A	0.75
ULN2004A	0.75
ULN2068	2.90
ULN2802	1.90
ULN2803	1.80
ULN2804	1.90
UPC575	2.75
UPC592H	2.00
UPC1156H	3.00
UPC1185H	5.00
XR210	4.00
XR2206	4.50
XR2207	3.75
XR2211	5.75
XR2216	6.75
XR2240	1.20
ZN404	1.00
ZN414	0.80
ZN419P	1.75
ZN423E	1.30
ZN424E	1.30
ZN425E8	3.50
ZN426E8	3.00
ZN427E8	6.00
ZN428E8	4.50
ZN429E8	2.25
ZN447E	9.00
ZN448 I	7.50
ZN449E	3.00
ZN450E	7.50
ZN459CP	3.00
ZN1034E	2.00
ZNA1040	6.60
ZNA134H	23.00
ZNA234E	9.50

VOLTAGE REGULATORS

1A FIXED VOLTAGE PLASTIC TO220

+VE			−VE	
5V	7805	0.45	7905	0.50
6V	7806	0.50	7906	0.50
8V	7808	0.50	7908	0.50
12V	7812	0.45	7912	0.50
15V	7815	0.50	7915	0.15
18V	7818	0.50	7918	0.50
24V	7824	0.50	7924	0.50

1A FIXED VOLTAGE PLASTIC TO92

5V 78L05	0.30	5V 79L05	0.45
6V 78L06	0.30	12V 79L12	0.50
8V 78L08	0.30	15V 79L15	0.50
12V 78L12	0.30		
15V 78L15	0.30		

OTHER REGULATORS

FIXED REGULATORS

LM309K	1A 5V	1.40
LM323K	3A 5V	3.50
78H05KC	5A 5V	5.40
78H12	5A 12V	6.40
78P05	10A 5V	9.00

VARIABLE REGULATORS

LM305AH		2.50
LM317T	TO-220	1.20
LM317K	TO3	2.40
LM337T		2.25
LM350T	10A+VAR	4.00
LM396K	10A+VAR	15.00
LM723N		0.50
78HHO5KC	5A 5V	5.75
78HGKC	5A+VAR	6.50
78GUIC	1A+VAR	2.25
79HGKC	5A—VAR	6.75
79GUIC	1A—VAR	2.50

SWITCHING REGULATIONS

ICL7660	2.50
SG3524	3.00
TL494	3.00
TL497	2.25
78S40	2.50
RC4195	1.50

COMPUTER COMPONENTS

CPU

1802CE	6.50
2650A	10.50
6502	4.50
65C02-2MHz	12.00
6502A	6.50
6502B	8.00
6800	2.50
6802	3.00
6809	6.50
6809E	10.00
68B09	10.00
68B09E	12.00
68000-LB	36.00
8035	3.50
80C35	6.00
8039	4.20
80C39	7.00
8080A	7.40
8085A	3.00
80C85A	7.50
8086	22.00
8087	1.20
8087-5	1.20
8087-8	1.60
8088	17.50
8741	15.00
8748	12.00
TMS1601	12.00
TMS9980	14.50
TMS9995	18.00
Z80	2.50
Z80A	2.90
Z80B	5.50
Z80H	7.50
TMS4500	14.00
TMS9901	5.00
TMS9902	5.00
TMS9911	18.00
TMS9914	14.00
Z80PIO	2.50
Z80APIO	2.75
Z80CTC	2.50
Z80ACTC	2.75
Z80DART	6.50
Z80ADART	7.00
Z80DMA	7.00
Z80ADMA	7.50
Z80ASIO/0/2/9	7.00
Z80BPIO	5.00
Z80BCTC	5.00
Z80BDART	9.00

[illegible]

2651	12.00
2816-30	20.00
3242	8.00
3245	4.50
6520	3.00
6522	3.50
6522A	5.50
6532	4.80
6551A	6.00
6821	
68B21	2.50
6829	12.50
6840	3.75
68B40	6.00
6850	1.80
68B50	2.50
6852	2.50
6854	6.50
68B54	8.00
6875	5.00
8154	8.50
8155	3.80
8156	3.80
8205	2.25
8212	2.00
8216	1.60
8224	P.O.A
8226	4.25
8228	5.50
8243	2.60
8250	12.00
8251A	3.25
8253C-5	3.50
8255AC-5	3.20
8256	18.00
8257C-5	54.00
8259C-5	4.00
8275	29.00
8279C-5	4.80
8282	4.00
8284	4.60
8287	3.80
8288D	6.50
8755A	16.00

[illegible]

2101	4.00
2107B	5.00
2111A-35	4.00
2114	1.50
2114-3	2.50
2147	4.00
4116	2.00
4116-20	1.50
41256-15	3.00
4164-15TI	3.00
4416-15	3.50
4532-20	2.50
5101/5501	4.00
5514/5114	4.00
5516	4.00
5517AP	4.00
6116P-3	3.50
6116LP-3	
6264LP-15	3.40
6514-45	4.00
6810	2.00
74S189	1.80
74S289	2.25
93415	6.00
93425	6.00

[illegible]

28L22	4.00
24S10	2.50
18S030	2.00
18SA030	2.00
74S188	1.80
74S287	2.25
74S288	1.80
74S387	2.25
82S23	1.50
82S123	1.50
82S129	1.75

[illegible]

2816-30	15.00
2K+8	30.00
9306 256bits (16×16)	4.50

EPROMs

2516+5V	3.50
2516-35	5.50
2532	4.50
2532-30	5.50
2564	11.00
2708	4.50
2716+5V	3.50
2716-35	5.50
2732	4.50
2732A-2	9.50
2732A-30	6.00
2732A-35	5.50
2764-25	2.00
27C64-25	6.00
27128-25	12.50
27256-25	4.00
27512	P.O.A
27512-25	14.00
TMS2716	5.00

CRT CONTROLLER

CRT5027	18.00
CRT5037	12.00
CRT6545	9.00
EF9364	8.00
EF9365	25.00
EF9366	25.00
EF9367	36.00
EF9369	12.00
MC6845	6.50
MC6845SP	6.50
MC6847	6.50
SFF96364	8.00
TMS9928	10.00

[illegible]

AD7581	15.00
ADC0808	11.90
AD561J	20.00
AM25S10	3.50
AM25LS2521	3.50
AM25LS2538	3.50
AM26LS31	1.20
AM26LS32	1.20
AM7910DC	25.00
DAC80CBI-V	28.00
DM8131	6.00
DP8304	3.50
DS3691	3.50
DS8830	1.40
DS8831	1.50
DS8832	1.50
DS8833	2.25
DS8836	1.50
DS8838	2.25
D7002	8.00
MC1488	0.60
MC1489	0.60
MC3446	2.50
MC3459	4.50
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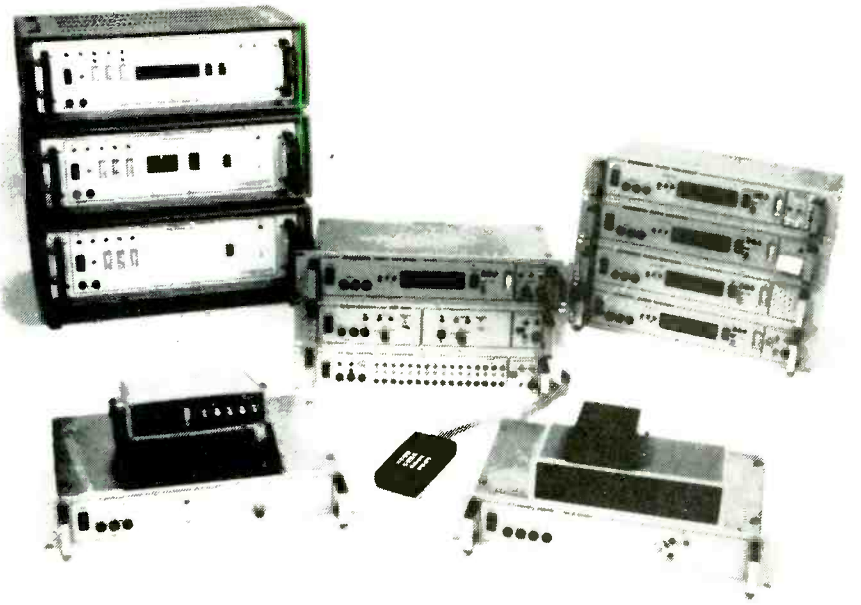

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VMEbus primer

Though current market activity is in 24bit address, 16bit data applications, many bus users are investing in VMEbus systems with a view to future upgrading.

The last decade has seen significant growth in the application of microprocessor-based systems, during which the variety of functions which need to be performed has grown. But because the combination of functions required depends on the application, the trend has been to incorporate functions into blocks. The modular approach has advantages. It
- allows the system builder to incorporate only the combination of functions required for the application
- enables standard modules to be used for a variety of applications
- makes modification of the system for increased function or performance much easier
- enables custom systems to be assembled more quickly and efficiently.

It is now very likely that an engineer will wish to use off-the-shelf modules from a variety of sources. Clearly the integration of boards from several manufacturers will be made easier if they have a standard interface.

An interface standard for microprocessor-based systems must define six main signal groups. At the simplest level, microprocessors operate by passing data from one location to another. Data is moved on a group of signals called the data bus to or from locations specified by addresses placed on the address bus. The movement of data is controlled by a collection of signals which may be loosely called control signals.

Since microprocessors have a facility for being interrupted, there must also be a collection of signals used to indicate when a device is requesting an interrupt and another group to acknowledge that interrupt request. A further group of signals will be required in multi-master systems where the address and data buses may be controlled by any one of several devices. This group will be used to control the arbitration. Finally, there are the basic utilities which the hardware requires to operate, such as power and clock signals.

In addition to the electrical interface, a standard must specify mechanical requirements, both for the electrical connections and the packaging of the components.

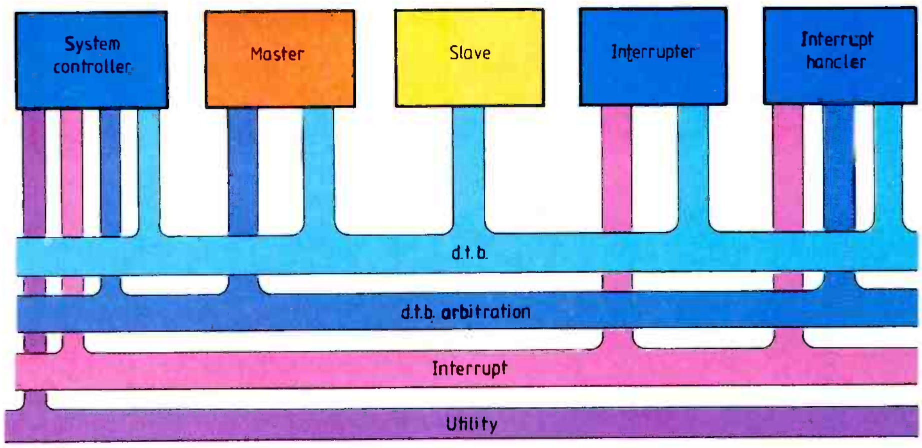


Fig.1. The VMEbus environment is a collection of functional modules which interact over a common backplane. VMEbus boards frequently contain several modules, but for simplicity each module can be thought of as a separate entity. Typically data will be transferred between a master and a slave or an interrupter and an interrupt handler via the backplane. The system controller module provides supervisor functions. Signals on the backplane can be gathered into four groups;
- **data transfer bus to transfer data between VMEbus boards includes the data bus, address bus and control signals**
- **signals to transfer control of the data transfer bus from one master to another**
- **request and acknowledge interrupts make up the priority interrupt bus**
- **system power and error signals on the utility bus.**

VMEbus is an excellent example of a well-defined microprocessor interface standard. It details all of the above signal groups in an unambiguous manner, but still provides scope for a wide variety of user configurations, with mechanical arrangements based on the popular Eurocard format.

HISTORY OF THE VMEBUS

In the late seventies, Motorola designed the EXORmacs 68000 development system. To ease the design process a paper was written to describe the bus used within this system. The bus was Versabus and the paper describing it was published in 1979. Motorola then designed a range of modules using this bus and in doing so revised the Versabus specification, publishing the revised document in 1980. Meanwhile, the European division of Motorola adopted this specification, for a range of modules based on the Eurocard packaging format. The new bus was called Versabus-E.

When Motorola, Mostek and Signetics entered an agreement for second sourcing of the 68000 and the development of support chips in the early eighties, they also agreed to support a standardized bus. They adopted Versabus-E, revised the specification and changed the name to VMEbus . In 1982 this group which by then had been joined by Thomson CSF, published an ammended specification, Revision B. Subsequently, both the IEC and the IEEE formed technical committees to formalise the VMEbus specification under IEC821BUS and IEEE P1014. The results of their involvement were combined, resulting in Revision C of the VMEbus specification, published in February of 1985. Further minor ammendments raised the revision to C.1, which is the release approved by the IEEE.

CURRENT SUPPORT

The VMEbus has achieved such popularity that, internationally, there are now over 200 vendors offering VMEbus support. Many of these vendors have associations with VITA, the VMEbus International Trade Association. This is a non-profit making body which helps to promote the VMEbus to the benefit of vendors and users. VITA also produce the VMEbus Compatible Products Directory, a helpful document for users and potential users of VMEbus products. The VMEbus specification revision C.1 is endorsed by VITA and is an essential document for anyone designing on VME. Copies of this specification are obtainable in the UK from High Technology Electronics Ltd in Southampton.

The range of products currently available covers processors, memory, mass storage devices, i/o specialist controllers and a variety of hardware and software support. The majority of the processor boards in the market place are based on Motorola devices, but there are many boards available which use processors from other manufacturers, including Intel, Zilog and National Semiconductor. One of the latest VMEbus boards designed by High Technology Electronics, HVME-SB286, is a single-board computer featuring the Intel 80286 processor.* It is a reflection of the versatility of the VMEbus that the current offerings include 8, 16 and 32-bit processors.

The selection of i/o boards on offer includes a number of analogue-to-digital and digital-to-analogue converters and a range of serial and parallel digital i/o boards.

For users wishing to configure VMSbus systems that include network interface, there are a number of Ethernet and MAP interface boards. However, the widest selection of special controller boards is in the graphics field, several using the popular and versatile NEC7220 graphics processor.

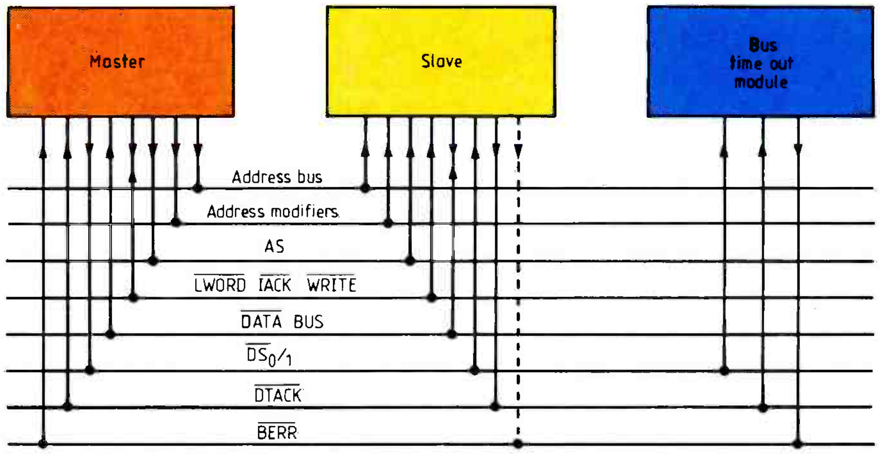


Fig.2. Data transfer in the VMEbus environment is initiated by a master. The master provides the address of the slave device to be accessed together with qualifying signals, address modifier, $\overline{IACK}$ etc. If the data transfer is a write cycle, the master must also provide the data. Slave receives data in a write cycle, or outputs data in a read cycle, in response to the master driving the data strobe low ($\overline{DS_0}$, $\overline{DS_1}$). Slave acknowledges that data has been completed by driving $\overline{DTACK}$ low, or if the slave detected an error in the transfer by driving $\overline{BERR}$ low. If the slave fails to respond within a time-out period, bus time-out drives the bus error signal low. Master terminates the cycle in response to either $\overline{DTACK}$ or $\overline{BERR}$ being driven low.

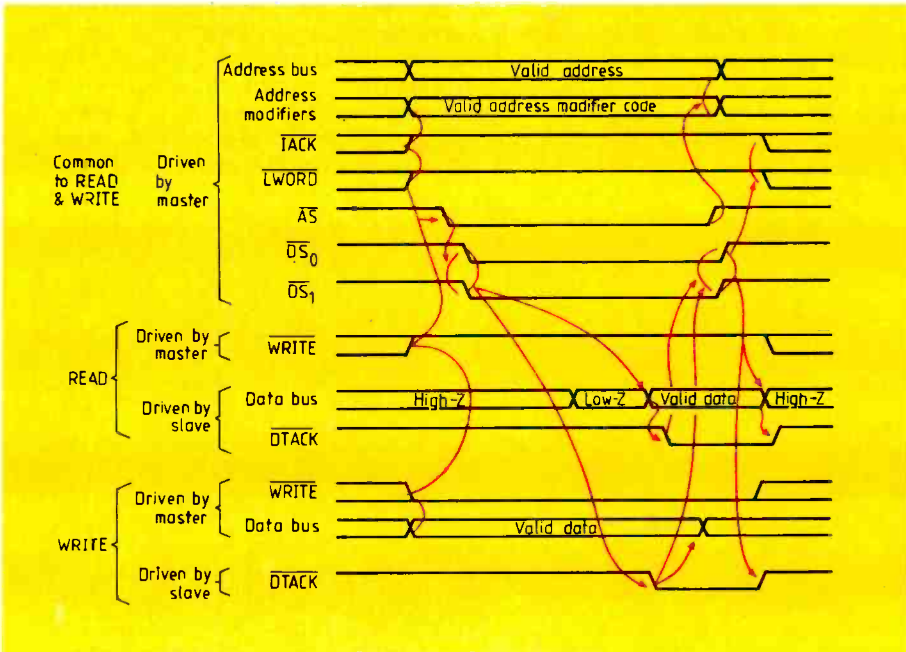


Fig.3. Read and write cycles are both initiated by the master, which indicates whether the cycle is a read or a write by driving the $\overline{WRITE}$ line to the appropriate state. During a read cycle, the slave places valid data onto the data bus in response to the data strobe being driven low. The slave indicates the availability of valid data on the bus by driving $\overline{DTACK}$ low. When the master has received the data, it drives the data strobe high which causes the slave to release the data bus then release $\overline{DTACK}$. During a write cycle, the master must place valid data on the data bus before driving either of the data strobes low. It must maintain this data in a valid condition until the slave has acknowledged receipt by driving $\overline{DTACK}$ low. The master may then release the data strobe causing the slave to release $\overline{DTACK}$.

FUTURE POTENTIAL

VMEbus has firmly established itself in the market place, but the majority of the current market activity is in the 24-bit address and 16-bit data field. This implies that many bus users are investing in VMEbus systems with a view to future uprgrading. Although there is already a choice of 32-bit processors, the selection is bound to increase as later devices such as the Intel 80386 are interfaced to the bus. Many of the slave boards currently available already have 32-bit capability. In these days of short product life cycle it makes a welcome change to have a product which is here today and will still be here tomorrow.

BUS OVERVIEW

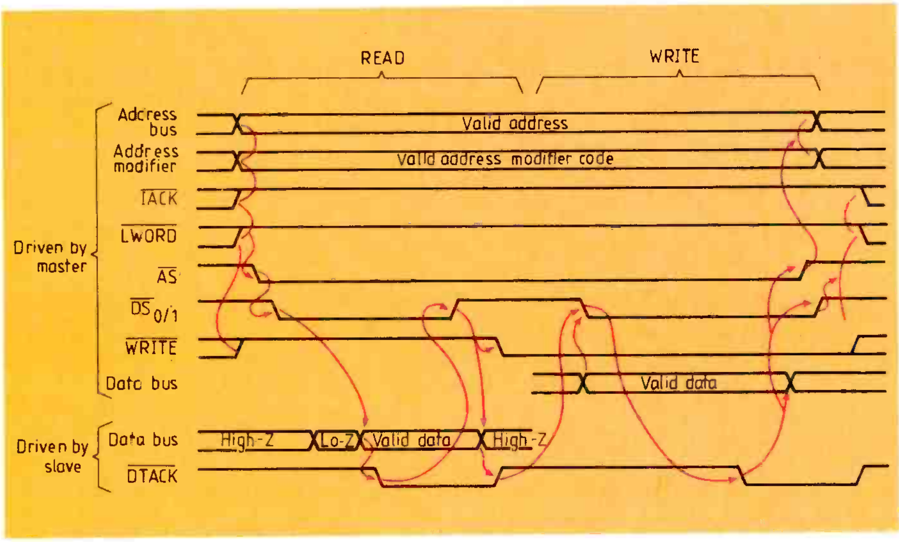
In a VMEbus system, data is transferred between system modules via a backplane. The module which controls the data transfer is called a master, the module which participates in the data transfer is called a slave. The time taken to transfer data between a master and a slave is not fixed by the master, but depends on the slave indicating that its part in the transfer has been completed. With this asynchronous arrangement there is the risk that if a master attempted to communicate with a non-existent or a defective slave, then the master could wait for a response from the slave indefinitely. To avoid this, each VMEbus system must contain a 'bus time out' module. This module activates an error signal if a master waits too long for a response from a slave. Masters must obviously be capable of recognising and responding to this error signal to recover from the error condition.

There are several functional modules which are used to explain the operation of the VMEbus, representing circuits or parts of circuits necessary for particular types of VMEbus boards to operate. Some functional modules, such as the 'bus time out' module, only occur once in a VMEbus system, whilst others such as interrupters, may occur many times. Many of the functional modules operate in a choice of modes. VMEbus board manufacturers often design their products to reflect this, enabling a single board to perform in a number of modes so that the most suitable configuration may be selected for the target system.

VMEbus is non-multiplexed so has separate signal lines for the address and data buses. Address of the next location to be accessed is transmitted on the address bus whilst data from the previous access is still being transferred on the data bus. This enables data transfers to take place at higher speeds than would be possible with a multiplexed architecture, where the same signal lines are used for the transmission of address and data.

Data may be transferred on the VMEbus as

*To be featured in a later article.



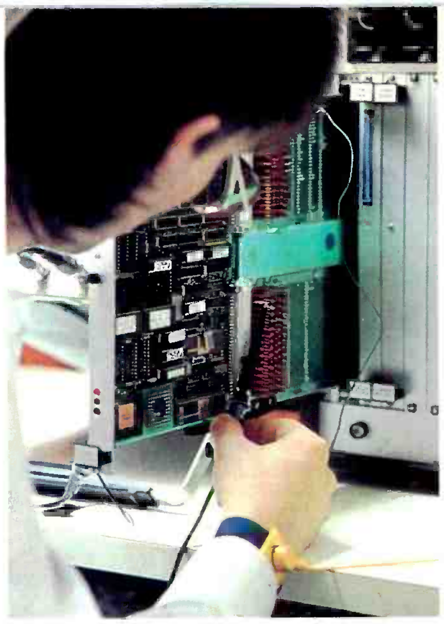
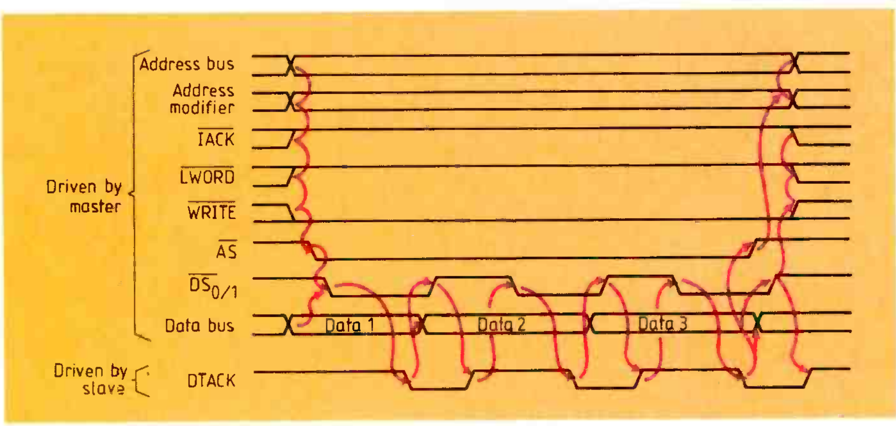


Fig.4,5. Read-modify-write cycles enable VMEbus master to perform test and set sequences on located in VMEbus memory without the risk of another master changing the condition of the flag during the test. The cycle starts as a memory read cycle, but when the master drives the data strobe high at the end of the read operation it maintains the same address on the bus, the same qualifying signals, and holds the address strobe (AS) active. The WRITE signal is driven low and modified data placed on the bus. The data strobe are driven low to perform WRITE. The cycle continues as a normal write cycle. The master sets up address and qualifying signals once for the start of block transfer, providing an efficient method of transferring large quantities of data. Block transfer cycles start in the same way as signal transfers except for a special address modifier code. At the end of the first and subsequent transfers the address and qualifying signals are held active. The data strobes are driven high then low again to start the next transfer. The slave uses the toggling of the data strobes to increment the address of the location being accessed. At the end of the block transfer, the address and qualifying signals are released.



bytes, words (16 bits), or longwords (32 bits). There is also a choice of address bus widths at 16, 24 or 32 bits giving a physical address range of 65K, 16M or 4Gbyte respectively. The ability of the VMEbus to support such a variety of address and data bus widths not only makes it a versatile bus but also enables a variety of devices to be interfaced to it. The mnemonics A_{16}, A_{24} and A_{32} denote the address bus widths supported by VMEbus boards; similarly, D_{08}, D_{16} and D_{32} denote the data bus widths supported.

This combination of non-mutiplexed buses and bus widths enables data to be transferred on the bus at up to 50Mbyte per second.

VMEbus is a multi-master bus, so a VMEbus system may contain more than one master. However, only one master may take control of the bus at a time, so each VMEbus system must include a module capable of determining which of the masters, if any, will take control of the bus. This module, called the arbiter, must be provided by the system controller board positioned in slot 1 of the VMEbus system. Each master in a VMEbus system must contain a module called a requester which determines when the master requires control of the bus and takes care of the necessary handshaking.

There are seven prioritized interrupt request signals on the VMEbus backplane. Any board capable of generating an interrupt request must contain an interrupter module. This module will not only generate the interrupt request, but will also determine when that interrupt request is being acknowledged and provide the necessary status information during the interrupt acknowledge sequence. For each interrupt request that may be generated, there must be a corresponding interrupt handler module. The handler must acknowledged the interrupt request, perform an interrupt acknowledge sequence and take some action as a result of the interrupt request having occurred.

A VMEbus system must contain an arbiter, an IACK daisy-chain driver module, a bus time out module and a system clock driver module. These functional modules must all be provided by the system controller board which must be installed in slot 1 (the left-most position when viewing the card frame from the direction in which boards are installed). Many VMEbus processor boards contain the functions performed by a system controller board, so it is not always necessary to have a separate system controller board.

The most commonly used format for VMEbus boards is the double Eurocard, but single Eurocards may be used. For boards using up to 24-bit addressing and the 16-bit data bus, there is no electrical requirement to use the double Eurocard, since all of the connections required are available on the upper backplane connector. The centre row of the lower connector is used for address bits A_{24}-A_{31} and data bits D_{16}-D_{31}. The VMEbus backplane is terminated. This has three advantages:

- When control of a signal line is passed from one device to another it will not be driven by either device. The termination network ensures that the signal will be in a known (inactive) state.
- When designing the VMEbus boards, savings can be made by not providing drivers for those signals which the board would only ever drive to an inactive state.
- The termination network helps to control the transmission line effects of the backplane.

Detailed operation of the VMEbus is described in the sections in smaller type; there are four parts.

Data transfer bus: Data is transferred between masters and slaves over the data bus. Masters select the slave which data will be transferred to or from using the address bus. There are several control signals used to supervise the data transfer. The address and data buses, together with the relevant control signals are referred to as the data transfer bus.

DTB arbitration: The VMEbus is a multimaster enviroment, which means that a system may contain several modules which may control data transfer on the data transfer bus. Clearly the d.t.b. may only be controlled by one master at a time. A system of arbitration has been included which determines whether:

— the d.t.b. is in use.
— one of more masters are requesting control of the d.t.b.
— which one of several master may take control of the d.t.b.

Interrupt handling: There are seven levels os prioritized interrupt request in the VMEbus standard, all acknowledged in the similar mannner. A VMEbus system may contain several interrupt handlers.

VMEbus utilities: In addition to the power supply, the VMEbus backplane carries several utilities such as error indicator signals and the system clock.

DATA TRANSFER BUS

The data transfer bus consists of address bus, data bus and those signal necessary to control the movement of data on the VMEbus. The d.t.b. signals are summarized in the panel.

Width of data transfer. Data is transferred on the VMEbus as eight bits (single byte), 16 bits (word or double byte), or 32 bis (longword or quad byte). The data strobes, DS_0 and $\overline{DS}_1$, together with address line A_{01} and $\overline{LWORD}$ are issued by the master to indicate the width of the data transfer and which parts of the data bus carry the data (see table). Single and double byte transfers are performed on data bits 0 to 15; quad byte transfers require the full 32-bit width. Mnemonics D_{08}, D_{16} and D_{32} denote the data bus width supported by VMEbus boards.

All data transfers on the VMEbus are performed in a similar manner. The only distinction between data fetch and opcode fetch cylces is the in the address modifier codes transmitted by the master.

Basic transfer. There are seven major stages controlling data transfer, assuming that the bus master controlling the transfer already has control of the VMEbus.

— Master places the address of the location to be accessed onto the address bus and places a valid address modifier code onto the address modifier lines.
— Master drives $\overline{IACK}$, $\overline{LWORD}$ and $\overline{WRITE}$ valid.
— Master qualifies the address and address modifier codes by driving the address strobe, $\overline{AS}$, low.
— Master initiates the data transfer by driving one or both of the data strobes, DS_0 or $\overline{DS}_1$ low.
— Slave responds that data transfer has occurred by driving $\overline{DTACK}$ low.
— Master terminates the cycle by driving the data strobes and the address strobes high.
— Slave drives $\overline{DTACK}$ high.

Data transfers are of five types: read, write, read-modify-write, block transfer, and unaligned transfer. Read and write cycles both closely follow the basic data transfer sequence illustrated, but there are differences in the timing relationships between the data strobes, $\overline{DTACK}$ and the availability of data.

Read. The master indicates a read cycle by driving the $\overline{WRITE}$ signal high before driving either of the data strobes low. The slave then places valid data onto the data bus and drives $\overline{DTACK}$ low to indicate that valid data is available. The master reads the data and drives the data strobes high. When the slave sees the data strobes go high it releases the data bus and then indicates that it is no longer driving the data bus by releasing $\overline{DTACK}$.

Write. The master drives the $\overline{WRITE}$ line low to indicate that it is a write cycle and places the data onto the bus. Then the data strobe is driven low to indicate the presence of valid data and which bytes of the bus are being

Data Transfer Type	Data Lines Used 00 07	08 15	16 23	24 31	Qualifying Signals DS_0	$\overline{DS}_1$	A_{01}	LWD
Single Byte								
Byte 0	–	0	–	–	HI	LOW	LOW	HI
Byte 1	1	–	–	–	LOW	HI	LOW	HI
Byte 2	–	2	–	–	HI	LOW	HI	HI
Byte 3	3	–	–	–	LOW	HI	HI	HI
Double Byte								
Byte 0-1	1	0	–	–	LOW	LOW	LOW	HI
Byte 2-3	3	2	–	–	LOW	LOW	HI	HI
Quad Byte								
Byte 0-3	3	2	1	0	LOW	LOW	LOW	LOW
Unaligned								
Byte 1-2		2	1		LOW	LOW	HI	LOW
Byte 0-2		2	1	0	HI	LOW	LOW	LOW
Byte 1-3	3	2	1		LOW	HI	LOW	LOW

SIGNALS CONTROLLING DATA TRANSFER

A01-A31: address bus. The master selects the slave by placing its address on the address bus. The address width used by the master may be 16 bits (short addressing), 24 bits (standard addressing), or 32 bits (extended addressing); bits 24 to 31 are transmitted via the P2 connector. The width of the valid address bus is indicated by the address modifier code which the master transmits at the same time as the address. Mnemonics A_{16}, A_{24} and A_{32} denote the address bus width supported by VMEbus boards.

The address used are all memory addresses. There is no port map into which peripheral devices may be mapped, however, it is generally accpeted (although not enforced by the specification) that i/o devices may be addressed using short addresses (16 bit). This 64 Kbyte block is mapped into the top 64 Kbytes to the 16 Mbyte memory space.

$AM_0 - AM_5$: address modifier code. The master also places an address modifier code onto the modifier lines. This 6-bit code qualifies the type of address being transmitted and the type of transfer about to take place. Address modifier codes in the range 10 to 1F are for user-defineable accesses. Those codes allocated for specific functions are summarised in the table; all other address modifier codes are reserved.

Address Width	Block Transfer	Program Access	Data Access	Any Access
Supervisor Access				
Short (16 bit)	–	–	–	2D
Standard (24 bit)	3F	3E	3D	–
Extended (32 bit)	0F	0E	0D	–
User Access				
Short (16 bit)	–	–	–	29
Standard (24 bit)	3B	3A	39	–
Extended (32 bit)	0B	0A	09	–

The address modifier codes provide a convenient method of partitioning the memory to provide memory protection for supervisor functions as illustrated in the code allocations. Similarly, the user-defineable modifier codes could be used to separate users or tasks. The modifier codes effectively increase the memory space available on the VMEbus since they provide a form of bank switch.

AS: address strobe. Used by the master to qualify the condition of the address, address modifiers, LWORD and IACK transmitted by the master during a data transfer cycle.

$\overline{D00\text{-}D31}$: data bus. Four bytes wide, but data will only be transferred on those bytes indicated the data strobes, address line A_{01} and $\overline{LWORD}$. Data bits D_{16}-D_{31} are transferred via the P2 connector.

$\overline{DS0/DS1}$: data strobe 0/1. Primarily they are used to indicate when data is being transferred via the the VMEbus. However, as DS_0 and DS_1 each related to specific bytes within the data bus, they also specify the width of the data field being tranferred (byte, word, or longword).

$\overline{LWORD}$: Longword. Whenever three or more bytes of data are transferred in a single cycle, data bits D_{16}-D_{31} must be used. $\overline{LWORD}$ indicates that the upper half of the 32-bit data bus will be used

$\overline{WRITE}$ is a control signal driven by the Master to indicate whether the data transfer is a read ($\overline{WRITE}$ high) or a write ($\overline{WRITE}$ low) cycle. The state of the $\overline{WRITE}$ signal is qualified by the data strobe.

$\overline{IACK}$: interrupt acknowledge. When an interrupt handler module acknowledges an interrupt request, it performs an interrupt acknowledge sequence on the VMEbus. As part of this sequence, a status indicator will be read from the device which generated the interrupt. The IACK signal will be driven low to distinguish it from a normal read.

$\overline{DTRACK}$: data transfer acknowledge is used by slave devices participating in a data transfer to indicate to the master that the transfer has occurred.

$\overline{BERR}$: bus error. If an error condition is detected during a data transfer, then the $\overline{BEER}$ signal will be activated by the device which detects the error. This may either be the participating slave or the bus time out module. Masters must be capable of responding to an active $\overline{BEER}$ signal.

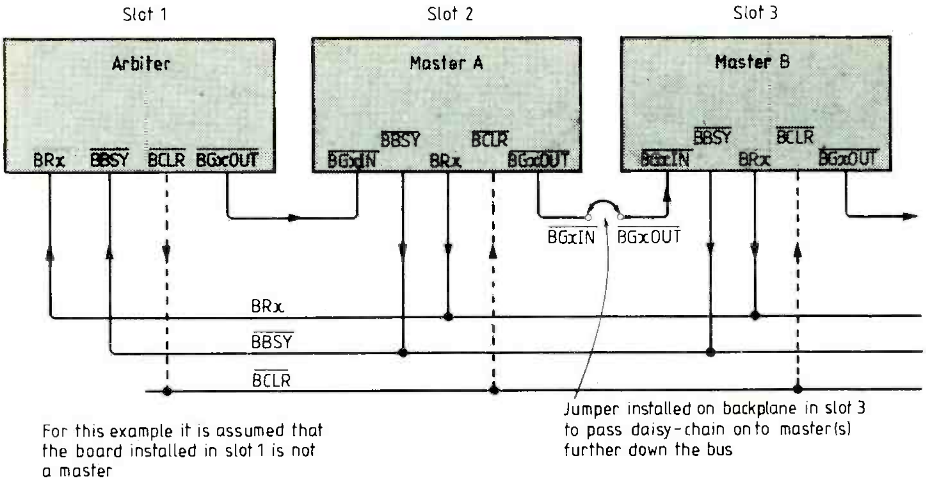
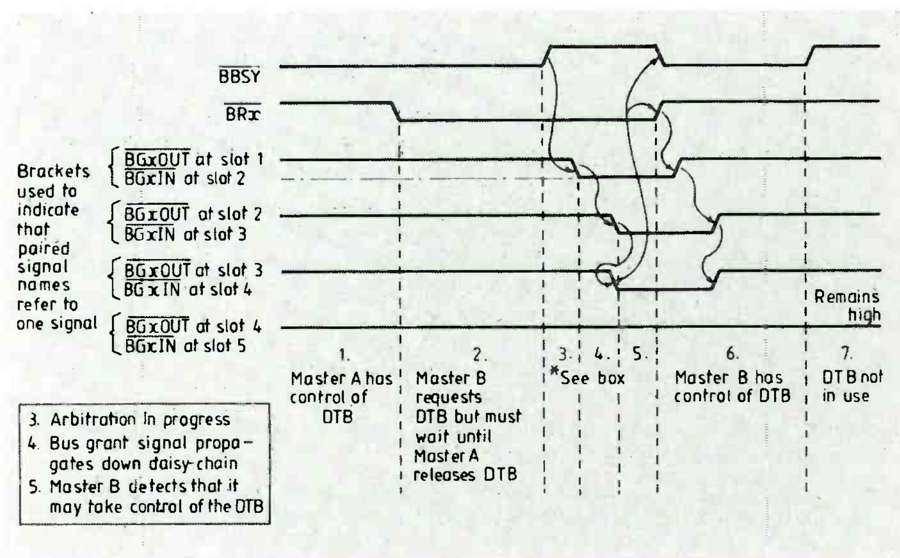


Fig.6,7. VMEbus masters bus control by activating one of four prioritized bus request lines. An arbiter (located in slot 1, the left-most board position) determines when control of the bus may be transferred and the level of bus request to which control will be granted. The arbiter indicates the level of bus request which may take control of the bus by activating a corresponding bus-grant daisy chain. The bus-grant signal then propagates down the daisy chain until it reaches the master that activated the request signal. This master will not propagate the grant signal further down the daisy chain, but takes control of the bus, indicating this by activating the bus-busy signal (BBSY). As the master releases control of the bus, it releases bus-busy. The arbiter is then free to grant control of the bus to another master.



used. When the slave has received the data, it drives DTACK low; the master may then remove the data from the bus and return the strobe high. Finally, the slave releases DTACK.

Read-modify-write. One of the problems encountered in multi-master systems is the use of test-and-set sequences to examine and modify semaphores held in the global address space. As an example, consider a semaphore used to indicate if a printer is being used. One master could read the semaphore to see whether the printer was available and whilst it was deciding that the printer was free, another master could change the state of the semaphore and start to use the printer. To avoid this, VMEbus supports read-modify-write cycles. The RMW cycle starts like a normal read cycle, but the sequence changes when the slave reponds with DTACK. When the master sees DTACK driven low by the slave, it drives the data strobe high and drives WRITE low. The slave sees the data strobe go high and releases first the data bus and then DTACK. As soon as this goes high, the master can place the modified data onto the data bus and drive the data strobe low. The cycle then continues as a normal write cycle. The address placed on the address bus unchanged between the read write part of the cycle. The master must maintain AS low throughout the cycle. By keeping AS low, the master prevents another from taking control of the d.t.b. part way through the cycle, since control may only be transferred if AS is high.

Block transfer. It is often desirable to transfer large quantities of data from one board to another, as would be the case when loading a file from a mass storage device. VMEbus achieves this using the block transfer feature, which starts like any other cycle, but at the end of the first data transfer AS is held low and the main address remains stable. The data strobe are then driven high and low again to start another cycle. Transitions of the data strobe must still be interlocked with transitions in DTACK, but the master does not issue a new address for each data transfer. The slave increments the address automatically each time the data strobe are driven high then low again. Because special interface hardware is required to perform block transfers, not all slave boards support this feature. To simplify board design, the VMEbus specification does not permit block transfers to cross 256 byte address boundaries.

Unaligned transfers. A master that performs 32-bit data transfers may need to fetch three bytes of data. There are three ways: three single-byte data transfers, one single-byte data transfer and one double-byte data transfer, or one three-byte, unaligned data transfer. Unaligned data transfers can improve system performance by reducing the number of accesses, though only boards with a 32-bit data bus can have the unaligned ability. Signals for unaligned data transfers follow the sequence for basic data transfer.

Pipelined addressing. The speed with which slaves respond to an access can sometimes be improved by providing the slave with the address of the location to be accessed earlier in the cycle. VMEbus provides for this by enabling the address to be pipelined, where the address of the next location to be accessed is transmitted on the address but whilst data from the previous access is still available on the bus.

DTB ARBITRATION

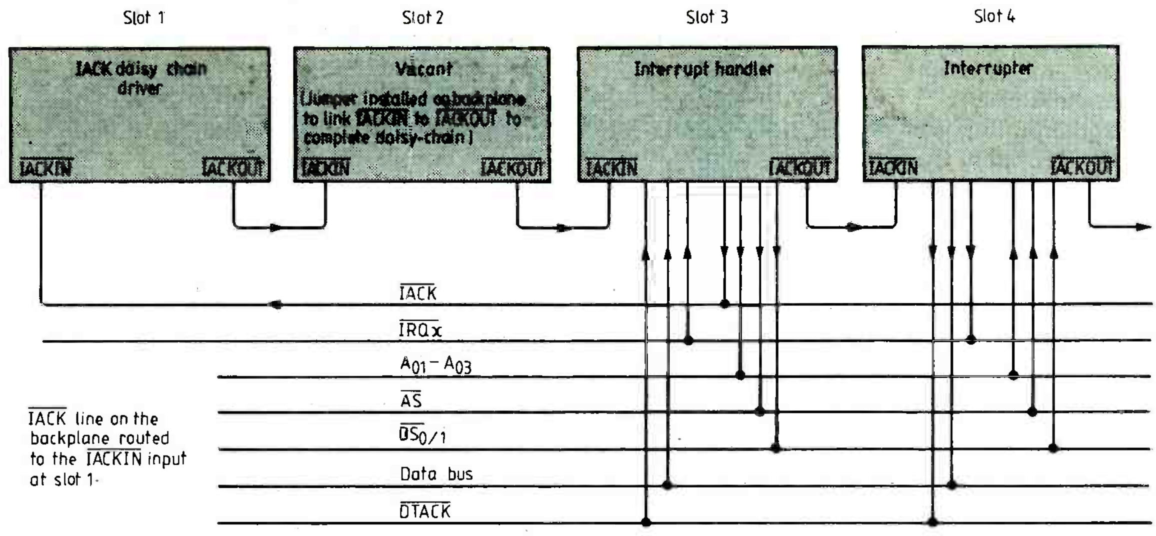
VMEbus is a multi-master bus in that data transfer can be controlled by any one of several devices. Clearly, only one such device can control the bus at a time. A scheme is therefore required to determine which device should take control and to supervise the transfer of control from one device to another.

In the VME environment, masters use one of four priortitized bus-request signals to indicate when they require the bus. An arbiter module located in slot 1* determines which of the active bus-request signals has the highest priority and grants control of the bus to that level. Bus-grant signals are daisy-chained through all of the slot positions, so for any one bus-grant level, masters nearest the slot 1 position have a higher priority than other masters using the same bus-grant level, but which are further away.

Masters indicate when they have control of the d.t.b. by driving the bus-busy line low: control cannot be transferred if the bus-busy signal is low. A master that has control may be informed that a higher priority master wishes to use the bus by the bus-clear signal.

Basic transfer of d.t.b. control. Each VMEbus master must contain a requester module which determines when the master requires control of the bus and handles the interchange required with the arbiter to obtain control of the bus. The requester module also determines the circumstances under

* The left-most slot position when viewing the card frame from direction in which boards are installed.



which control of the bus will be relinquished. Here is the sequence of events surrounding aquisition of d.t.b. control.

- Requester determines that the master requires control, and causes master to temporarily suspend activity, driving one of the bus request lines low.
- Arbiter receives bus request signal and, if this is the highest priority bus request pending and if the d.t.b. is not being used by another master, drives the bus grant daisy-chain corresponding to the bus request signal.
- Requester module receives the bus grant signal on the BGxIN input, and signals that it has control of the bus by driving the bus busy signal (BBSY) low. Releases bus request signal permiting master to continue it's activity. Requester does not pass the bus grant signal further down the daisy-chain.
- Arbiter sees the BBSY signal go low and drives the bus grant signal daisy-chain high.

The requester module drives BBSY low for as long as the master retains control of the bus. When this control is surrendered the reques-

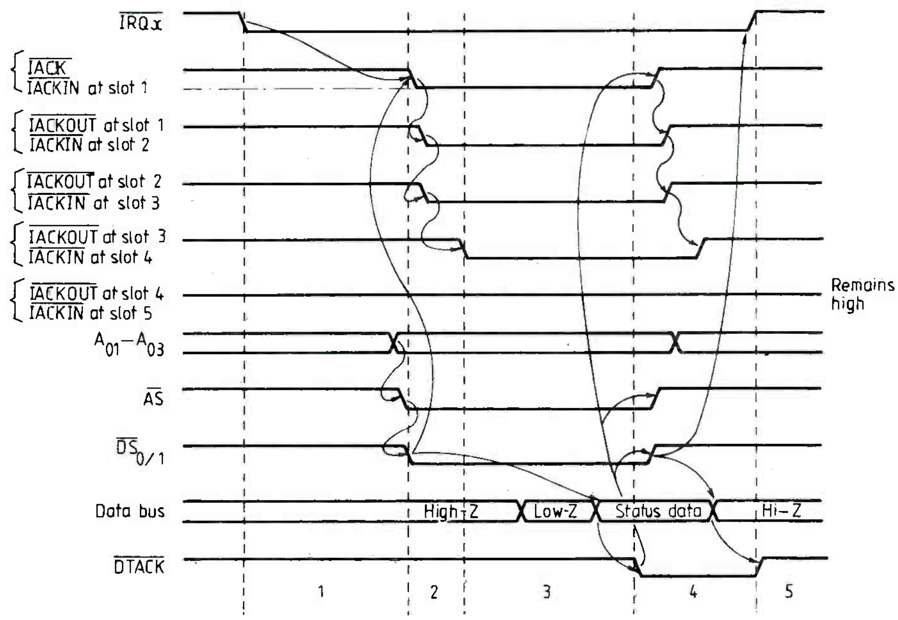


Fig.8,9. A VMEbus interrupter generates request by activating one of the seven prioritized interrupt request lines, $\overline{IRQ_1}$ to $\overline{IRQ_7}$. For each level of interrupt request there must be a corresponding interrupt handler. When a handler receives an interrupt request, it arbitrates for control of the bus, then performs an acknowledge cycle. During the interrupt acknowledge cycle the handler places a code on address lines 1 to 3 corresponding to the level of interrupt request being acknowledged, and drives the ACK line low. At the slot 1 position the IACK lines is routed to the interrupt-ackowledged daisy chain, until it reaches the interrupt that generated the request. This interrupted then compares the code on address lines 1 to 3 to see whether it matches the level at which the request was generated. If it does, the interrupter does not pass the acknowledged signal down the daisy chain, but places a code (status identifier or vector) onto the data bus and drives DTACK low. The interrupt handler responds by reading the code and terminating the interrupt acknowledge cycle.

DATA TRANSFER CONTROL SIGNALS

$BR_{0\text{-}3}$: bus request. Before a master can transfer data on the d.t.b., it must first request and gain control of the bus. A master indicates that it requires control by activating a bus request signal, BR_0 to BR_3. The last is frequently the highest priority bus request, but the priorities of the bus-request signals are determined by the arbiter. For each signal there is a corresponding bus-grant daisy chain; a requester must only use the bus-grant daisy-chain corresponding to the bus-request line which it is using. All other bus-grant daisy chains must be passed on by the requester.

$BG_{0\text{-}3}$/OUT: bus grant 0-3 in/out. The arbiter determines which of the active bus-request signals has the highest priority and grants control accordingly. It indicates the level to which control is being given by driving the corresponding bus-grant daisy chain, of which there are four, one for each of the bus request lines. Each can be thought of as a single line running the length of the backplane, but which is broken at each slot position, the two ends of which are called bus-grant in and bus-grant out. (The end nearest the slot 1 position is the in-connection, and the bus-grant-out signal at any slot will become the bus-grant-in signal at the next slot position to the right.) A requester must only use the bus-grant daisy chain corresponding to the bus request line it is using – all the others must be passed on by the requester.

As the bus-grant lines are broken at each slot position, VMEbus boards that are not capable of operating as bus masters, and therefore do not use the bus-grant daisy chains, must provide some method of passing on the bus-grant signals. Similarly, if a slot position is left vacant, then the bus-grant daisy chains must still be passed to other boards further along the backplane, usually using jumpers on the backplane.

BBSY: bus busy. When a master is granted control of the d.t.b. it signals that it has taken control by driving the BBSY signal low. The master will continue driving this signal low until it releases control of the bus. The arbiter can only grant control if BUSY is high.

BCLR: bus clear. Informs a master currently in control of the d.t.b. that another master (possibly of a higher priority) wishes to take control of the bus.

ter module releases the $\overline{BBSY}$ line; The backplane termination network pulls $\overline{BBSY}$ high and the arbiter module will be able to grant control to another master.

Arbitration algorithms. The arbiter may use one of several algorithms to determine which of the bus request signals has the highest priority. The simplest is the signal level arbiter (SCL), which only accepts bus request signals on $\overline{BR_3}$ and consequently only drives the bus grant-3 daisy-chain. A more popular arbiter is the PRI arbiter, which accepts all four bus requests on a fixed priority, with $\overline{BR_3}$ the highest priority and $\overline{BR_0}$ the lowest. The third type detailed in the VMEbus specification is the round robin select (RRS) arbiter which assigns priorities to the bus requests on a rotating basis, with the level at which the bus was last used having the lowest priority. Although the specification only details three types of arbiter, it is permissible to have an arbiter which uses either a combination of the above algorithms, or a completely different algorithm.

Release of the d.t.b. The requester module determines when control of the d.t.b. will be relinquished. There are two main types of requester module, the difference being the circumstances under which they release control. The first type surrenders control when the master no longer requires the bus (called 'release when done'). The second type maintains control until it sees a bus-request signal become active. RWD requesters are suited to masters that require the bus infrequently, but masters that make frequent use of the d.t.b. will operate more efficiently if they do not have to keep requesting control. This type of master is well suited to the ROR requester, since the ROR requester only releases the bus if another master wishes to take control.

All requester modules, or their masters, may monitor the $\overline{BCLR}$ and/or $\overline{ACFAIL}$ signals and release the bus when they see either of these signals become active.

INTERRUPT HANDLING

The VMEbus specification provides for seven prioritized interrupt request signals. The module that generates an interrupt request is called an interrupter, while the module which receives an request is called an interrupt handler.

A VMEbus system need not use any or all of the interrupt requests. However, for each interrupt request signal used there must be a handler. An interrupt handler may receive interrupt requests on any number and in any combination of the request lines. A VMEbus system may contain several handlers, but there should only be one handler for each request line. The mnemonic IH(x) denotes the request levels to which an interrupt handler can respond, where x is in the range 0-7.

Request and acknowledge. The interrupt request and acknowledge sequence is the same for all of the interrupt requests, but during the interrupt acknowledge cycle the interrupt handler transmits a code corresponding to the level of interrupt request being acknowledged. The basic sequence is:

— Interrupt generates an interrupt request.
— Interrupt handler receives request and requests control of the d.t.b.
— When the handler gains contol it places a three bit code corresponding to the level of the interrupt request onto address lines A_{01}-A_{03}, drives $\overline{IACK}$ low and then drives $\overline{AS}$ low.
— Interrupt handler drives data strobe low to indicate the width of the status data to be read. Handlers read status data as an 8, 16 or 32 bit field.
— The $\overline{IACK}$ daisy chain driver of the slot 1 board detects $\overline{IACKIN}$ low and the data strobe low, then drives its $\overline{IACKOUT}$ signal low (assumming this board is not an interrupter).
— The $\overline{IACK}$ signal propagates down the daisy chain until it reaches the interrupter that caused the interrupt request.
— Interrupter detects a falling edge on its $\overline{IACKIN}$ input and the data strobe low.
— The interrupter checks the three bit code on address lines A_{01}-A_{03} to see if it corresponds to the level at which the interrupter generated the request. If not, the interrupter passes the $\overline{IACK}$ on down the chain by driving its $\overline{IACKOUT}$ output low. If the code corresponds, the interrupter places its status data onto the data bus (assuming the width corresponds to the data width requested) and drives $\overline{DTACK}$ low.
— The handler sees $\overline{DTACK}$ go low and reads the status from the bus, terminates the acknowledge cycle and releases control of the d.t.b.
— The interrupter then releases $\overline{DTACK}$.

Release of request. VMEbus interrupter modules may be designed to release their interrupt request in two ways. Firstly, when the status data is read from the interrupter during the interrupt acknowledge cycle. This type is called a release-on-acknowledge interrupter (roak). And secondly, when a register on-board the interrupter is accessed by a VMEbus master. This type of interrupter is called a release-on-register-access interrupter (rora). Both types must provide status data during an interrupt acknowledge cycle.

INTERRUPT REQUEST SIGNALS

$\overline{IRQ1\text{-}7}$: interrupt request 1-7. The seven interrupt request lines are prioritized with $\overline{IRQ_7}$ having the highest priority and $\overline{IRQ_1}$ the lowest. There is no relationship between interrupt request priorities and bus request priorities.

$\overline{IACK}$: interrupt acknowledge. When an interrupt handler receives a request it must obtain control of the d.t.b. then perform an interrupt acknowledge cycle. This cycle bears similarities to a read cycle, but the handler drives the $\overline{IACK}$ signal low to distinguish the acknowledge for a read cycle.

The $\overline{IACK}$ signal is also used to drive the $\overline{IACK}$ daisy chain, used by interrupter module to determine whether the acknowledge sequence in progress is in response to their interrupt request. The $\overline{IACK}$ daisy chain is driven from the slot 1 position, but as a interrupt handler may be positioned anywhere in the VMEbus backplane, handlers only drive the $\overline{IACK}$ line. At the slot 1 position, the $\overline{IACK}$ line is connected to the $\overline{IACKIN}$ terminal of the P1 connector. The $\overline{IACK}$ daisy-chain is then driven by the system controller board. Thus the $\overline{IACK}$ signal is used to drive the $\overline{IACK}$ daisy-chain.

$\overline{IACKIN/OUT}$: interrupt acknowledge i/o. Two or more interrupters in a VMEbus system can share the same interrupt request line. The $\overline{IACK}$ daisy-chain avoids having more than one interrupter respond to the same acknowledge cycle. As $\overline{IACK}$ propagates down the chain, each interrupter has the opportunity to respond; if it does, it does not pass $\overline{IACK}$ on down the chain. Thus where interrupters share and interrupt request line, the interrupter nearest the slot 1 position will have the highest priority.

The $\overline{IACK}$ daisy chain can be thought of as a single line running the length of the backplane, but which is broken at each slot position, called $\overline{IACKIN}$ and $\overline{IACKOUT}$, (the end nearest slot 1 is the $\overline{IACKIN}$ connection). Thus $\overline{IACKOUT}$ at any slot becomes $\overline{IACKIN}$ at the next slot position.

Since the $\overline{IACK}$ daisy-chain is broken at each slot position, VMEbus boards not capable of operating as interrupters must provide some method of passing on the $\overline{IACK}$ daisy chain. If a slot position is left vacant, the $\overline{IACK}$ daisy chain must still be passed on to other boards further along the backplane usually by using jumpers.

VMEBUS OVERVIEW

To ensure that a VMEbus system is properly initialised the specification provides for a system reset signal, $\overline{SYSRESET}$, activated for a minimum period after power is applied. $\overline{SYSRESET}$ may be activated by any VMEbus board; this enables manual reset facilities to be included in VMEbus systems. There are connections for two fault indicator signals available on backplanes, $\overline{ACFAIL}$ and $\overline{SYSFAIL}$, though VMEbus systems need not drive either. $\overline{ACFAIL}$ indicates an imminent power failure, $\overline{SYSFAIL}$ indicates when a board within a VMEbus system is not able to perform its normal function, either because it has developed a fault or because it it performing an internal operation such as a self-test.

Power supplies detailed in the VMEbus specification allow for +5V, +12V, −12V and a +5V stand-by supply.

Dave Jones has been involved in the design of a variety of commercial and defence-related projects employing analogue digital and microprocessor techniques. He went to High Technology Electronics from IBM in 1985, having graduated from Portsmouth Polytechnic with an honours BSc in electrical and electronic engineering. Most recently he has worked as part of the team behind the first 80286 based VME bus single-board computer.

NEUTRIK Audio Measuring Systems

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THD, IMD and W&F are totally automatic, generated by an internal CPU and controllable via an IEEE 488 BUS.

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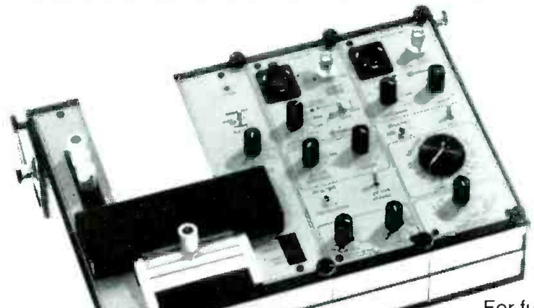
Dimensions:- Main Frame 3302, Input Module 3312 and Output Module 3322:- 30cm (11.75″) wide, 8.5cm (3.33″) high and 21.0cm (8.25″) deep.



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thandar
ELECTRONICS LIMITED

ENTER 19 ON REPLY CARD

Cases and enclosures

Choosing an enclosure may not be the most glamorous job in an engineer's life. But the outer clothing makes an important contribution to a product's appeal and may account for a significant portion of its manufacturing cost. This survey summarizes the product ranges of principal manufacturers and highlights some recent product launches.

Above: the Boss range of enclosures

Alusett

Multi-rack range of computer cabinets based on a skeleton of aluminium extrusions and with panels made of a p.v.c.-covered aluminium-polyethylene sandwich. Custom-designed enclosures can be assembled on request.

Beechcraft

Company specializes in custom-designed polyurethane mouldings for the electronics industry. The Exten range of standard enclosures comes in four basic sizes with two bezel options (upright panel or canted); vent slots are incorporated in the base. Prop-up handles, extra vents, special colours and r.f.i.-shielding paint are among the optional extras.

Boss Industrial Mouldings

Range extends from small die-cast boxes to large Eurocard consoles for computers, keyboards and display panels, with over 250 permutations of size, material and colour. Instrument cases in a.b.s. or a.b.s./metal can be supplied with solid walnut side-panels. Die-cast and a.b.s. boxes incorporate p.c.b. guides and stand-off bosses. One recently-launched range is a series of potting boxes in black a.b.s., in 11 sizes. Standard housings can be prepared to customers' requirements (for example, by pre-punching or modifying existing panels) and special units can be produced to individual specification.

Briticent-Fiskars

Several ranges of sealed enclosures: among them, a polycarbonate type with anti-static and fire-retardant properties approved for use in coal mines. A sealing gasket assures e.m.i. protection. Briticent also offer e.m.i. protection in a separate low-cost range of polycarbonate boxes ready sprayed with a copper-acrylic coating. The EFI range, made of impact-resistant a.b.s., is claimed almost completely resistant to aqueous acids, alkalis and salts.

CCS

Agents for equipment cases, racking systems and card-frames manufactured by Merath-Peltzer in West Germany. Custom design and manufacturing service for all types and sizes of aluminium enclosure in one-off quantities or large volumes; usual turn-round time is six weeks. The company also offers a backplane production and cable harness assembly service.

Daturr

Parent company, Knurr AG of Munich, claims to be one of Europe's largest manufacturers of 19in. equipment enclosures. Two ranges of extruded aluminium racks, Dacobas and Unirack, give many choices of height and depth, with steel or glazed doors and with various accessories and finish options. At lower cost, there is a further series of steel enclosures. A special shielded 19in. enclosure is available in fixed or mobile versions, with various accessories. For mounting electronic instruments or card-frame systems, Mocain cases are available in 2U, 3U, 4U and 6U heights with several widths and depths, in two powder-coated finishes. The company can modify standard products to customers' specifications, with special trim and colour.

Deltron

Enclosure range includes standard aluminium diecast boxes with screw-on lids; two-part heavy-gauge mild steel housings with ventilation slots; a case incorporating two black anodized extrusions for heat-sinking; sloping-front cases; a keyboard case; a robust transformer case with sub-chassis for heavy assemblies; and two two-part steel cases with carrying handles for portable or bench units.

Eldon Electric

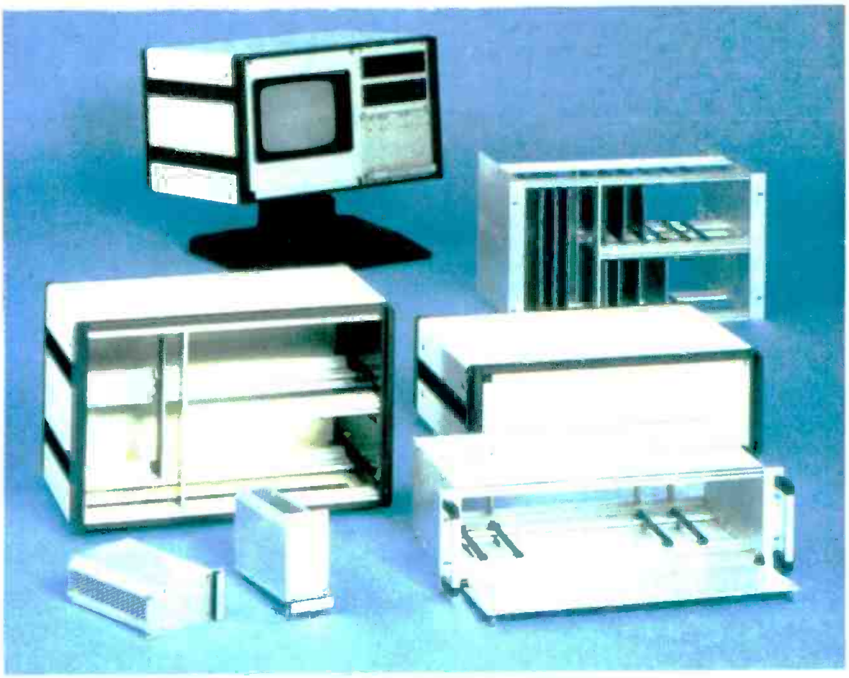
Several ranges of floor-standing and wall-mounting steel enclosures; 19in. swinging frames; control desk. Special enclosures produced to customers' drawings.

Enclosure Technology

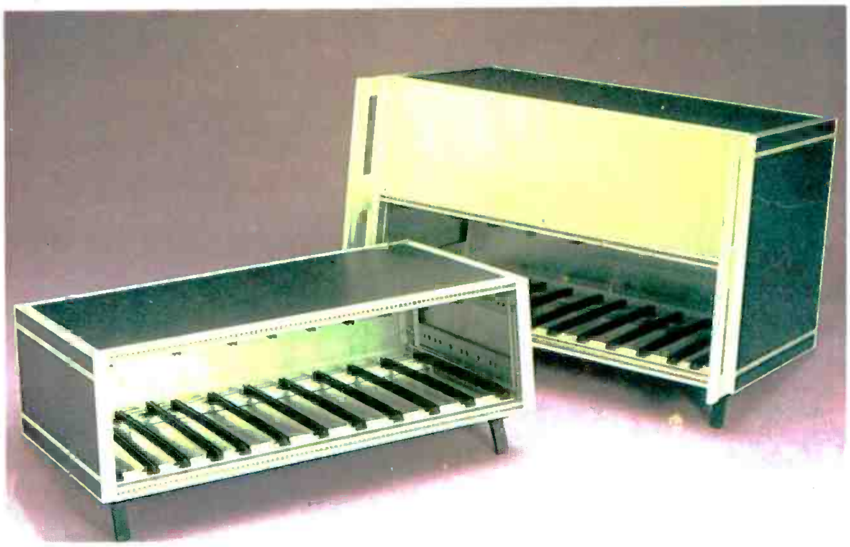
New products include Eurostyle aluminium instrument cases, available from stock in many versions including one for 19in. card-frames and chassis and another for panel-mounted instruments. The Agora cabinet range meets full IEC and DIN specifications; among its features are variable positioning of vertical rack mountings, lockable side-panels, baying options and a wide choice of fittings. Also supplied are the Euronorm sub-rack for anti-vibration applications, the Challenger all-plastic frame; Entel's 1U rack-mounting chassis and 3U 19in. socket chassis; the Synthese range of desks, tables, computer-type cabinets and cases; Ambiance and Technik cabinets; card-frames and guides. Full design consultation and prototype services are offered.

Fischer-Metroplast

Large range of hardware items includes many instrument cases and small boxes with various accessories. Among them are aluminium extruded cases, potting boxes, a two-part plastics hand-held case, ventilated cases, and a variety of 19in. types: frames, cases plates, modules, bus backplanes, aluminium profiles and more. Special sheet metal items can be produced to customer specification.



Daturr's versatile Mocain range, aimed at the OEM sector.



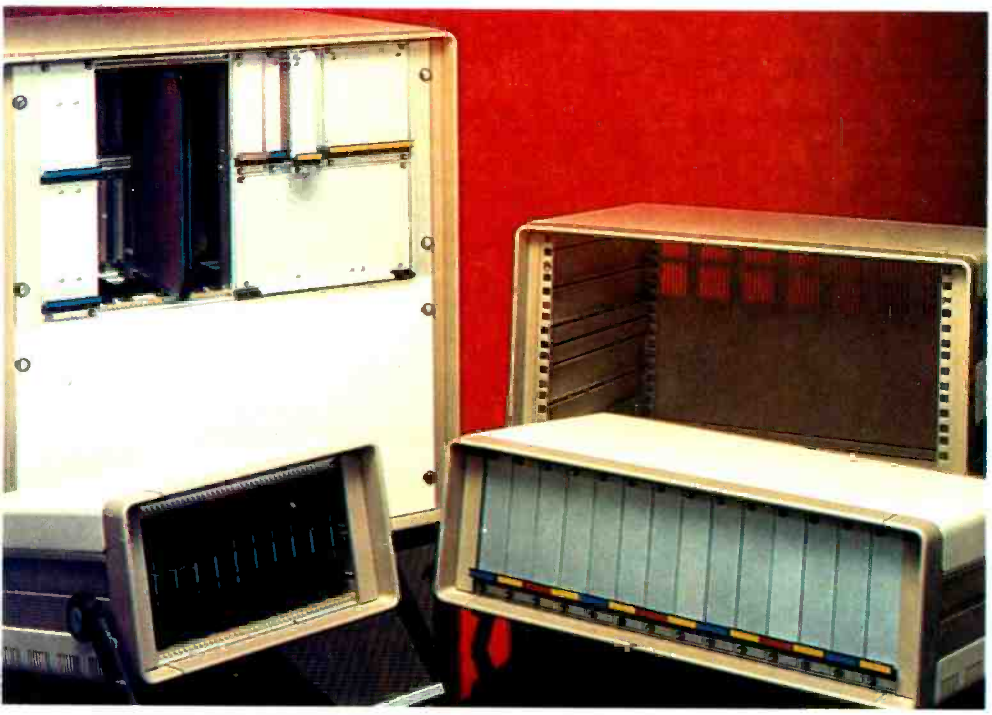
Models from the Motek Eurocard rack series, from Global Specialities.

West Hyde can supply 1100 different cases in over 750 sizes.

Developments in packaging

The business of electronic package – housing electronic systems in cases or enclosures – is becoming increasingly sophisticated.

STEVE HARPER (IMHOF)



The Image case range from Imhof: functional yet attractive.

Although the basic product of the enclosure manufacturer remains – at first glance – a straightforward box, the rapid growth of electronics has radically altered the role of the enclosure. What used to be a passive box can now be a major contributor to system performance on a variety of levels. And in addition to the requirements of performance, the market has demanded that the new generation of enclosures should largely be available as standard items.

To meet this need, the portfolios of today's principal enclosure manufacturers cover a wide range of products, including 19-inch racks, sub-rack systems, many styles of cases in a variety of materials, and a huge selection of accessories vital to application suitability.

Just five years or so ago, case products generally fell into two categories: the utilitarian/functional, easy to take apart and use, but unattractive to look at; and the aesthetically pleasing, which had concealed fixings to give cleaner lines, but which incurred a penalty by being harder to use, and more difficult to assemble and take apart.

Today's standard cases strike a balance between the two. The combination of good looks with functionality has largely been achieved through the use of new materials and by finding ways to conceal fixings while still leaving the electronics easily accessible.

As with enclosures generally, much emphasis has been placed on development standard case products to fulfil particular purposes, and the need for electronics to be wall mounted in a variety of hostile environments has led to the introduction of steel, wallmounted cases sealed to IP54 and IP55 (in accordance with the procedures of British Standard 5490).

To meet the need for larger enclosures in similar environments, sealed versions of free-standing racks sealed to IP66 are also available as standard.

The move of electronic systems into the front office is also reflected in the cases market, with desk top consoles, v.d.u. housings and instrument cases all a standard part of today's enclosure inventory.

Developments on the 19in. enclosure scene have been driven by two basic forces: the adoption of international standard specifications on dimensions, and customer requirement for key performance changes.

An important milestone in achieving standardization came with the adoption of specifications generated by the International Electro-Technical Commission, the British Standards Institution, and the Deutsche Industrie Normen bodies.

These specifications called for the adoption of a 600mm external width for instrument racks, and overall heights from 800mm up to a total of 2200mm in 200mm increments, and depths of 400, 600, 800 and 900mm. Despite metrication, two things remain unchanged: the 19in. panel width, and the height increment of 1¾in. (U). These were so firmly established that they were retained within IEC 297, BS5954, and DIN41494.

European enclosure manufacturers had been working with these dimensions since the late 1960s, but by and large British manufacturers had been slow to conform. The introduction by Imhof in 1979 of its S80-600 range – which conforms fully to these specifications – marked the real beginning of an emphasis on standard product performance.

These developments have brought direct benefits to racking systems users: the extra space provided by the 600mm rack width provides improved facilities for cable runs: power distribution is incorporated into the rear vertical members: and the design allows for infinite adjustment of the panel mounting members within the depth of the rack, even allowing them to be flush with the front face if required.

With the gradual introduction of more IEC based racking systems, a change of emphasis has occurred: many features which had always been available as extras, such as fan trays and integral power distribution facilities, have become standard.

Many recent developments in enclosure technology are attributable to the parallel surge forward taking place in the performance of electronics systems. As developing electronics enable designers to make more powerful and sophisticated systems, they want to concentrate on the capabilities of the system rather than having to spend time considering the packaging implications.

This, in turn, means that the enclosure manufacturer has to take steps to stay ahead of new developments, assess their impact on rack requirements, and refine specifications to take them into account.

Nowhere has this discipline been more clearly demonstrated than in the area of radio frequency interference (r.f.i.) screening. It became obvious that in environments where increasing amounts of complex circuitry were present, problems caused by uncontrolled electro-magnetic radiation in the frequency range up to 10GHz could be severe.

Technical and regulatory pressures, covering all aspects of r.f.i. from car ignition system suppression to telecom equipment, – have given rise to the availability of low cost standard r.f.i. screened enclosures. The techniques used in manufacturing non-standard screen products have been improved to make higher volume production possible at a realistic price.

Global Specialities

Motek range of modular racking systems, including 19in. types, chassis and instrument cases; many to DIN standard. Eurocard rack range, designed to accommodate single and double p.c.bs (mixed, in some versions), is available in a choice of colours and with a wide variety of accessories. Transistek range of extruded aluminium instrument enclosures includes three models in several standard sizes; optional vented top cover.

Hectaphone

Instrument cases in various styles, with a particular emphasis on keyboard-type enclosures for desk terminal units; Eurocard heatsink cases.

Imhof

Large range of electronic enclosures, with particular emphasis in screened types for security in telecommunications and data handling. Prices for the new Imshield 60 r.f.i.-screened modular rack series begin at just £350. Another recently-introduced product is a ruggedized card-frame, available in 19in. widths and capable of accepting all modules and accessories designed for Imhof's Inta-Euro 327 Eurocard sub-rack system. Imhof also market a range of static-protective carrying cases from Hofbauer of West Germany.

IPK (Ian P. Kinloch)

Lightweight aluminium rack-mounting cases with various depths, 1U to 3U high; no constructional fixings are visible on the front panel. Other sizes are available to special order. Prototype service.

J.D.R. Sheetmetal

Steel 19in. rack-mounted cases in 1U, 2U and 3U sizes; removable rear and side panels.

Klippon

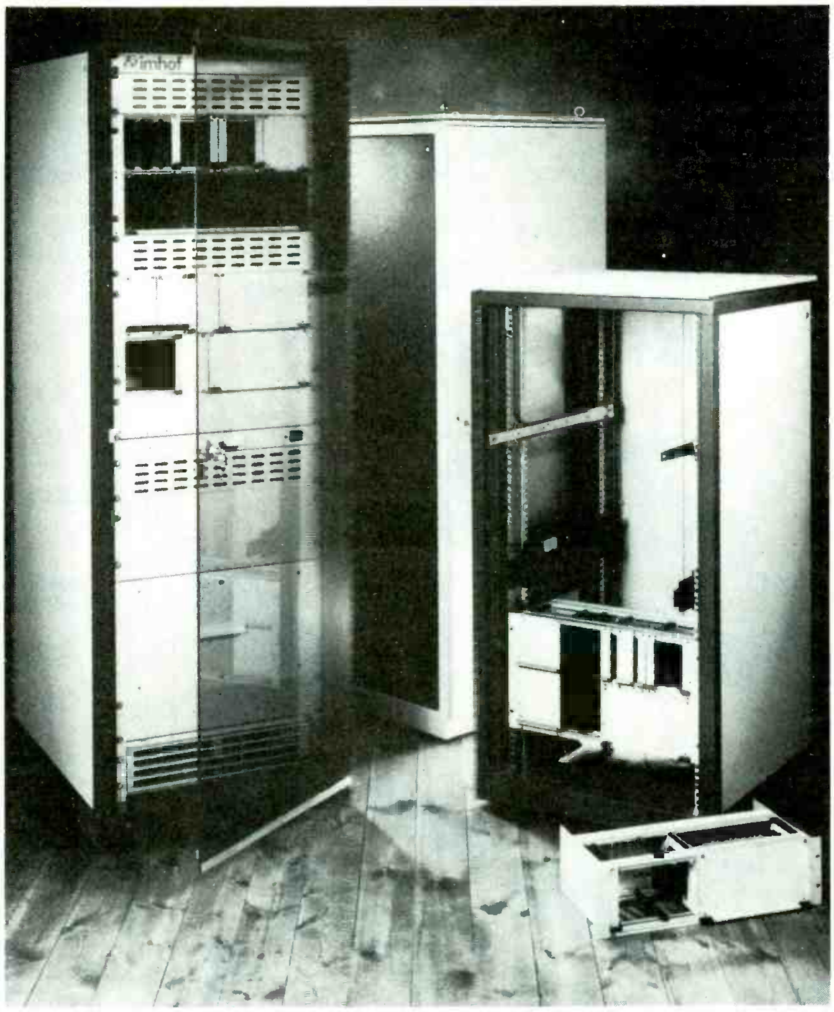
A variety of metal and plastics enclosures: K range of screwed die-cast aluminium boxes for indoor and outdoor use; two ranges of glass-fibre reinforced two-part boxes in polyester or polycarbonate, with clear or transparent lids; M range of glass-filled polycarbonate boxes designed for total insulation, self-extinguishing and capable of withstanding prolonged exposures to temperatures between −40°C and +80°C; hinged boxes in mild or stainless steel; Fibox series of control boxes in impact-resistant polycarbonate, dust and water protected, with p.c.b. slots and with a separate termination compartment; and the Piccolo series of small polycarbonate or a.b.s. enclosures.

Lincoln Binns

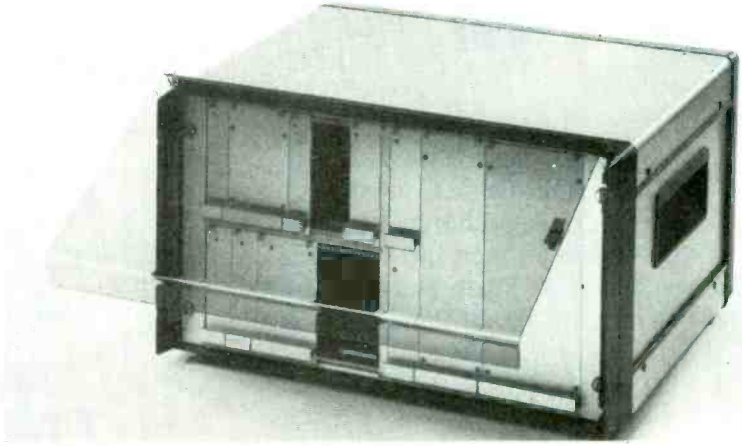
Linc-Ace range of aluminium enclosures based on three standard extrusions with matching end-plates; suitable for p.c.bs from 40×55mm up to 100×220. Sizes interlock with one another, enabling enclosures to be racked together. Accessories include a bracket for power semiconductors which slots into the extrusion for heat-sinking. Prices are comparable to those of die-cast aluminium boxes.

Olson

Numerous types of steel enclosure, including low-cost two-part cases, wall-mounted boxes, small 19in. rack units, drawer case units, consoles and keyboard cases. Finishes are textured acrylic or electrostatic powder epoxy. Non-standard types available by special order.



Above: some 19-inch units manufactured by Imhof.



Schroff's Comptec case is available with this transparent cover.

Rainford Racks

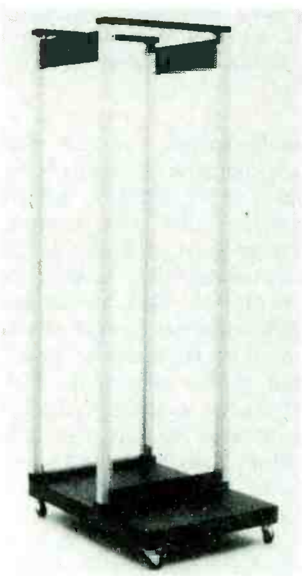
Several ranges of instrument cabinets, racks, cases, desk systems and accessories, including some special types. C65 r.f.i./e.m.i. shielding cabinets are quoted as giving up to 100dB of shielding over the range 10MHz to 1GHz. A range of e.m.p.-protected cabinets gives better than 80dB of protection at 1GHz. The company offers in-house design and testing facilities.

Rider Fenn & Ridgway

Variety of 19in. racks and housings and frames, intended especially for telecommunications applications. Prototype and experimental work undertaken, including precision sheet metal work, production presswork and assembly, paint-spraying and certificated welding.

Cases and enclosures

Reply card		Alumin. boxes	Plastics boxes	Instr. cases	Euro-card	Desk-top	Keyb'd enclo.	Sealed/ shielded	Card frame	19" rack	Control panels	Special types
EWW400	Alusett									▪		▪
EWW401	Beechcraft		▪									▪
EWW402	Boss Ind. Mouldings	▪	▪	▪	▪	▪	▪					
EWW403	Briticent Fiskars		▪					▪				
EWW404	CCS			▪					▪	▪		▪
EWW405	Daturr			▪	▪			▪	▪	▪	▪	
EWW406	Deltron	▪	▪		▪	▪						
EWW407	Eldon									▪	▪	▪
EWW408	Enclosure Technology			▪	▪	▪			▪	▪	▪	▪
EWW409	Fischer-Metroplast	▪	▪	▪	▪				▪	▪		▪
EWW410	Global Specialties		▪	▪	▪	▪			▪	▪	▪	
EWW411	Hectaphone			▪		▪	▪					
EWW412	Imhof	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
EWW413	IPK									▪		▪
EWW414	Klippon	▪	▪					▪				
EWW415	Lincoln-Binns	▪										
EWW416	J.D.R. Sheetmetal									▪		
EWW417	Olson			▪		▪	▪			▪	▪	▪
EWW418	Rainford Racks			▪				▪		▪		
EWW419	RFR									▪		▪
EWW420	Rittal			▪				▪	▪	▪	▪	
EWW421	Rose-Radiatron	▪	▪	▪	▪	▪	▪	▪		▪	▪	
EWW422	Schroff			▪	▪	▪		▪	▪	▪	▪	
EWW423	Sarel		▪	▪				▪		▪	▪	
EWW424	Vero	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	
EWW425	West Hyde	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
EWW426	XIXIN			▪				▪	▪	▪		▪



XIXIN's castor-mounted Labracks are built of aluminium extrusions on a steel base.

Rittal

Extensive ranges of racks and consoles: Rittal claims to be the world's largest manufacturer of standard enclosure systems. The new VR series of IEC 297/2 racks, made in the company's Plymouth factory, is assembled and sprayed to order from standard components, giving short lead-times for what is almost a custom-built product. To satisfy demand from government users and high-technology concerns, Rittal have low-cost e.m.i.-r.f.i. shielded rack which in tests achieved attenuation greater than 100dB. Other products include open-frame laboratory racks, the Uniset series of card-frames and a variety of instrument cases.

Rose-Radiatron

Wide range of standard equipment housings in cast aluminium, polyester and polycarbonate. An arc-sprayed zinc coating process now available gives r.f.i. shielding for plastics housings; and for metal boxes, a new polyurethane sealing gasket is said to maintain protection even after repeated resealing. Among other services offered are drilling, tapping, milling, coating and enamelling.

Sarel

Extensive range of steel industrial enclosures in various sizes and styles, many designed for resistance to unfavourable environments. Other series of enclosures include control desks, aluminium enclosures, 19in. racks and sub-racks. Plastics boxes are available in several styles and materials. These can also be supplied in r.f.i.-shielded versions through an aluminium sputtering process.

Schroff

Comprehensive ranges of modular housings for all types of electronics equipment: racks, sub-racks, industrial cabinets, r.f.i.-shielded enclosures, case systems, housings for v.d.u.s and microcomputer systems, desks and accessories.

Vero

Latest 103-page catalogue embraces a very large range of enclosures of all sorts: 19in. cases and rack systems; wall-mounted cases designed to resist adverse conditions; three types of v.d.u. housing; potting boxes; flip-top plastics cases for portable instruments; battery boxes; instrument cases with and without handles and other fittings; cases with an optional security fixing kit; moulded keyboard enclosures; modem cases; drawer cases; Eurocard systems; and much more.

West Hyde

Company's selection of enclosures is one of the widest in the UK: the 1986-87 catalogue details a range extending from miniature nylon or metal boxes to desk and computer cases, 19in. racks and associated hardware. Materials include aluminium, steel and glass-filled plastics. Among many recent introductions are the Europack VME card-frame; the Internorm range of 19in. rack cases, which won a design award at the Hanover fair; the Combicard system for Eurocard boards in a.b.s.; Palamos moulded enclosures for portable or bench-top instruments; and various panel accessories and fittings. The company claims to have particular expertise in the design and manufacture of card-frames, with a system which has MOD approval for use in environments subject to shock and vibration.

XIXIN

Low-cost cardframe for 160mm and 200mm Eurocards, supplied in kit form in standard 3U and 6U sizes. Labracks range of floor-standing racking designed for all-round access to the installed equipment. Base units are made from 2mm steel pre-punched to allow many different configurations of racking to be added. Recent products include a range of stainless steel enclosures with seam-welded joints and electro-polished finish.

BOOKS

Practical Electronics Microprocessor Handbook, by Ray Coles. Newnes Technical Books, 152 pages 188×245mm, soft covers, £13.50. Software and hardware details of 17 assorted devices from all the major families: four are single-chip processors, six are 16-bit and the rest eight-bit. Useful source of quick-reference data for the technician.

Current Research in Britain: Physical Sciences. British Library, 1196 A4-size pages, soft covers, £50 (by post from the British Library, Boston Spa, Wetherby, West Yorkshire LS23 7BQ; a handling charge of £2.50 is levied on overseas orders). This work is part of a four-volume set which replaces **Research in British Universities, Polytechnics and Colleges** (RBUPC). It lists some 60 000 research projects now being carried out in over 300 centres. Indexing is by institution, department, researcher, study area and keywords. Other volumes cover Biological Sciences (£50), Social Sciences (£38) and Humanities (£30); the complete set of four costs £150.

Space Tech 86: proceedings of a conference held in Geneva in May 1986. Online International Ltd (Pinner Green House, Ash Hill Drive, Pinner, Middlesex HA5 2AE), 249 A-4 pages, soft covers, £65 including postage. Prospects for space stations and other developments in space technology assessed in some 20 contributions by experts from around the world. The communications section includes John Everett of RSRE on paging by satellite; Karen Burt of British Aerospace on communications satellites of the future; NASA on lasers and electronically-hopped beam antennas for its Advanced Communications Technology Satellite; and contributors from the Hughes Corporation on satellite mobile communications. A section on new opportunities in space technology examines robotics and the use of expert systems.

CAD International Directory 1986, compiled by staff of the journal *Computer Aided Design*. Butterworth, 303 pages, hard covers, £30. Survey of products and services available in the fast-developing field of c.a.d. Extensive directory sections give details of c.a.d. software and hardware, consultancies, bureau services, organizations and training centres. Information contributed by the companies themselves through questionnaires is set out in a standard format to allow easy comparison. Introductory articles include a glossary of c.a.d. terms, a review of developments in computer-aided engineering and a look at trends in workstations.

Integrated Circuits and Microprocessors by R.C. Holland (West Glamorgan Institute of Higher Education). Pergamon Press, 200 pages. Soft covers, £9.50; hard covers, £19.50. Text for students, designed to support the electronic and microcomputer sections of courses in electronic engineering. Examines the i.c. buildings blocks of modern circuits, digital and analogue, with exercises and case studies and a glossary. An appendix reproduces data on the t.t.l. range of i.cs (with the same misprint repeated 21 times on its page headings: an apt warning of the hazards of leaving things to machines).

Old Telephones by Andrew Emmerson. Shire Publications Ltd (Shire Album 161), 32 pages, soft cover, £1.25. Enjoyable glance back at nearly a century of wired communications in Britain. In his text and through the many illustrations, the author describes not only the instruments but the whole telephone system and the way it worked. Tip for nostalgia buffs: ancient telephones can still be found decomposing peacefully at the end of private wires in places such as electricity sub-stations and other public utilities.

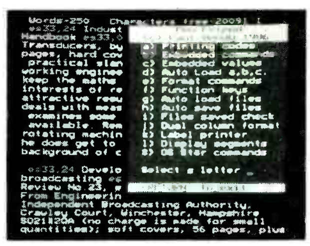
Signal Processor Based Modems Interface Guide. Rockwell International Corporation Semiconductor Products Division, December 1985, order number 685. Thick A4-size loose-leaf volume containing data and extensive application notes on the company's modem devices, cards and other products.

Microwave Field-Effect Transistors: Theory, Design and Applications, by Raymond S. Pengelly, second edition. Research Studies Press, John Wiley and Sons, 636 pages, hard covers £62.80. Comprehensive introduction to the theory and practice of microwave fets, gallium arsenide devices especially. Sections deal with device theory for small-signal and power devices, fabrication techniques, amplifier design, mixers, oscillators and integrated circuits. An especially interesting chapter examines a variety of novel fet circuits, among which are r.f. switches, phase-shifters, frequency discriminators, an osciplier, pulse multipliers and integrated optoelectronic circuits.

SOFTWARE

Digital Electronics: a computer-aided course (for secondary schools, ITECs etc.). Unit 1: Coding Information, by R.A. Sparkes (University of Stirling). Booklet (23 pages) and disc for BBC Microcomputer, Addison Wesley Publishers, £14.95 + v.a.t. Analogue quantities, digital data and the principles of combining the two are introduced by the booklet with the help of many diagrams and self-assessment questions. But the software fails to reach the same standard of presentation and interest value. Instead of expanding and developing the themes in the printed text, the four programs on the disc (in all, a bare 12K of Basic) are no more than brief illustrations of a few of the teaching points.

Secondary Science Microtechnology: BBC Soft, produced in association with the Microelectronics Education Programme. Cassette for the BBC Microcomputer, transferrable to disc, £8.25. An Ohm's Law tutor, logic tutors (very taxing), flip-flop tutor, servo simulation and a simple circuit-diagram drawing utility, intended for A-level and CSE students. Well-designed software, interesting to use and a bargain at the price. Unfortunately, the software protection (unusual in a BBC title) prevents it from running on the Master computer or even on the Model B when fitted with a non-standard DFS.



PenFriend: word-processor utilities in rom for the BBC Micro. Word Processing (0902-788207), P.O. Box 67, Wolverhampton, West Midlands; £14.95 inclusive. For users of the popular Wordwise Plus word-processor, this rom provides page-formatting, filing and other features through convenient drop-down menus. Suitable for both Model B and Master 128 computers, though it will not work across the Tube. A customization service is available.

Text-to-speech rom for BBC Microcomputer: Computer Concepts (0442-63933), £39.90 together with the complementary Speech Rom, or £11.50 as an upgrade to it. Enables the computer to speak almost any information you can get into or out of it: keyboard or RS423 input, printer output, disc files, text on the screen or blocks of hex data in memory. The articulation lacks *legato* and words can be hard to grasp at first hearing; but, among other applications, the package could be a wonderful help for the visually-handicapped computer user.

Two-dimensional Fourier transforms

As far as we know this is the only implementation of multidimensional signal processing concepts on a microcomputer of BBC proportions.

WEYSEL OMER

Appending the discussion on computing Fourier transforms, this article describes a means for the transformation of two-dimensional data for the BBC microcomputer, based on the FFT implementation detailed in the June and July issues of this journal. Applications relate extensively to image processing and to 2D systems frequency domain analysis.

To process multidimensional signals using the Fourier transform, the general interpretation of the classical equations expressing it has to be modified somewhat. Consider the substitution of a spatial variable, x in place of t, and the substitution of a spatial frequency variable, u in place of f. In the expression for the continuous complete frequency spectrum (equations 1&2). The perspective of the analysis is altered from a signal varying in time to a signal varying in space. An image is an example of a two-dimensional function which varies in the planes of two spatial variables: its continuous Fourier transform is obtained by evaluating equation 3.

DISCRETE TRANSFORMS

The image g(x,y) is a function whose instantaneous amplitude is related to the brightness at the point x,y as on a monochrome display. For all but the very simplest of images (e.g. a white square on black background), the solution of equation 3 is impossible. As in the case with the one-dimensional Fourier transform, the function can be sampled and quantized at discrete values of x and y (as shown in Fig.1 for N=8), and a general discrete form equation 3 applied – the two-dimensional discrete Fourier transform (2DFT), equation 4. It can easily be shown that it decomposes into two successive applications of 1DFTs as equations 5 & 6. Hence, the solution of the discrete form (4) first requires the computation of G(u,y) corresponding to the 1DFTs of N rows in the image, g(x,y). The overall results are obtained from the solution of equation 5 i.e. the DFTs of the columns of G(u,y).

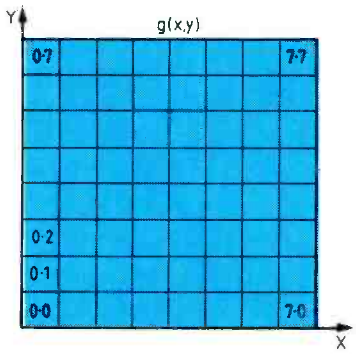
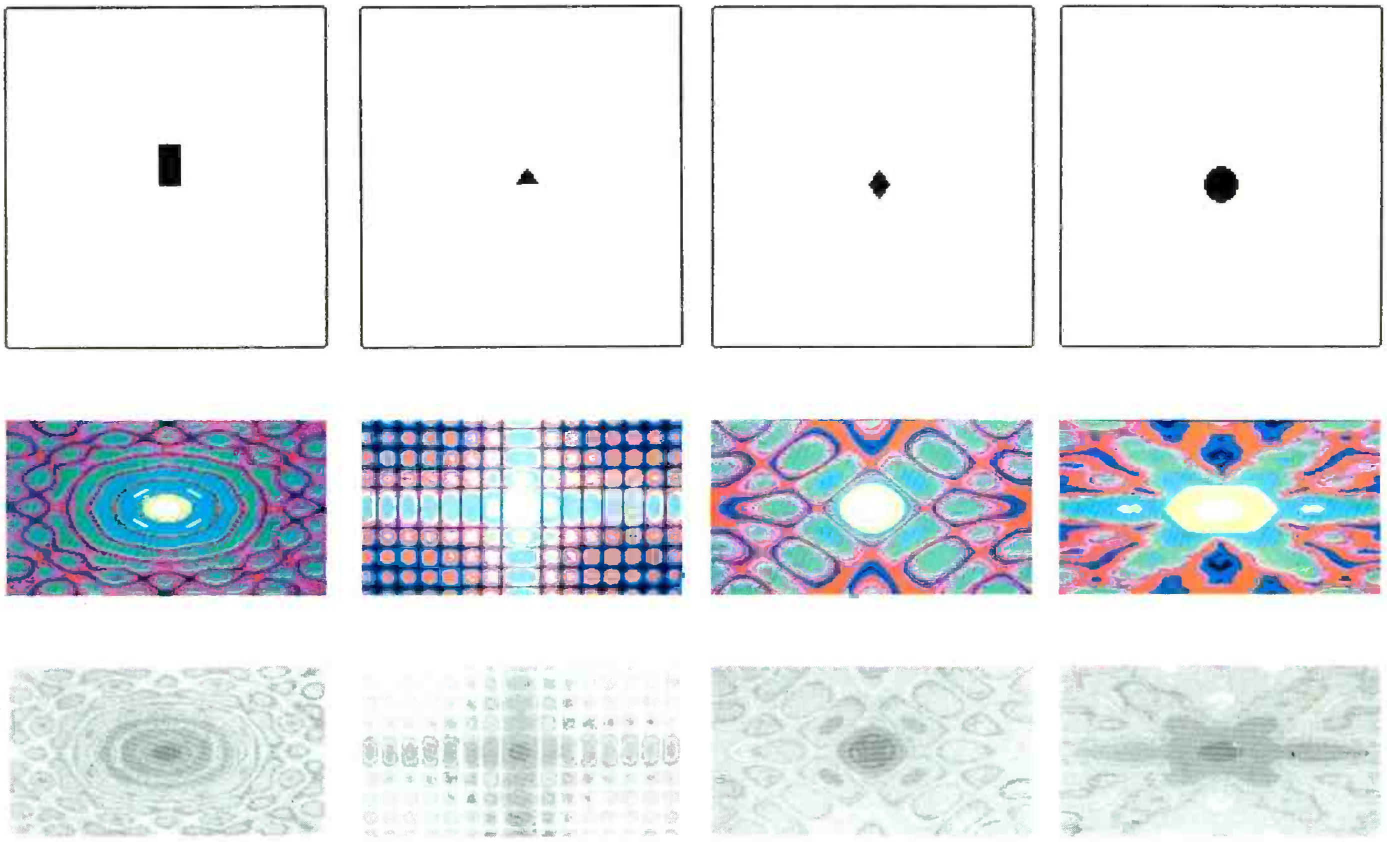


Fig.1. Representation of a digital image in matrix form with each picture element defined as a coordinate in the matrix.

IMPLEMENTATION

The FFT alogrithm was incorporated to compute equations 5 & 6 for N=128 i.e. an image of 128 by 128 picture elements. The



Two-dimensional Fourier transformations obtain the spectral content of image scenes. Transformations of simple shapes shown in psuedo-colour form give the grey-scale effect shown when viewed on a black and white monitor.

form of g(x,y) was that of a binary image (black and white only), placed in a defined window in the BBC mode 4 screen. Row transforms are computed and the results stored in a file on disc. Due to inherent data transfer problems in obtaining column elements on disc-based systems, it is necessary to transpose the matrix corresponding to G(u,y) so that the file is stored columnwise. Results of the DFTs of the columns (using the FFT) are then stored back in the original files as G(u,v).

The form of the 2D results are complex and therefore a choice of representations is available. This implementation uses the energy function, defined as

$$E(u,v)=Re^2(u,v)+Im^2(u,v).$$

This is computed for each row of G(u,v) and stored in the same disc file as E(u,v). To analyse visually the 2D Fourier transform results which appear themselves as 3D, the mode 2 colour screen of the BBC was utilised. A window of 128 by 128 colour elements allows the representation of E(u,v) as a 'plan view', where each element corresponds to a frequency harmonic whose amplitude is colour coded. The code is chosen so that the relative amplitudes appear on a grey scale when viewed on a monochrome display: highest amplitudes appear white, lowest black, and mid values, a relative grey. Examples of transformed images are shown.

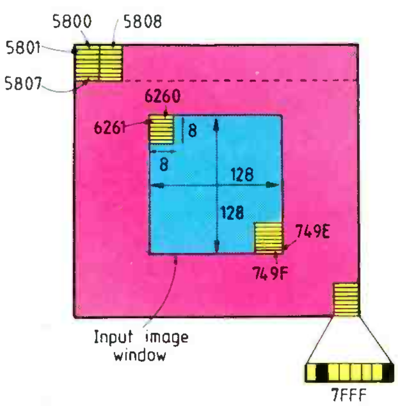


Fig.2. Boundaries of the window within which an input image must be positioned in the BBC mode 4 screen memory.

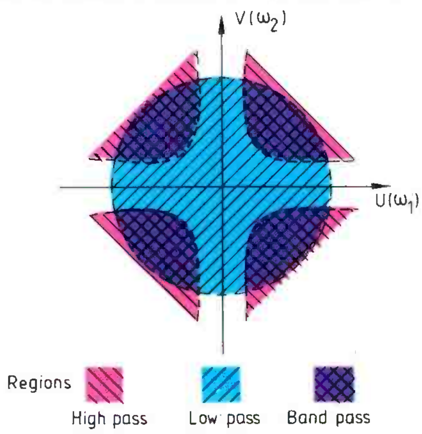


Fig.3. Low-pass, high-pass and bandpass regions in a frequency domain transformation, with the mean brightness level of the original image given by the amplitude for the central (d.c.) component.

USING THE ROUTINE

Firstly, the input routine to the program presented was arranged to process binary (mode 4) images; significant alterations would be necessary to transform grey-scaled images. The routine, although written entirely in machine language, executes in around 45 minutes and necessitates a disc

LISTING

```
10 MODE 4
20 FOR I=&62E0 TO &76D7 STEP &140:!I=&80808080
:!(I+4)=&80808080:NEXT
30 FOR I=&6258 TO &7657 STEP&140:!I=&01010101:
!(I+4)=&01010101:NEXT
40 FOR I=&7660 TO &76DF STEP8:?I=255:NEXT
50 FOR I=&6127 TO &61A6 STEP8:?I=255:NEXT
```

arrangement able to accommodate a 128K data file.

The 2DFT is loaded with *LOAD "F" which is an assembled 4K object file which must be loaded prior to each image transformation. The following should then be carried out to perform a transform.

- Initialize the mode 4 screen and establish a binary image (by a high-level language program or via a vision system) within the bounds of the spatial domain window defined in Fig.2. The listing above generates a frame defining the window and if the image is software generated, the relevant program steps could be included in the same program.
- Load (formatted) disc capable of holding a file of 128K. 'FFT.DAT' as this is the generated transform filename and would thus overwrite previously stored data. It follows that the results of only one transform can be stored on one disc.
- Begin transformation by typing CALL&1C3E.

After approximately 45 minutes, a file containing the 2D Fourier coefficients has been created. The colour encoding display routine executes automatically, plotting a white screen since threshold registers are initally cleared. These may be set using a program as follows:

```
10 !&2200=150000000
20 !&2204=10000000
30 !&2208=1000000
40 !&220C=100000
50 !&2210=55000
60 !&2214=8000
70 !&2218=300
```

This may be saved on the same disc as the image transform file. The levels, which initiate amplitudes of the grey-level scaling, may be varied appropriately to obtain the required colour definition in the frequency domain image. After execution of the above threshold initialisation, the display routine may be called with CALL&1CCA.

The register contents may be altered and the display routine executed until a satisfactory result is obtained whereupon the frequency domain image may be screen-dumped or saved on disc.

APPLICATION

The interpretation of transforms in terms of the 2D frequency spectrum is given in Fig.3. The presence of sharp points or corners in the input image manifests itself as significant high frequency components in the Fourier domain. Any periodicity which may not be discernible in the original image, is easily detected once transformed. Statistics relating to an image may also be readily obtained, i.e. average intensity. Removal of blurring in an image of enhancement of certain features may be achieved via filtering and reconstruction using the inverse transform. Current uses of 2DFTs are in such areas as Landsat image analysis, magnetic resonance imaging, Fourier optics and filter design. However, real-time image analysis (pattern recognition) for use in such applications as robotic vision systems is served by 1D transforms on edge-detected boundaries of objects in view. Such classification is obtained by the use of Fourier descriptors and Hough transforms (see Pratt) besides others.

Equations

The equation

$$G(f)=\int_{-\infty}^{\infty} g(t).\exp(-j2\pi ft)dt \qquad (1)$$

obtains the continuous complex frequency spectrum G(f) from the time function g(t). Substitute spatial variable x in place of t and u in place of f:

$$G(u)=\int_{-\infty}^{\infty} g(x).\exp(-j2\pi fx)dx \qquad (2)$$

For a two-dimensional function the continuous Fourier transform is obtained by evaluating

$$G(u,v)=\iint_{-\infty}^{\infty} g(x,y).\exp[(-j2\pi(ux+vy)]dx\,dy \qquad (3)$$

The general discrete form of (3) is

$$G(u,v)=\sum_{x=0}^{N-1}\sum_{y=0}^{N-1} g(x,y).\exp[-j2\pi(ux+vy)/N] \qquad (4)$$

where u,v=0,1,2 . . . N−1, which decomposes into

$$G(u,v)=\frac{1}{N}\sum_{y=0}^{N-1} G(u,y).\exp(-j2\pi vy/N) \qquad (5)$$

and

$$G(u,y)=N\left[\frac{1}{N}\sum_{x=0}^{N-1} g(x,y).\exp(-j2\pi ux/N)\right] \qquad (6)$$

Further reading

Digital Image Processing, by R.C. Gonzalez and P. Wintz, Addison-Wesley.
Digital Image Processing, by W.K. Pratt, Wiley.
Multidimensional Digital Signal Processing, by D.E. Dudgeon and R.M. Mersereau, Prentice Hall.
Digital Signal Processing, edited by N.B. Jones, Peter Peregrinus.

Weysel Omer graduated from Brighton Polytechnic earlier this year and is engaged on a PhD programme in the 'engineering applied to medicine' group at Imperial College, London University. This article, along with his previous ones in the June, July 1986 issues, constitutes part of his final year undergraduate project supervised by Graeme Awcock.

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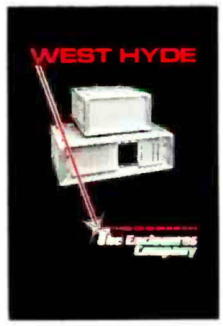

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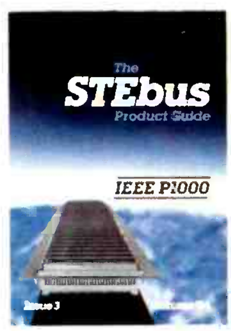

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Hands-on engineers

A plea for a return to basic thinking and to career engineering in the UK.

R.E. YOUNG

Anyone following the depressing reports and comments on the British economy, specifically as seen in British engineering as a whole, might well be forgiven for thinking that the country had moved out of modern technology altogether.

Thus in an article with a strong software bias it is suggested that British industry is so far behind its competitors in the application of robotics and computer-based techniques generally that it has very little real future left.

Even R&D is not immune. The United Kingdom is quoted as having "...just about the worst performance (record) in research and development compared with out competitors in the Western world."*

Clearly, these are extreme views and do not represent the full picture but, equally clearly, there is some foundation for them (one has only to look at the trade figures to see something of this). Also, it has to be admitted that it is only recently that counter arguments have started to appear in print, while a further admission is that much of the information has to be inferred (is indirect).

Nevertheless, it is in these recent utterances that a major element in the rebuttal lies, viz. education, where 'education' is used in its widest sense, extending from primary schooling to high-level apprenticeship and beyond. It is in this connection that the term 'hands-on experience' takes on a special significance in being used, in effect, as the subject heading for examination of the ways in which suitable candidates could be attracted into engineering as a profession.

The consequent implication is that there is a requirement for more engineers to be brought into the profession which, in turn, means that there are organizations in the UK who continue to see a future for engineering in this country, and furthermore would appear to be carrying out future planning on this basis. Much the same conclusions are reached in an article 'A scarcity of young talent stunts hi-tech expansion' (Edward Fennell, *Daily Telegraph*, June 17, 1986).

Taken in the light of the opening examples, the climate has indeed changed; and the stage has been reached where 'next steps' should be considered.

Briefly, the introduction of the term 'hand-on' means that, contrary to the conventional management approach, the thinking now is that engineers should have had lengthy shop-floor experience with working plant and equipment. To gauge the extent of this requirement for experience, it is not out of place to consider the procedure adopted by the medical profession, where an initial 'bedside' period of seven years is undertaken by everybody, including those intending to become specialists, and for the latter is followed by a further seven year's training. There is a parallel here and the salient point emerges that the building-up of a managing engineer's career demands that at least the classical seven years should be spent under apprenticeship conditions; and that this should be made completely clear in the process of attracting engineers into the profession.

This leads to the question of the image of engineering presented to the outside world. It has become apparent that there is a need for the presentation of the case for British Engineering, with its image having virtually disappeared as the result largely of the emergence of the generic term high technology. This disappearance can be seen to have been inevitable, and coincided with the spread of the computer. It all forms part of a general picture where it is accepted by many (quite understandably) that technical life has become so complicated that no single individual, or even group, can possibly comprehend or manage a modern large-scale technological project. This is, in effect, the acceptance of the principle of subordination to the specialist; and, in practical terms, to the establishment of watertight-compartment-type organizations with all their attendant disadvantages.

Not everybody will agree with this reading of the position, but with all deference, it is suggested that much of the air can be cleared by defining 'high-technology' as 'advanced engineering permeated by electronics' which in relation to the British case means that the UK has been 'in' high technology from the beginning and does not have to catch up from an impossible starting point. Extending the definition to 'advanced system engineering permeated by electronics' shows that Britain has not only had a high-technology presence for so long but has been in the lead in many of the major system advances such as in computer-based process, power generation and control.

Thus, even from this brief outline, it becomes apparent that the experience and technical ability available in the United Kingdom are still more than sufficient for an international-scale contribution to be made. This view can be reinforced by pointing out that the British power to invent is still regarded as unequalled. The importance of this power of invention lies in two main areas in the present context: the strength offered to project work by the adaptability and flexibility of thinking that comes with invention, and the ability to produce sub- and minor inventions which are so vital to development in an R&D programme. That this represents only one element in such a programme highlights the need for understanding (in the full sense of the word) coordination and direction of the whole project, that is, it brings out the magnitude of the task awaiting the managing engineer concerned.

This can be given form by using illustrations expressed in working language of some of the key principles involved. One outstanding issue arises with the need to make the maximum use of past experience in a new project and its conflict with the unknowns of the new. With a sufficient spread of experience and knowledge it is possible to decide when to analogize and when to start up new research; but this does demand informed technical judgement of a high order. In much the same vein, but at a somewhat different level, comes the need to determine when to go to the computer and when to use a pencil and the back of an envelope. (This is not original; although stemming from experience, it has appeared in print in serious discussion.)

Another aspect which should be brought in here is that references are beginning to return to "The computer being only as good as the information fed into it" – computer cognoscenti have a less elegant way of putting it.

The magnitude of the task awaiting the managing engineer at the head of a project has already been stressed. This can be taken further in stating that one of his main concerns is to ensure that the masses of data

continued on page 50

* Lord Gregson, president of the Parliamentary and Scientific Committee. *Daily Telegraph*, July 5, 1986.

Development of the caesium clock as a practical instrument led in 1971 to an experiment to verify Einstein's prediction of the "dilation of time", and its successful outcome helped to clarify certain aspects of interpretation in relativity theory. But a question remains: one prediction by Einstein concerning the relative rates of polar and equatorial clocks – has not been borne out in practice. It seems that the explanation which was originally put forward to account for this failure itself contains a flaw, so that the topic now requires a further round of attention from physicists and philosophers.

"If you want to know the time..."

The clocks-around-the-world experiment of 1971 finally confirmed the "dilation of time" of relativity theory – or did it?

W.A. SCOTT MURRAY

Ever since that statement was first published, in the famous paper which launched Einstein's special theory of relativity, scientific opinion has remained divided as to whether its burden was either meaningful or true. Among those who have questioned it may be cited Lord Rutherford (who said in jest that Anglo-Saxons had too much sense to understand it), Herbert Dingle[2] (himself a well-known supporter of the theory, turned renegade), and Louis Essen[3] (a world-renowned authority on the practical definition and measurement of time). Among those who have accepted it without question must be listed every convinced Relativist, past and present, bar none. Such overwhelming preponderance of talented opinion in its favour could not be gainsaid, were it not that the statement seems to contradict a premise of Einstein's own theory – the Principle of Relativity. Theory suggests that the clock on the equator may equally well be taken to be the clock "at rest", so that the polar clock must run slower than the equatorial clock by exactly the same amount.

This is one of several criticisms of relativity theory about which argument has persisted for some eighty years, and with good reason. Defence of the statement has taken on many forms: that Einstein was speaking figuratively and did not intend what he had written down so clearly in that paper to be interpreted in a literal sense; or that Einstein's result was correct but for the wrong reason, in that the example he gave referred to a rotating earth and hence required the *general theory* of relativity for its proper explanation; or, circularly, that since every physical test performed to date has confirmed the truth of the Special Relativity theory this example must also be true, and if we find it illogical – a "paradox" – it must be because we have failed to understand the theory properly: *"Only paranoics question Relativity"!*

> **"... If one of two synchronous clocks at A is moved in a closed curve with constant velocity v until it returns to A, the journey lasting t seconds, then by the clock which has remained at rest the travelled clock on its arrival at A will be $\frac{1}{2}tv^2/c^2$ seconds slow. Thence we conclude that a balance-clock at the equator must go more slowly by a very small amount than a precisely similar clock situated at one of the poles under otherwise identical conditions."**
>
> **Albert Einstein, 1905[1]**

It will also be claimed by cognoscenti that Einstein's statement has been proved by direct experimental measurement. Let us therefore examine the basis of that claim in detail.

HAFELE AND KEATINGS EXPERIMENT

By the year 1971 the new caesium-beam 'atomic' clock (our modern international standard of time) had been sufficiently developed to be called 'portable', to the extent that it could maintain an intrinsic accuracy of a few nanoseconds per day in the environment of a jet airliner. Accordingly, J.C. Hafele of the Washington University at St Louis, Missouri and Richard E. Keating of the US Naval Observatory in Washington, DC co-operated in an experiment[4] designed to measure the timekeeping performance of travelling clocks, in a direct observation of Einstein's "dilation of time".

A standard mean time was maintained on the ground at the observatory; four caesium clocks circumnavigated the world, first to the eastward and then to the westward. Having allowed for times spent on the ground, for courses and speeds actually flown, and for the effects of the change of the gravitational potential with altitude (in accord with the *general* relativity theory), the experimenters calculated that the westbound clocks should show a net gain of time, relative to the "fixed" time standard in Washington, of about 250 to 300 ns over the whole trip. By contrast, due to the approximate balancing of the two effects (motion and gravitation), the eastbound clocks should just about break even on completion. That was their theoretical prediction and, within the accuracy of their estimations of flight path, it was what they actually observed.

In the face of what seemed to them a magnificently clear-cut demonstration of the correctness of *both of* the relativity theories, it was difficult for the relativists to understand why the Hafele-Keating result did not immediately convince all scientists once-and-for-all of the truth of the relatively concept. But between the scepticism of the physicists on the one hand and the condescension of the mathematicians on the other, conditions for even discussing such difficult ideas have always been far from ideal.

The dissent of the non-relativists in this case might perhaps be put into words as follows:

According to Einstein's special theory the Principle of Relativity is paramount: that is, every observer in uniform motion is equally entitled to declare that his own local environmental system is at rest. In what way, then, do the clocks at the US Naval Observatory differ from those in the aircraft? If the westbound aircraft is moving westward at velocity v relative to the observatory, then so also is the observatory moving eastward at velocity v relative to that aircraft. Surely this must mean that each clock must run more slowly than the other – the well-known paradox?

What you have declared in your calculations is that because of the rotation of the earth *your eastbound clock is travelling* *fastest, at velocity $\Omega r + u$, the Naval Observatory is slower, at velocity $v = \Omega r$, and the westbound clock is slower still, at velocity $\Omega r - u$.* From this you claim to deduce, by Einstein's theories, that the eastbound clock will run slower than the observatory clock, while the westbond clock will run faster.* But measured relative to the observatory *the aircraft's speeds are the same, so that the proportional slowing of their clocks should also be the same, namely $\delta t/t = -\frac{1}{2}u^2/c^2$: differential time loss is zero.*

By assigning different absolute speeds to the two aircraft, as you have done, you have allowed one particular reference frame (that is, the frame which is at rest relative to the geocentre) to be preferred for this purpose over, for example, that of the Naval Observatory. If your experimental result agrees with your assumption of the existence of this preferred standard of rest – and it seems that it has done so – then it must deny Einstein's first postulate, the Principle of Relativity.

Far from demonstrating support for Einstein's theory therefore, as you intended it should, your experiment has in fact served to disprove its premise and hence the theory itself.

The experimenters had foreseen that particular criticism, and had taken care to forestall it by inserting the following sentences into their experimental report[5]:

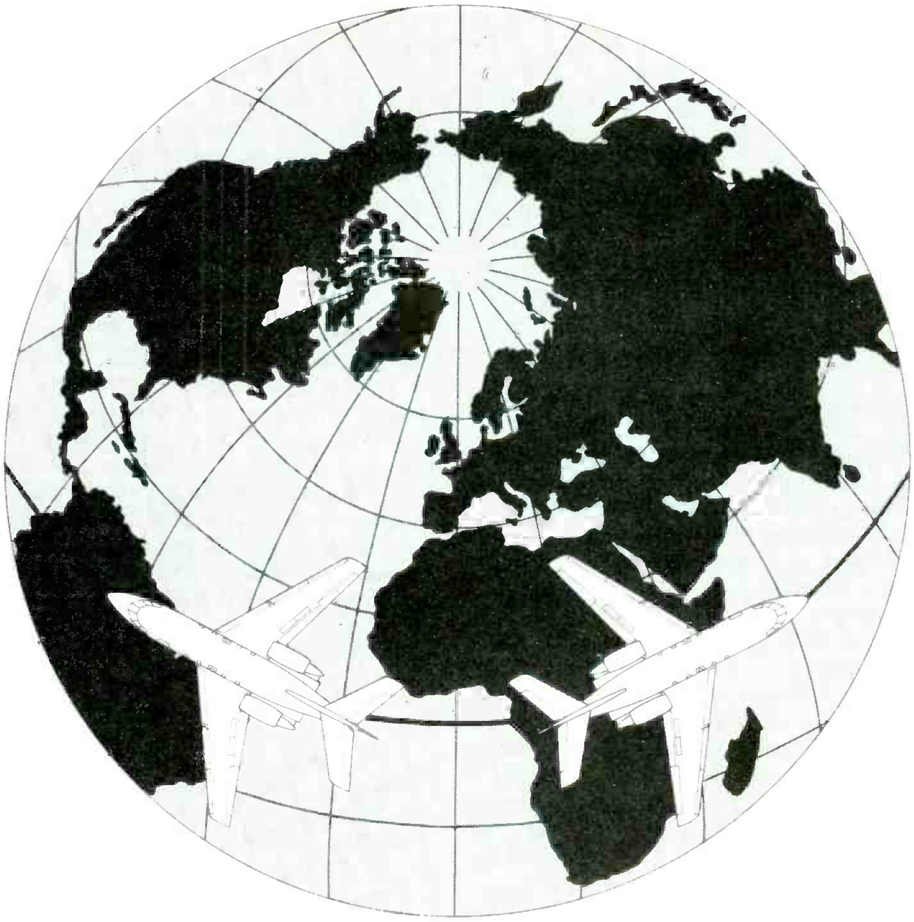
> "Because the earth rotates, standard clocks distributed at rest on the surface are not suitable in this case as candidates for coordiante clocks of an inertial space. Nevertheless, the relative timekeeping behaviour of terrestrial clocks can be evaluated by reference to hypothetical coordinate clocks of an underlying nonrotating (inertial) space."

– and again, as a footnote[6]

> "It is important to emphasise that special relativity purports to describe certain physical phenomena only relative to (or from the point of view of) inertial reference systems, and the speed of a clock relative to one of these systems determines its timekeeping behaviour (G. Builder, 1958)."

Although couched in esoteric, 'relativistic' jargon, what is being said here is extremely important because it proposes a re-interpretation of one aspect of special relativity which it suggests has been universally misunderstood. Paraphrased, it says that an *observer* must be "at rest relative to an inertial frame of reference" (i.e. unaccelerated himself) if the explanations of the physical observations are to be meaningful; *but not such restriction applies to the phenomenon being observed* – which might legitimately be an electron orbiting inside a hydrogen atom at about 10^{15} revolutions per second, or a muon travelling at over 99% of the speed of light and under enormous centripetal acceleration in a storage ring at CERN,[7] or a clock airborne in a Boeing 707. *And there is no need for any second "observer" to be involved: this Relativity is not reciprocal.*

By these criteria the relativistic equations



(the Lorentz transformations) do not require that there should be any symmetry between an observer's laboratory clock and the clocks of the muons that he may be examining. Reciprocity of time-keeping is to apply only between observers *both of whom* are moving inertially, and one of the three observers in Hafele and Keating's experiment was truly inertial. It seems to be *inertial* motion, not *relative* motion, that is now important. It is easily shown by this argument that any other 'inertial observer' – one situated above the north pole, say moving axially away from the earth at a constant, inertial velocity – will observe exactly the same time differences between the experimental clocks as would an observer who was "stationary" at the pole itself or, hypothetically, at the geocentre. But an earthbound observer, it seems, will see something different.

In summary, any technician who tries to compare the rates of clocks at the US Naval Observatory, Washington, DC with others at the Royal Greewich Observatory, Herstmonceux, or for that matter at the National Physical Laboratory in Teddington, is going to get a wrong answer.

FURTHER DISCUSSION: SOME CONSEQUENCES

The Hafele-Keating-Builder argument provides an answer to Dingle's 1967 question[8], which until now has gone unanswered. Dingle had quoted Einstein's statement (at the head of this article) and asked: "What entitled Einstein to conclude *from his [special relativity] theory* that the equatorial, and not the polar, clock worked the more slowly?" The answer, it now seems, is that it is only the 'fixed' (inertial) observer – at the pole – who is entitled to hold a valid opinion

HAFELE-KEATING-BUILDER RULES OF RELATIVITY

○ Estimates and observations of the behaviour of time as measured by clocks are valid only when referred to some real or hypothetical *inertial* (unaccelerated) frame of reference.
○ Clock readings estimated or observed from different inertial reference frames will differ as between each other, but all will be equally valid ('relativity of simultaniety').
○ If v is the velocity of any clock relative to any inertial reference frame K, then the rate of that clock as observed from K will be $\delta t/t = -\frac{1}{2}v^2/c^2$.
○ The rate of any clock depends directly upon the gravitational potential at the location of the clock.
○ If V is the difference between the gravitational potentials at the locations of any clock and any reference point Q, then the rate of that clock as observed from Q will be $\delta t/t = +V/c^2$.
○ No restriction of any kind is placed on the motion of the clock whose behaviour is being observed; and in particular the *acceleration* of an ideal clock, whether caused by graviational or local mechanical forces, has no effect on its timekeeping behaviour.
○ The effects of relative velocity (v) and relative gravitational potential (V) on timekeeping are simply additive. If either or both of V and v should vary during the observing period their overall effects on timekeeping are to be obtained by integration.

* Ω is earth's angular velocity, r is earth's radius, and u is speed of the aircraft over the earth's surface, assumed to be along the equator in this example: Ω = 465.1 m/s u ≈ 220 m/s.

about the physical fact of the relative rates of the clocks. Any observer whose state is not 'inertial' within a necessary degree of precision must automatically come to some erroneous conclusion. It would seem that the earlier argument, that the rotating earth is not an "inertial reference system" within the restrictions of the special relativity theory, was correct.

At the same time it is worth noting that the clock-slowing effect due to *motion* which was observed in this experiment, assumed genuine (and most certainly it needs to be confirmed by repetition), is according to this explanation entirely due to the *special or restricted* relativity theory; Einstein's *general* relativity theory is involved here only as a necessary correction to allow for the variation of the earth's gravitational potential with altitude. This is a static effect – a point which will become important later on. And, remarkably, nowhwere has there been an mention of *acceleration*.

This new interpretation of relativity is completely at variance with previous attempts to resolve the twins paradox (the asymmetrical-ageing variant of the clock paradox, during a space journey). The standard explanation, for example by Sir Hermann Bondi[9], supposes that some unspecified effect of *acceleration* modifies the behaviour of one of the clocks; it fails through its vague inability to handle more than one case without changing the assumption. Even the explanation due to Einstein himself[10], which is specific enough but which relies on a abstruse and unconvincing *ad hoc* argument (devised for a different purpose anyway), permits *an accelerated observer* to draw correct deductions about a distant clock. Nor is this the only difficulty that arises if one follows this route: for the paper by Builder, on which Hafele and Keating chose to rely, was in fact arguing the case for a Very Special theory of relativity of Builder's own, in which he claimed,

> "Thus we conclude that the relative retardation of clocks predicted by the restricted theory *does indeed compel us to recognise the causal significance of absolute velocities."* (*My italics*).

So clearly we are no longer dealing with Einstein's theory of relativity; there seems to be little left of that but the name! Nevertheless, the new interpretation (or theory) is self-consistent, has provided an answer to Dingle's Question, seems to have resolved the twins paradox, and incidentally seems to agree with experience – that is, the Hafele-Keating experimental results are consistent with the Builder interpretation – so that one has no choice but to take it seriously. Not least of its virtues is that, despite Dingle's protest, it supports Einstein's polar-vs-equatorial clock contention word for word.

EXPERIMENTAL TEST OF EINSTEIN'S STATEMENT

But we have not reached the end of the matter. Is it really true that a clock on the equator will run more slowly than a clock at one of the earth's poles, as Einstein originally suggested?* This is an issue that could be put to practical test. Hafele and Keating by their experiment have alerted us to the accuracy to be expected of modern atomic clocks. The amount of the differential timekeeping discrepancy between polar and equatorial clocks, according to *all* interpretations of special relativitiy, is not in doubt: given the earth's equatorial velocity $v = \Omega = 465.08$ m/s, it is

$$\delta t/t = -\tfrac{1}{2}v^2/c^2 = -1.2033\times10^{-12}$$

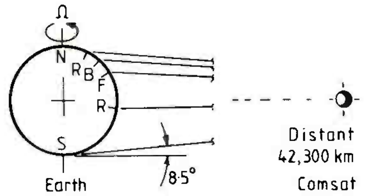
$$\text{or } \Delta t = -104.0\text{ns per day.}$$

A discrepancy of this magnitude is well within the measurement capability of installed (non-portable) caesium clocks, and to make matters easier still, the rate is constant and cumulative over an observing period of unlimited duration. Thus neither the intrinsic accuracy of the clocks nor their readability is a determining factor in the feasibility of this experiment.

Various difficulties present in the Hafele-Keating experiment are not relevant here. For example, two sources of error were the integrated geographic locations of the clocks, then carried in aircraft but now fixed, and their velocities over the surface, now zero. There, gravitational effects of altitude varied from zero at sea level to $\Delta t = +113$ns per day at the 12km operating altitude of the 707. Here, the south pole is the obvious choice, since it lies on a land mass and it is the site of a permanent international scientific base. Its height is some 3,000 metres above sea level; if the modern city of Quito (altitude 2,850m) were selected as the corresponding equatorial site, the timing discrepancy due to altitude (gravitational potential, from the *general* relativity theory) would also be reduced to insignificance. We would then be testing the time dilation of special relativity alone, directly, and without confusing side-issues.

The only technical problem remaining in this experiment is the obvious one – how does one compare the readings of the polar and equatorial clocks *in situ?* The well-tried method is to rely on radio signals for the transmission of timing information between them. Provided the comparison is mutual (that is, by simultaneous two-way links), such communications links are self-compensating: slow phase drifts in both directions over the same transmission path will cancel each other out to second order. Synchronous or geostationary communication satellites, whose residual station-keeping errors are limited to just a few kilometres and whose relative motions are smooth and very accurately repetitive over the sidereal day, are entirely suitable for this task. (It will be remembered that we are interested in the *differential rates* of these clocks, not their synchronization, so the mean length of the link is immaterial).

However, for our purpose the Satcom link suffers from the prohibitive snag that geostationary satellites are necessarily positioned some 8½ degrees below the local horizon as seen from the pole itself (Fig. 2), so that the timing waveforms would have to be relayed over about 1,000 km by tropospheric scatter or short-wave ionospheric link before being transmitted out to the satellite. Such links are notoriously prone to



multipath interference effects: the result would be to destroy the vital self-compensatory properties of the two-way links. So for the time being we cannot work to and from the poles themselves.

But all is not quite lost. Probably the highest latitude for a terminal with *en clair* access to a synchronous satellite – while also incidentally looking under the auroral multipath zone – is about 70°. Iceland is an obvious candidate. A clock in the observatory at Reykjavik, at 64° north and at sea level, could with great convenience be compared by direct satellite link with a similar clock at Recife, Brazil, at 7° south and also at sea level. As promising sites to complete an experimental network one might suggest Brighton (51°N) on the UK coast near Herstmonceux, and Funchal (32°N) in Madeira. The predicted relative time dilations at these stations are readily calculable: between Reykjavik and Recife the sliprate should be −82.5 ns per day, and even over the short Sussex-Madeira link it should still be −33.6 ns/day – that is, a discrepancy of one complete cycle per day at 30MHz.

We do not need to perform this experiment today because its result is known already. International time centres have been comparing the rates of each others' standard clocks for many years as a matter of routine. The finding is that relativistic differential time dilation as predicted by Einstein and implied by Hafele and Keating does *not* in fact take place. No mention of it appears in the CCIR Report which deals with the presumed effects of relativity on international timekeeping.[12] If this result puzzles you, you have my sympathy; please read on.

A WHIFF OF PARADOX...

Let me amplify that a little, and try to make it clearer. Hafele and Keating's formula for the proportional timekeeping behaviour of their airborne clocks, or time dilation, was

$$\delta t/t = gh/c^2 - \tfrac{1}{2}v^2/c^2. \qquad (1)$$

The term $-\tfrac{1}{2}v^2/c^2$ is Einstein's 1905 prediction due to motion at velocity v (by special relativity theory), where

$$v = \Omega r \cos\phi + u, \qquad (2)$$

ϕ being the latitude and u being, effectively, the eastward component of the aircraft's speed over the earth's surface. The term $+gh/c^2$ is an extra, static contribution from *general* relativity theory, due to the earth's gravitational field; if g is the acceleration, then gh represents the gravitational potential, relative to the earth's surface, of an airborne clock at altitude h. It is held by the Relativists that the Hafele-Keating results,

* Einstein's text (at the head of this article) is the statement that clock B runs slower than clock A *while clock A runs faster than clock B*, and as such it involves no "paradox".

which are said to be entirely consistent with equation 1, provide via its term gh/c^2 and $\frac{1}{2}v^2/c^2$ a complete and satisfactory confirmation of both the general and the special relativity theories.

That would be a magnificent outcome if it were true, but unfortunately it suffers from the following small difficulty. Rather than flying these aircraft, keep them on the ground for a day or so. Then their altitude above sea level becomes permanently $h = 0$ and their ground-speed remains permanently $u = 0$. Making those simplifying substitutions in (1) – which must of course apply just as well to clocks in grounded aircraft – the time-dilation prediction becomes

$$\delta t/t = -\tfrac{1}{2}v^2/c^2 = \tfrac{1}{2}(\Omega r \cos\phi)^2/c^2, \quad (3)$$

where $v = \Omega \cos\phi$ is simply the eastward motion due to earth rotation (only) of the grounded aircraft at latitude ϕ. And it must describe equally well the eastward velocity of the US Naval Observatory at its latitude, or the Reykjavik and Recife Observatories at their respective latitudes.

Clearly, by this relativistic formula the local dilation of time, $\delta t/t$, should be proportional to the simple function ($\cos^2\phi$) of an observatory's latitude, as predicted by Einstein and in agreement with the Hafele-Keating experimental result. But the truth is that the timekeeping of fixed (earthbound) observatories at sea level does not demonstrate a systematic dependence on latitude. Surely somebody should have asked, Why not?

...AND A RELATIVISTIC WRIGGLE

This failure of fundamental theory, which from the point of view of the philosophy of science might be considered quite an important failure, was relegated by Hafele and Keating to a mere footnote in their report, in which they cited a dicussion[13] by W.J. Cocke:

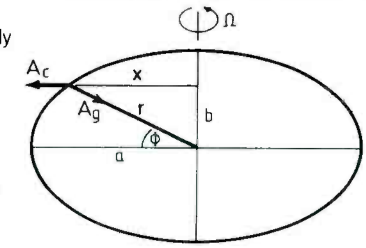
> "Clocks at rest on the earth's surface (at average sea level) keep the same relativistic time independently of latitude differences. The effect of the difference in surface speed at different latitudes is cancelled to lowest order by a corresponding effect from the difference in surface potential owing to the oblate figure of the earth."[14]

Although just what the 'relativistic time' means in this context is not clear, we can still analyse this argument. As defined above, (gh) was the gravitational potential, relative to sea level, due to flight at altitude h. Here it would seem that another kind of 'h' – H, say – actually the height difference between the earth's local radius r at latitude ϕ and its polar radius b, due to oblateness – is to be made responsible for cancelling out the two relativistic effects of velocity (Special theory) and gravitational potential (General theory) exactly, in accord with the very convenient equation

$$gH/c^2 - \tfrac{1}{2}v^2/c^2 = 0! \quad (4)$$

The elegant simplicity of this proposal may well serve, for believers, to conceal the fact that it is intenable. The reason why the earth's surface follows its flattened, oblate (eliptically curved) shape is simply that everywhere on its surface, neglecting effects

Fig.3. The vector accelerations acting on any particle or body at sea level and geocentric latitude ϕ are two:



$\mathbf{A_g} = GM/r^2$, purely gravitational toward the geocentre, and
$\mathbf{A_c} = +\Omega^2 r \cos\phi$, centrifugal away from the axis of rotation.

Put $\mathbf{A_c} = +\Omega^2 r \cos\phi = \Omega\mathbf{x} = -dV_c/dx$ (i.e. $-$ grad V_c).

Then on integrating, $V_c = -\tfrac{1}{2}\Omega^2\mathbf{x}^2 + C$. (A)

At the pole, where $x = 0$, set $V_c = 0$; thus $C = 0$, so that $V_c = -\tfrac{1}{2}\Omega^2 x^2 = -\tfrac{1}{2}\mathbf{v}^2$.

Also, on integrating $\mathbf{A_g} = -GM/r^2 = -$grad V_g, one obtains

$$V_g = \left[-\frac{GM}{r}\right]_b^r = \frac{GM}{br}(r-b) \approx +gH, \quad (B)$$

having set $H = (r-b) = 0$ at the pole. Hence the total gravitational potential due to both force fields combined is

$$V = V_g + V_c = (gH - \tfrac{1}{2}v^2) \quad (C)$$

– which by definition is zero over the entire geoid surface. Thus the contribution of general relativity to timekeeping at sea level is nil.

Note particularly that the term $-\tfrac{1}{2}v^2$ in (C) is derived from the gravitational potential (general relativity), and is not to be identified with the term $-\tfrac{1}{2}v^2/c^2$ of equation 1 in the main text, which was derived from the Lorentz transformations (of the special relativity theory).

gravity (plumb-line) is at right angles to the local horizontal (spirit-level); if it were not, the oceans would flow north or south to make it so. The fallacy in the argument lies in assuming that the gravitational term $V_g = (GM/r^2)H = gH$ represents the whole of the matter; but the centrifugal term V_c (the cause of the earth's oblateness) must also be included. When it is, (see panel), the total gravitational potential at each observatory clock is not just $V_g = gH$ as in equalion 4, but exactly $V_g + V_c = 0$.[15] Pace W.J. Cocke, the surface of the geoid – mean sea level, where $h = 0$ – is now (and always has been) a unipotential surface world-wide.

In other words, the gravitational potential at sea level is the same everywhere in the world. Hafele and Keating's *"difference in surface potential owing to the oblate figure of the earth"* does not exist. It follows that general relativity is irrelevant to this argument, since its contribution is zero; it does not influence the timekeeping of clocks at sea level at different latitudes, however desirable such an influence might have been for the defence of relativity theory.

INTERIM CONCLUSION

"To sum up: In 1905 Albert Einstein predicted, as a consequence of relativity theory, free of paradox, that an ideal clock [at sea level] on the equator would run more slowly than an identical clock [also at sea level] at the earth's pole. An experiment performed in 1971 purported to confirm the influence of both special and general relativistic effects on the timekeeping of quasi-ideal clocks. The theory which was said to underlie that experiment was also seen to support Einstein's original prediction.

"However, it is observed that the differential slowing of clocks due to latitude alone (independent of geographic motion and altitude), which was predicted by Einstein, does not in fact take place. It seems that the explanation put forward – and apparently generally accepted – to account for this theoretical failure was physically unsound."

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13. Cocke, W.J. Relativistic corrections for terrestrial clock synchronisation: *Phys.Rev.Lett.* vol.16, 1966 p.662.
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15. 'Measured' numerical values inserted into eqn 4 will not yield the result $V_g + V_c = 0$, because the earth is neither spherical nor of uniform density and one has to deal with small differences between very large quantities; for example, the observed value of "g" at the poles is 9.8321 m/s² whereas the calculated value from GM/b^2 is 9.8660 m/s², a discrepancy exceeding 0.3%. It is as though the apparent position of the goecentre varied by up to 11km, depending on the observer's latitude. The direction of the local vertical is subject to a similar small discrepancy (5.4′ arc at latitude 45°) for the same reasons. The precise statement is that the geoid is defined as a unipotential surface in earth coordinates – if one understands potential in its usual, field-theory sense.

Dr Scott Murray's biography appeared in the June 1983 issue.

APPLICATIONS SUMMARY

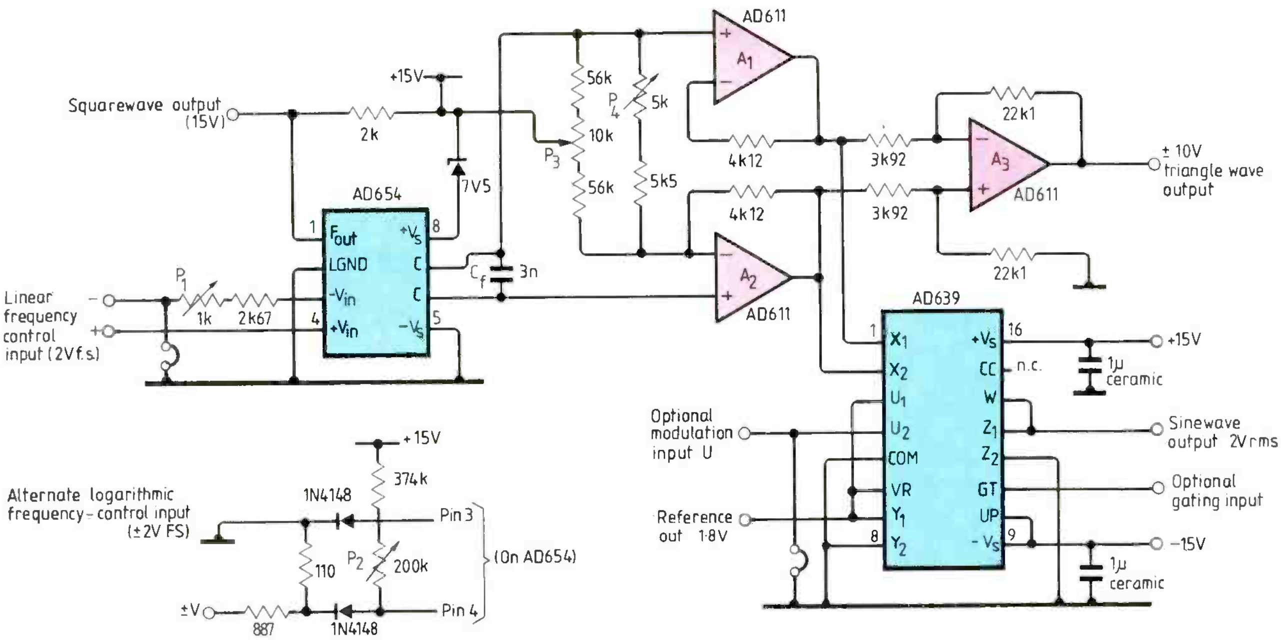
FUNCTION GENERATOR

Analogue shaping techniques are used in the AD639 to provide all normal trigonometric functions and their inverses. Selection requires only an input voltage representing an angle.

In this function-generator circuit, part of the 639's 12-page data sheet, frequency from 20Hz to 20kHz is voltage controlled and amplitude is within 0.1dB of 2V r.m.s. Amplitude modulation is possible using the U_2 input.

Other applications in the Analog Devices data sheet are a four-quadrant sine/cosine multiplier and a sine/cosine oscillator. Connections for basic cosine, tangent and arctangent output are also given.

EWW300 on reply card



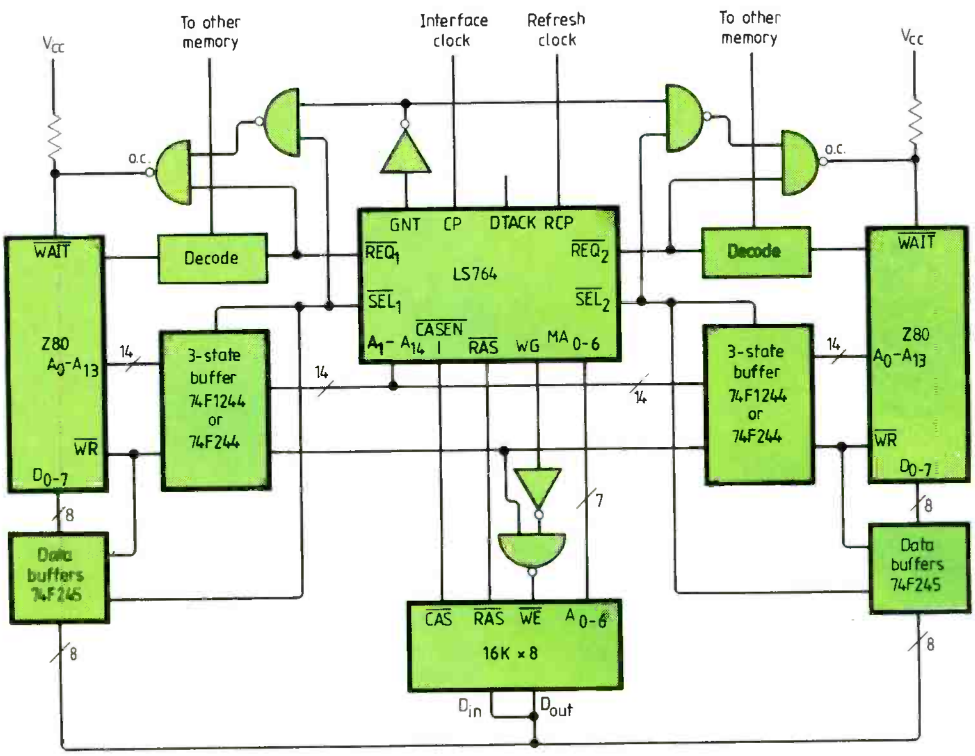
DYNAMIC-RAM CONTROLLER

Two microprocessors can access the same bank of d-ram using the 74LS764 dual-ported controller. Arbitration, signal timing, address multiplexing and refresh generation are performed by the 764 which, with nine address lines, can control up to 1M-byte of ram.

Note M86-1196/RST from Mullard details the device and shows three memory-sharing circuits, this one for two Z80 processors, one for a Z80 and 68000 and one for two 68000 devices.

Clock rates of up to 30MHz can be used; adjustable refresh timing is possible through use of a separate refresh clock section. Provided that both c.p.us operate from the same clock, the controller also allows priority to be given to a particular processor.

EWW301 on reply card



Settling time measurements

Automatically measuring the settling time of an operational amplifier using a programmable digitizing oscilloscope.

Settling time is the time required, following the initiation of a specified stimulus to a linear system, for the output to enter and remain within the limits of a specified error band centered on the ideal steady-state output value. For example, when testing the settling time of an op-amp, the system stimulus is a step change of the applied input voltage usually scaled so that the output swings between its upper and lower design limits.

When testing a digital-to-analogue converter, the stimulus is the application of a digital word or clocking signal that causes the output to swing between zero and full scale. Figure one shows how settling time is specified for these two applications.

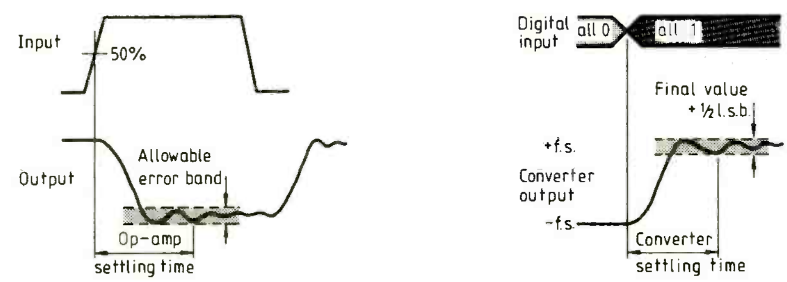


Fig.1. Specification of settling time measurements for an op-amp, left, and a d-to-a converter, right.

TEST SETUP

Whether settling time is measured manually or automatically, the success of the measurement depends on the ability to resolve small variations of the base or top of a relatively large signal accurately. Typical error-band specifications, usually expressed as a percentage of final value, range between 0.1% and 0.001%.

One of the best ways to make this measurement is to use the virtual ground method. This is a differential probing technique which allows signal error, i.e. settling information, to be analysed directly. The general set up for this test is illustrated in Fig. 2.

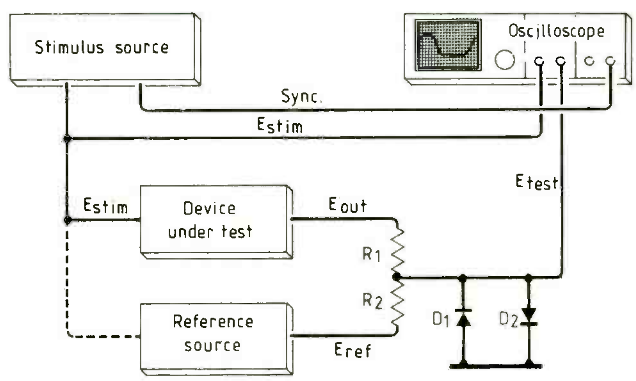


Fig.2. Typical test set up for settling-time measurement. This method allows signal error to be analysed directly.

At the virtual ground point, the signal under test is summed with a reference signal equal in magnitude to the final value of the test waveform but of opposite polarity. Voltage at the summing node, E_{test}, is zero when the signal under test E_{out} has the same magnitude as reference voltage E_{ref}.

While the test waveform is settling error waveform E_{test} can be measured to determine the degree to which E_{out} has settled. Since $E_{test}=(E_{out}+E_{ref})/2$, amplitude of the error waveform is reduced by a factor of two and the error band should be adjusted accordingly. Figure three illustrates the relationship between E_{out}, E_{ref}, and E_{test}.

The signals could be summed in an oscilloscope using an A+B mode, but this would require a wider dynamic range than is usual for instrument inputs.

Summing with $R_{1,2}$ allows clamp diodes $D_{1,2}$ to be included to limit the maximum voltage excursion of E_{out}. This minimizes input overdrive and effectively controls test-system recovery time.

For this example, the device under test is a 741S high speed op-amp. This amplifier is to be used as an output buffer for an eight-bit d-to-a converter and is configured as a unity gain, inverting, current-to-voltage converter. Its full-scale output is −10 to +10V and the specified settling-time error band is 0.1% f.s.

The test system, Fig. 4, consists of a function generator as the stimulus, a test fixture for the op-amp, an automatic digital oscilloscope for measuring the response and a p.c. as the system controller.

The function generator must be able to produce a low distortion squarewave that has a specified settling time. When operated into high impedance, it should supply the required voltage swing into the test fixture. Since the amplifier is used in inverting mode, the squarewave stimulus can also be used as the reference voltage applied to the summing network.

The test fixture is a carefully laid-out p.c.b. containing the components shown in Fig. 4 and a socket for the op-amp. A BNC cable couples the stimulus signal and two test points allow direct connection of the oscilloscope probes to the test circuit.

A pair of 10:1 probes couple the test fixtures signals to the oscilloscope. The stimulus signal is input to channel one and error signal E_{test} is input to channel two. A BNC cables connects the function generator sync. output to the main trigger external input of the automatic oscilloscope; the sync. ouput triggers the oscilloscope.

Analysing the E_{test} measurement path shows that its effective bandwidth is approximately 1MHz, due primiarily to the high source impedance of the $R_{1,2}$ summing network taken with the clamp diode and probe capacitance. This bandwidth should

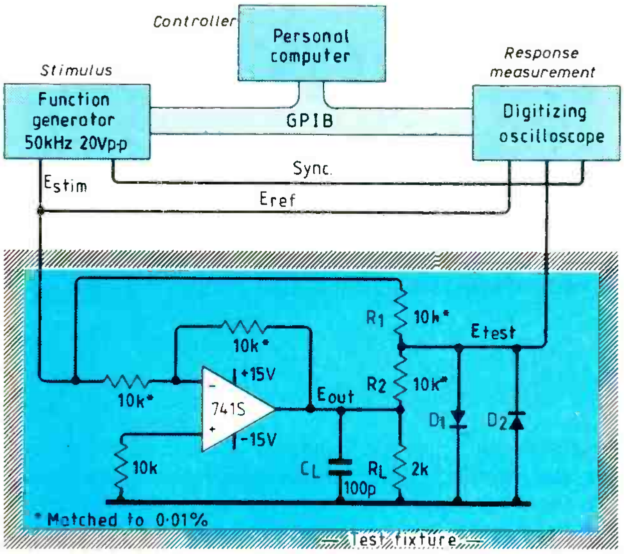


Fig.4. Set up for automatic settling-time measurement of a high-speed op-amp.

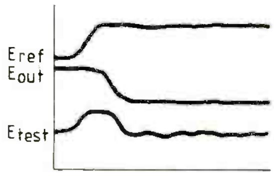


Fig.3. Test waveforms for settling-time measurement. Waveform E_{test} represents the degree to which the E_{out} has settled.

be adequate for the measurement of the 741S op-amp, but may need to be reconsidered for other measurements.

MEASUREMENT ALGORITHM

When making an automatic measurement, the computer needs to perform the same sequence of operations as an operator performs when making manual measurements. Measuring settling time is basically measuring the time between two signal sources; the necessary steps are shown in Fig. 5.

There are several important considerations to be made when designing a test system to measure settling time. System noise, stray capacitance, signal reflections, and ground path impedance can all cause significant measurement errors. Here are some suggestions that can improve measurement accuracy.

While the reference source selected depends on the specific measurement application, it is important that the source output has a low noise content. If a pulse generator or function generator is used, both amplitude accuracy and settling time must be well-defined and within the test requirements. This is particularly true if the stimulus signal is not accessible or is difficult to trigger on.

Resistors used to sum E_{out} and E_{ref} should be good quality metal-film types and should be tightly matched to minimize the gain error at E_{test}. Select the resistors to a tolerance at least one order of magnitude better than the error band being tested. For example, if the error band is 0.1%, match R_1, to 0.01%.

Alternatively, a potentiometer can be used to trim the summing network. Also, since R_1 and R_2 in parallel determine the source impedance of E_{test} their value should be made as small as possible without excessively loading the device under test.

Diodes should be Schottky barrier types. Of primary importance are the diode's capacitance, reverse recovery time and current/voltage characteristics. Also, the diodes must be connected to a good, low-impedance ground.

Because the source impedance of the $R_{1,2}$ summing network is high and capacitance at the test fixture is unavoidable, the wrong probe can drastically affect wide bandwidth measurements. In many cases, the lower capacitance of a resistive divider probe or an active probe makes them an important addition to a test system.

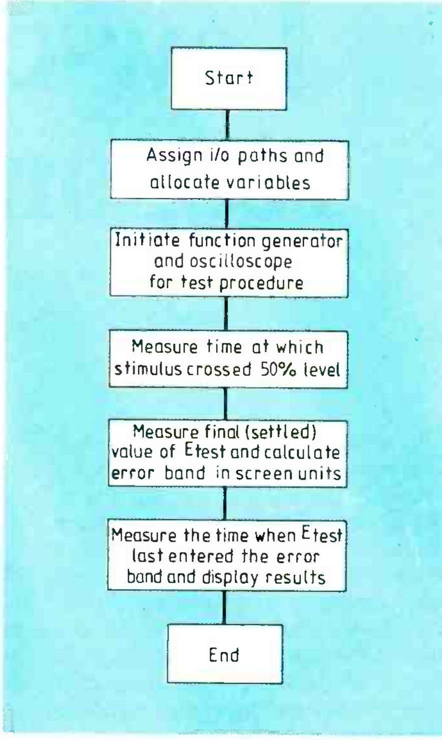


Fig.5. In the test set up of Fig. 4, a computer controls the measurement. This flow chart outlines the program requirements.

Most oscilloscopes have a dynamic range of approximately five divisions beyond top and bottom of screen. To reduce effects of system noise and to improve resolution, the display signal should be scaled as large as possible. However, beyond 20 divisions of vertical deflection the recovery time of the oscilloscope will affect the measurement.

Low-cost automated response using GPIB

Measurements for personal computers using IEEE488 bus.

T. SEGARAN

This software approach enables simple automated measurements, without needing the full g.p.i.b. capability to do parallel poll and SRQ handling, on any personal computer with two eight-bit user ports. The hardware costs just a few pounds.

Using a general-purpose interface adaptor so that software overhead can be kept to a minimum allows for full implementation of the g.p.i.b. interface. But other approaches are more cost-effective where only a particular aspect of the interface function needs to be used. For example, if a low-cost controller is required to automate a measurement, and either store or display the results on a screen, an ideal solution will be to use any common microcomputer with two eight-bit i/o ports and a minimum of additional hardware.

A computer with two eight-bit i/o ports is required to act as a controller talker and listener. As a controller the interface indicates which instrument is addressed at any particular moment and initializes the bus when necessary. As a talker, it sets up specific measurement parameters and ranges for the instrument currently being addressed. Finally, as a listener, it receives measured data from an instrument and performs some functions on it like storage and display.

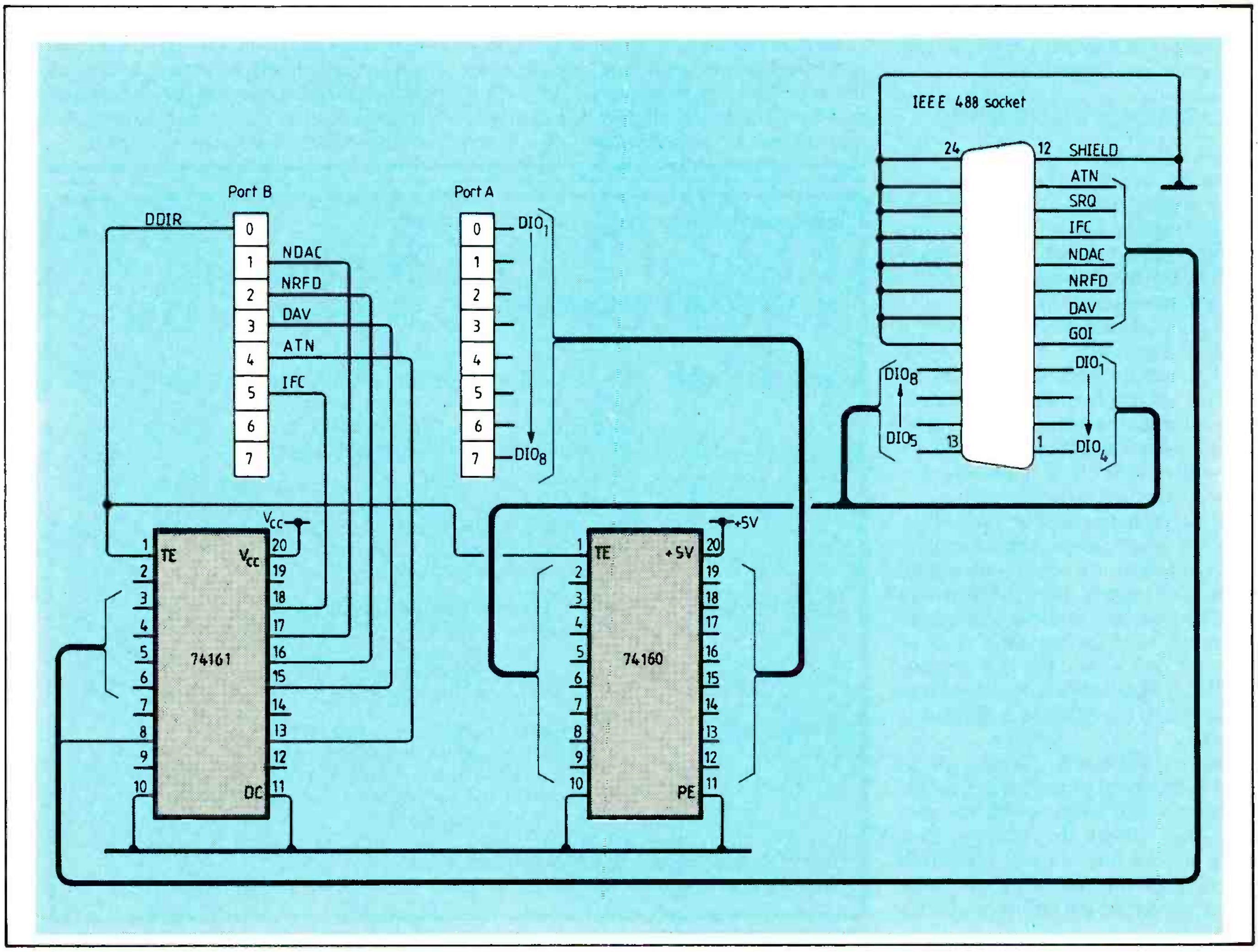
To implement g.p.i.b. on a computer you need two eight-bit i/o ports. One i/o port forms the data highway and the other consists of two control lines and three handshake lines. The two control lines are IFC and ATN. Signal REN will be hard-wired low so that whenever a particular instrument is addressed its front panel controls will also be disabled.

Necessary hardware connections are shown below. The bus tranceivers enable one to meet the correct drive conditions and also to switch from sending to receiving data. An extra i/o bit is necessary to decide data direction through the transceiver.

Port A is connected to the data lines and is fairly easy to handle using POKE and PEEK commands. However, some bits in port B are used as inputs while some are outputs, therefore a bit-handling facility is necessary. For this reason and for faster data transfer, these lines are controlled with a machine-code routine.

Software to implement the interface consists of the following subroutines. Before this first routine to set an instrument to 'talk' or

Fig.1. GPIB interface hardware. In many applications, a very simple hardware interface suffices – most of the work is done in software.



'listen' is entered, variable A must be set to the required address, which could be the talk or listen address of that particular instrument.

PROG. A PSEUDOCODE

CALL SUB D TO LOGICALLY INVERT ADDRESS

SET PORT A AS OUTPUT

PLACE CONTENTS OF VARIABLE A IN PORT A

SET NDAC, NRFD OF PORT B AS INPUTS

SET DAV, ATN AND IFC AS OUTPUTS

STROBE IFC LOW TO CLEAR AND INITIALIZE BUS

SET ATN LOW

SET DAV HIGH

WAIT FOR NRFD TO GO HIGH

SET DAV LOW

WAIT FOR NDAC TO GO HIGH

SET DAV HIGH

RETURN

This next subroutine takes the contents of string A$ and sends it to the instrument that has been addressed to listen. The Ascii codes are inverted to satisfy the requirement that the logic is active low.

PROG. B PSEUDOCODE

SET PORT A AS OUTPUT

SET NDAC, NRFD, OF PORT B AS INPUTS

SET DAV, ATN AND IFC AS OUTPUTS

SET ATN HIGH

SET DAV HIGH

FOR THE STRING A$ PROCESS ALL THE "LETTERS"

  OBTAIN ASCII OF LETTER

  INVERT IT LOGICALLY

  PLACE IN PORT A

  OBSERVE THREE WIRE HANDSHAKE PROCESS

NEXT LETTER

RETURN

The following subroutine accepts data from the designated talker, and makes the computer a listener. Received data is inverted logically and string A$ is created, which holds the data. This is in exponential form and is converted to a real number R by the last section of the routine.

PROG.C PSEUDOCODE

SET PORT A AS INPUT

SET NDAC, NRFD, ATN, IFC AS OUTPUTS

SET DAV AS INPUTS

CLEAR STRING A$

SET ATN HIGH

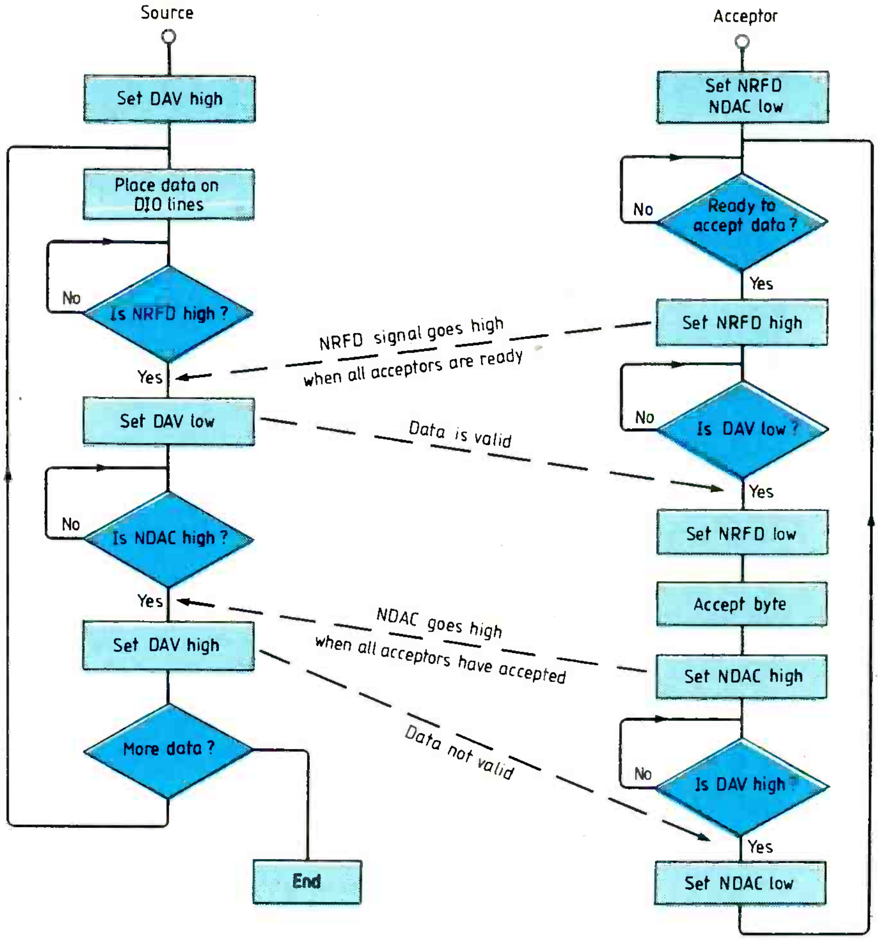


Fig. 2. Three-wire handshaking flow.

SET NDAC, NRFD LOW

DO FOLLOWING UNTIL RECEIVED BYTE B REPRESENTS LINE FEED:

  OBSERVE THREE-WIRE HANDSHAKE PROCESS

  PLACE RECEIVED BYTE IN VARIABLE B

  LOGICALLY INVERT CONTENTS OF B

  ADD STRING REPRESENTATION OF B A$ UNLESS IT REPRESENTS CARRIAGE RETURN

CONTINUE

CALCULATE REAL NUMBER MANTISSA/EXPONENT FORMAT

PLACE THIS IN VARIABLE R

RETURN

The fourth subroutine controls the line of port B using the USR command which enables one to mix Basic and assembly-language routines. It operates on a single bit, either setting, resetting or returning its state in X, depending on the USR call. For example,

X = USR (Q) sets bit zero high

X = USR (Q1) sets bit zero low and

X = USR (Q2) returns the state of bit zero in X

It also is entered when the logical significance of a byte is to be changed.

PROG.D. PSEUDOCODE

DETERMINE WHETHER I/O BIT OPERATION OR BYTE INVERSION REQUIRED

FOR BIT OPERATION

  DETERMINE WHICH I/O BIT OF PORT B IS REFERRED

  SET, RESET OR READ BIT AS REQUIRED

  PLACE READ VALUE IN RELEVANT LOCATION

RETURN

FOR BYTE INVERSION

  FETCH BYTE FROM RELEVANT MEMORY ADDRESS

  PLACE THE INVERTED BYTE BACK IN STORE

RETURN

The frequency response measurement program calls up the relevant subroutines A,B or C after setting the required values in A and A$.

FREQUENCY-RESPONSE PSEUDOCODE

SET A TO ADDRESS OF AUDIO ANALYER (8903A)

CALL SUB A

SET A$ TO SELECT LEVEL AND MEASUREMENT PARAMETERS ON 8905A

With a personal computer, some software and a few t.t.l. i.cs, the 8903A audio analyser becomes an audio test station.

CALL SUB B

FOR FREQ = START FREQ TO STOP FREQ, STEP

SET A$ TO FREQ

CALL SUB B

CALL SUB C

STORE R IN ARRAY

NEXT FREQUENCY

COMPUTE GAIN IN DB FROM STORED ARRAY

DISPLAY GRAPH OF FREQ VS GAIN ON SCREEN

The external transceivers are needed to meet the drive conditions on the g.p.i.b. interface. The 74160 has open-collector outputs and can be set for send or receive by placing TE (pin 1) high or low respectively. (PE to low sets output to open-collector).

The 74161 is specially designed for controllers. By keeping DC low (pin 11) ATN, REN and IFC are always designated as outputs, since a controller always has this configuration. Note that NDAC and NRFD can only be open-collector outputs since operation of the handshake allows the slowest instrument, being the last to release these then, to control the speed of information flow.

GPIB/IEEE488 INTERFACE PROTOCOLS

Addressing and data transfer take place over an eight-bit bus. Five control lines indicate and set the status of the bus. Interface clear (IFC) is used by a controller to initialize the bus to a known state. In this state, none of the instruments is addressed and the controller is in charge. Attention (ATN) is used by the controller to indicate the significance of the information on the bus.

When the ATN line is low, all the instruments interpret the information on the bus as being an address. If an instrument recognizes the address as being its own, then it interprets further data bytes as being set-up information. When the set-up information is being put on the bus the ATN line is put high by controller.

Remote-enable line REN is set low by the controller when addressing an instrument to disable front panel controls. The other two lines carry service request SRQ and end or identify (EOI) signals. The EOI signals, optionally indicating the end of a multi-byte transfer, are not necessary for the simple application and are beyond the scope of this article.

Three remaining lines are used for handshaking during byte transfers on the bus, data valid (DAV) not ready for data (NRFD) and no data accepted (NDAC).

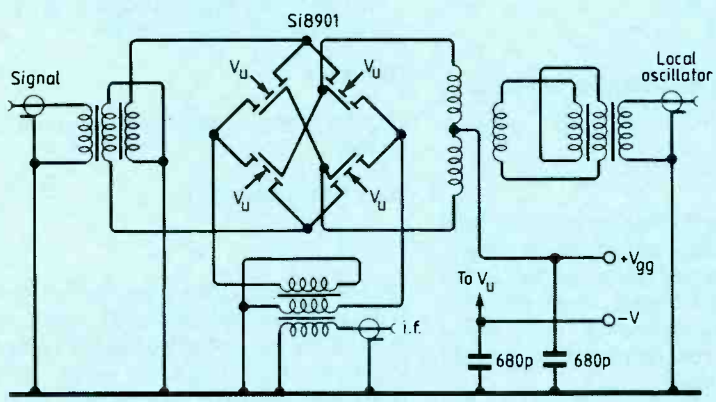
APPLICATIONS SUMMARY

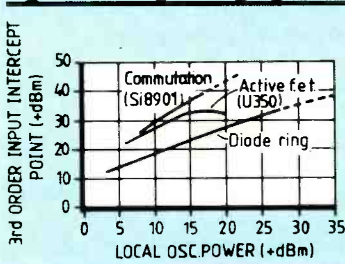
DOUBLE-BALANCED MIXER

Commutation gives a wide dynamic range without increasing local oscillator drive in a double-balanced mixer circuit from Siliconix. Input third-order intercept points higher than 39dBm with 17dBm of local-oscillator drive have been achieved.

Unlike conventional diode-ring or active-fet mixers, the commutation mixer relies on the switching actions of quad fets. This mixer is in effect a pair of switches reversing the signal-carrier phase at a rate determined by local-oscillator frequency.

The note, called Designing a super-high dynamic range double-balanced mixer, also includes data on the Si8901 ring demodulator/balanced mixer used in the prototype design. EWW303 on reply card





Performance comparison of double-balanced mixers. Compared with conventional diode-ring double-balanced mixers, the 8901 mixer gives an order of magnitude performance improvement at local-oscillator power levels.

DTI to study custom i.cs

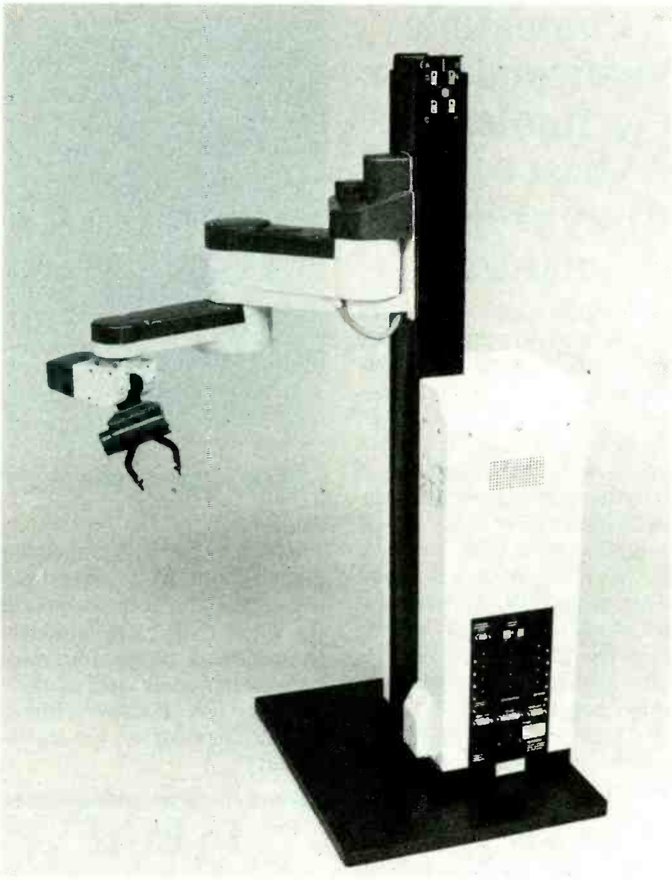
The current and potential use of custom-made integrated circuits is to be the subject of a study by the Department of Trade and Industry. Despite the reliability, cost-saving and enhanced performance offered by these devices, many companies, especially small concerns seem reluctant to use them. The consultancy team will study the circuits, their use and the factors that may be inhibiting potential users. The Association of Instrumentation, Control and Automation (Gambica). The National Economic Development Office and the Electronic Components Industry Federation have all expressed a strong interest and will be participating in the study which is being carried out by Michael Shortland Associates in collaboration with Butler Cox and Partners. Anyone wishing to contribute information or comments should contact them at 100 High Path Road, Guildford, Surrey. Telephone: 0438 859535.

As if to reinforce the need for such a study, a newsletter has come from a market research organisation, Nu-Markets Associates. In it Prof.Stan Hurst of the Open University details the types of application-specific i.cs (asics); gate arrays are uncommitted chips that need an interconnection overlay, while cell-library i.cs are designed from a range of predesigned cells which are then ordered to provide the required function and manufactured using all the stages of chip fabrication. He points out that there are now a number of design suites available for low-cost computers and he envisages the day when "every equipment designer in both large and small companies will have a c.a.d. system on the desk." Software and equipment is becoming more complex and yet easier to use so that electronic beam lithography will permit a very rapid turnround service for gate array design which, can then be committed to a corresponding cell library or other design if required for production.

The newsletter gives many examples of the new approach to i.c. production. Many of the major I.C. manufacturers are now forming alliances between themselves or with third-party c.a.d. system designers, to enter the asic field which they may see as a threat to their standard products. Independently, Intel have told us that they are to offer a c-mos gate array service originally developed by IBM for their internal use. In return IBM will have access to the Intel cell library.

Automatic volume measurement

A new system has been installed at British Airways Cargo centre. It can measure the volume of cargo automatically. The problem is that freight charges do not only depend on weight. Lightweight, bulky cargoes are charged by volume and also present problems for packing the cargo holds of the aircraft. This needed a tape measure and a lot of time. Now the packages are passed at a uniform speed through an opto-electrinic scanning gate which acquires a complete profile of the side and top of each package. The packages are also automatically weighed. The information is stored and processed in a system computer which can then give the required volume measurement. The line-scan cameras and computer interfaces are produced by Integrated Photomatrix Ltd, who specialize in opto-electronics.



RTX is claimed to be the world's first 'personal working robot'. Controlled by an IBM PC and using totally accessible software, the six-axis arm can pick up a 2kg load and place it anywhere within a 30 cubic feet space. "A robot with a 0.1mm accuracy moving at 9m/s is overkill if all you want to do is place p.c.bs onto a piece of test equipment" comments Tim Jones, technical director and co-founder of UMI. RTX is designed for mass production and currently costs £5000. UMI can be reached on 01-871 1339.

Eiffel tower in space

One can imagine the rocket-like shape of the Eiffel tower rising majestically skyward, but this is not to happen: Candidates at a recent competition have been asked to propose a durable structure in space, visible to the naked eye from earth, and symbolising universal communication. The structure should have neither commercial nor military applications though the delegates to the Congress of the Committee on Space Research (Copsar) have been invited to submit ideas for scientific and peaceful use. The project (with technical assistance from the French National Space Studies Centre and help from ESA) is part of the Centenary celebrations for the tower which was the subject of a similar competition, won by Gustav Eiffel in 1886 and erected for the Paris Exposition, 1889.

Phone sockets liberalized

As from the first of December it is legal to add your own sockets and extensions to the public telephone networks. There are one or two conditions: All equipment and wiring must be of approved types. There must be a new-type master socket provided by the public network. All add-ons can be taken from wire plugged into the front of the master socket, not connected directly. It is planned to produce a new pattern of master socket which will enable direct rather than plug-in connection of extension wiring. Sockets offered by retail outlets should have clear instructions related to their installation.

Windows screened from r.f.i.

Very thin, transparent coatings on glass can provide an effective electromagnetic screen to radio frequency interference; according to research carried out by ERA technology. Such glass panels can reduce the emmissions from computer devices (thus preventing electronic eavesdropping) and protect against high-intensity radiation from radar transmitters. The high-frequency tests carried out by ERA agree with accepted screening theory and have permitted the derivation of simple expressions to obtain a rapid assessment of screening performance on the sheet resistance value, a report covering the work, ERA report 86-0056R, can be obtained from ERA Technology Ltd, Cleeve Road, Leatherhead, Surrey KT22 7SA.

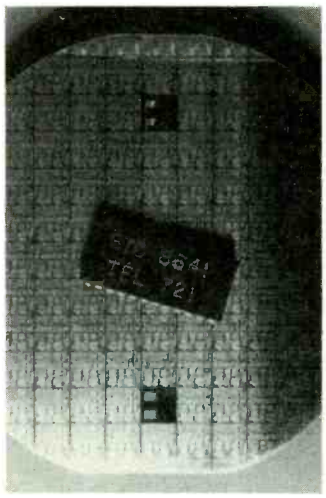
Transducer film

A plastic film has both piezo and pyro-electric properties. Its piezo effects allow it to be used for touch-sensitive keyboards, in loudspeakers and microphones. It can also be used as a heat detector and in strain gauges. In an alarm system, it has been used to detect an intruder at more than 6m. Its other advantages are that it can be shaped or moulded for specific application, can be cut or punctured without loss of function and is impervious to most chemicals. The poled Kynar polyvinylidene fluoride (PVDF) film has been developed in the US by Pennwalt Corp.

Honour for Ray Dolby

Dr. Ray Dolby, of the noise reduction system for tape recordings, has been awarded the OBE by the Queen. As he is an American citizen, the award is honorary and carries no title. Dr. Dolby studied in Cambridge and gained his PhD while researching at the Cavendish Laboratory. He has been consultant to the UKAEA and a UNESCO technical adviser in India. The A-type noise reduction system is twenty years old. B-type has been accepted as a standard for cassette recorders and players and a new system, spectral recording, has been announced for use in professional music recording, broadcasting and many other applications.

Compatible semiconductor technology is "first whole Alvey project to mature"



A compatible set of semiconductor process steps can produce devices that extend from low-power high-performance c-mos to very fast bipolar devices as well as devices that merge the two processes. Under installation at STC Components semiconductor division at Foots Cray and set for production of 1.25μm derives next year, the process is a joint Alvey project (with Racal and British Aerospace). A spin-off from this project has led to a 2μm installation at Foots Cray which has been making static rams since early 1985, alongside existing lines of 5 and 2.5μm n-mos production.

The first product of the "integrated technology concept" is a merged technology device which expoits the self-alignment of c-mos with the high performance of polysilicon emmitters and allows cmos devices to have totally unaffected by bipolar current gain is an application-specific digital signal processor that offers a lower cost route to transcoding of 64kbit/s.p.c.m. to adaptive differential p.c.m. and vice versa.

STC aim for only "moderate capacity" of 2000 wafers per week. "We aim to manufacture the more challenging products to enable us to improve our sales revenue per wafer" said marketing manager Richard Phipps. STC Semiconductors are on 01-300 3333.

In Brief

Canadian Home Shopping Network (CHSN), which operates through the cable networks, now has a satellite link so that Canadian shoppers in even the remotest areas can buy the goods displayed on their tv sets. The link is only one-way; shoppers need to use the telephone to order the goods.

CONFERENCE & EXHIBITIONS

3-4 December 1986
Satellite Broadcasting. Conference. Tara Hotel, London Online, as above.

9-11 December 1986
Videotex International Conference and exhibition. Wembley Conference Centre, London. Online, as above.

23-27 February 1987
Fiarex 87 international electronics trade fair. Rai Exhibition Centre, Amsterdam. Rai Gebouw, Europaplein, Amsterdam.

3-6 March 1987
International Open Systems Conference (and a MAP seminar, 4 March). Barbican Centre, London. Online, as above Semicon Europa 87 exhibition of semiconductor equipment and materials. Zuspa Convention Centre, Zurich. Enquiries to Cochrane Communications, Tel: 01 353 8807.

24-26 March 1987
Cadcam 87 exhibition. NEC Birmingham.
EMAP int. Exhibitions, Tel: 01 608 1161.

25-26 March 1987
Instrumentation Bristol 87 Exhibition. Bristol Crest Hotel. Trident Int. Exhibitions, Tel: 0822 4671.

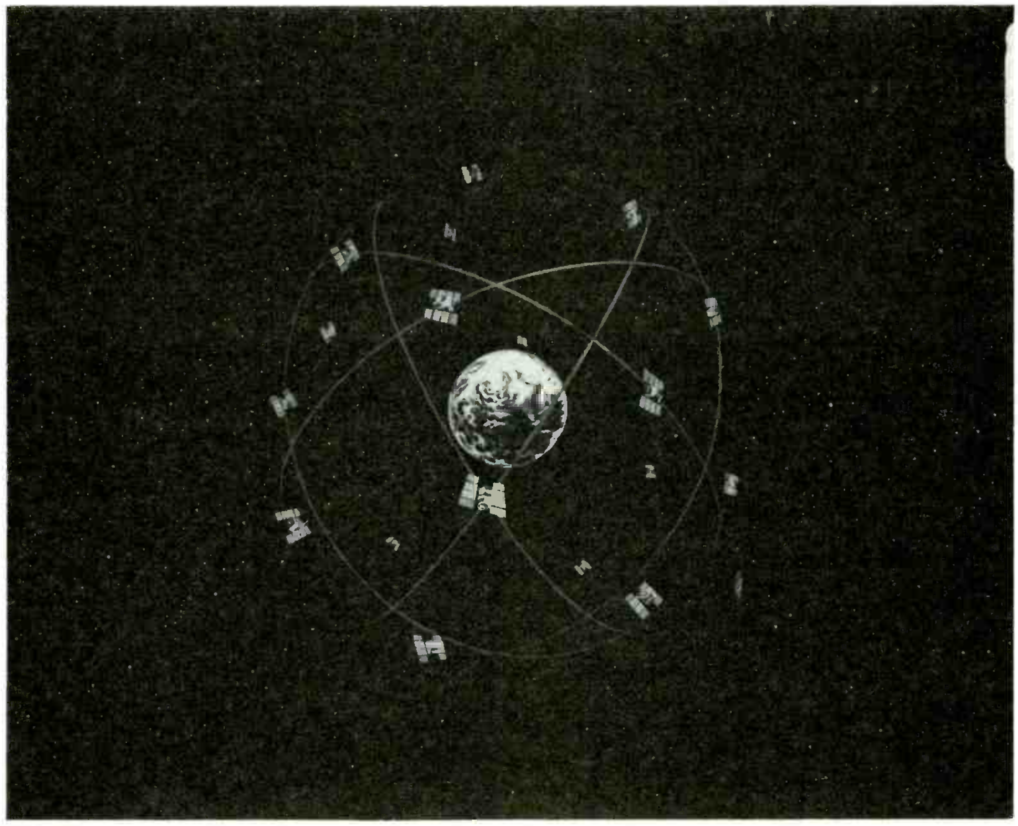
6-8 April 1987
Offshore computers conference and exhibition. Heathrow Penta Hotel, London. Offshore Conferences, Tel: 01 549 5831.

28-29 April 1987
Cellular and mobile communications Conference. Barbican Centre, London. Online, as above. Value-added network services (VANS) Conference. Barbican Centre, London. Online as above.

28-30 April 1987
City communications exhibition. Barbican Centre, London. Online, As above.

18-20 June 1987
Television measurements, Third international IERE conference. Montreux, Switzerland. IERE Tel: 01 388 3071.

Inmarsat and satellite navigation



Olof Lundberg, Director-general of the International Marine Satellite Organization, Inmarsat, has made a plea for the rationalization of satellite navigation and communication systems. In an address to the 1986 conference of the Royal Institute of Navigation, he pointed out that Inmarsat was founded for that very purpose but many nations are forging ahead with their own, usually military, systems.

The United States, for example, has five different systems which are to be phased out and replaced by the Global Positioning System (GPS) also called Navstar. This will consist of 18 satellites in a network of orbits so arranged that three are 'visible' at any specific time at any point on the globe. Any two satellites used together can enable users to determine their precise location, speed and time and use passive (i.e. receive only) instruments which can perform the timing and triangulation operations. A third satellite is used to provide altitude information. The USSR is developing a similar system with 12 satellites, known as Glonass. It uses spread-spectrum techniques in frequency bands near those of GPS and both systems are broadcast and could accommodate an infinite number of users. They are both being developed primarily for military use but would be of great benefit for civil aviation and maritime use.

Objections to such systems related to cost, accuracy, international acceptance, coverage and other problems. Taking GPS as an example, receivers are expensive (though becoming cheaper). US Congress has decreed that civil use will be free of any fees, but it could change its mind. Military users will be able to use the Precise Positioning Service which is highly accurate, but national security demands that civil users will be restricted to the standard positioning service (SPS) which is accurate to about 100m. [Readers might remember that Magnavox found a way round this with their MX4400 receiver – News Aug. 1986]. The fourth source of contention is the international acceptability of such systems which are under the control of a signal country – and its armed forces.

Matters are further complicated by the proposal of a separate commercial system providing radiodetermination satellite services (RDSS) Proposed by the US Federal Communications Commission (FCC), the two-way Geostar satellite system has been recommended. Objections to this system centre around the wide bandwidth required and the limited number of users at one time. Users will have to pay a registration fee and usage fees. Yet another commercial system, the Mobile Satellite Service, has been proposed, by the Omninet Corp, and accepted by the FCC. This is based chiefly on speech communication for mobile voice and rural radio and telephone services. Further proliferation is likely as the FCC believes that competition provides choice and encourages excellence. International competition comes from the European Space Agency Navsat system and the Granas system proposed by SEL in West Germany.

Olof Lundberg has reached a number of conclusions: that there is a demand for an international satellite mobile communications and radiodetermination service; that the USA will rationalize its federal system but will also encourage commercial services; that there will be a number of different services; that there will be stronger links between communications and navigation systems and between maritime and aeronautical users.

He reiterated that Inmarsat was set up to coordinate exactly such services. Many of them are already available through their channels. The Inmarsat Standard C ship station is about the size of a shoebox and will be as low-cost as any proposed. It provides message communications through the international telex and data networks. Automatic position-reporting and polling could find more applications if the national systems collaborated to produce a universal format and access arrangements to enable the data to be automatically transmitted and processed. Ranging systems for position determination could and should be provided by Inmarsat, who are planning to demonstrate the accuracy obtainable from geostationary satellites during the approaching year.

Another service required internationally is an "integrity" channel; a system that could monitor and validate satellite navigation systems so that users of, say Glonass or GPS, can be assured (within 10s) of the correct working of the system. The channel could be used to provide differential corrections to enable precise navigation or position determination. Inmarsat is studying the feasibility of providing such a channel.

Aircraft can be provided with surveillance systems that automatically provide position and ranging reports to traffic controllers. These can even be independent of the aircraft's own navigation system as the traffic control computer could interrogate the satellites directly as to the aircraft's position.

Dr Lundberg suggested that the framework already existed within Inmarsat for an international body that could accommodate under its umbrella the multiplicity of systems that would and could provide international and neutral management of national systems which may not, by themselves be wholly acceptable, but which could become acceptable if an international buffer were adopted.

CIRCUIT IDEAS

Subcode converter for c.d.

Serial subcode data from a Pioneer PD6010 disc player is converted by this interface into twelve bytes for feeding into a microprocessor.

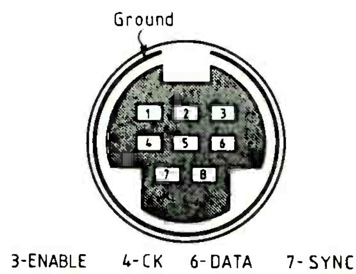
Data from the player is shifted into an LS164 register using the player's clock signal which also increments input-bit counter IC_{2a}. When eight bits have been shifted the bit-counter's D output goes high. This triggers the LS123 monostable mulitvibrator, causing parellel data from the shift register to be written into ram. At the same time, the write pulse clears the bit counter and increments ram-address counter IC_{2b}.

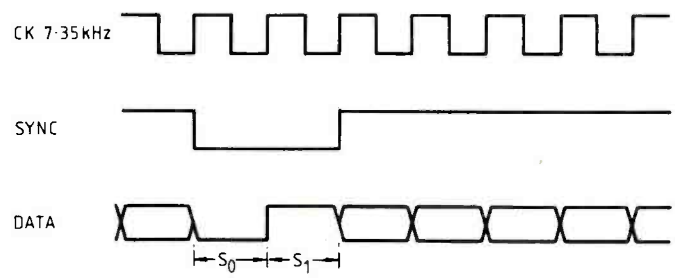
When a sync pulse is sent by the player, both counters are cleared and a DATA READY signal is produced., The falling edge of this signal interrupts the microprocessor connected to the interface. Signals ENABLE and SYNC from the player are gated together to inhibit DATA READY when incoming subcode data is invalid.

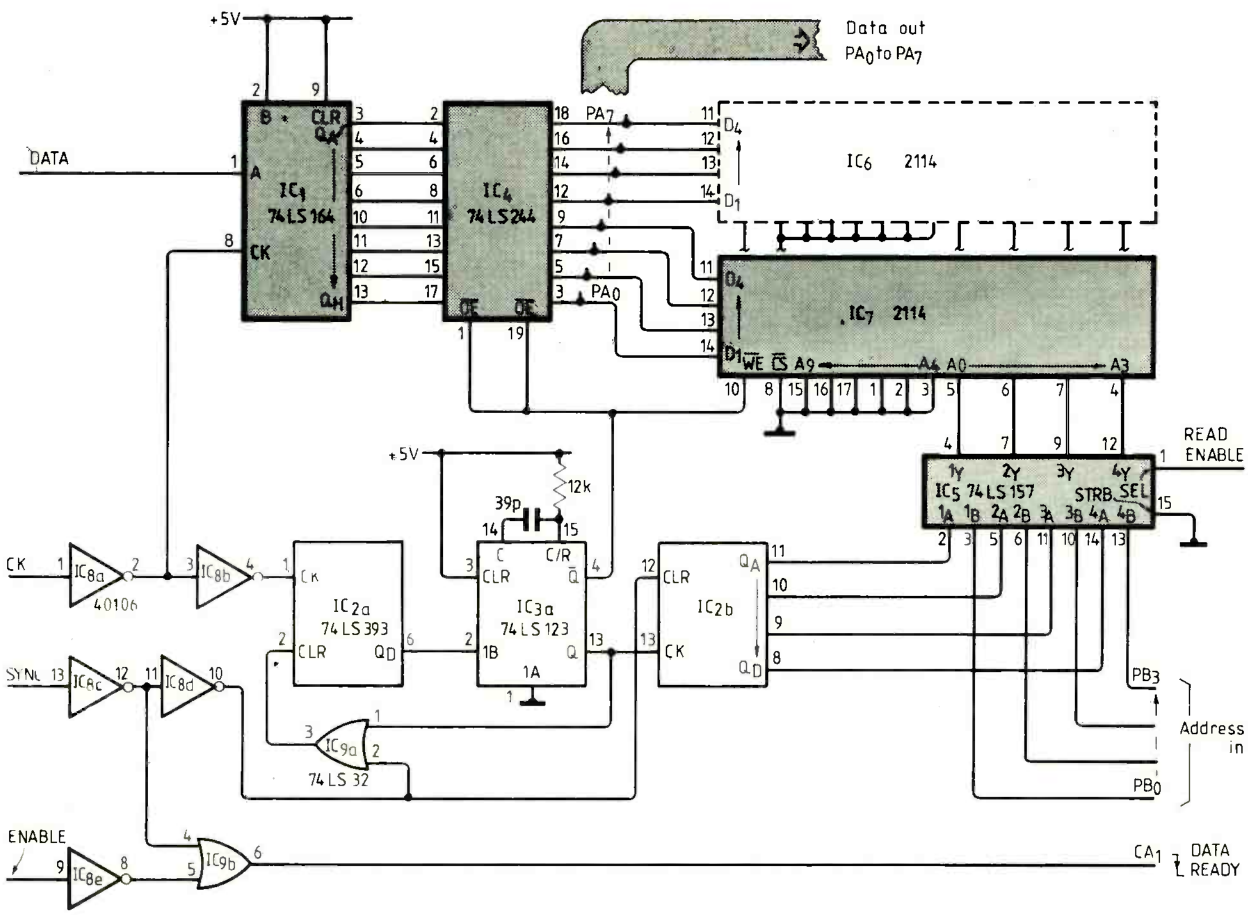
In response to the interrupt, the processor gains access to the ram address lines by taking the multiplexer select input high so that the 12 bytes can be read. Data must be read within 1.3ms of the falling edge of DATA READY since the interface generates a write pulse for the next subcode block after this time. Reading can still take place after the DATA READY signal returns high.

In a 6502-based computer with a 6422 v.i.a., the CB_1 input can be used to sense the DATA READY interrupt. Data format is described in Watkinson's article 'Subcodes explained' in *E&WW,* September 1986.

P. Griffiths
Uppingham
Leicestershire.







CIRCUIT IDEAS

One i.c. p.w.m. power amplifier

In this pulse-width-modulated amplifier intended for voice-grade communications receivers, a UC3637 switched-mode control i.c. functions as a class AD audio power amplifier.

Bandwidth is 300Hz to 2kHz, voltage gain is around 10 and maximum input voltage is about 1V pk-pk. These quantities are impossible to measure directly because audio output is available only as sound from the loudspeaker. Electrical output from the amplifier is a pulse waveform which the loudspeaker filters to form the audio signal.

The amplifier operates in an open loop configuration with output switching frequency set to 30kHz. Closed-loop operation is possible but the switching frequency must be increased to the point where switching losses become excessive. Without feedback, the 3637's pulse-width modulator is very linear.

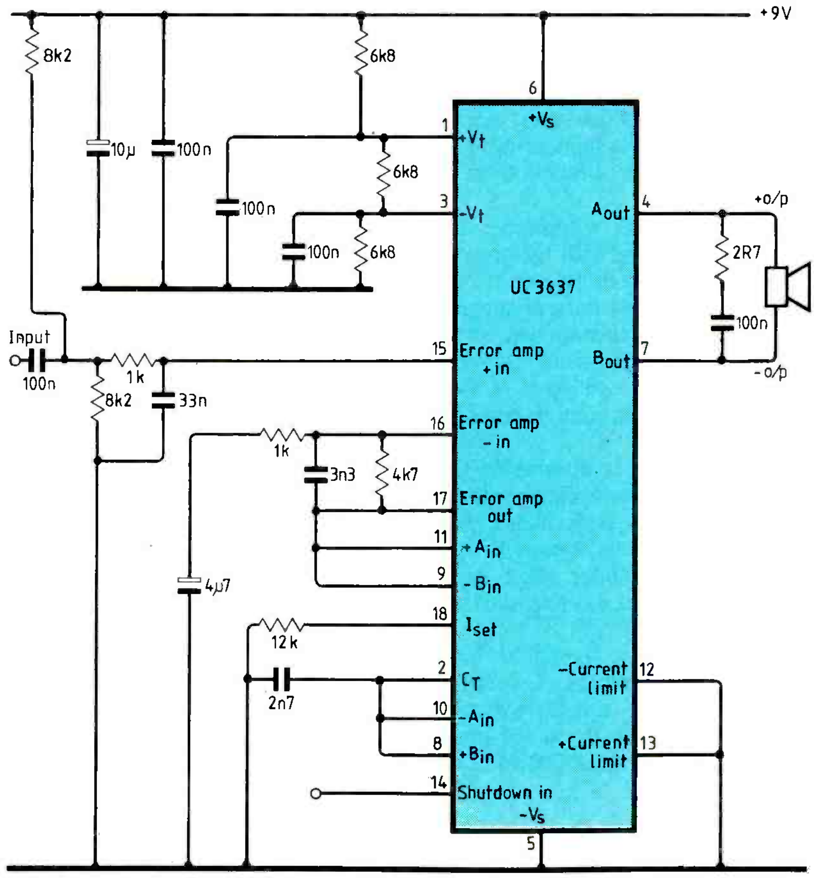
A small 8Ω loudspeaker can be driven at adequate volume levels but for safe continuous operation, the amplifier should drive a load resistance of at least 30Ω. Addition of a four-transistor H-bridge driver would increase output capability.

Supply current is 145mA during normal operation with a 30Ω load. Taking the shutdown input high, to about 7V or higher, or letting if float reduces supply current to 29mA.

A low-pass filter at the amplifier input is designed for 600Ω. If this value is different, adjust the value of the 1kΩ resistor connected to pin 15 so that the sum of this resistor and the output resistance is about 1.6kΩ.

The entire amplifier, including the loudspeaker, should be shielded to prevent radiated r.f.i.

G. Embler
Palo Alto
California



Call-cost calculator

If you have meter pulses on your telephone line, a cheap pocket calculator and simple circuit can be used to monitor call costs without making physical contact with the telephone line.

To put the meter pulses on your line, BT will charge about £17 and a £2.50 a quarter rental charge* thereafter. The pulses are easily distinguished from other line currents since they are high-amplitude signals fed down both wires of the line in parallel and earth referenced.

All that's needed to detect the pulses is a capacitive pick-up device consisting of a dozen turns of wire wrapped around the telephone line (or a medium-sized Bulldog clip). Earth connection can be made to a nearby radiator or pipe of any sort.

The circuit is based on a quad analogue-gate and can be made small enough to fit inside a pocket calculator. It is powered from the calculator batteries and draws very little current in standby mode.

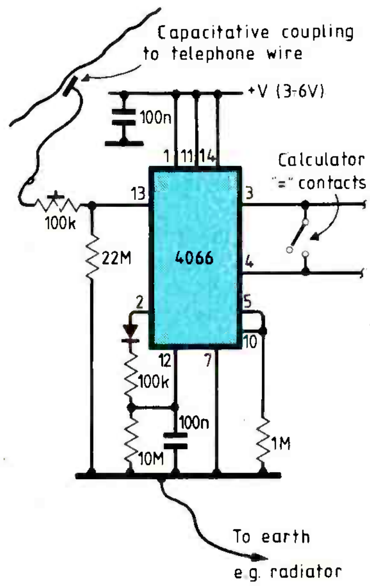
Functionally the circuit consists of a high-impedance buffer followed by a rectifier and smoothing network to reject short-duration interference. The final stage cleans up the pulse and provides a switch output.

Output connections are wired in parallel with the calculator keypad "=" key. The calculator should have an auto-constant facility, as most do. Try to obtain a calculator without automatic shut-off, otherwise the setting-up procedure will have to be carried out each time a call is made.

Before making a call, press the clear key, enter the unit cost (currently 5.75p), press the plus key twice, then press the equal key. Check counting by pressing the equal key, then press zero. Each time a pulse is received, the calculator adds the unit cost to the displayed total. The total can be left to accumulate or be zeroed before each call is made.

Making connections on some types of calculator keyboards may prove difficult, though a combination of screws, conductive paint and solder will cope with most types.

John Hartley
Amersham
Buckinghamshire



*Pre-November rates.

CIRCUIT IDEAS

Autobiasing preamplifier

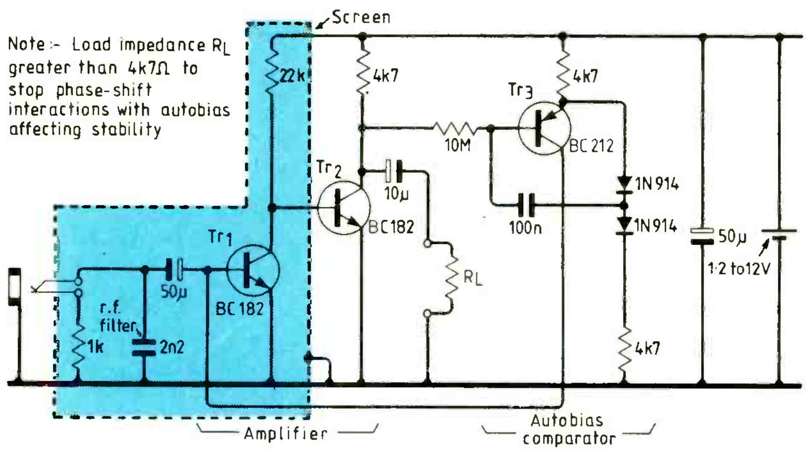
Resistor-based autobiasing circuits do not work well with low supply voltages. This general-purpose preamplifier uses active autobiasing and runs with supplies from 1.2 to at least 12V, taking about 0.5mA from a 2.4V supply.

Active autobiasing uses a transistor to compare mean output level with a reference voltage and feed back corrections even at low supply voltages. In most low-noise preamplifiers, V_{CE} is kept small to minimize shot noise. Here, the first transistor is kept almost saturated and the collector of the second is at mid-rail for maximum output-voltage swing.

Low-frequency roll-off is determined by the low-pass filter used to average output level and high-frequency performance depends on transistor characteristics. With the input open-circuit, the filter must give sufficient attenuation near d.c. to make the autobiasing stable.

Input-signal impedance should be less than about 1kΩ, and amplitude a few millivolts, so the amplifier is suitable for coil microphones and tape heads. In the prototype, $Tr_{1,2}$ had gains of about 500 and Tr_3 about 190.

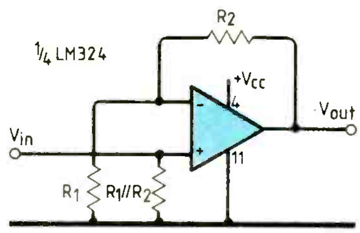
P.J. Ratcliffe
Stevenage
Hertfordshire



Half-wave rectifier

A basic LM324 non-inverting amplifier working from a single-rail supply can be considered as a precision half-wave rectifier. Note that the peak negative value of V_{in} must not exceed 300mV. For higher voltage, add a series resistor at the input to form a potential divider. A coupling capacitor may be used if necessary.

Kerim Fahme
Autolight
Aleppo
Syria



Compact digital echo unit ▶

Despite its simplicity, this compact sound-delay unit gives a repeating echo with a half-second period and good fidelity. Input and output are at line level and current consumption is about 65mA.

Two controls are provided; the delay-time control gives the period between echos and the recirculate control sets the fraction of the delayed signal fed back to give multiple echos. The unit's single 64K-bit ram i.c. gives a comparable memory to echo units with eight-bit converters and 8K-byte of storage.

Simplicity is achieved through use of a type of digital/analogue conversion known as delta-sigma modulation. As well as requiring few components, this type of converter produces only one output bit and so does not suffer from the same kind of clipping distortion that occurs when conventional converters are overdriven. Instead, over-large signals cause slew-rate distortion which is far less noticeable to the ear. This means that far less headroom needs to be allowed for sound peaks when setting up and the overall signal-to-noise ratio is correspondingly increased.

Each memory location is selected in turn; on each selection, old contents are read and new data is written. Time taken to cycle round all 65536 locations is the echo or delay time.

Counter IC_9 is constantly clocked at around 500kHz by the oscillator formed by $IC_{11a,b}$. This counter is used as a sequencer to control the rest of the digital electronics. It counts through four phases 00, 10, 01 and 11, performing the following actions.

In phase 00, IC_{11c} goes low, incrementing the main address counter $IC_{7,8}$. During the rest of this state, the address counter ripples through and settles down.

During phase 10, IC_{11d} pulls the memory RAS line low. This causes the memory to latch the low eight bits of the address counter and takes care of memory refresh. At about 30ns after RAS, the signal propagates through the delay section around IC_{10b}. This causes data selectors $IC_{5,6}$ to switch and present the high-order eight bits of data to the memory. At the same time, CAS is pulled low.

Phase 01 causes the memory device to recall its stored information for the current address and put it on pin 14. This data is latched into IC_{3b} on the transition to the next state.

The memory's WE line is held low during phase 11, causing data from IC_{3a} to overwrite the data that has just been read out. At the end of the state, CAS, RAS and WE all go high and IC_{3a} is clocked to fetch a new bit from the input.

I have built the unit into an existing commercial mixing desk between the echo-send and echo-return connections. It is wired so that it switches out when an external effects unit is plugged in. However the circuit can be used as a stand-alone unit without modification.

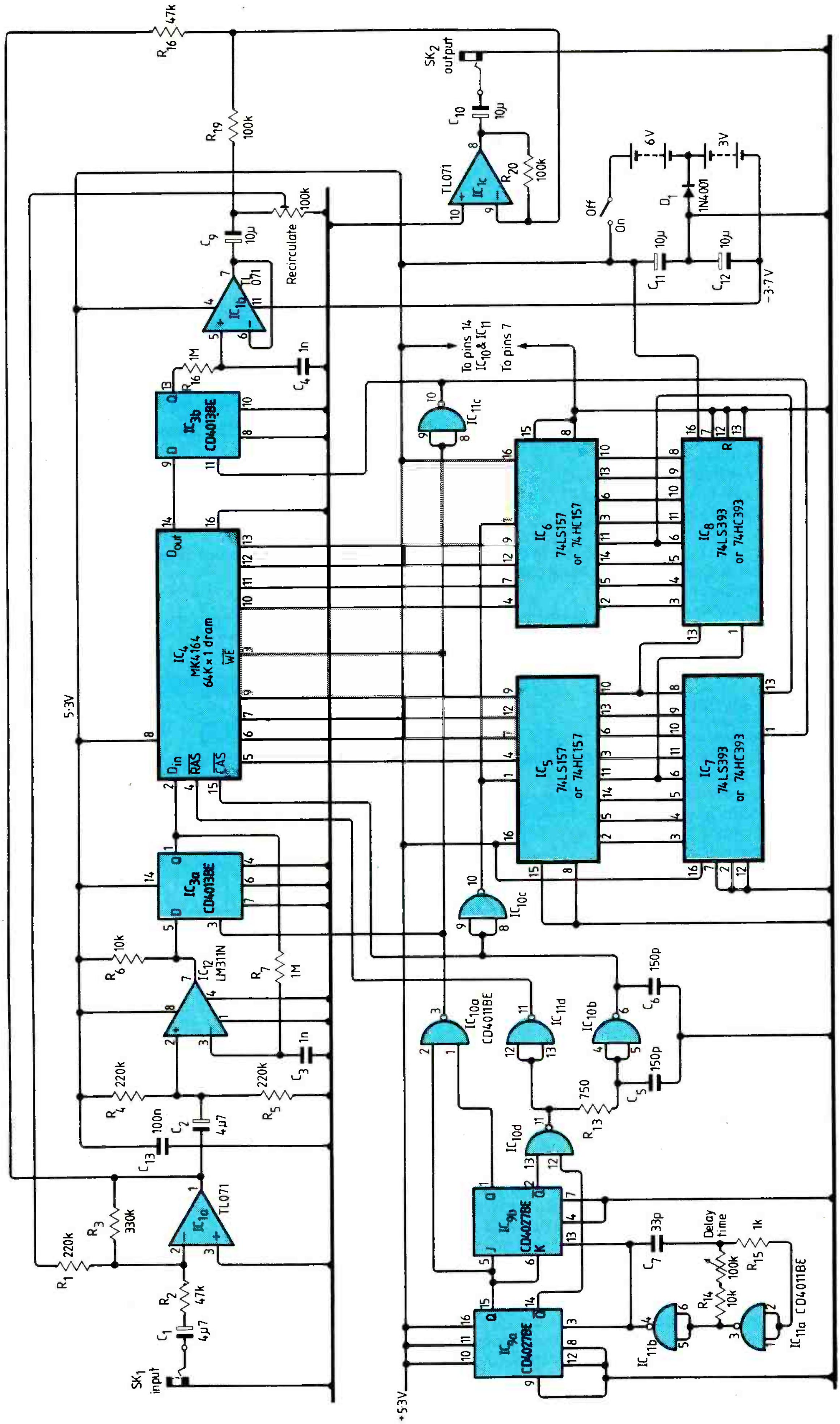
Using battery power only a single-pole on/off switch is needed. When the circuit is switched off, the diode prevents power drain from the −3V battery.

D.J. Greaves
St John's College
Cambrige

DON'T WASTE GOOD IDEAS
We prefer circuit idea contributions with neat drawings and widely-spaced typescripts, but we would rather have scribbles on "the back of an envelope" than let good ideas be wasted.

Submissions are judged on originality and/or usefulness so these points should be brought to the fore, preferably in the first sentence.

Minimum payment of £35 is made for published circuits, normally early in the month following publication.


SK1 input
SK2 output
C1 4μ7
R2 47k
R1 220k
R3 330k
IC1a TL071
C13 100n
C2 4μ7
R4 220k
R5 220k
IC12 LM311N
R6 10k
R7 1M
C3 1n
IC3a CD4013BE
5·3V
IC4 MK4164 64K × 1 dram
IC3b CD4013BE
R16 1M
C4 1n
IC1b TL071
C9 10μ
Recirculate 100k
R19 100k
R16 47k
IC1c TL071
R20 100k
C10 10μ
IC5 74LS157 or 74HC157
IC6 74LS157 or 74HC157
IC7 74LS393 or 74HC393
IC8 74LS393 or 74HC393
IC10c
IC11c
To pins 14 IC10 & IC11
To pins 7
Off
On
6V
3V
D1 1N4001
C11 10μ
C12 10μ
-3·7V
IC10a CD4011BE
IC11d
IC10b
C6 150p
C5 150p
R13 750
IC10d
IC9b CD4027BE
IC9a CD4027BE
C7 33p
Delay time
R14 10k
100k
R15 1k
IC11b
IC11a CD4011BE
+5·3V

Wide-area binary paging

To conclude this two-part article, an examination of the signalling formats used in radio-paging.

J.C. KIRBY

A number of different signalling formats exist. Among them GOLAY and POCSAG been adopted by pager manufacturers. POCSAG is the Post Office Code Standardisation Advisory Group format; the GOLAY code comes from Motorola.

A POCSAG transmission always begins with a preamble followed by a batch of codewords (Fig.4). The preamble consists of alternating ones and noughts repeated for at least 576 bits, enough for the paging units to acquire bit synchronization. The bit rate is 512 bits per second and so the preamble lasts for just over one second.

Every batch must contain 17 codewords, each 32 bits long. The first is a synchronization codeword, to give the pager word synchronization (Fig.5). Eight frames each of two codewords must follow. These may be address codewords, message codewords or idle codewords.

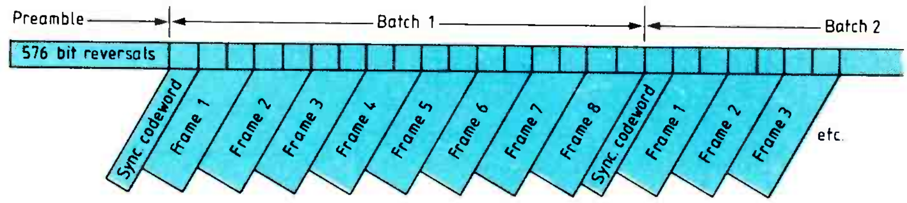


Fig.4. Data structure of POCSAG code. There are two codewords in every frame, eight frames plus one extra codeword in every batch.

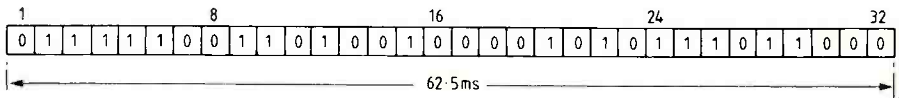


Fig.5. Synchronization codeword for POCSAG. The word takes 62.5ms to send; its bit pattern never changes.

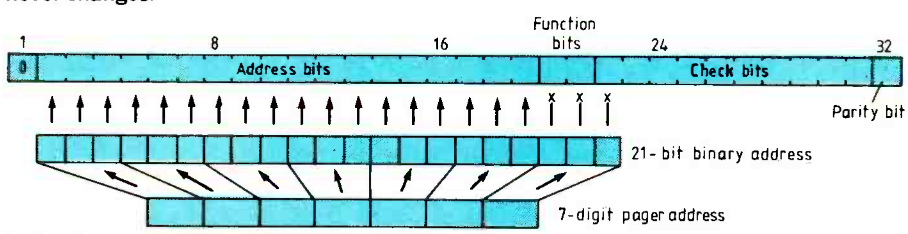


Fig.6. Address codewords. Bits 2-19 uniquely identify a single paging receiver.

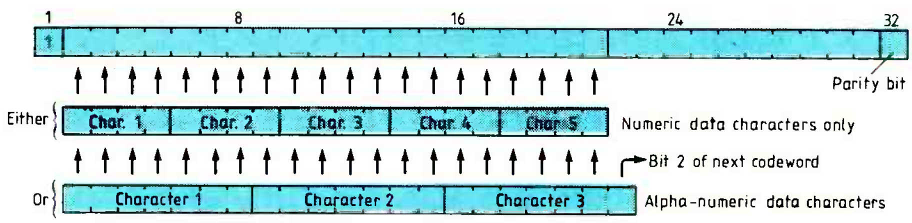


Fig.7. POCSAG message codewords. Twenty message bits are available: when seven-bit alpha-numeric text is being sent, some characters become split between one codeword and the next.

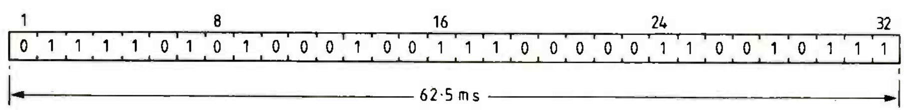


Fig.8. Idle codeword. This bit pattern may not occur in any other codeword.

ADDRESS CODEWORDS

The structure of an address codeword is illustrated in Fig.6. Bit 1 is always zero. The next 18 bits distinguish the address of the pager. POCSAG pagers have seven-digit decimal address codes which translate into 21 binary bits. Only the most significant 18 bits are transmitted, however, the remaining three address bits serving to define which of the eight frames in the address codeword will be used for transmission of the address code. Bits 20 and 21 offer four different function codes indicating to the pager which sequence of bleeps to use during alert.

Ten parity check bits follow. These correspond to the co-efficients of the terms from x^9 and x^0 in the remainder polynomial when a polynomial having terms x^{31} down to x^{10} (the first 21 information bits) is divided, modulo 2, by the generating polynomial $x^{10}+x^9+x^8+x^6+x^5+x^3+1$.

Using check bits means that one or two bit errors in 32 bits of address codeword can be corrected by the pager. The final bit of the codeword (bit 32) is an even parity check bit for the whole codeword.

MESSAGE CODEWORDS

Structure of a message codeword is illustrated in Fig.7. Bit 1 is always set to binary 1. The next 20 bits in the message codeword identify characters to be displayed, but this depends upon the type of pager. The character set of a numeric-only display pager consists of figures 0 to 9, a star symbol, the letter U, a space, hyphen and comma. These 15 characters require 4 bits (0000-1111), so five numeric characters are sent per message codeword.

In the case of the alpha-numeric display pager, 128 characters are defined (although not all are printable), and seven bits are required per character. Three seven-bit characters cannot fit into 20 bits and so remaining bits of a character are sent in the next message codeword.

The 10 check bits are again calculated from the first 21 bits of the codeword. Bit 32 is always an even parity bit. Once message codewords have begun, they continue until the end of the message is reached, except that a synchronization code word must be inserted after each 18 frames to maintain the batch structure.

One bit error in 32 bits can be corrected from a message codeword.

IDLE CODEWORD

The idle codeword, a pattern of bits which can never occur randomly, is transmitted in the absence of any address or message codewords. It may fill a part-used frame, or can pad out the batch to its correct length (Fig.8).

GOLAY

The GOLAY sequential code (GSC) is truly asynchronous. It has functional addressing, which means that the actual address code determines how the pager will bleep. (In

POCSAG the function code is separate.)

A design objective was to produce a code suitable for use on a channel carrying both voice and data paging. No system operator in the UK, to the writer's knowledge, ever mixes binary data (f.s.k.) and voice (f.m.) on the same wide-area paging channel.

Transmissions are usually batched for maximum throughput, although GOLAY allows transmission of individual calls. For example an urgent call to a hospital team can be transmitted immediately upon receipt, where even a 30 second maximum batch wait may be too long.

GOLAY's preamble is complicated (Fig.9). The word repeated in the preamble is selected from a choice of ten. Ten preambles divide the population of pagers into ten groups except where pagers without any battery-saving feature are used. In this case the same preamble is common to all pagers and the addressing capacity of the system is reduced by a factor of ten.

In addition, the polarity of the preamble words signifies whether an individual or a batch call is due.

The preamble is sent at 300 bit/s except during the comma, and it lasts 1.4s. The comma is simply a sequence of 14 bit reversals transmitted at 600 bit/s.

CODEWORDS

A start codeword, an activation codeword and an address codeword all have the same format (Fig.10) and take 0.202s seconds to transmit.

Each codeword has a comma and two words and a 'gap'. The two words are separated by a gap of half a bit (at 300 bit/s). The gap bit is opposite in polarity to the first bit of the word which follows. The words within the codeword have 12 information bits and 11 parity bits.

Within the address codeword, word 1 has only 50 possible values and word 2 has about 2000 possible values; so the number of possible combinations is 100 000. Since there are ten possible preambles and pagers distinguish between them, a maximum code capacity of one million is realized.

Complements of each address codeword are also recognized by pagers providing four more addresses for each code.

DATA BLOCKS

Data blocks, transmitted at 600 bit/s, also last for 0.202 seconds. The gap is at the beginning. Following on are eight words of 15 bits each. Data is encoded using the 15,7 cyclic BCH code. Eight alpha characters or twelve numeric data characters are encoded into one data block (Fig.11).

This tone-only pager can produce four different bleep patterns.

Message length is limited to 80 alpha characters, because there is a maximum limit of ten consecutive data blocks.

Error correction is good: three errors can be corrected in 23 bits of address information, and 16 errors in 120 bits of message.

GOLAY OR POCSAG THEN?

Consider the features of each format (Table 2). The fade-length comparisons suggest that if a GOLAY subscriber has received an alert, then he is more likely to receive an uncorrupted message. POCSAG, on the other hand, offers more correction to its address information than for its data information.

Bit synchronization is essential to POCSAG, and pagers acquire bit synchronization during the preamble. Since groups of POCSAG pagers are assigned specific time slots, they can switch into low current mode for periods whilst calls are transmitted to other POCSAG pagers. This achieves a reasonable battery life, but may sacrifice, according to Motorola, flexibility to permit other code formats and voice on the same channel. Another preamble must be sent before the next batch of POCSAG data, since pagers will have lost synchronization during the transmission of speech and other formats. The argument is that extra transmission of preamble results in wasted air time.

Since GOLAY is an asynchronous code, its pages can be interspersed randomly among the transmission of voice etc. This gives, it is suggested, greater flexibility of system implementation.

Digital Mobile Communications have en-

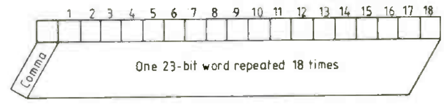


Fig.9. Preamble structure of GOLAY sequential code (Motorola).

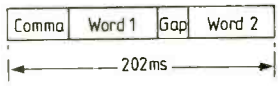


Fig.10. GOLAY codeword format, each word contains 23 bits and is transmitted at 300 bit/s. The gap is equal to half a bit at 300 bit/s.

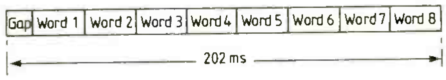


Fig.11. GOLAY data block format. Each word contains 15 bits and is transmitted at 600 bit/s.

countered no problems in operation of either format, but have no plans to create a voice and data channel. Data is transmitted on a v.h.f. frequency, whereas the company's high-quality voice paging service uses a frequency in the u.h.f. band.

All POCSAG mentioned previously refers to the 512 bit/s code, but it should be mentioned that a faster code is being introduced with a signalling rate of 1200 bit/s. All addressing and data coding is identical, but in comparing this with 512 bit/s data, timings etc. should be reduced accordingly. BT Radiopaging hope to implement this before the end of the year. Other operators also have networks capable of 1200 bit/s transmission and are awaiting the supply of pagers.

TABLE 2: features of the two signalling formats

	GOLAY	POCSAG
Code capacity	1 million of 4 addresses	2 million of 4 functions
Tone-only call rate	5 calls per second	15 calls per second
Data call rate (80 characters)	0.45 calls per second	0.52 calls per seconds
Battery saving option	Yes	Yes
Error correction	Yes	Yes
Correction of bit errors:		
Address bits	3 out of 23 bits	2 out of 32 bits
Data bits	16 out of 120 bits	1 out of 32 bits
Max. tolerable signal drop out		
Address word	10ms	4ms
Data word	27ms	2ms

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A standard code for Radiopaging, British Post Office Standard Advisory Group, 1976-1977.

Considerations for Future Paging, *Communications* October 1981.

MPT 1325 VHF and UHF radio transmitters for use at base stations in the wide area paging service, Department of Trade and Industry, 1986.

Quasi-synchronous operation of two or more transmitters, Pye Telecommunications Ltd, 1980.

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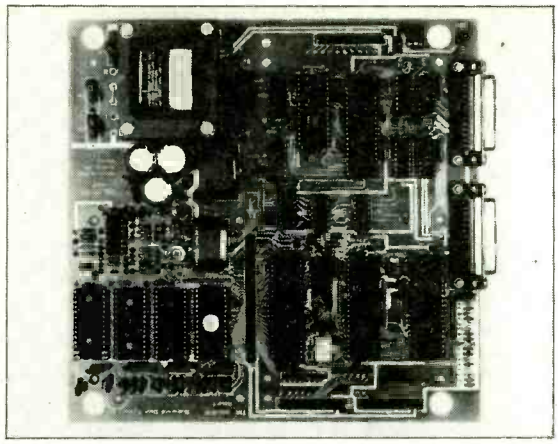

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Getting to the root of root-mean-square

R.m.s. is another expression often used without much thought. JW roots out the true meaning.

JOULES WATT

What is your r.m.s. music power? During very quiet passages, perhaps in the silence just before a dramatic chord – nothing at all!

So do such ideas have any meaning, or are they figments of advertisers' imaginations?

ROOT MEAN SQUARE – OR AVERAGES?

The woolly thinking does not end with amplifiers. I came across a student a short time ago, who was quite convinced that the r.m.s. voltage reading produced by his train of square waves on the AVOmeter a.c. range bore some resemblance to the truth. A quick look at an oscilloscope showing the same square waves indicated how very far out he was. It took quite a while for him to find why he had an 11% error!

Therefore, are the meter manufacturers conning us for some reason, regarding their r.m.s. a.c. ranges? The answer is no – not if you keep strictly to sine waves, because by a bit of juggling of the meter calibration, an *average* has been used to denote an r.m.s. value. You can see at once that in no way could you estimate a music r.m.s. value on such a meter.

The simple sine wave estimation of r.m.s. is achieved by rectifying the wave, then averaging the result and displaying the average – but with r.m.s. values marked on the scale. This process is called finding the m.a.d. (mean average deviation) and in this case use is made of the known relationship between the m.a.d. and the r.m.s. values for a sine wave. All waveforms have r.m.s. values and m.a.d. values as well. But here's the rub; the relation between m.a.d. and r.m.s. varies greatly according to the shape of the waves you are looking at. So, average-reading rectifier meters are strictly for sine waves. Figure 1 illustrates the point.

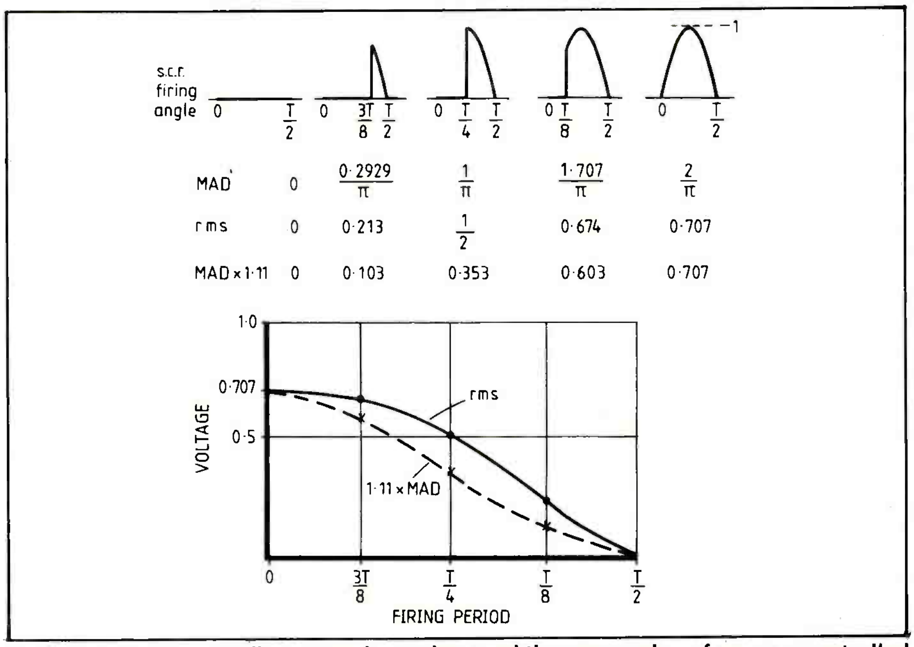

Fig.1. If an average-reading meter is used to read the r.m.s. value of an s.c.r.-controlled waveform, the errors likely might reach 30%.

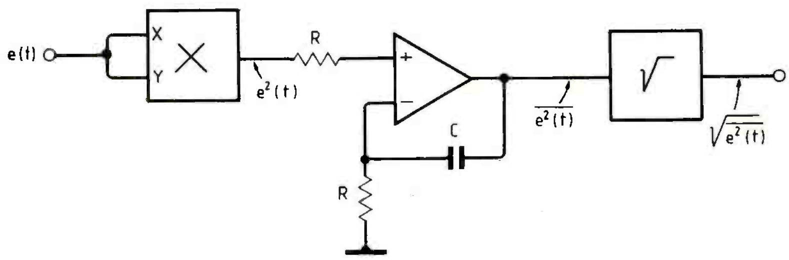

Fig.2. Direct analogue squaring, filtering and square rooting appears easy, but the output dynamic range of the squarer might have to reach thousands to one.

M.a.d. is not the simple average – because for many waveforms and signals such an average is zero: there is no d.c. component. Some people have termed the m.a.d. the "one-sided" average, but this is not very accurate. It is the absolute value that is relevant and its derivation can be written:

$$E_{mad}=\frac{1}{t_o}\int_0^{t_o} e(t)dt$$

where t_o is the averaging time over which the operation is required. As the time passes, the average is up-dated every t_o. This amounts to what statisticians call the running average. Summing the squares of the instantaneous values, averaging, then taking the square root yields the r.m.s. value:

$$E_{rms}=\sqrt{\frac{1}{t_o}\int_0^{t_o} e^2(t)dt}$$

Finally, there is a maximum value reached by a waveform as it varies about the zero mean. This is the peak value, E_{pk}.

Historically, the ratio of the r.m.s. value to the m.a.d. was called the *form factor* by the power engineers. It was briefly, discussed by Ken Smith in his "Power supplies..." articles.

A ratio of equal significance is that between the peak and the r.m.s. This is called the *crest factor*, and is a measure of the peakiness relative to the energy content of a given wave shape.

Summarizing these ratios:

$$\text{Crest factor} = K_C = \frac{E_{pk}}{E_{rms}}$$

$$\text{Form factor} = K_F = \frac{E_{rms}}{E_{rmd}}$$

POWER

An even worse misuse, is the meaningless statement "r.m.s. power" seen on some

TABLE 1. A number of waveforms are here shown with their r.m.s., m.a.d., and K_C values. A true-r.m.s. converter will give the correct value, but errors increase as the crest factor increases.

		r m s	MAD	K_F	K_C
Sine wave	$\hat{V}$, 0	$\frac{\hat{V}}{\sqrt{2}}$	$\frac{2\hat{V}}{\pi}$	$\frac{\pi}{2\sqrt{2}} = 1{\cdot}111$	$\sqrt{2} = 1{\cdot}414$
Triangular wave	$\hat{V}$, 0	$\frac{\hat{V}}{\sqrt{3}}$	$\frac{\hat{V}}{2}$	$\frac{2}{\sqrt{3}} = 1{\cdot}155$	$\sqrt{3} = 1{\cdot}732$
Symmetrical square wave	$\hat{V}$, 0	$\hat{V}$	$\hat{V}$	1	1
Pulses	δ-duty factor, $\hat{V}$, δT, 0, T	$\hat{V}\sqrt{\delta}$	$\hat{V}\delta$	$\frac{1}{\sqrt{\delta}}$	$\frac{1}{\sqrt{\delta}}$

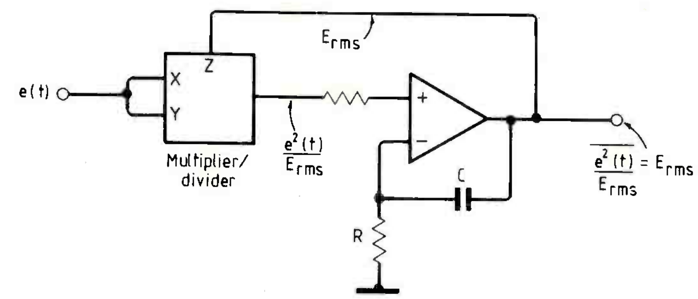

Fig.3. The circuit block at the front end of an implicit r.m.s. converter is a multiplier/divider which yields a much lower output dynamic range requirement.

specifications. There is an r.m.s. *voltage* or an r.m.s. *current*, but what can r.m.s. power mean? Power is rate of using energy. This can vary with time and therefore an instantaneous peak power can be talked about and the *average* is the appropriate quality for a mean over a given time – not r.m.s.

R.M.S TO D.C. CONVERSION

The measure of true r.m.s. values must be a little more detailed than the simple methods common in a.c. meters. A direct application of the expression for r.m.s. can be realised by analogue methods.

Figure 2 illustrates the use of a squaring circuit followed by an averager (i.e. a low pass filter with a characteristic time t_o together with a square-rooter. The main problem with this approach is the dynamic range. If you suppose that an input signal has a dynamic range of 100:1, (100mV to 10V, say), then the output of the squarer must have a dynamic range of 10 000:1.

By using a three-input multiplier/divider device, this problem can be overcome. Figure 3 shows the diagram of what is known as an implicit r.m.s. computing circuit. Because E_{rms} is a very slowly changing voltage over the averaging time, it passes the averager very nearly unchanged. In other words, it can be used to carry out the division *before* the averaging. The output of the first stage now has a dynamic range of the same order as the input.

What now limits the signal handling capacity of these r.m.s. circuits is the crest factor. Large crest factors means high peaks with rather small r.m.s. values. The dynamic range has to be wide enough to cope without limiting – which would introduce errors.

Table 1 lists a few of the more common waveshapes with the appropriate factors and quantities. Noise and music waveforms are not deterministic in this way, and their statistical properties are all we have.

SPECIALIZED CHIPS

The Linear Device people have come up with chips that will do the whole job. All the designer has to do is watch the levels for the dynamic range and set the time constant component values for the desired averaging time. Analog Devices market the 536^2, which is a dedicated r.m.s.-to-d.c. converter. Raytheon produce a logarithmic multiplier chip (the type 4200) which implements r.m.s. measurements with a minimum of external components.

Finally, digital realisation of the r.m.s. conversion function has been implemented – as one might expect. One way used an eprom look-up table for the squaring operation, summed and stored a whole series of the squared data words (over a one second period, say) then passed the accumulated data, after division by the number of samples, to a digital square rooter. The final eight-bit word represented the r.m.s. value.

References

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Hands-on engineers

continued from page 27

which come in are split into orderly streams which can be analysed and interpreted and put into practical engineering form (data marshalling). This process is far from being as simple as it looks, and whether it is, for example, for a far-reaching R&D project or for the complete design of a large scale control system, the need for the widest possible hands-on experience cannot be over-emphasised.

The final conclusion is that the need for staff of the highest calibre to be used applies even for minor fault investigation. This principle is so often obscured by the fact that the solution to a difficult fault turns out to be simple in the extreme – as with a good invention – and in retrospect it is not easy to see how the expenditure of so much effort was required. In response it may be added that one of the indirect objectives of working in this way is to ensure as far as possible that vital information is not missed, something which has to be borne in mind throughout the whole duration of a project.

This, then, is the final picture seen from the point of view of someone wishing to establish that there has been a return to a management attitude (virtually a change in way of thinking) which recognizes the importance of putting 'staff engineers' on work containing any form of unknown, even if it does seem beneath them. In parenthesis, it should be added that the world has been made fully aware that a single, isolated, elementary fault can cause the complete breakdown of the biggest installation both on Earth and in space.

The term 'staff engineer' has been chosen for what has become a somewhat indeterminate classification which, as already implied, is needed to cover those who provide the modern equivalent of "...designing works of public utility (given in the context of bridges, canals, gas works etc.)" as well as continuing to meet these original requirements of providing ultimate service to humanity. This is not the purely academic issue which it may seem – as many will know, this question of name, and all that goes with it, have exercised the minds of representative bodies over the years; and it is becoming increasingly clear that, on the grounds of defining responsibility alone, a satisfactory title has to be found for this vital section of the community.

This whole matter has been ventilated, perhaps slightly indirectly, by the writer in a *Wireless World* article (March 1985). The problem to be met here is that of relating educational qualifications to the name Chartered Engineer – an obvious choice. In the discussion given in the *Wireless World* article, apart from commending the HNC route, (particularly suited to 'generally' hands-on engineers) it is suggested that a return to giving recognition to the three R's would be more than desirable; and it is of interest that such a return in now being put forward as near-mandatory, literally at government level.

Trunked mobile radio in Band III

GEC's national voice-and-data network uses the shared-system concept to offer a wide range of communications services to businesses small and large.

P.J. DELOW

In recent years users have been increasingly attracted by shared systems, such as common base stations and message handling. Growth rates in this market area are several times greater than for p.m.r. as a whole, reflecting the user benefits; such shared systems can offer considerable spectrum efficiency improvements, particularly if trunking techniques are employed.

GEC will use its allocation of spectrum to construct an integrated network which will provide a full range of communications facilities for the business users. This network will overcome the shortcomings of existing shared systems, particularly coverage limitations, and will offer services not currently available.

The network concept is illustrated in Fig.1. This diagram assumes a selective mobile-to-mobile call, but other classes of call are treated similarly. Mobiles communicate through their respective trunked common base stations, which are interconnected by a voice and data switching network. This allows authorised mobiles to communicate as they roam throughout the combined coverage area of the networked base stations.

Mobiles and network communicate by digital signalling, either on nominated control channels when a call is not in progress, or by blank-and-burst signalling during a call. Each base station has available a pool of frequency pairs which are assigned to calls on demand. Accordingly, mobiles must be frequency-agile (synthesized) over the band used by the network.

The voice and data switching network includes digital voice switches, packet data switches and digital transmission links. Setting-up and clearing down of calls within this network is vested in a network control sub-system. This is shown conceptually in Fig.1. as a single element, but in the real network a number of processors will be distributed throughout its extent. This control sub-system is assisted by a network data-base which holds up-to-date information on users, including tracking data to enable the network to locate them easily. The network data-base is also a distributed sub-system.

Performance of the network is monitored and optimized by a network management sub-system. This is also responsible for maintaining a central register of users and providing billing information.

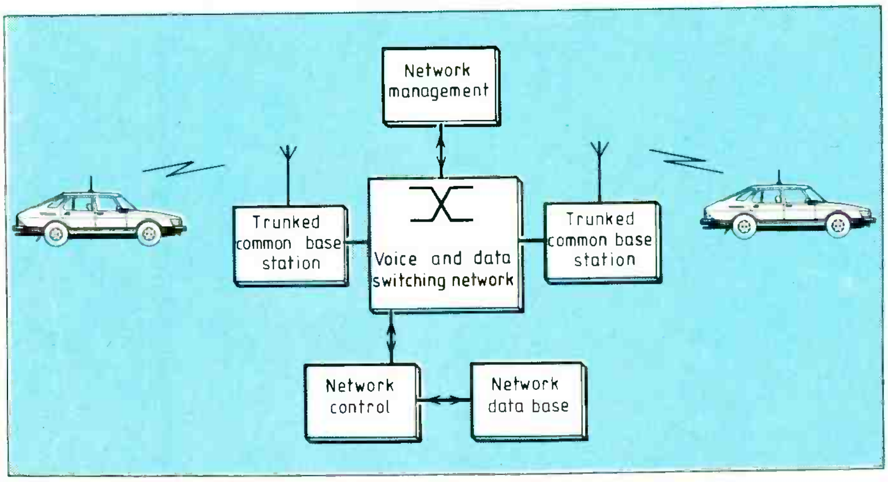


Fig.1. How the system handles a mobile-to-mobile call. Users are free to communicate throughout the area covered by the network of base stations.

NETWORK REALIZATION

The network is arranged in a four-level hierarchy. At the lowest level are the mobile unit and customer's fixed terminal equipment.

Base stations, grouped into traffic areas, occupy the second level of the hierarchy. All base stations within the same traffic area are connected, in a star configuration, to a traffic area switching centre (TASC). This forms the third level in the hierarchy, the highest at which call set-up operations are carried out.

A network management centre (NMC) occupies the topmost level. It serves as overseer of the general system operation, maintains customer records and collates billing and traffic data.

USER INTERFACE

The British government licence terms for Band III network operators will prohibit them from dealing directly with end users, except in special circumstances. Accordingly, service providers will have to be appointed to act as a link between the network operators and the users. Service providers will be reponsible for the terminal equipment, mobile and fixed, which customers operate.

To ensure satisfactory peformance, this equipment must be totally compatible with the network. However, it is highly desirable

FACILITIES OFFERED

GEC's national network will provide a flexible carrier for basic voice and data communications. The limits to these facilities will probably be set by commercial and regulatory considerations, rather than technical constraints. Current plans embody the following services:

VOICE SERVICES
- selective, two-party calls
- fleet calls (broadcast and group)
- dispatcher facilities (including queueing and multi-desk working)
- priority and emergency
- unattended mode (storage of call data at the mobile for call-back)
- p.a.b.x. incoming and outgoing calls
- p.s.t.n. outgoing calls – mobile to telephone unit
- advice of call transfer
- value-added voice services

DATA SERVICES
- status reporting
- circuit-switched data (audio band)
- store-and-forward short data messages
- shared data channel
- bureau data services
- access to public data services
- vehicle tracking and security

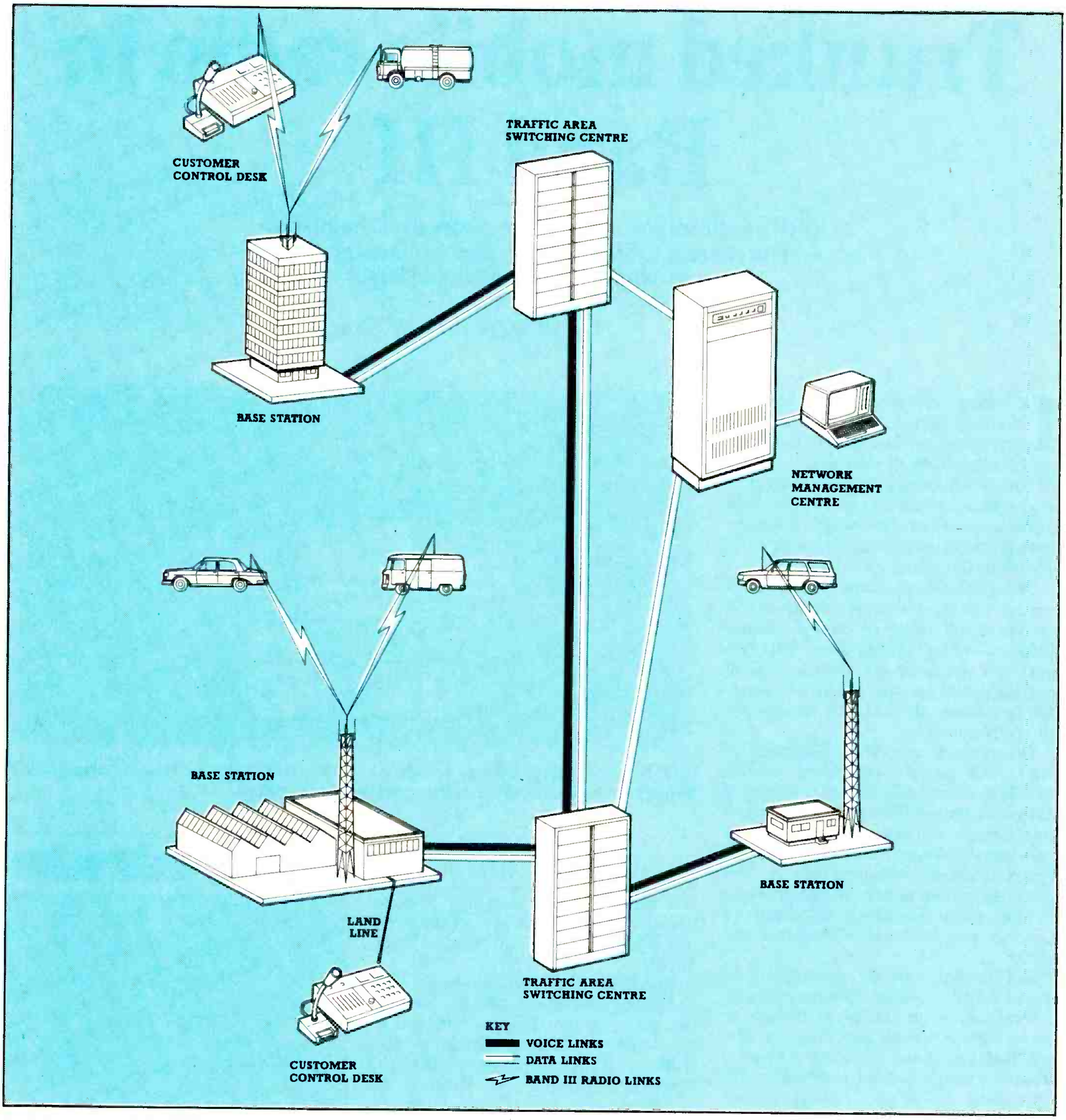


Fig.2. Structure of the GEC network. A common pool of communications channels is shared out dynamically.

that users should have a choice of equipment and scope for customization to suit their own requirements. These requirements can be met by specifying two standard interfaces between the network and users' equipment: the air interface and the line interface. Providing these specifications are satisfied, service providers and customers will be free to configure the terminal equipment as they desire.

The air interface will provide a standard for units which use Band III radio as their means of interconnection with the network. This will encompass all mobile units and some 'fixed mobile' control units. The air interface specification is being produced by a collaboration between the Department of Trade and Industry, the network operators and the service providers. It is based on the work carried out to produce the digital signalling standard for trunked systems, MPT1327.

When work is complete the air interface specification will be published and all radio equipment offered for Band III networks will be required to comply with it. This will allow users to benefit from freedom of choice and price competition and should enable manufacturers to enjoy economies of scale.

LINE INTERFACE

Many users will find that their communications requirements will be best satisfied by a direct line connection from their office, control centre or p.a.b.x. into the network. GEC will publish a line interface specification to enable service providers to obtain suitable equipments.

In view of the relatively small volume of the fixed equipment market compared to the mobile market and the greater variability to be expected between networks in the technical realization of a line interconnection, the DTI are not sponsoring a common line interface between all networks.

The line interface will be provided by a line terminating unit, which can be a fairly standard piece of equipment regardless of the customization required to meet special user requirements. These may be met by additional equipment designed individually.

Peter Delow is technical manager of GEC Communication Networks Ltd.

RESEARCH NOTES

A new approach to short term weather forecasting

The UK will soon benefit from a new approach to precision weather forecasting. FRONTIERS, an advanced image manipulation system originally developed by Logica for the Meteorological Office, is to enter service at the Met. Office Headquarters, Bracknell.

FRONTIERS is the result of some five years research at the Met. Office laboratories at Malvern. Logica supported the evolution of the system throughout the research programme and has recently been contracted to build the operational version.

The FRONTIERS concept allows meteorologists to study and correct data from a network of weather radars covering England, Wales and Ireland. The detailed rainfall maps provided by the radars are further enhanced by merging in satellite-derived imagery, giving rainfall fields accurate in both intensity and location. The latter are used to predict the movement of the rain areas for the next six hours.

The system has a high (5km) resolution and uses measurements made in real time, updated every 15 minutes. This permits more accurate and detailed short-term rainfall forecasts than was previously possible.

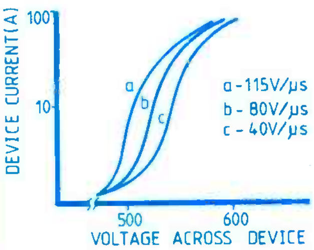
The DEC VAX-based system uses high-resolution graphics and a variety of input devices, including touch-sensitive screens, to provide meteorologists with easy access to the image manipulation facilities.

Metal oxide Varistors and transients

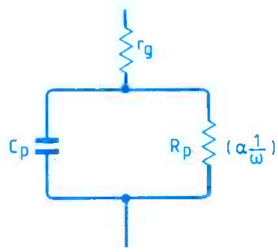
Varistors, as their name implies, are non-linear resistors used to suppress transients and overloads in power switching circuits. They are constructed by sintering together zinc oxide (ZnO) with various other oxide dopants in powder form. The non-linear properties derive from the semiconducting nature of the grain structure in the bulk material.

D. de Cogan and M. Leeson at the University of Nottingham have been investigating a curious feature of Varistors, namely their tendency to pass disproportionately high currents when subject to a voltage pulse. This current overshoot, which has been observed many times in the past, has been assumed to be due to the capacitance of the crystalline microstructure.

Using commercial Varistors, the Nottingham researchers compared the effects of different voltage rise times on the V/I curves of the Varistors. These showed quite clearly that the current through a Varistor at a fixed applied voltage is larger for larger values of dv/dt.



What these curves also show is that the effect is not simply due to the capacitance of the device. It can however be explained by a modification of the popular equivalent circuit, viz:



Since a fast pulse contains a greater proportion of high frequencies, a higher current will flow through Rp. For a pulse of infinite dv/dt, the current is limited only by r_g, the grain resistance.

This response to fast transients probably explains why Varistors are so effective in protecting power semiconductors. But, say the Nottingham researchers, it may also explain why Varistors themselves fail prematurely, unless dv/dt is controlled by a snubber network.

New m.f. broadcasting antenna designs

The US National Association of Broadcasters (NAB) is planning practical tests on two new types of m.f. broadcasting antenna, designed to minimize unwanted skywave. Current antennas, mostly vertical towers or wires, radiate less than 15% of their energy into usable groundwave – the signal that provides the primary service for the listener. Not only is this inefficient, it can also lead to problems after dark when the spurious skywave is reflected back to earth by the D layer of the ionosphere. This can result in co-channel interference hundreds or thousands of kilometres from the primary service area of the transmitter. One of the new antenna designs, by Richard Biby of Communications Engineering Services, Arlington, Va., is based on a conventional vertical monopole, surrounded by a number of short vertical auxiliary radiators. These are placed to increase the groundwave and to cancel out unwanted skywave.

The other novel design to be tried by the NAB is by Ogden Prestholdt of A.D. Ring & Associates, Washington. It employs a combination of vertical, horizontal and diagonal elements to give, it's hoped, separate control over groundwave and skywave components of the signal.

Construction of both experimental antennas is expected to take a year, after which there will be another year of comparative field tests.

67 GHz bandwidth photo-diode

Wideband photodiodes are assuming increasing importance with the growth of infra-red optical communications systems operating in the gigabit/sec region. Primary design considerations are the need to keep the active area small to reduce device capacitance and the need to keep the layers thin to minimize electron transit time. Another limiting factor is the need to keep electrical parasitics as low as possible by mounting the device in a wavelength microstrip or coaxial fitting.

Using a coaxial mount, scientists at AT & T Bell Laboratories, Holmdell, New Jersey, have constructed an indium gallium arsenide (InGaAs) infra-red photodiode with a modulation response from d.c. to 67 GHz. This is the fastest response so far reported for this type of device, a PIN diode with an active area of 150µm^2 and an intrinsic layer thickness of 0.5µm.

The actual frequency response was determined by a Fourier analysis of the impulse response to a 1.3µm laser operating at a repetition rate of 3.7GHz. The AT & T Bell researchers say the 67GHz (3dB) response indicates that parasitics are the limiting factor with the present design. Higher bandwidths may be possible if care is taken to reduce parasitics, though they admit that transit time will prevent a very significant increase.

New insight into dielectric breakdown

Steven R. Kurtz and Robert A. Anderson of the US Sandia National Laboratories have made what they claim to be the first ever direct measurements of charge distribution in the dielectric of a capacitor stressed to near breakdown. This is now providing new insight into why electrical insulation fails and also why it sometimes becomes conductive when subject to intense radiation.

The material Sandia are using for their experiments is Mylar (polyethylene terephthalate), a material commonly used in capacitor construction. Space charge is injected from a high voltage placed across metal films deposited on either side of a Mylar film. The resulting capacitor is then subject to brief pulses of radiation from an infra-red laser, which generate an acoustic wave that propagates through the Mylar film, causing a brief deformation. The resulting localized changes in capacitance, in conjunction with the space charge, generate a current across the metal films which provides a direct measure of the space charge. Knowing the rate at which the acoustic wave propagates through the Mylar then enables the Sandia researchers to create a detailed map of what goes on in every part of the stressed dielectric.

One interesting finding is that the charge distribution near the electrodes does not increase in direct proportion to the applied field. In fact there's a reduction as the field approaches 4MV cm^{-1}. Kurtz and Anderson attribute this to the onset of tunnelling. This, they say, may produce high current densities which ultimately lead to dielectric breakdown.

Space charge mapping is now being used to investigate other properties of Mylar capacitors, including radiation-induced breakdown. Active components, its seems, are not the only ones that are subject to the damaging effects of e.m.p. or cosmic rays from space.

50 farads in a cotton reel

The Insulating Systems Department of ERA Technology has developed and tested a method of making capacitors with an unprecedently high capacitance per unit volume. A 50F 1V unit would be about the size and shape of a cotton reel – $16cm^3$. The energy storage density, about 6 joule/cm^3, has been achieved by exploiting the principle of an electric double layer, already a feature of some commercially available memory back-up capacitors. Up till now, however, these double layer capacitors have not been available in values of more than a few farads.

Although the ERA design has so far only been fabricated experimentally in values of 4-5F, Mike Weller of the Insulating Systems Department believes it is inherently extendable to any required size.

Tests on the prototype indicate discharge characteristics and an ability to retain an almost full charge for many months.

Atomic particles break energy record

Researchers at CERN, the European Laboratory for Particle Physics, have accelerated atomic nuclei to the highest energy ever achieved in the laboratory. CERN's machines, which extend for many kilometres underground, normally work with protons, but to extend their studies of matter, the physicists chose to work with oxygen ions which are 16 times heavier and which carry a double charge. To provide these ions, one of CERN's injector accelerators was adapted in collaboration with the West German Gesellschaft für Schwerionenforschung and the Lawrence Berkeley Laboratory in California. Both these research teams have a strong tradition of research with ion beams, but only CERN's system of interlinked accelerators could provide the energy levels needed.

After leaving the injector, the ions passed through several accelerators, ending up in the Super Proton-Synchrotron (SPS) with an energy level of 3.2 TeV. In absolute terms this isn't a huge amount of energy, but carried on oxygen nuclei, it represents a huge concentration of energy.

Using the ion beams, CERN physicists will search for signs of the so-called 'quark-gluon' plasma, a state of matter thought to exist under extreme conditions where protons and neutrons fuse into a 'soup' of the constituent quarks and gluons. This state of matter is thought to have existed in the first second after the Big Bang that created the Universe and before matter condensed to form atoms and molecules. Preliminary experiments with the oxygen ion beam have already demonstrated that useful results will be achieved when the experimental programme gets fully under way.

CERN's track record with high energy research is already impressive. It was in the SPS accelerator in 1983 that proton/anti-proton collisions revealed evidence of the W and Z particles. These are the particles that mediate the so-called 'weak force', the agent of radioactive decay. The same experiment later provided evidence for yet another building brick of matter, one of the predicted family of 5 quarks, the component parts of neutrons and protons.

Perception of voltage dips

Voltage dips occur on any supply network when load is suddenly applied or disconnected. Most of the time such dips go unnoticed, especially if loads are well-regulated or of a sort that don't rely on continuity, e.g. heating or refrigeration plant. Lighting is entirely different, however. Electricity authorities are frequently faced with complaints about flickering lights, especially in rural areas at the ends of long supply lines.

One solution, though an expensive one, would be to reinforce the supply network to minimize such dips. A more practical approach, and one that's recently been the subject of study at the Electricity Council Research Centre at Capenhurst, is to try and identify the characteristics of supply dips that are most annoying and then take steps to mitigate them.

An experiment was carried out in which people reading were exposed to voltage fluctuations of different waveforms at different time intervals. In each case the source of illumination was a standard tungsten lamp. The percentage modulation of the waveform was adjusted in each case until the subject noticed the fluctuation and until they said that such a fluctuation would be annoying if it occurred regularly.

These tests showed that different waveforms need different percentage modulations for perception and annoyance to occur. In general, the faster the voltage change, the greater the degree of annoyance. This suggests that once a troublesome load has been identified, the effects of switching it on and off could be minimized by the use of a 'soft start' system.

In order to identify the source of voltage dips, it is necessary tc have some means of measuring their subjective effect and for this purpose the ECRC has developed a digital 'flicker meter'. This will predict whether a voltage fluctuation applied to it will cause annoyance to anyone using a tungsten lamp connected to the same supply. Tests have shown that the meter's readings compare very closely with the subjective effects of a large number of different waveforms. It is now available commercially from the licensee Dicoll Electronics Ltd. of Basingstoke.

Polarisation diversity in radar

It has long been acknowledged that polarization is a dimension of radar backscatter that can provide additional target information. However, several factors such as cost, technical complexity and incomplete knowledge have placed severe limits on progress in this field. Up till now, therefore, much of the description of a radar target has been derived from the amplitude, the frequency, the phase and the bearing of the returned signal.

In a paper published by the I.E.E.E., Dino Guili reviews some of the latest developments in radar polarization studies. These include the polarization behaviour of different target objects and ways in which this can change under differing conditions of motion and according to the resolution of the radar.

Dual-polarization radar can now effectively distinguish between light rain, heavy rain, hail and snow on account of the differing shape, and hence reflective properties, of the different hydrometeors.

Guili's paper goes on to look at other valuable features of polarization-diversity radar, including its military potential for obviating or at least minimizing the effects of 'chaff' and jamming. Several technical options are offered for implementing these theoretical possibilities, few of which have yet been studied extensively. Guili concludes that only when experience has been gained with such operational radars will it be possible to assess the techniques definitively. *(Proc. IEEE,* Vol. 74, No. 2)

Cost-effective baseband signal generator

A novel and simple method of generating periodic waveforms

M. CHARNLEY

Although designed specifically to support a research project involved in the investigation of multiplexing strategies suitable for the simultaneous transmission of speech and data over land-mobile radio links[1], the principle used in this design can be extended to cater for many different types of application. An attractive feature of the method used to reproduce various baseband test signals is the fact that, as well as generating sinusoidal test tones at standard audio frequencies, many other user-defined complex signals which extend over a defined bandwidth can be produced and switch-selected when required. In contrast, using standard pieces of test equipment would demand a far greater level of complexity to achieve the same result.

In general, assessment of the dynamic performance of electronic systems, such as amplifiers and filters, usually demands that a suitable test signal be injected at the input and the resulting output waveform examined. In this way, frequency response and distortion can be quantified. Consequently, many pieces of test equipment are available to enable a wide range of performance measurements to be carried out. Although the system to be described does not offer a new performance-assessment strategy, it does provide the engineer with the possibility of developing and using unique waveforms for specific measurement tasks. These customized waveforms can be produced without the need to modify the electronic system used in their generation.

Figure 1 is the block diagram of the configuration which has successfully been used to generate and store a library of periodic baseband signals. Each waveform is stored as a pulse-code-modulated data frame, which consists of 64, 8-bit quantized samples extending over a 5ms sequence. Consequently, each waveform can contain, in theory at least, frequency components extending up to 6.4kHz, as defined by the Nyquist sampling theorem. Increasing the number of samples and/or modifying the data frame length can, of course, enable periodic signals covering a much wider bandwidth to be obtained. However, as previously indicated, the system was designed to provide test signals for a radio telephony speech band up to 3kHz. The stored waveform data samples are output in a cyclic manner, repeating every 5ms as determined by the 12.8kHz clock frequency, as 8-bit codewords to a d-to-a converter.

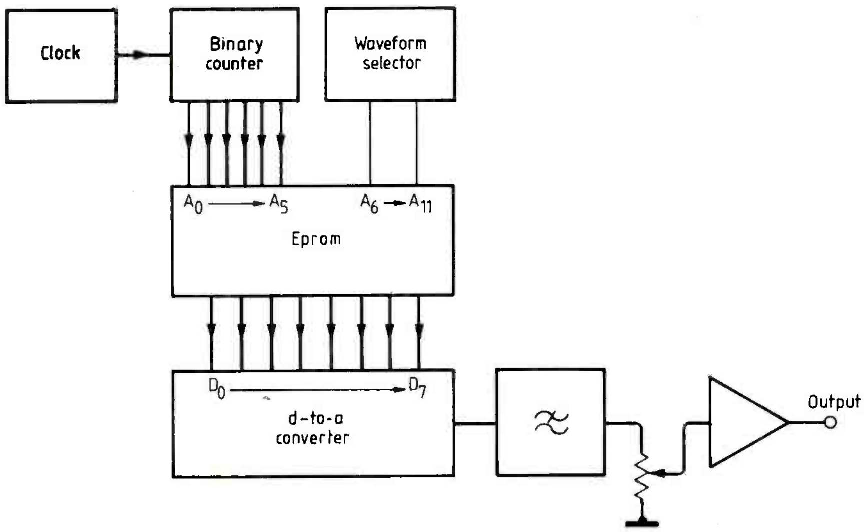


Fig.1. Schematic block diagram of the baseband waveform generator.

In response to the frame sequence of 8-bit data codewords, the converter reproduces a quantized approximation to the stored baseband waveform which has been selected. As Fig.2 shows, the low-order addresses needed to access the 64 data samples per frame are produced by a six-stage binary counter, which in turn is driven by the clock generator. In contrast, the high-order address, which defines the baseband waveform to be generated, is determined by a hex. code thumbwheel switch arrangement. The low cost and availablity of the 2716 eprom makes it an obvious choice for this application: a 64-byte data frame for each individual waveform means that a total of 32 distinct test signals can be catered for, if required, by the standard configuration.

The remaining circuitry following the d-to-a converter consists of a low-pass filter to smooth out the quantized signal from the converter and reproduce the desired band-limited periodic test signal. A means of adjusting the output level has also been included.

A SELECTION OF BASEBAND SIGNALS

As previously indicated, as well as generating standard audio test signals such as 400Hz and 1kHz tones, the stored-waveform technique encourages the design of other different complex test signals. Before reviewing certain signals which have been adopted for investigating the effect of baseband signal processing, it is useful to indicate the quality of sinusoidal test signals that can be obtained using this method. Practical measurements have confirmed that the second-harmonic distortion using this con-

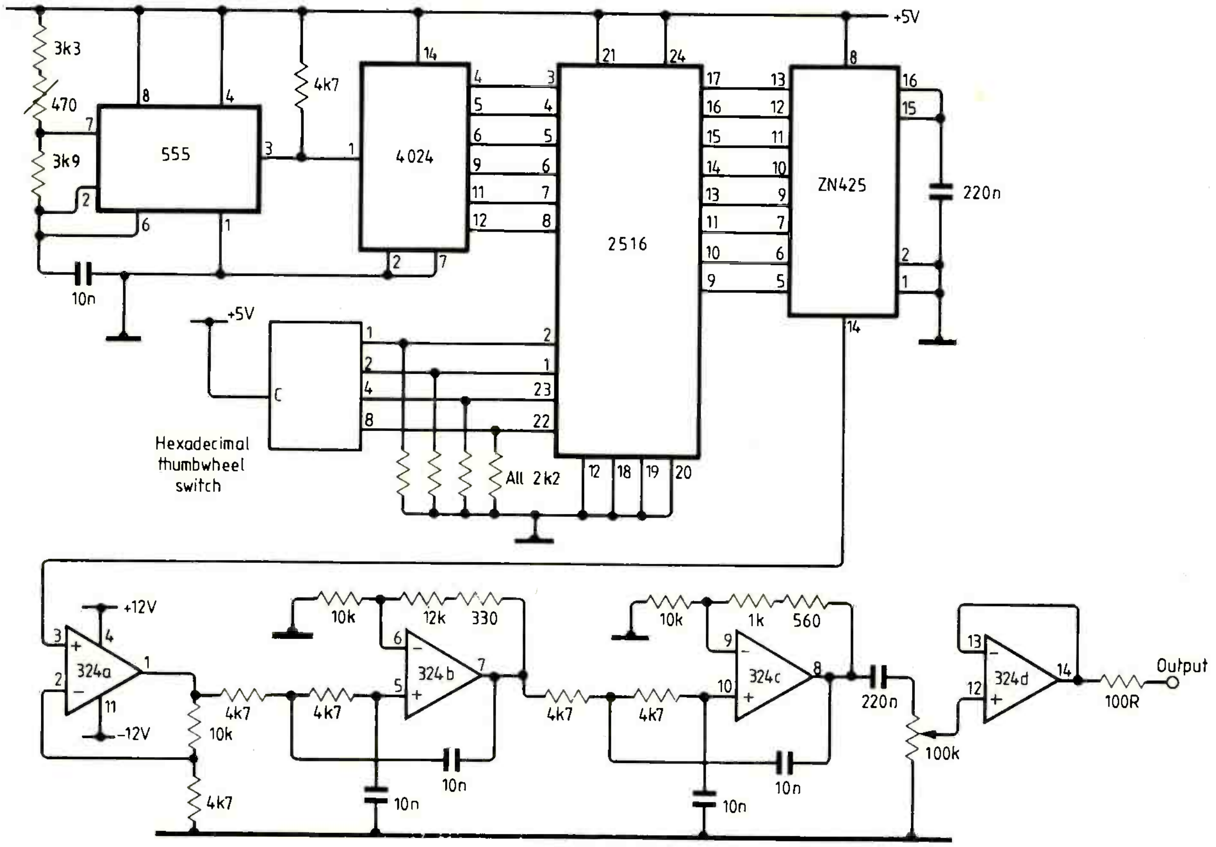


Fig.2. Circuit diagram of the baseband test signal generator.

figuration is better than 0.5% and the third harmonic generated is less than 0.3%. These values compared very favourably with laboratory signal generators which employ oscillators. Also, high frequency stability is assured, provided that a crystal oscillator is used as the clock generator.

Figure 3 shows a small selection of test signals that have been successfully generated using this technique, indicating both their time-domain and frequency-domain representations. The waveform of Fig.3(b) consists of the sum of two audio tones, 800Hz and 1200Hz, and is used as a test signal for assessing the non-linearity of baseband speech-signal processing systems. Any non-linearity in such systems leads to the generation of spurious frequency components in the output signal which take the form of harmonics and intermodulation products related to the input signal tones. This technique of assessing non-linearity is known as 'two-tone' testing and is well established in the testing of r.t. circuits.

The next waveform in the sequence, Fig.3(c), is a more complex audio test signal consisting of four distinct frequency components which are odd and prime number multiples of a 200Hz fundamental which is itself excluded.

$$f(t)=\sum_{\substack{i \\ i\neq 1 \\ i\neq \text{even} \\ i=\text{prime}}}^{11} \sin(\omega i t+\phi i)$$

where i can take the values 3,5,7 and 11.

The amplitudes of the sinusoidal components are all equal; however, their phase values ($\phi 1$) are chosen to ensure a composite waveform with a controlled peak-to-r.m.s. value. The ratio of peak to r.m.s., defined here as the dynamic range of the test signal, should be as small as possible, since a smaller dynamic range will minimize the effect of quantization noise introduced by the d-to-a process. The problem of how to adjust the phase angles of a periodic signal with a given power spectrum to minimize the 'peak-to-trough' ratio of the resultant signal envelope is dealt with in detail in Ref.2.

This particular test signal, covering a range of frequencies from 600Hz to 2200Hz, has proved very useful in assessing the performance of a quadrature-based, narrow-band, angle-modulated system[1] which is under investigation as a possible multiplexer for speech and f.f.s.k.-modulated data in mobile radio.

A test signal composed of prime sinusoids is well suited to the rapid measurement of frequency response when used in conjunction with a microcomputer-based measuring system using a discrete Fourier transform to derive a spectral information from the output of a test system[3]. Any non-linearities in a system being tested in this way will not corrupt the frequency response estimates at the specific test frequencies. This is because the input signal consists of a sum of sinusoidal components which, as already described, are odd and prime number multiples of a reference fundamental frequency. Consequently, any spurious distortion products generated will fall at frequencies other than those contained in the test signal.

The final test signal shown in Fig.3(d) has been designed to have a specific amplitude spectrum; a sinc(x) distribution from zero to 1.6kHz, with a peak value occurring at 800Hz. As indicated by the spectrum analyser display of Fig.3(d), the signal consists of a fundamental at 200Hz and harmonics up to and including the seventh. Spectral zeros of the distribution are chosen to occur at d.c. and the eighth harmonic.

The amplitudes of each harmonic component are weighted according to the expression

$$a_n=K\frac{\sin(x)}{x}$$

where K=An amplitude scaling component
$x=n(\tau/T\text{-}1)$ for n=r1;2;3;4;5;6;7
T=waveform period (in this case 5ms)
$\tau=T/4$

Phases of the individual components have been selected to yield a dynamic range of less than 10dB. This waveform was designed to investigate the likely levels of distortion and crosstalk that would be produced by synchronous detection of an orthogonal multiplexing strategy based on narrow-band angle modulation after successive stages of frequency multiplication[4]. The amplitude spectrum of the baseband signal, recovered after multiplication by a coherent local carrier, is compared to the original amplitude spectrum to assess the amount of spectral distortion introduced.

OBTAINING THE TEST-SIGNAL DATA

The success of the stored-waveform concept for generating complex test signals depends to large extent on the p.c.m. data frame that is stored in the eprom as the waveform signature to be reproduced by the d-to-a converter. Clearly, this depends on the ability to obtain accurate sample values at equally spaced intervals over the desired time period for each waveform. Once these instantaneous values have been obtained, it is a relatively simple matter to optimize the steps in sample values over the amplitude range of the frame period and convert them to 8-bit codewords. Since the waveforms are periodic, they will all contain discrete frequency components and can therefore be accurately defined by a Fourier series.

Such a representation can easily be evaluated to express the instantaneous amplitude of the composite signal at all sampling instants over the period using a microcomputer running a high-level language such as Basic.

Even if a micro is not available, the instantaneous values can be calculated to significant degree of accuracy, on a point-to-point basis, with a calculator possessing the basic sin/cos trig. functions. Inevitably, this second option will demand a great deal of time to complete if the calculator is not the programmable type. The method used by the author to derive the p.c.m. data-frame waveform signatures is based on a c.a.e. package known as Astec 3[5,6] – a general-purpose analogue circuit and system package capable of performing d.c.,a.c., and transient analysis.

The reference to Astec 3 is included here for the sake of completeness. There is absolutely no need to resort to such levels of sophistication as c.a.e. software packages to obtain the data-frame signatures.

When one considers the very small hardware costs involved, and the inherent programmability, this unit is worthy of serious considerations for any lab. or test environment.

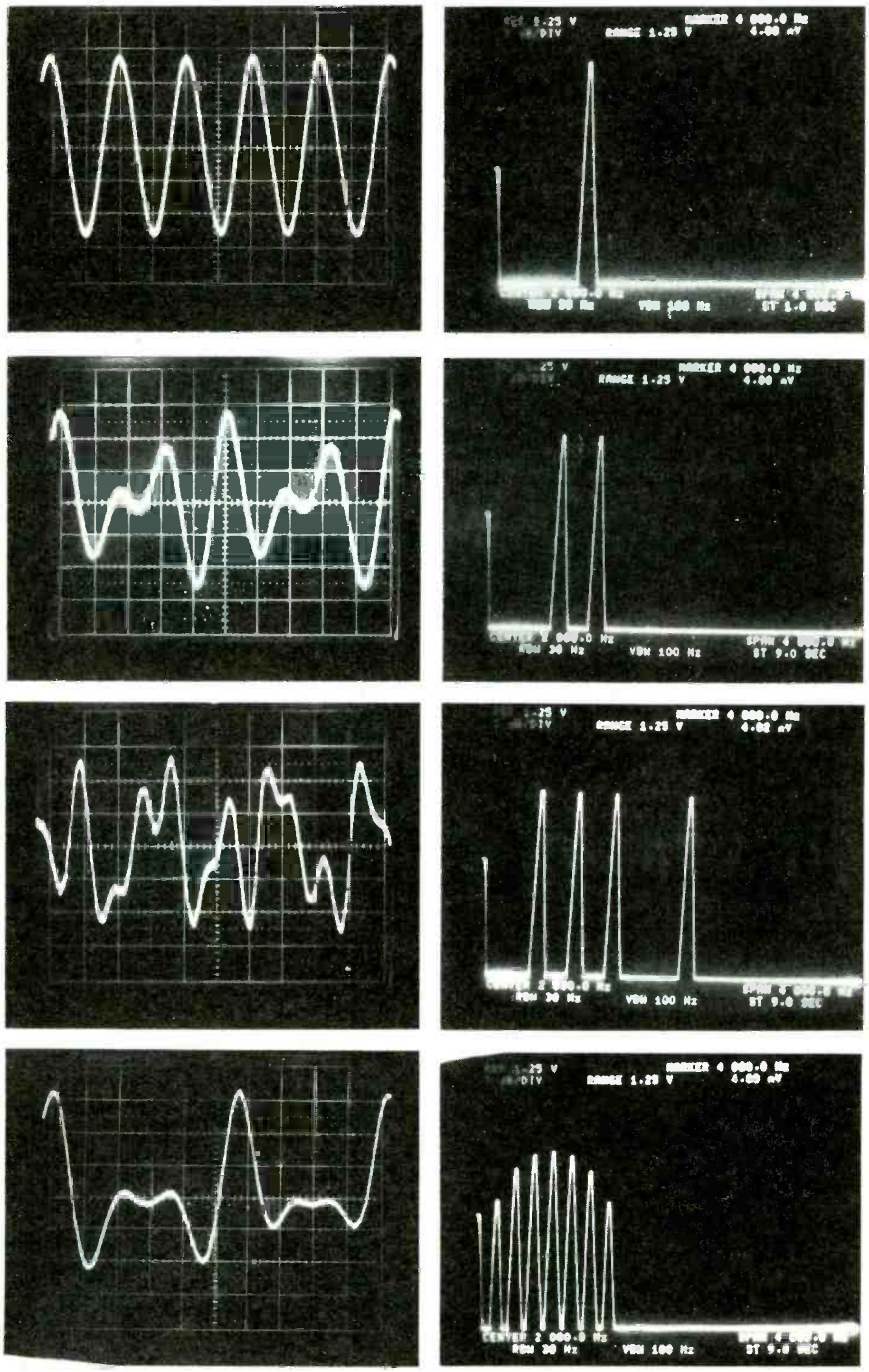


Fig.3. A selection of test signals successfully generated by the stored waveform method: 1kHz sinusoidal test tone(a); a two tone test signal(b); a prime sinusoid complex test signal(c) and a complex audio test signal with sinc(x) discrete amplitude spectrum at (d). y scale 0·5V/div., x scale 0·5 ms/div.

Fig.4. A 10ms transient simulation of the sinc(x) distribution, using Astec 3.

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M. CHARNLEY.

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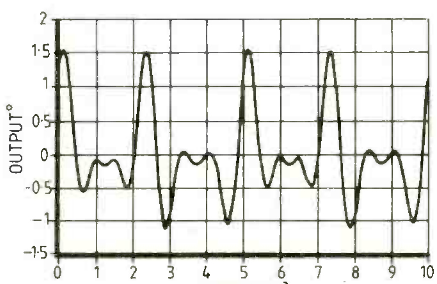


Fig.4. A 10ms transient simulation of the sinc(x) distribution, using Astec 3.

FEEDBACK

Telephone anniversary

Next year is the 75th anniversary of the first public and private automatic (dial telephone) exchanged in this country and I am engaged in research for an article to make sure the events do not go unrecorded. There are a number of uncertainties about the really early exchanges, not least, for instance, the tones provided. It was some years before ringing tone was standardized and dial tone provided. In consequence I would be most pleased to hear from anybody who has knowledge or reminiscences of the early exchanges.

Although there are a number of museums with telephone equipment, there is a limited scope for preservation under official auspices, and private switchboards have not figured in these collections. It would be interesting, therefore, if anyone would care to nominate the oldest private exchanges still in service, and it may be possible to prevent some unique museum pieces from going to scrap.

Please write to me at the address shown or leave a message on 0604-844130; every response will be followed up.

Andrew Emmerson,
71 Falcutt Way,
Northampton NN2 8PH.

Surplus equipment, please

Readers might remember the article (*E&WW* July 1985) describing electronics club work within the Youth Service. I would like to thank generally all the readers who contacted me regarding this kind of work and wish them well with any projects that have started. By the way, Professor James of the National Youth Council, and the people at the National Youth Bureau, Leicester, are very interested in the implications of this kind of work. So if any readers have suggestions or comments, let me encourage them to communicate with these bodies.

With respect to my work in Thanet, it is still progressing well and a member has just been admitted to university on an electronics degree course. He has become an avid reader of *E&WW*.

Here is a point well worth mentioning to readers who are responsible for the disposal of surplus material. As an example, an acquaintance of mine mentioned that a Kent electronics firm was disposing of a quantity of obsolete test equipment and components. I drove off to see the stores manager, but when I got there he said, "We have just got shot of that lot a week ago – on a skip. Nobody wanted it. There was a couple of signal gens., a 'scope or two, an early sweeper – and quite a few boxes of bits... We offered the lot to a broker, but as it was mainly valve equipment, he didn't want to know. The local college and school were not interested either. There was also a small lathe – with the tail stock missing. I wish we had known you were keen."

Needless to say, I was disappointed, as this kind of support is life blood to unfunded voluntary youth work. Therefore if there are any other small firms – or anyone for that matter, with older apparatus such as radio equipment, 'scopes, sweepers, meters, small machine or hand tools for disposal, then my work could make direct and valuable use of it.

K.L. Smith,
Staple,
Canterbury.

If readers wish to write to Dr Smith, I will be happy to forward their letters from this office – Ed.

Frequency allocations

Mr Price, in his letter on longwave frequency allocations (*E&WW*, October, 1986), seems to imply that only if the channels are centred on multiples of 9kHz will the intermodulation products formed in a receiver fall on a carrier frequency. This criterion is met for any equispaced group of channels.

So a group of channels could have been chosen to include 200kHz and thus preserve a unique and widely available frequency or time standard. As it was, the UK delegation to WARC 1979 was obliged to subscribe to the purely bureaucratic nicety of having all the frequencies divisible by 9.

With the advanced state of present date technology, I do not believe the argument that receiver design is simplified can be given much weight.

J.L.Eaton,
Great Bookham, Surrey.

Radio-frequency ignition hazards

In his report on my presentation at the Birmingham URSI Colloquium ('Communications Commentary', *EWW* September, page 9), I am afraid that Pat Hawker has allowed his journalistic nose for a whiff of scandal to get the better of his engineering judgement.

I made it very clear that British Standards 6656 and 6657 are the very best that can be achieved by the traditional process whereby a committee identifies all of the physical effects involved and then decides what level of multiplying factor, associated with each of these effects, can be considered to constitute a 'reasonable worst case', more extreme sets of circumstances factors, a great deal of time is spent deciding which set of circumstances constitutes a 'reasonable worst cause', more extreme sets of circumstances being then deemed to be so bizarre as to have a negligible probability of occurrence. The same decision process must occur in the drafting of all safety standards, be they for aircraft guidance systems, electric mowers or toilet seats.

The problem in the drafting of a safety standard for r.f. ignition hazards is that excessive caution can exacerbate other types of hazard. For instance, on an offshore oil production platform, the number of portable transceivers may have to be restricted: as a result, an urgent message (such as 'man overboard' or 'gas leak spotted') may be delayed, with hazardous consequences. It is therefore essential that the set of circumstances deemed to be 'reasonable worst case' should be no more extreme than is absolutely necessary, and the guidance of the Health & Safety Executive on this point was respected by all concerned, since the HSE has to carry the ultimate responsibility on such matters.

In advocating adherence to extreme worst cases, justified by an unscientific appeal to 'Murphy's Law', Pat Hawker effectively shoots himself in the foot. For one thing there would be no question of allowing mere amateurs to use such dangerous devices as radio transmitters! There would also be men with red flags walking ahead of all horseless carriages.

As in most areas of human activity, absolute safety is simply not achievable, except by banning the activity (in the present case this would mean a ban on all radio transmitters). The aim of any safety standard is therefore to reduce the probability of occurrence of an accident to a level that is neglible compared with everyday risks that are generally accepted by the public (mainly determined by the risks of disease, and of road traffic accidents).

The decision on what constitutes a reasonable worst case is implicitly a decision on probabilities. At present this is undertaken intuitively, on the basis of the collective experience of the committee members. The ongoing research that I described at the colloquium (funded by the Science and Engineering Research Council) will attempt to quantify the probabilistic factors involved, so that a more informed decision may be taken when the time to revise the standard comes again. As we had expected, our preliminary results are showing that, although the factors and configurations for each step in the British Standards appeared to represent 'reasonable worst cases', the probability of each is very low. When all the steps necessary for an accident are concatenated, the product of the probabilities is so low as to be negligible.

Our work will have to be validated carefully by a future committee but our results suggest that a substantial reduction in the stringency of the Standards will be possible without compromising safety (i.e. without bringing the probability of an accident up to a non-neglible level). No-one, least of all a radio amateur, should lose any sleep over this process. In fact, they should rest more easily, knowing that the probabilistic factors are well-quantified, rather than being based on intuition.

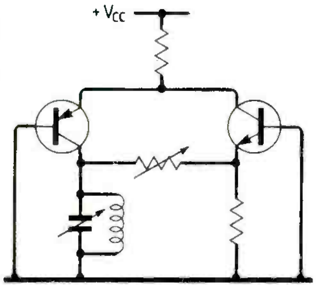
Peter S. Excell,
Senior Lecturer,
University of Bradford.

Novel Q-meter

Mr Egerton's article in the October E&WW is both timely and useful, as there seems to be a revival of interest in simple test equipment. No doubt this is partly due to the huge prices commanded by proprietary equipment, symptomatic of which is the recent claim of 'low-cost' coupled with a £7000+ price-tag!.

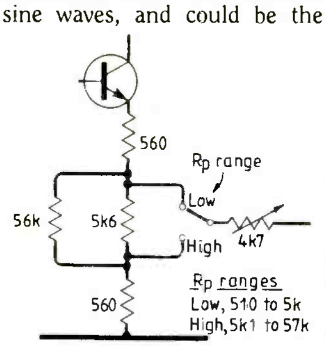
Unfortunately, there are some problems with the circuit diagrams which may cause much confusion, and lead prospective users of the new technique to believe that it doesn't work.

The first diagram is meant to illustrate the principle of the two-terminal oscillator, and as such could be permitted to take liberties with such incidentals as d.c. levels. However, there are more fundamental problems. There are two n-p-n. transistors shown, with their corresponding electrodes connected to opposite supply rails. This cannot be, and simply reversing the emitter arrow on the left-hand device to make it p-n-p still results in a single polarity-inversion around the loop, and not an oscillator. What appears necessary is to invert the right-hand device, and take the upper supply-rail as negative. This gives a long-tailed pair oscillator, described many years ago in *WW* by 'Thomas Roddam', with variable emitter feedback. However, the practical circuit is not the same at all. It is a loop containing two common-base stages, and is perhaps new. Fig.1 shows the basic circuit, with the two followers omitted.



Because the oscillator transistors are in common base, oscillation is possible up to a frequency near f_t, but the frequency will be seriously affected by the transistor characteristics. A limit of $f_t/10$ would be prudent.

In the practical circuit, there are more problems. The 4k7 resistor should go to the +15V rail, not otherwise used, while the 2N3906 base, etc. goes to +5V. The unmarked decoupling capacitor could be 100nF ceramic. The 'Q or R_p range' potential divider values should be as shown in Fig.2: the preferred values are more convenient and make only a slight difference to the R_p range. The circuit is capable of producing quite low-distortion sine waves, and could be the basis for a low-cost signal generator. These days a 1V output is often useful.



I hope that these comments will be helpful. Mr Egerton's technique has sufficient merit to justify the clearing up of these potential difficulties.

J.M. Woodgate,
Rayleigh,
Essex.

Well into retirement, I have been experimenting with various circuits which have appeared in the popular press featuring transistorized Q meters – my modest requirement being accuracy around 5% and covering frequencies from 200kHz to 1 megaherz. Results have been inconsistent with Q values indicated by old Marconi and Boonton instruments, valve-operated.

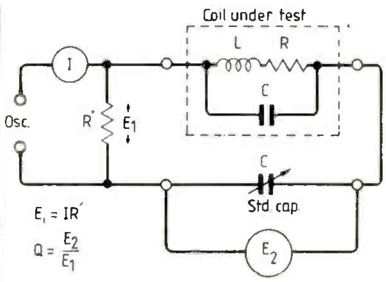
Clearly the requirement is to inject a small known value of e.m.f., occasioning minimum resistive loss, and then to measure resulting voltage appearing across coil or capacitor at resonance at the required frequency – the voltmeter load to be small compared to the dynamic resistance at resonance. I have never come across the "conventional Q meters" circuit referred to by your contributor. My ancient Marconi Q meter keeps the injection resistance down to 0.04 ohms. I believe Boonton uses 0.02 ohms. The introduction of an "ammeter" in series as shown would add some further indeterminate resistance of the order of 10 to 20 ohms perhaps (the actual value depending on the temperature reached by the filament of the thermocouple). This would more or less completely mask the effective series resistance of the circuit under test.

The basic "alternative Q meter" illustrates n-p-n (and p-n-p?) transistors in harness, and has the appeal of simplicity, but how does it work and where does one introduce the supply volts? When the writer constructed the final version, how did he verify the results and against what instrument? Surely all the hardware engulfing the coil under test would impair its potential Q and the figure arrived at from the "calibrated resistor" would show effective circuit Q.

Nevertheless, I'm delighted someone has shown an interest in what appears to be an obsolete instrument reserved for Analoguists Anonymous.

Frank Henry,
Chatham,
Kent.

Regarding "Novel Q Meters" on p.38 of the October issue of the *Wireless World*, I totally disagree with Mr McKenny-Egerton Junior's proposition that the "inelegant beast requiring much calculation and considerable thought on the part of the operator to avoid erroneous measurements is no longer in vogue". Additionally, the illustration of the "inelegant



beast" described under "Conventional Q meters" on p.39 bears no resemblance to Q meters as used in industry and research over the last 50 years.

The attached schematic shows the standard layout of a practical Q meter, and it will be seen that the ammeter actually measures the current through the feed resistors and thus establishes the input voltage. The valve voltmeter measures the e.m.f. across the capacitor and Q is the ratio of the two voltages – a very complicated, nerve-shattering experience to measure and calculate! The resistance was originally 0.04 ohm, and the input current 0.25 amp; the valve voltmeter had a full scale reading of 5 volts (Q = 500). On the Q = 250 range, the current was increased to 0.5 amp.

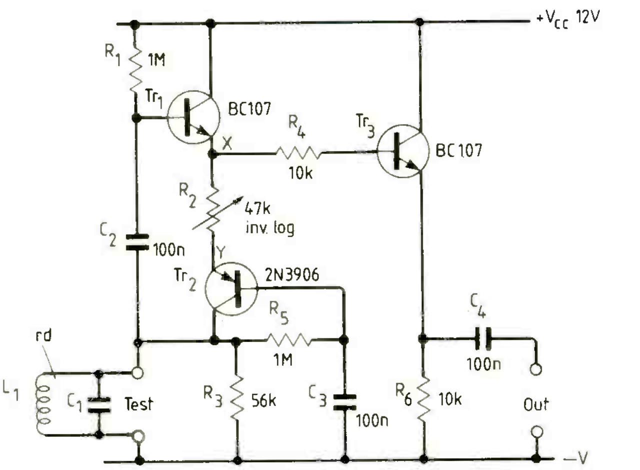
The instrument was designed by Les Woods of the Philco Corporation (USA) in the early 1930s, manufactured by the Boonton Company (USA) and produced in the UK by Ekco Instruments (who became Marconi-Ekco, and much later, Marconi Instruments – their TF 1245 Q-meter is a direct descendant in basic concept from Les Woods' original design.)

I would be very interested to know the date and name of the manufacturer of the Q Meter which Mr McKenny-Egerton Junior illustrated under the title "Conventional Q meters".

Stanley Kelly,
Broadstairs,
Kent.

A simpler circuit which covers a wider range of dynamic resistance is shown here. Like Mr Egerton's, this is essentially a calibrated negative resistance in the form of a complementary emitter-coupled oscillator. Emitter-follower Tr_1 drives common-base amplifier Tr_2, whose load contains the LC

FEEDBACK



circuit under test. When R_2 is set at the critical point its scale is read off in the dynamic resistance (r_d) of the LC circuit.

If Tr_1 has a voltage gain of 1, and Tr_2 a current gain of 1, the circuit oscillates when R_2 is equal to or less than the collector load of Tr_2. In practice, the gains are less than 1, and the collector load is not simply the LC circuit, but this in parallel with R_1, R_3, R_5 and a couple of transistor impedances. The presence of the output buffer Tr_3 also has some effect.

Fortunately, all these uncertainties can be calibrated out. Calibration consists of substituting a physical resistor for the LC. The circuit can then be made to produce relaxation oscillations. So long as the amplification is the same at the (low) relaxation-oscillation frequency as at the LC frequency the value of the physical resistance is the same as the corresponding r_d and the scale of R_2 can be marked accordingly. Thus R_2 can be calibrated from a resistance box or a selection of known resistances. Strictly speaking, V_{CC} should be increased to compensate for the d.c. drop in the physical resistor but in practice it is not worth the trouble.

For R_2, use a carbon-track potentiometer with an earthed metal case. It is important to avoid stray capacitance from X to Y and from X to earth: both make the circuit read high. (R_4 buffers the effect of the input capacitance of Tr_3.)

Audio transistors can be used, since modern planar types have high cutoff frequencies. It is useful to choose types with low collector-base capacitances (C_{OB}) since these fall across the input terminals.

For many years I have kept one of these 'negative-resistance generators', made up in a two-ounce tobacco tin, handy on the work-bench. It is invaluable for quick checks on coils, capacitors, i.f. transformers, etc. Sometimes it is possible to make tests on components in-situ in other circuits, but care should then be used to avoid damagingly high amplitudes of oscillation. This entails starting with R_2 at maximum and reducing it slowly to find the critical setting. Two silicon diodes back-to-back parallel across the input will limit amplitude to about 1V peak. An inverse log. pot. is the best for R_2, since regeneration then increases with clockwise rotation and the tapering enables low values of r_d to be read off easily. The minimum achievable negative resistance depends on the maximum current through Tr_1 and Tr_2, hence on h_{fe} and V_{CC}. Values down to about 100Ω are readily obtainable.

G.W. Short,
Westminster,
London.

Relativity

Alan Watson (Feedback, October, 1986) asks for experimental evidence to contradict Einstein's second postulate. There isn't a lot, but what there is conclusively rules out the special theory of relativity (STR) as a conceivable explanation of physical phenomena.

In his original paper[1] Einstein developed the Lorentz transformations – on which STR is entirely dependent – from two equations which Einstein claimed expressed the form of the wavefront radiating from a flash of light, as seen by two observers in uniform mutual relative motion. In fact, at least one of the equations must be false, for the only way the equations could both be true would be that flashes of light could arise without any physical cause and that the flash should have zero duration in time. This is contrary to all experience – real flashes of light are of finite duration, however small, and require lamps of some kind. For a detailed discussion, see reference 2.

Another piece of observational evidence which contradicts Einstein, though perhaps not quite so conclusively, comes from spectroscopic binary stars. De Sitter[3] argued that measurements of the radial component of motion of a spectroscopic binary fit in with Kepler's laws if no allowance is made for different travelling times for light emitted at different points in the orbit of the star (and so for different velocities of the source relative to Earth). On the other hand, he claims, Kepler's laws would appear to be broken if the travelling times were actually different. De Sitter also points out that if the velocity of the light depends on the time of emission, some overlapping of the light emitted at different times is to be expected, causing an apparent splitting of spectrum lines into two or more components. This splitting, he says, is not observed.

De Sitter's points are hailed by supporters of STR as the best direct observational evidence for the theory. It is unfortunate, therefore, that neither of de Sitter's contentions is true[4]. Kepler's laws are not seen to be violated because the distances, separation of stars, and orbital velocities are such as to make it impossible to see a violation, and splitting of spectrum lines *is* observed. While the splitting does not *prove* that Einstein's second postulate is false, it cannot be held to be true until the splitting is explained in some other way. This point seems to escape the notice of the supporters of STR.

A further consideration is that by virtue of its paradoxical features, STR can be used to predict more than one outcome for more or less any experiment. At most, only one can be right. The actual outcome will contradict all the other predictions.

Prof. R.A. Waldron,
University of Ulster.

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1. A. Einstein: *Annalen der Physik 17*, 891.(1905).
2. R.A. Waldron: The Wave and Ballistic Theories of Light – a Critical Review (Muller, 1977), pp. 73-77.
3. W. de Sitter: *Physikalische Zeitschrift 14*, 429, (1913).
4. R.A. Waldron: *loc. cit.*, pp. 98-103.

In his article of June, 1986, p.41, M.H. Butterfield states that the theory of relativity has changed very little since Einstein described it, and I therefore suggest, with respect, that he refers to my paper in the *Wireless World* of October 1978, p.44, and to my earlier papers mentioned there. In these I argue that the theory is demolished by its own internal errors and contradictions. Butterfield admits that Einstein's assumption of the constancy of the velocity of light might be difficult to swallow since it goes against common sense but what scientists seem to be unable to accept is that it also contravenes the foundations of science. Science is based on experimental results which are expressed in terms of the units of measurement, which must not be duplicated if contradictions are to be avoided. By making the velocity of light constant Einstein duplicated the units because the units of time and length were already defined.

Einstein committed another grave error by using thought experiments which are a travesty of science. They cannot give new results and when they appear to do so it is because errors or additional assumptions have been made. They are used by many writers, including Butterfield in their attempts to explain or support the theory of relativity.

L. Essen,
Great Bookham, Surrey.

8085 development on the BBC Micro

Software for the simple 8085 controller board described in September

J. L. GORDON

Firmware for the prototype board was listed in the earlier article. The origin of the code is at 0200_{16}, but on reset, a JUMP instruction to 02F2 is executed. This is identified by the label START in the assembly listing.

The first task performed by the firmware on reset is to set the stack pointer to $80FF_{16}$. This location is within the ram of the p.i.a. In the present version of the code, the stack is situated in the p.i.a. ram and is therefore be restricted to 128 bytes. If the stack should attempt to grow beyond this limit, the microprocessor controller will crash. But the advantage of placing the stack here is that the full 1K of main memory is available to the user.

Next the firmware sets up the data direction register of port B for communication on the lower four bits. Bit 0 represents data in, bit 1 data out, bit 2 input handshake and bit 3 output handshake. In addition, the output handshake line is forced high. This prevents the sending machine from allowing a data transfer before the controller is ready.

Finally the main loop of the program is entered. This consists of two simple calls:

- receive four bytes from sender
- interpret command and do job.

This loop is executed continuously provided that command is returned to the control firmware. The four byte block of data used in the firmware is made up as follows: byte 1 is the control byte specifying the command; bytes 2 and 3 are low and high address bytes; and byte 4 is the data byte.

In the control byte, value 1 means 'accept data to address', value 2 means 'send data from address' and value 5 'execute program at address'. Routines exist within the firmware to perform these three functions. To allow asynchronous operation, handshaking on the data transfer is done bit by bit. From the controller's point of view, sending a bit involves the following steps:

- look at input handshake line
- wait for it to become high
- put bit to send on data out line
- clear handshake out line
- wait for handshake in to go low
- set handshake out line.

Receiving a bit is accomplished as follows:

- wait a set time for handshake input to go low
- if low then continue, else fail
- read data bit on data in line
- make handshake out line low
- wait for handshake in line to go high
- set handshake out line high.

When the controller is connected to another machine (for example, a BBC microcomputer running the communication software), the cables must be crossed as follows: data in to data out, data out to data in, handshake in to handshake out, handshake out to handshake in. This arrangement has worked successfully in several different machines with different microprocessors running at various clock speeds.

With this simple communication technique, data transfer is allowed only in one direction at a time. A drawback is that if both devices decide to send at the same time, both machines will lock up. The programmer should therefore try to stop this condition occurring. More complex communication routines may be developed when the board is functional and, when they have been proved error-free, installed in eprom.

SOFTWARE

In the communication program is machine-code which includes the primitive routines also provided in the 8085 controller firmware. These routines differ in the assembly languages that they are written in. The BBC version works with port B of a 6522 v.i.a. The program offers options to send, receive and run.

Data sent to the controller is verified and any difference between the byte sent and the byte received is reported as a failure. Since four bytes must be sent for each one put into the controller's memory, communication is fairly slow, although quite reliable. But this is not really a problem because the controller has only 1K of user ram. With the 8085 controller, 1K-byte may be sent in 70 seconds and received in 36 seconds.

Sending involves the transfer of nine bytes: four send, four request-verify and one for the verified byte. Receiving involves five bytes, four send and one receive. With a Basic program, the transfer rate is about 140 bytes per second. With asynchronous operation, the speed of transfer depends on the slowest machine.

An 80-track disc containing software for this project can be supplied by the author at a cost of £5. Requests should be sent to him at 19 Windlebrook Crescent, Windle, St Helens, Merseyside WA10 6DY.

The BBC microcomputer may interrupt the communication task at any time to attend to normal housekeeping. The bit-transfer routines of the communication program therefore disable interrupts whilst data is transmitted or received.

The communication routine is directly compatible with the firmware in the controller and the two should not get out-of-step. If, however, the user selects the option to run the program installed in the controller, then the controller must either be reset or its program should cause a jump to 0000 on completion in order to continue with the communication process.

The function of the loader is to take a named target file from disc, from the T (for Target) directory, and send it to the controller with the correct address for each data byte. Address and data are part of the target file.

The user will be asked to supply a run address for the file. If no address is entered, the first address in the file will be taken as the run address.

USING THE ASSEMBLER

The 8085 assembler is the final program in the software package. It loads a file called ASMCODE, a data file containing op-codes. The file consists of three columns: op-code, octal value and number of bytes per op-code. Data for the file may be entered as records consisting of three entries (or fields) per record, two string and one numeric field.

Note that the last four entries in the file are not real op-codes but pseudo op-codes. These are found in most assemblers in one form or another. In building a file, it is important to ensure that these records appear right at the end, immediately before the final, dummy record END.

The letter X in the octal value field indicates that the assembler must add to the op-code value according to the operand used.

MAX, a constant in the assembler, set the maximum number of lines which may be entered. Lines are stored as single string entries in the array text$(). This string array is treated as a link list and so never has to be sorted or shuffled if lines are added or deleted. Line numbers are generated when the file is listed but are not relevant to the file unless the commands Kill or Merge are used.

Assembly is a two-pass operation. On the first pass the assembler attempts to assign values to all labels. No errors are reported unless a value cannot be assigned because of an operand field error. The second pass produces target code and reports any errors.

Full-wave rectifier uses one diode

It should be possible to produce full-wave rectification using only a single diode – if only by accident.

FRANK A. REGIER

The student of Fourier series is often surprised to find that a full-rectified sine wave differs from a half-rectified wave of twice the amplitude only in the presence of absence or a fundamental-frequency sine wave. The panel shows the half-wave-rectifier has the form of e_1, and the full-wave rectified wave has the form of e_3, from which it is clear that e_3 can be formed from e_1 by the addition of the sine wave $e_2 = -E_0 \sin \omega t$. These waves are shown in Fig.1, and it can be seen either from the Fourier series or from direct inspection of the waveforms that $e_3 = e_1 + e_2$. This relation suggests that it should be possible to build a full-wave rectifier utilizing this principle of voltage addition and having only one diode.

A naive application of this idea results in the circuit of Fig.2. This circuit will clearly not operate as intended because the two transformer voltages are simply added and their sum rectified, resulting in the voltage e_5 of Fig.3. Since $e_5 = e_4$ and e_2 must be as shown in Fig.1, e_4 must have the form shown in Fig.3.

The difficulty with the circuit of Fig.2 is that the voltage e_4, which was intended to have the form e_1, is allowed to go negative. The obvious cure is a clamping diode, resulting in the circuit Fig.4. This circuit does indeed produce the desired output e_3 but does not of course qualify as a full-wave rectifier with only one diode.

Fig.4 can be simplified and put in more familiar form if it is recognized that the potential at the bottom of the lower winding is the same as that at the centre of the upper winding. The lower winding can accordingly be replaced by a centre tap on the upper winding. The result is the circuit of Fig.5, which is of course simply a conventional full-wave rectifier.

Although we have not yet succeeded in forming a one-diode full-wave rectifier based on the addition of voltages e_1 and e_2, it doesn't follow that it can't be done. If the half-wave rectifier part of Fig.2 is given a resistive load and no current is drawn from the combined circuit, the voltage e_4 will not go negative, and the output will have the desired form e_3.

More generally, either circuit of Fig.6 will produce the output voltage e_6 shown in Fig.7, and this approaches the desired form e_3 if R_L is much greater than R_1.

The circuit of Fig.6(b) is occasionally produced by accident when one diode in a conventional full-wave rectifier fails.

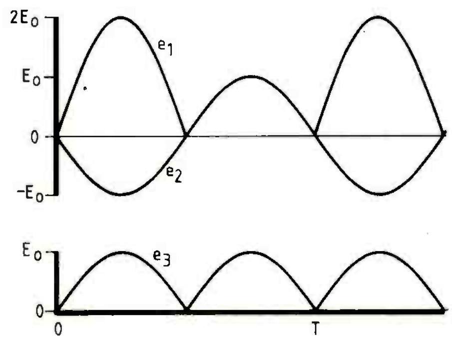

Fig.1. Full-wave rectified wave e_3 is formed by the addition of half-wave rectified wave e_1 and sine wave e_2.

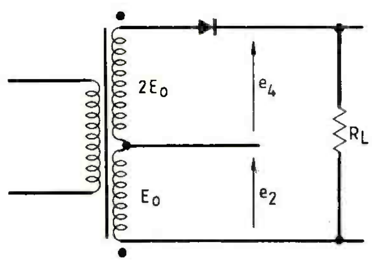

Fig.2. Unsuccessful attempt at a full-wave rectifier with one diode. E_0 and $2E_0$ are the peak voltages of the two windings.

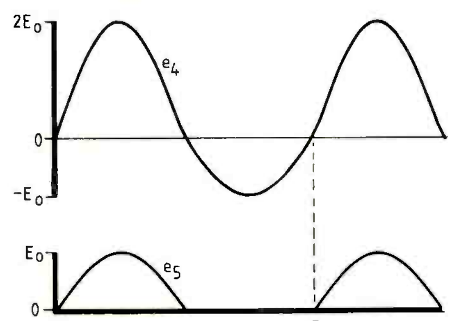

Fig.3. Voltages e_4 and e_5 occuring in the circuit of Fig.2; e_2 is shown in Fig.1.

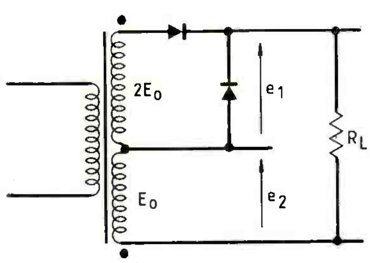

Fig.4. The circuit of Fig.2 modified by the addition of a clamping diode produce the desired full-wave rectified output e_3.

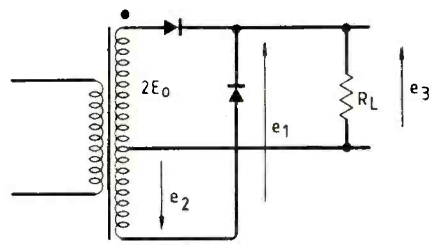

Fig.5. Conventional full-wave rectifier, equivalent to and desired from the circuit of Fig.4.

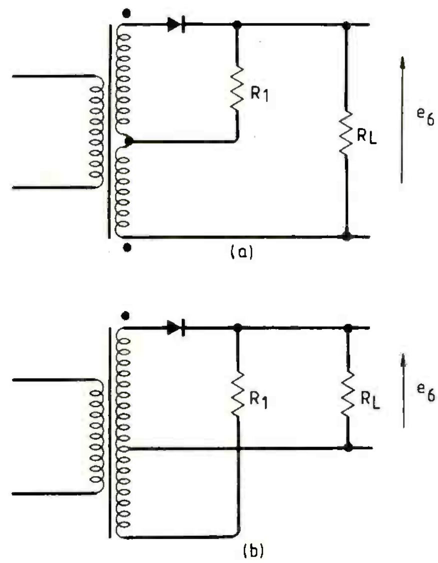

Fig.6. Equivalent one-diode rectifier circuits using two (a) and one (b) transformer secondary windings and producing the output voltage waveform e_6 shown in Fig.7.

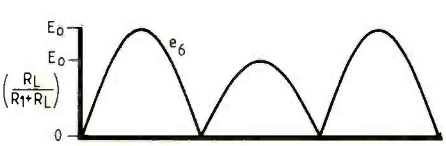

Fig.7. The output voltage e_6 produced by the circuit of Fig.6 approaches the desired form e_3 if R_L is much greater than R_1.

$$e_1 = \frac{2E_0}{\pi}\left[1 + \frac{\pi}{2}\sin\omega t - \frac{2}{3}\cos 2\omega t - \frac{2}{15}\cos 4\omega t - \frac{2}{35}\cos 6\omega t \ldots\right]$$

$$e_3 = \frac{2E_0}{\pi}\left[1 - \frac{2}{3}\cos 2\omega t - \frac{2}{15}\cos 4\omega t - \frac{2}{35}\cos 6\omega t \ldots\right]$$

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Satellites in Australian broadcasting

Australia has just the right kind a geography and demography to benefit from satellite transmissions. It has a small population of about 15 million (less than a third of that of the UK) spread over a huge land mass of nearly three million square miles (more than thirty times the area of the UK). Obtaining electromagnetic coverage, for whatever purpose, is therefore difficult and expensive by terrestrial methods. The Australian government knew from the start that they could achieve complete coverage of the entire continent with a single transmitter on a geostationary satellite, and in 1979 they went ahead to establish a national, domestic satellite system.

Called AUSSAT, this comprehensive Ku-band system is owned and operated by Aussat Pty Ltd. The government holds 75% of the company's shares and Telecom Australia the remainder. Its purpose is to provide services for telecommunications, broadcasting, air traffic control, banking, mining, the press, private network customers, education, the police and other public organizations.

The first phase is now almost complete, with two Hughes HS376 satellites in operation and a third due to be launched soon. The first satellite was put up in August 1985 by NASA's 'Discovery' space shuttle and is in geostationary orbit at 160°E. The second was launched in November 1985 by space shuttle 'Atlantis' and has an orbital slot at 156°E. Satellite No 3, completing the first phase, will be positioned at 164°E after launching by the European Space Agency's Ariane rocket in early 1987.

Each spacecraft, with a cylindrical structure 2.2m in diameter and 6.6m high, carries 15 transponders. Four of these have an r.f. output power of 30W while the remaining eleven give 12W. The high-power ones are used for broadcasting applications. Spare transponders are carried. Uplinks to the transponders operate in the 14-14.5 GHz band, while downlink transmissions are in the 12.25-12.75 GHz band.

Coverage from each satellite is provided by two national beams, encompassing the entire continent, and four spot beams for particular areas.

Quick off the mark to utilize the AUSSAT system was the Australian Broadcasting Corporation. They have had transponders on lease for over a year now, for two purposes in their National Broadcasting Services. One function is to distribute sound, vision and data signals to broadcasting stations in the seven states. The second has been to provide direct broadcasting from the satellites to individual homes in remote areas beyond the reach of terrestrial radio and television.

This second system is called the Homestead and Community Broadcasting Satellite Service (HACBSS). It provides each home with the ABC radio and PAL television services that are appropriate to that part of the country. So far about 2,500 homes have installed receiving equipment, made by Plessey Australia.

At the recent International Broadcasting Convention at Brighton, E.G. Warren of ABC was at pains to point out that HACBSS is not a universal d.b.s. system as specified in the WARC 1977 plan. Although it operates in the 12.5-12.75 GHz sub-band allocated to Region 3 d.b.s. it does not use the orbital slots reserved for Australian d.b.s. satellites.

The HACBSS direct broadcasts are beamed to particular areas by the appropriate spot beams, fed from four 30W transponders and one 12W transponder. Homes in New South Wales, Queensland, Victoria and Tasmania receive HACBSS signals from the south-east beam of the 160°E satellite. Homes in Western Australia, the Northern Territory and South Australia get theirs from a spot beam of the 156°E satellite, vertically polarized for W. Australia and horizontally polarized for the rest.

Mr Warren said that this scheme gives the majority of the populated areas an e.i.r.p. of at least 47 dBW, with only small areas receiving less than 44 dBW. For these radiated powers, receiving dish antennas with diameters of 1.2m to 1.8m are adequate.

The HACBSS direct broadcasts are also used to distribute signals from Sydney to the various ABC radio and television transmitters throughout the country. A national beam is employed for this as well.

For the whole continent the distribution arrangements are quite complicated but can be studied in the IBC 86 published papers. As a worst-case example, a PAL signal from a Sydney tv studio is decoded to RGB and encoded to B-MAC (see later), uplinked from Sydney to the satellite, received in, say, Adelaide, decoded to PAL, recorded onto and replayed from video tape to give the necessary time delay for that geographical zone, decoded to RGB, encoded to B-MAC, uplinked from Adelaide to satellite, received at a transmitting station in South Australia, decoded to PAL and finally broadcast to the local audience.

B-MAC was chosen as the satellite transmission format – as distinct from, say, C-MAC/packets – simply because B-MAC encoding and decoding equipment was already available from a manufacturer when the AUSSAT satellites were launched in late 1985. B-MAC uses the same principle of multiplexed analogue components for the vision signal as in the original MAC system proposed by the IBA and later adopted by the EBU in the European C-MAC/packets standard. But the rest of the signal is different because B-MAC was originally designed for a satellite scrambled pay-tv system. Viewers' decoders can be individually addressed, though ABC is only utilizing this facility for its own signal distribution system.

Six digital audio channels using Dolby adaptive delta modulation are provided by four-level data added to the signal during the vision horizontal blanking interval. Two of these are used as stereo sound channels for television, the others for two mono and one stereo radio programmes. During the vertical blanking interval a data packet is transmitted. ABC use this for a form of teletext that they call Mactext.

The B-MAC sysem and equipment was developed about five years ago by the Canadian company Digital Video Systems Corporation, now a subsidiary of Scientific Atlanta. Keith Lucas, an engineer associated with the conception and development of MAC at the IBA, now works for them.

UK d.b. satellite design

Also presented at IBC 86 at Brighton was a small-scale model of a satellite that could be used for d.b.s. in the UK. It was shown by British Aerospace, who have offered the design to competing applicants now being considered by the IBA for the d.b.s. contracts currently available. Three new tv services and some teletext services are to be taken up.

BAe's proposed design is a version of their existing Eurostar 86 satellite already sold to INMARSAT (see diagram). The spacecraft main body, constructed in aluminium honeycomb and carbon-fibre-reinforced plastic, is about 1.6m square. When the two folded solar arrays are fully extended the total span is 15m. These two arrays turn slowly to track the sun and generate a total power of at least 1kW at the solstices. The whole craft is position-stabilized in three axes, using small momentum wheels to give gyroscopic 'stiffness'.

The repeater electronics, shown by BAe in breadboard form, is designed around six 100W travelling-wave tube r.f. wideband power amplifiers. As the Japanese experiences showed in 1984, the reliability of high-power t.w.ts in space is a critical matter. Apparently the tube cathodes are the most vulnerable items. BAe have chosen AEG tubes, in transmitters supplied by the German company ANT. In the operational satellite only three of the six t.w.t. amplifiers are in use at a time. Possible damage due to switching the tubes on and off is avoided by keeping them on 24 hours a day.

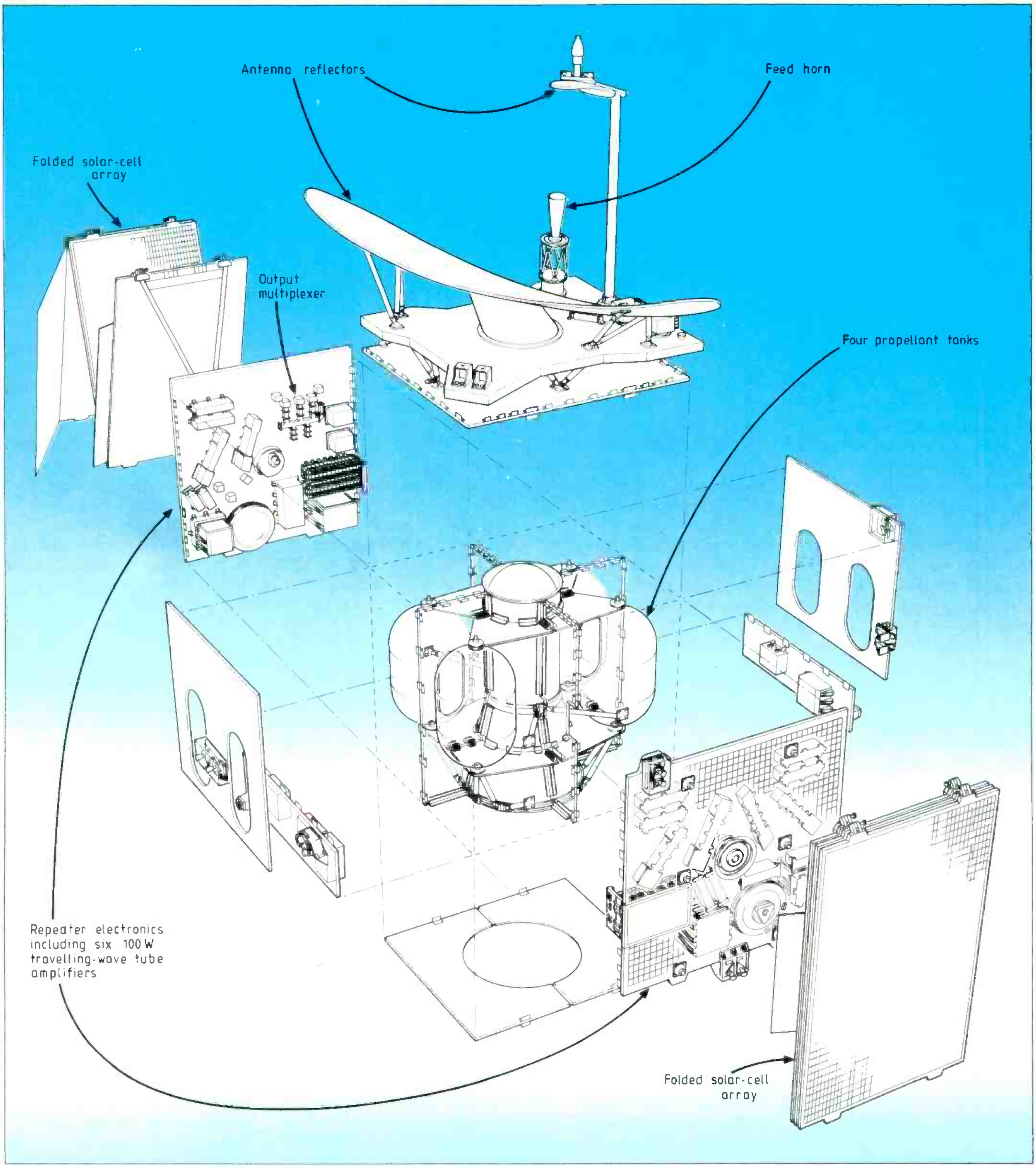
Received uplink signals go to a wideband single-conversion front end. After frequency conversion, filters establish the 27-MHz channel. Then individual channel amplifiers, with gain control, drive the t.w.t. amplifiers.

The r.f. output passes through

a multiplexer to the single feed-point of the antenna system. This uses two reflectors with surfaces shaped to give the required beam coverage. The main reflector is elliptical and measures 2.8m by 1.1m. BAe claim that this design is lighter and has lower losses than an antenna using several feed horns, a passive splitting and phasing network and a single reflector.

In the transmission beam the e.i.r.p. is expected to be 59 dBW at the outer edge of the coverage. BAe reckon that with this power the domestic receiving dish need not have a diameter greater than 45cm. In the satellite the G/T figure of merit of its receiving system is −5 dB/K.

Seven commercial groups have applied for the d.b.s. contracts. The wide range of companies within these includes, electronics manufacturers, retailers and rental firms, telecom and broadcast network operators, publishers, film companies, shipping, travel and hotel firms, banks, and existing television programme contractors.



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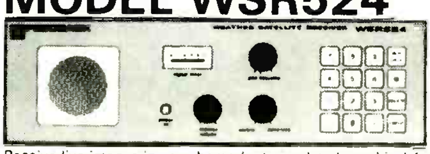

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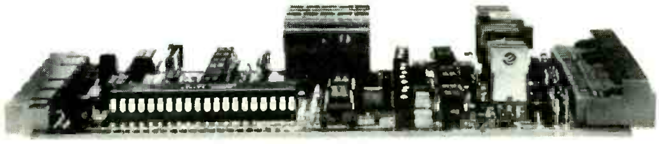

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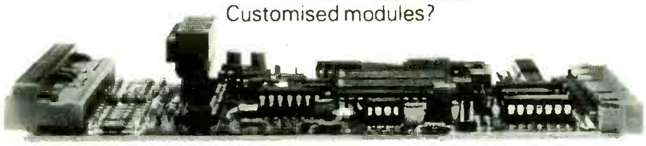

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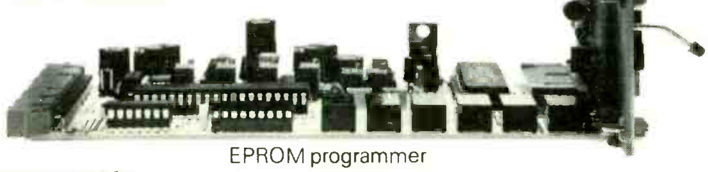

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Video frame store

This high-performance system offers many features at a reasonable cost. Circuit description begins with the analogue section.

D.E.A. CLARKE

The analogue board performs all analogue signal processing and digital-analogue-digital conversion and would be useful as the front-end of any digital video application. It requires only clock and blanking signals to operate.

Anti-aliasing filters are not incorporated in the basic unit because user requirements will vary depending on the application. It is fairly straightforward, and standard practice, to connect filters between the video source and frame store as required.

SYNC SEPARATORS

The composite video input signal (1V p-p) is terminated by R_1 and a.c. coupled by C_2 (or separate sync can be used.) The signal is then clamped to about 2.5V by the potential divider $R_{3,4}$ and diode D_1, Fig. 9. Resistor R_2 provides a time constant when switching between video sources.

Colour burst, if present, is filtered out by R_5/C_3 and the resultant signal applied to the comparator IC_{2a}. Sync slicing level is set by potentiometer P_1 with $R_{6,7}$. Positive going composite syncs appear at IC_{2a} pin 1 and are inverted at IC_3 pin 10.

Composite syncs are integrated by R_9/C_4 and field syncs extracted by IC_{2b}; the clipping level is set by the divider $R_{11,10}$. Hysteresis is provided by R_{12} which prevents double triggering on residual line-sync edges. Field syncs appear at IC_2b pin 7.

This field sync waveform has an uncertain relationship with respect to line sync and can cause vertical jitter on the display. However, this is the simplest method for handling non-standard video sources and is therefore provided as a link-selectable option (FS_1).

A jitter-free, digitally-derived field sync waveform is generated on the control board for use with the on-board test video generator and standard video sources.

VIDEO AMPLIFIER AND A.D.C.

The 1V p-p input signal from R_1 (Fig. 10) must be amplified and clamped at a precise d.c. level for feeding to the a.d.c. The signal is a.c.-coupled by C_6 and applied to the non-inverting input of the fast op-amp IC_4. The trailing edge of the line sync is differentiated by C_5, the resulting negative spike is inverted at IC_3 pin 8. This positive pulse switches TR_1 which clamps the video waveform black-level to approximately 0.8V set by the poteniometer $P_2/R_{17,18}$.

Voltage gain of IC_4 is set to about 3.6 by P_3/R_{19} and the compensation network R_{20}/C_8 selected for optimum pulse response; the 3dB bandwidth is about 8MHz. The amplified video signal now has an amplitude of 2.5V and sits 2.5V above ground, meeting the input voltage specification of the a.d.c. IC_5 (+2.5V to +5V).

Converter IC_5 is a relatively inexpensive type (around £16, 1-off) from Mullard. Previously, such devices were available only in hybrid form and cost well over £100. The i.c. has a maximum conversion rate of 22 mega-samples/s and a resolution of seven bits. It acquires the sample virtually instantaneously and therefore does not require a sample-and-hold.

Link 1 selects whether two's complement (link open) or binary codes are available at the data outputs.

The incoming clock (CK_1) is delayed and inverted by IC_3. Data from the a.d.c. is available on the positive edge and latched by IC_4, which is a 74F364 (input hold time <4ns). The a.d.c. data is guaranteed to be held for 6ns, thus ensuring correct latching on the same clock edge. Notice that the a.d.c. data is justified towards m.s.b. and bit 0 tied to 0V in order to extract the maximum dynamic range from the video ouput d.a.c.

The latch outputs are tri-stated (signal LE) when memory or host data is applied to the bus.

D.A.C. AND VIDEO OUTPUT

The d.a.c. IC_7 (Mullard PNA 7518) is a companion device to the a.d.c. It is relatively inexpensive (around £9), works at clock rates to 30MHz, and has a resolution of eight bits (256 levels). Data from the bus is internally latched on the positive edge of the clock input.

The d.a.c. negative reference input V_{refl} is clamped to about 0.7V to ensure that the video ouput black-level sits above the ground, thereby simplifying the insertion of syncs. The positive reference voltage V_{refh} is derived from R_{25} in conjuction with the d.a.c. ladder resistance. The ladder resistance is relatively stable with temperature but varies from device to device (150-300Ω).

A convenient point at which to insert blanking pulses is V_{refh}, which is clamped to V_{refl} (0.7V) by Tr_2 driven by blanking pulses derived on the control board. The maximum

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- modular construction allowing retrospective enhancement.

Link options enable straightforward upgrading to 256K rams when their cost becomes reasonable.

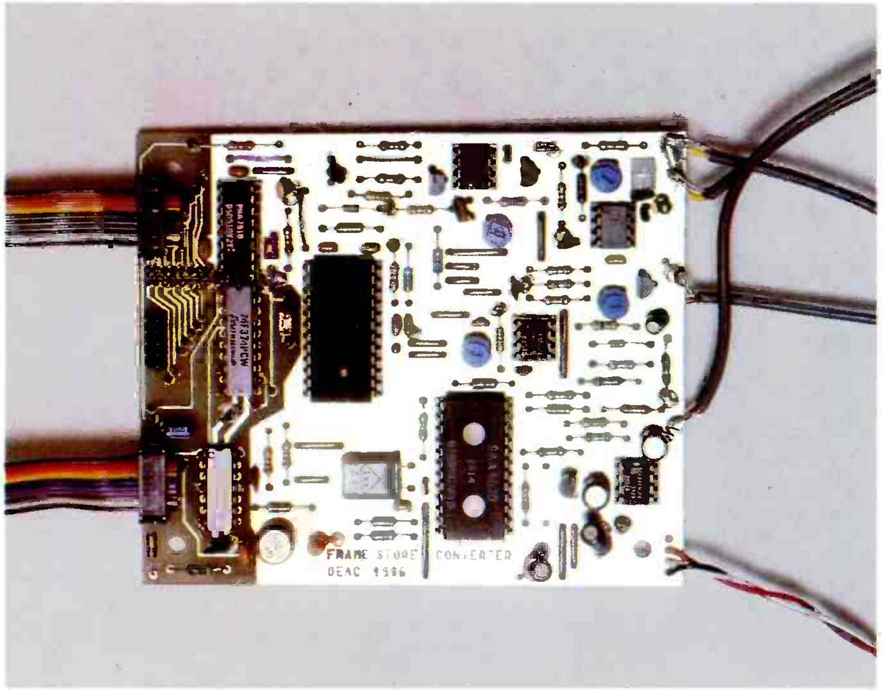
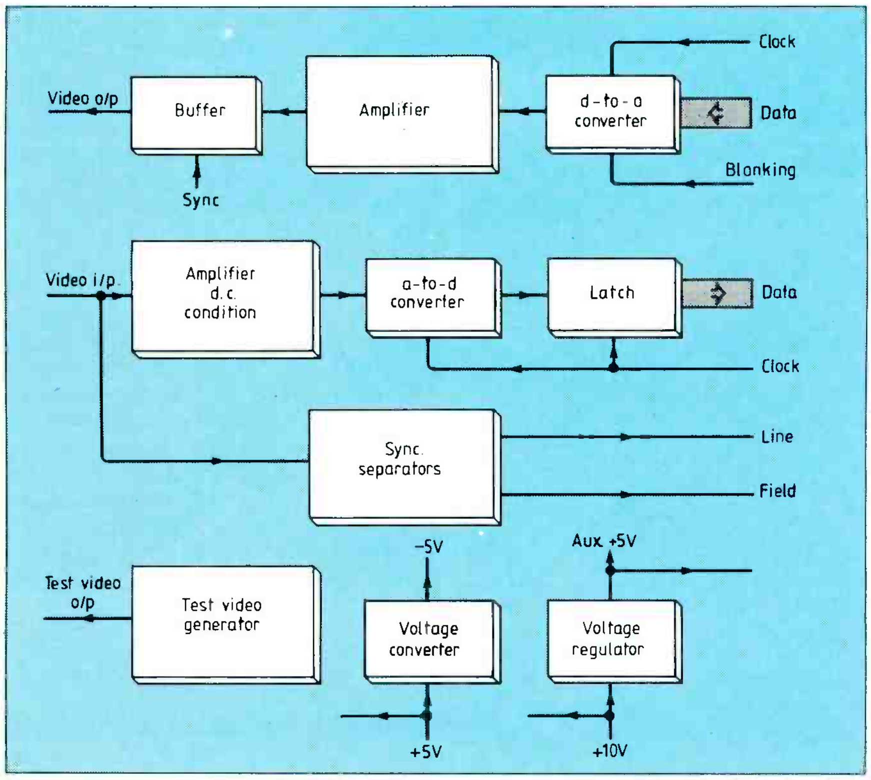
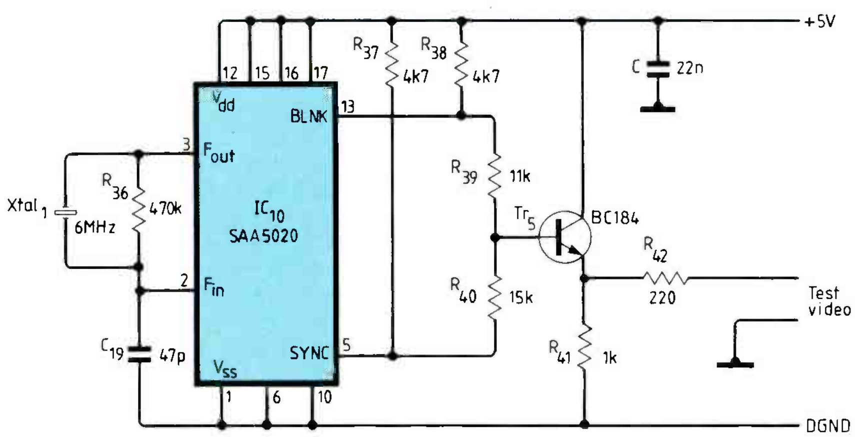


Fig.7. Prototype analogue board.





gate threshold of Tr_2 is 2.4V with respect to the source (which is at 0.7V); minimum blanking pulse amplitude therefore needs to be 3.1V, and this is ensured by the pull-up R_{24}.

Positive going video from the d.a.c. is boosted to about 1.4V p-p (and 1.2V d.c. offset) by IC_8 which is a fast op-amp; the video amplitude is set by P_4/R_{28}. Compensation network C_{16}/R_{30} has been selected for optimum pulse response; overall (3dB) bandwidth is about 8MHz.

Negative-going syncs are inserted by Tr_3. Sync amplitude is set to about 0.6V by $R_{32,33}$. Emitter follower Tr_4 buffers the output for driving a 75Ω load.

Link 3 determines whether two's complement (link open) or binary codes are selected.

TEST GENERATOR

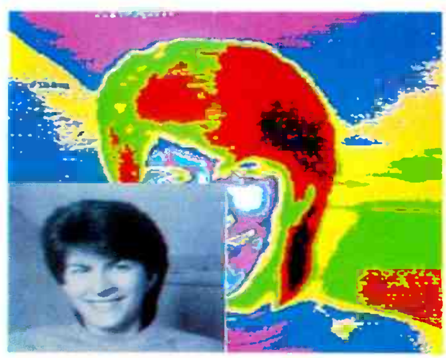
The analogue board incorporates an optional video test generator which has been found very useful for stand-alone use of the frame grabber. The unit will not function without a video source and its internal generator can be switched-in when necessary. It produces a white rectangle on a black ground.

One method of generating CCIR standard syncs is to use a teletext display i.c. The chosen for this unit is a Mullard device, type SAA5020 (teletext timing generator). An internal clock buffer (pins 2,3) turns into an oscillator with a 6MHz crystal and R_{36}/C_{19} connected.

With the control inputs connected as shown, composite syncs appear at pin 5 and a gating signal which can be used as a video signal at pin 13. Pull-ups R_{37}/R_{38} ensure full 5V swing on thse outputs. The two signals are added by R_{39}, R_{40} and buffered by an emitter follower Tr_5. Resistor R_{42} limits the output to 1V p-p into a 75Ω load.

CONTROL BOARD

The purpose of the control board is to supply a clock and blanking signal to the analogue



The frame store is an excellent tool for image manipulation. Later articles will introduce some of its possibilities.

Fig.8. Analogue board. Fast digital conversion is made possible at reasonable cost by two new Mullard devices.

Fig.12. This video test source produces a white rectangle on a black ground. The teletext timing generator i.c., SAA5020, offers a method of producing CCIR standard syncs at little cost.

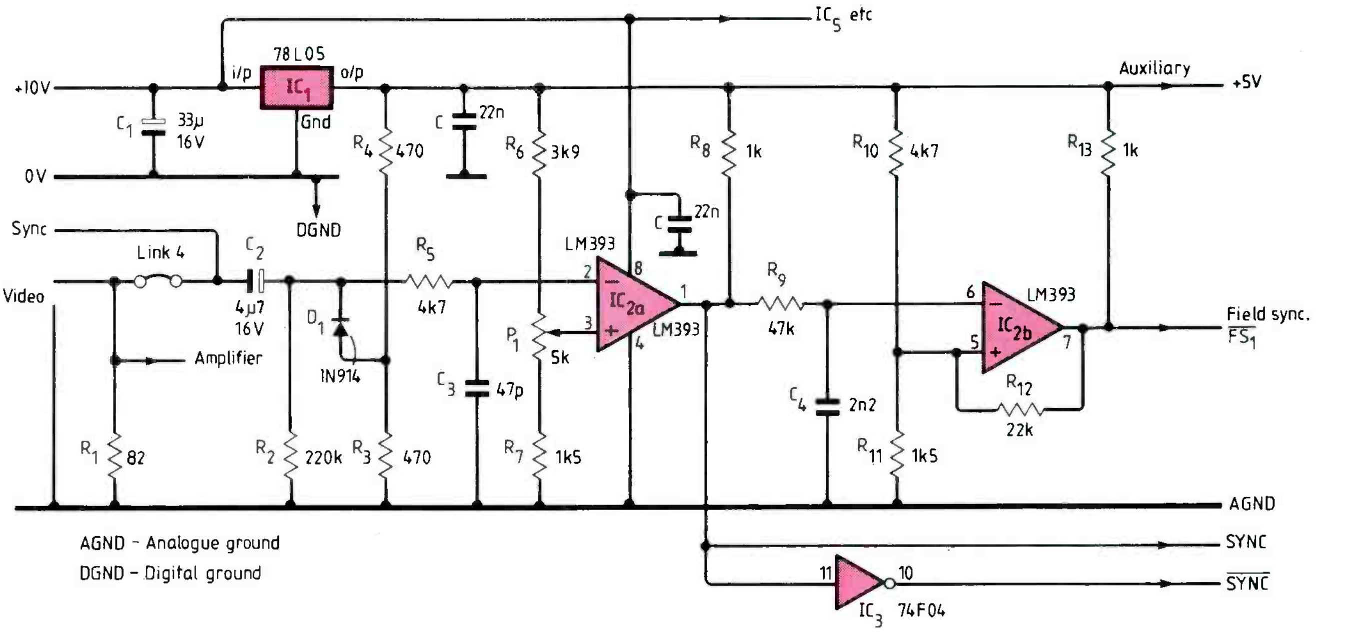


Fig.9. Sync separators. The doubly-regulated 5V supply from IC_1 also feeds the clock generator and a monostable on the control board.

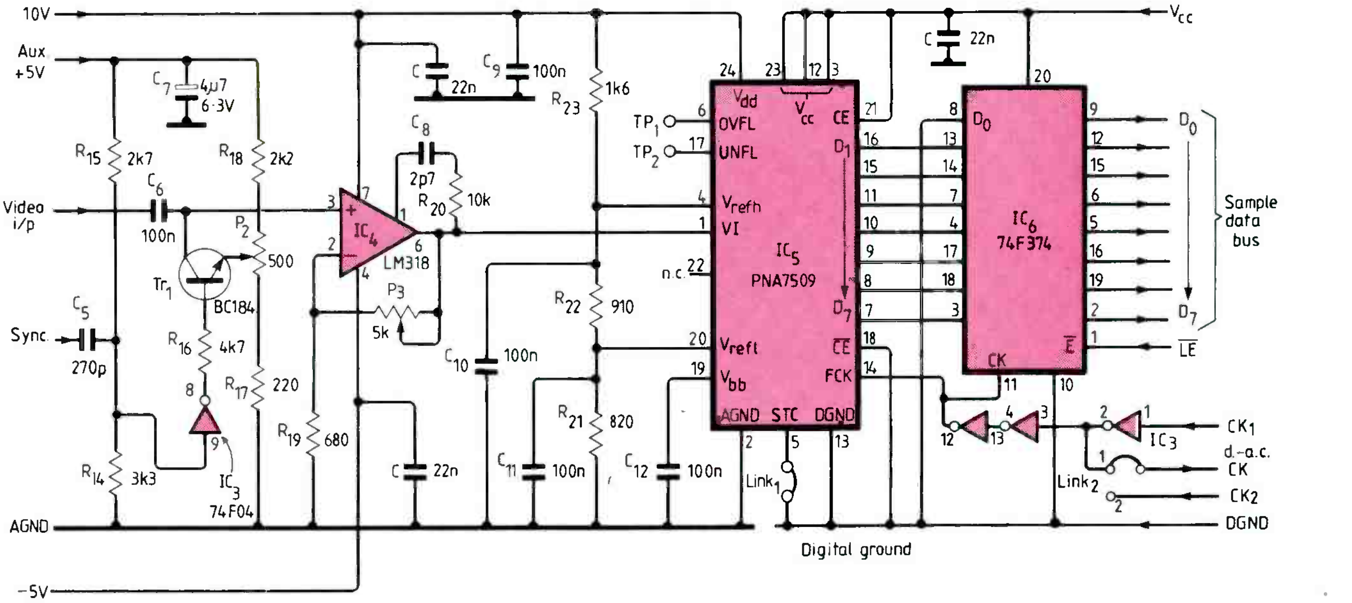


Fig.10. Signal conditioning amplifier and flash converter. Decoupling capacitors marked C are 0.22nF high-frequency types throughout; resistors are 0.25W, 5%.

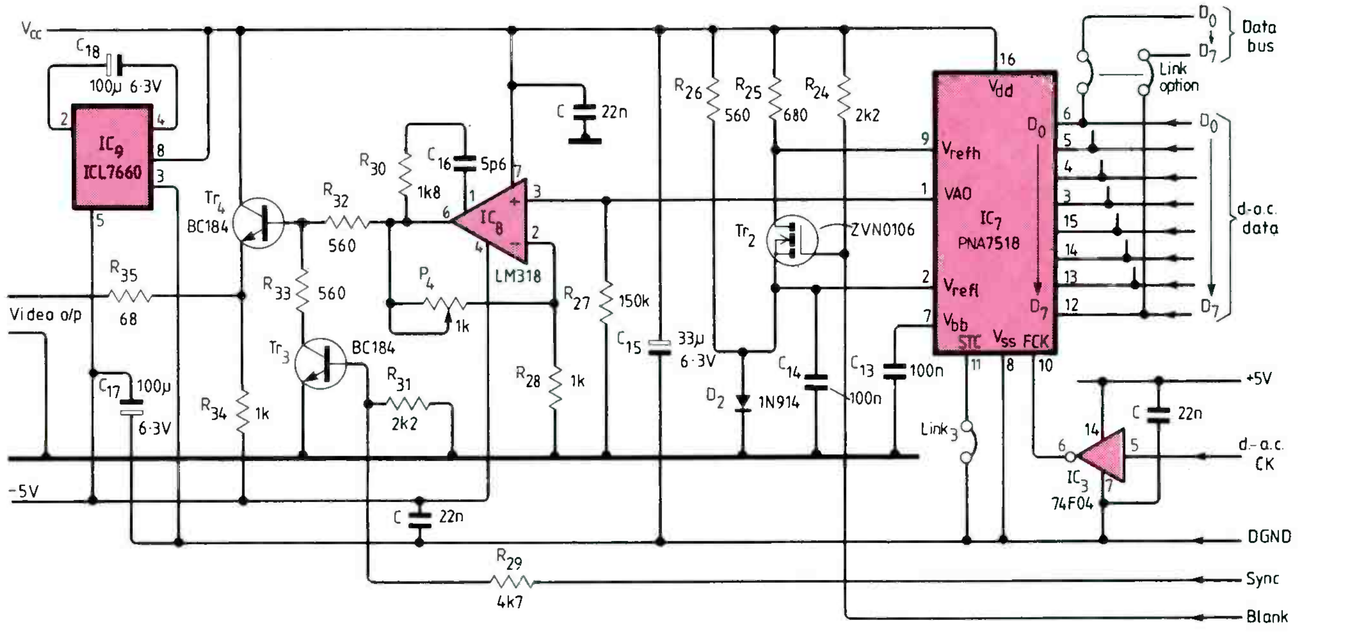


Fig.11. Video d.a.c. and buffer. Power mosfet Tr_2 has an on-resistance of about 4Ω and switches very fast.

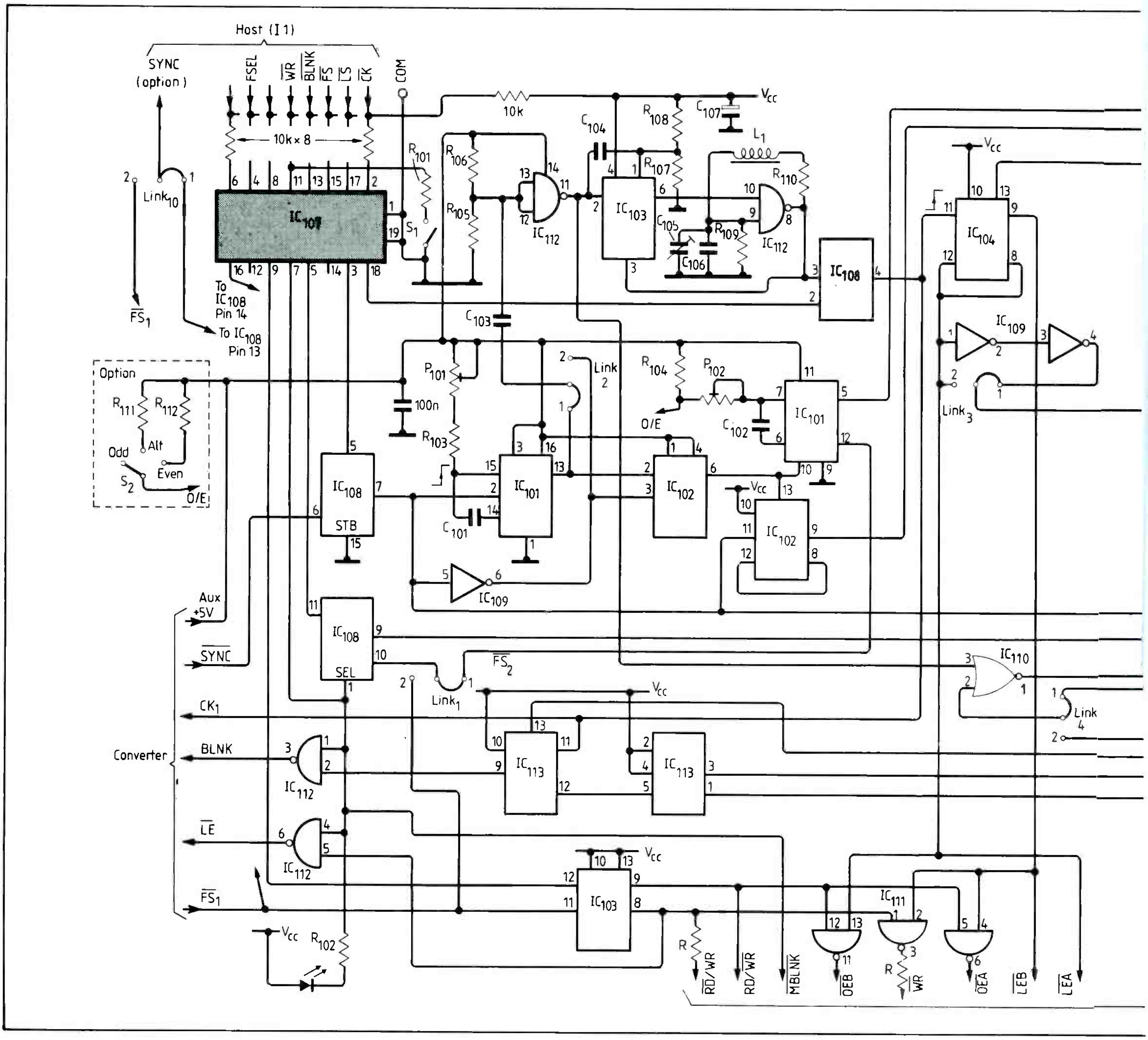
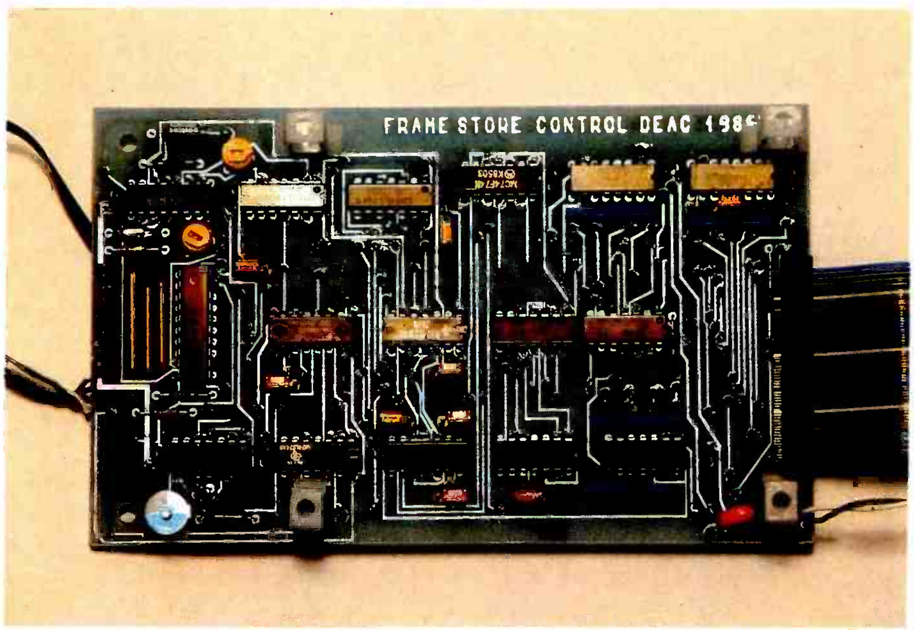


Fig.13 (above). The control board. A set of p.c.bs is in preparation (pictures, right and on page 70); details later.

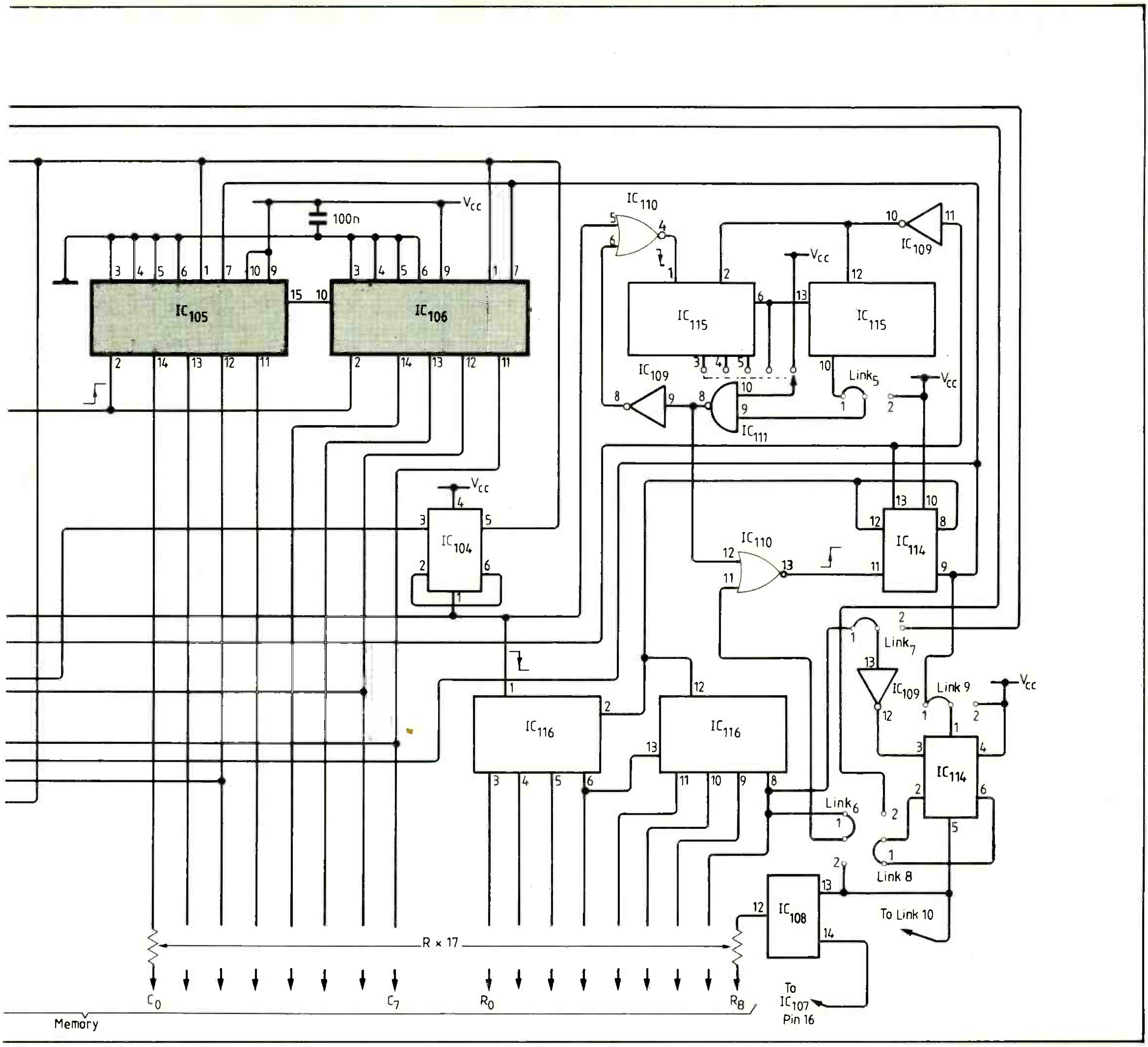


board, and address and control signals to the memory board. Interface circuitry for an external computer is also provided.

The prototype control board (right) consists of a single-height Euro-p.c.b. Component numbers have been prefixed by 1 to distinguish them from components on other boards.

It is necessary to phase-lock the master clock oscillator to the incoming video signal to prevent random horizontal displacement of the picture.

Several approaches are possible for the design of this oscillator. These range from phase locked loops to simple gated oscillators. I approached the problem from the angle of minimum complexity and maximum reliability; and after designing and evaluating different types with varying com-



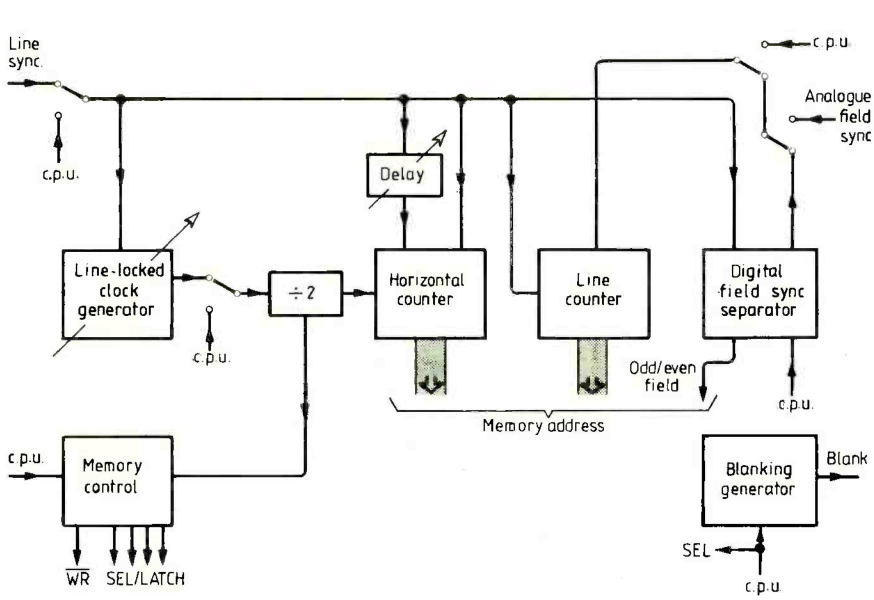


Fig.14 (left). Block diagram of the control board. The system can work with or without a host computer.

plexity, ended up with a simple gated oscillator with very good performance and stability.

The basic oscillator comprises a Schmitt-trigger nand gate IC_{112}, inductor L_1 and variable capacitor C_{105}. These form a feedback oscillator with Q controlled by the series resistor R_{110}.

To phase-lock the oscillator to the incoming video signal, it is gated off at IC_{112} (pin 10) by a narrow pulse derived from line sync. The oscillator could simply be gated directly by the line sync waveform, but the point at which oscillation is terminated would be undefined and so the mark-space ratio of the final clock cycle in the line would be random. To avoid this, the gating is synchronized to the clock itself.

to be continued

Hard disc interfacing

Falling prices and easy-to-use controllers bring hard-disc drives into the realms of add-on periperals.

J.H. ADAMS

Hard or fixed disc drives, usually Winchester types, are appearing in more and more high-performance microcomputers. As a result, the cost of drive units has fallen until now, byte for byte, they are at least ten times cheaper than floppy-disc drives.

Despite this cost fall, hard disc drives are not significantly affecting the general add-on peripheral field as they are perceived as being difficult and expensive to interface to general-purpose microcomputers in hardware and software terms.

Certainly the i.cs involved are almost as expensive as the drive unit and the drive sends out data so fast that it would overwhelm most microcomputers. But the same factor that has brought down the cost of drives – the enormous IBM PC and clone market – has led the manufacturer of the highly priced i.cs to supply ready-built drive controllers capable of working with high or low-performance systems at a reasonable price.

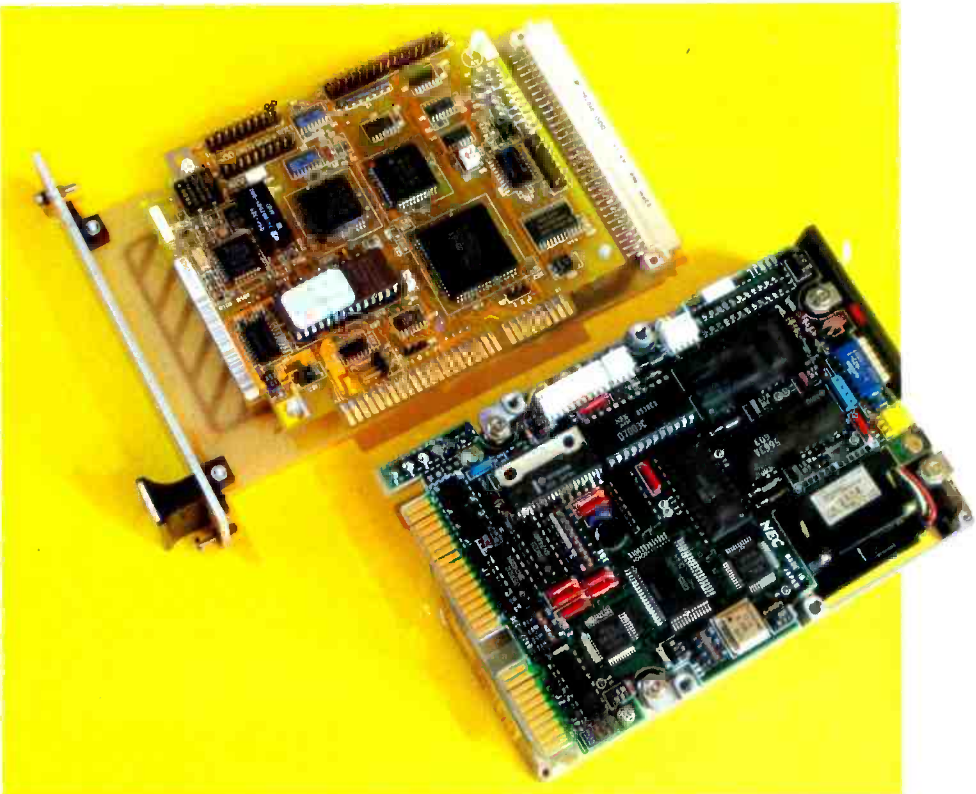
With the aid of a working example in the form of a hard-disc interface to the SC84 microcomputer, this article describes how such a ready built controller is applied.

When fitting a hard-disc drive to a computer, there are two distinct interfaces. The interface between the controller and drive unit is usually well defined. In the design example it is an ST506 type, which is similar to a floppy-disc drive interface. Open-collector active-low drive control signals are used and each alternate line on the cable is grounded. The difference is a separate 20-way signal cable carrying data to and from the drive using RS422 balanced lines. Lines conforming to RS422 can carry data at up to 10 Mbaud over 1200m and so are well suited to the 5Mbaud requirement of standard hard-disc drives.

The second interface, between the controller and host computer, should be made to suit the host's internal bus. In the design example, the controller used is intended for the IBM bus but the structure of this interface and options on the controller interface make connection to a different bus quite easy.

For the design example, the controller chosen is a Western Digital WD1002S-WX1. Through extensive use of surface-mounting technology, this half IBM-size board measures only 4.9 by 3.8in and is small enough to sit on a Eurocard. A slightly cheaper alternative using conventional mounting technology, the WD1002S-WX2, measures 8 by 3.8in.

The controller board is a complete microcomputer with its own instruction set. These



Using a proprietary controller card like the WX1 shown here greatly simplifies hard-disc interfacing and reduces costs. Note that the interface boards are not wired together.

instructions cover drive-parameter initialization, resetting, seeking specific cylinder positions, reading/writing single or multiple sectors, formatting single or multiple sectors and self-testing.

Besides features such as programmable write precompensation and reduced write current to improve reliability, the controller includes an error-correction code (e.c.c.) function and options for d.m.a. and interrupt-on-completion functions.

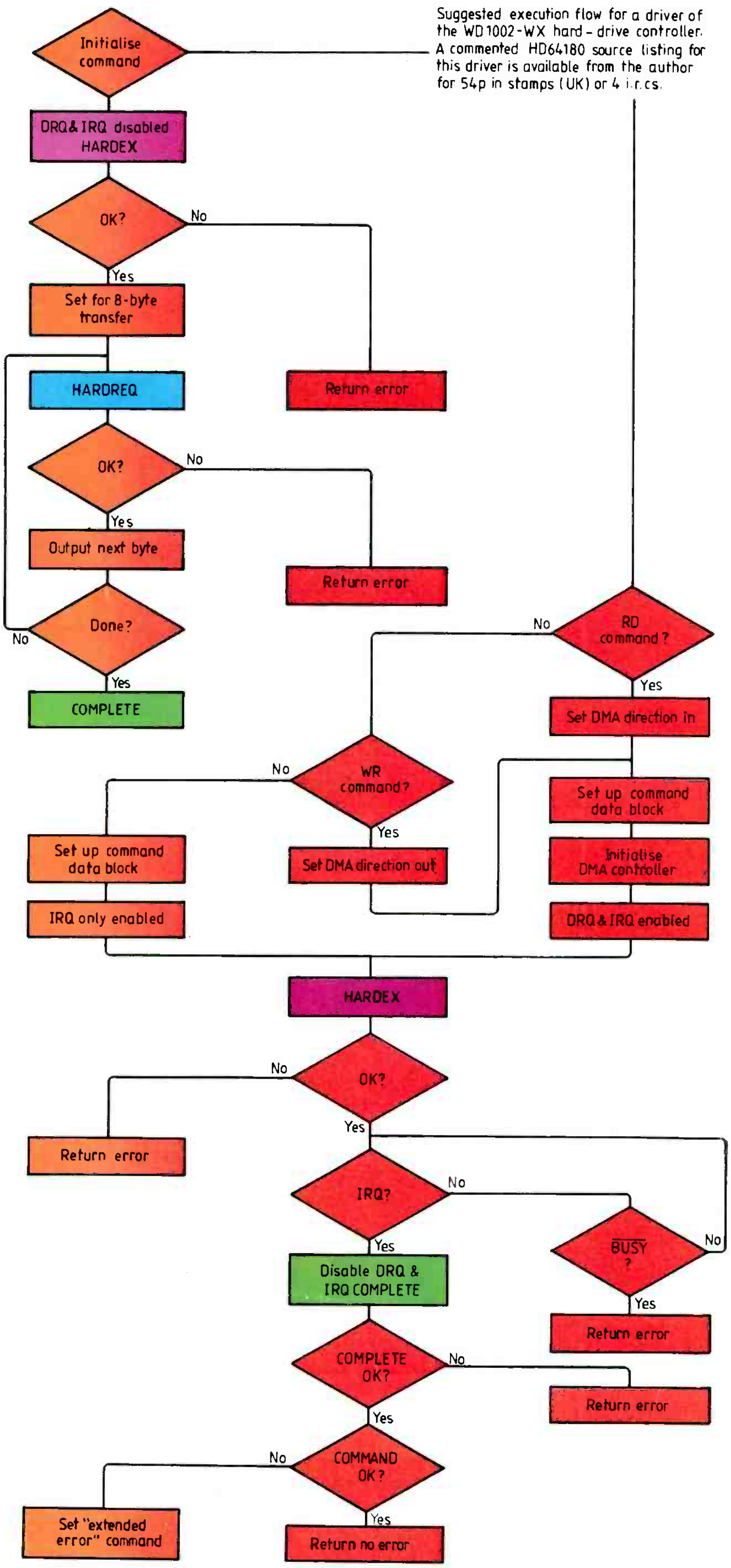
There is a fully-decoded 8K-byte eprom on the board and an eight-bit input port. These features can form part of the hard-disc system, as they do in the IBM PC, or alternatively become general system facilities.

The host interface is designed for a non-multiplexed 8-bit data and 20-bit address bus with 8088 control signals. How such signals are derived from HD64180 Z80-like signals using simple gates and inverters is shown in the circuit diagram. Most of the circuit is devoted to matching two different types of d.m.a. system.

In direct memory access, d.m.a., data is transferred from one part of a system to another as a background task to the main processing. This task is performed by a dedicated i.c. or, as with the HD64180, by a controller integrated into the processor. Transfers to be discussed here are between memory and an i/o device.

The d.m.a. controller is initialized with data including source memory address or i/o port number, destination memory address or i/o port number, transfer count and a flag for increment or decrement memory address. Once initialized, on receipt of a hardware request signal from a device, the d.m.a. controller gains control of the system bus, makes the transfer and then hands control back to the main processor. This process may repeat until access is complete or may be controlled by the d.m.a. rate requested by the device. In practice there are two distinct methods used for the transfer.

The 8237 d.m.a. controller, as fitted to the IBM-PC, has a series of request (DRQ) inputs and matching acknowledge (DACK) outputs. On receipt of a DRQ signal the controller sets the corresponding DACK line active. This line goes directly to the requesting device and is used as a cue in conjuction with IOR or IOW to gate data from or to the device, independent of chip select or addressing logic. This means that the d.m.a. controller can be sending the memory address for the other



Suggested execution flow for a driver of the WD1002-WX hard-drive controller. A commented HD64180 source listing for this driver is available from the author for 54p in stamps (UK) or 4 i.r.c.s.

end of the transfer and by activating the MEMWR or MEMRD signal data is transferred directly between the two.

During this transfer another signal, AEN, is produced which disables all devices it drives so that they (i/o devices) don't interpret the memory address and i/o control strobe as an invitation to perform a conventional i/o operation during the d.m.a. transfer. Increased speed is the advantage of this type of d.m.a. Disadvantages are the extra bus lines required and the dedication of DACK lines to individual devices, making expansion difficult.

The HD64180 d.m.a. controller responds to a d.m.a. request by performing two processor-like cycles to transfer the data. There is no intrinsic DACK signal; 'servicing' of the requesting device acts as an acknowledge. This interrupt-like service allows the system to be expanded almost indefinitely but also means that the d.m.a. process is slower. Having two – and more – d.m.a. systems complicates using peripheral devices in d.m.a. applications.

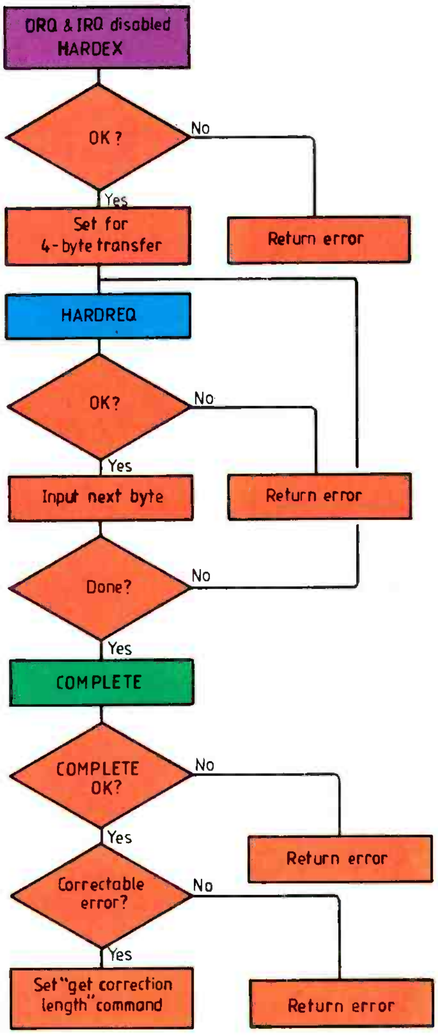
Probably the most dissimilar examples of d.m.a. processing are the 8237 and the HD64180 so the approach taken in the circuitry should cover other processors' requirements. By gating HD64180 $\overline{\text{IOE}}$, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals together, an active-high signal is produced during any i/o operation. This combined signal is inverted using part of a transparent latch wired to be permanently transparent and then gated with the ST signal to produce an active-low signal signifying a d.m.a. i/o operation. When active, this signal freezes the states of the DRQ lines coming from the hard-disc controller.

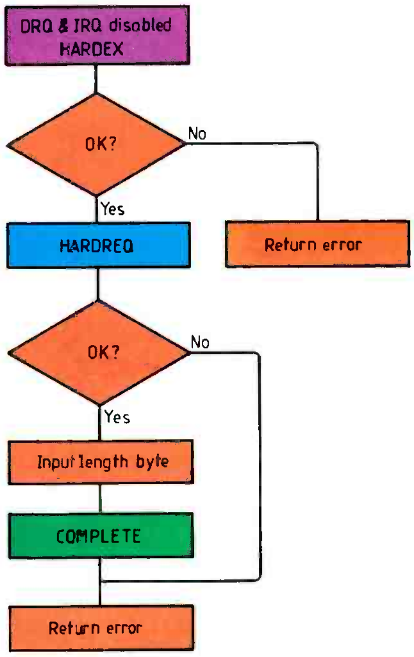
After further gating with the "DMA I/O" signal, this latched signal forms an active-low signal signifying "d.m.a. i/o taking place in response to my d.m.a. request" which conforms to the 8237 $\overline{\text{DACK}}$ signal. Signal DRQ has to be latched because one of the responses of the peripheral board to a $\overline{\text{DACK}}$ signal is to turn off the DRQ. If DRQ is not latched, the DACK signal is removed immediately.

One awkward feature of the controller board is that its DRQ output floats when the controller d.m.a. is disabled. An open-collector gate drives the bus $\overline{\text{DREQ}}$ line and polarity of the DRQ signal combines with the naturally high input of t.t.l. gates to produce a permanently active $\overline{\text{DREQ}}$ signal under these conditions.

To counter this effect a pull-down resistor is used. The resistor's value must be low enough to pull the low-power Schottky t.t.l. input to a logical zero when DRQ is disabled yet high enough to allow the controller to pull the DRQ line high enough to produce a logical one without overloading its output. For this reason, only low-power Schottky t.t.l. must be used for this device.

The circuit is a general purpose IBM interface with extra DRQ and INT lines which are not used with the SC84 implementation of the hard disc interface but which may be of use in other applications. Signal AEN is provided but should not be used in SC84, the AEN input to the controller being wired low. No buffering of the address or data lines is provided as it is expected that the peripheral





board will provide standard buffering.

When using the unit in the SC84 the controller board should be mounted on an IBM inter-face card using nylon p.c.b. spacers and hard wired to it using short sections of ribbon and single cable.

To the host computer, the hard disc controller appears as an 8-Kbyte eprom at address C8000-C9FFF (48000-49FFF for SC84) in the memory map and as four consecutive i/o points at addresses 0320-3 or, by a link option, 0324-7. The first port is a bi-directional data port. Status of the controller is provided by the second port, which is read only. While read-only, this port may be written to in order to reset the microprocessor on the controller board. The third port is read-only and reads the external eight-bit port described earlier. This port can also be written to in order to prime the controller board for a command sequence. Interrupt and d.m.a. hardware functions are enabled or disabled through the fourth port, which is write only. When using a Z80 or HD64180-based host, load the BC register with the i/o port address and then use instructions IN g,(C) and OUT (C),g to effect the transfer between the port and general-purpose register g.

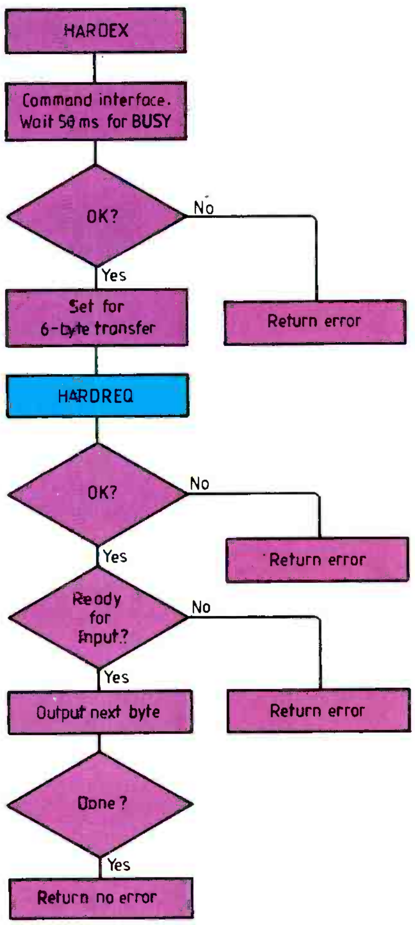
There are four phases in the controller execution sequence – selection, command, data (some commands only) and completion. The BUSY flag is set by the selection phase and remains active through to the completion phase. During the command phase six bytes of data are passed to the controller. Most commands have no data phase but if they do, data is transferred by either d.m.a. or programmed means.

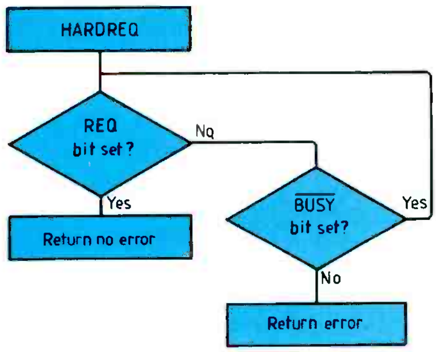
If the IRQ function is selected during the command phase, the IRQ bit in the status register or the external IRQ signal can be used to indicate that the controller is ready to pass to the completion phase. When the host reads the completion byte from the controller data port the command is completed. Any error in the command execution is signalled in this byte.

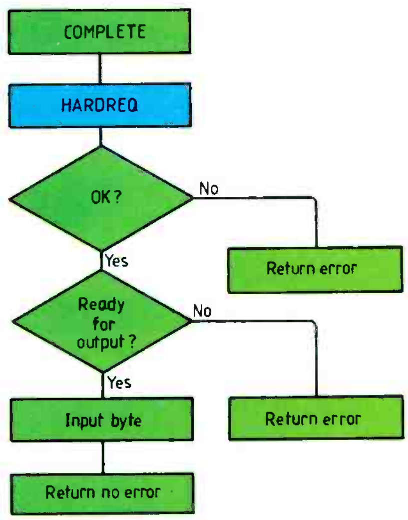
In the event of an error, the host may execute another command for reading the status of the last operation to obtain information about the error. Note that this command is completely separate from the one it is reporting on and is subject to its own errors. Software for the controller must allow for this.

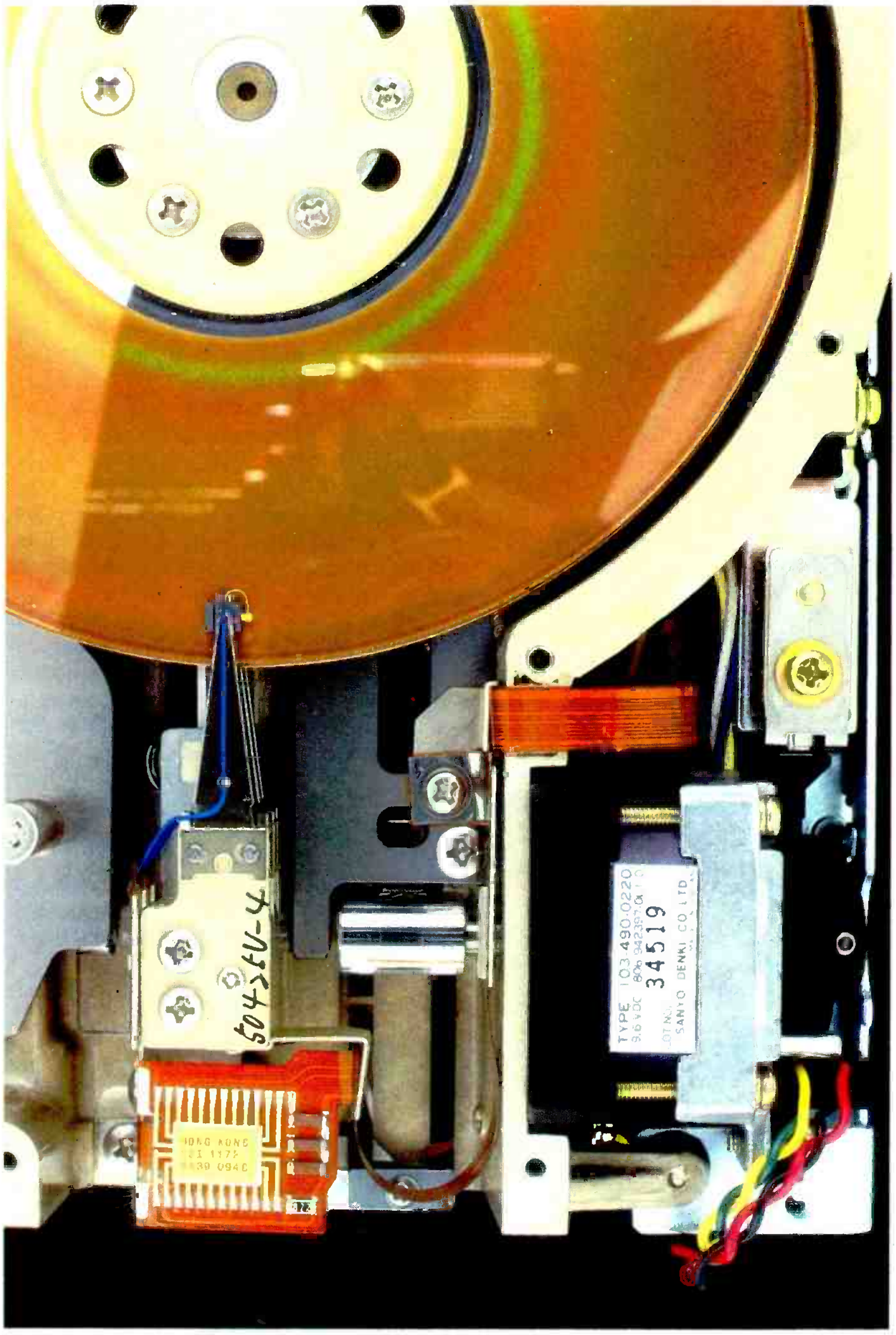
All non-d.m.a. data transfers between the host and port 0320 of the controller must be qualified by the bits BUSY, C/D, I/O and REQ in the status register. Driving software must contain a routine to check the status of the controller (REQ and BUSY set) before contemplating a transfer and then must further check C/D and I/O to make sure that the direction and type of transfer expected by the host is that expected by the controller.

Error data available when the command completion byte indicates an error has the same structure as the first four bytes of the









Hard drive controller-board connections and options

A	Edge connector	B
n.c.	1	0V
D_7	2	RESET
D_6	2	+5
D_5	4	NC (IRQ_2)
D_4	5	NC
D_3	6	NC
D_2	7	NC
D_1	8	NC
D_0	9	+12
NC	10	0V
0V (AEN)	11	NC
A_{18}	12	MEMWR
A_{18}	13	IOW
A_{17}	14	IOR
A_{16}	15	DACK
A_{15}	16	DRQ
A_{14}	17	NC
A_{13}	18	NC
A_{12}	19	NC
A_{11}	20	NC
A_{10}	21	NC
A_9	22	NC
A_8	23	NC (IRQ_5)
A_7	24	NC
A_6	25	NC
A_5	26	NC
A_4	27	NC
A_3	28	NC
A_2	29	+5
A_1	30	NC
A_0	31	0V

Hard-drive option switches; SW_1 (D3126), TERMRES SW (D5126) – all switches on, SW_2 (D3126), DS (D5126) – switch 2 on, all others off, SW_3 (D3126) – all switches off.

J_1 is 34 way ribbon cable to drive J_2 is unused and J_3 is 20 way ribbon cable to drive.

Option links in place are W_3 link 1-2, W_4 link 2-3 nd W_6 link 2-3.

command block except that the first byte is the error code with bit seven set to indicate validity of the current and subsequent three bytes. By reading this code back into the buffer used for the command block, the block is automatically set to retry or continue since the details returned are those of the failed sector and/or track when an error occurs or in the event of no error those of the next track.

Sector count is the number of sectors to be processed during read, write and verify operations. Sector interleave is the skew allowed in between sequentially numbered sectors and applies during formatting operations.

Interleaving (or skewing) is necessary as the hard-disc controller reads data from a sector into an internal buffer memory and then offers the data to the host computer (or vice versa for writes). Hence if truly sequential sectors were used, unless the host was extremely fast, the start of the next sector to be processed would already have passed under the drive heads before the system was ready to process it. A delay of one disc revolution would be needed before that sector could actually be accessed. The optimum interleave is a function of the host processor's ability to service the internal buffer.

Unfortunately, Western Digital (and other controller manufacturers) do not provide direct d.m.a. bypassing the buffer, for systems such as the SC84 which are easily fast enough to process the disc data directly. More annoyingly the controller card cannot handle the interleave of two (i.e. read/write every other sector) even when the external d.m.a. process only takes half a sector period, and so the minimum practical interleave appears to three.

Thus it takes three disc revolutions rather than one to read a complete track. This is the price to be paid for using an off-the-shelf product. In practice this may not greatly affect overall system performance. While it adds 100ms to the time taken to read a complete cylinder (34-Kbytes), the average seek time of 85ms and the fact that files are rarely written as one contiguous block means that operations to access different parts of the file may become dominant.

All errors other than e.c.c. ones are affected by the general-retry bit. When the bit is set any error is immediately reported. When the bit is clear ten attempts are made to recover the error. If the requested sector is not found, recalibration to cylinder zero, a re-seek and then ten more attempts to execute the command are carried out.

When the e.c.c. retry bit is set the e.c.c. code is used to attempt to correct an error as soon as one is detected. When the bit is clear no attempt is made to correct the error until two consecutive error patterns are the same, providing extra protection against error.

Stepping rates vary between 3ms (bit pattern 000) and 10.5μs (bit pattern 111). Given a drive capable of "buffered seeks" as high a rate as the drive can accept should be used. Buffered seeks are ones where the number of stepping pulses are logged rather than executed by the drive, which then produces the optimum sequence of pulses to move and settle the head as quickly as possible. Increased speed produced by this "intelligent" stepping is quite impressive and so drives with buffered seek capability should be chosen.

A feature of this controller is that it doesn't check the seek-complete signal at the end of the SEEK command's execution but at the latest point possible in the following command. Thus the host computer can issue a seek, do something else such as set

Controller board data structures

Port 320 bit significance (returned by routine COMPLETE)

Bit	Label	Function
1	E	Set if an error occured
5	D	Drive number

Port 321

Bit	Label	Function
0	REQ	Controller is ready for a data transfer when set.
1	I/O	Controller is to be read when bit set, written to when bit clear.
2	C/D	Data is expected when bit set, a command or status byte when bit clear.
3	BUSY	Controller is executing a command if bit set.
4	DRQ	D.m.a. request bit.
5	IRQ	Interrupt request bit.

Port 323 bit significance

Bit	Label	Function
0	DRQEN	Enables DRQ external signal and status bit.
1	IRQEN	Enables IRQ external signal and status bit.

Command block

Byte	Function
	Op-code for command to be executed
1	Bits 0 to 4, head number. Bit 5, drive number
2	Bits 0 to 4, sector number. Bits 5 to 7; m.s.b. of cylinder number
3	L.s.r. of cylinder number
4	Sector count or interleave
5	Bits 0 to 2, step rate. Bit 6, e.c.c. retry bit. Bit 7, general-retry bit.

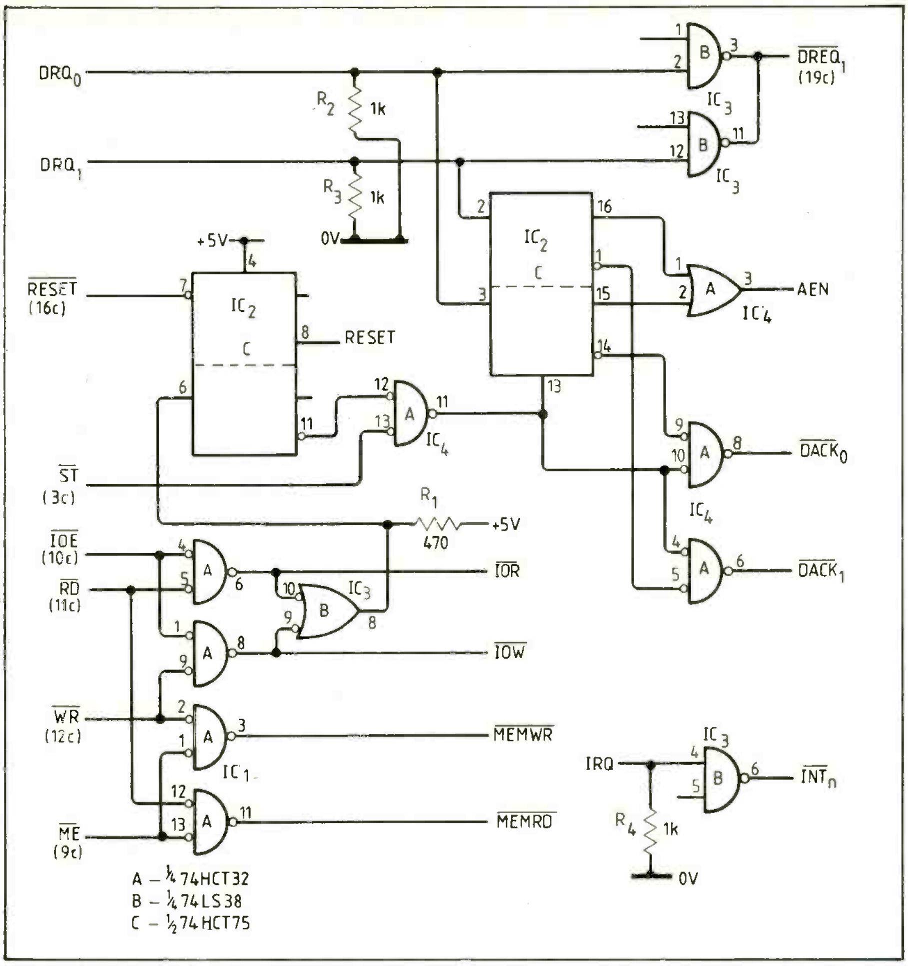
Initialisation data

Length	Function
Word	Number of cylinders (615)
Byte	Number of heads (4)
Word	Reduced write-current start cylinder (doesn't matter)
Word	Write precompensation start cylinder (128)
Byte	Maximum e.c.c. Burst Length (11)

Values in parenthesis are for the NEC D5126 drive

Error codes in hexadecimal

Code	Error
00	No error
02	SEEK COMPLETE has not become active (occurs 3.5s after executing SEEK)
03	WRITE FAULT active
04	DRDY not active when drive selected
06	TRACK ZERO has not become active during a RECALIBRATE instruction
08	Drive still seeking. This is no so much an error as a request to wait
11	Uncorrectable read error
12	Data address mark not found in sector
15	Sector identification requested not found
18	Corrected read error. This warns that the read was marginal. The e.c.c. burst length may be read to assess how bade the potential failure was, and on the strength of that, the sector re-written or the complete track reformatted.
19	An attempt to access a track marked as being bad
20	Invalid op-code
21	Invalid sector number
30	Error during sector-buffer test
31	Internal rom sum-check error diagnostic test of controller c.p.u.
32	Error during test of e.c.c. generator.



Interfacing Z80-like signals to a low-cost controller board is easy – most of the circuit is devoted to matching two different d.m.a. systems. The connector numbers are for SC84 using the 64180 processor.

These commands ignore command block parameters.

Op-code	Operation
0E	Read sector buffer
0F	Write sector buffer
E0	Execute sector buffer diagnostic test
E4	Execute controller diagnostic test

Only a drive needs to be specified in these commands.

Op-code	Operation
00	Test drive ready
01	Recalibrate to track zero (also needs general-retry bit)
03	Read status or last operation
0C	Initialise drive parameters
0D	Read e.c.c. burst length (only valid after error type 18)
E3	Execute drive diagnostic test (also needs general-retry bit and step rate)

These commands need all parameters. Byte four is the sector count.

Op-code	Operation
05	Verify sectors
08	Read sectors
0A	Write sectors, e.c.c. bit not used
E5	Read long
E6	Write long

Following commands need all parameters to be valid, although the sector and e.c.c. parameters are not used. Byte four is the interleaved factor.

Op-code	Operation
04	Format complete drive
06	Format track
07	Format bad track
0B	Seek specified track (byte 4 not used)

Format commands generate 17 sectors of 512 bytes each numbered 0 to 16 and interleaved as specified.

All diagnostic commands start with E_{16}. No error codes are generated by the executive controller-diagnostics test. The series of tests are repeatedly executed until an error occurs or until the controller is primed by writing to port 0322. When an error occurs and error code is put on the ST506 head-select lines. Under these conditions, the head number implies 1, error in WD1010A. 2, error in WD11C00-17 e.c.c. mechanism, 3, error in sector buffer, 4, error in WD1015 ram and 5, error in WD1015 rom.

Read and write-long operations allow the e.c.c. system to be tested. If an e.c.c. error is occurring it may be due to a disc fault, an e.c.c. checker fault or an e.c.c. generator fault. Read-long reads both the 512 data bytes and the four appended e.c.c. bytes. Used after a conventional write, this command can be used to see it is the e.c.c. pattern on the disc or the e.c.c. checker that it at fault.

Having performed the read-long test, the write-long operation writes both the 512 data bytes and four e.c.c. bytes back onto the disc, bypassing the e.c.c. generator. Now, reading the sector normally it can be establishes whether the disc or e.c.c. generator is at fault.

DRIVE AND CONTROLLER PRICES

Two drives suitable for this development are similar in performance and storage capacity, the only differences being in size and power consumption. The D5126 has the outline of a half-height 5.25in floppy-disç drive and requires 5V at 1A and 12V at 1.8A (2.5A peak start up current).

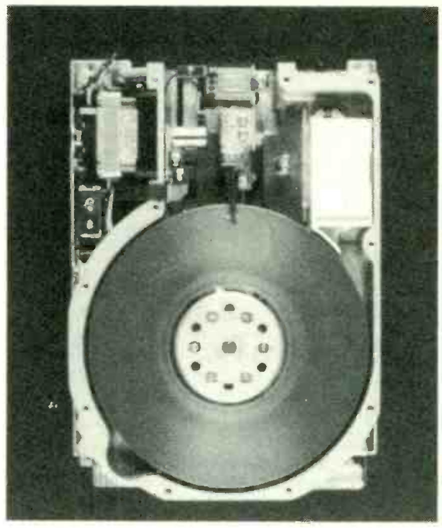
A smaller unit with the outline of a 3.5in floppy-disc drive is the D3126 requires about half the power of the larger drive. As the drives are almost the same price, the smaller one is the best choice, especially where power consumption and cooling need to be considered.

Pronto are offering these NEC drives and WD interface cards to E&WW readers at special prices. The D3126 20-Mbyte 3.5in drive is £341.73, and the DS5126 20-Mbyte drive is £333.26. Cables are included with the controllers, which are the WD1002S-WX2 at £89.63 and the WD1002-WX1 at £99.76.

All prices include v.a.t., UK postage and packing. Please send cheque with order to Barry Rennick at Pronto Electronic Systems, City Gate House, 399 Eastern Avenue, Gants Hill, Ilford, Essex IG2 6LR.

Boards for the SC84 to WX1 interface circuit shown in this article are available from Combe Martin Electronics at King Street, Combe Martin, North Devon EX34 0AD for £8 each inclusive (UK or overseas).

Components are available from John Adams. The complete SC84-to-WX1 interface set is £7.25 excluding v.a.t. to UK readers, £7.75 to readers within Europe and £8.25 to readers outside Europe. Small modifications are needed to the board and kit if the WC2 board is used. John is at 5 The Close, Radlett, Hertfordshire WD7 8HA.



another drive seeking and then return and perform a read or write command. All of this serves to speed up the system.

OPERATING SYSTEM REQUIREMENTS

Application of a hard disc drive requires the hardware to implement it, the driver to operate it and a system which can use it. To an operating system there are only two differences between hard and floppy discs. The most obvious is storage capacity, the other is the cost of the disc.

To expand on the latter point, if a floppy disc is not perfect you can replace it for one or two pounds. Perfection in a hard disc may literally cost hundreds of pounds as it is not just the disc but the whole drive that has to be replaced. For this reason manufacturers of hard drives supply units which are not 100% defect-free. In fact hard drives are graded by the manufacturer. A commercial compromise is struck and so the drive you obtain may have defects which the operating sysem must be able to tolerate. There is no hard and fast rule as to number of defects but a common practice is that cylinder zero of the drive must be perfect.

Imperfections can be handled in three ways. In some systems the controller reserves tracks which it substitutes for faulty ones much in the same way that in the new, larger, dynamic memories, rows of extra storage cells are available to connected in place of faulty ones. This technique reduces disc capacity by the number of reserved tracks and also slows disc access since the reserved tracks may be on a completely different part of the disc.

A technique which maximises good disc space is for the controller to split the disc into logical and physical storage units and then form a translation table between the two, the mapping of which skips over defective physical units. This allows the host computer to talk to the hard drive controller in terms of logical units wihout it needing to know of tracks, heads or sectors, but is makes the controller quite complex.

The third technique is similar to the second except that the mapping-out of defective areas on the disc is handled by the operating system. Being part of the operating system rather than a hardware subsystem enhances overall system flexibility.

Most disc-operating systems maintain files and a directory of those files. The directory contains an entry for each file detailing at the least the name of the file and the point on the disc at which the file begins. Thus the directory links something a human recognizes with something the computer can use to provide access to the named file. It is over this aspect that operating systems falter when presented with a hard disc as, simply due to the disc's enormous capacity the directory may contain hundreds – even thousands of files names.

Operating systems pre-dating large storage media, such as CP/M, were essentially single-directory systems. Later versions of CP/M and CP/M-compatible systems such as ZCPR have allowed extra directories to be placed on discs but the changes have subdivided the hard disc into many smaller units rather than expanding the attributes of the operating system.

Directories created under such systems are almost completely isolated from each other. Post-hard-disc systems, such as MS-DOS also support multiple directories but each directory is part of a hierarchical system. Thus at the highest level is a single directory often called the root, below which may be sub-directories called ACCOUNTS, CAR, ARTICLES, BILLS, etc. Within the BILLS environment for example there may be further directories called GAS, WATER, ELECTRIC and CLEANING and in each of those, directory files such as 1984, 1985 etc., or even other directories.

Structured directories of MS-DOS are more in line with the human approach to filing. You have an office within which are filing cabinets, within which are drawers, within which are files, within which are papers, on which are paragraphs etc., etc., but MS-DOS is not an eight bit system and so users of eight bit systems such as SC84 have not had access to such facilities.

To complete the application of a hard disc to the SC84, a new version of the operating system SCIDOS, version 3.0A, has been developed which offers the same concepts and native commands as MS-DOS but in a CP/M compatible system and in a package one tenth the size of MS-DOS! The difference in size illustrates the benefits of RISC (reduced instruction-set computing) as a means of minimizing code and of implementing software at assembly-language level. The resident portion of the DOS occupies less than 3-Kbytes of logical memory leaving the user with more than 59-Kbytes of working space.

New features introduced in this version of Scidos are a fully-structured, hierarchical directory system with user-defined search paths and file sizes only limited by disc capacity. File (and directory) allocation is on the daisy-chain system, resulting in typically 15% extra storage capability on a floppy disc. CP/M application software is incapable of handling any of the new features so to control them are in the enhanced CCP. This now processes BAT files and commands CHDIR, MKDIR, RMDIR, PATH and COPY in an MS-DOS-like way as well as recognizing command file-specifications including pathways.

Signal processing on a PC

Waveform processing, display and manipulation is possible with a software package from Tektronix for use on an IBM PC-AT or XT. Signal processing algorithms, enhanced graphics and flexible data structures are included in the package. Time-domain displays can be converted into frequency-domain using an FFT program. More than 190 processing functions are provided through a menu-driven interface. The programs are written in C and may be accessed directly through C, by menu selection or through a Basic interface included in the program. The signal processing and display (SPD) package includes colour and graphics with multiple displays and grids. An anti-aliasing wave display removes the staircase effect of digital sampling.
226 on reply card.

HPIB extender

A major enhancement to the GPIB (HPIB, IEEE 488) interface is Hewlett-Packard's HP37204A extender which allows the bus (restricted in its definition to two metres) to be used up to 1250m. This means that the bus can now be used for distributed equipment all over a factory or office environment for testing, measurement and control. For example, a number of printers and plotters can be controlled from a single port on a computer. A system can be expanded by adding single extenders and the multi-point capability allows daisy chaining of remote sites. Up to 30 sites can be linked in this way.
217 on reply card.

Signal source with pulses

Sine, triangle, squarewaves and pulse trains can be generated by the Global 8241 multipurpose programmable pulse/function generator. The frequency range is 2MHz to 20MHz. It provides complete control over amplitude, symmetry, offset, pulse width and pulse delay. It is claimed to be the only instrument which allows independent adjustment of the rise and fall times of leading/trailing edges. Output can be continuous, gated or triggered internally and externally. An internal timer is provided for repeated trigger generation and a burst counter can provide a specific number of bursts up to 500 000. The instrument can be programmed though a GPIB interface and battery-backed ram can store and recall up to 10 front panel settings.
212 on reply card.

Low-cost function generator

All British in design and manufacture is the Jupiter 500 function generator from Black Star Ltd, which offers sine, triangle and squarewaves from 0.1Hz to 500KHz. A special feature is the instrument's high output amplitude which can be varied up to 30V peak-to-peak with a d.c. offset from −15 to +15V. There is also a low level output and a t.t.l. square wave that can drive up to 30 loads. Output amplitude and frequency sweep are voltage-controlled through external connectors.
213 on reply card.

Precision watts

Six different version of the Yew 2533 precision power meter cater for different applications including those where distorted waveforms can cause measurement problems. Three 6-digit displays are incorporated and the instrument can measure volts, amps and watts in single or three-phase circuits and will produce parallel analogue outputs for each measured parameter. The computer can calculate and display real, reactive or apparent power and power factor. Accuracy is 0.01%, voltage and current imputs of 30 to 600V and 0.5 to 20A are autoranging and will cover frequencies up to 20kHz. Internal processing enables the programming of transformer ratios for direct reading from external transformers. IEE 488 and RS232c interfaces are available.
224 on reply card.

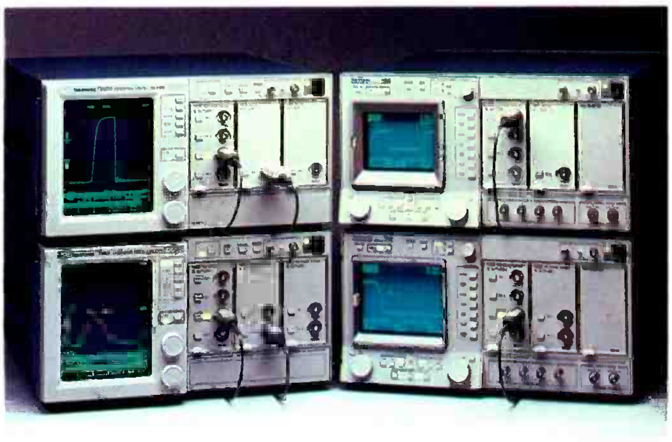
New generation of oscilloscopes

The most noticeable difference between the new 11000 series oscilloscopes from Tektronix and more conventional ones is the absence of the majority of front controls and buttons. This is because they have been replaced by a touch-screen controller. Internally, powerful computing processors have been added to offer such facilities as automatic display of waveform, trigger control, cursor control, windows, pull-down menus and many other facilities, all operated just by touching the appropriate part of the screen. In multi-trace displays, for example, waveforms of interest are highlighted by operator touch. Displayed measurement data then refers to the waveform which is highlighted. Mathematical manipulation of the waveform to calculate and display, for example, power factors.

Four models have been produced in the new series; two analogue and two digital; more are promised. Depending on the section of plug-in input modules up to eight waveforms can be displayed at one time. The two analogue oscilloscopes are 400 and 500MHz models, both with built in 500MHz counter/timers and a counter-view trace enables the user to see exactly which part of the waveform is being measured. Traces can be superimposed, added to or subtracted from each other, with the Y-T and X-Y signals being displayed simultaneously. Despite being analogue instruments, they can store digitally reference waveforms for comparison. Highly accurate timebases are included.

The two digitizing oscillocopes are 500MHz and 1Ghz and display 10240 points across the screen. Each has a 9in screen and is claimed to have the largest waveform display area of any oscilloscope. They have triggering levels that are accurate to within 1% of full-scale and adjustable in 0.1% increments. 10-bit vertical resolution is offered and it is possible to have 14-bit resolution with signal averaging.

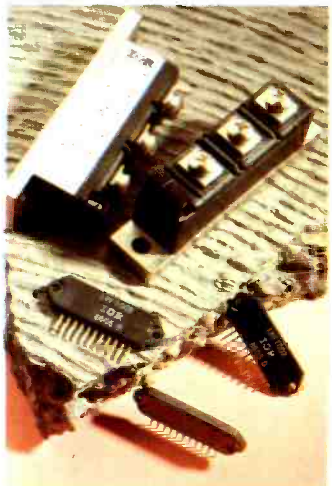
All the models incorporated a self-calibrating system and have both RS232C and GPIB interfaces for communication and control. They can be operated remotely through these interfaces in automatic test rigs. The digital instruments have a Centronics printer port.
205 on reply card.



NEW PRODUCTS
COMPONENTS

Power switching hexfets

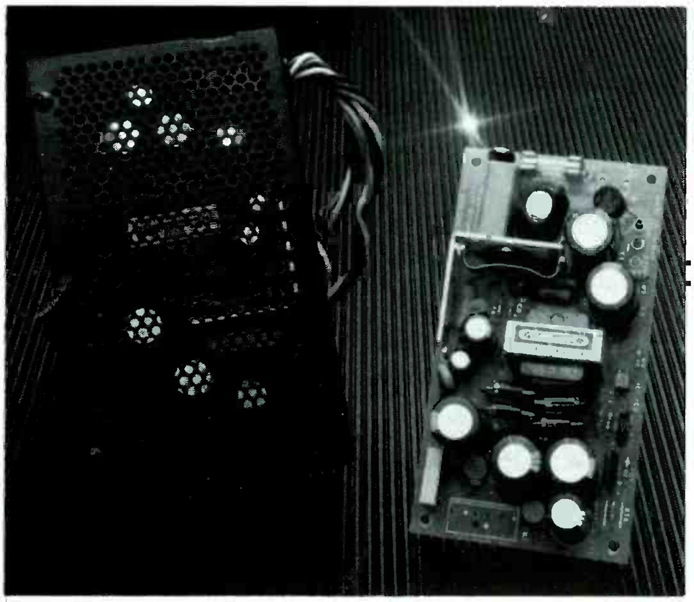
Hexpak is a high-power device containing four power transistors in either parallel or half-bridge configuration. Handling currents up to 145A and a very low residual drain/source resistance, with fast switching, the device is suitable for switching high energy pulses. Their compactness eases assembly and saves space. These IR devices are available through Hi-Tek Electronics.
223 on reply card



Isolated power Darlingtons

Two 1000V versions of the Semikron range of power Darlington modules feature a built-in isolated baseplate which makes it easier to mount one or several onto a common heatsink while all electrical connections are on the top of the package. The devices incorporate parallel connected, fast recovery, inverse diodes and so reduce the count of external components.

SK30DB100D has a maximum continuous collector current rating of 30A while the SK30DB100D can handle 50A. Each has a total power disipation of 300 and 400W respectively.
210 on reply card.



Low cost switchers to order

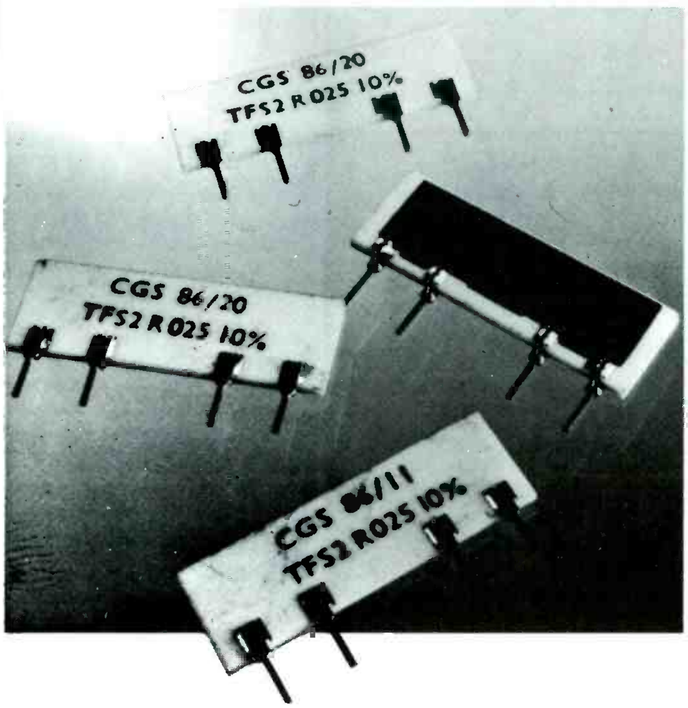
A range of six 30W switching power supplies can be arranged to meet customers' specific requirements for voltage and cabling. The ACP-188 series of flyback supplies from Akhter offers single, dual or triple outputs and can be supplied with or without ventilated case. Output voltages range from −12 to +24V with currents from 0.2 to 6A. All models operate at an efficiency of about 70%.

The supplies can provide a 40W output for a burst of up to 20s which makes the 12V version suitable for disc drives, stepper motors and solenoids. Unlike many power supplies they do not need a minimum load and are capable of driving high-energy circuits. The caged versions are sized to fit a 5.25in half-height hard disc drive.
244 on reply card.

Thick-film resistors

Thick-film shunts are used for current sensing applications on densely populated p.c.bs. The four-terminal TFS2 series from CGS. allows detection of very small changes in voltage or current levels due to environmental changes.

Stability is <2%/1000h at the rated dissipation of 2W at a maximum current of 10A. Temperature coefficient is ±0.05%/°C. Values available are 10 and 20mΩ with 10% tolerance and 50, 100, 250 and 500mΩ and 1Ω. with 5% tolerance.
243 on reply card.



Desolderer

Simple ideas are often the best and this desoldering tool from Antex is a good illustration. It combines a sprung desoldering pump with one of their soldering iron elements. Push the nozzle onto the point to be desoldered, hold for a couple of seconds and release; the solder is drawn up and, because the pump is heated, it remains fluid and can be ejected using the same action. As the pump is fixed permanently to the heating element, this is a separate tool, not an add-on for the soldering iron.
220 on reply card.

Flat relays

Provided with a dil package and a height of only 6.5mm, the SA series of relays from SDS-Relais are available with one or two open or closed contact. Low wattage on the coils makes tham suitable for use in telecommunications, measurement or alarm systems on p.c.b. with high density of components. Isolation between coil and contacts is 1500V. The relays can be combined with the C series of switching circuits which provide latching of the relay with no further power comsumption.
213 on reply card.

Stable p.c.b. film

A new film for the photographic images of p.c.b. racks has been produced by Dupont. As component pinouts become closer and more complex further precision is needed in the production of the boards. Currently used films can change dimensions rapidly with changes in temperature and humidity. Dimension Master, the film with a new polyester base and hard emulsion, expands three to five times more slowly in response to humidity changes and under a normal humidity cycle of ±8% relative humidity over 24h, the film will remain within a tolerance of 1 in 24000. It is also thicker and tougher than conventional films so will last longer. The principle advantage is that it may be used in existing production phototooling equipment, without needing to upgrade to accommodate p.c.bs requiring greater precision.
219 on reply card.

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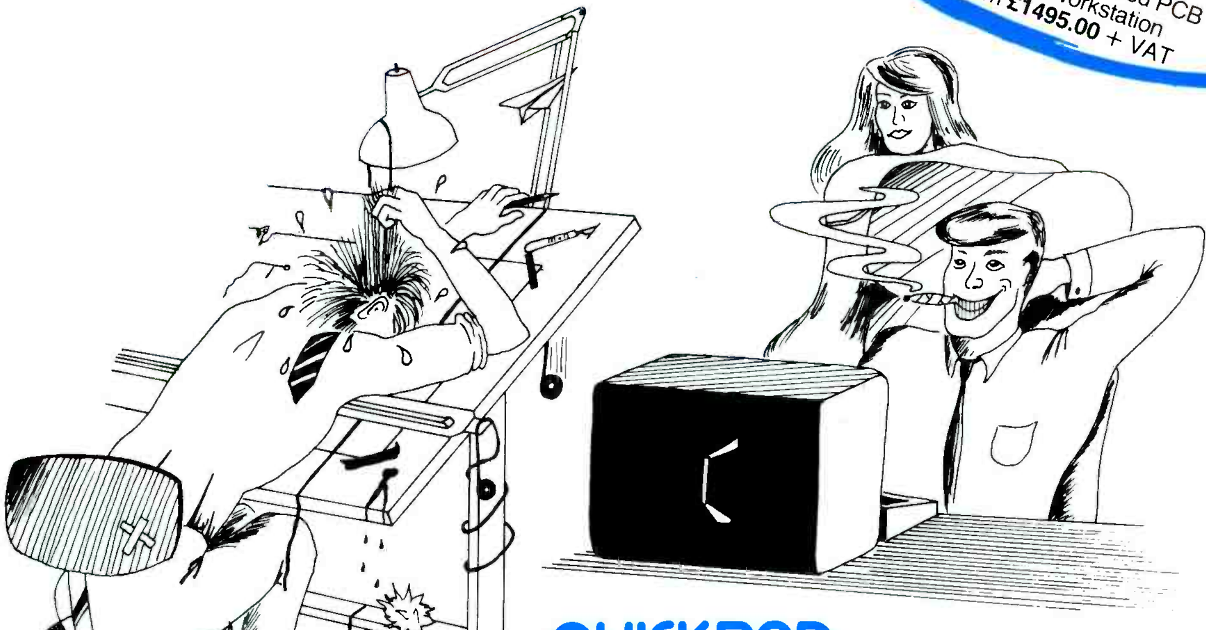

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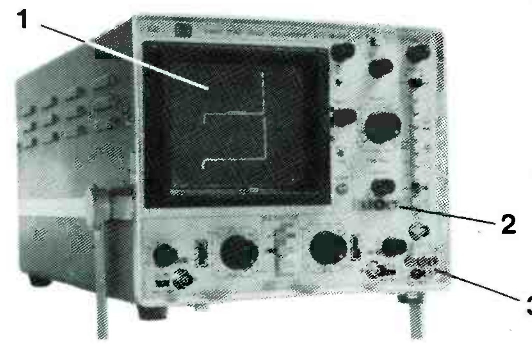

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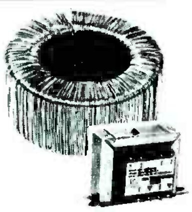

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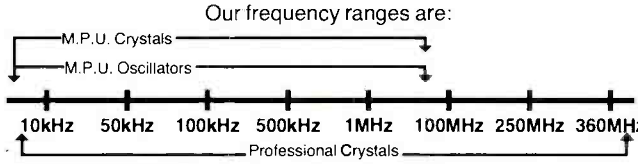

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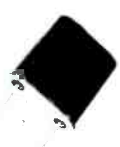

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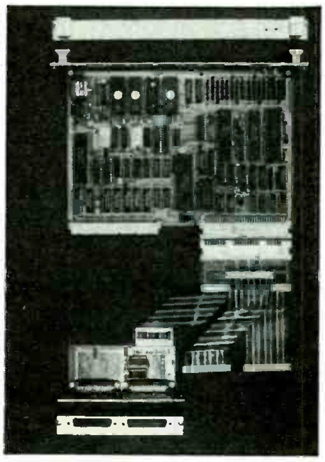
ENTER 23 ON REPLY CARD

STE processor card

A double Eurocard is used to implement a c.p.u. card built around the STE bus. The SPC-180 from Kemitron uses the Hitachi HD64180 processor which runs Z80 code, has two serial channels, an on-chip timer, runs at 6MHz and can address up to 2Mbit ram. The board is provided with 512Kb of eprom or 96K of static ram. A further two serial channels are provided which can be configured to RS232, 20mA, or RS422. Disc control facilities include a SASI interface for hard disc. Further facilities include a maths co-processor, real-time clock, watchdog timer and status indicator. The second DIN connector allows the board to be completely plug-in and all connectors can be routed through the backplane. The board may be incorporated into an STE-based system and, as it contains all the necessary functions, can also be used as a stand-alone computer.
221 on reply card.

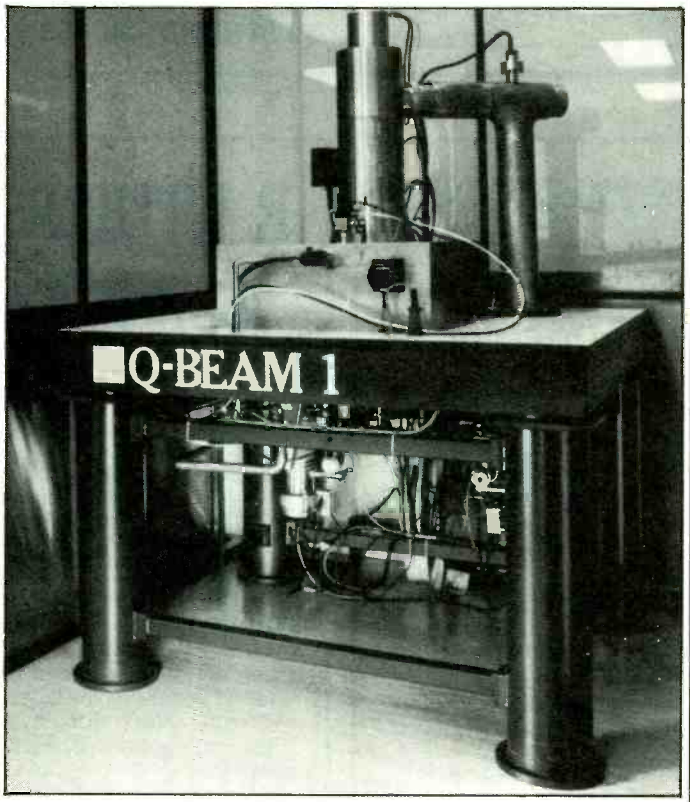


Fastest p.c.b. design

The Vutrax p.c.b. design system from GM Design has not been changed but, used with the Compaq 386 computer, its speed has been increased by two to three times. This is the fastest design system available in the market today, claims GM. An example is the ability to autoroute the tracks on a circuit board with more than 100 components to 98% completion in three minutes. The computer is built around the Intel 32-bit 80386 processor and features up to 14Mbytes of ram, 130Mbyte of hard disc storage with a 25ms average access time and 40Mbytes of tape streamer backup. Alan Mallyon (the marketing manager of GM) claims that the 386 offers the power of a much larger "number cruncher" in a desk-top. A series of one-day seminars has been arranged to demonstrate the capabilities of the system.
233 on reply card.

RS232 made easy

An RS232 rescue kit comes from Componedex. It contains a selection of useful and educational items for interfacing computers with printers, Terminals and modems. Included is the Cablefaker breakout box and monitor, a gender change ribbon cable, patch box and tools and a 200-page manual *RS232 made easy* along with quick reference card.
229 on reply card.



Low cost quick chip design

An advanced, fully integrated, heirarchical design system, providing automatic layout, simulation, routing and rule checking of gate arrays is provided by the Quickchip c.a.d. package for v.l.s.i. from Qudos. Based around the 32-bit Acorn Cambridge Workstation, the entire system including the c.a.d. software, 4MByte of ram, 20MByte hard disc, colour monitor, floating point maths, and a software bundle of five standard languages, all costs £7500 which is less than the cost of software alone on many systems. Quickchip is also available for computers running Unix. Designs produced on the system are submitted to Qudos on floppy disc or magnetic tape and can be manufactured, using their electron-beam lithography facility in a very short time.
235 on reply card.

STE-bus SCSI interface board

Mass storage peripherals with standard SCSI interfaces can be easily connected to the STE-bus using a board from Arcom Control Systems. The single Eurocard use the NCR5380 i.c. to control up to eight storage devices and can be used with an external d.m.a. controller for high-speed applications. Arcom has drives for the Rodime 20MByte hard discs and the routines work with any of their STE-bus c.p.u. cards running under Concurrent DOS, CP/M-80, or OS-9. Data transfer rates under OS control are typically three times faster than floppy discs; outside the constraints of the operating system the rate can be ten times faster.
242 on reply card.

68000 cross assembler

The latest addition to the XA8 series of cross assemblers from Real Time Systems is the X68000 which is suitable for the 68008 and 68010 as well as the 68000. It will run on Unix and VMS computers and on PC/MS-DOS computers (IBM-PC and clones). The XA8 series is available for more than 60 target processors, running under a wide variety of operating systems. It provides full listings, macros and repeats, conditional assembly, importing of files, division of a program into sections, temporary labels and absolute addressing or relocatable code. The manufacturers' instructions mnemonics are used.
236 on reply card.

Transputer development systems

The 16-bit version of the Inmos transputer is now available from Hawke Components. Claimed to be faster than the 32-bit device (T414), the T212 has all the same features: 2Kbytes of on-chip sram and four communications links. Using Occam concurrency it is possible to achieve very high speed procedure calls, process switching, and interrupt latency. Also from Hawke is a series of transputer evaluation boards. The IMS B003 has three 32-bit transputers, B006 has nine 16-bit devices and the B007 has one 32-bit transputer along with a video ram and a colour look-up table to provide a video graphic driver board. Ten B003 boards (i.e. 40 32-bit transputers) are combined in the ITEM400 which offers up to 400mips.
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NEW PRODUCTS
COMPUTING

Video controller improved

A new c-mos version (HD6345) of their c.r.t. controller has been produced by Hitachi. Compatible with the HD6845 n-mos version, the new chip offers a higher clock frequency – 4.5MHz which allows an improved screen update. Its flexible screen format offers enhanced facilities including four split screens and smoother scrolling. The 6345 is compatible with the 68 family of processors while a similar device the HD6443 is for use with the 80 family including the Z80. The device offers a variety of functions under m.p.u. control including programmable timing signal output for c.r.t. monitor and display screen control operation. It can be applied to all types of c.r.t. displays. A standard 40-pin package is used for the device which operates over a range of 1 to 2MHz bus speeds.
241 on reply card.

Fast d.s.p.

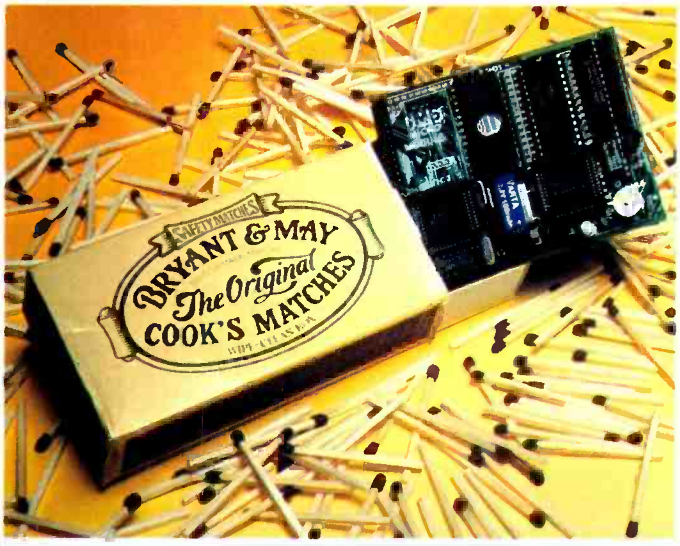
A new digital signal processor has been announced by Motorola even before its predecessor has been released. The DSP56001 offers a speed of 10.25mips, and 56bits. It is functionally identical to the DSP56000 but instead of 2Kwords of program rom it has 512words of program ram and a hardware bootstrap that enables this ram to be loaded with the user's program easily. The advantage is that it does not need to be mask programmed and becomes an off-the-shelf product. There are also two other roms. The X-rom is preprogrammed with Mu-law and A-law to linear conversion tables for the interfacing of codec/filter chips and time division multiplexed networks, the Y-rom has a sine table for waveform generation and F.F.T. analysis. Also on the chip are serial communications interface, a synchronous serial interface, and a host interface.

The processor has seven buses so that the three arithmetical logic units and the program controller are not waiting for each other. Applications include communications and speech processing as well as high-speed control, image processing for instrumentation and navigation and audio. Both d.s.ps are to be available in sample quantities early in 1987 and for those who can't wait or want to get cracking in advance, Motorola have made available a simulation package and macro-assembler in versions to run on many micro and minicomputers.
208 on reply card.

Matchbox Beeb

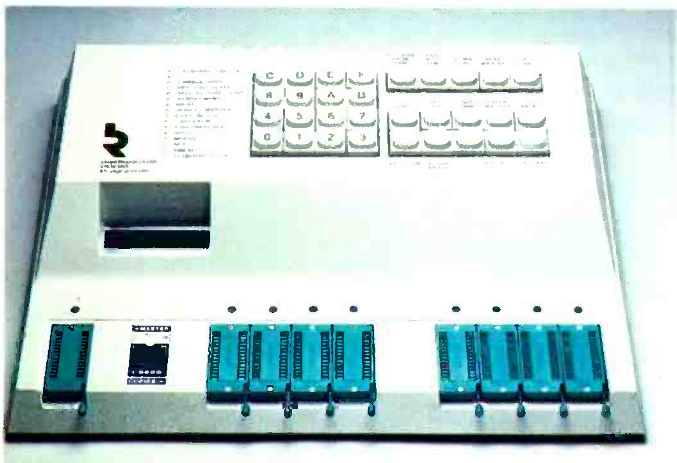
A multitasking version of the BBC micro has been mounted on a multilayer board, by Cambridge Microprocessor Systems. It combines surface mounted components with conventional ones to fit on a board just 3.5 by 2.5in. The 6502-compatible system can support a whole host of functions including three independent programmable serial channels, RS422/423 interfaces, high speed synchronous serial interface, quad duart, two stepper motor outputs, four analogue input channels, 35 independent user definable i/o ports, liquid crystal display interface driver, six programmable counter/timers, real time clock, p.w.m. facility, up to 64K battery-backed ram 2K to 3Mbytes of eprom, 8MHz clock and a watch-dog facility. In addition it is possible to have a full-colour video output which includes teletext, user definable characters and 32K of paged ram. The board can be programmed in BBC Basic, Pascal, Forth or any other high-level language and can be networked to up to 126 remote stations.

The computer is designed as a control component for use by o.e.ms and can be used for almost any control/monitoring task from simple switching to complex applications requiring the full video display. The simplest configuration costs as little as £50, for the full bells and whistles variety it goes up to £300.
207 on reply card.



Improved eprom programmer

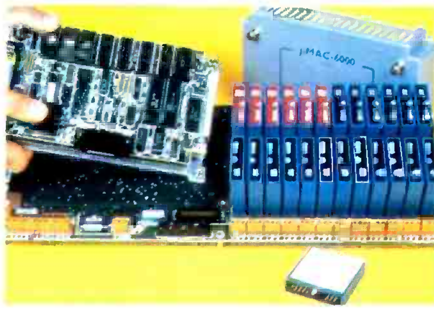
The hardware of the Lloyd Research 1000 series of eprom programmers is as good as it was but there has been a great improvement in the software to enable very rapid programming. It is now possible to download and program in one command, without manual intervention. The instrument can store such parameters as device type and set details and can store the files for eight different programs which can be all be programmed individually. Many more device types have been added to the internal list. The programmer can cope with eight 27256s at the same time or two sets of four 27512/3s. Another addition is the ability to program the Hitachi range of ZTAT processors which incorporate eproms. To accommodate these a low-cost adapter is added.
209 on reply card.



Industrial computer

A single-board computer system from Analog Devices is particularly suited to analogue input and output. It communicates through single-channel signal conditioning modules which may be configured to input and output, channel by channel. The computer combines direct sensor input, analogue signal conditioning and processing circuitry on a single board. Additional processing boards may be added which communicate through the GPIB interface so the computing power remains sufficient to cope, however, complex the system.

Applications for the µMAC-6000 include process control and monitoring and machinery control. Examples are test automation, boiler and furnace control energy management. It can be used as a remote slave processor in distributed control applications. The basic version consists of the computer board, which includes analogue and digital i/o circuitry. This fits into a backplane which accommodates 24 signal conditioning modules. The



system uses the 16-bit 8MHz 80188 processor and has space for the 8087 co-processor, if required. It features 14-bit d-to-a and a-to-d conversion, 16 low-speed counters, two high-speed counters, six frequency inputs, a real-time clock, 64K of user prom and 256K of battery ram, there is also 1Kbyte of e-eprom which can be reprogrammed without removing from the board, and can be used to store conversion factors, calibration constants, correction coefficients and the like. There is an RS422 port for communication with a host computer, two RS232 interfaces as well as the GPIB. The basic system can accept 72 i/o signals. The system can be expanded in many ways. The RS422bus can be used in a multi-drop mode to allow a host computer to communicate with up to 15 µMAC-6000s. The system may be programmed in C (libraries of additional routines for the control of applications are provided) or in a special version of Basic, although C provides much faster processing.
206 on reply card.

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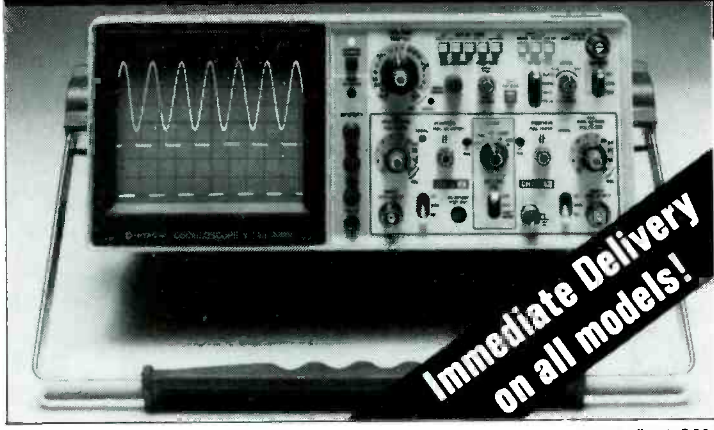

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Clean-up for video

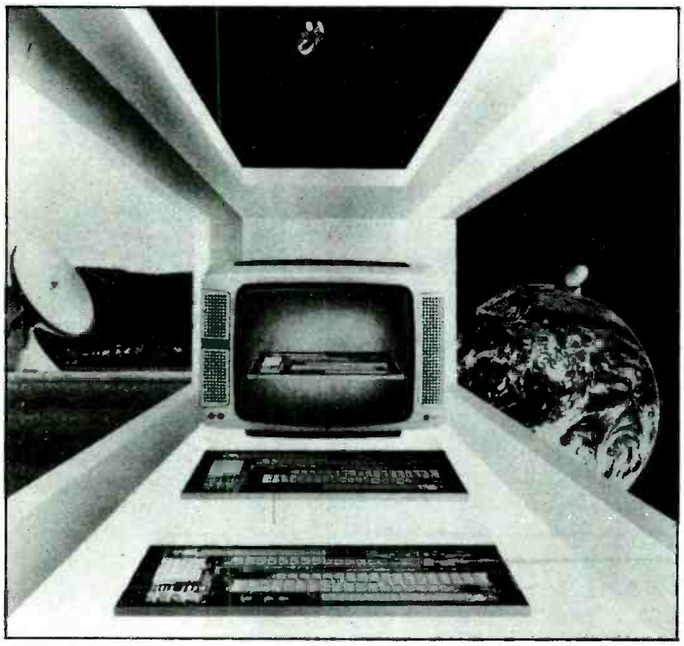
A real-time video noise processor can be used to improve the quality of a tv picture containing random noise. It is possible to process at 3000 pictures/min very poor signals where the noise exceeds the available signal. Improvements to the signal/noise ratio can be selected between 2:1 and 45:1 with corresponding processing times of 80ms to 82s. The Eltime video noise reduction system contains two frame store boards to hold the pre and post-processing images. The process can be viewed and controlled manually or an 'improvement factor' can be selected, allowing the processing to be continuous. Applications include enhancing low-power X-ray, electron microscope, night-vision infra-red, ultrasonic, and may other research and surveillance images.
225 on reply card.

Towards HDTV

Although standards for high definition tv have not be finalized, BAL components realize that any system will require high-precision delay lines and have produced 20MHz lines in both fixed and programmable formats. They have an amplitude ripple of <0.2dB at lower delay times and <0.3dB at the higher rates. Group delay ripple is <20ns peak-to-peak. Total delays are from 100 to 500ns in fixed modules and 5 to 155ns for the programmable ones. Impedance in all cases is 75Ω. BAL anticipate that this will meet most requirements for the initial stages but are contiuing work on widening the bandwidth and reducing physical size. A 30MHz delay line is likely to be announced soon. 240 on reply card.

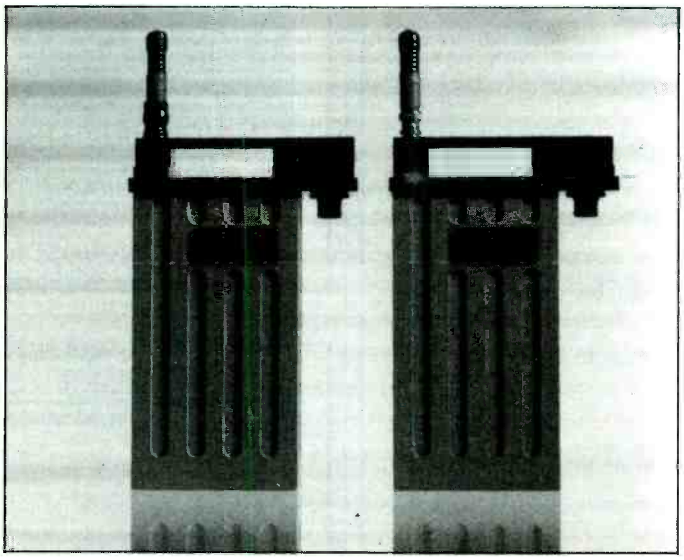
R.f. distribution amplifiers

A range of low-noise receiver multicouplers for the 70 to 250MHz range is claimed to be highly reliable. This is due, says Beronheath, to the use of generously rated power devices in a negative feedback circuit combined in an hierarchical structure, exclusive to this design. Input bandpass filters, including Butterworth and Tchebyshev designs, may be specified to meet individual requirements. 4,8, or 16 outputs can be provided (larger or intermediate numbers to special order). Input/output gain can vary between 0 and 3dB (more if needed) above the splitting level with low v.s.w.r. on input and output. Broadband circuits are used in the splitters and offer good interport isolation. Despite the high reliability, the units are easy to service.
214 on reply card.



DBS decoder chip

A single-chip decoder for use in direct broadcasting by satellite using the D2-MAC/packet system has been produced by ITT. Called the DMA 2270, the devices meets all the requirement of the D2-MAC standard, itself a subset of the C-MAC standard. Due to the baseband configuration, the chip is also suitable for decoding cable tv signals. The decoder is able to treat different sound services automatically by decoding the packet header. Eight sound channels are available for each tv service. All sound packets are converted into sequences of 14-bit samples. Medium-quality channels are up-sampled to the 32kHz sampling frequency so that all subsequent processing uses only one data format.
222 on reply card.



Radio data transmission

A single-channel version of Measurement Devices' Microtel transmits and receives data by digital telemetry. The system combines the functions of antenna, radio and modem in one unit. A simplex system consists of two portable units: each has a serial data port and up to five channels in the u.h.f. 400 to 500MHz band. Data rate is 1200Baud and it is possible to transmit over 50km as long as 'line of radio sight' is maintained. Two sets of units can be used to establish a duplex link. Applications include remote monitoring and control and guidance of unmanned vehicles.
228 on reply card.

Compact s.s.b. transceiver

Claimed to be the most compact full-feature s.s.b. transceiver in the world, the Link/4000 comes from Danish Communication Systems. It incorporates two microprocessors and 192K of ram. This allows the display to offer 'help' messages at the appropriate moment and monitors all the function of the set. There is a complete self-test on startup and the internal programs can control up to 80 preprogrammed frequency pairs and store up to 400 frequencies in memory.

Dual parallel amplifier stages ensure continuation of transmission in the event of a failure in one of the stages. An automatic antenna tuner, located on the set or remotely, can compensate for a broken antenna automatically. The tranceiver is designed for use in fixed/mobile operation on land or sea and has been particularly designed to be easy to use. A.c. or d.c. power can be used and the set can operate in simplex, semi or full duplex depending on the antenna installation; full duplex requires two antennas. Type approved under CEPT specifications the set can be installed, operated and serviced worldwide.
216 on reply card.

Digital video effects

This twin-channel system from CEL combines image control facilities from their Maurice controller with twin frame stores and an integral vision mixer/combiner. Called the P148-3, the system allows manipulated images and their relative keys to be combined to form composite pictures with internally generated background colour matt or external background or foreground sources and keys. The flexible system offers a touch-screen interface with access to the many functions though they can also be controlled by a computer through an RS422/432 interface. It combines wipes and mixes with the ability to build composite pictures from up to five layers. Three internal video sources are provided; a background matt, a caption generator which can also be used as another background and a picture black.

Clever software allows the system to provide complex functions despite the fact that has only two effects buses. The controller itself can be reconfigured by software to match different equipment combinations and it can be controlled through screen menus. All software; programs or control configurations can be downloaded from disc.
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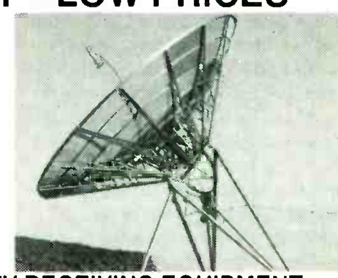

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TELEVISION BROADCAST

Encrypting tv

CSP International have been awarded a Home Office contract to study how "subscription television", as envisaged by the Peacock Committee, could be implemented in the UK, not only for d.b.s. services but also for the BBC and possibly for ITV services. This has come at a time when techniques for encrypting television signals have become technically possible but when the practicalities of this method of financing broadcasting, particularly when introduced on to existing services not requiring any special decoder, remain uncertain. In the United States the introduction of scrambling by Home Box Office early this year decimated the sale of C-band TVROs, although recently there has been some revival of sales. The special decoders add significantly to receiver costs, apart from the imposition of the subscription charges.

European broadcasters have developed sophisticated forms of "conditional access" encryption that automatically "disconnects" viewers whose subscriptions have not been paid. Both the BBC and IBA have implemented systems in respect of "Datacast" and "Subscriber User Group Services" on teletext. The Belgian French-language service RTBF have developed a patented addressable "DAVE" (digital audio visual encrypting) system based on very large-scale integration claimed to provide "absolute security" against piracy, capable of providing a credit limit for pay-tv and with an electronic lock against unauthorized use.

In a paper at the recent international IEE conference on "Secure Communication Systems", D.T. Wright and S.M. Edwardson of BBC Research described some of the problems of key management in broadcast conditional access systems. They pointed out that unlike encryption for communications, any broadcast system has to be designed to last for many years, possibly for many millions of users. The broadcaster needs to be reasonably confident that his conditional access system, specified now, will remain secure against sophisticated technological piracy throughout its many years of service. Being a one-way system there is no permanent return path to provide the administrative convenience of efficient interactive dialogue with the user as available for most encryption applications. Electronic encryption based on secure "keys" normally involved frequent change of keys. Over-air addressing involved the problem of how frequently can each viewer be individually addressed without imposing an excessive data transmission requirement.

There is also the problem, already to be seen in the USA, of different broadcasters and cable operators developing or selecting entirely different systems, increasing still further the cost to the viewer wishing to watch a number of channels.

Even where all technological problems can be solved, there remains the question of mixed "advertising – supported" and "all-subscription" channels. Would viewers, for example, pay to watch BBC News if they could watch ITN free?

No more UK cameras?

The closing of the Andover facility of Link Electronics and the concentration of its OB vehicles and systems activities in Newbury where it will share facilities with Quantel, another UEI company, must put in question the future of broadcast camera production in the UK. There seems little or no likelihood of production of the Link 130 camera being transferred to Newbury, even if the firm remains a camera supplier.

The Link 130 has recently been the only camera designed and manufactured in the UK, with both EMI and more recently Marconi withdrawing from this market. Similarly, in the United States, RCA have moved out of the broadcast camera market.

In Europe, Philips and Bosch have joined forces as BTS (Broadcast Television Services) and Thomson-CSF with the support of the French Government remain active in this field. But Japanese electronics and lenses are now dominant in most parts of the world.

Closing of Link's Andover plant has led to a number of redundancies among highly specialized engineers.

IBC 86 showed that similar pressures are mounting in the field of video tape recorders. With Marconi no longer manufacturing, there is no UK production. RCA are similarly out. Pioneering Ampex are still a major force but the new M.II machines using ½in metal-particle tape demonstrated by Panasonic and JVC threaten to open a new format battle. Unlike other ½in tape formats, the M.II prototypes appear to provide a performance that makes them serious contenders not just for electronic news gathering but for all applications including studio and post-production use. NBC have opted for M.II machines for their new New York City production centre. But with relatively new 1in format C machines in most studios an immediate swing to M.II is unlikely, though Sony must be worried at the threat to their very successful ½in Betacam and their new Betacam-SP.

No u.h.f. tv in USA?

Whereas the UK has, as a result of the interim (1982) Merriman Report, closed down all v.h.f. television broadcasting and concentrated on u.h.f. (Bands 4 & 5), possibly extending later to 12 GHz d.b.s., the North Americans are seriously thinking of closing all u.h.f. broadcast services. Increasingly, u.h.f. channels have been utilized mainly by the public service and ethnic channels (e.g. Spanish language) and it is claimed these could be accommodated on cable.

For more than 25 years u.h.f. broadcasting has been regarded as very much a second best. The FCC forced setmakers to provide u.h.f. tuners, but many of these had no r.f. amplifier and tend to be noisy by European standards. More recently the FCC are opening u.h.f. to land-mobile services on a shared basis and the possibility of mutual interference appears to be one reason for the possible closing of u.h.f.

It is perhaps ironical that another drawback, the power costs of running high-power u.h.f. transmitters (often 110kW output, compared to the highest power UK Crystal Palace station with two 40kW units per channel) could be much reduced by use of higher efficiency klystrons or the new "klystrode" (half klystron, half tetrode) device which can operate in Class B, and which is now being offered is vision transmitters of up to 60kW output with a figure of merit better than 123% (figure of merit equals peak sync. power output divided by average picture power input, including sync. pulses). Gain at 23dB is less than achievable with a four-cavity klystron but it is claimed that lifetime, despite the incorporation of a grid wire, should approach that of a klystron. Four-cavity klystrons now have greatly improved conversion efficiency by switching the beam power and by the use of annular beam control. Efficiencies of 60 to 65% can be achieved operationally and with careful control of pre-correction this could be raised to over 80%.

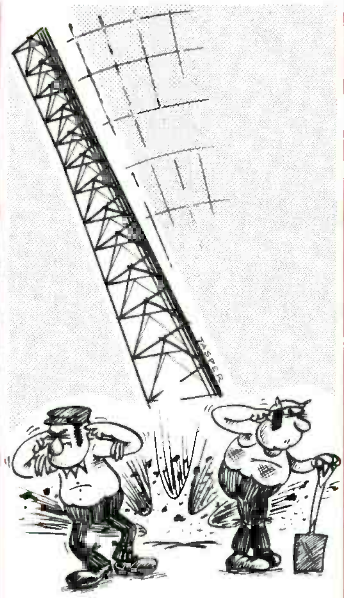
RADIO BROADCAST

Protecting masts

The triangular steel masts widely used for broadcasting and communications are vulnerable to corrosion and to lightning strikes, with the major potential hazard from indirect lightning strikes being the possibility of damage to any solid-state equipment connected to the antenna system. Despite the claims of solid-state transmitter manufacturers that their equipment is fully protected this in practice depends, particularly in the case of medium-wave equipment, on the installation being adequately earthed, both in respect of the antenna system and the power-supply system. An indication of the extent to which this may need to be taken is underlined in a recent 127-page publication of the European Broadcasting Union: "The protection of broadcasting installations against damage by lightning" compiled by specialist engineers of RAI (Italy), IBA (UK), Deutsche Bundepost (FRG) and Osterreichischer Rundfunk (Austria).

One problem is that v.h.f. and u.h.f. transmitting stations are often built on hills or mountains where the earth conductivity is very poor and various systems of "earthing improvement" are necessary. This may include increasing soil conductivity by injecting highly-conducting solutions in order to reduce the contact and bedding resistance of the earth electrodes. The authors point out that, formerly, use was made of saline solutions, but these contributed to corrosion. More recently hygroscopic emulsions have been developed; in order to permit the emulsion to penetrate the rock, blasting may be necessary. Emulsion injection can result in lower earthing resistance, independent of fluctuations in air temperature and humidity and provides a useful degree of corrosion prevention.

The *ABU Technical Review* (September, 1986) includes a report from China on metallic corrosion in medium-wave antenna masts. There are over 550 m.f. and h.f. transmitting stations in mainland China. Serious corrosion has been found a problem at a site close to an



industrial city in south-eastern China, where there are relatively lightweight steel triangular masts 106.5m and 147m high. The segments most affected were at altitudes of about 65 to 108m. Microanalysis of the corroded sections showed an abundance of sulphur which was deemed to come from sulphur dioxide pollution from local power stations and factories. Harmful smog from many chimney stacks does not diffuse quickly under low wind speeds and high humidity.

The Chinese broadcast engineers have concluded that careful attention needs to be paid to question of air pollution when choosing sites and that metal-protection needs to be considered in relation to environmental conditions. Techniques such as surfact blasting, hot spraying immediately with an Al-Mg alloy coating with a sealed layer painted over the coating are recommended in polluted areas. In less polluted environments masts can be sprayed with a non-metallic paint on the steel base after blasting. The Chinese plan in future to use aluminized coating and steel base combined metallurgically, with resulting stronger bond strength. The aluminized coating with an inside layer of ferroluminium and an outer layer of high concentration aluminium will, it is claimed, be more resistant to atmospheric corrosion.

Lithium 1.3Ah batteries

Duracell alkaline battery advertising claims, not met by many of the large number of 'export' batteries (grey imports?) being sold in UK shops, have again been under attack, despite the insistence that the advertisements now make it clear that alkaline batteries compare best with the cheaper carbon zinc units only when delivering substantial currents over long periods.

Meanwhile, in the USA, H. Taylor of the Duracell Research Centre has been describing new "high-power consumer-replaceable lithium manganese dioxide batteries" (*IEEE Trans, C-E,* No 3, August, 1986, pages 694 to 699). This notes that while the first Li-MnO_2 cells were small, coin shaped units for watches and calculators, high-power 6V batteries of up to 1.3Ah capacity were introduced on the American market last year. Lithium batteries present a potential explosion hazard and in these cells three safety mechanisms have been incorporated: a positive temperature-coefficient (p.t.c.) device which would limit output current in the event of a short-circuit (without such protection short-circuit current could be about 10A); a vent; and a separator which is heat sensitive and would close to prevent internal flow of ions between anode and cathode. The batteries are claimed to have a shelf life of five years, to deliver energy at temperatures down to −20°C and to outperform commercial aqueous and lithium systems.

SAFT America Inc have opted for lithium copper oxide (Li CuO) and lithium copper oxyphosphate batteries as consumer products. Both, like Li-MnO, are solid cathode systems regarded as essential to meet safety requirements. Lithium copper cells offer the same 1.5V nominal voltage as alkaline and carbon zinc cells but with greatly extended shelf life. In the small AA size they offer about three times more energy capacity than carbon zinc cells, though they are suitable only for current drains of less than about 50 mA and about 1A or less for the larger D cells. Some Li-CuO cells have been on discharge for more than 13 years and are typically used for such long-term applications as memory back-up.

Spectrum shake-up?

As forecast in *E&WW*, December, 1985 ("Selling the spectrum?" page 9) the DTI are likely to recommend to Government that radical changes should be made in the way that the radio frequency spectrum used for broadcasting and land mobile communications should be managed in future. The proposals will reflect the keynote speech made by A.J. Nieduszynski of DTI RRD at last year's IERE Land Mobile Radio Conference in which he stated that "a piece of spectrum carries a potential price tag." In effect, the proposals, some of which would require legislation, could be seen as a form of privatization of the spectrum with two new private companies formed to administer on a day-to-day basis the assignment of radio frequencies to users. One company or organization would look after broadcast frequencies; the second would be concerned with communications.

It is possible that initial assignments would be auctioned or awarded to those who could best use frequencies for the rapid commercial development of commercially-profitable services. They would then be free to lease frequencies, possibly on an established fixed tariff, to individual companies. In effect it seems possible that broadcasting authorities, such as the BBC and IBA and possibly the mooted Radio Authority, would largely be responsible for administering their own frequencies.

For services such as amateur radio or c.b. radio, where blocks of frequencies rather than specific channels are made available to individuals, it seems unlikely that these services would come under the spectrum management companies, and no proposals have apparently been formulated. Defence services would largely administer their own frequencies, though this raises questions as to how much of the radio spectrum would be assigned for defence and how this could be varied.

Working both ways

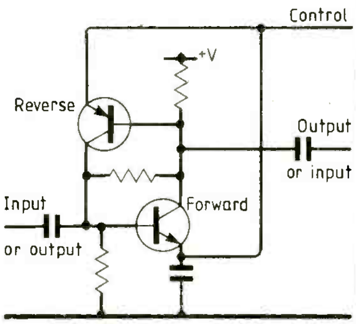
For many years, h.f. transmitters and receivers were built as separate units. The wartime development of hand-transportable suitcase stations, initially for covert radio links, retained this separation although usually sharing the same power supply unit. An exception was the Russian Belka M-2 equipment in which the audio-output valve of the receiver was switched to become a crystal-controlled power oscillator.

The era of the true h.f. transceiver really dawned with the development of mobile s.s.b. radiotelephones, pioneered largely by Collins Radio in the late 1950s, when it was found that costs and size could be usefully reduced by employing the same s.s.b. mechanical or crystal filter for both s.s.b. generation and receiver selectivity.

More recently further economies and size reduction have resulted from the use of bilateral (i.e. reversible) mixers and amplying stages.

In 1974, Redifon (now Rediffusion Radio Systems Ltd), in association with Dr R.C.V. Macario of the University of Swansea, used a reversible circuit board based on two Siemens TCA440 and a Plessey SL621. This was used as the basis of the Safari 100-watt s.s.b. radio telephone, believed to have been the world's first dashboard-mounted h.f. radiophone.

More recently, D. Holman of Plessey Electronics Systems Research has shown how the battery-operated Plessey Model PTR5300 10W/1W manpack set has been considerably simplified, to the extent of eliminating eight relay and four amplifying operations by the substitution of reversible amplifiers in place of unidirectional stages. Figure 1(a) shows the unit before modification: Fig. 1(b) with reversible amplifiers. Figure 2 shows how the direction of the amplifiers is reversed by means of a switching control line.



Self-tuning antenna system for h.f.

The use of frequency-hopping techniques on h.f. has led to renewed interest in broad-band and self-tuning antenna systems. Rohde & Schwarz GmbH, for example, have introduced a self-tuning dipole with an overall element length of about 10m, using the established technique of two vee-shaped elements forming each half of the doublet and with an adaptive tuning/matching network immediately beneath the feedpoint, for which there is no requirement to provide control signals.

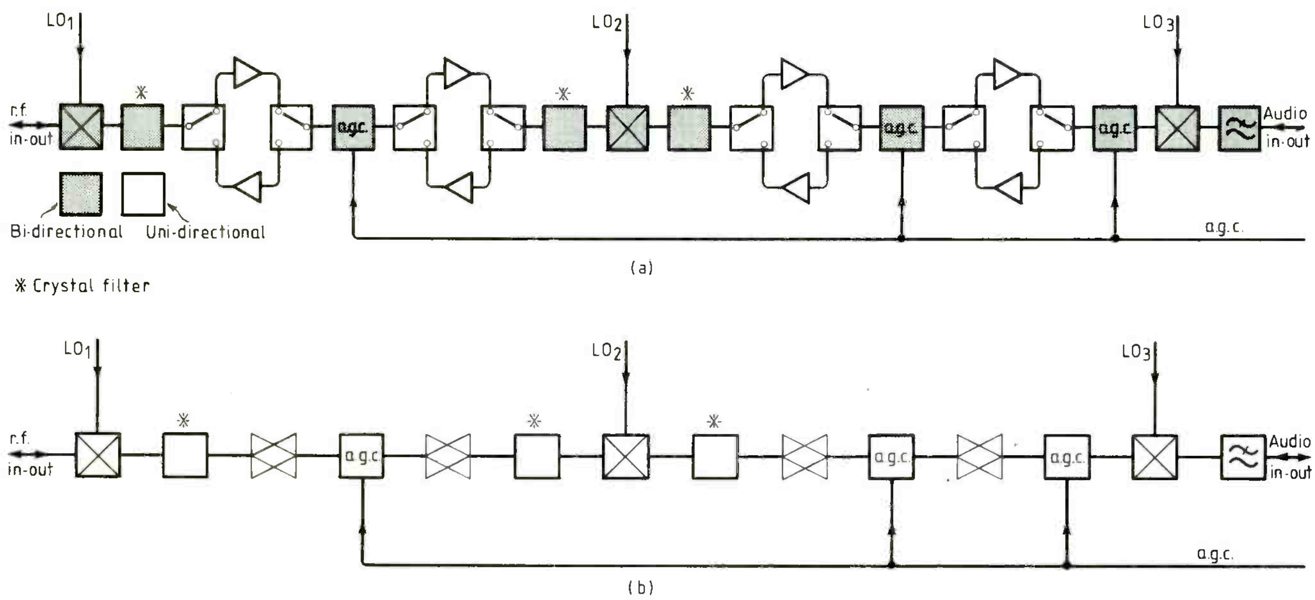
Automatic, adaptive tuning is independent of variable conditions in the near-field, including changes of soil conductivity. The non-volatile tuning memory updates with each correction, reducing the setting time for a subsequent change of frequency to about 60 milli-seconds, permitting rapid change of frequency though presumably not fast enough for military frequency-hopping. It is rated for transmitters up to 1kW.

Mould nears completion

Due for completion in 1987, the Home Defence "Mould" v.h.f./u.h.f. area-coverage radio system has been designed to provide command communications between mobile and static units within ten regional systems. Based on the Pye Pegasus v.h.f. equipment with Selcall selective calling and, for Phase 2, the Pye synthesized FM914, it provides f.m. voice communication between district headquarters, G.O.C. Rovers, subordinate headquarters and Regular and Territorial Army battalions.

Conceived in the early 1970s, it involved £7-million phase 1 and £3-million phase 2 enhancements – Mould uses single-channel hill-top-site (h.t.s.) repeaters linked by v.h.f. or u.h.f. point-to-point links with a maximum of seven hops between users. Future possibilities include the use of the h.t.s. stations to provide also ground-to-air communications. Inter-regional working, not currently possible, is leading to the development of an interface with the British Telecom network.

The phase 1 Pegasus units are 18-channel (12.5kHz) radios operating between 68 and 88 MHz. The link equipments use 140 to 150 MHz (25kHz) and 420 to 450 MHz (25kHz). When complete there will be 90 discrete nets using 150 h.t.s. repeaters and 200 links using 227 different v.h.f./u.h.f. channels. A few isolated complaints of interference to radio amateurs using 430 to 440 MHz as secondary users have been received. Maintenance and repair of the h.t.s. sites has been in the hands of the four T.A. Home Defence Signal Regiments of 2 Signal Brigade (though these may be replaced by contract maintenance). User radios are maintained by R.E.M.E. A detailed description of "Mould" appears in the Summer 1986 issue of *The Journal of the Royal Signals Institution.*



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AA119	0.10
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AAZ13	0.30
AAZ15	0.30
AAZ17	0.30
AC107	0.55
AC125	0.35
AC126	0.35
AC127	0.40
AC128	0.35
AC141	0.35
AC141K	0.45
AC142	0.40
AC142K	0.45
AC176	0.35
AC187	0.35
AC188	0.37
ACY17	2.25
ACY18	1.55
ACY19	1.80
ACY20	1.50
ACY21	1.55
ACY39	4.00
AD149	1.00
AD161	0.50
AD162	0.60
ADZ11	12.50
ADZ12	12.50
AF106	0.60
AF14	3.50
AF115	3.50
AF116	3.50
AF117	4.00
AF139	0.55
AF186	0.75
AF239	0.65
AFZ11	3.75
AFZ12	5.00
ASY26	1.40
ASY27	1.00
ASZ15	2.20

ASZ16	2.00
ASZ17	1.60
ASZ20	4.50
ASZ21	4.75
AUY10	3.50
BA145	0.13
BA148	0.15
BA154	0.06
BA155	0.11
BA156	0.06
BAW62	0.05
BAX13	0.05
BAX16	0.06
BC107	0.12
BC108	0.12
BC109	0.14
BC113	0.12
BC114	0.12
BC115	0.12
BC116	0.19
BC117	0.24
BC118	0.30
BC125	0.25
BC126	0.25
BC135	0.18
BC136	0.18
BC137	0.22
BC147	0.12
BC148	0.12
BC149	0.12
BC157	0.12
BC158	0.13
BC159	0.12
BC167	0.10
BC170	0.09
BC171	0.11
BC172	0.09
BC173	0.09
BC177	0.15
BC178	0.28
BC179	0.15

BC182	0.11
BC183	0.09
BC184	0.11
BC212	0.11
BC213	0.11
BC214	0.11
BC237	0.09
BC238	0.09
BC301	0.36
BC303	0.36
BC307	0.09
BC308	0.09
BC327	0.09
BC328	0.09
BC337	0.09
BC338	0.09
BCY30	3.75
BCY31	3.75
BCY32	3.75
BCY33	2.50
BCY34	2.50
BCY39	3.60
BCY40	3.00
BCY42	0.32
BCY43	0.45
BCY58	0.25
BCY70	0.21
BCY71	0.21
BCY72	0.21
BCZ11	3.50
BD115	0.35
BD123	2.30
BD124	2.50
BD131	0.42
BD132	0.42
BD135	0.27
BD136	0.27
BD137	0.30
BD138	0.30
BD139	0.30
BD140	0.30
BD144	2.00
BD181	0.75

BD183	0.75
BD237	0.35
BD238	0.35
BDX10	0.91
BDX32	2.00
BDY10	2.40
BDY20	1.50
BDY60	1.50
BF115	0.30
BF152	0.16
BF153	0.19
BF154	0.17
BF159	0.20
BF160	0.20
BF166	0.35
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BF173	0.45
BF177	0.30
BF178	0.30
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BF181	0.25
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BF183	0.30
BF184	0.30
BF185	0.30
BF194	0.15
BF195	0.15
BF196	0.15
BF197	0.15
BF200	0.33
BF224	0.20
BF241	0.20
BF244	0.35
BF257	0.30
BF258	0.30
BF259	0.30
BF336	0.30
BF337	0.30
BF338	3.00
BFS21	4.00
BFS28	2.50
BFS61	0.30

BFS98	0.30
BFW10	1.04
BFW11	1.04
BFX84	0.28
BFX85	0.28
BFX87	0.28
BFX88	0.28
BFY50	0.28
BFY51	0.28
BFY52	0.28
BFY64	0.36
BFY90	0.65
BSX19	0.27
BSX20	0.27
BSX21	0.27
BT106	1.65
BTY79 400K	3.00
BU205	1.20
BU206	1.20
BU208	2.00
BY100	0.42
BY126	0.15
BY127	0.15
BZX61	0.17
Series	
BZY88	0.10
Series	
BZY93	8.00
Series	
BZY93	0.12
Series	
BZY95	1.64
Series	
BZY96	2.00
Series	
CRS1 40	0.60
CRS3 40	0.75
CRS3 60	0.90
GEX66	0.30
GEX541	6.50
GJ3M	3.00
GM0378A	1.75
KS100A	0.45

MJE340	0.79
MJE370	0.73
MJE371	1.05
MJE520	0.75
MJ521	0.73
MJE2955	2.25
MJE3055	2.00
MPF103	0.55
MPF104	0.55
MPF105	0.55
MPSA06	0.17
MPSA56	0.17
MPSU01	1.11
MPSU06	1.33
MPSU56	1.71
NE555	0.45
NKT401	4.00
NKT403	3.50
NKT404	4.00
OA5	1.75
OA7	0.75
OA10	0.55
OA47	0.15
OA70	0.22
OA79	0.21
OA81	0.21
OA85	0.21
OA90	0.08
OA91	0.08
OA95	0.08
OA200	0.15
OA202	0.15
OA211	1.00
OAZ200	1.50
OAZ201	1.50
OAZ206	1.50
OAZ207	1.50
OC16	5.00
OC20	6.00
OC22	4.50
OC23	10.00
OC24	3.00
OC25	0.79

OC26	1.50
OC28	5.50
OC29	4.40
OC35	4.00
OC36	4.00
OC41	1.20
OC42	1.50
OC43	1.50
OC44	1.25
OC45	0.85
OC71	0.65
OC72	2.20
OC73	1.45
OC74	1.40
OC75	1.40
OC76	1.60
OC77	2.75
OC81	0.90
OC81Z	4.00
OC82	0.95
OC83	1.40
OC84	1.40
OC122	6.50
OC123	6.50
OC139	12.00
OC140	18.00
OC141	18.00
OC170	4.40
OC171	4.40
OC200	4.00
OC201	5.50
OC202	5.50
OC203	5.50
OC204	7.00
OC205	10.00
OC206	8.50
OC207	18.00
OCP71	2.50
ORP12	2.40
R2008B	1.95
R2009	2.25
R2010B	2.00
TIC44	0.48

TIC226D	1.20
TI1209	0.29
TIP29A	0.35
TIP30A	0.36
TIP31A	0.25
TIP32A	0.25
TIP33A	0.53
TIP34A	0.60
TIP41A	0.38
TIP42A	0.42
TIP110	0.10
TIP117	0.45
TIP125	0.35
TIP130	0.45
TIP131	0.45
TIP132	0.48
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TIP137	0.48
TIP140	0.85
TIP141	0.85
TIP142	0.85
TIP2955	0.60
TIP2955T	0.45
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ZS140	0.25
ZS170	0.21
ZS178	0.54
ZS272	0.23
ZS278	0.57
ZTX107	0.12
ZTX108	0.12
ZTX109	0.12
ZTX300	0.13
ZTX301	0.14
ZTX302	0.14
ZTX303	0.14
ZTX304	0.14
ZTX311	0.13
ZTX314	0.25
ZTX500	0.14
ZTX501	0.14
ZTX502	0.14

ZTX503	0.14
ZTX504	0.20
ZTX531	0.20
ZTX550	0.25
IN914	0.03
IN916	0.03
IN4001	0.04
IN4002	0.04
IN4003	0.04
IN4004	0.04
IN4005	0.04
IN4006	0.04
IN4007	0.05
IN4009	0.06
IN4148	0.03
IN5400	0.10
IN5401	0.11
IS44	0.04
IS290	0.10
IS921	0.12
2G301	1.00
2G302	1.20
2G306	1.50
2N404	1.50
2N696	0.30
2N697	0.36
2N698	0.38
2N705	2.50
2N706	0.20
2N708	0.22
2N930	0.25
2N1131	0.35
2N1132	0.35
2N1302	1.80
2N1303	0.90
2N1304	3.00
2N1305	1.00
2N1306	3.00
2N1307	1.20
2N1308	4.00
2N1309	1.50
2N1613	0.30
2N1671	5.00

2N1893	0.30
2N2147	8.00
2N2148	2.75
2N2218	0.32
2N2219	0.32
2N2220	0.22
2N2221	0.22
2N2222	0.20
2N2223	7.50
2N2368	0.23
2N2369	0.23
2N2384	0.24
2N2646	0.75
2N2904	0.30
2N2904	0.30
2N2905	0.30
2N2906	0.22
2N2907	0.22
2N2924	0.12
2N2925	0.22
2N2926	0.12
2N3053	0.30
2N3054	0.55
2N3055	0.70
2N3440	0.60
2N3441	0.75
2N3442	1.00
2N3641	5.00
2N3702	0.11
2N3703	0.11
2N3704	0.11
2N3705	0.11
2N3706	0.11
2N3707	0.11
2N3708	0.11
2N3709	0.11
2N3710	0.11
2N3711	0.10
2N3771	1.20
2N3772	1.20
2N3773	1.60
2N3819	0.50
2N3820	0.60

2N3823	0.80
2N3866	1.00
2N3904	0.10
2N3905	0.10
2N3906	0.10
2N405X	0.12
2N4059	0.20
2N4060	0.12
2N4061	0.12
2N4062	0.15
2N4124	0.13
2N4126	0.13
2N4248	0.25
2N4288	0.15
2N4289	0.12
2N4400	0.12
2N4401	0.12
2N4402	0.12
2N5457	0.45
2N5458	0.40
2N5459	0.40
2S017	16.00
2S019	25.00
2S024	35.00
2S025	35.00
2S026	40.00
2S103	2.50
2S302	5.50
2S303	5.50
2S322	5.00
2S325	4.00
2S701	12.50
2S745A	1.75
2S746A	1.75

VALVES

A1834	9.00
A2087	13.50
A2134	17.50
A2293	16.00
A2426	35.00
A2521	25.00
A2900	15.00
A3343	45.00
AZ31	2.75
AZ41	2.60
BK448	114.90
BK484	155.35
BS90	58.00
BS810	60.00
BT5	58.95
BT17	185.00
B119	44.05
B129	349.15
B169	354.80
B195	129.90
CBL31	4.00
CL33	4.00
CY31	3.00
C1K	20.00
C3A	22.00
C3JA	22.00
DA41	25.00
DA42	18.70
DAF91	1.75
DAF96	1.75
DET22	35.00
DET24	49.00
DF91	1.75
DF96	1.75
DK91	1.75
DK92	2.00
DK96	1.75
DL92	2.00
DL94	1.75
DL96	1.75
DLS10	14.00
DLS15	12.50
DLS16	12.50
DLS19	12.50
DM70	2.00
DM71	2.00
DM160	4.75
DY87	1.50
DY802	1.50
E55L	50.00
E80CC	15.00
E80CF	11.27
E80F	14.19
E80L	13.73
E81CC	8.00
E81L	13.27
E82CC	8.10
E83CC	8.40
E86C	8.25
E88C	8.25
E88C	10.33
E90CC	9.47
E90F	9.90
E91H	6.25
E92CC	8.75
E99F	9.10
E130L	18.50

E180CC	10.50
E180F	12.05
E182CC	13.25
E186F	11.50
E188CC	8.91
E280F	22.51
E283CC	12.00
E288CC	17.50
W810F	35.48
EA52	32.25
EA76	2.50
EABC80	1.25
EAC91	3.50
EAF42	2.50
EAF801	2.00
EB41	4.00
EB91	1.50
EBC33	2.50
EBC41	2.50
EBC81	1.50
EBC90	1.25
EBF80	1.50
EBF83	1.75
EBF89	1.50
EBL31	10.00
EC90	1.25
EC91	8.00
EC92	1.75
EC175	462.00
ECC33	4.50
ECC35	4.50
ECC40	5.50
ECC81	1.75
ECC82	1.75
ECC83	1.75
ECC84	1.75
ECC85	1.75
ECC86	2.50
ECC88	3.50
ECC89	2.00
ECC91	8.93
ECC189	2.10
ECC807	1.75
ECC808	3.00
ECF80	1.50
ECF82	1.50
ECF86	2.50
ECH35	3.00
ECH42	3.50
ECH81	3.00
ECH83	2.50
ECH84	2.50
ECL80	1.50
ECL81	1.75
ECL82	1.50
ECL83	3.00
ECL84	1.50
ECL85	1.50
ECL86	1.75
EF37A	5.00
EF39	2.75
EF40	5.00
EF41	3.50
EF42	4.50
EF50	2.50
EF54	5.00
EF55	3.50
EF80	1.75
EF83	4.00

EF85	1.75
EF86	3.50
EF89	2.50
EF91	2.95
EF92	6.37
EF93	1.50
EF94	2.50
EF95	5.99
EF98	2.00
EF183	2.00
EF184	2.00
EF804S	12.00
EF805S	15.00
EH90	1.75
EK90	1.50
EL32	2.50
EL33	4.00
EL34MUL	4.00
EL36	2.50
EL41	2.80
EL42	2.50
EL60	18.50
EL81	5.25
EL83	6.00
EL84	2.25
EL86	2.75
EL90	3.25
EL91	7.39
EL95	2.00
EL156	30.00
EL360	18.50
EL500	3.00
EL509	10.00
EL821	13.00
EL822	13.97
ELL80	25.00
EM34	8.00
EM80	2.50
EM81	2.50
EM84	2.00
EM85	2.75
EM87	2.50
EN32	25.00
EN91	6.50
EN92	6.96
EY51	2.75
EY81	2.50
EY83	2.50
EY84	9.24
EY86	1.75
EY88	1.75
EY500A	3.00
EY802	1.75
EZ35	1.75
EZ40	2.50
EZ41	2.50
EZ80	1.50
EZ81	1.50
EZ90	3.00
FW4-500	3.50
FW4-800	3.50
GL371K	35.00
G551K	12.00
G180.2M	17.50
G240.2D	12.00
G400.1K	17.50
GN4	9.00
GN4A	9.00
GN4A	9.00

GS16	16.00
GT1C	25.00
GU50	20.00
GU51	20.00
GXU1	15.35
GXU2	30.00
GXU3	25.40
GXU4	44.50
GXU50	20.00
GY501	3.00
GZ32	4.00
GZ33	4.75
GZ34	4.00
GZ37	4.95
KT61	5.00
K166	15.00
K177 Gold Lion	12.00
KT88 Gold Lion	20.00
KTW61	2.50
KTW62	2.50
KTW63	2.50
M8079	12.34
M8080	8.25
M8081	9.82
M8082	9.69
M8083	10.25
M8091	10.43
M8096	6.80
M8097	8.10
M8098	8.15
M8099	8.00
M8100	10.30
M8136	11.75
M8137	12.25
M8140	6.00
M8141	6.50
M8142	8.75
M9144	7.50
M8149	6.50
M8161	9.35
M8162	11.75
M8163	8.25
M8190	5.00
M8195	10.85
M8196	7.50
M8204	7.05
M8212	11.37
M8223	6.00
M8224	6.30
M8225	4.50
M8248	14.03
MD2901	115.00
MU14	2.50
MX119	55.00
MX123	86.00
MX145	61.50
MX151	18.30
MX152	150.00
MX161	175.00
MX163	19.50
MX164	26.40
MX166	147.00
MX168	57.00
N78	15.00
OA2	3.25
OA3	2.50
OA4	6.00

OB3	2.50
OC2	4.55
OC3	2.50
OD3	2.50
OZ4	3.50
PC86	2.50
PC88	2.50
PC95	1.75
PC97	1.75
PC900	1.75
PCC84	1.50
PCC85	1.50
PCC88	2.00
PCC89	1.75
PCC189	2.50
PCC805	1.60
PCC806	1.60
PCF82	2.00
PCF80	2.00
PCF82	1.50
PCF86	2.50
PCF87	2.00
PCF200	3.25
PCF201	3.25
PCF801	2.50
PCF802	2.50
PCF805	1.70
PCF806	1.70
PCF808	1.70
PCL82	2.00
PCL83	3.00
PCL84	2.00
PCL85	2.50
PCL86	2.50
PCL805/85	2.50
PD500	6.00
PE06-40N	45.00
PFL200	2.50
PL36	2.50
PL81	1.75
PL81A	2.00
PL82	1.50
PL83	2.50
PL84	2.00
PL504	2.50
PL508	5.50
PL509	6.00
PL519	6.00
PL801	1.50
PL802	6.00
PY33	2.50
PY81	1.50
PY82	1.50
PY83	1.25
PY88	2.00
PY500A	4.00
PY800	1.50
PY801	1.50
QE451	82.50
QQV02-6	38.00
QQV03-10	26.25
QQV03-20A	48.38
QQV06-40A	46.00
QQV07-50	76.65
QQZ06-40A	62.20

QU37	12.50
QV03-12	6.80
QV04-7	3.50
QV08-100	197.40
QY3-65	63.24
QY3-125	78.48
QY4-250	74.00
QY4-400	87.20
QY5-500	208.00
QY5-3000A	566.80
QZ06-20	46.00
R10	6.00
R17	3.00
R18	3.00
R19	9.24
R20	2.50
RG3-1250	59.50
RG3-250A	32.68
RG3-1250	59.00
RG4-1250	61.60
RG4-3000	99.45
RR3-250	40.00
RR3-1250	45.75
SHE12	65.00
S130	6.00
S130P	6.00
STV280-40	14.00
STV280-80	21.00
SU41	5.00
SU42	10.00
TD03-10	35.00
TD03-10F	35.00
TT15	50.00
TT21	37.50
TT22	37.50
TT100	60.00
TY2-125	78.75
TY4-400	88.20
TY4-500	124.26
TY5-500	272.50
TY6-800	231.00
TY6-5000A	632.20
TY6-5000B	395.00
TY6-5000W	523.00
TY7-6000A	632.00
TY7-6000W	579.00
TZ40	25.00
U18.20	3.50
U19	13.75
U25	2.50
U26	2.50
U37	12.00
UABC80	1.25
UAF42	2.50
UB41	3.00
UBC41	2.25
UBF89	1.50
UCC84	1.75
UCC85	1.85
UFC80	2.00
UCH42	2.50
UCH81	2.50

UCL82	1.75
UCL83	2.75
UF41	2.00
UF42	2.10
UF80	1.75
UF85	1.75
UF89	2.00
UL41	5.00
UL84	1.75
UM80	2.00
UY41	2.25
UY81	2.25
VLS631	15.00
XG1-2500	100.00
XG5-500	30.00
XG2-6400	185.00
XR1-1600A	53.75
XR1-3200	110.00
XR1-3200A	
XR1-6400	165.00
YD1120	395.00
YD1240	588.60
Z803U	25.00
Z259	25.00
ZM1001	8.00
ZM1020	9.00
ZM1020	9.00
ZM1022	9.00
ZM1023	9.00
ZM1040	19.36
ZM1041	16.66
ZM1042	17.77
IB3GT	3.00
IB24	25.00
IB35A	48.00
IB63	64.00
IR5	1.75
IS5	1.75
IT4	1.75
2AS15	11.50
2C39A	60.00
2C43	70.00
2D21	3.25
2E26	8.25
2J4Z	98.00
2J55	245.00
2J70A	383.00
2J70B	336.00
2K25	125.00
3400Z	115.00
3500Z	100.00
3A5	3.00
3B24	11.00
3B28	15.35
3B29	20.05
3B240M	17.50
3B241M	17.50
3C23	25.00
3C24	12.00
3CX100A	47.00
3E29	45.00
3S4	2.00
3V4	1.75
4-65A	60.00
4-125A	60.00

4-250A	80.00
4-400A	87.00
4B32	20.00
4C35	120.00
4CX250B	58.00
4CX350A	105.00
4X150A	60.00
4X150D	56.00
5B254M	35.00
5B255M	35.00
5C22	160.00
5J180E	2500.00
5R4GY	5.50
5U4G	3.00
5U4GB	2.50
5V4G	2.50
5Y3GT	2.50
5Z3	4.00
5Z4G	2.50
5Z4GT	2.50
6-30L2	1.75
6AB4	1.75
6AB7	3.00
6AC7	3.00
6AF4A	4.25
6AG7	3.00
6AH6	5.00
6AK5	5.99
6AK6	2.50
6AL5	1.50
6AM4	4.00
6AM5	9.69
6AM6	6.02
6AN5	4.75
6AN8A	3.50
2AQ5	3.25
6AS6	8.66
6AS7G	8.75
6AT6	1.25
6AU5GT	5.00
6AU6	2.50
6AV5GA	4.50
6AV6	1.50
6AX5GT	3.00
6B7	3.25
6B8	3.25
6BA6	1.50
6BA7	5.00
6BA8A	4.00
6BC4	4.00
6BR6	1.50
6BH6	2.50
6BJ6	2.25
6BK4	4.50
6BL6	125.00
6BL7GT	4.50
6BM6	115.00
6BN6	2.00
6BQ7A	3.50
6BR7	6.00
6BT8A	3.50
6BS7	6.00
6BW6	6.00
6BW7	1.50
6BX7GT	5.00
6BZ6	2.75
6C4	1.25
6CB6A	2.50
6CD6GA	5.00

6CG7	2.50
6CH6	13.00
6CL	63.75
6CW4	8.00
6D2	1.50
6DK6	3.00
6DQ6B	4.75
6EA8	3.00
6EB8	2.50
6EW6	2.25
6F6	3.00
6F23	1.60
6F28	1.60
6F33	33.50
6H1	14.00
6H3N	2.75
6H6	3.00
6J4	5.50
6J6	8.93
6J7	4.75
6JE6	7.50
6K6GT	2.75
6K7	3.00
6K8	3.00
6KD6	8.00
6L6G	5.00
6I6GA	3.50
6L6GC	5.75
6L6GT	3.00
6L7	2.50
6N2P	2.50
6N3P	2.50
6N7	3.00
6P225	4.00
6Q7	3.75
6K7	3.25
6RHH8 6KN8	10.00
6SA7	3.00
6SC7	2.75
6SF7	2.50
6SH7	3.00
6SJ7	3.25
6SK7	3.50
6SL7GT	3.00
6SN7GT	3.00
6SQ7	3.40
6SR7	4.00
6SS7	2.75
6U5G	3.50
6U8A	2.25
6V6GT	4.25
6X4	3.00
6X5GT	1.75
7B7	2.50
7C3	4.00
7C6	2.50
7H7	4.00
7R7	4.25
7S7	3.50
7Y4	2.25
7Z4	2.00
12AH8	5.00
12AT6	1.50
12AT7	1.75
12AU6	2.50
12AU7	1.75
12AV6	2.50

12AW7	3.50
12AX7	1.75
12AY7A	4.00
12B4A	3.50
12BA6	2.50
12BE6	2.50
12BH7	2.75
12BY7	3.00
12E1 TT	28.00
12E14	65.00
12E1	20.00
13E1	170.00
19H5	47.50
24B9	67.25
30C15	2.00
30C17	2.00
30C18	2.00
30F5	1.60
30FL1.2	1.38
30FL12	1.80
30FL14	2.00
30L1	1.50
30L15	2.00
30L17	2.00
30P4	2.50
30P19	2.50
30PL1	3.00
30PL14	1.80
30PL15	1.80
35W4	1.00
50C4	1.50
75B1	6.05
75C1	4.50
85A1	7.50
85A2	6.45
90AG	20.00
90AV	20.00
90C1	6.00
90CG	14.54
90CV	15.45
92AG	20.00
92AV	20.00
95A1	8.45
150BA	6.50
150B3	8.35
150C2	3.25
150C4	6.00
211	35.00
723AB	125.00
803	25.00
805	45.00
807	3.75
811A	18.33
812A	43.00
813 valve	65.00
833A	193.16
866A	35.00
872A	20.00
922	6.00
931A	18.50
1624	4.00
1625	3.50
2050	7.50
4212E	300.00
4212H	300.00
5544	110.00
5545	150.00
5551A	120.00

5552A	155.35
5642	9.00
5654	10.30
5651	4.45
5670	4.50
5675	28.00
5687	6.00
5696	4.50
5718	7.50
5725	5.50
5726	11.37
5727	7.05
5749	2.50
5751	4.00
5763	4.50
5814A	4.00
5840	4.00
5842	12.00
5876A	31.50
5879	5.00
5886	17.50
5963	2.50
5965	3.50
6005	2.25
6021	4.50
6057	12.25
6058	12.34
6059	6.00
6061	6.00
6063	3.75
6064	10.25
6067	11.75
6072	6.00
6080	14.00
6097A	235.00
6097B	200.00
6146A	12.00
6146B	12.00
6159B	19.00
6189	9.50
6201	11.40
6442	20.00
6550	8.00
6883B	12.50
6973	7.50
7025	3.00
7027A	8.00
7551	6.25
7586	15.00
7587	23.00
7609	56.00
7868	6.00
7895	12.00
8068	16.50
8136	2.50
8417	6.00
18042	11.53
18045	10.49
18046	11.53

Tested Ex-Equipment 4CX250B 8.50
CV Devices
Large stocks
Prices on application

BASES

B7G Unskirted	0.40
B7G Skirted	0.50
B9A Unskirted	0.40
B9A Skirted	0.50
B9D	0.55
Int Octal	0.40
Loctal	0.55
Nuvistor base	2.00
Valve screening can all sizes	0.40

CRTs

2AP1	8.50
2BP1	9.00
3BP1	20.00
3DP1	5.00
3EG1	10.00
3FP7	6.00
3GP1	6.00
3JP1	8.00
3JP2	8.00
3JP7	10.00
3KP1	15.00
3RP1	35.00
3WP1	20.00
5ADP1	55.00
6CP1	10.00

5CP1A	40.00
5P15A	15.00
5UP7	25.00
DG7-5	63.32
DG7-31	58.07
DG7-32	58.07
DG7-36	65.00
DH3-91	56.83
DH7-11	113.12
VCR138	12.00
VCR138A	12.50
VCR139A	8.00
VCR517B	10.00
VCR517C	10.00

CRT sockets
Prices on application

I/C sockets
Texas
low profile

8 pin	10p
14 pin	10p
16 pin	10p

INTEGRATED CIRCUITS

7400	0.16
7400	0.35
7401	0.36
6402	0.36
7403	0.36
7404	0.42
7405	0.42
7406	0.48
7407	0.55
7408	0.36
7409	0.36
7410	0.36
7411	0.40
7312	0.42
7413	0.36

7416	0.48
7417	0.48
7420	0.48
7422	0.36
7423	0.36
7424	0.36
7427	0.36
7428	0.36
7430	0.36
7432	0.36
7433	0.55
7437	0.36
7438	0.36
7439	0.36
7440	0.36

7441	0.48
7442	1.25
7450	0.30
7451	0.30
7453	0.30
7454	0.30
7460	0.30
7470	0.48
7472	0.30
7473	0.48
7474	0.36
7475	0.65
7476	0.48
7480	0.32
7483	0.48

7484	0.72
7486	0.54
7490	0.72
7491	0.36
7492	0.54
7493	0.54
7494	0.78
7495	0.65
7496	0.60
7497	3.90
74100	0.84
74107	0.36
74109	0.54
74110	0.48
74111	0.51
74116	1.50
74118	1.20
74119	1.50

74120	0.75
74121	0.54
74122	0.70
74123	0.60
74125	0.60
74126	0.54
74128	0.55
74136	0.70
74141	0.46
74143	1.30
74145	0.72
74147	1.50
74148	1.40
74150	1.60
74151	0.36
74154	1.40
74155	0.60
74156	0.48

74159	1.75
74170	1.20
74172	4.00
74173	0.72
74174	0.60
74175	1.00
74176	1.00
74180	1.48
74190	1.20
74191	1.20
74192	1.10
74193	0.60
74194	1.10
74195	0.72
74196	1.00
74197	1.00
74198	2.20
74199	2.20

TAA570	1.75
TAA630S	1.75
TAA700	3.00
TBA480Q	1.50
TBA520Q	1.50
TBA530	1.50
TBA550Q	1.75
TBA560Q	1.75
TBA673	1.75
TBA700	1.50
TBA700Q	1.75
TBA750Q	1.50
TBA800	1.00
TBA920	1.75
TBA990	1.50
TCA270Q	1.00
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How linear is linear?

An algebraic method of determining non-linearity in a long-tailed pair, with an application in the evaluation of mixer performance in receivers

R. J. IRVINE

Readers may be interested in an extension of part of the theory presented by F. J. Lidgey in part 2 of his article "The tale of the long-tail pair", (*E&WW* October 1985), concerning the linear differential transconductance amplifer. The problem arises that equation (5a).

$$V_{IN}/V_T = \log_e((I_1/I_0)/(1-(I_1/I_0))) + ((I_1/I_0)-1/2)I_0R/V_T$$

expresses the input voltage V_{IN} as a function of the output current I_1, where what we would prefer is an expression for I_1 as a function of V_{IN}, in order to be able to quantify the non-linearity in the amplifier. Equation (5a) cannot be solved algebraically to give an expression in closed form for I_1 as a function of V_{IN}. However, apart from resorting to graphical or numerical methods, there remains one other option, which is to find a power series solution for the output current as a function of the input voltage.

By substituting $i=I_1-I_0/2=I_0/2-I_2$ and $I_L=I_0/2$, where I_L is the current in each of the "legs" of the linearized tail (see Fig.1), then equation (5a) simplifies to:

$$V_{IN}=(I_LR).\left(\frac{i}{I_L}\right)+V_T\log_e\left\{\frac{1+(i/I_L)}{1-(i/I_L)}\right\} \qquad (1)$$

Using the expansion

$$\log_e(1+x)=x-\frac{x^2}{2}+\frac{x^3}{3}-\frac{x^4}{4}+\ldots \quad |x|<1$$

then V_{IN} can be written as a power series in (i/I_L)

$$V_{IN}=(I_LR)\left(\frac{i}{I_L}\right)+2V_T\left\{\left(\frac{i}{I_L}\right)+\frac{1}{3}\left(\frac{i}{I_L}\right)^3+\frac{1}{5}\left(\frac{i}{I_L}\right)^5+\ldots\right\} \qquad (2)$$

It is interesting to note that no even powers of (i/I_L) appear in this series. Stated generally, the problem is this: given the power series

$$y=\sum_{r=1}^{\infty} b_r x^r \qquad (3)$$

how do we find the inverse series

$$x=\sum_{s=1}^{\infty} a_s y^s \qquad (4)$$

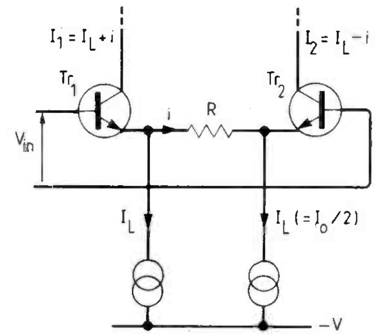

Fig.1

If the latter series exists and is convergent, then substituting (4) in (3) gives

$$y=\sum_{r=1}^{\infty} b_r\left(\sum_{s=1}^{\infty} a_s y^s\right)^r \qquad (5)$$

The right hand side of equation (5) may be expanded and, by equating powers of y on both sides of the equation, the coefficients a_s may be found in terms of the coefficients b_r. Expanding as far as the third power of y gives the following results:

$$a_1=\frac{1}{b_1} \qquad (6a)$$

$$a_2=\frac{-b_2}{b_1^3} \qquad (6b)$$

$$a_3=\frac{2b_2^2}{b_1^5}-\frac{b_3}{b_1^4} \qquad (6c)$$

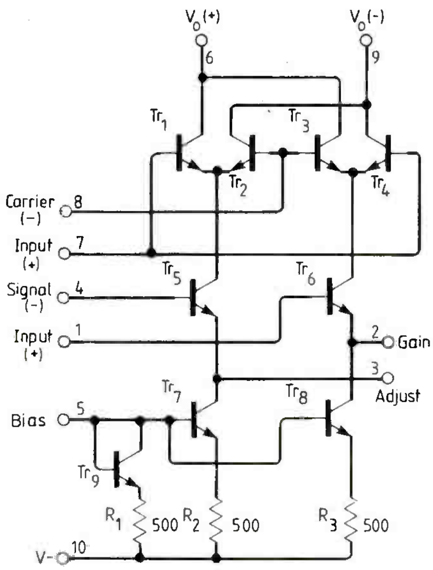

Fig.2. MC1496

Returning to the application in hand we have, by inspection of equation (2),

$$b_1=I_LR+2V_T \qquad (7a)$$

$$b_2=0 \qquad (7b)$$

$$b_3=2V_T/3 \qquad (7c)$$

Using equations (6) gives

$$a_1=1/(I_LR+2V_t) \qquad (8a)$$

$$a_2=0 \qquad (8b)$$

$$a_3=-(2V_T/3)/(I_LR+2V_T)^4 \qquad (8c)$$

so that the power series as far as the third order for (i/I_L) as a function of V_{IN} is given by

$$\left(\frac{i}{I_L}\right)=\frac{1}{(I_LR+2V_T)}.V_{IN}-\frac{(2V_T/3)}{(I_LR+2V_T)^4}.V_{IN}^3\ldots \qquad (9)$$

It can be shown that since equation (2) has no even powers of (i/I_L) then there are no even powers of V_{IN} in equation (9).

Neglecting the non-linear terms for a moment, then if $I_LR \gg 2V_T$, equation (9) reduces to

$$i=\frac{V_{IN}}{R} \qquad (10)$$

If $V_{IN} \ll I_LR+2V_T$ then the fifth order term in V_{IN} can be neglected in comparison with the third order term, so that it is the third order term which represents the most significant deviation from linearity.

Analysis of this kind is important in a number of applications: as well as forming the basis of the four-quadrant multiplier in Fig.9 of F. J. Lidgey's article, the linearized long-tail pair is also used in doubly balanced mixer integrated circuits, e.g. the Motorola and Signetics MC 1496. Such a mixer might be used in a radio receiver to multiply an incoming signal with the output from a local oscillator in order to generate a signal at the intermediate frequency. If the mixer has non-linear characteristics, then it may also combine two or more signals at its input to give a spurious output signal at or near the intermediate frequency[1]. This process is

continued on p.107

TELECOMMS TOPICS

ADRIAN MORANT

PABXs from the exchange

Both Mercury and British Telecom have announced plans to offer Centrex services based on 10,000 line telephone exchanges, the former having stated that it expects to be able to offer the service in the City of London before the end of the year while the latter is planning to launch a trial, also in the City, early next year. Centrex, a contraction of 'central exchange', will allow the features normally associated with a p.a.b.x. to be provided directly from the public telephone exchange.

Currently, no switching system developed in Europe can offer proven Centrex facilities, so Mercury has placed an order, believed to be worth £2m, with Northern Telecom while BT has signed with AT&T and Philips Telecommunications UK Ltd for an ESS-PRX switch. However, BT has now specified the provision of these services on System X and Ericsson's AXE10 (System Y) exchanges to be used on the network.

While this service has been offered in a basic form in the USA for a number of years it is the technology of today's advanced digital exchanges which, together with optical fibres, make it feasible to obtain the sophisticated performance that is now becoming available.

Centrex provides an alternative to on-site p.a.b.xs. It allows users to adopt the advanced features of modern p.a.b.xs without having to plan, purchase, accommodate and install their own equipment and also allows them the flexibility to accommodate the changing needs of growing organisations.

It can be considered as having the p.a.b.x. sited at the local public telephone exchange with wires associated with each extension running all the way back to that exchange. It is expected, however, that it will be implemented via a single optical-fibre cable to a building. This will be the equivalent to possibly hundreds of ordinary copper wires and be economically viable.

One essential factor being that whereas p.a.b.xs can be supplied by independent vendors as well as the network supplier, e.g. BT, Centrex will be the province of the carrier. In fact, the Office of Telecommunications (Oftel) is looking at the implications on these developments on the Branch Systems General Licence (BSGL) which covers the systems run by most users of telecommunication services.

Greater cellular capacity in London

The Department of Trade and Industry (DTI) has made available additional channels in the London area for cellular radio. This should enable the maximum traffic capacity of both the Vodafone and Cellnet systems to be doubled in the central London area where congestion has been experienced. It will take, however, an appreciable time for the effects to filter through to the user, since none of the existing sets are able to make use of these extra channels and neither network is yet suitably equipped.

Initially 1,000 channels were designated for cellular services. 600 of them were allocated equally between the two networks, with the remaining 400 reserved for the projected pan-European digital cellular service. Of the additional channels that are becoming available, because of re-allocation of frequencies currently allocated to the Ministry of Defence, 200 will become available to each operator. In due course, if demand justifies it, a further 120 channels could be made available to each operator. This, would make 620 instead of the 300 that each operator has at present and so increase the number of subscribers that the networks can support without the quality of service becoming noticeably degraded.

Growing networks

The number of private wide area networks (wans) in Western Europe will almost double in the next six years to 1992. By then, according to a study carried out by Logica as part of its Telematica multi-client market service, the number will have grown to 18,640 from today's 9,430. Similarly, the market for all packet-switching products will have grown from $84 million in 1986 to $163m in 1991.

Other findings of the report indicate that the market for multiplexers and network multiplexers will also grow over the same period. While it will be larger, from $200m to $330, it will be growing at a lower rate, with the result that the packet-switching share of the total wan market will have risen from 29 to 33%.

P.b.x. suppliers such as Plessey in the UK and Germany's Siemens have been busy developing interworking between their p.b.x.s and packet switches. This approach will assure them of a long-term advantage among small and medium sized customers once the p.b.x. gains acceptance as a reliable data carrier.

At the same time, IBM's move into the data networking market will be watched with considerable interest in the near future. It is currently developing a new networking strategy and is intending to increase its share of the data networking market. Its moves into local area networking, protocol conversion and p.b.xs are evidence of this. It is likely that IBM will develop or badge other networking products in the near future. Although it will take time to gain large shares of the established markets for the more specialized and already proven products (such as large packet switches), and although many users will react unfavourably towards IBM in order to maintain a measure of supplier independence, IBM's long term effect on the market will be considerable.

BT digital progress

London's first major System X exchange has opened and already it is handling over 3,500 subscriber lines. In Wood Street, in the City of London, it is a key exchange for City Institutions such as the Bank of England. By next March BT will have provided over one million digital subscriber connections and is aiming for 12 million such connections by the end of the decade.

Already 45 of BT's 55 main digital switching centres are already in service and it is introducing the CCITT Common Channel Signalling System No 7. It claims that it has the largest interconnected digital network in the world – a total of 70 System X exchanges with 165,000 lines in operation. Now, with its programme well under way, one new digital exchange is entering service every working day.

The first of the Ericsson AXE exchanges is also being brought into service at Sevenoaks, Kent. AXE was selected by BT as the alternative to System X and thus often referred to as System Y.

As part of its digitalization programme BT has its 80kbit/s IDA (integrated digital access) pilot scheme serving 60 telephone areas. In total, there are roughly 1000 single line accesses available plus a few 2Mbit/s multiline ones for p.b.xs. From next year BT will be making the 144kbit/s CCITT standard single line accesses available.

Optical-fibre links in Hong Kong

As part of the increasing digitalization of the Hong Kong network, a 140Mbit/s single-mode optical system operating at 1300nm will connect the Cable and Wireless (HK) satellite earth station, the submarine cable station and Hong Kong's international telecommunications facilities at the C&W headquarters in new Mercury House, Wanchai. Provided by GEC Telecommunications, the new optical-fibre link will complement the existing analogue microwave system and analogue cables linking these systems.

In addition, the existing cross-harbour optical fibre cable system, connecting New Mercury House to the second international switching centre in Tsim Sha Tsui, Kowloon, will be upgraded from 34Mbit/s to 140Mbit/s. For this system, the optical transmission equipment has been designed with leds (rather than the lasers in the system above) to optimize the use of the existing multimode fibre cable over the relatively short 2.5km path.

Irish National videotex

The Irish National Telecommunications Authority, Telecom Eireann, has awarded Micro Scope plc the contract to provide its national videotex network. Telecom Eireann anticipates that the pilot service of the network, based on MicroScope's videotex access points (v.a.ps), will go live in the autumn.

The 96 port network has v.a.ps situated in Dublin, Limerick, Galway and Cork, providing local call access to the users. The network will provide support for single and multi-standard videotex terminals including all of the European videotex standards. These are the CEPT terminal standards known as Profile 1, 2 and 3 on which the German Bildschirmtext, Teletel (France) and Prestel services respectively are based.,

Support will also be provided for ASCII terminals. Gateway protocols (for host computer connection) supported will include Prestel Gateway and X.29. The network will include a transcoding facility between terminal standards and international Gateway access to videotex services in the UK, France, Germany and other European countries. The national videotex network of Eire has also been designed to provide access to a comprehensive electronic mailbox system, Eirmail.

Tokyo running out of numbers

The three-digit station-code numbering system in metropolitan Tokyo is expected to reach its limit of usable telephone numbers by next March. Consequently, Nippon Telegraph and Telephone Corporation (NTT) has announced that an extra digit will be added to certain 3-digit codes in the 23 wards of Tokyo from January 1987.

As the first measure to expand the system, pocket bell pages will be given four-digit station codes from January 1987 and first-time general telephone subscribers will be assigned four-digit station codes in January 1988.

According to an NTT spokesman: "The new measure initially will apply only to first-time subscribers. The approximately five million telephones which are now installed in metropolitan Tokyo will continue to have three-digit station codes until the beginning of 1993."

German packet network upgrade

The German PTT, the Deutsche Bundespost, has placed a $10 million contract with Northern Telecom for equipment to expand its Datex-P packet switching network to meet the rapid growth of demand.

It is based on NT's SL-10 data packet switching systems which were initially installed and operational in spring 1980. The primary network services offered are the CCITT standards X.3, X.25, X.28 and X.29 with international connections to over 50 data networks in 32 countries being provided by the X.75 gateway service. At the end of last year the network consisted of 45 switching nodes distributed in 17 cities throughout Germany, supporting over 15,000 user-data connections. The network is growing at a rate of 5 per cent monthly at present.

CERN Geneva to become integrated

CERN, the European Laboratory for particle physics, is to establish a distributed communications network to serve its operations spread over a number of different locations. It has placed an order with ITT's Norwegian company Standard Telefon og Kabelfabrik (STK) for an ITT 5500 BCS system which will initially serve 11 sites at CERN locations in the Geneva area.

Under the contract STK will supply an integrated services digital network (ISDN) to provide voice and data communications. It will allow interconnection with a variety of computers and terminals, connectivity with the existing CERN data network and the present crossbar p.a.b.x. as well as direct in-dialling to all CERN telephones. The ultimate capacity of the network is intended to be more than 12,000 ports, of which more than half would be data ports.

Airlines data update

The largest private data network in the world has just been re-equipped with low-speed (2,400 to 9,600 bit/s) modems. The international airline communications network run by SITA, which is owned by nearly 300 major international airlines, has installed these modems in 36 countries around the world extending from Algeria to Uruguay and including the UK, USA and Russia.

BT expands packet switching

In order to meet demand for international information technology services, doubling annually throughout this decade, British Telecom International (BTI) has opened a £3.7 million exchange computer data. The second to be brought into service by BTI for its international packet switched service (IPSS) it provides greatly increased call handling capacity and additional customer and network facilities to provide industry and commerce with fast, reliable and economical data communications with 50 countries offering access to and from 73 different packet switched data networks.

The new gateway uses the DPS 1500 packet switch developed and manufactured by Bell Telephone Manufacturing Company, Antwerp, and supplied and installed by STC Telecommunications.

Link to London embassy

The satellite communications link between the American Embassy in London and the US State Department in Washington has been officially opened. The new 1.6Mbit/s British Telecom Satstream link via Intelsat is dedicated to the exclusive use of the State Department and provides a flexible means of carrying voice and data traffic.

Since this London link was installed, the State Department has placed an order with BT to extend the service to US Embassy in Bonn, West Germany.

BellSouth International plans expansion

BellSouth, one of the Regional Bell Operating Companies of the USA is establishing a company in London as part of its planned expansion, with particular reference to Europe and Latin America. When speaking in London recently Ms Mylle H. Bell, BellSouth International president, said that international operations would constitute an increasing amount of BellSouth's business and that the parent company would provide whatever resources were necessary.

The BSI approach is "to work with and through the local communications community". This is underlined by the agreement with London-based Air Call to form a joint venture called Air Call Communications, which will offer cellular, mobile paging media response and telephone answering services in Grat Britain and other European countries. In addition to an agreement with the city of Metz, France, regarding a Teleport which will offer advanced communications services to high volume users, BSI has held discussions with both the French and German PTTs.

In addition, Brian Hailes who, prior to joing BSI spent nine years with ITT in London, Brussels and the USA, has been appointed v.p. marketing. He is responsible for world-wide markets with the exception of the Hong Kong basin. He sees Europe, especially UK and France, as being the areas of major importance. However, Hailes, who works out of Atlanta, Georgia, is also looking to Arabian Gulf and Northern Middle East area for business "on an opportunistic basis".

Using the Data Encryption Standard

Hardware and software for interfacing a WD2002 data encryption device to a Z80 processor

BRIAN P. McARDLE

Encryption or encipherment[1] is the process that changes data into secret form. The original data is known as plaintext or cleartext and the encrypted data as ciphertext. The encryption operation is described by the equation

$$\hat{E}_K(P)=C \qquad (1)$$

where P,C and K are the plaintext, ciphertext and key respectively. In electronic encryption P and C are the electronic representation of characters. The purpose of the key is to vary the operation. A change of key results in a different C from the same P. The inverse or decryption operation is described by the equation

$$\hat{E}_K^{-1}(C)=\hat{D}_K(C)=P. \qquad (2)$$

Normally the only part of $\hat{E}_K$ or $\hat{D}_K$ that is varied is K. A user chooses a key from a set of possible keys, {K}. This particular key must be kept secret since it must be assumed that an unauthorized listener (cryptanalyst) to an encrypted message would know the fixed operations. He may also know some plaintext such the plaintext-ciphertext pairs can be formed: Therefore in a satisfactory cryptosystem.

1. The number of possible keys must be very large to prevent a cryptanalyst from trying each key in turn in equation 2 until meaningful decrypted data is obtained.
2. The fixed operations must be very complicated such that a key cannot be deduced from a plaintext-ciphertext pair(s).

DATA ENCRYPTION STANDARD

The Data Encryption Standard (DES)[2] (Fig.2.) was selected by the U.S. National Bureau of Standards in 1977 to protect computer data by encrypting the binary coded information. Plaintext, key and ciphertext blocks consists of 64, 56 and 64 bits respectively.

The algorithm has 16 stages and a key block of 48 bits is generated from the original 56 bits at each stage. The plaintext block is divided into two sub-blocks, L_0 and R_0, of bits each by the initial permutation. The right block, R_0, and first key block, K_1, are used to generate a new block which undergoes an exclusive-or operation with L_0 to produce R_1.

The f function is very complicated and is not considered in this article. The reader is referred to FIPS PUB 46, National Bureau of Standards[2] for a more detailed description.

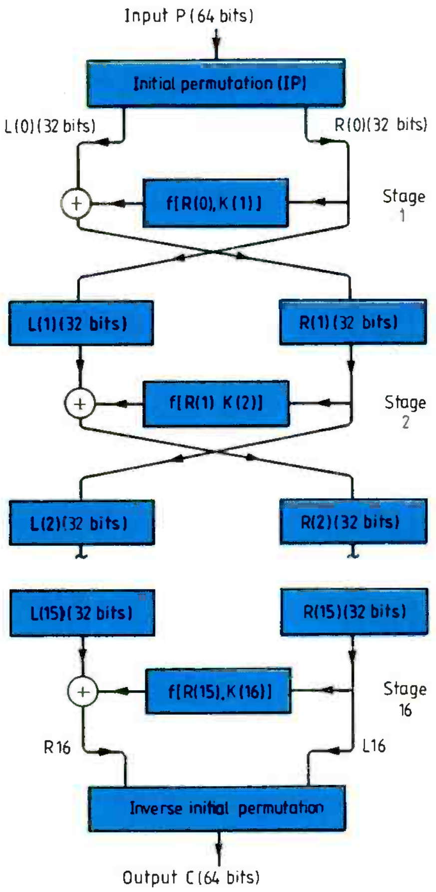

Fig.1. Data encryption algorithm.

This procedure is repeated for the stages j=1 to 16 and the encryption operation is described by the equations

$$L_j=R_{j-1}$$

$$R_j=f(R_{j-1},K_j)\oplus L_{j-1}$$

Input blocks to the inverse initial permutation are L_{16} and R_{16} and the output is the ciphertext block. Decryption involves the same process but applies the keys in reverse order.

Keys, K_1 to K_{16}, are generated by the method shown in Fig.2. An input block of 64 bits is reduced to 56 bits and formed into two sub-blocks, C_0 and D_0, by permuted choice 1[2]. The eight redundant bits are generally used as parity bits.

The first key, K_1, is generated from the two blocks by permuted choice 2[2]. Then the bits of C_0 and D_0 are shifted once and K_2 is generated. This procedure is repeated for the 16 stages with the following shift arrangement,

1,1,2,2,2,2,2,2,1,2,2,2,2,2,2,1.

Operations within the algorithm are very complicated. Each bit of the ciphertext block depends on the full plaintext and key blocks. Hence it is impossible to establish a relationship between individual bits of the three blocks. The main criticism centres on the size of the key block of 56 bits. A user chooses a key block from a set of 2^{56} possible blocks. All other operations are fixed and cannot be varied.

The designer[3] of the standard estimated that a computer which could make a search of the set of possible blocks in approximately one day would not be available before the year 2000. This now seems unlikely. However, double or triple encryption[4] should prolong the life-span. For the present the standard is cryptographically secure.

IMPLEMENTATION

To avoid modifications by users the standard must be implemented in hardware. It is available on a number of integrated circuits, such as the Western Digital 2002 and Intel 8294, which can be interfaced to eight-bit microprocessors.

Figure 3 shows the interfacing arrangement for a WD2002 device in a design prototyping board of a Multitech Micro-Professor kit, which is based upon a Z80 microprocessor. The $\overline{CS}$ input is put low to enter or read data. The $\overline{ACT}$ input is put high to initiate execution of the algorithm. The $\overline{E/D}$ input is put low to encrypt or high to decrypt. These three inputs are obtained from a parallel input/output device (Z80-p.i.o) designed to interface the Z80 microprocessor to peripheral devices. Data lines (B_0 to B_7) are connected to the system's data bus. Input $\overline{WE}$ is put low to enter data into the device from the data bus; $\overline{RE}$ is put low to read data from the device on to the data bus. These inputs are obtained from two unused chip-select outputs on the address decoder. The $\overline{WE}$ or $\overline{RE}$ input is put low by placing \$E800 or \$E000 as appropriate on the address bus. Otherwise both inputs are high. Inputs $\overline{CK}$ and $\overline{MR}$ are connected to the system's clock and reset lines respec-

```
10  DATA 161,176,193,208
20  DATA 224,241,161,176
30  FOR I=1 TO 8
40  READ K
50  POKE 61509+I,K
60  NEXT I
70  INPUT ''E OR D'',R$
80  IF R$=''E'' THEN 110
90  IF R$=''D'' THEN 230
100 GOTO 70
110 POKE 61445,02
120 FOR I=1 TO 8
130 INPUT''PLAINTEXT'',P$
140 P=ASCII(P$)
150 POKE 61517+I,P
160 NEXT I
170 CALL 61440
180 FOR I=1 TO 8
190 C=PEEK(61517+I)
200 PRINT''CIPHERTEXT'';C
210 NEXT I
220 GOTO 120
230 POKE 61445,06
240 FOR I=1 TO 8
250 INPUT''CIPHERTEXT'',C
260 POKE 61517+I,C
270 NEXT I
280 CALL 61440
290 FOR I=1 TO 8
300 P=PEEK(61517+I)
310 P$=CHR$(P)
320 PRINT''PLAINTEXT '';P$
330 NEXT I
340 GOTO 240
```

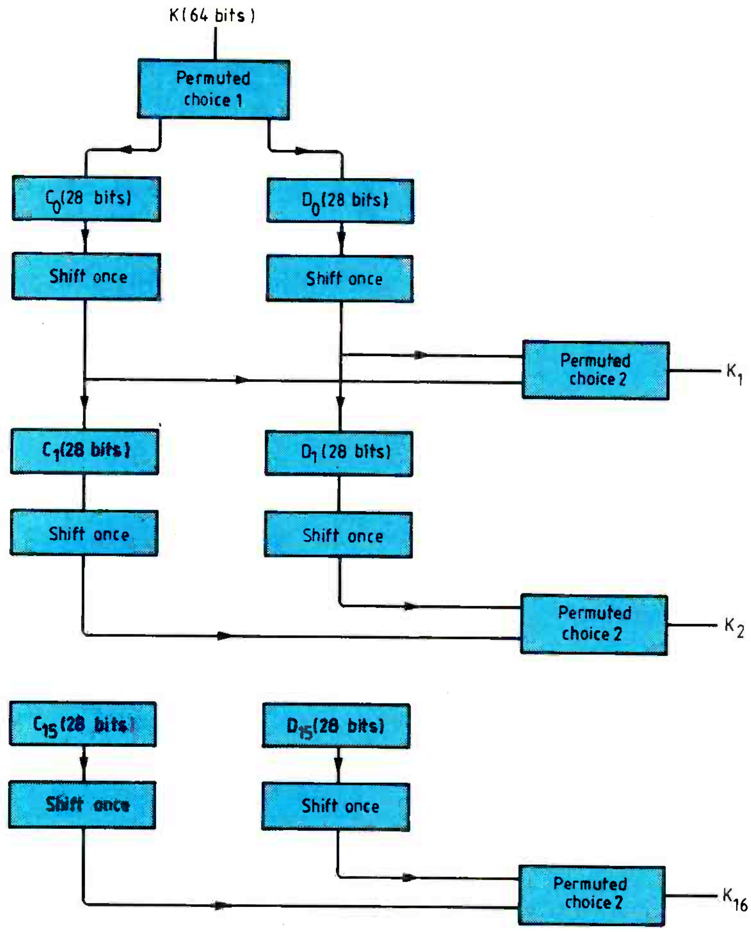

Fig.2. Key blocks for the Data Encryption Standard.

tively. For this particular mode of operation the DPS and CRPS inputs are tied high and low respectively. The reader is referred to WD2001/2 data sheet (Western Digital Corporation) for a more detailed description of the device.

Encryption/decryption operation is initiated by putting CS low, ACT high and E/D low or high as appropriate. Then the key block is loaded by pulsing the WE input low eight times with appropriate bytes on the data bus. The key block uses 56 bits and the eight redundant bits are used as parity bits; parity of every key byte must be odd. Once the key block has been entered it cannot be read. Data is loaded after the key block using the same method. After approximately 50 clock periods the encrypted/decrypted data block becomes available and its is read out by pulsing the RE input low eight times. The Z80 microprocessor controls the operation of the WD2002 but does not take part in the encryption/decryption operation: this happens entirely within the WD2002.

PROGRAM

The program is written in Basic and stored in location $F100 upwards. Encryption and decryption are handled by a machine code sub-routine stored at $F000: the key bytes are entered into memory at locations $F046 to $F0AD by the Poke statement. The user is requested to input E to encrypt or D to decrypt.

For encryption, the number $02 is stored in location $F005. The plaintext block is entered as eight Ascii characters, which are changed to eight data bytes and entered into memory at locations $F04E to $F055 using Poke. After execution of the encryption sub-routine these locations contain the encrypted data bytes which are read using Peek and output to the display. Then the user is requested to input the next plaintext block.

For decryption the number $06 is stored in location $F005. Ciphertext is entered into memory at locations $F04E to $F055. After execution of the decryption sub-routine, decrypted data bytes are read from memory, changed back to characters of the Ascii alphabet and displayed. Then the user is requested to input the next ciphertext block.

If K=(161,176,193,208,224,241,161,

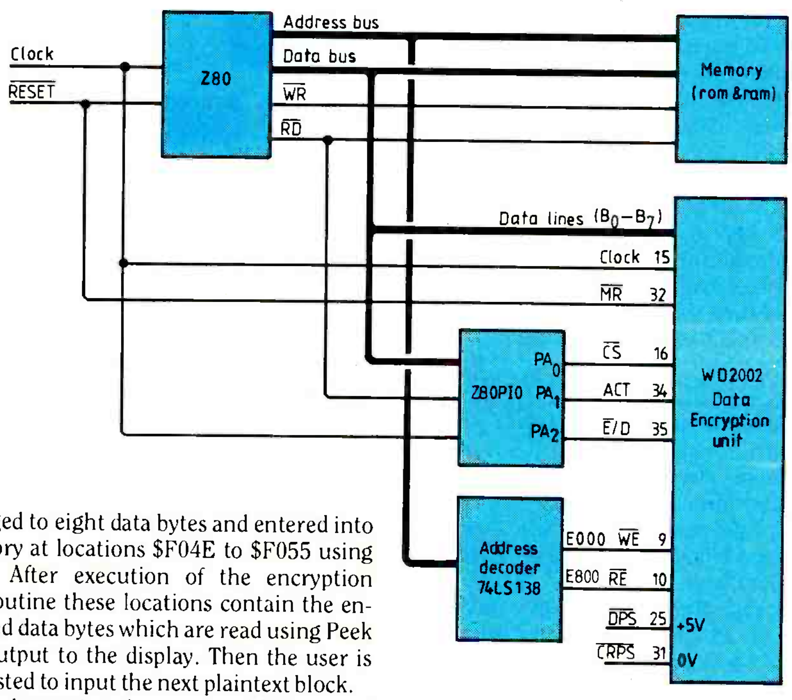

Fig.3. Interfacing the WD2002 to the Micro-Professor Z80 system.

For details of the Micro-Professor single-board microcomputer, contact Flight Electronics at Southampton on 0703-227721. The unit is also available from Verospeed on 0703-644555.

This encryption-decryption rountine is called by the Basic program (facing page).

```
$F000  MVIA ##0F     3E  0F
$F002  OUT $6A       D3  6A
$F004  MVIA ##02     3E  02
$F006  OUT $68       D3  68
$F008  LXI $F046     21  46  F0
$F00B  MVIB ##00     06  00
$F00D  MOV A,M       7E
$F00E  STA $E800     32  00  E8
$F011  INX H         23
$F012  INR B         04
$F013  MOV A,B       78
$F014  CPI ##08      FE  08
$F016  JNZ $F00D     C2  0D  F0
$F019  MVIB ##00     06  00
$F01B  MOV A,M       7E
$F01C  STA $E800     32  00  E8
$F01F  INX H         23
$F020  INR B         04
$F021  MOV A,B       78
$F022  CPI ##08      FE  08
$F024  JNZ $F01B     C2  1B  F0
$F027  MVIA ##00     3E  00
$F029  NOP           00
$F02A  INR A         3C
$F02B  CPI ##FF      FE  FF
$F02D  JNZ $F029     C2  29  F0
$F030  LXI $F04E     21  4E  F0
$F033  MVIB ##00     06  00
$F035  LDA $E000     3A  00  E0
$F038  MOV M,A       77
$F039  INX H         23
$F03A  INR B         04
$F03B  MOV A,B       78
$F03C  CPI ##08      FE  08
$F03E  JNZ $F035     C2  35  F0
$F041  MVIA ##01     3E  01
$F043  OUT $68       D3  68
$F045  RET           C9
```

176] and P=[A,B,C,D,E,F,G,H] then C=[192,87,116,149,195,29,56,121].

The main disadvantage is that the ciphertext block consists of eight numbers ranging from 0 to 255. The Ascii alphabet has 128 characters and consequently half of the 256 combinations of a byte are not required. Hence the ciphertext block must be expressed in numeric form. Any one of the 2^{56} key blocks can be used but each key byte must have odd parity. Nevertheless. the standard offers an inexpensive and secure cryptosystem.

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1. Denning, Dorothy E., Cryptography and Data Security. Addison Wesley, Reading (1982).
2. Data Encryption Standard: FIPS PUB 46, National Bureau of Standards, Washington D.C. U.S.A. (1977)
3. Kinnucan, Paul, Data Encryption Gurus: Tuchman and Meyer. Cryptologia, volume 2, no.3 (1978).
4. Merkle, Ralph C., On the Security of Multiple Encryption. *Communications of the ACM*, volume 24, no.7 (1981).

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FEEDBACK

Bel-ringing

It is futile for Joules Watt ('Ringing the changes on Bels' October, 1986) to claim that decibels are 'meaningless' when applied to voltage ratios.

True, the original definition of a Bel was $\log_{10}$ of a power ratio, so that dB = 10 $\log_{10}$ (power ratio). The circuit resistance being unchanged, since $P=E^2/R$, then $P_1/P_2 = E^2_1/E^2_2$; so now if dB = $\log_{10}$ (power ratio), then also dB = 20 $\log_{10}$ (voltage ratio) *for constant resistance*.

The fact is that throughout the telecommunications industry, dB is used to represent 20 $\log_{10}$ (voltage ratio) *irrespective of resistance* and is understood by telecommunications engineers, authors, technicians and practitioners in general to mean just that. Telecommunicators do use dB to represent power ratios as well, but in any case it is either obvious from the context which ratio is intended, or, indeed as JW hints, has to be made explicitly clear.

The IEEE's reported head-in-the-sand comment about dB with letters appended, again does not alter the fact that dBV, dBμV, dBm, dBW and other such convenient short-hand terminologies are widely used and recognised as absolute measurements in telecommunications. The joker in this pack is dBm (dB relative to 1mW) which is usually understood to represent a voltage across a defined resistance, and so dBm should always be accompanied by a defined resistance (e.g. '0dBm across 100ohms' represents $(10^{-3}\text{W} \times 100\text{ohms})^{1/2} = 316\text{mV}$).

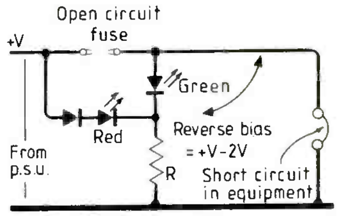
This muddle, I'm afraid, JW, is the real world of engineering. However, there is no real problem as long as everyone does understand the accepted practice, and as long as the issue is not clouded with transcendental functions, and theoretical paradoxes...

JW's 1 megohm input/50 ohm output/unity-voltage-gain amplifier can quite meaningfully and unambiguously be said to have a voltage gain of 0dB (=20 $\log_{10}$ unity) and a power gain of 43dB (= 10 $\log_{10}$ 20,000).

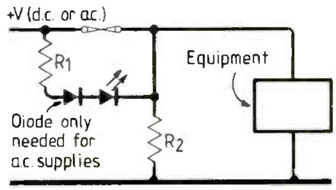
Brian J Pollard,
Watford,
Herts.

Fuse condition indicator

The published design (July 1986) will undergo the condition illustrated in Fig.1 should a short

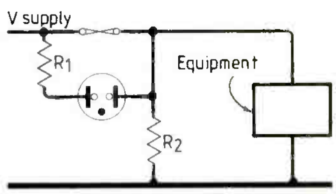


circuit occur in the monitored equipment. If the supply voltage exceeds a few volts the green led will suffer excessive reverse bias and will ultimately be damaged.



$R_1=R_2$, chosen for suitable led current

There are two possible improved approaches to monitoring fuse behaviour. The circuit in Fig.2 is exclusively for low to medium voltage supplies (a.c. or d.c.).



$R_1=R_2$, chosen for suitable neon current

The second version, shown in Fig.3 is intended for higher voltage rails (typically over 100V), again a.c. or d.c.

S. Whitt,
Ipswich.

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AN240P	2.80	MC1327	1.70	STK043	15.50	TBA550Q	1.95	TDA2530	1.95		
AN612	2.15	MC1349P	1.20	STK078	11.95	TBA560C	1.45	TDA2532	1.95		
AN7116	1.50	MC1351P	1.50	STK433	5.95	TBA460CQ	1.45	TDA2540	1.95		
AN7140	3.50	MC1357	2.35	STK435	7.95	TBA570	1.00	TDA2545A	2.15		
AN7145	3.50	MC1358	1.58	STK437	7.95	TBA651R	2.50	TDA2451	2.15		
AN7150	2.95	MC1495	3.00	STK439	7.95	TBA720A	2.45	TDA2560	2.15		
BA521	3.35	MC1496	1.25	STK461	11.50	TBA750Q	2.65	TDA2571A	4.50		
CA1352E	1.75	MC145106P7	7.95	TA7061AP	3.95	TBA800	0.89	TDA2581	2.95		
CA3086	0.46			TA7108P	1.50	TBA810AS	1.65	TDA2593	2.95		
CA3123E	1.50	MC1723	0.50	TA7120P	1.65	TBA810P	1.65	TDA2600	6.50		
HA1366W	3.50	MC3357	2.75	TA7130P	1.50	TBA820M	0.75	TDA2610	3.50		
HA1377	3.50	ML231B	1.75	TA7176AP	2.95	TBA820Q	1.45	TDA2611A	1.95		
HA1156W	1.50	MSM5807	6.75	TA7203	2.95	TBA890	2.50	TDA2640	3.50		
HA1339A	2.95	PLL02A	5.75	TA7204P	2.15	TBA920	1.65	TDA2680A	2.75		
HA1398	2.75	SAA500A	3.50	TA7205AP	1.15	TBA950/2X	2.35	TDA2690	2.45		
HA1551	2.95	SAA1025	7.25	TA7222AP	1.80	TBA990	1.49	TDA3310	2.95		
LA1230	1.95	SAS560S	1.75	TA7227P	4.25	TCA270	1.50	TDA3560	5.50		
LA4031P	1.96	SAS570S	1.75	TA7310P	1.80	TCA270SQ	1.50	UPC566H	2.95		
LA4102	2.95	SAS580	2.85	TA7313AP	2.95	TCA650	3.50	UPC575C2	2.75		
LA4140	2.95	SL917B	7.50	TA7321P	2.25	TCA800	6.95	UPC1025H	1.95		
LA4400	4.15	SL1310	1.80	TA7146P	2.50	TCA940	1.65	UPC1028H	1.95		
LA44..	1.95	SL1327	1.10	TA7609P	3.95	TDA440	3.50	UPC1032H	1.50		
LA44..	2.50	SL1327Q	1.10	TA7611AP	2.95	TDA1001	2.95	UPC1156H	2.75		
LA4430	2.50	SN76003N	3.95	TAA310A	2.50	TDA1002A	2.95	UPC1158H	0.75		
LA4461	3.95	SN76023N	3.95	TAA320A	1.95	TDA1006A	2.50	UPC1157C2	1.95		
LC7120	3.25	SN76033N	3.95	TAA350A	1.95	TDA1035	2.50	UPC1181H	1.25		
LC7130	3.50	SN76110N	0.89	TAA570	1.95	TDA1037	1.95	UPC1182H	2.95		
LC7131	5.50	SN76115N	1.25	TAA661B	1.95	TDA1074A	1.95	UPC1185H	3.95		
LM324N	0.45	SN76131N	1.30	TBA700	1.70	TDA1170	1.95	UPC1191V	1.50		
LM380N8	1.50	SN76226DN	2.95	TBA120AS/B/C/		TDA1190	2.15	UPC1350C	2.95		
LM380N14	1.75	SN76226N	1.05	SA/SB/T/U	1.00	TDA1270Q	5.50	UPC1353C	2.45		
LM383T	2.95	SN76533N	1.65	TBA395	1.50	TDA1327	1.70	UPC1365C	3.95		
LM3900N	3.50	SN76544	2.65	TBA396	0.75	TDA2002	1.95	UPC2002H	1.95		
M51513L	2.30	SN76570N	1.00	TBA440N	2.55	TDA2003	1.95	555	0.36		
M51515L	2.95	SN76650N	1.15	TBA480Q	1.25	TDA2004	2.95	556	0.60		
M51521L	1.50	SN76660N	0.80	TBA510	2.50	TDA2005	2.95	723	0.50		
MB3712	2.00	STK014	7.95	TBA510Q	2.50	TDA2006	1.95	741	0.35		
				TBA520	1.10	TDA2020	2.95	747	0.50		
				TBA520Q	1.10	TDA2030	2.80	748	0.35		
				TBA530	1.10	TDA2190	3.95	7805	0.65		
				TBA530Q	1.10	TDA2522	1.95	7808	0.60		
								7815	0.65		

SEMICONDUCTORS

AAY12	0.25	BC182	0.10	BD232	0.35	BFR91	1.75	RCA16335	0.80		
AC125	0.20	BC182LB	0.10	BD233	0.35	BFT42	0.35	SKE5F	1.45		
AC126	0.45	BC183	0.10	BD234	0.35	BFT43	0.35	TIP29	0.40		
AC127	0.20	BC183L	0.09	BD236	0.49	BFW92	0.85	TIP29C	0.42		
AC128	0.23	BC184LB	0.09	BD237	0.40	BFX29	0.30	TIP30C	0.43		
AC128K	0.32	BC204	0.10	BD238	0.40	BFX84	0.26	TIP31C	0.55		
AC141	0.28	BC207B	0.13	BD242	0.65	BFX85	0.32	TIP32C	0.42		
AC142K	0.45	BC208B	0.13	BD246	0.75	BFX86	0.30	TIP33C	0.95		
AC176	0.22	BC212	0.09	BD376	0.32	BFX88	0.25	TIP34B	0.95		
AC176K	0.31	BC212L	0.09	BD410	0.65	BFY50	0.21	TIP41A	0.45		
AC187	0.25	BC212LA	0.09	BD434	0.65	BFY51	0.21	TIP41C	0.45		
AC187K	0.28	BC213	0.09	BD437	0.75	BFY52	0.25	TIP42C	0.47		
AC188	0.25	BC213L	0.09	BD438	0.75	BFY90	0.77	TIP47	0.65		
AC188K	0.37	BC214	0.09	BD520	0.65	BLY48	1.75	TIP120	0.60		
ACY17	1.15	BC214C	0.09	BD538	0.65	BRY39	0.45	TIP125	0.65		
AD142	0.79	BC214L	0.09	BD597	0.95	BR100	0.26	TIP142	1.75		
AD143	0.82	BC237B	0.09	BD589	0.45	BR110	0.49	TIP161	2.95		
AD149	0.70	BC238	0.09	BD701	1.25	BR103	0.55	TIP2955	0.85		
AD161	0.39	BC239	0.12	BD702	1.25	BRC4443	1.15	TIP3055	0.55		
AD162	0.39	BC251A	0.12	BD707	0.90	BT100A/0	20.85	TIS91	0.20		
AD161/2	0.90	BC252A	0.15	BDX32	1.50	BT106	1.49	TV106/2	1.50		
AF106	0.50	BC258	0.25	BF115	0.35	BT116	1.20	2N1308	1.35		
AF114	1.95	BC258A	0.39	BF119	0.35	BT119	3.15	2N2219	0.28		
AF115	2.95	BC2284	0.30	BF119	0.65	BT120	1.65	2N2222	0.29		
AF116	2.95	BC300	0.30	BF127	0.39	BU105	1.95	2N2905	0.40		
AF117	2.95	BC301	0.30	BF154	0.20	BU108	1.69	2N3053	0.40		
AF121	0.60	BC303	0.26	BF158	0.22	BU124	1.25	2N3054	0.59		
AF124	0.65	BC307B	0.09	BF160	0.27	BU125	1.25	2N3055	0.52		
AF125	0.35	BC327	0.10	BF167	0.27	BU126	1.60	2N3702	0.12		
AF126	0.32	BC328	0.10	BF173	0.22	BU204	1.55	2N3703	0.12		
AF127	0.65	BC337	0.10	BF177	0.38	BU205	1.30	2N3704	0.12		
AF139	0.40	BC338	0.09	BF178	0.26	BU208	1.39	2N3705	0.20		
AF150	0.60	BC347A	0.13	BF179	0.34	BU208A	1.52	2N3706	0.12		
AF178	1.95	BC461	0.35	BF180	0.29	BU208D	1.85	2N3708	0.12		
AF239	0.42	BC478	0.20	BF181	0.29	BU3276	1.20	2N3733	9.50		
AFZ12	3.75	BC527	0.20	BF182	0.29	BU407	1.24	2N3733	2.75		
ASY27	0.85	BC547	0.10	BF183	0.29	BU500	2.25	2N3792	1.35		
AU106	4.50	BC548	0.10	BF184	0.28	BU508A	1.95	2N4427	1.95		
AU107	3.50	BC549A	0.10	BF185	0.28	BU526	1.90	2N4444	1.15		
AU110	3.50	BC550	0.14	BF194	0.11	BU80Y	2.25	2N5294	0.42		
AU113	4.50	BC557	0.08	BF195	0.11	BUY69B	1.70	2N5296	0.48		
BC107A	0.11	BC557B	0.80	BF196	0.11	MJ3000	1.98	2N5298	0.60		
BC107B	0.11	BC558	0.10	BF197	0.11	MJE340	0.40	2N5485	0.45		
BC108	0.10	BCY33A	1.60	BF198	0.16	MJE520	0.48	2N5496	0.95		
BC108A	0.11	BD115	0.30	BF199	0.14	MPSA13	0.29	2SA715	0.60		
BC108B	0.12	BD124P	0.59	BF200	0.40	MPSA92	0.30	2SC495	0.80		
BC109	0.10	BD131	0.42	BF241	0.15	MRF237	4.95	2SC496	0.80		
BC109B	0.12	BD132	0.42	BF245	0.30	MRF450A	13.95	2SC1096	0.80		
BC109C	0.12	BD133	0.40	BF257	0.28	MRF453	17.50	2SC1106	2.50		
BC114	0.11	BD135	0.30	BF258	0.28	MRF454	26.50	2SC1172Y	2.20		
BC116A	0.15	BD136	0.30	BF259	0.28	MRF455	17.50	2SC1173	1.15		
BC117	0.19	BD137	0.32	BF271	0.26	MRF475	2.95	2SC1306	1.40		
BC119	0.24	BD138	0.30	BF273	0.18	MRF477	10.00	2SC1307	2.95		
BC125	0.25	BD139	0.32	BF336	0.34	MRF838	13.95	2SC1364	0.50		
BC139	0.20	BD140	0.30	BF337	0.29	OC16W	2.50	2SC1449	0.80		
BC140	0.31	BD144	1.10	BF338	0.32	OC23	1.50	2SC1678	1.25		
BC141	0.25	BD150C	0.29	BF355	0.37	OC28	1.50	2SC1909	1.25		
BC142	0.21	BD159	0.65	BF362	0.38	OC29	2.25	2SC1945	2.65		
BC143	0.24	BD160	1.50	BF363	0.65	OC32	2.25	2SC1954	0.95		
BC147A	0.12	BD166	0.55	BF371	0.25	OC42	0.75	2SC1957	0.80		
BC147B	0.12	BD179	0.72	BF394	0.19	OC44	0.75	2SC1969	1.95		
BC148A	0.09	BD181	0.45	BF422	0.32	OC45	0.55	2SC2028	1.15		
BC148B	0.09	BD182	0.70	BF457	0.32	OC70	0.45	2SC2029	1.95		
BC149	0.09	BD183	0.70	BF458	0.36	OC71	0.55	2SC2078	1.45		
BC157	0.12	BD201	0.83	BF459	0.36	OC72	0.85	2SC2091	0.85		
BC158	0.09	BD202	0.65	BF467	0.68	OC75	0.95	2SC2098	2.95		
BC159	0.09	BD203	0.78	BF494	0.45	OC81	0.50	2SC2166	1.95		
BC1174	0.09	BD204	0.70	BF495	0.45	OC171	3.50	2SC2314	0.80		
BC174A	0.09	BD222	0.46	BF595	0.23	R2008B	1.45	2SC2371	0.36		
BC177	0.15	BD223	0.59	BF597	0.25	R2010B	1.45	2SD234	0.50		
BC178	0.15	BD225	0.48	BFR39	0.23	R2322	0.58	3N211	2.95		
				BFR81	0.25	R2323	0.66	3SK88	0.95		
				BFR88	0.30	R2540	2.48				
				BFR90	1.50	HCA16334	0.90				

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BA154	0.06	BY299-800	0.22	IN4007	0.06
BA156	0.15	BYX10	0.20	IN4148	0.02
BA157	0.30	BYX36-150R	0.20	IN4448	0.10
BAX13	0.04	BYX38-600R	0.60	IN5401	0.12
BAX16	0.06	BYX55-600	0.30	IN5402	0.14
BB105B	0.30	BYX71-600	1.10	IN5403	0.12
BT151	0.79	BZY95C30	0.35	IN5406	0.13
BY126	0.10	CS4B	4.50	IN5407	0.16
BY127	0.11	CS10B	8.45	IN5408	0.16
BY133	0.15	OA47	0.09	ITT44	0.04
BY164	0.45	OA90	0.05	ITT923	0.15
BY176	1.20	OA91	0.06	ITT2002	0.20
BY179	0.63	OA95	0.06		
BT182	0.55	OA202	0.10		
BY184	0.35	IN21DR	5.00		
BT199	0.40	IN23B	5.00		
BY206	0.14	IN23C	5.00		
		IN23ER	5.00		
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THORN 9800	22.40

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CME1428W	39.00	DP7.6	35.00	M40-120W	59.00
CME1523W	39.00	DN13 78	35.00	M43-12LG/01	65.00
CME1431GH	39.00	F16-101GM	75.00	M44-120LC	65.00
CME1431W	39.00	F16-101LD	75.00	M44-120GR	65.00
CME202GH	45.00	F21-130GR	75.00	M50-120GH	65.00
CME2024W	45.00	F21-130LC	75.00	M50-120GR	65.00
CME2325W	45.00	F31-10GM	75.00	M50-120GV	65.00
CME3218W	45.00	F31-10GR	75.00	M50-120LC	65.00
CME3132GH	45.00	F31-10LC	75.00	M61-120W	75.00
CME3155W	45.00	F31-10LD	75.00	SE3A/P31	40.00
CRE1400	25.00	F31-12LD	75.00	SE4/D/P7	45.00
CV1450	35.00	F31-13GR	75.00	SE42BP31AL	55.00
CV1526	19.00	F31-13LD	75.00	SE42BP31	55.00
CV2185	15.00	F31-13LG	75.00	SE5FP31	55.00
CV2191	19.00	F41-123LC	185.00	T948H	65.00
CV2193	15.00	F41-141LG	185.00	V5004LD	59.00
CV5119	85.00	F41-142LC	185.00	V6048CAL	59.00
CV5320	85.00	M7-120W	19.00	V6048J	49.00
CVX389	55.00	M7-120GH	19.00	V6064BP31	55.00
D9-110GH	39.50	M14-100GM	45.00	V6069GH	55.00
D10-210GH	45.00	M14-100LC	45.00	V6070P31	65.00
D10-210GH68B	65.00	M17-151GVR	175.00	V7030	59.00
D10-230GH	35.00	M17-151GR	175.00	V7031GH	59.00
D10-230GM	35.00	M19-100W	45.00	V7031/67A	59.00
D10293-GY/90	55.00	M19-103W	55.00	V7035A	49.00
D13-30GH	49.50	M23-110GH	55.00	V7037GH	45.00
D13-51GL/26	85.00	M23-111LD	55.00	V8004GR	65.00
D13-51GM/26	85.00	M23-112GM	55.00	V8006GH	65.00
D13-45GH/01	55.00	M23-112GV	55.00	V8010A	65.00
D13-610GH	59.00	M23-112GW	55.00	3BPI	11.50
D13-511GH	59.00	M23-112KA	55.00	3DPI	11.50
D13-611GM	59.00	M24-120GM	59.00	3H/OBM	55.00
D13-630GH	59.00	M24-120LC	59.00	3WPI	18.50
D14-150GH	75.00	M24-120WAR	59.00	4EPI	30.00
D14-150GM	75.00	M24-121GH	55.00	5BHP1	30.00
D14-162GH/84	59.00	M28-12GH	55.00	5BHP1FF	30.00
D14-172GR	55.00	M28-13LC	49.00	5BHP31	30.00
D14-172GV	55.00	M28-13LG	49.00	5CPI	10.00
D14-173GH	55.00	M28-13GR	49.00	5T01A	15.00
D14-173GM	53.00	M28-131GR	55.00	6EP7/S	39.00
D14-173GR	55.00	M28-133GH	55.00	13BPI	13.50
D14-181GH/98	65.00	M31-101GH	55.00	13BPA4	17.50
D14-181GJ	55.00	M31-182GR	55.00	17DWP4	25.00
D14-181GM	53.00	M31-182GV	53.00	32J/1085	69.00
D14-181GM50	59.00	M31-184W	65.00	1273	39.00
D14-182GH	59.00	M31-184GH	85.00	1564	45.00
D14-200BE	89.00	M31-184P31	65.00	1844	80.00
D14-200GA/50	85.00	M31-185W	69.00	9442E1	75.00
D14-200GM	75.00	M31-190GH	55.00	95447GM	75.00
D14-210GH	75.00	M31-190GR	55.00	95449GM	75.00
D14-270GH/50	75.00	M31-190LA	55.00	7709631	78.50
D14-310W	110.00	M31-191GV	55.00		
D14-320GH/82	85.00	M31-220W	59.00		
D14-340GH/KM	45.00	M31-270GY	65.00		
D14-340KA	45.00	M31-271P31	65.00		
D16-100GH	65.00	M31-271GW	65.00		
D16-100GH-65	69.00	M31-271W	65.00		
D16-100GH/67	65.00	M36-141W	75.00		
D16-100GH/79	69.00	M36-170LG	75.00		
D16-100GH/97	65.00	M38-101GH	65.00		
D18-160GH	69.00	M38-103GR	65.00		
D21-10GH	65.00	M38-120W	65.00		
DG7-5	55.00	M38-120WA	65.00		
DB7.6	35.00	M38-121GHR	65.00		
DB7.36	55.00	M38-121LA	65.00		
DG7.32	45.00	M38-122GW	65.00		
DG13.2	45.00	M38-140LA	65.00		

WIREWOUND RESISTORS

4 watt	2R4-10K	0.20
7 watt	R47-22K	0.20
11 watt	1R-15K	0.25
17 watt	1R-15K	0.30

SPECIAL OFFER

High Resolution Philips 12" M31-325GH £35.00 each coils + trans available

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VIDEO HEADS

3HSS Suitable for Most JVC and Ferguson models	29.50
3HSS(H) Suitable for Hitachi VT5000, VT8000, VT6000, VT8500, VT7000	33.95
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VIDEO BELT KITS

Akai VS9300/9500/9800	3.75	Sanyo VTC 5500	3.75
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JVCH HR 3330/3660	4.50	Sanyo VTC 9300P	3.90
JVC HR 3360/3660	4.50	Sharp VC 6300	3.75
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Panasonic NV 2000B	3.75	Sharp VC 8300	3.75
Panasonic 3000B	3.75	Sharp VC 9300	3.75
Panasonic NV7000	3.50	Sony SL 3000B	3.75
Panasonic NV8600B/8610B/VOII	3.75	Sony SL 8000/8080	4.50
		Sony SL C7/J7	4.00
		Toshiba V5470	4.50

BETAMIX VIDEO HEADS

PS3B (1 Pin) Suitable for Sony and Toshiba 5000 Series and NEC PV2400	39.50
RSV-3-B Suitable for Sony SL8000, SL8080, SLD7ME	39.50
DSR-10-R Suitable for Sony SLC5, SLC6, SLC7	39.50
Sanyo Head for VTC9300/9500	41.50
Sanyo Head for VTC 5300/5000	41.50

SANYO ORIGINAL VIDEO PARTS

SANYO ORIGINAL PART NUMBER	MODEL	DESCRIPTION	
4-529-10800B	VTC5150	Reel Motor 3.6W	9.95
4-527T-23501	VARIOUS	Motor Assy.	9.75
4-527V-51000	5150	Capston Motor	29.95
143-0-4904-00900	FVHP615	Gear Idler Assy	5.95
143-2-457T-05900	VTC9455	Stopper Reel Base	0.55
143-0-545T-01701	VARIOUS	Pinch Roller Assy.	8.95
143-0-545T-01700	VARIOUS	Pinch Roller Assy.	1.95
143-0-551T-VTC9300		Idler Assy.	0.95
143-0-661T-03800	VARIOUS	Loading Roller	0.95
143-0-662T-01201	VTC5150	Reel Drive Pulley	8.50
143-0-9974-00100	FVHP615	Mod Kit IC BA6304A	1.95

Video Head Cleaning Tape (VHS Automatic wet/dry)	6.50
Video Head Aerosol Cleaner	0.85
Video Copying Lead and Connector Kit 'Z/V'	7.95

VIDEO ALIGNMENT TAPES

S-2P Colour Bars 30 min.	49.50
S-3P Stairsteps 30 min.	49.50

E H T MULTIPLIERS

ITT CVC20	6.35
ITT CVC30	6.35
PHILIPS G8.550	6.96
RANK T20A	6.91
THORN 3000/3500	7.57
THORN 8500	8.00
THORN 9000	8.00
UNIVERSAL TRIPLER	5.45

VARICAP TUNERS

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ELC1043/06 MULLARD	8.65
U321	8.25
U322	8.25
U324	11.00

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DECCA, ITT, CVC20 6WAY	7.95
ITT VCV5-7-WAY	10.19
PHILIPS G8 (550) 6-WAY	14.49

200MA QUICK BLOW FUSES

100MA	8p each
200MA – 5 AMP	5p each

THERMISTORS

VA1040	0.23
VA1056S	0.23
VA1104	0.70
VA8650	0.45
VA1097	0.25

20MM ANTI SURGE FUSES

100MA-800MA	15p each
1A-5AMP	12p each

REPLACEMENT ELECTROLYTIC CAPACITORS

DECCA 30(400-400/350V)	2.85
DECCA 80/100 (400/305V)	2.99
DECCA 1700 (200-200-400-350V)	3.55
GEC 2110 (600/300V)	2.25
ITT CVC20 (200/400V)	1.80
PHILIPS G (600/300V)	2.25
PHILIPS G9 (2200×63V)	1.19
PHILIPS G11 (470/250V)	2.35

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HEAT SINK COMPOUND	1.00	PUSH PULL MAINS SWITCH (DECCA, GFC, RANK, THORN ETC.)	1.02
FREEZE IT	0.95	PYE IF GAIN MODULE	6.99
SOLDA MOP	0.64	ANODE CAP (27kV)	0.69
SWITCH CLEANER	0.85		
WD40	1.75		

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63	1.20
A41	22.50
A42	17.50
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AF96	0.65
C70	1.75
C90	1.20
CX-4-5000	25.00
ET16	28.50
ET18	28.50
ET22	35.00
ET23	35.00
ET24	39.00
ET25	22.00
ET29	32.00
F91	1.00
F92	0.60
F96	0.65
F97	1.00
H63	1.20
H77	0.90
H79	0.56
H149	2.00
K91	0.90
K92	1.20
L35	2.50
L63	1.00
L70	2.50
L73	1.50
L92	0.95
L93	1.10
L94	2.50
L96	2.50
LS10	13.50
LS16	10.00
M70	1.95
M160	3.50
Y51	1.50
Y86/87	0.65
Y802	0.72
80L	29.50
81L	12.00
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83CC	3.50
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88CC	3.50
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91H	4.50
92CC	3.95
99F	6.99
130L	18.50
182CC	9.00
180F	6.50
186F	8.50
188CC	7.50
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280F	19.50
283CC	10.00
288CC	13.50
E810F	29.50
E1148	1.00
E1524	6.95
EA50	1.00
EA76	1.95
EA79	1.95
EABC80	0.70
EAC91	2.50
EAF42	1.20
EAF801	2.00
EB34	1.50
EB41	3.95
EB91	0.85
EBC33	2.50
EBC41	1.95
EBC81	1.50
EBC90	0.90

EBC91	0.90
EBF80	0.95
EBF83	0.95
EBF85	0.95
EBF89	0.70
EBF93	0.95
EBL1	2.50
EBL21	2.00
EC52	0.75
EC70	1.75
EC81	7.95
EC86	1.00
EC88	1.00
EC90	1.10
EC91	5.50
EC92	1.95
EC93	1.50
EC95	7.00
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ECC32	3.50
ECC33	3.50
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ECC81	1.15
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ECC83 Brimar	1.35
ECC83 Philips	1.95
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ECC83 Tungsram	1.50
ECC84	0.50
ECC85	0.75
ECC86	2.75
ECC88	0.95
ECC91	2.00
ECC180	0.72
ECC189	1.95
ECC801S	3.50
ECC803S	4.95
ECC804	0.60
ECC2000	12.00
ECF80	1.15
ECF82	1.15
ECF86	1.70
ECF200	1.85
ECF202	1.85
ECF801	0.85
ECF805	2.50
ECF806	10.25
ECH3	2.50
ECH4	3.00
ECH35	3.50
ECH42	1.50
ECH81	1.00
ECH83	1.00
ECH84	1.00
ECH2000	1.50
ECL80	0.60
ECL82	0.79
ECL83	2.50
ECL84	0.74
ECL85	0.69
ECL86	0.95
ECL805	0.69
EF37A	2.50
EF39	1.50
EF40	4.50
EF41	3.50
EF42	3.50
EF50	2.50
EF55	4.95
EF70	1.20
EF71	1.50
EF72	1.20
EF73	1.00
EF80	0.55
EF83	3.95
EF85	0.50
EF86	2.25
EF86 Mullard	4.50
EF89	1.50
EF91	1.95
EF92	2.15
EF93	0.95
EF94	0.95
EF95	1.95
EF97	0.90
EF98	0.90
EF183	0.65
EF184	0.65
EF730	1.80
EF731	3.50
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EF800	11.00
EF804S	19.50
EF805S	13.50
EF806S	14.50
EF812	0.65
EFL200	1.50
EH90	0.72
EK90	0.95
EL32	0.95
EL33	5.00
EL34	2.25
EL34 Mullard/Philips	4.50
EL36	1.95
EL37	9.00
EL38	6.50
EL41	3.50
EL42	2.00
EL81	6.95
EL83	5.95
EL84 Brimar	0.95
EL84 Mullard	2.95
EL85	4.50
EL86	1.25
EL90	1.75
EL91	6.00
EL95	1.75

EL153	12.15
EL183E	3.50
EL18P	3.50
EL360	6.75
EL500	1.40
EL504	1.40
EL509	5.25
EL519	6.95
EL802	3.65
EL821	8.50
EL822	12.95
EM1	9.00
EM4	9.00
EM80	0.70
EM81	0.70
EM84	1.65
EM85	3.95
EM87	2.50
EN32	15.00
EN91	1.95
EN92	4.50
EY51	0.80
EY81	2.35
EY83	1.50
EY84	5.95
EY86/87	0.50
EY88	0.55
EY91	5.50
EY802	0.70
EX35	0.75
EZ40	2.75
EZ41	2.75
EZ80	0.75
EZ81	0.75
EZ90	1.50
F606	2.95
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G55/1K	9.00
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GC10B	17.50
GC10D	17.50
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GC10/4E	17.50
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GD86W	6.00
GDT120M	5.00
GN4	6.00
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GR10G	4.00
GS10C	16.50
GS10H	12.00
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GT1C	14.00
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GTN175M	8.00
GTR150W	1.00
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GY501	1.50
GY802	1.50
GZ30	1.50
GZ31	1.50
GZ32	1.50
GZ33	4.50
GZ34	2.15
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HAA91	1.00
HABC80	0.90
HBC90	0.75
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HF93	0.75
HF94	1.50
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HL2K	4.95
HL23DD	4.00
HL41	3.50
HL42DD	3.50
HL90	0.70
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HL133×DD	3.50
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KT44	4.00
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KT66 USA	9.95
KT66 GEC	17.50
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KTW61	2.50
KTW62	2.50
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L102/2K	6.95
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LB7-20	95.00
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M502A	60.00
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M5143	155.00
M8079	6.00
M8082	7.50
M8083	3.25
M8091	7.50
M8096	3.00
M8098	5.50
M8099	5.00
M8100	5.50
M8136	7.00
M8137	7.95
M8161	6.50
M8162	5.50
M8163	5.50

M8190	4.50
M8195	6.50
M8196	5.50
M8204	5.50
M8223	4.50
M8224	2.00
M8225	3.95
ME1401	29.50
ME1402	29.50
ME1501	14.00
MH4	3.50
MHL6	4.00
ML4	4.50
MS4B	5.50
MU14	3.50
MZ1-100	125.00
N37	12.50
N78	9.85
OA2	0.85
OA2WA	2.50
OA3	2.50
OB2	0.85
OB2WA	2.50
OC2	2.50
OC3	1.50
OD3	1.70
OM4	1.00
OM5B	3.00
OM6	1.75
ORP43	2.50
ORP50	3.95
P61	2.50
P41	2.50
PABC80	0.75
PC86	0.75
PC88	0.75
PC92	3.50
PC97	1.10
PC800	1.10
PC900	1.25
PCC84	0.40
PCC85	0.55
PCC88	0.70
PCC89	0.70
PCC189	0.70
PCC805	0.70
PCC806	0.80
PCE82	0.80
PCF80	0.65
PCF82	0.60
PCF84	0.65
PCF86	1.20
PCF87	0.40
PCF200	1.80
PCF201	1.80
PCF800	0.40
PCF801	1.35
PCF802	0.60
PCF805	1.25
PCF806	1.00
PCF808	1.25
PCH200	1.50
PCL82	0.85
PCL83	2.50
PCL84	0.75
PCL85	0.80
PCL86	0.85
PCL800	0.80
PCL805	0.90
PE1-100	69.00
PEN25	2.00
PEN40DD	2.50
PEN45	3.00
PEN45DD	3.00
PNE46	2.00
PE06-4oN	42.00
PFL200	0.95
PL21	2.50
PL36	0.95
PL38	1.50
PL81	0.72
PL81A	0.72
PL82	0.60
PL83	0.52
PL84	0.78
PL88	1.00
PL95	1.75
PL302	1.00
PL345	12.50
PL500	1.10
PL504	1.15
PL508	1.75
PL509	4.85
PL519	4.95
PL802T	3.50
PL820	2.95
PL5557	29.50
PY32	0.60
PY33	0.50
PY81	0.70
PY82	0.70
PY83	0.70
PY88	0.65
PY500A	1.95
PY800	0.79
PY801	0.79
QB3-300	54.95
QB3-1750	139.50
QB5-3500	495.00
QE03-10	4.95
QE08-200	145.00
QF40	65.00
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QQE02-5	19.50
QQE03-12	7.95
QQE03-20	35.00
QQE06-40	45.00
QQV02-6	19.50
QQV03-10	5.50
QQV03-10 Mullard	15.00
QQV03-20	25.00
QQV06-40A	27.50
QQV06-40A Mullard	45.00
QQV07-50	63.50
QQZ03-20	42.50
QS75/20	1.50
QS75/40	3.00
QS92/10	5.00
QS95/10	4.85
QS108/45	4.00
QS150/15	6.95
QS150/30	1.15
QS150/45	7.00
QS1200	3.95
QS1202	3.95

QS1203	4.15
QS1205	3.95
QS1206	1.05
QS1207	0.90
QS1208	0.90
QS1209	3.15
QS1210	1.50
QS1211	1.50
QS1212	3.20
QS1213	5.00
QS1215	2.10
QS1218	5.00
QU37	9.50
QV03-12	5.75
QV05-25	1.75
QV06-20	29.50
QV08-100	145.00
QV2-2500	45.00
QY3-125	65.00
QY4-250	70.00
QY4-400	76.00
R10	4.00
R16	12.00
R17	1.50
R18	2.50
R19	2.50
R20	1.20
R1169	55.00
RG1-125	4.95
RG1-240A	14.50
RG3-250A	3.50
RG3-1250A	35.00
RK2K25	62.50
RK-208	12.00
RL16	1.50
RPL16	12.00
RPY13	2.50
RPY43	2.50
RPY82	2.50
RR3-250	15.00
RR3-1250	35.00
RS613	45.00
RS685	54.95
RSS688	52.15
S6F17	5.95
S6F33	28.95
S11E12	38.00
A30/2K	12.00
S104/1K	10.00
S109/1K	15.00
S130	5.59
S130P	5.95
SC1/800	6.00
SC1/1100	6.00
SC1/1200	5.00
SC1/1300	6.00
SC1/200	9.00
SP41	5.00
SP42	3.00
SP4B	4.95
SS501	35.00
ST11	1.50
STV280/40	11.95
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Trends in the 68000 family

Consistent structure makes the 68000 family architecture easy to learn and program.

DAVID BURNS AND DAVID JONES

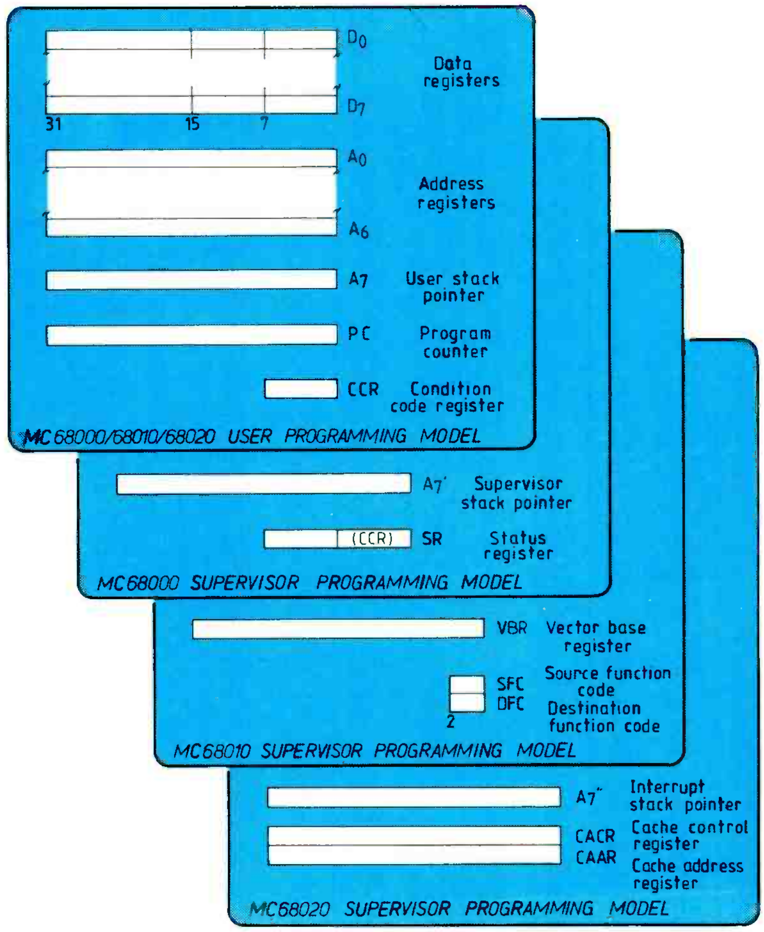


Fig.1. Programming model for the 68000. There are sixteen 32-bit general-purpose registers, a 32-bit program counter and an eight-bit condition-code register. The seven address registers and the stack pointer may be used for long-word operations and all 16 registers may be used as index registers.

At its introduction in 1979 the 16/32-bit MC68000 represented a break away from traditional accumulator-based microprocessors, its general-purpose architecture being more akin to that of a modern minicomputer. Now the family includes upwardly-compatible devices with such features as virtual memory, 32-bit data buses and instruction caches.

The MC68000 was Motorola's first 16 bit microprocessor. Internally its architecture is 32 bits with an external data bus of 16 bits and external address bus of 24 bits. Programming model Fig. 1 shows the MC68000 architecture, which is of a general purpose nature with eight data registers D_{0-7} and seven address registers A_{0-6}. When combined with the 56 basic instructions and 14 addressing modes, these registers provide many thousands of possible instruction operations.

Fundamental to the design of the M68000 family is the definition of user and supervisor modes. This is supported internally by the provision of separate stack pointers for both the user mode (A_7) and the supervisor mode (A_7'). The concept of the user/supervisor split results in the situation wherein user code can only access a certain range of "non-privileged" instructions.

Additional instructions, which can be used to alter system states such as interrupt masking and tracing, can only be executed in supervisor mode. In an operating-system environment this means that only the most reliable code – the kernel for example – executes in the supervisor state and all other code executes in user mode.

Instruction sequencing on the M68000 is performed by a collection of microcoded operations stored in internal rom areas called microroms and nanoroms. Unlike random-logic decoding, this instruction microcoding allows the processor to have a predictable outcome for all possible instructions and operations. This provides a secure system with the ability to detect errors such as illegal instructions or divide by zero and handle these using exception handling within supervisor mode. Security provided by these features is especially important in modern operating systems such as Unix.

Externally the user/supervisor split is also supported in hardware via three function pins. Encodings on these pins indicate user data or program, supervisor data or program and c.p.u. space, Fig.2. Control functions such as interrupt acknowledge use c.p.u. space. Again a level of security can be implemented via the function codes by using them in the memory decoding. This can allow an area of supervisor data space to be protected against accesses from an executing user program which could possibly run out of control and corrupt the supervisor data. A situation like this could well cause a catastrophic system failure if a level of protection was not provided.

68010 ADDS VIRTUAL-MEMORY PROCESSING

Production of the MC68010 meant the addition of a virtual-memory (v.m.) 16/32-bit microprocessor to the 68000 family. Virtual memory has existed for a number of years in main-frame and indeed mini computers. The MC68010 is an enhanced version of the MC68000 with additional on-chip hardware and microcode for the v.m. facility.

A virtual-memory computer system is one in which the user appears to have access to a very large processor addressing range while in fact only a small proportion of this range may be physically present. Implementing a virtual-memory (v.m.) system allows a microprocessor-based computer to be designed with a small amount of high-speed,

Function codes FC2	FC1	FC0	Memory/peripheral access
0	0	0	Reserved for future enhancements
0	0	1	User data space
0	1	0	User program space
0	1	1	Reserved for user definition
1	0	0	Reserved for future enhancements
1	0	1	Supervisor data space
1	1	0	Supervisor program space
1	1	1	c.p.u. space

Fig.2. Function code outputs. These signals indicate the mode, user or supervisor, and the cycle type currently being executed.

expensive silicon memory and large amounts of v.m. on cheaper magnetic-storage devices. When a location in virtual memory is accessed which is not present in the physical memory, the access must be suspended until the information is presented to physical memory from backup memory.

When the 68010 accesses a memory location outside physical memory a bus-error signal should be generated and passed to the processor. This causes the program register contents and all processor internal-state information to be placed on the supervisor stack. This fault address, caused by the memory-management unit selecting a new area of virtual memory, makes the processor enter a bus-error software handling routine. The user can then find the fault address on the stack and initiate a replacement algorithm using i/o hardware such as a direct-memory access controller to fetch data from backup memory into physical memory. On leaving the bus-error handler, the faulted instruction is continued from where the fault occured as the information can now be found in the physical memory.

Three new registers have been added to the 68010 supervisor programming model as shown in Fig.1. The vector-base register, VBR, is used to offset the position of the interrupt and exception-vector table to any memory space in the processor address range. The alternate function-code registers for source (SFC) and destination (DFC) data transfers allow the supervisor program to pass privileged data to the user programs.

Supervisor mode has also been enhanced to allow full implementation of virtual-machine operation. Virtual machine operation is a mechanism by which a number of operating systems can be run on the same processor, all controlled by the governing operating system which is the only one running in supervisor mode. Each general operating system appears to the user as if it were executing in supervisor mode but in actual fact it is running in user mode, being controlled by the governing operating system.

PIPELINING INCREASES PROCESSING EFFICIENCY

The MC68020 contains a 256-byte direct-mapped instruction cache to improve performance. Instruction accesses to the cache are performed in two cycles as opposed to a minimum of three cycles when an external memory operation is performed. Op-codes fetched from the cache are therefore loaded into the pipeline one cycle earlier than from external memory and so instruction decoding takes place that much sooner.

Control of the cache is provided by the functions of the cache enable/disable, cache-freeze and clear-entry facilities. Cache freeze is of particular interest in applications where there is a time-critical section of code. The relevant section of code can be frozen into the cache, i.e. there will be no need to fetch instructions from external memory, and this will provide a very fast processor-bound software function. By making full use of the general-purpose address and data registers within the processor a considerable increase in performance can be achieved by removing any need to access external memory.

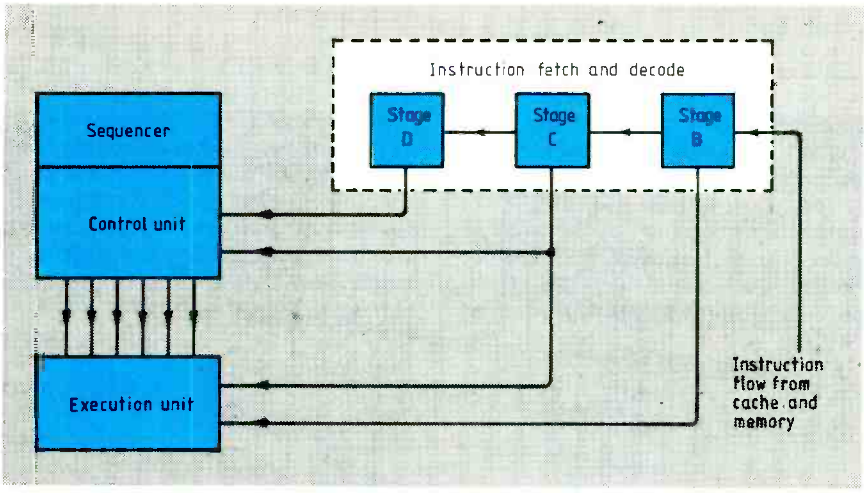


Fig.3. Pipelining greatly increases the device's instruction processing ability by allowing various functions to be executed concurrently.

Internal operations of the processor are not stopped if the device is halted or arbitrated from the bus. Applications can be configured to allow other system activity, such as disk i/o *via* d.m.a. when the processor is performing a long computational sequence where the instructions will be fetched from the cache and the arithmetic operations will be performed on the internal registers.

Paramount to the performance of the MC68020 is the pipeline structure, Fig.3, which greatly increases the processor's instruction processing efficiency. The basic pipeline consists of three stages (B,C and D) each of which has its own particular function and associated a.l.u. Stage B of the pipeline is associated with effective-address calculations and extraction of embedded operands. Stage C performs the initial instruction decoding for the nano and micro roms, and stage D completes instruction execution.

Processing in separate areas of the pipeline is done concurrently. For example an instruction may be performing its final write to memory concurrently with another instruction's prefetch from the cache. This concurrency not only increases the data throughput but also decreases overall instruction execution time.

Having a three-stage pipeline means that several different instructions can be executed in parallel. Because of the nature of the sequencer and bus controller, execution of adjacent instructions can overlap, i.e. the data bus activity of one instruction can overlap the internal execution of the next instruction. This situation can easily arise where the total execution time of the second instruction is completely absorbed by the first instruction, resulting in a zero clock-cycle execution time for the second.

The overlap situation most often occurs when processor-bound instructions follow memory write instructions, as for example in

MOVE.L D4,(A1); move data register to address pointed by A_1.

ADD.L D3,D5; add data registers D_3 and D_5, result in D_5

where the ADD will be completely absorbed by the data write associated with the MOVE instruction. While the bus controller is performing the write to (A_1) the sequencer will complete the internal execution of the ADD instruction.

ON-CHIP CACHE MEMORY

The cache on the MC68020 is an area of very fast, on-chip memory which allows the processor to access instructions faster than it could by going to external memory. The MC68020 has a 256 byte on chip cache, which is organized as 64 long-word entries.

This cache is developed as a direct-mapped architecture which means that the lower portion of the address bus (A_{2-7} in the case of the MC68020) is used to "directly" index into one of these 64 entries ($A_{0,1}$ are not needed to address long words). The fact that the cache index is so small (only up to address line A_7) means that the cache will be multiply mapped throughout the whole memory map of the processor which is 4 gibabytes in the case of the 68020.

When an instruction is fetched from external memory an entry is also made in the on-chip cache. On making this entry, the processor also stores a copy of the upper section of the address bus which is referenced as the TAG field to the actual stored data item.

When this address is next accessed the processor is able to compare the stored TAG with the present address – bus state to determine whether the required instruction is in the cache. If this comparison is valid then the processor reads the instruction directly out of the on-chip cache without the need to go to external memory.

To fully utilise the on-chip cache, areas of code which need to be executed quickly can be written as loops. The first time through the loop the instructions will have to be fetched from external memory but they will be copied into the on-chip cache. On subsequent loops of the code these instructions will be found in the cache; the processor will not need to go to external memory and execution time for the loop will be reduced considerably (a fetch from the cache takes two cycles whereas a fetch from external memory takes a minimum of three cycles). Use of an on-chip cache can therefore greatly increase the overall system performance.

THE COPROCESSOR INTERFACE

A 32-bit computer design may incorporate not only a 68020 processor but also processing elements of equal complexity. These additional complex processors, or coprocessors, provide a logical extension to the microprocessor features. To simplify the interface of coprocessors to the 68020, in addition to other benefits, the 68000 coprocessor interface was integrated into the chip. Coprocessors with the 68000 interface protocol create a very efficient system. The m.p.u. and coprocessor are so tightly coupled that the user is never aware that the functions are on separate chips.

The method of communication with a coprocessor over the coprocessor interface is defined by the coprocessor protocol. The protocol uses standard 68000 bus cycles and therefore no additional external hardware need be used. In addition the 68020 can be designed for asynchronous bus operation, allowing different clock speeds, and so the m.p.u. or coprocessor can be optimized for maximum system performance.

Communication with a coprocessor is similar to communication with a peripheral except that instead of communicating over normal address space, c.p.u. address space is accessed (all functions codes equal to one). Within this c.p.u. address space an area of memory is reserved for up to eight coprocessor sets of memory-mapped registers called coprocessor-interface registers (CIR). All communication between the m.p.u. and a coprocessor is done through the CIR set for each coprocessor.

The m.p.u. and coprocessor operate together as follows: the m.p.u. fetches and stores operands, calculates effective addresses and handles any traps for the operating system when errors or exceptions occur. The coprocessor on the other hand understands its own instructions, knows what and how much data it needs, determines concurrency and synchronization and initiates operating system traps.

Benefits of such a system are many. Integration of the processor and coprocessor is simplified. Secondly, the coprocessor can act as a peripheral for other M68000 family members or other processors, and system designers can design their own coprocessor to perform a dedicated function, for example a graphics controller. Finally coprocessors can be used to extend the instruction set of the MC68020 in specific applications. Concurrent operation between m.p.u. and coprocessor is possible.

At present Motorola has two 32-bit coprocessors for the 68020, namely the MC68881 floating-point coprocessor and the MC68851 demand-page memory-management unit (m.m.u.). The 68881 implements the full IEEE standard for binary floating-point arithmetic (P754) and a full set of trigonometric and transcendental functions is included. The 68851 can form part of a paged virtual-memory system with the MC68020 m.p.u.

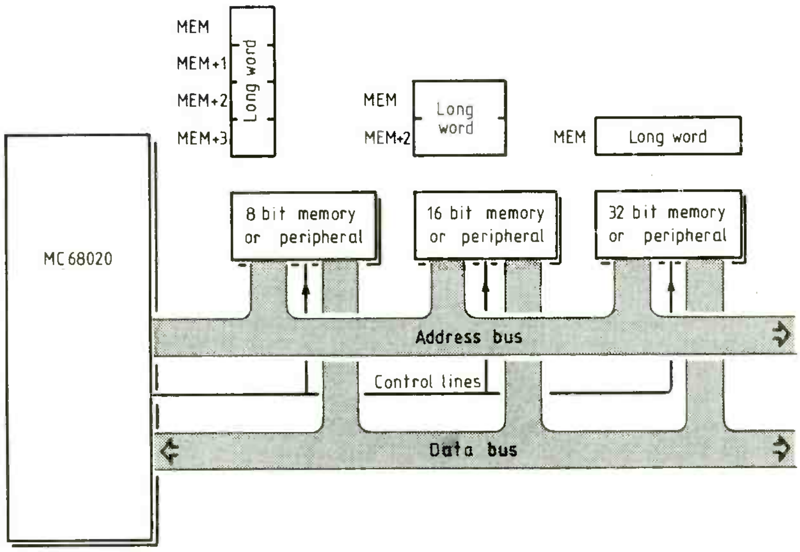
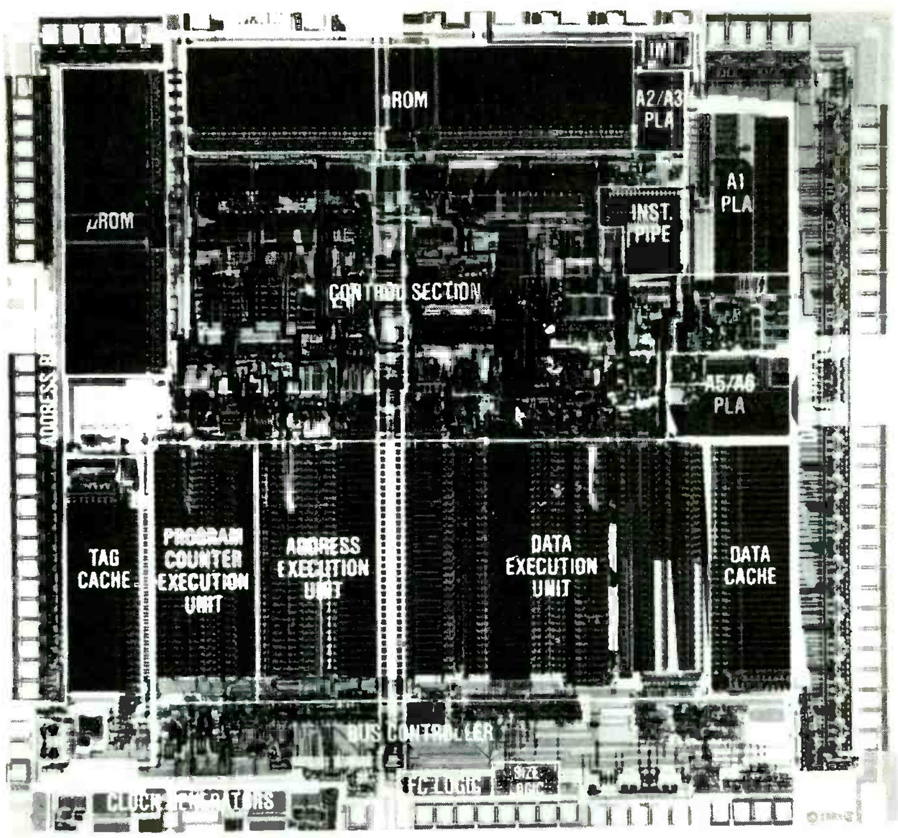


Fig.4. Dynamic bus sizing allows peripherals with different sized buses to be used on the 32-bit bus.



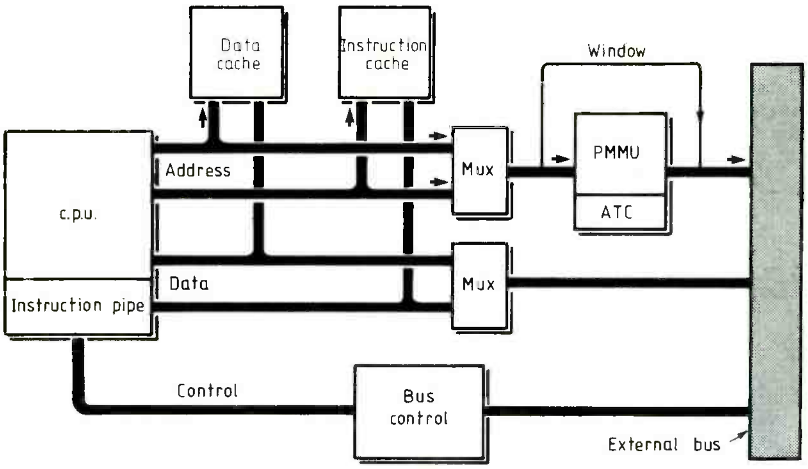
In the 68020, on-chip memory is used so that instructions can be executed without using external memory. This speeds up execution time.

DYNAMIC BUS SIZING

Dynamic bus sizing is used in the 68020 to alleviate the hardware/software problem associated with device size and its relevant bus size. The 68020 automatically performs byte, word or long-word operations to any size device or bus whether 8, 16 or 32 bits. As a simple example, consider a long-word write (32-bit) to a byte-sized device (8-bit) using for example MOVE.L D4, (A1). With the aid of bus signals, the 68020 is able to detect the 8-bit device and automatically perform four consecutive byte writes to the device while sequencing through the relevant address to give the correct byte offset within the long word. The processor performs this automatically without affecting user software.

In addition to dealing with different sized devices, dynamic bus sizing also takes care of data misalignment within memory. Again, considering an example the method will become clearer, Fig.4. If the processor is performing a long-word read from 32-bit memory but the address is not on a long word boundary, e.g. 2003_{16}, then the processor will automatically perform two consecutive reads to get information. The most

68030 DOUBLES ITS PREDECESSOR'S PERFORMANCE



The most recent introduction to the 68000 family is a second-generation 32-bit processor, the MC68030, with a higher level of integration. This device has all the features of, and is upwardly compatible with, the 68020 but it includes enhancements that more than double its performance. These features are enhanced parallel operation, dual burst-fillable caches, dual internal data and address buses, improved bus interfacing and paged memory management.

The 68030 is the first 32-bit processor to include both on-chip instruction and data caches. These independent caches incorporate a burst-fill mode for taking advantage of the shorter access times that are possible with paged-mode, nibble-mode and static-column d-ram technology.

Internally the processor has a Harvard-style architecture with two independent 32-bit address and data buses so the c.p.u., caches, memory management unit and bus controller can operate in parallel. As a result, the 68030 can simultaneously access instructions from the instruction cache, data from the data cache and an instruction or data from external memory.

Compatibility with the 68020 is maintained by incorporation of an asynchronous bus interface (minimum three clock cycles) with support for dynamic bus sizing. In addition, the device operates a new synchronous bus interface (minimum two clock cycles) for faster access to any external cache subsystems. This synchronous bus interface can also be linked to the burst-fill mechanism for very rapid filling of the internal caches (minimum one clock cycle). Dynamic configuration of these buses is possible on a cycle-to-cycle basis which increases flexibility.

The result of integrating memory-management unit in a device with Harvard-style architecture is that logical-to-physical address translations are hidden by concurrent cache accesses. System degradation due to memory-management-unit translations is therefore eliminated. The memory-management unit in the 68030 is a version of the 68851 paged m.m.u.

Harvard architecture involves the use of separate data and address buses for data and instructions within the processor. This increases bus bandwidth.

significant byte will be fetched by a long-word read from a base address of 2000_{16} and the least-significant three bytes will be fetched by a long-word read at a base address of 2004_{16}. Internally the processor has demultiplexing circuitry to route the relevant section of the data bus to the relevant section of a register.

IMPROVED INSTRUCTION SET

New software instructions have been added to the 68020 and all source-code is upwardly compatible with other 68000 family members. For the compiler writer, and ultimately the user of high-level languages, powerful instructions have been added. These instructions make the manipulation of strings, arrays and other data types much more efficient. This manipulation can also be made more precise by using the new addressing modes to extract a single data element of a data type (arrays records, strings etc.)

With these additions to a high-level language compiler, optimized assembly-language code can be produced, hence improving speed and performance. As the trend today is toward high-level language software development for microprocessors, this is an important feature.

Expanding from 16 to 32-bits was not seen as simply expanding the width of the data bus. Most of the instructions have been enhanced to operate on 32 bits of data or use 32-bit offsets. Arithmetical instructions include a 64-by-32-bit divide and a 32-by-32-bit multiply to give a 64-bit result. A 32-bit 'barrel shifter' allows between 1 and 32-bits of data to be shifted in a data register in a single clock cycle.

Multiprocessor applications are simplified by inclusion of two additional read-modify-write instructions for enhanced semaphore addressing. A range of bit-field instructions has been added to permit complex bit-mapped graphics applications. With the new addressing modes and instructions, the 68020 can be made into a dedicated graphics processor with little difficulty.

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How linear is linear

continued from page 97

called intermodulation and one measure of the intermodulation performance of a mixer is to find the ratio of the unwanted third order intermodulation product to the linear output, when two signals of amplitude S are applied at the input. If an amplifier has a transfer function of the form.

$$V_{OUT}=a_1V_{IN}+a_3V_{IN}^3$$

then it can be shown that this ratio is given by

$$r=\left|\left(\frac{3}{4}a_3.S^3\right)/(a_1S)\right|$$

$$=\left|\frac{3a_3}{4a_1}\right|.S^2 \qquad (11)$$

The third-order two-tone input intercept (closely related to the dynamic range of the mixer) is defined as the value of S for which the third-order intermodulation product is equal in amplitude to the wanted linear output, ie.

$r=1$

$$S_{intercept}=\left|\frac{4a_1}{3a_3}\right|^{1/2} \qquad (12)$$

Thus, for a mixer circuit using the linearized long-tail pair at the signal input,

$$S_{intercept}=(I_LR+2V_T)^{3/2}/(V_T/2)^{1/2} \qquad (13)$$

At first sight it appears from equation (13) that by increasing I_LR we should be able to make the intercept level as high as we please, but there is a price to be paid for improved intermodulation performance. I_L can only be increased within the limits of transistor maximum collector current and power dissipation. I_LR can only be increased further by increasing R. However, as R is increased, the Johnson noise generated in the resistor itself may become the most significant contribution to the effective noise level seen at the input to the linearized long-tail pair. Thus the intermodulation performance may only be improved within the limit imposed by the noise level which is acceptable in a particular application. In a mixer in the front-end of a communications receiver the acceptable noise level may be relatively low.

Reference

1. W. Hayward and D. DeMaw, "Solid State Design for the Radio Amateur", American Radio Relay League, 1977, Appendix 3.

The author graduated in physics at Oxford in 1983, specializing in electronics. He now examines applications for semiconductor device patents at the European Patent Office in the Hague.

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Our contribution this month comes from Barry Seward-Thompson, who is Principal of DECollege, Digital Equipment Company

Attitudes in the IT industry - the key to the future

Information technology, in both its broadest meaning and as applied specifically to business computer systems, is adopting a different role in our business lives and as a consequence will have a different influence on the way we work in the future. In the past, users of computers and related systems such as word processors have had to have a specific knowledge of either the system itself or the software running on it to make it operate. Even relatively recently, a computer system would be ordered on the basis that it was the closest fit to a company's requirements and that working practices and individuals' skills would need to change to accommodate the system.

This position is now changing. In the future, workers will expect computers to be a benefit to them and will not expect - nor should they need - to know in detail how the system works. More importantly, the user will be very much more aware that the benefits of IT exist and are there to be tapped - the best recent example of this of course being the automation of the Stock Exchange in London and the use of IT products to effect the changes in the transactions that are performed. Additionally, the user will expect that the system to meet his or her needs exists and will be unconcerned with the actual manufacturer other than that they provide the benefits he demands as part of his working life (who knows or cares how a telephone exchange works?).

ATTITUDES, NOT SKILLS

As a manufacturer and supplier of computer systems, DEC has realized that to remain competitive and to ensure that people buy our computers and not our competitors', a crucial change in our own requirements for personnel and their skills is needed for the future. With specific exceptions (such as engineering), we will not need people with specific IT skills - i.e. programming, detailed knowledge of computer architectures and so on. What we will need are people who can communicate with our customers, interpreting their needs for the system specifiers, who can educate our customers in the benefits of IT, can appreciate the role of IT generally in the business world and can complement this with a willingness and ability to face change with flexibility. In short, we will be looking for the correct attitude, not the correct formal skill-based qualification.

It is to meet this need that I was asked to create DECollege within DEC with a brief to ensure that the future growth of DEC in this country is not constricted by any lack or shortage in the type of people we will need. In other words, people with what we perceive to be the correct skills and attitudes must be available internally or externally whenever we require them. DECollege is not a building but a "virtual" college acting as a consultancy to DEC's line managers - who have responsibility for their future staffing requirements - and which acts to promote both external and internal training, and awareness programmes.

HIGH GROWTH, GREATER DEMANDS

DECollege is particularly needed because DEC is in a very high-growth industry. Needs are therefore changing more rapidly than in other industries and this has brought about a long term focus on the future.

As I have already mentioned, the computer industry originally started with the provision of computer systems which users then applied to the best of their ability. The systems were not specific to particular needs nor did the software available cope with the demands of the user. Now, the working and business population has absorbed IT and demands the benefits it can give. In the future, therefore, we will need a flexible, application-oriented approach to the customer and not a technical one. We will need people with an ability to appreciate a user's business needs and have these converted into a computer-based solution. The user himself will not care how it works, as long as it does work. And few people in DEC will need a detailed technical knowledge. The principal focus will be on understanding customer problems and the application of IT at a non-technical level.

So what sort of person will DEC be looking for in the future? We will not be looking for specific skills, except, of course in that we will be seeking people with a specific attitude to work, with maturity based on experience in the real world and with a flexible approach to working. The academic training of an individual at school and beyond will be important as an index to the intelligence of that individual, but the specific skill associated with the training will be unimportant. On a broad scale, the individual will need an understanding of IT and how IT relates to business and commerce, not detailed knowledge. An analogy is driving a car - we do not need to know how a combustion engine works to drive it - all we are concerned about is that the ignition key will start it and it will go. The growth of the car industry is not dependent on technical expertise.

Specific skills will be taught as necessary. This training has to be continuous because of the rapid changes in the industry. Initial training becomes a very minor extra investment which is well worth while if the right individual is hired.

Personal qualities of the individual are also important. DEC will be looking for a flexible and positive attitude to work - for instance, that a change of job specification is regarded as an opportunity and a challenge rather than a retrograde step. Indeed, DEC believes that a number of career changes only adds to the qualities of the employee and promotes a career path through the company; and a part of this philosophy emphasizes that sideways movement can be just as positive a step for individual growth as straightforward promotion.

One of the biggest problems facing DEC today is identifying the right people in the crowd. The skill shortage today for companies like ours is not in IT skills but the overall skills and attitudes outlined above - application, maturity and positive attitudes, ideally backed with an outline appreciation of the capabilities of IT. To combat this, we must address the future labour pool: we must start to talk to school children, teachers and parents, explaining the role IT has to play in industry. University students and lecturers must similarly be addressed, although whereas the school level is a broad imparting of information and knowledge, the latter must begin to build relationships through specifics such as courses, student sponsorships and so on. Finally, potential employees in the ranks of the unemployed and redundant need to be identified, assessed, re-educated and re-trained to adopt new responsibilities

A specific example of the last, which supports some of the points I have raised on attitudes, personal qualities and flexibility, is the InterManagement Associates' "Workshop" Project, based in Corby. This project will comprise three computer databases, one on the skills and attributes of unemployed people, the second on the details of jobs available in the so-called sunset industries and finally - and most importantly - the training programmes available and necessary to bridge the gaps between personal attributes and particular jobs.

DEC believes that an overall change is needed in the way companies identify and train their personnel. In DEC, this is the role of DECollege. But on a broader level, the way in which children and students are taught may need revising. In the past, curricula have been criticized for not being biased towards the engineering and science subjects to equip students for the industrial business environment. For the future, with IT becoming all-pervasive, these criticisms need re-assessing. I have already stated that it is not a specific qualification that DEC needs; more important is a level of intelligence, well developed personal attitudes and, most importantly, awareness of business needs. And all courses will need elements of IT introducing as appropriate and on a general level.

To summarize, then, companies such as ours need to think to the future, to ensure our survival in a competitive and continually burgeoning industry. We need to invest in the right sort of staff for our needs and to ensure that moves are made now to build the skills and attitudes we will need then. The skill requirement will change drastically, shifting in the main from academic qualifications to a more rounded experience and outlook. Most importantly, for the average IT user the benefits of IT and a general appreciation of what IT is and what IT can do will be needed rather than a detailed knowledge of programming or systems.

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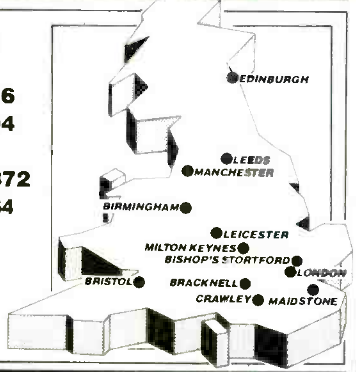

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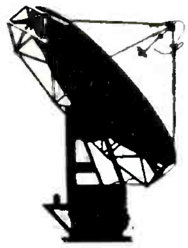

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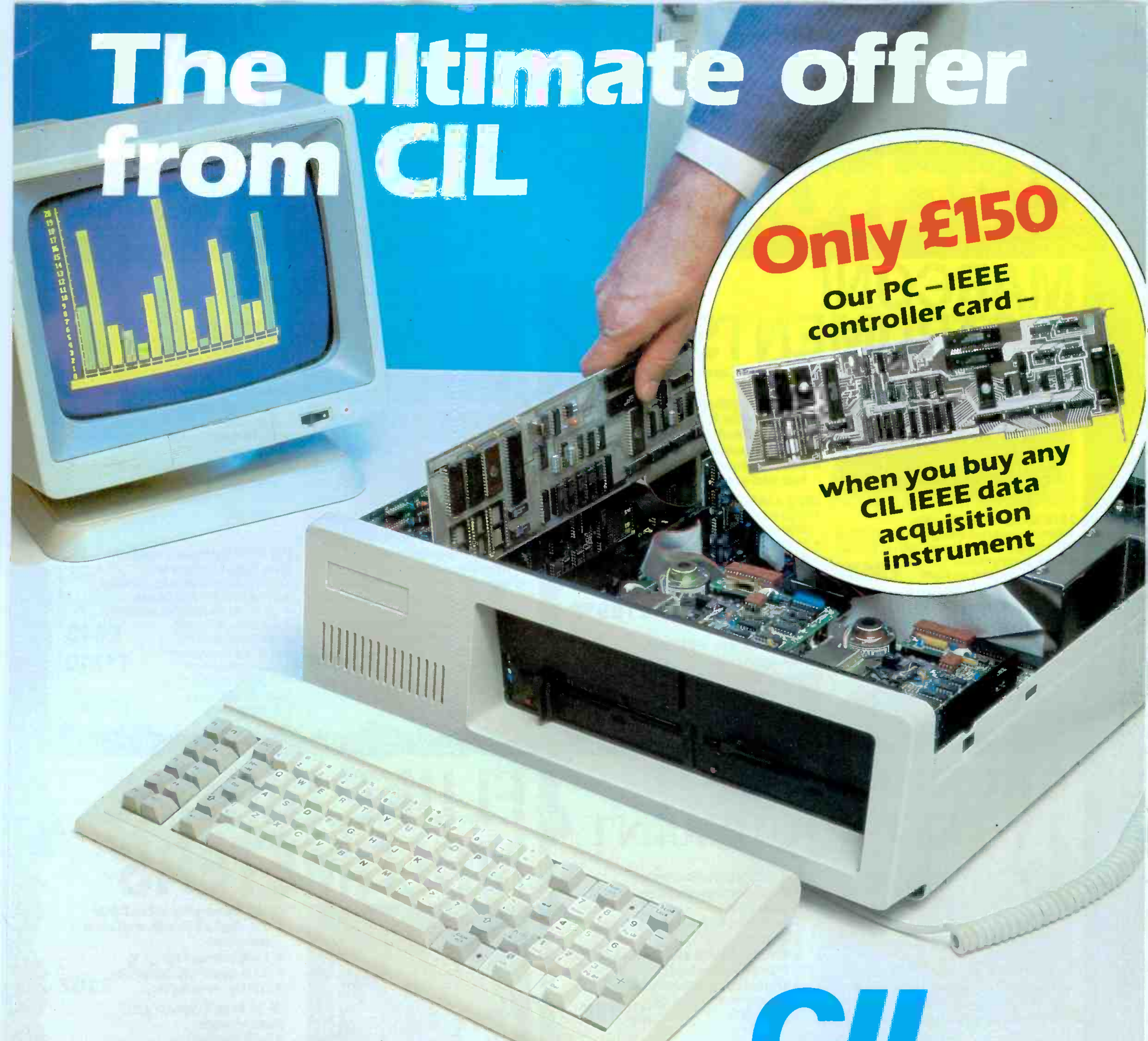

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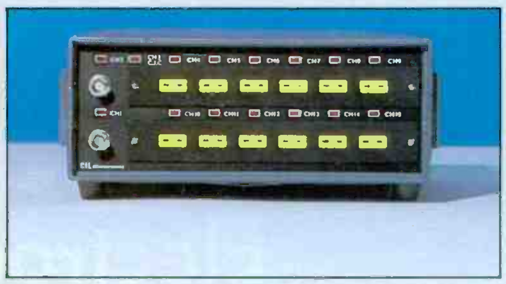

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