NOVEMBER 30, 1981

**IC MAKERS SEEK FOUNDRY BUSINESS FOR IDLE LINES/81**

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Automating IC design, part 2/116

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# Electronics®

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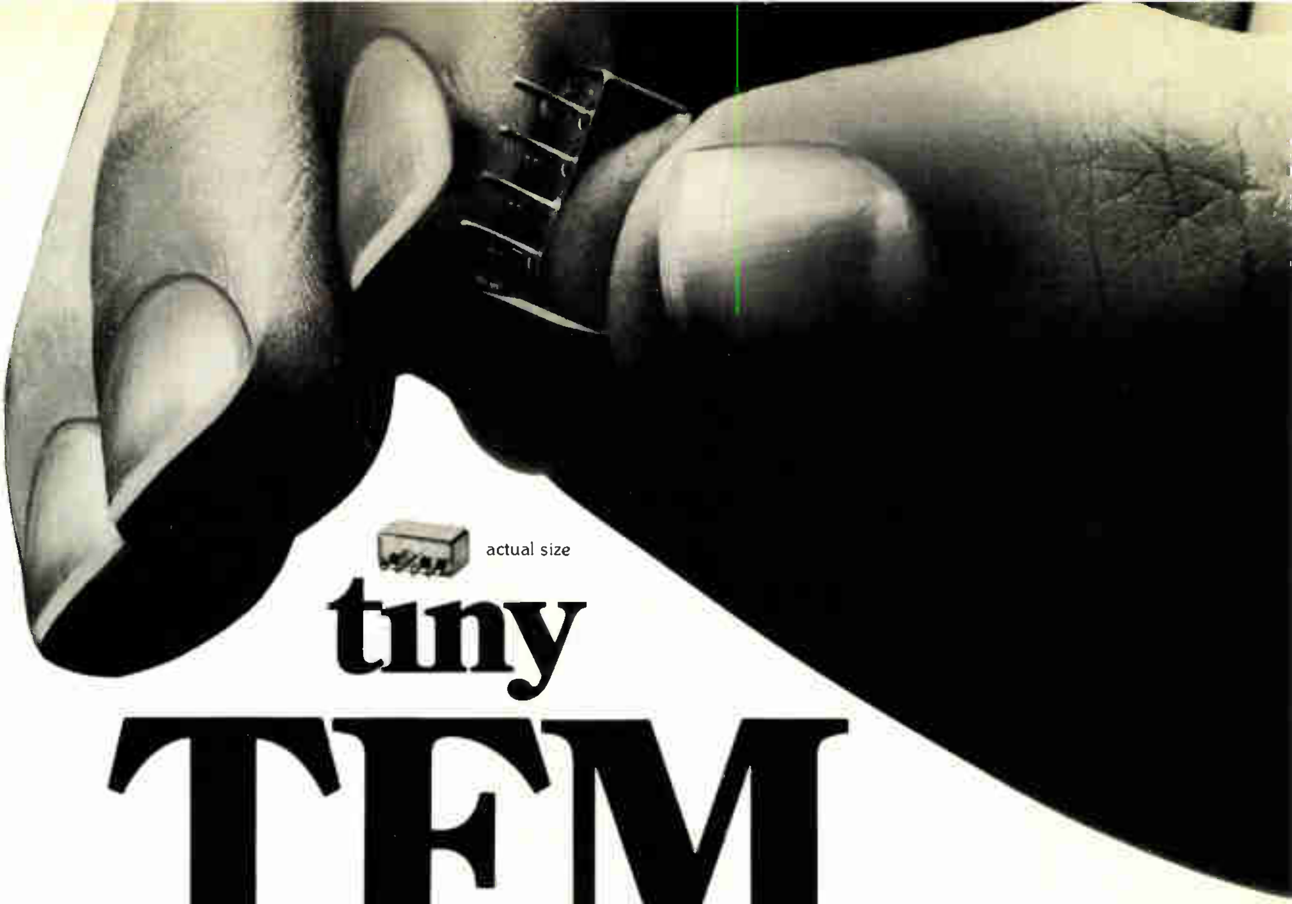

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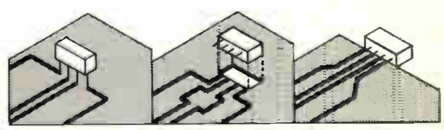


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| Model No. | Frequency Range MHz | | Conversion Loss dB, Typical | | Isolation dB, Typical | | | | | | Price | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | One Octave from | | Lower Band Edge to One Decade Higher | | Mid Range | | Upper Band Edge to One Octave Lower | | $ | |
| | LO/RF | IF | Band Edge | Total Range | LO-RF | LO-IF | LO-RF | LO-IF | LO-RF | LO-IF | EA. | QTY. |
| TFM-2 | 1-1000 | DC-1000 | 6.0 | 7.0 | 50 | 45 | 40 | 35 | 30 | 25 | 11.95 | (1-49) |
| TFM-3 | .04-400 | DC-400 | 5.3 | 6.0 | 60 | 55 | 50 | 45 | 35 | 35 | 19.95 | (5-49) |
| TFM-4 | 5-1250 | DC-1250 | 6.0 | 7.5 | 50 | 45 | 40 | 35 | 30 | 25 | 21.95 | (5-49) |
| •TFM-11 | 1-2000 | 5-600 | 7.0 | 7.5 | 50 | 45 | 35 | 27 | 25 | 25 | 39.95 | (1-24) |
| •TFM-12 | 800 1250 | 50-90 | — | 6.0 | 35 | 30 | 35 | 30 | 35 | 30 | 39. 95 | (1-24) |
| ••TFM-15 | 10-3000 | 10-800 | 6.3 | 6.5 | 35 | 30 | 35 | 30 | 35 | 30 | 49.95 | (1-9) |
| ••TFM-150 | 10-2000 | DC-1000 | 6.0 | 6.5 | 32 | 33 | 35 | 30 | 35 | 30 | 39.95 | (1-9) |

•If Port is not DC coupled
••+10 dBm LO. +5 dBm RF at 1dB compression

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.


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# Electronics

**The International Magazine of Electronic Technology**

**Vol. 54, No. 24 • November 30, 1981**

# Publisher's letter

**The 16-bit microprocessor** pictured on the cover is the largest commercial bipolar circuit ever produced. Fabricating the Am29116 cost Advanced Micro Devices Inc. over three years of development time—and intrigued Microsystems editor Colin Johnson enough to pay a visit to the Sunnyvale, Calif. company that culminated in the article beginning on page 98.

What he found was that the group in charge of AMD's successful bit-slice processor family (built around the Am2901 and 2903) was looking for another project as early as 1978. AMD's customers were remarking that, though the bit-slice parts were adequate for their major applications area—controllers—the chips' microinstruction set was not optimized for it. Also, the great majority of applications were cascading four slices to 16-bit width.

So in defining the 29116 architecture, coauthor Bill Harman designed a part whose microinstruction set was optimized for control, and he also added on-chip hardware modules to greatly enhance throughput. Fortunately, Imox—AMD's advanced oxide-isolated process that uses emitter-coupled logic internally and TTL translators at the pins—became available shortly thereafter, giving the 29116 the speed it needed. When the die size calculations were done, though, "it was huge," admits coauthor Deepak Mithani, senior applications engineer on the project. "But when we evaluated just how the part was going to perform, we decided to go ahead and build it."

It did present AMD's circuit and fabrication engineers with quite a challenge: the 29116 has a microcycle time of 100 nanoseconds and dissipates 3.5 watts. "That's something that they said could not be done three years ago," Mithani adds, "and it proves that bipolar technology is still alive and well."

---

**Four more articles** in our continuing series on automating IC design that premiered last issue begin on page 116. Few of the authors' companies will seem familiar because, as before, many of the firms are start-ups, pioneers in the burgeoning business of supplying tools for design automation. Senior editor John Posa, who rode herd on the series, sees the start-up trend as a natural one, stemming from the needs of the consumer. "Alvin Toffler wrote in 'Future Shock' that one day diversity will cost no more than uniformity," he says. "I've thought about that since we began the series, and it seems to apply directly to the IC industry.

"People have never really wanted standard parts—they've had to settle for them. What they really need is precise solutions to their problems, but the only way to get that has been through handcrafting—which has become prohibitively expensive.

"These articles describe the tools that will soon be in the hands of the system designer," John continues, "like graphics work stations and development systems that allow a circuit function to be swiftly executed in silicon."

## Wanted: a Silicon Valley editor

*Electronics* has a key editorial position open for a journalist who can cover business and technology developments in semiconductors, test and measuring instruments, and computers. Based in our Palo Alto, Calif., bureau, the job requires a newsperson who can build a beat and turn out sprightly copy. A background in engineering or science is desirable, but not mandatory; more important is a desire to report on and write original stories about high technology. We pay competitive salaries with excellent fringe benefits. Write, telling why you are the person for the job, to the Managing Editor (News), at *Electronics*, 1221 Ave. of the Americas, New York, N. Y. 10020.

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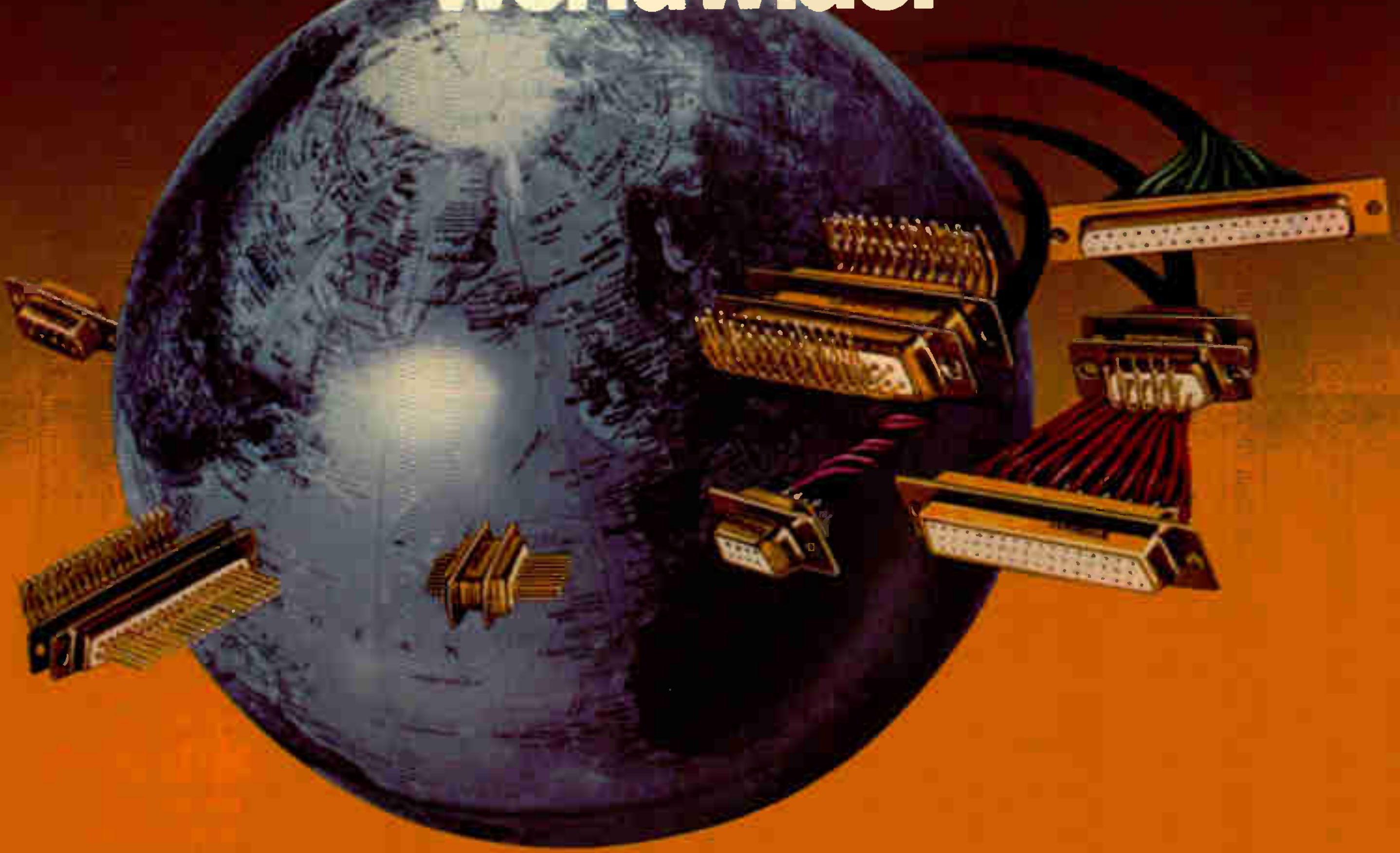

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## News update

■ Back in business after its emergence from Chapter IX of the bankruptcy laws last spring [*Electronics*, April 7, p. 34], R. C. Sanders Technology Systems Inc. is ready to send its first product out the door. Limited deliveries start this month, and volume deliveries in the first quarter 1982, of the Nashua, N. H., firm's S700 letter-quality and graphics matrix printer. A direct descendant of Sanders' original Media 12/7 printer, the S700 uses the same patented process to produce letter-quality as well as draft and correspondence copy in multiple fonts and formats with no change in print head [*Electronics*, April 13, 1978, p. 47].

But if the S700's print technology is an old one for Sanders, it faces new rivals in an increasingly competitive marketplace. Introductions in the past month have included Integral Data Systems Inc.'s Prism printer [*Electronics*, Nov. 17, p. 47], Digital Equipment Corp.'s Letterprinter 100, and Centronics Data Computer Corp.'s Printstation 353.

The S700 is by far the most expensive of these at $3,360, but Sanders vice president David Moros asserts its speed, print quality, and flexibility make it a strong entry.

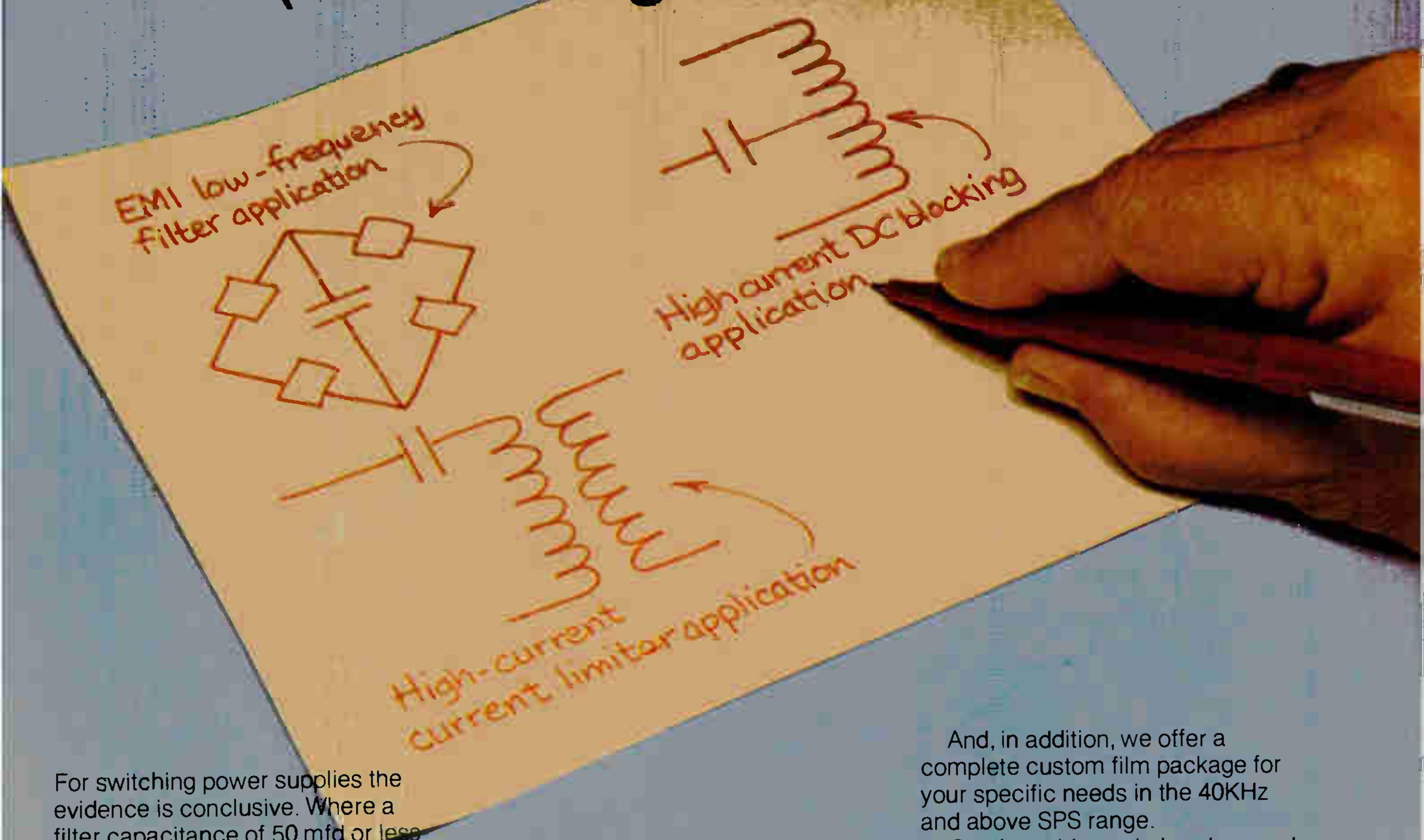
**Faster.** "This printer can run at up to about 300 characters per second in draft mode, and up to 70 cps for letter-quality; that beats the others," Moros maintains. The S700 also can store up to 12 fonts in microprocessor memory for access under host-computer or operator control. "You can intermix typefaces and never skip a beat." By contrast, the DEC printer accommodates a maximum of eight fonts implemented in read-only memory; the Centronics unit also has eight fonts.

This is the company's first stab at the printer market since the cancellation of an exclusive marketing contract with a European office-equipment firm sent Sanders into bankruptcy in 1980. It will seek to market the S700 as widely as possible.

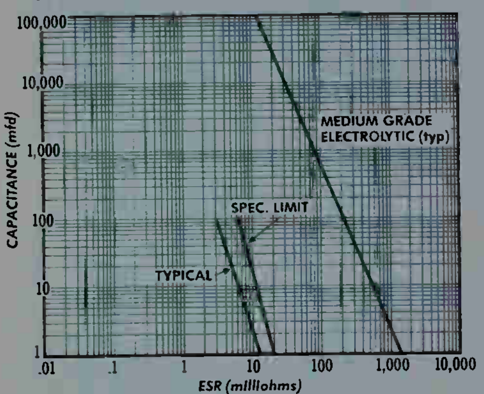
"We plan to sell through distributors as well as directly to original-equipment makers and end users of business and word-processing systems," says Moros. **-Linda Lowe**

# Why the switch is on to film capacitor filters.

## (30-80% higher SPS efficiency.)




For switching power supplies the evidence is conclusive. Where a filter capacitance of 50 mfd or less will do, metallized polypropylene (film) capacitors far surpass electrolytics in impedance characteristics.

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# People

## Bausch & Lomb's Bower sees rise in digital-plotter sales

Call them personal computers or small business computers, but to digital-plotter manufacturers, the growing popularity of the microcomputers is simply a boon, says L. C. (Roy) Bower, vice president of instrument systems for Bausch & Lomb Inc. and recently named site manager for the Houston Instruments operations in Austin, Texas.

"Originally, people just played with them [small computers], but now they are getting serious," says the 60-year-old native of Newton, Mass., who received his bachelor of science degree in electrical engineering from Northeastern University in Boston. "They want to add things like more memory, plotters, and digitizers. Up until maybe four or five years ago, people using plotters were in scientific fields. So it's really been an explosion," he adds.

The explosion is a colorful one, what with the introduction of multicolor pen options, which "has recently opened that door much, much wider," notes Bower, who joined Houston Instruments 15 years ago when it was still a small firm in the Houston area. Although originally the company made X-Y analog recorders, eventually it moved both into the digital era and to the Texas capital, where it now occupies a plant of 90,000 square feet on 20 acres. In 1974, Houston Instruments was acquired by Bausch & Lomb.

"I would hazard a guess that most people don't really need more than three or four colors. But someone comes out with four colors—as we did—and then somebody else comes out with six, then we come out with eight, and so on."

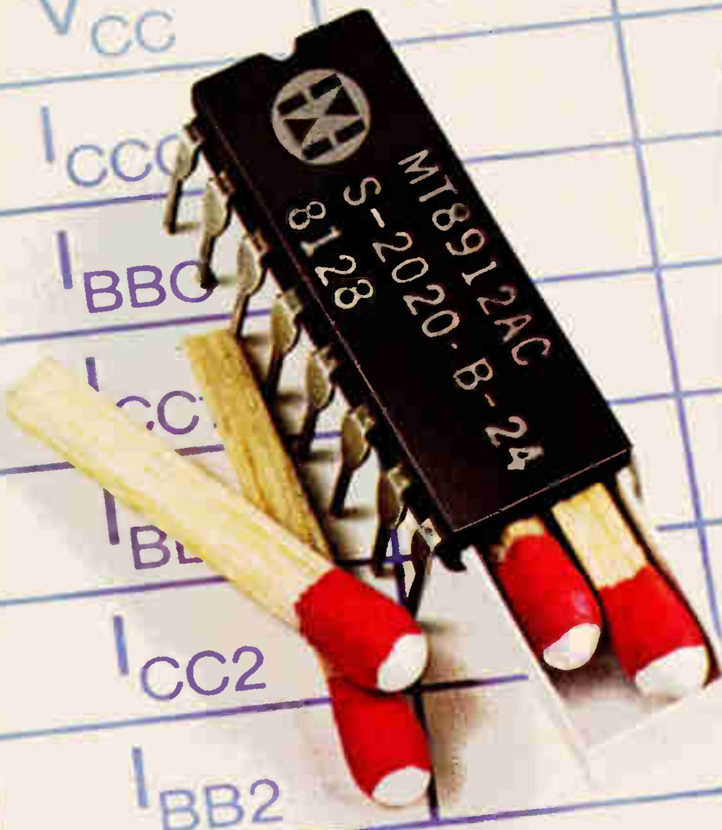
However, electrostatic plotters is one area where color has yet to make an impact. "I'm waiting for it to happen at any moment," says Bower. "Everyone has black and white electrostatic units and everyone is fighting for more dots per inch, better resolution. But the real breakthrough will come with color." Currently, Bower estimates, the electrostatic digital-plotter market is growing at 30% annually, compared with 20% for pen-based plotters.

**Good times.** For L. C. Bower, the increase in sales of personal computers means that his digital-plotter business will boom.

Another growth area, with an annual rate of 35%, has been in digitizers, also produced by Houston Instruments. "They are the new kid on the block," Bower says. Even though digitizers have been around for years, he believes their sudden popularity results from the growth in computer-aided design and the use of digitizers as microcomputer peripherals. He estimates that today's digitizer market stands at $40 million, compared with only $10 million two years ago.

## Geils confident he'll find way to help ease teacher shortage

As teachers of electronics and other engineering technologies desert American campuses in growing numbers for the higher salaries and better-equipped laboratories of industry, John W. Geils has been given the assignment of trying to stop America from eating its own seed corn. He sees it as an awesome but

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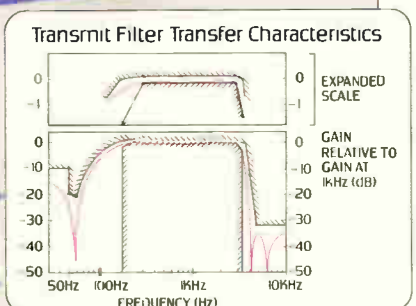
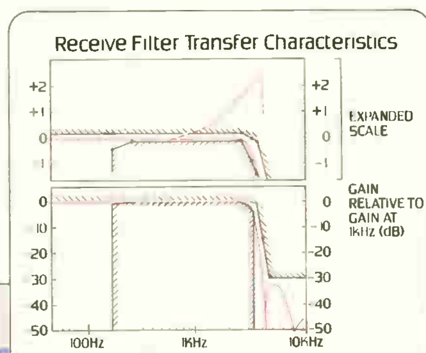
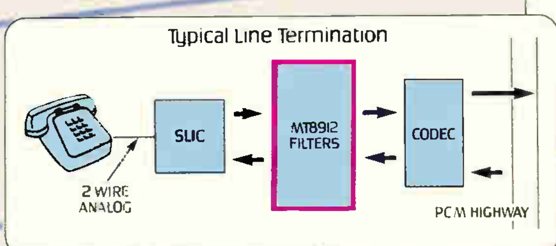
Consider too the MT8912's **power supply rejection ratio: 40 dB** at 1kHz. In addition, the Mitel MT8912 is pin for pin compatible with the Intel I 2912. It meets AT&T D3/D4 and CCITT G712 specifications. The receive filter includes sinx/x correction and there is external gain adjustment of both transmit and receive filters.

All in all, it's a case of hot specs guaranteeing you hot performance.

Find out more about what the Mitel MT8912 can do for your application by contacting your local Mitel sales office.



not insurmountable task.

Geils, 60, is on loan for two years to the American Society of Engineering Education from American Telephone & Telegraph Co., where he was director of network administration. He came to the ASEE's Washington headquarters shortly after Labor Day to head the faculty shortage project initially sponsored by eight major U.S. corporations: AT&T, Du Pont, Exxon, IBM, Union Carbide, and what he calls the three generals—General Electric, General Motors, and General Telephone & Electronics.

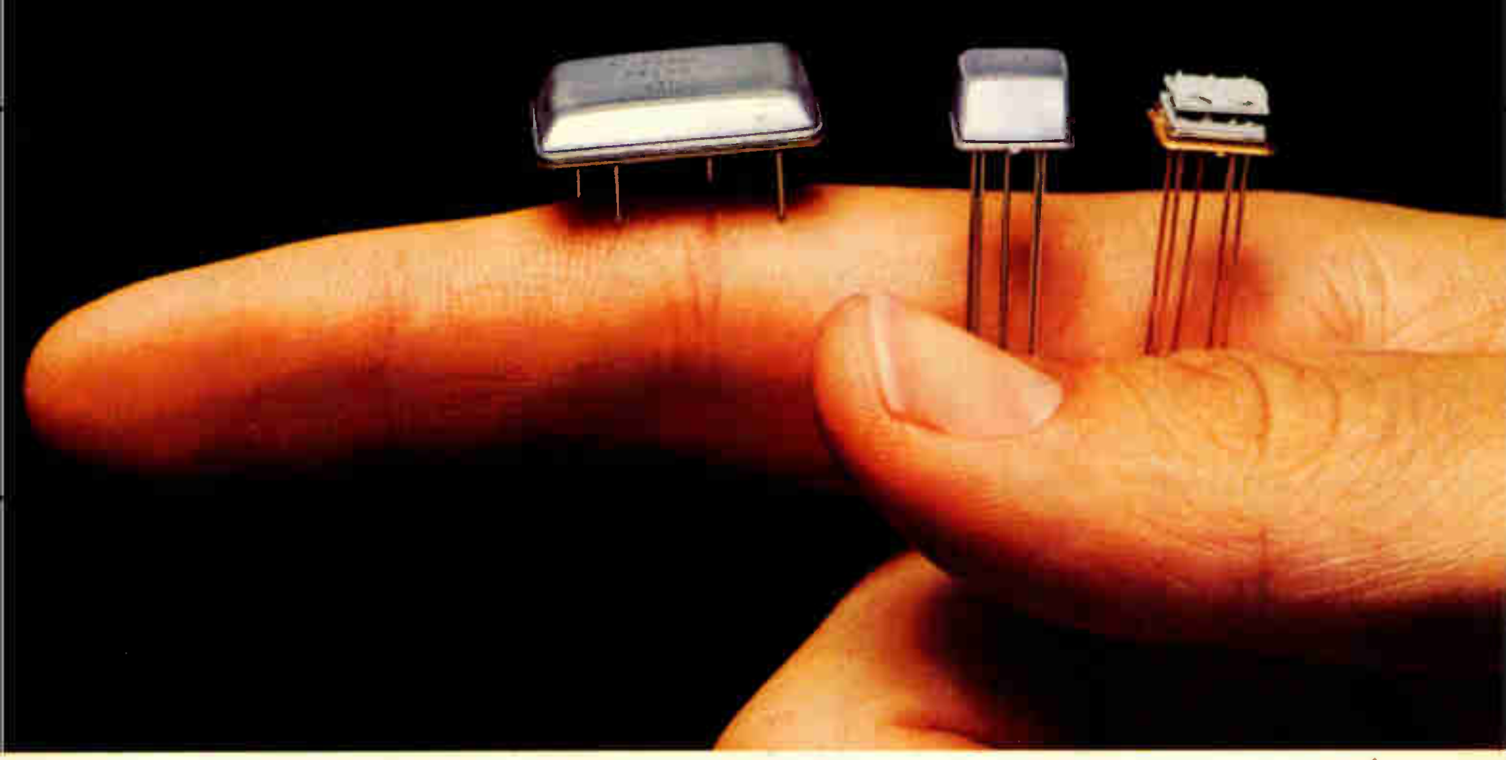
Now, he adds, Hewlett-Packard and Rockwell International have joined the effort, as have three trade associations—the American Electronics Association, the Computer and Business Equipment Manufacturers Association, and the Electronic Industries Association. Moreover, the AT&T executive says the project will get logistical support from the Engineering Manpower Council, as well as the National Society of Professional Engineers.

Bringing together an accurate and adequate data base relevant to the issue may be Geils's most challenging judgmental problem in view of some of the skewed national statistics developed on the issue that fail to sufficiently factor—in demographic considerations. Nevertheless, Geils, who has a bachelor's degree in electrical engineering from Rensselaer Polytechnic Institute, expects to have useful data developed by early next year.

Following that, Geils's task of developing a plan acceptable to academia, industry, and government that can be implemented successfully presents problems more political than technological in nature. Yet the fact that he is charged with carrying this out on an annual budget of some $100,000 seems not to faze him. The engineering faculty shortage and its ramifications, he reminds listeners, "is a social problem, not an engineering problem," that requires at the start more in the way of changes in the attitudes of academia, industry, and government, than it does a big bankroll. ☐

# The Power FET SSR

# Its low resistance is a real turn-on



It certainly is. We've used power FET technology to reduce the ON resistance in the output stage below 0.3 ohms. That means it can switch low level signals with no offset voltage. It also means it can handle full load currents at higher ambient temperatures.

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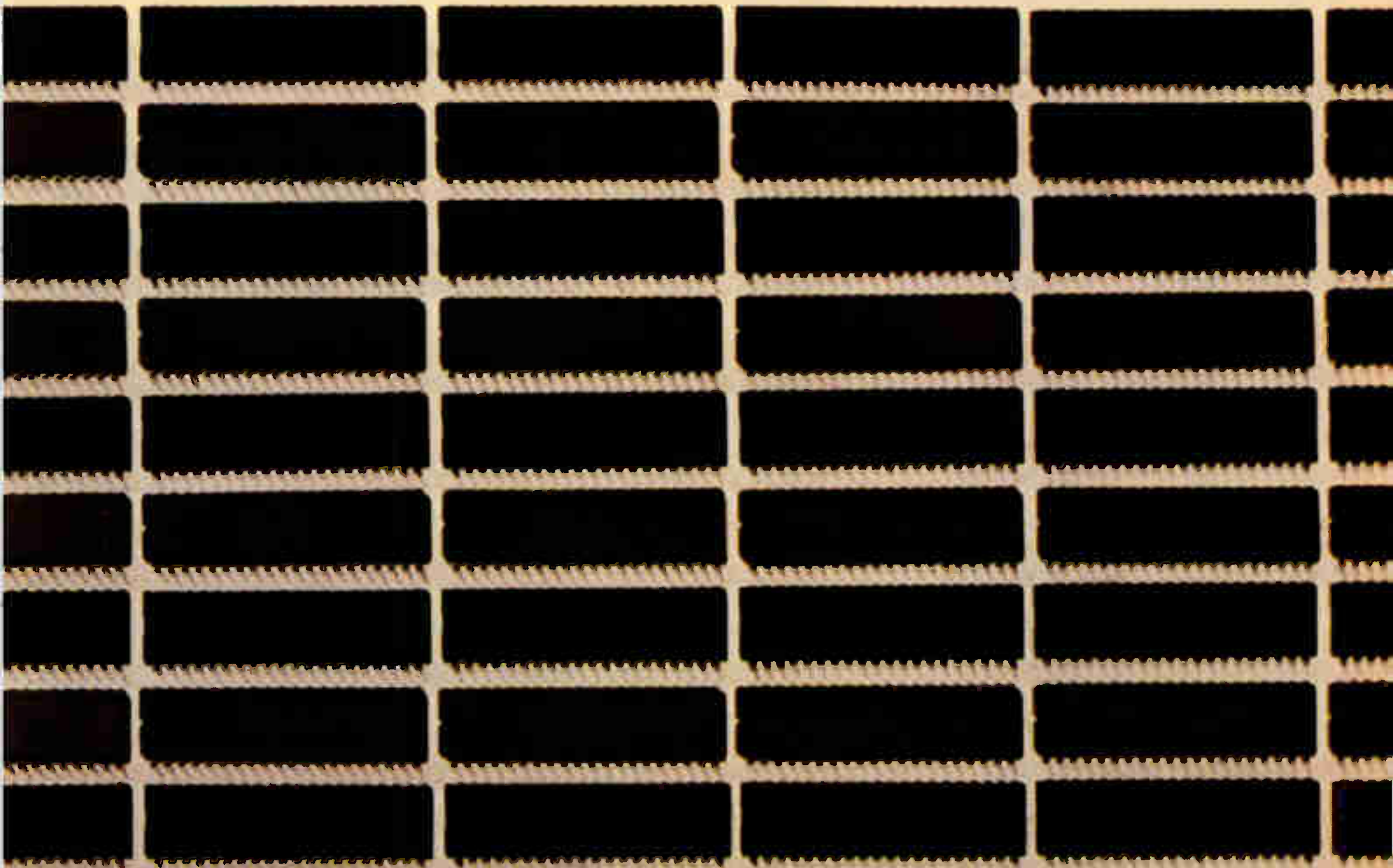

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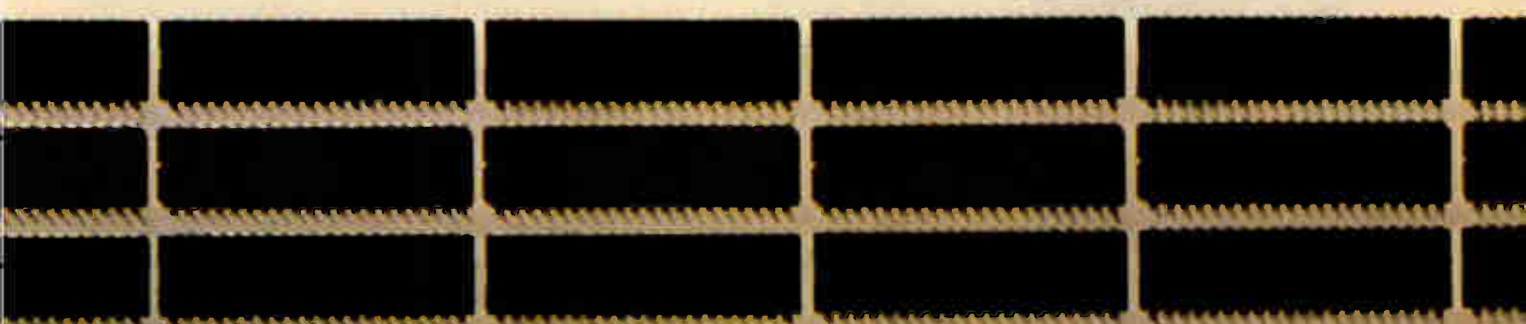

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# Getting the education act together

When it comes to playing the tune that the nation's engineering colleges and universities can't cope with the rising number of students clamoring to enroll because of increasingly severe faculty shortages, America's management and labor choirs seem to sing in harmony. Yet the flip side of that record produces only discordant sounds about whether or not the nation is in the midst of an engineering shortage that, too, threatens to get worse. The noise level is loudest when it comes to consideration of electronics.

Industry groups like the American Electronics Association say that the EE shortage is going from bad to worse. [*Electronics,* Nov. 17, p. 96]. Professional groups, like the Institute of Electrical and Electronics Engineers and its U. S. Activities Board, disagree in part, while the increasing number of engineers being laid off in the current recession disagree completely. Yes, says the IEEE, there are some shortages in some electronic specialties in some parts of the country.

As for the Government, the National Science Foundation seems to be tone-deaf, probably because its lyrics are written with cold data. The Department of Defense is, of course, studying the issue separately, wondering if its shortage of EEs is more a matter of quality than quantity, as Federal pay ceilings force the most talented out of the system and into the waiting arms of military contractors. This leaves the Pentagon with only the tired, the weary, and the demoralized who are neither equipped nor interested in evaluating advances in the state of the art.

The Defense Department's peculiar problems are worthy of a study in themselves. For example, are the nation's budget cutters saving only pennies in salaries at the cost of billions of dollars in military systems that fail to meet performance and price promises because the best and the brightest have quit? There are increasing numbers in the military who would give their best computers to prove that to the White House and Congress.

But there is a larger and far more important point to be made on the dispute over the shortages of engineering faculties, graduates, and student laboratory facilities: it deals with the global competition in high technology, be it electronics, mechanics, or chemistry. While the profusion of studies on the state of America's engineering arts seem to be growing at an exponential rate, virtually all of them are inwardly directed.

Is anyone out there looking at these issues in relation to America's competitors in Europe and Japan, determining how they seem to successfully educate and employ their youth in engineering? Is anyone acquiring data on systems of education as well as on the quality and quantity of engineers in other societies?

Unfortunately—perhaps tragically for the long run—the answers seem to be no, as industry, labor, and Government pursue separate courses, seemingly bent on making points that highlight only their own individual special interests. In such conflicts, the national interest is guaranteed to lose.

It is far past the time when the country's engineers, their educators, employers, and Government must begin coordinating their efforts instead of disputing statistics among themselves as the talent crisis continues to expand. Crises invariably produce inefficient responses such as those we now see. But, as one engineering executive accurately put it, "America has been responding only to crises since 1776, hasn't it?" The answer, of course, is yes. But now it is time to change.


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# Meetings

**6th Meeting on Integrated and Guided-Wave Optics,** Optical Society of America and IEEE (OSA, 1816 Jefferson Place, N. W., Washington, D. C. 20036), Asilomar Conference Center, Pacific Grove, Calif., Jan. 6–8, 1982.

**5th Los Angeles Technical Symposium,** International Society for Optical Engineering (SPIE, P. O. Box 10, Bellingham, Wash. 98227), Los Angeles Marriott Hotel, Los Angeles, Jan. 25–29.

**1st Spacecraft Electronics Conference,** EIA (Frank A. Mitchell, EIA, 2001 Eye St., N. W., Washington, D. C. 20006), Hyatt Hotel, Los Angeles, Jan. 26–28.

**Advanced Semiconductor Equipment Exposition and Conference,** Electronic Representatives Association and Cartlidge & Associates Inc. (CAI, 491 Macara Ave., Sunnyvale, Calif. 94086), Convention Center, San Jose, Calif., Jan. 26–28.

**Annual Reliability and Maintainability Symposium,** American Society for Quality Control, Institute of Electrical and Electronics Engineers (H. C. Jones, Westinghouse, MS 3608, P. O. Box 1521, Baltimore, Md. 21203), Biltmore Hotel, Los Angeles, Jan. 26–28.

**1st Military Computers and Software Seminar,** American Defense Preparedness Association (ADPA, 900 Rosslyn Center, 170 North Moore St., Arlington, Va. 22209), Sheraton National Hotel, Arlington, Va., Jan. 27–28.

**Workshop On Reliability of Local Networks,** IEEE (Robert S. Swarz, Prime Computer, Inc., 500 Old Connecticut Path, Framingham, Mass. 01701), South Padre Hilton Resort, Brownsville, Texas, Feb. 3–5.

**16th Annual Television Conference,** Society of Motion Picture and Television Engineers (Lynne Robinson, 862 Scarsdale Ave., Scarsdale, N. Y. 10583), Opryland Hotel, Nashville, Tenn., Feb. 5–6.

**5th European Exhibition and Congress for Telecommunications,** Online GmbH (Postfach 10 08 66, D-5620 Velbert 1, West Germany), Düsseldorf Fairgrounds, West Germany, Feb. 8–11.

**Aerospace and Electronic Systems Winter Convention,** Institute of Electrical and Electronics Engineers (Tom S. Schuler, Rockwell International, P. O. Box 3105, Anaheim, Calif. 92803), Sheraton-Universal Hotel, Hollywood, Calif., Feb. 9–11.

**International Solid State Circuits Conference,** Institute of Electrical and Electronics Engineers (L. Winner, 301 Almeria Ave., Coral Gables, Fla. 33134), Hilton Hotel, San Francisco, Feb. 10–12.

**Aerospace Applications Conference,** IEEE (Russel Gaspari, Hughes Aircraft Co., MS S12/V305, P. O. Box 92919, Los Angeles, Calif. 90009), Woodbridge Conference Center, Snowmass, Colo., Feb. 21–28.

**Nepcon '82 West,** Cahners Exposition Group (222 West Adams St., Suite 999, Chicago, Ill. 60606), Anaheim Convention Center, Anaheim, Calif., Feb. 23–25.

**Compcon Spring,** IEEE (Harry Hayman, P. O. Box 639, Silver Spring, Md. 20901), Jack Tar Hotel, San Francisco, Feb. 26–28.

**Robots VI Conference and Exposition,** Society of Manufacturing Engineers (1 SME Dr., P. O. Box 930, Dearborn, Mich. 48128), Cobo Hall, Detroit, March 1–4.

**9th Communications Satellite Systems Conference,** American Institute of Aeronautics and Astronautics (1290 Avenue of the Americas, New York, N. Y. 10104), Town and Country Hotel, San Diego, Calif., March 7–11.

**Spring Engineering Conference,** Society of Cable Television Engineers (1900 L Street, N. W., Suite 614, Washington, D. C. 20036), Copley Plaza Hotel, Boston, March 8–10.

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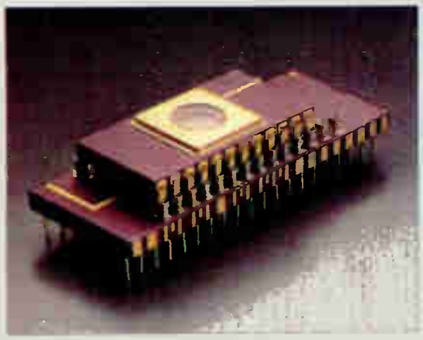

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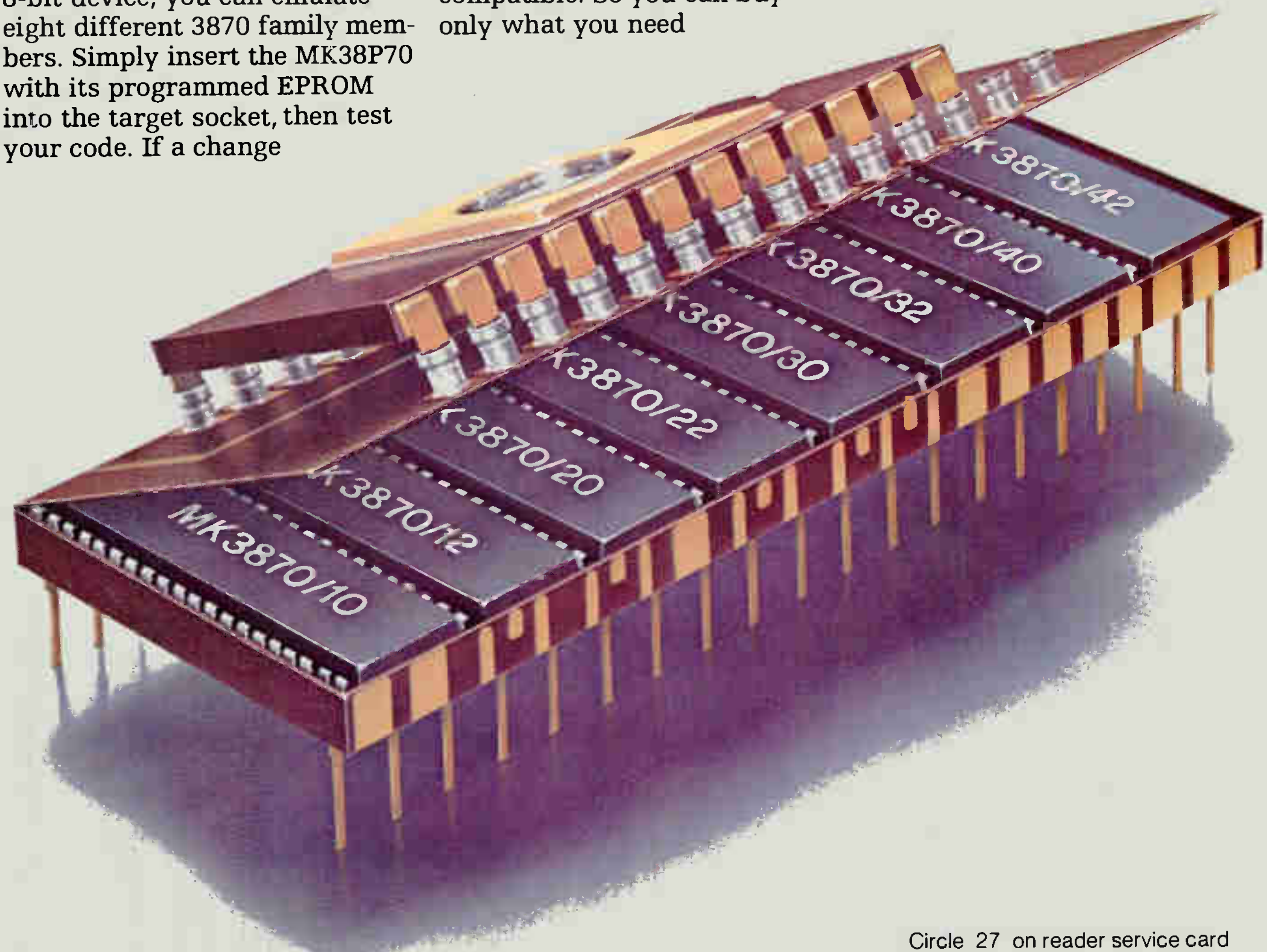
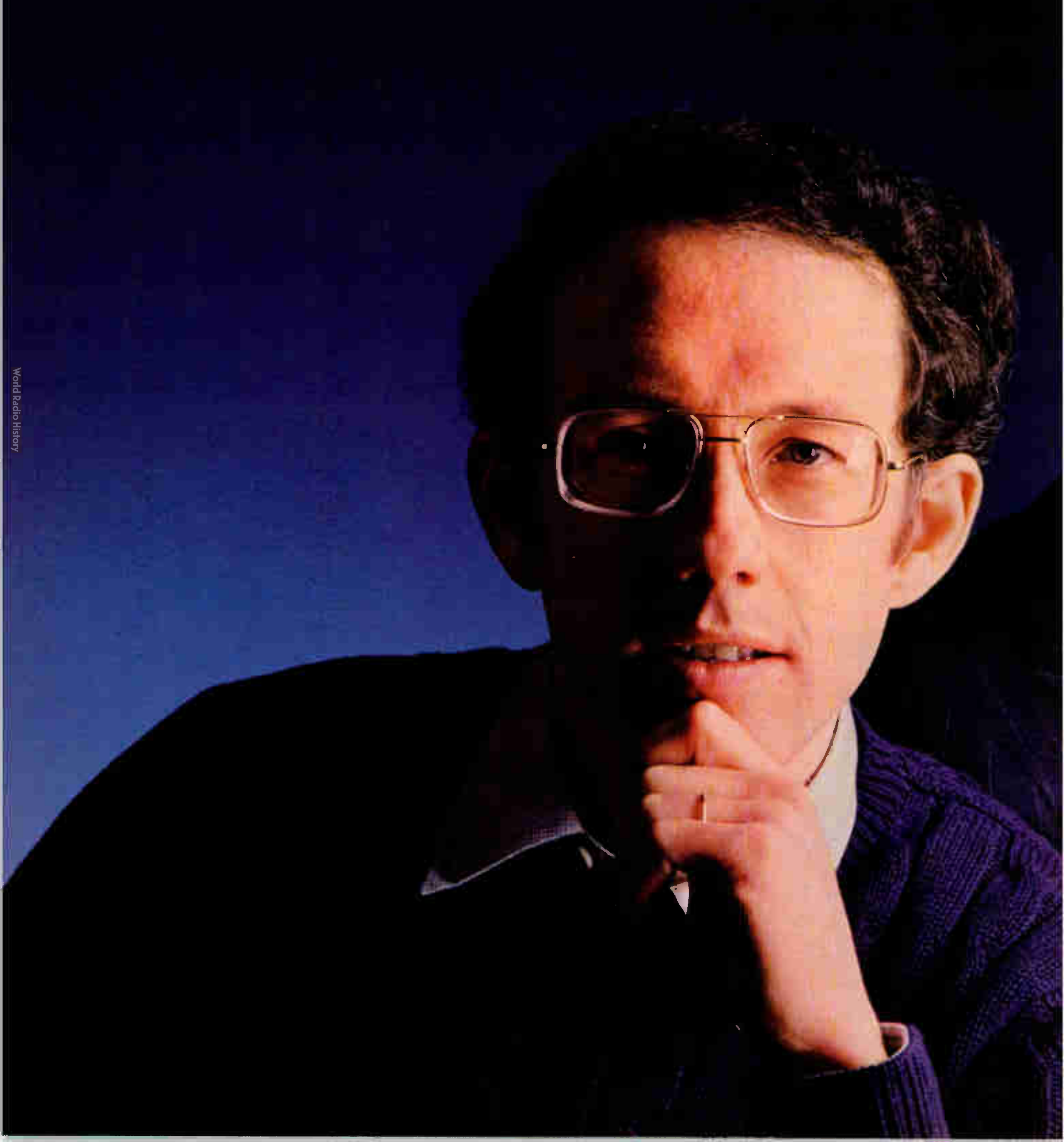



Circle 27 on reader service card



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LTX RESPONDS



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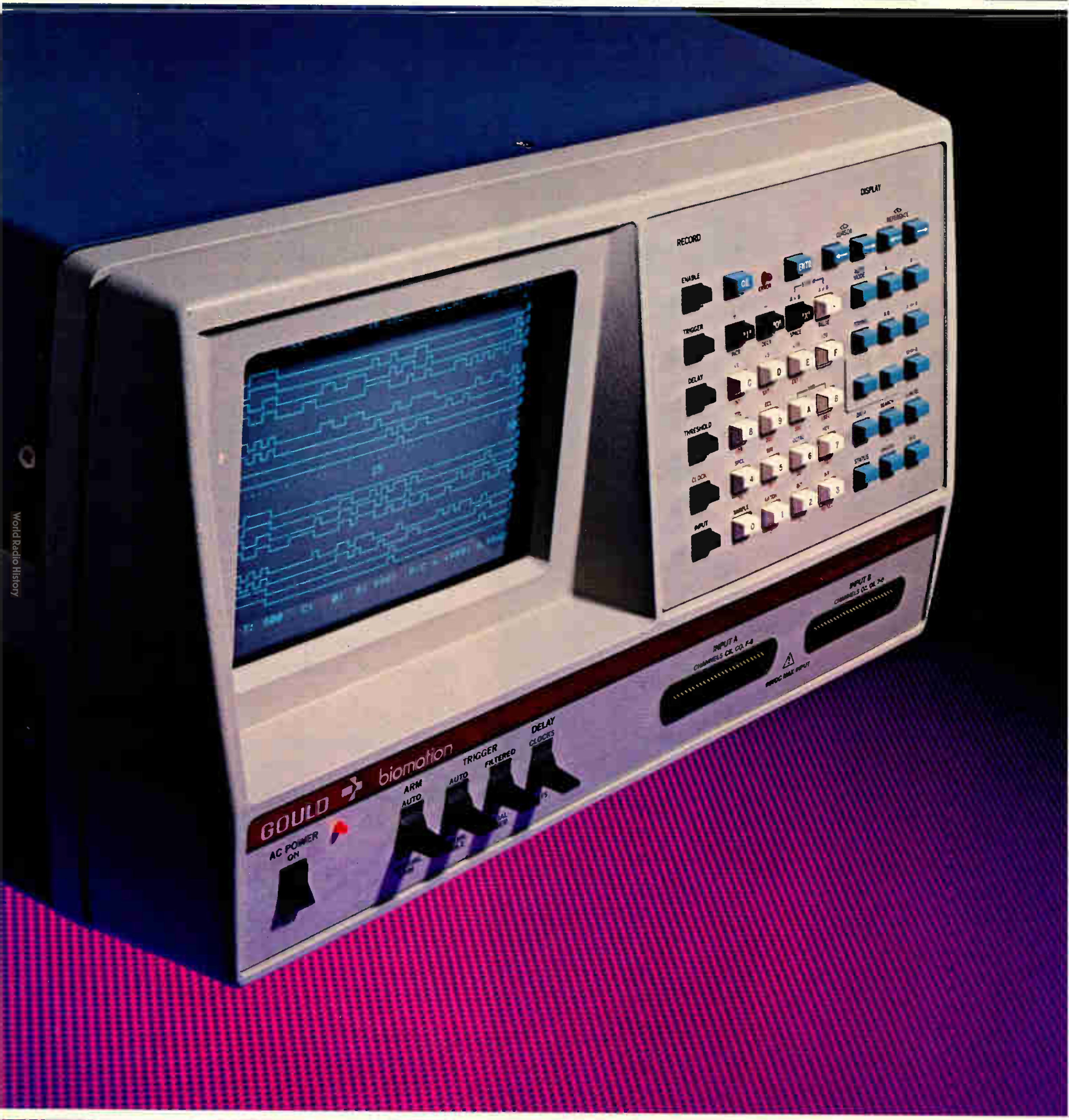
# GOULD BIOMATION K100-D



# 7 reasons why the K100-D is now the world's best-selling logic analyzer.

## How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

**1. It's easy to systematize.**

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

**2. It's concise.**

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

**3. It's fast.**

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

**4. It's deep.**

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

**5. It's clear.**

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in user-specifiable hexadecimal, octal, binary or ASCII.

**6. It has remote diagnostics.**

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

**7. It's well supported.**

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.

The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.

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# Electronics newsletter

**New halide resists respond to all media**

Halide-based photoresists hundreds to thousands of times more sensitive than existing polymer resists, but with equal resolution, may appear within two years, say researchers at GCA Corp., Bedford, Mass. Long used in high-resolution photomasks, halides have never succeeded as resists because of coating defects in the emulsion carrying the halide molecules. **The new two-layer technique eliminates the emulsion, evaporating a 2,000-Å thick layer of halide onto a much thicker polymer film.** A key advantage of the approach is that the halide film is very sensitive to all common resist media—light, electron beams, and X rays. Thus, it could cut the exposure time for fine geometries, allow easy combination of two or more exposure media in a single resist step, and cut the energy needed for an exposure—a possibility especially attractive for X-ray applications.

**Test data-handling is another GenRad factory-automation tool**

Watch for GenRad Inc. to unveil a factory data-management system in the first half of 1982. Based on the Concord, Mass., firm's GRnet minicomputer network system, the new capability—for now called test data management, or TDM—would collect, transmit, store, and analyze data on failures, yields, test trends, and defects. **TDM would also grow to perform full-scale industrial data-base management,** extending GenRad's markets beyond its installed base of testers. With GRnet its first move and TDM its second, the company is committed to carving out a share of the growing factory-automation market. Competition in this market recently intensified with Teradyne's introduction of its Marathon system (see p. 169) and Marconi's announcement of a paperless rework station [*Electronics*, Oct. 20, p. 264].

**IC stocks undervalued, says investment banker**

Times may be tough for U. S. semiconductor companies, but the picture is not as bleak as Wall Street has painted, believes Hambrecht & Quist of San Francisco, Calif., one of the nation's largest investment banking houses. In a recent report, "The Semiconductor Industry: A Propitious Investment Opportunity," the bank declares that "semiconductor stock prices have eroded to the point where their current valuations are similar to the distressed valuations accorded at the market low of October 1974." **It is at this point that latent earning potential will attract investors** because the current depressed valuations more than adequately discount the anemic state of the industry. Its estimates of semiconductor profits, based on results from Texas Instruments, Motorola, National Semiconductor, Intel, and Advanced Micro Devices indicate a decline of 67% this year, compared to a 62% reduction in 1975. Profit declines could be even more severe for semiconductor makers that are subsidiaries, such as Mostek and Fairchild, Hambrecht & Quist believes.

**RCA develops ultrasensitive IR camera**

An experimental infrared camera from RCA Corp., scheduled to be unveiled this week, captures images on platinum silicide detectors in a charge-coupled-device array. The 64-by-128-element array, made at the firm's laboratories in Princeton, N. J., improves its previous efforts by an order of magnitude increase in responsiveness in the 3-to-5 $\mu$m wavelength range—**the camera can resolve the vein structure of a human hand.** The key to the advance is the deposition of uniformly thin layers of platinum, 20 to 100 Å thick, to form the Schottky-barrier diode detectors on a p-type silicon structure.

# Electronics newsletter

**DEC increases 11/23's memory**

In the new PDP-11/23 Plus, the Digital Equipment Corp. of Maynard, Mass., is finally implementing a 22-bit addressing and backplane system rumored for months to be on the way. The 11/23 Plus will be offered initially with up to 1 megabyte of memory, **although with 22-bit addressing, there is room for growth to four times that amount.** The standard 11/23 presently addresses 64 K-bytes directly using a 16-bit word or up to 256 K-bytes with an 18-bit memory-management option. The new processor, aimed at original-equipment manufacturers, will sell for $8,500 stripped, and in its minimum system configuration (with bulk storage, terminal, and RSX-11M operating-system license) for $26,700.

**More Winchesters coming from 3M**

Though long a supplier of disk media to original-equipment manufacturers, it was not until May that 3M Co. quietly slipped into the disk-drive business with its introduction of the 8400 and 8500 series of 8-in. Winchester drives. Now, the St. Paul, Minn., company has extensive plans to build upon that beachhead. 3M engineers are working on a follow-on 8-in. Winchester product, code-named Alpine, **that will at least double the 60-megabyte unformatted capacity of the 8533,** while maintaining the same three-platter design and form factor. Scheduled for introduction late next year, Alpine is expected to reach from 120- to 150-megabyte capacities without resorting to thin-film heads or the advanced metal-coat media technologies that 3M plans subsequently.

**Autodin to get $103 million revamp**

According to a report to be released next month by the market research firm, Frost and Sullivan Inc. of New York, Autodin, the Defense Department's worldwide automatic digital communications network, **will be updated over the next five years by equipment procurements worth some $103 million in current dollars.** In addition, the technology to be employed for improving the reliability of the automatic switching centers, packet-switching nodes, and interconnecting trunk networks in the system has a potential spinoff value of $390 million for nonmilitary Government agencies and the private sector, the company says.

**Sandia advancing state of the art in nuclear-resistant gear**

A new generation of monitoring instrumentation being designed to survive a worst-case nuclear power plant accident must withstand temperatures to 250°C and radiation of 200 megarads. **These specifications, far above even military requirements, can be met,** claims Sandia National Laboratories in Albuquerque, N. M. Researchers there are applying high-temperature, high-radiation weapons technology. The pressure transmitters, hydrogen sensors, and multiplexers, to operate accurately for up to 200 days after an accident, will be demonstrated within two years, they say.

**Key component for microwave receiver developed**

Researchers at RCA Laboratories in Princeton, N. J., have come up with one of the missing links needed for the design of a monolithic gallium arsenide microwave receiver: **a passive component known as a 180° hybrid.** This broad-bandwidth device is used to drive the balanced mixers needed in low-noise receivers. Until now, the available broadband hybrids could not be deposited on planar structures—the essential geometry for monolithic devices.

## Data Instruments

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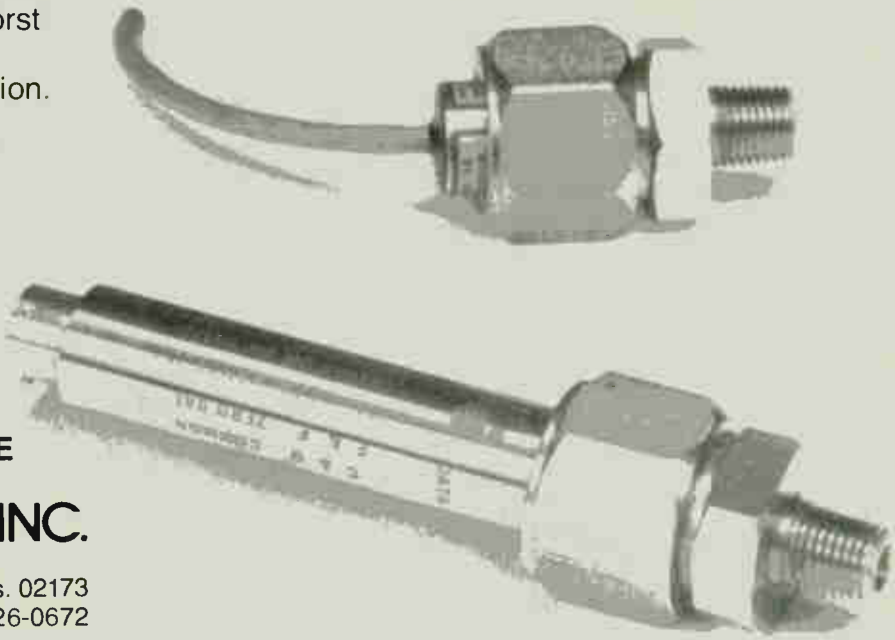

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|---|---|---|
|  |  | |
| ☐ | ☐ | *1. Which country has the world's most productive work force?* |
| ☐ | ☐ | *2. Which country spends the most for research and development?* |
| ☐ | ☐ | *3. Which country exported more goods last year than any other country in the world?* |

*We wouldn't be surprised if you answered "Japan" to all three questions. After all, Japan's gains in these areas have been impressive, as has its press.*

*But in fact, despite recent trends, according to the Department of Labor's Bureau of Labor Statistics, real gross domestic product per employed person—the national measure of productivity—shows Japan behind the United States by 31.6%.*

*As for research and development, based on the latest National Science Foundation figures available, the United States spent three times more than Japan.*

*And in exports, the most recent International Trade Statistics Yearbook shows that even in manufactured goods alone U.S. exports had a dollar value about 39% greater than exports from Japan.*

*So Japan may be gaining, but it hasn't beaten America. In many areas it hasn't even caught up. Which is not to say the challenge from Japan is a hollow one. We know it is real.*

*We know individual companies in Japan, with which many of us compete, achieve excellent productivity levels.*

*We know U.S. spending, of itself, will not generate innovation. It takes commitment to leadership.*

*We know U.S. trade balances with Japan in certain businesses have shifted to Japan's advantage.*

*But we are a strong country with outstanding resources and a formidable overall lead. As we take notice of things we need to do, and get on with them, we can build on that strength and maintain our ability to compete successfully anywhere in the world.*

*America is a winner. A winner has confidence. In fact, one can't win without confidence. Yet, the way things have been written and spoken of lately, you'd think we'd lost our winning ways. Not true. We have great strengths. Let's build on them. We have great ability to recommit—to overcome challenge.*

*As for Motorola, we believe we are already doing much better than the average American company you would compare us to, and most Japanese companies as well. We have plans and programs in place that are working to improve constantly our quality and productivity, and to keep sharp the cutting edge of our technology.*

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Circle 37 on reader service card

# Thermal cycling activates, 'freezes' liquid-crystal display

*by Roderic Beresford, Components Editor*

With no need for refreshing, dot-matrix array expands to 512 rows and 576 columns for portable terminal

**For years, the** light-absorbing and -scattering properties of liquid-crystal displays have charmed researchers into believing they could be fashioned into cathode-ray-tube–like systems that were flat and consumed little power. However, this ideal display has been kept on the back burner because of the problems of addressing each dot in the display.

But now Kylex Inc. has overcome this problem by selecting the molecular alignment of a dot with an electric field during thermal cycling. In one of the largest arrays yet of dot-matrix LCDs, the Mountain View, Calif., firm has placed a matrix of 512 rows and 576 columns into a 6-by-7-inch LCD panel mounted in a prototype portable terminal.

A similar approach in a much smaller, less complex array has been tried in an experimental projection TV system and in a computer display by the Thomson-CSF laboratory at Corbeville, France [*Electronics*, April 21, p. 73]. But what remains to be seen is whether the quirks of such thermal addressing will be preferable to the expense of building large-area panels directly on monolithic or thin-film drivers, as others are trying. Kylex's liquid-crystal material is a mixture of cyanobiphenyls and light-absorbing dye molecules.

**Phases.** In its quiescent state, the host crystal is in the smectic phase, with molecules aligned in parallel planes. The dye molecules follow this orderly configuration in which little light is absorbed.

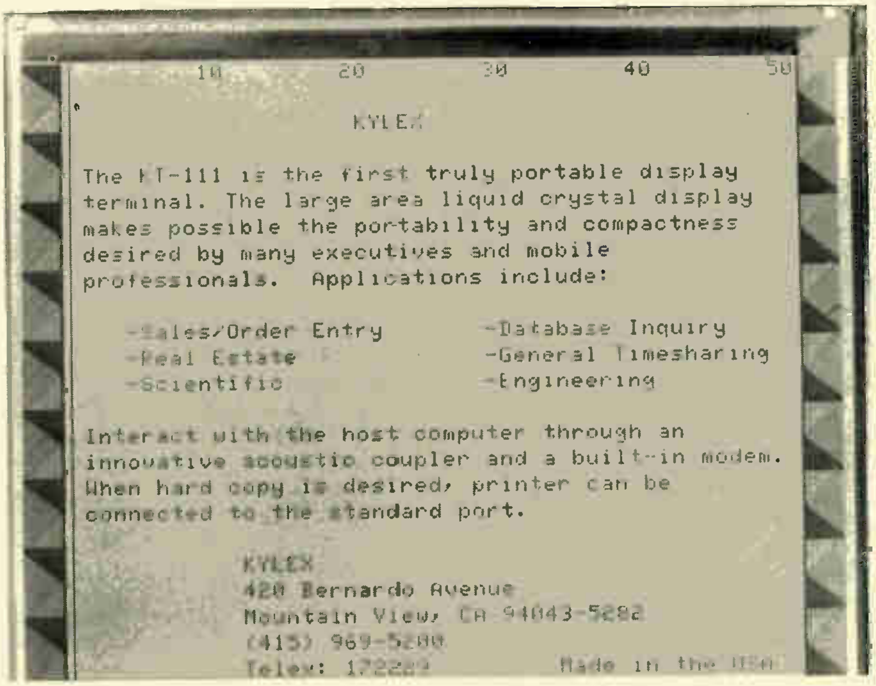
A brief current pulse applied to a row electrode locally heats the crystal to 55°C and into the isotropic, or randomly oriented, phase. As the crystal rapidly cools, it passes through the nematic phase, where the LCD molecules are sensitive to an electric field, before returning to the smectic phase.

Cooling to 40°C in the presence of an electric field—supplied by the column electrode voltage—returns the host to the normal smectic phase. However, cooling with no voltage produces a highly distorted texture that is absorbing, hence opaque.

Both states persist indefinitely, giving the display a static nonvolatile memory. With this memory, no refreshing is required, hence many more rows may be multiplexed than in conventional displays. Removing the opaque, colored state requires either a row-heating pulse, or a column pulse much longer and larger than the writing pulse.

"At our maximum writing rate of about 1,200 characters/second, a 500-line display consumes about 10 watts," says David H. Davies, vice-president for technology at Kylex. "But in a typical application, such as a terminal, the writing rate averages far lower, and thus the power consumption would be around 0.5 w."

The writing speed, which is between 4 and 10 milliseconds/row,




**Hot spots.** Liquid-crystal displays from Kylex may be multiplexed to more than 500 rows. This 6-by-7-inch panel of 280 by 360 dots can be written at over 1,000 characters/s.

is determined by the time the crystal needs to cool. The main complication is that the writing pulse's power must be reduced as the ambient temperature rises or as the writing rate increases. Otherwise, the display overheats and cannot return to the smectic phase.

"We control the write-pulse width with software in the portable terminal," adds Davies. "A Z80 processor checks the past writing history of a row, as well as an ambient temperature sensor, to determine the minimum power needed to write that row. About 20 s of writing history needs to be stored by the processor."

A speedier display must cool off faster after a row-writing pulse. Faster cooling requires a smaller area. Thomson-CSF achieved 60-microsecond row-writing times with a 5-millimeter-square panel.

Kylex is not pursuing the technology for TV applications. However, specific plans for commercialization are awaiting word from Kylex's new corporate parent. Earlier this month, Exxon Enterprises Inc. was negotiating to sell Kylex to another large company. Independently, a group of Kylex employees were looking for capital to spin off a new company to bring the technology to market.

## Production

# E-beam, ultraviolet photolithography join in single-resist step for precision, speed

An advantage of scanning electron-beam lithography is also a disadvantage. Because an electron beam exposes a very small area at a time, it can lay down very fine integrated-circuit geometries. But the beam takes longer to expose a large area than an optical exposure.

So to keep some of the speed characteristics of optical systems, process engineers at present separate mask steps into those requiring the fine geometries possible with the electron-beam technique and those where the coarse geometries possible with optical systems are sufficient.

Now a team of researchers at the Sperry Corp.'s Research Center in Sudbury, Mass., has combined electron-beam and optical exposure in a single resist step. The resulting method retains the fine geometry possible with electron-beam masking, while regaining much of the speed lost in the process.

Technical staff member Terrell D. Berker notes that "depending on chip geometry, it's possible to cut the area requiring electron-beam exposure from as much as 20% to 30% of a chip to as little as 1%, simply by exposing only the fine lines with the beam and reserving larger, coarser areas for exposure with ultraviolet light.

"It is possible to cut electron-beam masking time by a factor of 5 to 10 or more." She adds that, if the mask-generation process is automated, as with a Calma system, it is simple to sieve out the fine and coarse geometries and reserve the latter for UV exposure.

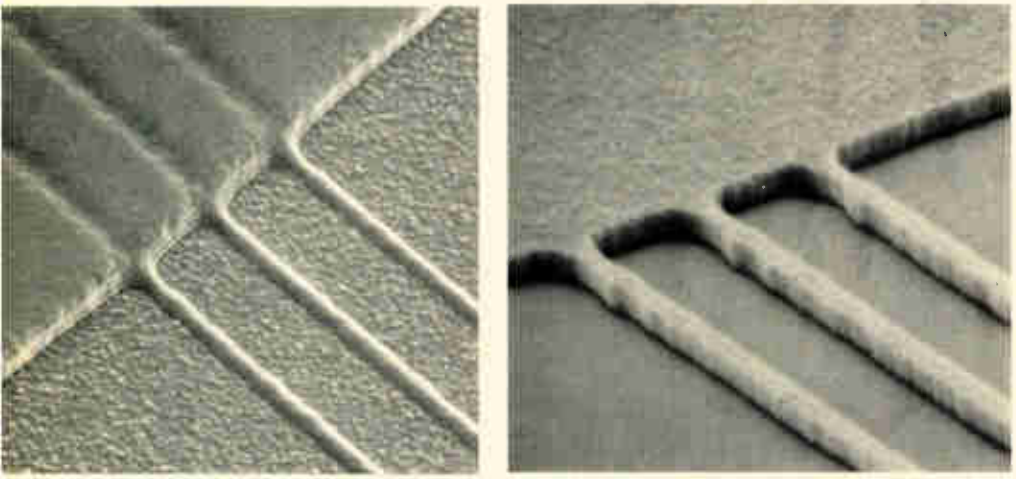
**Positively standard.** Berker and fellow staff member Stephen E. Bernacki, call their approach single-resist mixed lithography. In practice, standard positive photoresists (like Shipley Co.'s 3000 series) are used to coat the wafer, then an electron beam writes the areas where geometries are finest. (The Sperry team routinely achieves 0.4-micrometer line widths with the technique).

Afterward, using a light- or dark-field mask to obtain the required positive or negative optical image, large-area features are laid down with a UV light source. Only after both exposures is the resist developed and etching begun.

Some experimentation was needed to find the right combination of exposure and development time, but the Sperry researchers termed the problem a minor one. The system is said to adapt well to production. "We now are using it in Sudbury on a routine basis for experimental and custom LSI," says Berker.

**Application.** Berker adds that computer maker Sperry Univac may apply the technique when it begins using electron-beam lithography. "They like the fact that the approach uses standard optical resists with which they are familiar, rather than specialized electron-beam resists, which some process engineers appear to dislike," she says.

Berker and Bernacki note that the system saves the most time when used in conjunction with full-wafer exposure systems and somewhat less with wafer steppers. With the former, it is possible to expose all the



**Combination.** Negative image developed on resist, above left, shows 0.4 $\mu m$ lines exposed with an electron beam. "Plateau" was exposed to UV light. Photo at right, taken after plasma etch and resist removal, shows 0.4 $\mu m$ lines intact.

coarse areas on a wafer simultaneously with ultraviolet light, whereas with steppers, the exposure proceeds one area at a time. Still, they say that the time saved overall is "significant." -James B. Brinton

## Computers

# Total immersion cools supercomputer logic

"We have no backup now. We're betting the company—at least at the high end—on liquid immersion technology," declares John A. Rollwagen, recently named chairman at Cray Research Inc., Mendotta Heights, Minn. Rollwagen's reference is to the company's decision this month to back a design developed by founder Seymour R. Cray for the the firm's next-generation Cray-2 supercomputer.

Cray's approach uses 16-gate emitter-coupled logic chips housed in tightly packed modules immersed in an inert fluorocarbon cooling liquid. It was selected over a competing design under development at Cray Laboratories in Boulder, Colo., that relies upon very large-scale integraed ECL gate-array technology. The Boulder activity will now be diverted to other efforts, probably aimed at Cray-1 enhancements.

Meanwhile, Seymour Cray, after stepping down as the company chairman, has put up his own building near Cray's Chippewa Falls, Wis., facility, where he will work as an independent contractor heading a 25-person work force that will remain on the Cray Research payroll. The group will develop a Cray-2 prototype to which Cray Research has first rights, says Rollwagen, who continues as president and chief executive officer.

**Fluorinert.** Although machines such as the Cray-1 and Control Data Corp.'s competing Cyber 205 use freon cooling, the Cray-2 will use Fluorinert, a cooling liquid supplied by 3M Co., St. Paul, Minn., that is used for other electrical applications. Liquid cooling is not uncommon in large computers—IBM's 3081, for example, uses water cooling. But the cooling system design developed by Cray is unusual.

Modules consisting of eight 4-by-8-inch circuit cards will be totally immersed in the circulation liquid, which will carry away the heat generated by the tightly packed bipolar circuitry. Usually, the cooling liquid flows through a heat sink to which the circuits are attached.

With 700 logic chips per module, each eight-board set will dissipate from 600 to 700 watts, says Robert A. Allen, an engineering manager at the Chippewa Falls plant. Each of the four processors in the Cray-2's multiprocessor architecture will contain 36 logic modules as well as 64 memory modules having 4-K bipolar random-access memory devices.

Compared with the Cray-1's 32-megabyte memory, the Cray-2's main memory will have 256 megabytes. The chips are flow-soldered to the cards, so that each eight-card set may be packed into a module less than 1 in. deep, Allen says.

With a 4-nanosecond cycle speed, the Cray-2 is expected to be 6 to 12 times faster than the Cray-1 uniprocessor with its 12-ns clock. Cray rates its top Cray-1 machine at around 80 megaflops (million floating-point operations per second) for typical short- to medium-length vector-processing problems, says planning vice president Peter Gregory.

Comparisons of the Cray-1 and the competitive Cyber-205 vary widely by type of applications, although CDC claims instruction rates up to 800 megaflops. Observers tend to rate the two machines as about equal.

But as one analyst says, "The Cray-2 should far surpass anything that's on the market today . . . it serves notice that Cray intends to remain on the forefront of supercomputer technology." The Cray-2 will not be ready for market, however, until about 1985. -Wesley R. Iversen

## Peripherals

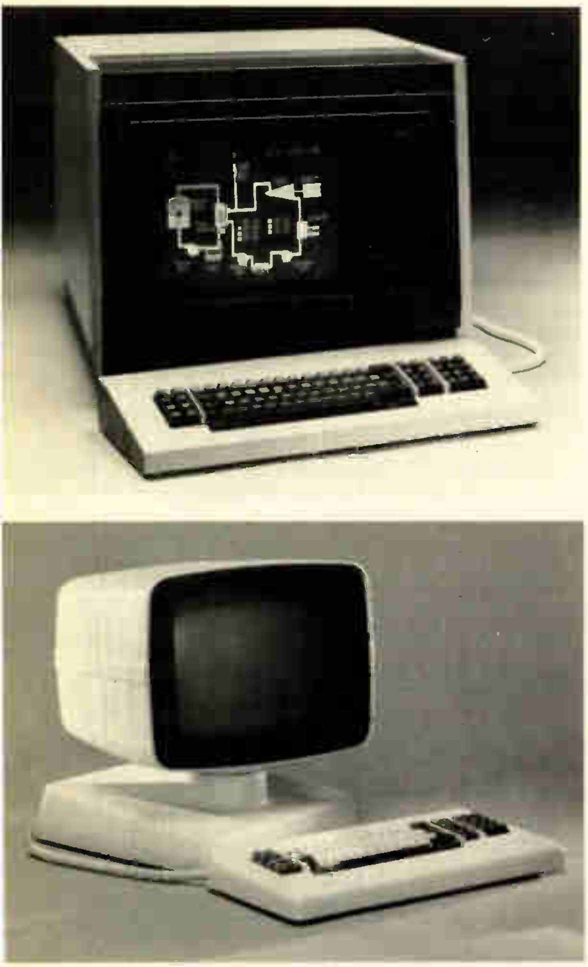
# Terminal maker swaps rights to circuitry for another's cabinet design and tooling

One way to get to market quickly and cheaply is to reverse-engineer a competitor's product. Though it is easier and more ethical to work out a technology trade with another firm, companies rarely do.

Lee Data Corp. of Minneapolis and Atlanta-based Colorgraphic Communications Corp. have, however, pulled off such a trade to the benefit of both firms. Colorgraphic traded production rights to the analog circuitry that drives the color cathode-ray-tube display in its MVI-7 console system. In return, it obtained rights to a new ergonomic, or human-engineered, console cabinet design from Lee, as well as access to Lee's cabinet vendor—and thereby, the benefits of more than $150,000 of Lee-funded tooling.

It is turning out to be a good marriage. Ezra Mintz, president of Colorgraphic, estimates that "we both saved each other at least $200,000 and one or two man-years of effort." He expects the cabinet not only to be cheaper than the sheet metal enclosure used before, but also to attract more customers with its tilting and swiveling CRT mount and detachable keyboard, which can reduce operator fatigue.

**Full-color.** Lee, meanwhile, which has had its series 300 line of terminals emulating IBM Corp.'s 3200 series for about two years, will graduate to a full-color capability without having to go to the expense of locating and hiring analog-video design engineers—a rare breed according to Douglas M. Pihl, operations vice president for Lee. Pihl says that "high-resolution, low-cost color-video-driver design is an unpopular field for American engineers; most of the leading-edge designs are coming out of Japan these days." But not



**Good looker.** Colorgraphic Communications traded production rights to the analog circuitry driving the color CRT in its MVI-7 console, top left, for the jazzier looking cabinetry of Lee Data's IBM 3270-compatible terminal, below. Both vendors will add new products.

all, as witnesses Colorgraphic.

As a result of their deal, both firms will introduce new products in the first quarter. From Lee will come the $3,500 model 1230—to compete with IBM's $4,400-to-$6,000 model 3279 color terminal—which will offer a variety of communications protocols as well as terminal functions. Among them will be bisynchronous communications, and compatibility with IBM's SNA systems network architecture.

**Concentration.** For its part, Colorgraphic plans to emulate Digital Equipment Corp.'s VT100 terminal, which has almost become a *de facto* industry standard—but adding color. The company thought for some time that it might go after the IBM 3279 market, but elected to forego it. "The service and support requirements of that market were too great for a small company," Mintz says. However, his company will continue to offer its MVI-7 color terminal in non-IBM markets [*Electronics*, July 28, p. 14].

So, in the first quarter of 1982, Colorgraphic will introduce its MVI-100, a color version of the VT100. The terminal will list for about $2,750—less than $500 more than a monochrome VT100. It will have all the features of the VT100, including the ability to accommodate DEC's new VT18X personal computer option [*Electronics*, Nov. 3, p. 58].

Though both DEC systems are monochrome, the MVI-100 will include firmware that converts routines run on the new terminal to take advantage of color. The unit also will emulate terminals from Lear-Siegler and Hazeltine, two of the three largest makers of monochrome CRT terminals for the original-equipment maker. The third company is Applied Digital Data Systems, now an NCR subsidiary.

Both firms may include the personal computer offerings of DEC and IBM in their new terminals. They may also offer modified personal computer options of their own; Lee, for example, may offer an equivalent of the IBM Personal Computer, but with the ability to operate as a system-compatible preprocessor in IBM setups. Colorgraphic has plans to drop a MC68000-based 16/32-bit processor card into its console, and also would go for IBM or DEC compatibility. **-James B. Brinton**

## Microprocessors

# Ada compiler, APU readied for Z8000

Zilog Inc. may be No. 4 in the sales of 16-bit microprocessors, but it is spending money like No. 1 to develop the supporting hardware, software, and systems for its Z8000 family. In effect, the Cupertino, Calif., subsidiary of Exxon Computer Systems Group has almost a blank check from its oil company parent, according to president Manny Fernandez.

Two of its biggest programs are to develop a compiler for the Department of Defense's Ada language and an arithmetic processing unit. These are major undertakings. The compiler will involve a full implementation of Ada, and it will be submitted to the DOD for certification. None is yet available except for partial implementations. The APU will be similar to Intel's 8087—the only one out now—but faster, according to Fernandez. Zilog says it will be available during the third quarter of 1982.

He hopes these and other efforts will go a long way to dispelling any worries among potential customers caused when Advanced Micro Devices Inc. earlier this fall left the systems business that it had been building around the Z8000. AMD continues to make the Z8000 as a component, and Zilog, according to Fernandez, is signing agreements with other second sources as well.

**Military hand.** The compiler is expected to strengthen Zilog's already strong position in the military market. The Z8000 was the first 16-bit instruction set to be licensed for military use, though it was recently joined by the 8086 instruction set from Intel Corp. Intel has an Ada compiler, though it is for the iAPX-432 and is not a full implementation. Subset Ada compilers for 68000s are available from TeleSoft Inc. and for UCSD p-code systems from Western Digital Corp.

Zilog is contracting for the Ada compiler with the Data Systems division of Litton Systems Inc., Colorado Springs, Colo., which already has extensive experience with military systems. It will be implemented on Zilog's System 8000 minicomputer and will produce code for the Z800-1, -2, -3, and -4 machines.

The APU, which Zilog claims will be two to five times faster than Intel's 8087, will perform IEEE-compatible floating-point operations of addition, subtraction, multiplication, division, square root, and remaindering—all with 80-bit precision. It also does binary-to-decimal and decimal-to-binary conversions. The unit takes only 10 microseconds for all operations except square root, which requires 12 $\mu$s.

Zilog estimates that a system using its high-speed Z8004 processor, Z8015 virtual memory manager, and an APU will have seven times the performance level of a VAX-750 minicomputer.

**Other efforts.** Zilog is also covering other microprocessor applications. At the high end, it is working on the 32-bit Z80000 that will be instruction-set compatible with the company's 16-bit Z8000 and will compete with similar offerings, such as Intel's iAPX-386 and Motorola's 32-bit version of the 68000. In fact, Zilog's System 8000 minicomputer already has 32-bit data paths and could accept the Z80000 when it becomes available.

Zilog, estimated by industry sources to be doing about $45 million in business annually, also expects to maintain its dominance in the 8-bit arena by offering the Z800—a brand new design that will be instruction-set compatible with the 8-bit Z80 but will have a Z8000-compatible 16-bit interface, enlarged memory-addressing capability, and throughput seven times that of a Z80. All this makes "the Z800 the single biggest undertaking in Zilog's history," according to Fernandez.

An agreement is also currently in negotiation with a U. S. firm—probably RCA Corp.—to implement the Z8000 design in complementary-MOS technology. **-R. Colin Johnson**

## Meteorology

# Radiosonde goes to digital transmission

The old pairing of balloons and weather measurement has acquired a digital look in a new device from Beukers Laboratories Inc. A supplier of gear for measuring weather data for 18 years, the St. James, N. Y., firm has designed the first microprocessor-controlled radiosonde.

Radiosondes have been used by meteorologists for perhaps the last 50 years. They incorporate temperature-, pressure-, and humidity-sensing devices with a telemetry transmitter that broadcasts their measurements to the ground. All the hardware is housed in a relatively cheap, lightweight package borne aloft by a balloon.

Each year, the 147 nations of the United Nations–sponsored World Meteorological Association launch hundreds of thousands of radiosondes to track short- and long-term weather conditions. They are each used once and then literally lost to the winds.

**Worries.** Problems common with the device are distortion and signal error due to noise and channel fading, worrisome to the meteorologists who want data to be as accurate as possible. But the logical solution—sophistication or high power for the transmitter—is ruled out, because of the needs for low cost (the entire package is made for about $50) and battery operation, points out John M. Beukers, president of Beukers Laboratories.

Beukers easily hit on the answer. He moved from the previous analog design to one that transmitted the sensor measurements digitally via a parity-checked bit stream. Thus the integrity of the data may be checked before it is accepted by the ground station and entered into the meteorological data base.

Beukers relied on what are three essentially off-the-shelf digital chips to hit the $50 bogey—no mean feat when the target is a piece of analog gear that has long been engineered and reengineered. The winning devices are an eight-channel multiplexer, an 11-bit analog-to-digital converter, and the system controller—a preprogrammed 4-bit microprocessor with on-chip read-only memory.

**Package.** The electronics fits on a pair of printed-circuit boards on which are also mounted a thermistor (for sensing temperature), a humidity-sensing element, and a switched barometer, or baroswitch.

The radiosonde is packaged within a polystyrene foam case measuring 10¼ by 6½ and 3½ inches thick, and weighing 370 grams with the battery. Its milliwatts of power are supplied by an 18-volt battery, and it operates at the 403- or 1,680-megahertz frequencies reserved for the meteorologists.

Offered as an option is a receiver tuned to navigation signals from worldwide radio-navigation networks like the Loran and Omega systems. The signals are retransmitted to the ground station.

From a measurement of the elapsed time between the retransmitted navigation signals, it is possible to determine the wind velocity at the balloon's altitude, Beukers explains.

Voltages in the sensor channels are sequentially read by the a-d converter, buffered and formatted into a serial ASCII data stream, and transmitted at a 300-bit-per-second rate. The microprocessor adds preamble, parity, and other housekeeping information to the data stream. It is programmed for the entire sequence of functions. VIZ Co., Philadelphia, which also makes the sensors, builds the radiosondes in conjunction with Beukers labs. **-Harvey J. Hindin**

## Employment

# EE shortage divides industry, IEEE

What is the solution to the national shortage of electronics engineers and computer scientists? The quick answer is money—although not necessarily in the form of higher salaries, if the Institute of Electrical and Electronics Engineers latest income survey is representative.

Comparing 1980 mean salaries with 1978 figures, the IEEE data shows the annual average income for all electronics engineers climbed 15.7% in the two-year period to $36,659. Components and subassembly engineers were getting the most dollars ($39,659 in 1980), although the largest percentage gains have been scored in the growing markets for computer hardware (27.6% to $34,755) and medical electronics (26.9% to $38,589).

**Priorities.** Although members of the IEEE U. S. Activities Board agree with industry organizations like the American Electronics Association in Palo Alto, Calif., that the shortages exist and are not subject to quick solutions, they are divided on the nature of the shortages and how they may be best resolved. What both sides do agree on is that more money is needed for recruiting more and better faculty for the country's colleges and universities, enlarging and upgrading their laboratory facilities, and training engineers thoroughly in fundamentals.

A variety of efforts by industry and government aim to identify and articulate specific answers for the manpower problem. Notable among them is the $1.9 million study of the structure and dynamics of the U. S. engineering profession started by the National Research Council under the sponsorship of the National Academy of Engineering. Also starting at the American Society of Engineering Education in Washington is a two-year, $200,000 program funded by 10 companies to develop a plan to alleviate faculty shortages.

At the same time, the American Electronics Association is encouraging its member companies to contribute 2% of their research and development budgets to the nation's universities. In addition, the Semiconductor Industry Association, Cupertino, Calif., is developing a program for funding university programs in semiconductor research.

**Numbers.** What troubles a number of officials in the IEEE, however, is the way the AEA identifies the shortage of electronics specialists [*Electronics*, Nov. 17, p. 96]. The IEEE's Bruno Weinschel, chairman of the American Association of Engineering Societies' engineering affairs council, disputes the AEA's latest survey of 671 companies that projects a U. S. shortage of computer scientists and electronics engineers of 129,000 by 1985, which amounts to about 25,000 annually.

Weinschel contends that the AEA's data is skewed in part since one-half the corporate sample included West Coast corporations. The shortage is most severe in the west where engineers are unwilling to move because of the high cost of housing, mortgages, and other living expenses. In addition, Weinschel points out that each large military supplier competing for the same new contract sees himself as a winner, thereby distorting demand projections.

AEA president Edward E. Ferrey says the association stands by its numbers, noting that although the corporate sample may have been weighted toward California-based companies, it also includes data for all plant operations in many other states.

**-Ray Connolly**

## News brief

**Simpler operating systems, new 4300s from IBM**

A new simplified operating system, along with four new processors in the mid-range 4300 line, heralds the first IBM mainframe computer system that can probably be used without professional operators and a trained data-processing staff. At least some users should be able to install the new 4321 and 4331 systems with its Small System Executive, designed by IBM to reduce the data-processing skills required by users, and use them like minicomputer or small business systems. Several speakers at the International Data Corp. Executive Conference in New Orleans earlier this month saw this development as another step in a trend at International Business Machines Corp. to bring computing closer to end users. Other examples: the recent Datamaster small business system and IBM Personal Computer.

The four new processors fill in gaps in the 4300 line and create a new entry level. The low-end 4321 processor, priced at a relatively low $85,000, delivers increased price performance. The 4300 line-up now contains the following processors in increasing order of performance: 4321 (new), 4331 Model Group 1, 4331 Model Group 11 (new), 4331 Model Group 2, 4341 Model Group 10 (new), 4341 Model Group 1, 4341 Model Group 11 (new) and 4341 Model Group 2.

### Office automation

# More gear readied for total management

Although its announcements are more a reflection of its new approach to the market than of totally new products, Data General Corp.'s Comprehensive Electronic Office (CEO) line is poised for delivery, according to the Westboro, Mass., firm [*Electronics*, Nov. 17. p. 33].

"And that's the difference between us and them," says Ed Zander, director of marketing at the Information Systems division. "The other companies made promises but most of them are not delivering yet."

The other companies—who disagree with that statement, naturally—include Hewlett-Packard, Digital Equipment Corp., and Wang, all of whom introduced office-automation efforts this month [*Electronics*, Nov. 3, pp. 42, 106, and 110].

**Evaluation.** Perhaps delivery as quick as today is not necessary, but it certainly will be soon. "The coming year will be the year of evaluation by a lot of Fortune 1,000 firms," Zander continues. Industry sources besides Zander feel that 1982 will see many firms assessing whether the electronic office really can deliver the productivity and, by implication, an improved bottom line. If the answer is yes, the firms will likely be placing large orders.

More than just office automation is on the line here. "Integrated information management" will be the catch-phrase of the '80s, Zander says. By this he means that managers will have information available to them whether it resides at remote offices or locally, in their own. Data processing, graphics display, and word processing will be handled at one work station, with electronic

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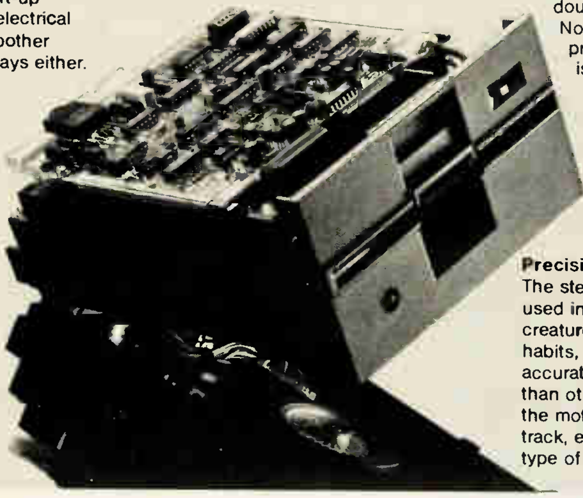





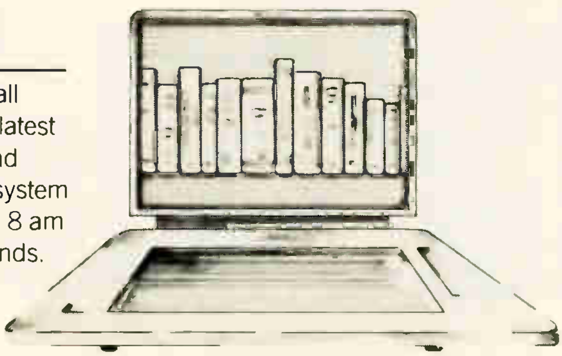



mail passing among users of local and remote computers.

"If big companies like ours can't break into this business in 1982, they may not have a chance by 1984 or 1985," Zander says. Others also realize this—hence the spate of announcements and promises.

Using its 16- and 32-bit Eclipse computers as a core, Data General has developed the software to reproduce the office process. It defines this as the flow of information among all personnel—executive, managerial, professional, and clerical—electronically recreating the "day-to-day interaction among personnel and throughout departments," according to office-automation marketing manager, Barbara Babcock. Often, office functions are automated separately and the results strung together, she adds.

**No jargon.** To make the system more attractive to nontechnical users, DG is adopting a business vocabulary for its wares. Instead of the rather forbidding "data-base management," Data General refers to "electronic filing." In CEO, "documents" are kept in "folders" that reside in "drawers." Users have private "filing cabinets" and CEO even includes an electronic "wastebasket." Deleted documents are in wastebasket memory until a "janitor empties" it. If something is thrown away inadvertently, it can be "uncrumpled," or retrieved, until the wastebasket is finally erased.

The CEO products include Data General's Present decision-support software, its Xodiac local network, a Codasyl-compliant data base with interactive query and graphics output, and access to host computers compatible with IBM Corp.'s Systems Network Architecture SNA protocol. They operate under the Advanced Operating System (AOS) or AOS/Virtual Storage and use Cobol, Fortran, Basic, and PL/1.

The system is menu-oriented. Also, an instant-interrupt key allows a user to cease work at a terminal—say, to answer a phone and place a message in the system—and return to the job being done without having to start over. **-James B. Brinton**

| | 1976 | 1977 | 1978 | 1979 | 1980 | 1981 |
|---|---|---|---|---|---|---|
| OP AMPS/ COMPARATORS | GENERAL PURPOSE BIFET FAMILY: TL080 | LOW NOISE BIFET FAMILY: TL070 | LOW POWER BIFET FAMILY: TL060 | VERY LOW OFFSET BIFETS: TL087, TL287 | FIRST NFET: TL064 SINGLE SUPPLY | NFET OP AMPS & COMPARATOR: TL091/2, TL311 SINGLE SUPPLY |
| VOLTAGE REGULATORS | SECOND SOURCED µA78/79XX FAMILIES | SWITCHING REGS. TL497, TL494; SG3524 | SHUNT REG. TL431, 3 TO 9V DC CONV. TL496 | 2ND GENERATION PWM REGULATOR: TL493, & ADJUSTABLE TL317 | SECOND SOURCED LM337 & MC3423 | HIGH-VOLTAGE (125V): TL783 PRECISION REG.: TL780-XX SERIES |
| PERIPHERAL DRIVERS | SECOND SOURCED ULN2001A SERIES | SN75466 SERIES | SN75416 SERIES | LOW-POWER, PNP-LOGIC SN75446 SERIES | SECOND SOURCED ULN2064 SERIES | QUAD LOW-PWR. LOGIC: SN75436 SN75437A SN75438 |
| LINE CIRCUITS | GENERAL PURPOSE DRIVERS/REC: SN75158/75140 | EIA RS422 DUAL: SN75159 | SECOND SOURCED AM26LS31 AM26LS32A | IEEE-488 8-CHANNEL SN75160 FAMILY | EIA RS422 EIA RS423 SN75172 SERIES DRIVERS/REC. | EIA RS422 SN75176 SERIES TRANSCEIVERS |
| A-D CONVERTERS | | DUAL SLOPE: TL505 | SINGLE SLOPE: TL507 | ANALOG LEVEL DETECTOR: TL480 FAMILY | SECOND SOURCED ADC0809 | SWITCHED CAPACITOR 8-BIT, TL520 ADC |
| DISPLAY DRIVERS | VLED DRIVERS: SN75494 SERIES | QUAD AC PLASMA DRIVERS: SN75426/427 | THERMAL PRINT HEAD DRIVER: SN75490 | BCD TO 7 SEGMENT HIGH-VOLTAGE DRIVER: SN75584 | 32-BIT AC PLASMA DRIVERS: SN75500/-03 | VF DISPLAY DRVS.: SN75512/-13; UCN4810 |
| SPECIAL FUNCTION ICs | ANALOG SWITCHES: TL182 SERIES | HALL EFFECT: TL170 | TIMERS: µA2240 | CURRENT MIRRORS: TL011 FAMILY | BIFET BUFFER: TL068 | NFET SAMPLE & HOLD: TL195 |

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# Washington newsletter

**Navy claims first for thin films . . .**

The first fabrication of a new class of antimony-doped thin films for possible use in military microcircuits or luminescent panel displays is being claimed by the Naval Research Laboratory in Washington. The new process provides a class of luminescent and semiconducting materials "never before fabricated by any other method," contend its developers, **and it is "relatively inexpensive, simple, and highly efficient."** Research physicist John F. Giuliani and NRL fellow Abraham Auerback, now with General Electric Co., have applied for a patent on the development.

**. . . based on $SbF_5$ and halogens**

The NRL process involves passing ultraviolet light from a continuous-wave xenon lamp through the gas-phase reaction between antimony pentafluoride and a variety of compounds containing halogens. **That produces condensation of a photoconductive film on the inside of the illuminated window of the gas chamber.** Changes in the resulting film's resistivity with time are monitored to measure the film's thickness with an electrometer attached by electrodes to the window's surface. Film size is determined by the area of light-beam illumination. Use of a UV laser with the technique could produce micrometer-size features, says the NRL.

**Escalating F/A-18 costs prompt second look**

The Navy's escalating expenditures on the McDonnell Douglas Corp.'s F/A-18 fighter and attack aircraft are prompting reconsideration of the proposed 1,377-plane purchase in the Congress, as well as in segments of the Navy itself. That is the conclusion of a program review by the Congressional Research Service. Costs of the F/A-18 Hornet, says the review, **ate up 32% of the Navy's total aviation budget in fiscal 1981, up from 26% and 12%, respectively, in the two immediately preceding years.** The Reagan Administration proposal to increase naval aviation procurement in fiscal 1982 to $9.4 billion dropped the percentage to 26%, the report notes. Both critics and supporters of the program are concerned, says the review, with the critics complaining that programs for ships, other aircraft, and readiness and training may be sacrificed for the Hornet, while supporters fear that procurement quantities may be cut back if cost controls are ineffective.

**Congressman Coyne adopts electronic mail**

Congressmen and their constituents will correspond more quickly and cheaply using computer communications instead of the U. S. mails, if a Pennsylvania Republican is any precedent. Rep. James Coyne has installed in his House offices a computer communications terminal from DialCom, a supplier of equipment, that is linked to his House Information System data bank. Coyne's constituents who have terminals—his district lies outside Philadelphia in Bucks and Montgomery Counties—**may access his office terminal directly once they request the access code.** Coyne estimates that several thousand constituents own terminals, and estimates as well that such a constituent would pay no more for night and weekend messages than the 20¢ per message now charged for first-class mail. Both those figures caused raised eyebrows when the Congressman unveiled his system in late November. Coyne's terminal receives messages around the clock and dumps them into the House Information System's memory, from which they are later retrieved by his staffers and, on request, relayed to other House members.

# Washington commentary

## The real threat to defense spending next year

The uncommon candor from Office of Management and Budget director David Stockman over the Reagan administration's cuts in Federal spending and in taxes may yet lead to his departure. However, his prospects are small beer compared with the burden his comments on U. S. military spending and its management have put on the Pentagon and its contractors in high-power technologies like electronics. Stockman's observations on these and other Federal economic issues in the Atlantic Monthly for December deserve to be read in full, rather than simply read about in other media accounts. His criticisms are sure to surface again, particularly when President Reagan's military spending program for the fiscal year 1983 goes to Congress in January.

### What Stockman said . . .

Among the most damaging remarks on the U. S. military establishment made by Stockman—who later confirmed the accuracy of the quotes—are these:

- "As soon as we get past this first phase in the [budget-cutting] process, I'm really going to go after the Pentagon," he remarked last February. "The whole question is blatant inefficiency, poor deployment of manpower, contracting idiocy, and, hell, I think that [Defense Secretary] Weinberger is going to be a pretty good mark over there. He's not a tool of the military-industrial complex. I mean, he hasn't been steeped in its excuses and rationalizations for 20 years, and I think that he'll back off on a lot of this stuff."
- "The defense budget in the out-years won't be nearly as high as we are showing now, in my judgment. Hell, I think there's a kind of swamp of $10 [billion] to $20 [billion] to $30 [billion] worth of waste that can be ferreted out if you really push hard."
- Later in the year, Stockman said of the Pentagon: "They got a blank check. We didn't have the time during that February-March period to do anything with Defense . . . so I let it go. But it worked perfectly, because they got so goddamned greedy that they got themselves strung way out there on a limb."
- Then, in September, the OMB director predicted, "Defense is setting itself up for a big fall. If the Pentagon isn't careful, they are going to turn it into a priorities debate in an election year."

That last prospect makes most military-electronics contractors shudder. Moreover, they are suspicious of the motivation of those Democrats on Capitol Hill who are calling for Stockman's retention. "The Democratic National Committee," moans one lobbyist, "could caricature Stockman just as well as—perhaps better than—the Republicans did with [House Speaker] Tip O'Neill" in the award-winning TV commercial during the 1980 Republican sweep. "That could be devastating in a congressional election year when the economy is in recession. Stockman's already written the script. Now he's got to go and be forgotten before he does more damage."

Although such reactions roll readily from the tongue, they completely overlook the rising tide of censure of the Defense Department's managers and their increasingly costly programs by a far more threatening collection of Senate and House members—each a determined hawk. Among their number are Senate Republicans like the Armed Services Committee chairman John Tower of Texas, Strom Thurmond of South Carolina, Barry Goldwater of Arizona, and Dan Quayle of Indiana, as well as such hard-line Democrats as Sam Nunn of Georgia and Ernest Hollings of South Carolina.

### . . . echoes from Capitol Hill

The list of cost-conscious hawks on the House side is equally impressive, embracing members like Melvin Price of Illinois, chairman of the Armed Services Committee and its research and defense subcommittee; Virginia's Dan Daniel, readiness subcommittee chairman; and New York's Joseph Addabbo, leader of the defense subcommittee for appropriations. Although their targets vary substantially, all are looking hard at program overruns and cost controls.

Can they all be wrong in their various criticisms? Certainly they cannot all be ignored, much less swept aside.

Beyond this obvious response to that question is a message for the Pentagon and its contractors—who leapt at the Reagan Administration's funding increases earlier this year that called for more of everything without identifying a goal more specific than beat the Russians [*Electronics*, June 30, p. 58]. Even the most dedicated hawks now see economic and performance flaws in the Reagan military program. Also, these congressional leaders, unlike David Stockman, are certain to be around in January to make their mark on the first military spending program that will be the responsibility of President Reagan and his Secretary of Defense, rather than a quick modification of their predecessors' plans.

**-Ray Connolly**

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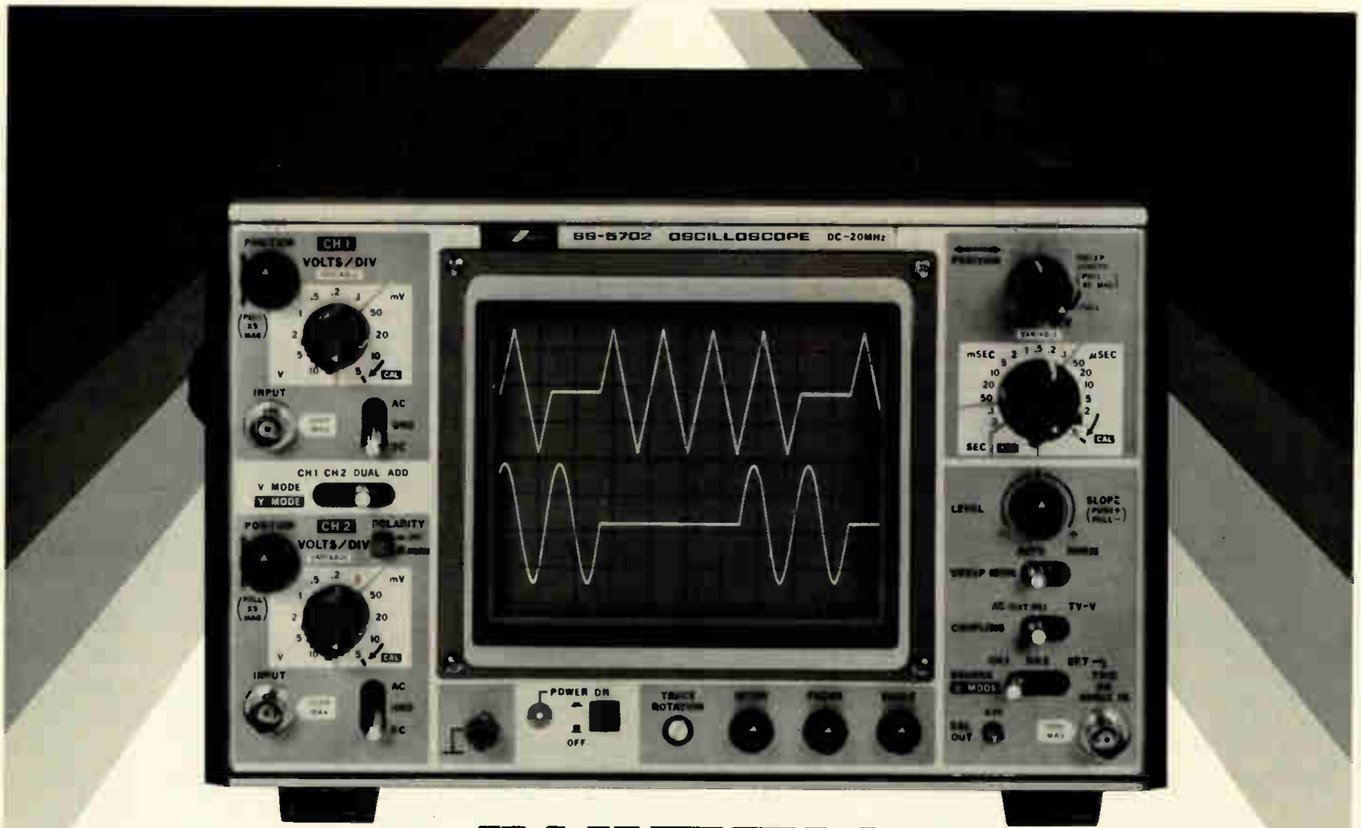


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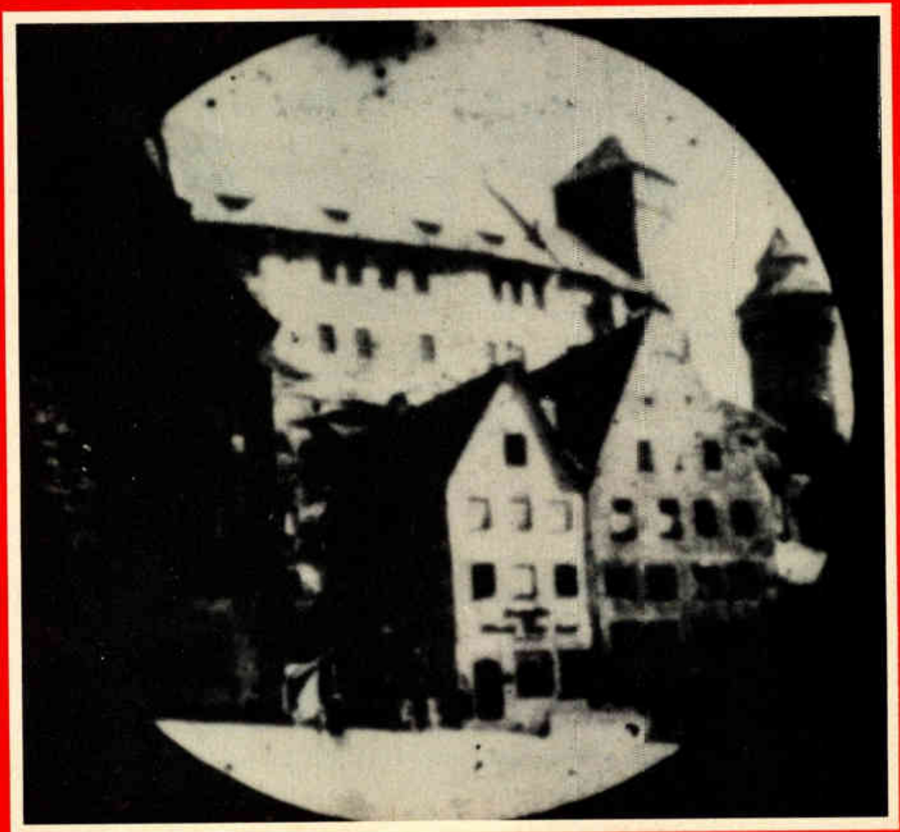
# Electronics International®

## GaAs diffusion process costs 90% less: page 65

The low-light-level imaging tube that helped take this picture at night employs a gallium arsenide photocathode: page 68



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# International newsletter

**Fastest IC claimed by Thomson-CSF**

Thomson-CSF has developed the world's fastest room-temperature integrated circuit. The 11-stage gallium arsenide ring oscillator boasts **a propagation delay of only 22 ps at 25°C,** according to the company's central laboratory in the Paris suburb of Corbeville. The circuit owes its speed to electron confinement at the aluminum gallium arsenide and GaAs heterojunctions—also the basis for Fujitsu Ltd.'s high-electron-mobility transistor [*Electronics*, Oct. 20, p. 73]. Molecular beam epitaxy yields a final single-atom layer of 0.4 nm and a 0.6-$\mu$m gate length.

**Two European firms to form joint video venture with JVC**

Eager to start production of video equipment in Europe, AEG Telefunken of Frankfurt, West Germany, and Britain's Thorn-EMI PLC appear ready to set up a **three-way joint venture with Victor Company of Japan Ltd.** The door has been left open for Thomson-Brandt of France—if management wants to join after nationalization has been decided. The new company will use Victor know-how to manufacture video-cassette recorders in West Germany, video-disk players in England and, if Thomson-Brandt comes aboard, video cameras in France.

**Grundig pushes flat color TV set**

Determined to stay in the forefront of television set technology, West Germany's Grundig AG is developing a flat color TV screen that could go into production within three to four years and be **priced about the same as conventional tubes.** Unlike the small models currently being developed by other firms, the Grundig screen measures 20 inches diagonally, "conforming to living room standards," an official at the Fürth-based firm says. Reluctant to give further details, Grundig will only say that the screen is a plasma type, about 4 in. deep, and that a laboratory version is already working. The German company sees a flat TV screen married to a digital chassis as one of the most innovative steps in future TV engineering.

**Plessey and GI get together on ICs**

Once, General Instrument Corp. of Hicksville, N. Y., came within a gnat's whisker of buying Plessey Ltd.'s semiconductor operation in the UK; now the two companies are getting together again—but this time for a more limited collaboration. Having cooperated on a frequency-locked TV tuning system, with Plessey supplying its high-speed bipolar capability and GI its MOS capability, **the two companies are now to dual-source GI's videotex chip set** for which Plessey is to develop a custom-designed bipolar data slicer. Also, both will share future development of GI's volume-selling PIC1650 series of single-chip microcomputers. Plessey will develop silicon-gate complementary-MOS versions of the present metal-gate C-MOS and n-channel MOS range, and GI will enlarge the family with a more complex silicon-gate C-MOS version providing additional random-access memory, read-only memory, on-chip converters, and so on.

**Ferranti, GTE eye deregulated British telecom market**

Britain's Ferranti Electronics Ltd. and America's General Telephone & Electronics Corp., the second-largest U. S. telephone manufacturer, are forming a joint UK company to participate in the newly liberalized British telecommunications market. Initially **the company will manufacture and market GTE telephone terminal equipment**—including a credit-verification terminal—and private automatic branch exchanges, but joint developments are also in the plans. An early target will be electronic mail.

Ferranti, for example, has recently launched a computer-controlled telex switch to handle upcoming teletex services and which could readily be interfaced with GTE's digital PABX. Target for the joint company is a $50-million turnover within three years.

**Sweden starts Teletex service**

On Nov. 26, the Swedish Board of Telecommunications introduced Teletex service—a text-communication, word-processing, and data-storage system that **links cathode-ray-tube terminals to each other and to the international Telex system** [*Electronics*, April 7, 1981, p. 101]. The service currently uses CRT terminals from Philips Data division of Canada and printers from Philips GmbH of West Germany. Other makers of terminals will be allowed to market equipment to the public. A total of 417 alphanumeric characters can be created on the screen of the intelligent user terminals, which are based on the 16-bit Z8002 microprocessor.

**Radio pager standard on the way**

Following the recommendation of its radio-paging study group, the International Radio Consultative Committee will likely ratify the industry's first paging standard some time next year. The recommended standard is the one **developed by British Telecom** in consultation with its suppliers and has sufficient capacity to address over 2 million subscribers at over 1,000 calls per minute. Called Pocsag, for post office code-standardization advisory group, it is being introduced by British Telecom as the basis for its national paging network.

**Britain latching onto local nets**

Local networks are beginning to catch on in the UK according to Datapoint Ltd., which **has just taken its hundredth order** for its Attached Resource Computer. With 80 systems now installed, the San Antonio, Texas, company says orders are coming in at the rate of 8 a month. Worldwide, the U. S. company, has sold 2,000 ARC systems. Datapoint is now eyeing the newly deregulated UK market as a target for its private branch exchange, a move that will bring it into confrontation with Plessey, Ferranti, GTE, and ICL among others.

**Addenda**

Watch for West Germany's Bertelsmann AG, by its own account the world's largest publishing and printing concern, to become **Europe's first producer of laser-read video disks** to be used with the Laser-Vision system from Philips Gloeilampenfabrieken NV, Eindhoven, the Netherlands. . . . Philips, incidentally, received what it says is "Europe's, and probably the world's **largest single order" for numerical-control systems.** The contract, for 5,000 NC systems worth more than $80 million, comes from the German machine manufacturer Maho. . . . Matsushita Electric Industrial Co. has donated $1 million to the Harvard Business School for the establishment of the Konosuke Matsushita Professorship of Leadership, which will fund teaching and field research into the qualities of effective leadership. This is **the first chair in the Harvard Business School established by a non-U. S. company.** . . . Production of optical fiber for telecommunications has begun at Fibres Optiques Industries—a joint venture of Thomson-CSF, St. Gobain-Pont-à-Mousson, and Corning Investments Inc. that is based in the Paris suburb of Conflans-Sainte-Honorine [*Electronics*, Jan. 27, 1981, p. 68].

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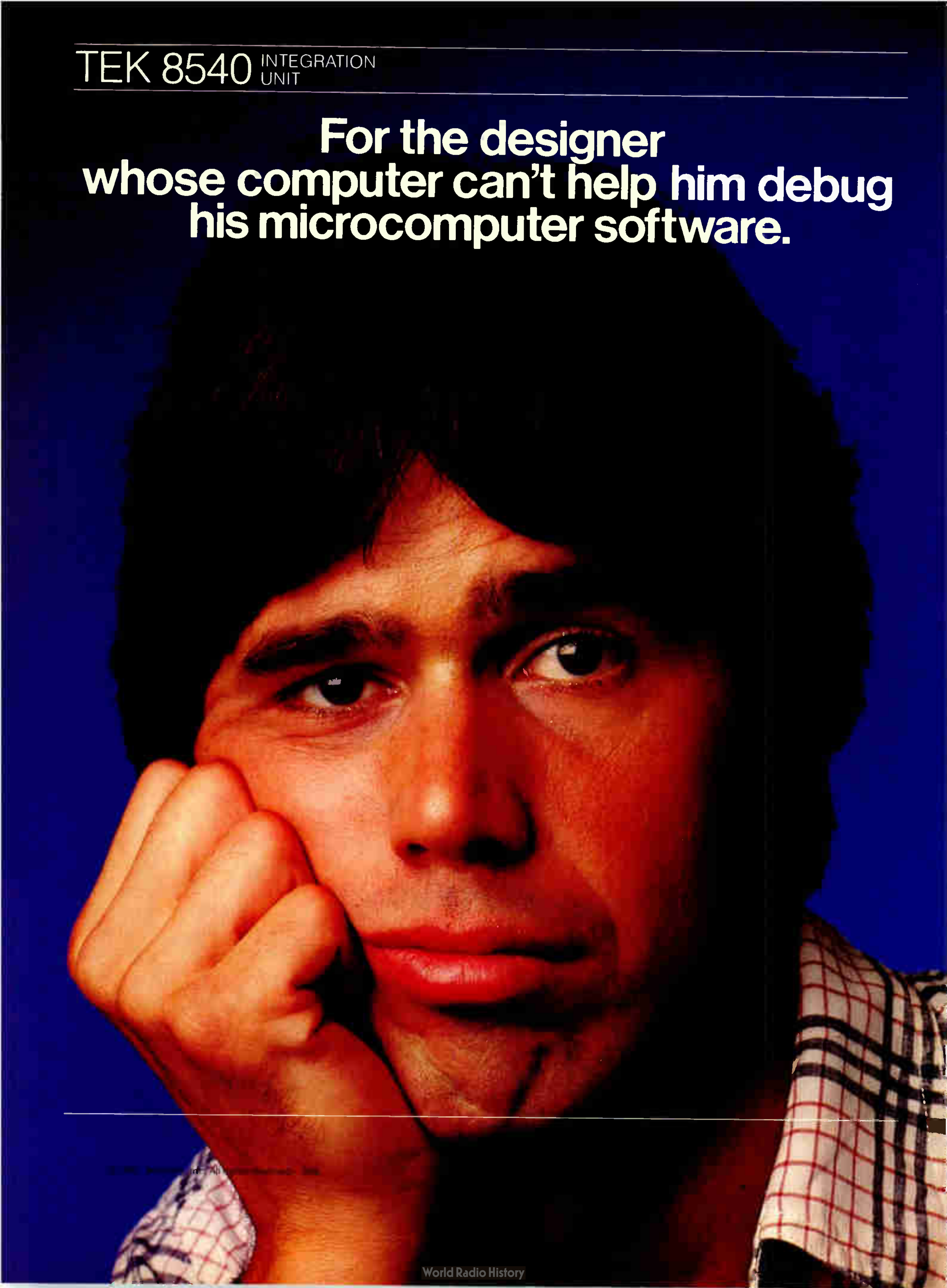
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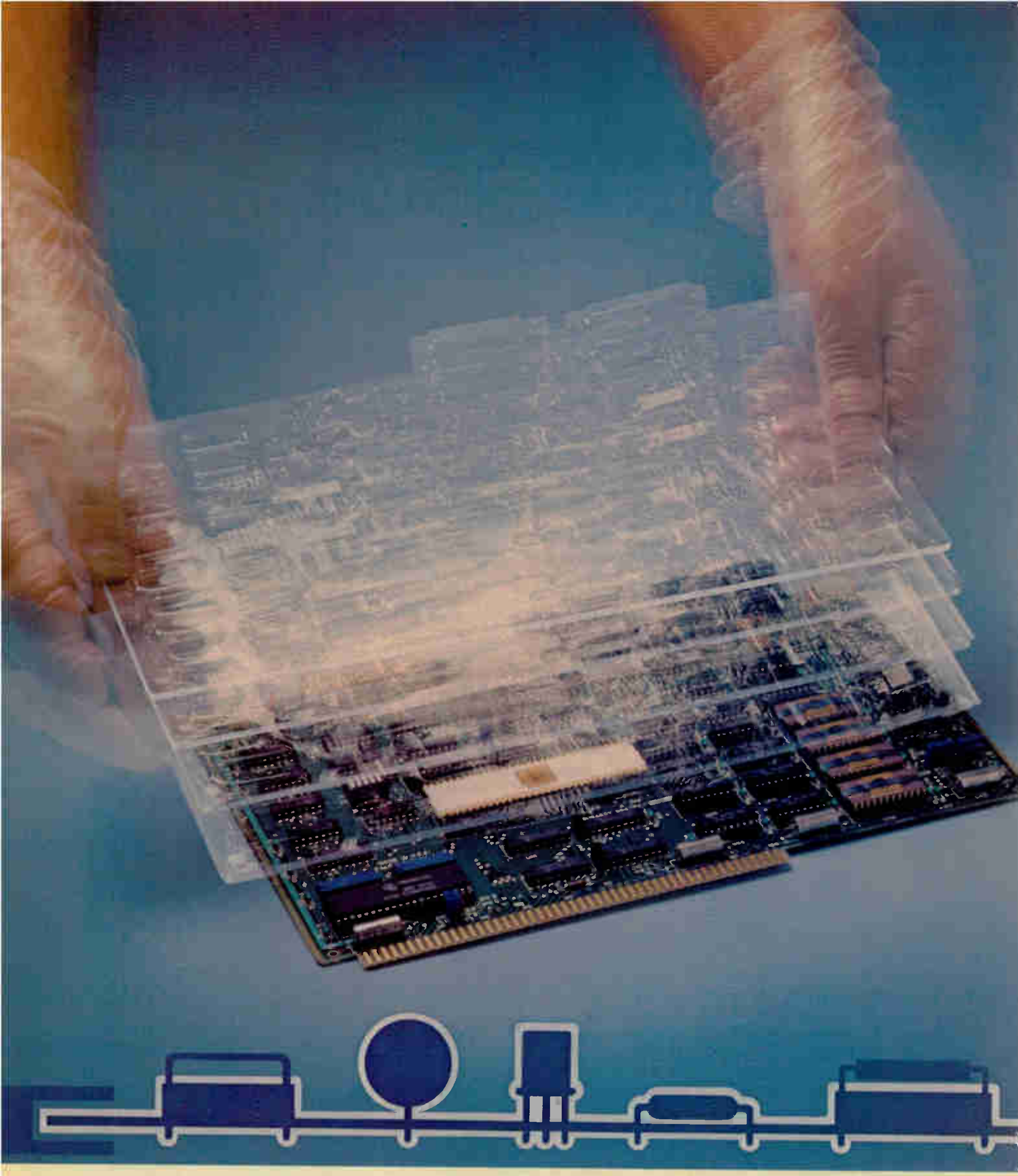

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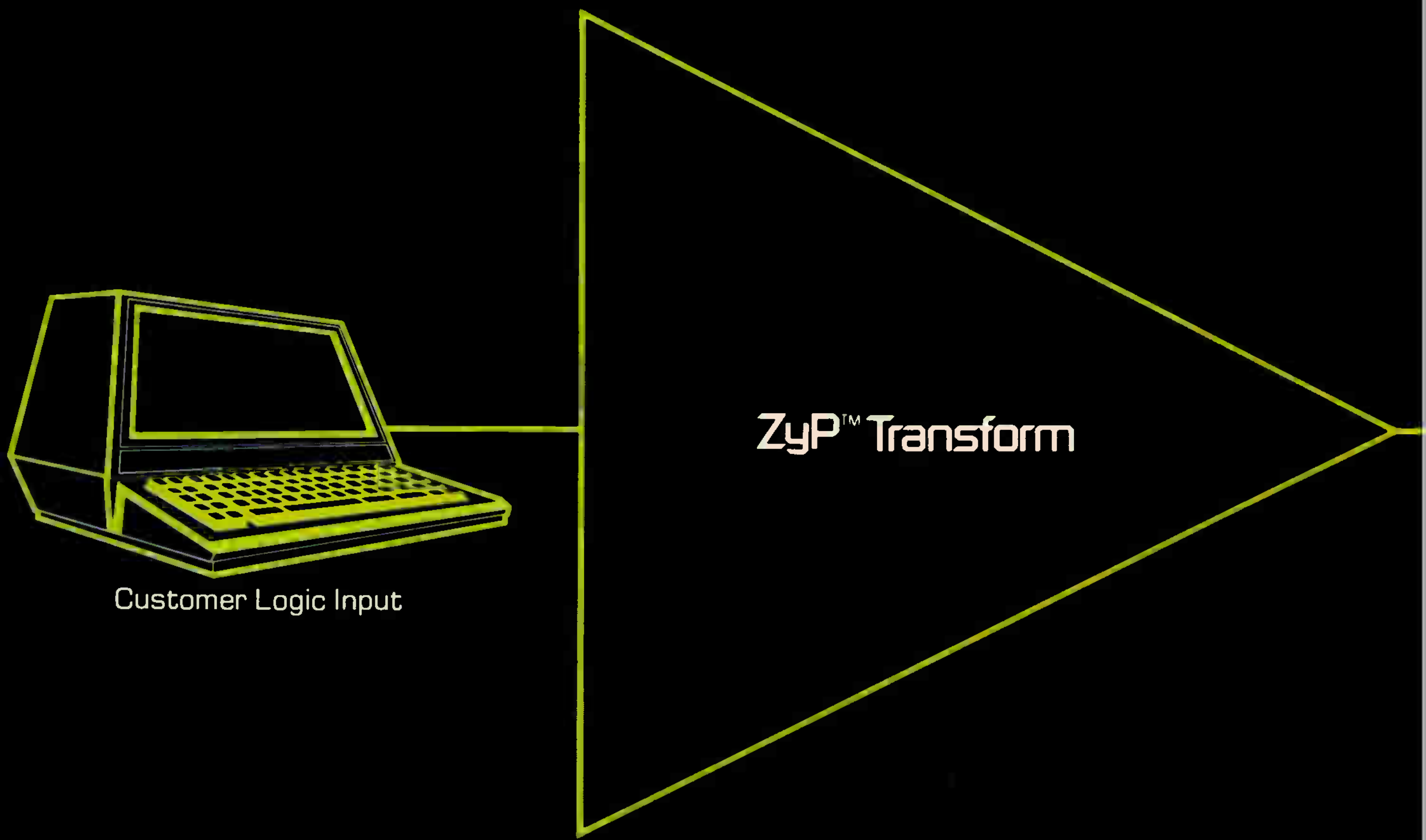


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# Simpler diffusion augurs mass-produced GaAs devices

*by John Gosch, Frankfurt bureau manager*

Dopant-carrying emulsion also serves as protective layer, so that wafers can be processed in an open oven

**A novel diffusion** process produces field-effect-transistor channels directly and inexpensively in gallium arsenide and other III-V semiconductor compounds. Developed by researchers at the University of Duisburg in West Germany, it involves spinning a dopant-laden emulsion onto a wafer.

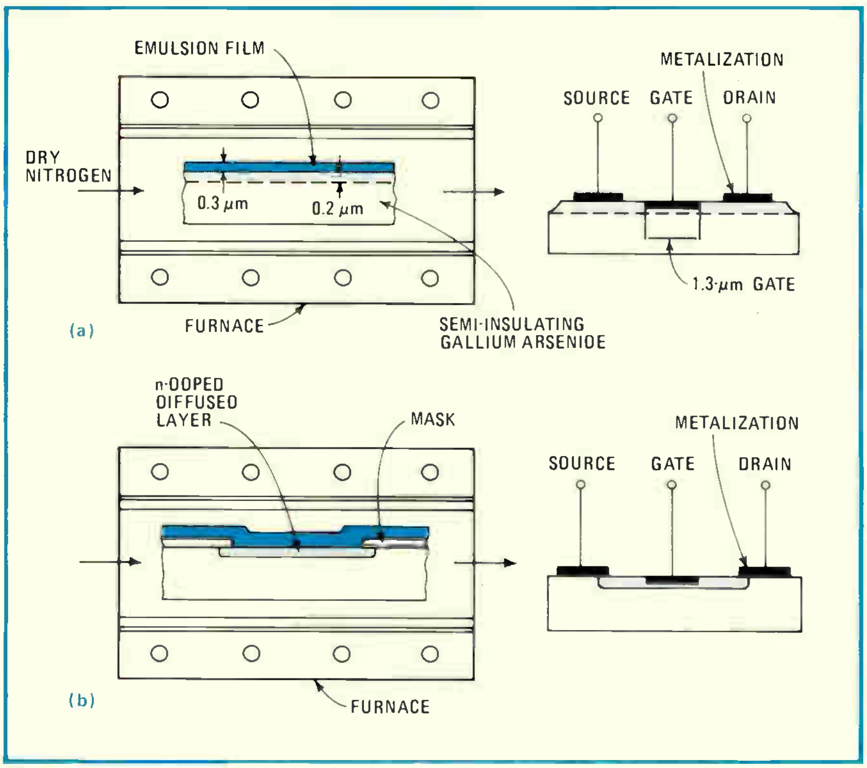
According to Klaus Heime, who heads the Duisburg group, the equipment needed to implement the process is up to 10 times less expensive than that required for the ion-implantation or epitaxial deposition methods usually applied to channel fabrication in GaAs substrates. Yet, performance is equal to or even better than that obtained from such components. The process is applicable to both n-type and p-type diffusion, either across the whole wafer or selectively.

Diffusion into GaAs has until now been impossible to do economically—that is, in an open-tube furnace—because at the diffusion temperature the high arsenic vapor pressure damages the wafer surface. In the Duisburg process, the emulsion avoids this. A product of Demetron GmbH, a German chemical firm, it is spun on the GaAs wafer with a photoresist spinner. At high temperatures, it changes into a doped silicon dioxide layer. This conversion, explains Norbert Arnold, the group's process specialist, "is the most important aspect of the process." With its dopant, the oxide layer not only constitutes a solid diffusion source, it also protects the wafer surface against pitting and dislocations.

**Specifics.** The formation of the doped oxide layer and the diffusion take place simultaneously in an open quartz-tube furnace in a pure nitrogen atmosphere and at temperatures between 550° and 900°C. The temperature to be used depends on the semiconductor material and the kind of dopant involved, as well as on the desired diffusion depth. For example, 800°C is required to diffuse a 0.1-micrometer tin-doped layer into a GaAs wafer in just 15 minutes.

During the diffusion process, the surface remains mirrorlike. Only in the undoped regions could some submicrometer pits be detected, Arnold notes. In the doped regions, however, there was no damage at all. So, unlike in an ion-implantation process, the surface need not be annealed. After the diffusion process, the oxide film is etched away in hydrofluoric acid at room temperature. To fabricate devices, the ohmic contacts and the gates are produced as usual.

The figure shows the Duisburg process using two selective-diffusion




**Neat.** A GaAs wafer covered in a dopant-carrying emulsion is heated at 750°C for 30 min. If wholly diffused, it requires a mesa etch (a); selective diffusion creates self-isolated FETs.

methods. One is an etching process that defines the dimensions of the doped oxide layer (top), and the other involves a masking layer of, for example, silicon nitride (bottom). With either method, wafer areas can be diffused and completely planar devices and circuits made.

The process is thus similar to well-established silicon planar technology. To implement the diffusion, all that is needed is a furnace, which means low cost. Since the furnace can be of the open-tube type, mass fabrication is possible, so it is little wonder that semiconductor houses both in the U.S. and Europe are showing interest in the process.

Thus far, Heime and his group have made Schottky-gate FETs with 1.3-$\mu$m gate lengths, as well as Schottky diodes. Further applications of the process, Heime says, are in highly doped contact layers, highly p-doped layers for pn junctions in junction FETs, and optoelectronic devices such as light-emitting, laser, and photodiodes.

**Superior.** The performance of the devices fabricated so far is excellent, notes Heinrich Daembkes, the researcher who carried out the measurements. While the noise characteristics are just as good as those of ion-implanted devices, the transconductance per millimeter of gate width is far higher—from 120 to 140 millimhos, depending on channel technology, versus 90 to 100 mmho for ion-implanted channels.

**Many advantages.** This, Daembkes says, spells an improvement in gain at comparable transit frequencies, making the process well-suited for microwave components. Furthermore, the diffused devices are smaller. At the same current, a higher device density can be achieved. High frequency measurements have shown a cutoff frequency of about 20 gigahertz.

Further work at the Duisburg University labs is aimed at applying the process to other III-V compounds. Preliminary experiments have shown that diffusions at 650°C in indium phosphide are possible without surface degradation. This indicates that the process is applicable also to ternary and quaternary alloys. InP and InGaAs pn-junction FETs are now in development—devices that lend themselves well to integrated optics.

## Japan

# MITI 'reluctant' to meet U. S. demands for military know-how from Japan

Mid-November reports that Japan's foreign ministry now backs the export of military technology to the U.S. sparked considerable controversy in Tokyo. Even the country's profit-starved defense electronics industry seems nonplussed. And with officials at the Ministries of Foreign Affairs and International Trade and Industry (MITI) insisting that the question is still under study, it seems unlikely that a decision will be reached by year-end, as the U. S. Department of Defense hopes.

As early as midway through the Carter Administration, top DOD officials, seeking a stronger defense role for Japan, had started warning their Japanese counterparts that the flow of defense technology must no longer be unidirectional—from the U. S. to Japan. Such reciprocity would break with that country's long-time, domestically popular policy of prohibiting military exports in any form, but the U. S. request did not generate much attention until reiterated last summer by Richard Delauer, undersecretary of defense for research and engineering.

**Protest.** Now the lines are being clearly drawn in Japan following the leak of a foreign ministry draft suggesting that a policy exception for the U. S. could be justified under the terms of the Japan-U. S. Security Treaty and the bilateral Mutual Defense Assistance Agreement. The news touched off a storm of protest in the press and the Parliament, despite government claims that the draft was not its final decision.

Indeed, Japan's powerful bureaucracy is still split on the question, which will ultimately be decided by the cabinet after the ministries presumably reach a consensus. Although the Defense Agency and Foreign Ministry appear to favor accommodating the U. S., the more conservative MITI remains unconvinced. "We are taking a wait-and-see stance," says Masamitsu Hiroumi, director of MITI's Foreign Exchange and Trade Finance division, though he admits that MITI is "reluctant" to see a change in its policy.

**Catch-22.** Clouding the picture further is the failure by U. S. authorities to specify which Japanese technologies they might want. Experts on both sides of the Pacific mention microcomputers, very high-speed integrated circuits, fiber optics, and robots as likely candidates, but no one is sure. U. S. officials are reluctant to get more specific until the policy is changed, and the Japanese are uncomfortable about changing their policy without knowing what the U. S. wants.

Some Japanese experts claim their country has little to offer in any case. "Japan is ahead in some areas of basic technology and in production methods, but those are tiny areas compared to America's overall superiority," says Takeshi Abe, general manager of the Government Requirements Marketing division at Mitsubishi Electric Corp. Abe adds that Japan's defense electronics industry does not foresee significant new business in selling technology to the U. S. At the Japan Ordnance Association, executive director Jinshichi Hirano agrees with those American experts who assume that the U. S. would be interested more in component technology than in purchasing whole systems. "I don't think we have any systems the U. S. wants," Hirano says.

That sentiment is seconded by at least some U. S. defense contractors. "We don't think there's much here

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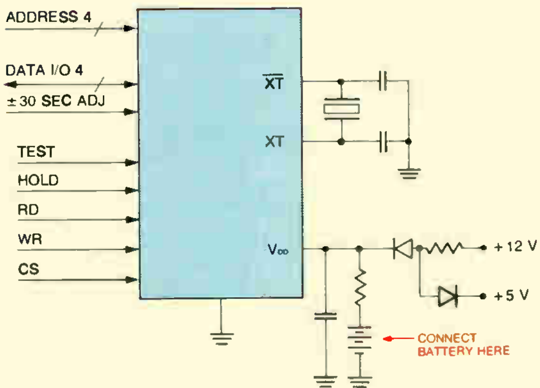


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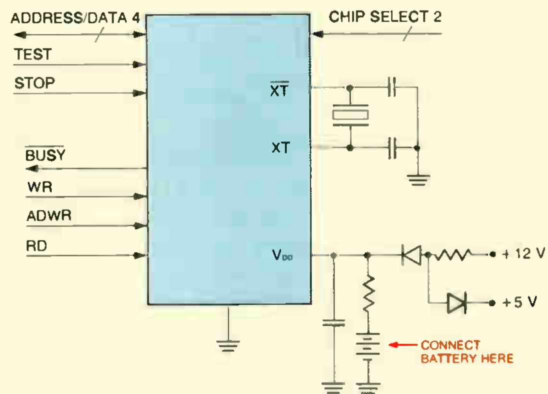


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worth making a big case about," says an American defense executive based in Tokyo.

Observers point to other problems in balancing the technology flow. Whereas in the U. S. much military R&D is Government-funded and -owned, most Japanese defense technology is developed privately. So even if Japanese policy were changed, it would not ensure that companies there would happily transfer their prized technology. Some Japanese executives even worry about eventual U. S. efforts to dictate Japanese R&D projects.

By the same token, some American businessmen ask why the U. S. is aggressively seeking something else to buy from Japan when bilateral trade is so skewed in its favor already. Others question whether it is wise to make the U. S. defense even partially dependent on Japan. "Everyone is dreaming up the worst hobgoblins," notes one U. S. official.

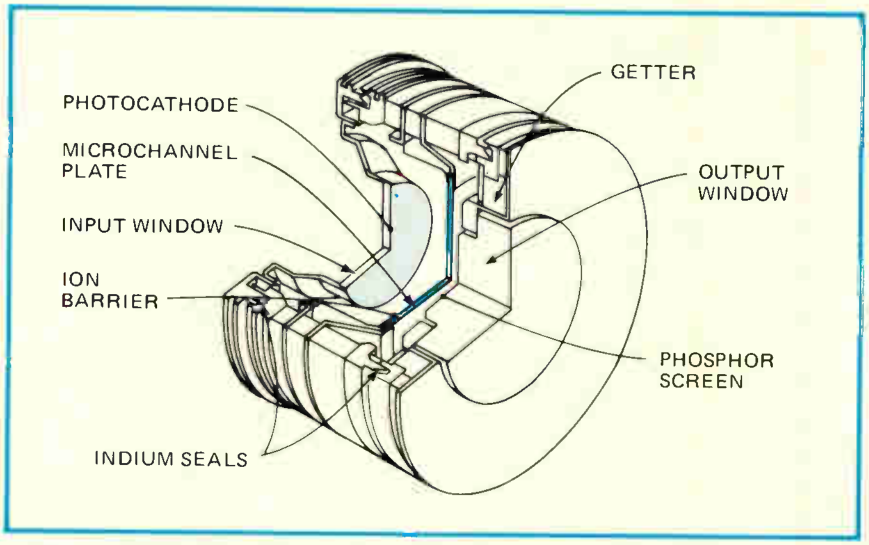
All the naysaying aside, eventual agreement seems likely. For one thing, Japanese leaders may see a policy exception for the U. S. as a politically acceptable way to mitigate U. S. demands for huge hikes in Japanese defense spending. But it appears unrealistic to expect much of a direct payoff for U. S. defense anytime soon. **-Robert Neff**

## France

# GaAs photocathode aids sight at night

Night-vision systems depend for their quality on their photosensitive element, usually a photocathode. By employing gallium arsenide in this device, French researchers have made it four times as sensitive as the last generation of S 25 photocathodes, which employ antimony, sodium, potassium, and cesium as their active element.

Thanks to the new photocathode, the prototype low-light-level imaging tube based on it is also more compact and structurally simpler than its predecessors. Developed by the Laboratoires d'Electronique et de Physique Appliquée in Limeil-Brévannes, the tube not only extends the range of human vision toward low levels of luminance but also increases its spectral sensitivity into the near infrared.




**Unusually refined.** The highly sensitive surface (tinted area) of the photocathode in this prototype low-light-level imaging tube consists of a layer of gallium arsenide only 2 $\mu$m thick.

The GaAs layer that converts these photons so efficiently into electrons is only 2 micrometers thick. The fragility of such a thin layer could have posed a problem in the fabrication of the tube.

"Since working with a 2-$\mu$m wafer of gallium arsenide is not very practical, we began with a very thick substrate of GaAs and grew the layers we needed on it by means of either liquid-phase or vapor-phase epitaxy," explains Jean-Claude Richard, a LEP engineer who worked on the development of the tube. "Then we called in the chemists who found us a method of separating the layers we wanted from the rest."

**The recipe.** The GaAs substrate is 300 $\mu$m thick, and the first step is to grow a 10-$\mu$m-thick layer of gallium aluminum arsenide on it. The 2-$\mu$m layer of GaAs is in turn grown on that layer and, finally, another 10-$\mu$m layer of GaAlAs on the 2-$\mu$m GaAs layer. After the application of a very thin nonreflective layer of silicon nitride, a glass substrate and then a sapphire window are thermally bonded to the epitaxial structure. When the GaAs substrate and the first layer of epitaxy are etched off by a series of chemical processes, the 2-$\mu$m active layer of GaAs is exposed and the rest of the fabrication is carried out under extreme vacuum.

The surface of the GaAs is first cleaned by raising its temperature to about 600° C and then activated, or given a negative electron affinity, by cesium dioxide adsorption. This modifies the dipole layer where it meets the vacuum so that the conduction band becomes higher than vacuum level. (The positive electron affinity of earlier active elements is less efficient.)

Apart from the photocathode, the tube's other elements are standard—a microchannel plate used as a multiplier, a phosphor screen, and a fiber-optic output window.

**Operation.** The tube works thus: light entering the photocathode is converted into photoelectrons, which are then multiplied by the microchannel plate. The image is formed upside down on a P20 phosphor screen and inverted by the fiber-optic window on which the screen is deposited. The only problem is that the active surface of the photocathode is in line with the microchannel plate and the ions and gases that it releases.

Since this desorption would degrade the photocathode, the tube has two vacuum chambers, one between the photocathode and the input of

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the microchannel plate, the other between the microchannel plate and the screen (see figure). Additionally, a 50-angstrom-thick film of alumina on the input surface of the microchannel plate acts as an ion barrier. The integrity of the vacuum chambers is assured by two indium seals.

Tubes made in this way perform significantly better than earlier generations. Sensitivity rises dramatically from about 250 to more than 1,000 microamperes per lumen. In addition there is a clear improvement in spectral sensitivity, and hence image contrast, with a quantum output of more than 0.25 electron for each incident photon, and resolution is 20% better.

**Undistorted.** Another advantage is inherent in the very structure of the tube. "Because the surface of the photocathode is flat, we are forced to use proximity focusing," points out Richard, "and since that means there is no enlargement of the image, there is also almost no distortion." LEP, the principal Philips research laboratory in France, will be unveiling the tube at the Exposition de Physique in Paris that will begin on Dec. 7. **-Robert T. Gallagher**

**Japan**

## Hitachi MOS FET handles high voltages, aims at world market in switching supplies

One of the ingredients that Japanese electronic-equipment manufacturers want to add to the formula that already has brought them stunning success in export markets is universal power supplies that can handle line voltages from 80 to 240 volts and thus operate almost anywhere in the world.

Such supplies should start appearing soon. Hitachi Ltd. has started off with samples of an n-channel MOS field-effect transistor with a drain-to-source rating of 800 V, the value needed for switching power supplies that work off 240 V.

The high rating is coupled with high efficiency at high switching frequencies. Even at 1 megahertz, the total loss for the new MOS FET and a small bipolar driver is only 10 watts with an input power of 100 W at 140 V. The higher the switching frequency, the smaller and lighter the power supply.

**Low loss.** At more common switching frequencies of 50 kilohertz and lower, the loss drops to a mere 2 W. Bipolar switching transistors cannot match these efficiencies because, among other reasons, the fall times of their switching pulses are from 5 to 10 times longer than those of MOS FET pulses.

Another advantage of MOS FETs is that, unlike bipolars, they are immune to thermal runaway. On top of that, Hitachi fabricates the new transistors using a triple-diffusion process that skirts the difficulties of growing thick epitaxial layers, so the devices can be competitively priced.

Siemens AG of West Germany, International Rectifier Corp., and Motorola Inc.'s Semiconductor Sector, among others, have high-voltage MOS FETs. But they are expensive and hard to come by in Japan—hence the Hitachi effort.

The new MOS FETs were developed by the company's Central Research Laboratory in Tokyo and its Takasaki works some 60 miles to the northwest. Minoru Nagata, the chief researcher involved, explains that Hitachi's new device is like many other power MOS units, made up of thousands of parallel transistors.

Each MOS FET is basically a diffusion self-aligned device in which current flows from the source through a lateral channel and then vertically to a drain contact on the back of the chip. Hitachi uses a rectangular geometry for the transistors.

**High and low.** Such transistors require a thick high-resistivity $n^-$ layer for the active region to obtain a high-voltage breakdown. However, if the chip substrate is excessively

thick, the remainder must be a highly doped, low-resistivity material for low saturation resistance.

Usually a high-resistivity epitaxial layer is grown on a low-resistivity wafer to meet these requirements. However, Nagata says that sufficiently thick epitaxial layers tend to have projections and other imperfections that degrade yield.

Rather than struggle with the epitaxy, Hitachi engineers took a page out of the book on bipolar process technology and designed a triple-diffused device. The starting material is a high-resistivity n- wafer with phosphorus diffused through the back to convert all but the top 90 micrometers of a 250-$\mu$m-thick substrate into a highly doped low-resistivity region. Conventional double diffusion is then used to fabricate the silicon-gate devices.

**The final picture.** The completed parts have about 5,000 unit transistors in parallel, each measuring 90 by 90 $\mu$m on a chip that measures 6.7 by 6.7 millimeters. The maximum drain-current rating is 5 amperes, with a typical saturation resistance of only 1.7 ohms.

The device, which comes packaged in a TO-3 can, has a maximum dissipation of 125 W. In many well-designed applications, however, the power-handling capability is limited by the drain current rather than the dissipation rating.

Besides switching power supplies, the transistors can be used in dc-dc converters, ultrasonic power oscillators, and rf amplifiers. The cutoff frequency is about 2 MHz.

Hitachi is now offering samples of the devices and expects to be producing them at the rate of about 5,000 units per month by sometime next spring. Genro Takemura, a senior applications engineer at the Takasai works, says in addition that the firm can increase production to between 5,000 and 10,000 devices a month within three months after orders are received.

In Japan the sample price for the new transistor (designated 2SK351) is \$17, falling to \$12.60 in lots of 1,000; U. S. prices are \$25 and \$19 respectively. **-Charles Cohen**

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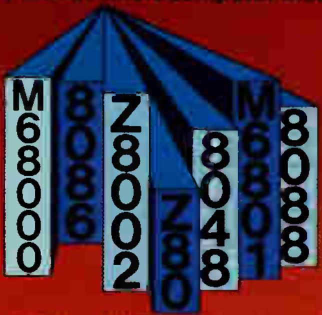


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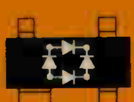
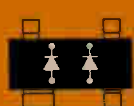


The planar silicon diode bridge BGX 50A – presumably "the world's smallest bridge" – offers full-wave rectification up to the MHz range (70 V, 200 mA, 350 mW).



The planar silicon duo diodes BAW 56G and GT each consist of two separated medium-fast diodes for reverse voltages of 70 or > 300 V, respectively. Their advantages: more flexible circuit design, simplified storage.

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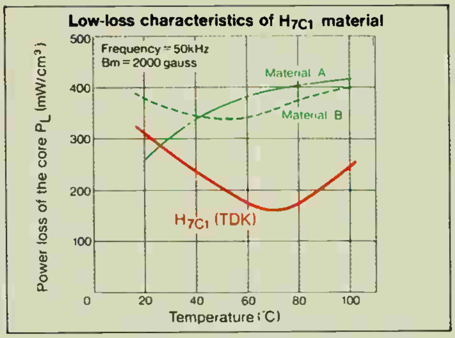


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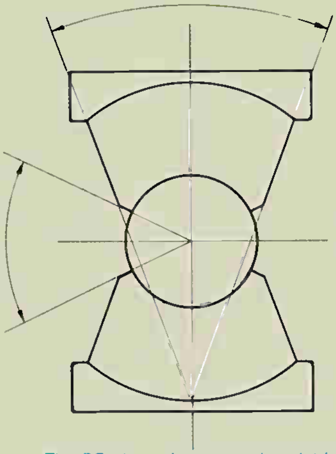

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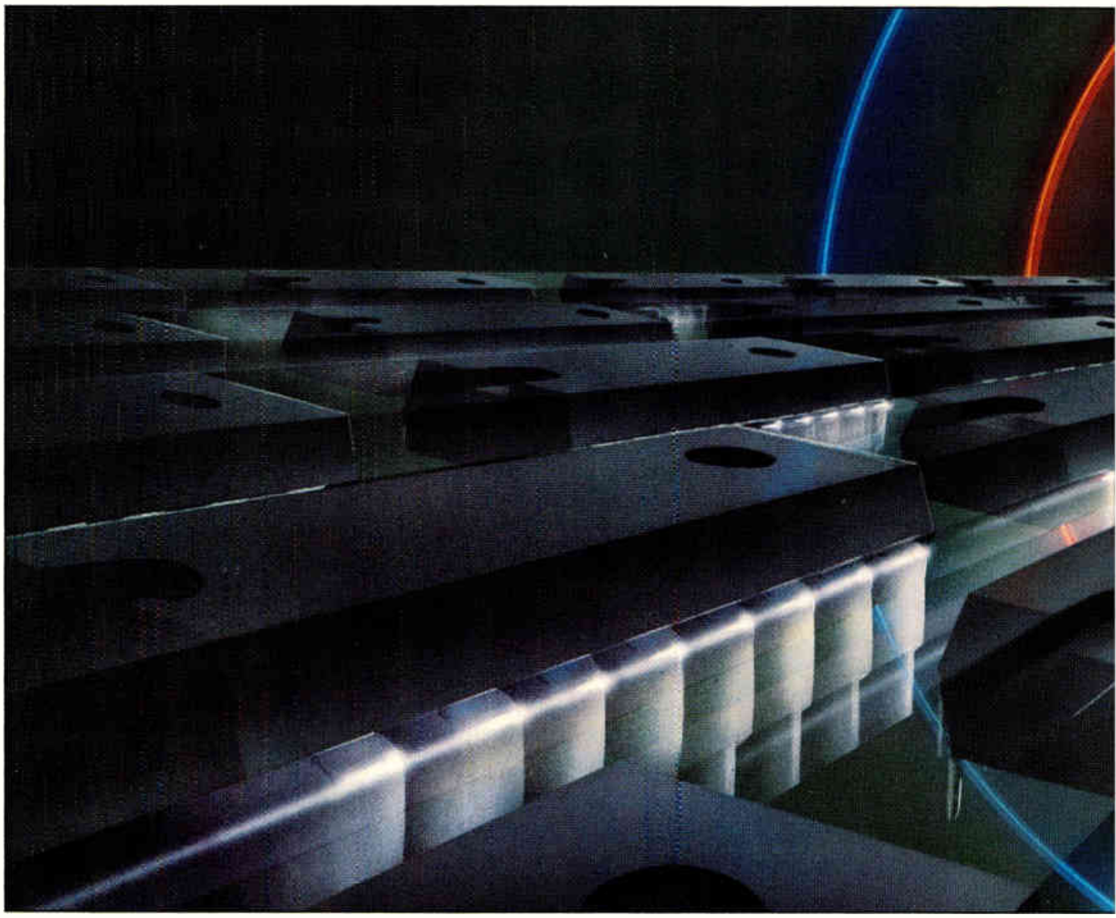

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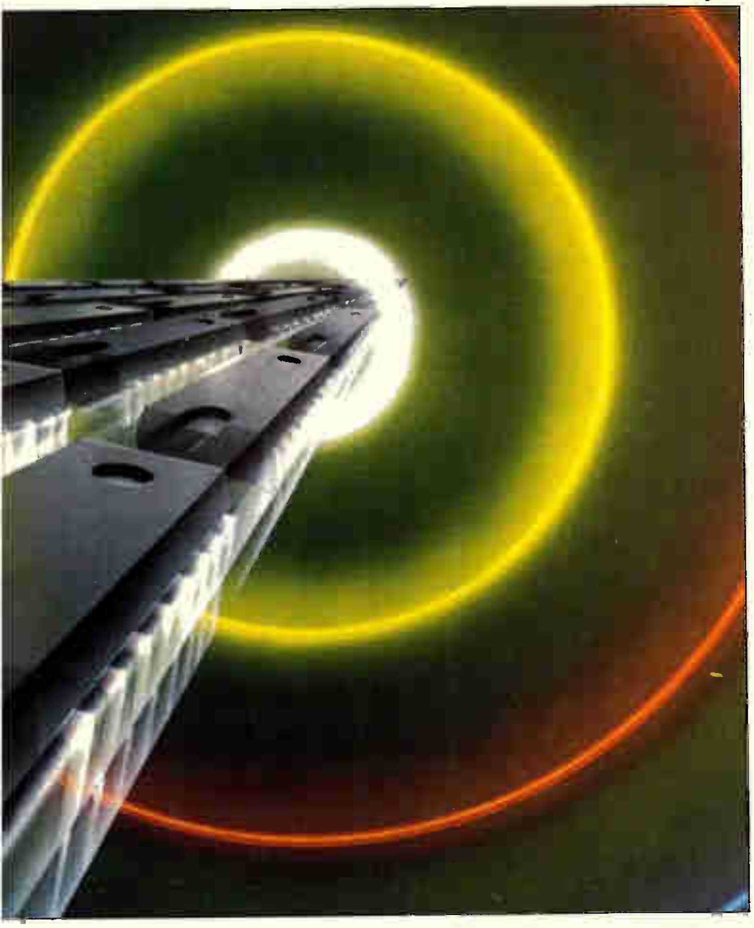

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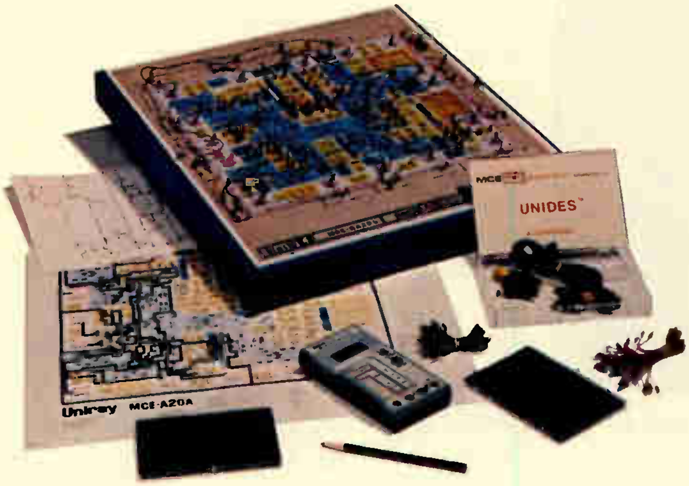


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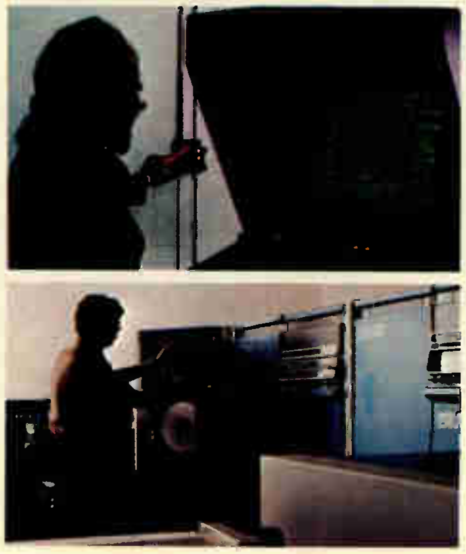

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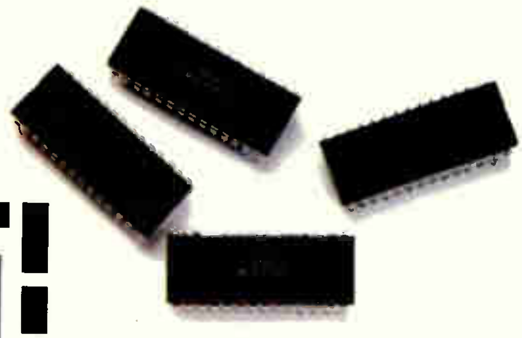


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# Silicon foundries gaining adherents

## But others in semiconductor industry question whether such operations are meeting a long-term need

*by Larry Waller, Los Angeles bureau*

**With most pieces** finally falling into place so a thorough test may be given to the trendy silicon-foundry idea, the pro and con battle line is already forming. According to popular opinion, foundries will either sweep through the semiconductor industry as the wave of the future or fade into the background as increased demand once again spurs sales of the standard devices that currently make up the backbone of the business.

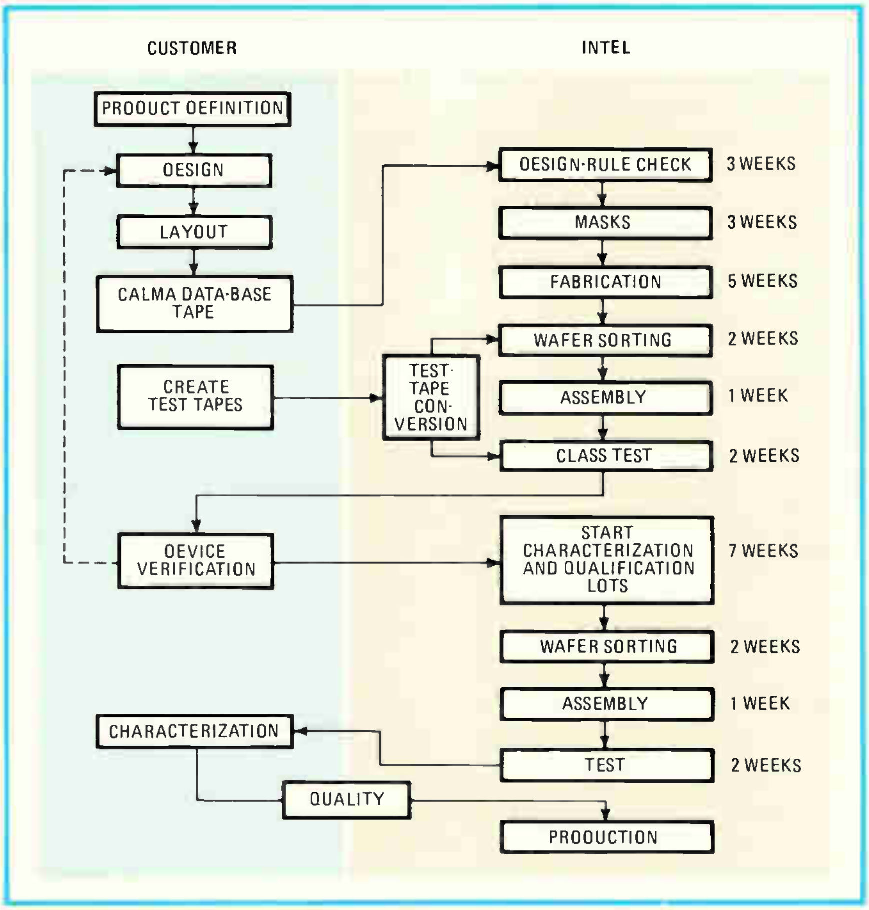
It is too early now to judge how foundries will fare, but the opinions of those involved as participants and interested observers help shed some light. The overriding issue is major, nothing less than "how we will do LSI [large-scale integration] of the 1980s," says an analyst at the worldwide consulting firm McKinsey & Co., which has studied the question for its clients.

What appears to be the sudden interest in foundries is gaining impetus from a number of converging factors. Perhaps most interesting to market watchers is the increase in excess fabrication capacity that has been caused by expansion followed by soft demand. Another is the growth in available design-automation software. Finally, and possibly most important, is the mushrooming need for custom chips.

Helping to intensify the present interest is the decision of Intel Corp., which moved with considerable fanfare in late summer to position itself strongly in the foundry business. The Santa Clara, Calif., firm, a leading innovator in semiconductors, is devoting substantial resources to establish a foundry in Chandler, Ariz., and is shooting for $100 million in sales from it by 1985 [*Electronics*, Sept. 8, p. 39].

Furthermore, it not only is offering its most advanced processes to customers, but is willing to take orders for 10,000 to 20,000 integrated circuits. This quantity is far less than what a major semiconductor house previously would touch.

A few skeptics who wonder what all the fuss is about say that the only thing new about foundries is the term itself (coined by Intel chairman Gordon E. Moore in the mid 1970s). "What's the big deal about Intel jumping in?" ask officials at both American Microsystems Inc. and National Semiconductor Corp., the clear volume leaders. AMI does some $75 million a year as a foundry and National perhaps half of that,




**Who does what.** Intel provides this chart delineating its and customers' responsibilities in its silicon-foundry activities. Firm's entry into the foundry business has helped quicken interest in the concept as well as heat up the debate about its merits.

sources in the industry say.

At both firms, the mood is to welcome Intel's entry as confirmation of the market potential. "I don't see Intel hurting us," says Cliff Vaughn, AMI's product manager for custom-designed products. "The business is growing like mad." Market projections are nebulous at best, but Intel's vice chairman, Robert N. Noyce, estimates that the market could reach $680 million annually by 1985, from today's $135 million.

Intel is jumping into the foundry fracas with strength by offering its most advanced processes, including H-MOS (high-performance MOS) and complementary H-MOS. The company has two foundry customers now, with prototype production of devices planned for early 1982, according to Robert Dahlberg, who is customer program manager.

**Sophisticated users.** Although the objective is eventually to serve some first-time users, Dahlberg states that at present only "sophisticated customers who know what they are doing" can be handled. One widespread doubt concerns Intel's continuing commitment to its foundry when the demand for standards turns up, although Moore and Noyce say emphatically they are in the field for the long haul. Although it is too early to give out odds, a financial analyst who closely follows Intel backs them strongly.

James Magid of New York's L. F. Rothschild, Unterberg & Towbin says that Intel will not abandon foundries, but could well expand the business from 1983 on. Moreover, Magid does not believe excess capacity is the issue "because Intel alone is offering state-of-the-art processes." The mature processes offered by all the rest are what will be in oversupply, he adds.

In addition, Magid's projections show that when Intel's foundry operation is in full swing, it should be a very profitable enterprise, throwing off higher gross-profit margins than even high-volume standard devices. The reason is that foundry work is interleaved with other production, with the major investment made only in marketing and customer service, says Intel's Dahlberg.

But whatever experts believe the long-range effects of foundries will be, all hands agree that the most immediate effect will be felt most by captive semiconductor producers. "I know of one [plan] already dropped," says Howard Dicken, president of Integrated Circuit Engineering, Scottsdale, Ariz., which counsels on the subject. Moreover, "many in the offing are being reexamined," he says, in light of Intel's move and other foundry offerings. Financial analyst Magid goes further, saying "captives are a glorious mutant" that have seen their day.

Nevertheless, doubts still persist among knowledgeable industry veterans. A representative view comes from William Howard, vice president for technology and planning at Motorola Inc.'s Semiconductor Business Sector. "I'm not sure a pure foundry can exist as a business proposition," he says, since volumes and competitive pricing may not support it. Intel is not a pure foundry and more resembles a company doing semicustom work for big quantity customers, which most major houses already do, he adds.

And looming over the subject is a market question that is basic to the future of the foundry. "How fast and to what degree would successful silicon foundries erode standard-device sales," is how Robert J. Conrads phrases it. He is a principal at McKinsey's Los Angeles office who is trying to provide some guidelines to Japanese clients. "This is the heart of the matter."

**An Eastern view.** The Japanese view of U. S. foundry developments starts with a professed lack of information, which most U. S. observers dismiss as a typical strategem. McKinsey already has done a detailed study for one unnamed Japanese client, and U. S. technologists who visit the islands report their counterparts well-informed.

Tadaski Tarui, chief engineer of the Semiconductor division at Toshiba Corp. says his firm would consider doing foundry work if asked, but nobody has. He believes, however, that the Intel move is "one wave of the future."

He notes that Toshiba would give out design rules, but not process details. Officials at two other major firms, Nippon Electric Co. and Hitachi Ltd., say they would consider offering foundry services on a case-by-case basis. □

## Opening the foundry's doors

How is a pure silicon foundry—one that does no other business—organized? For one of the few such firms in existence—Microcircuit Engineering Inc. of West Palm Beach, Fla. —the key is decentralization.

The company was started in 1977 by James D. Norrish. Besides its Florida operation, it now has one in Sunnyvale, Calif., and a third in Nüremberg, West Germany. The West Palm Beach site is a prototype. The plant encompasses 30,000 square feet; the equipment is less than two years old. Its computer-controlled diffusion furnaces can handle 4-inch wafers, and the plant has automated-layout systems, projection aligners, plasma etchers, ion-implantation systems, laser trimmers, and a variety of other gear.

A number of technologies are available, suited to linear as well as digital circuits: integrated-injection logic, for instance. There is also a power linear integrated-circuit capability. In addition to Schottky TTL and MOS, technologies that merge both bipolar and field-effect transistors are available.

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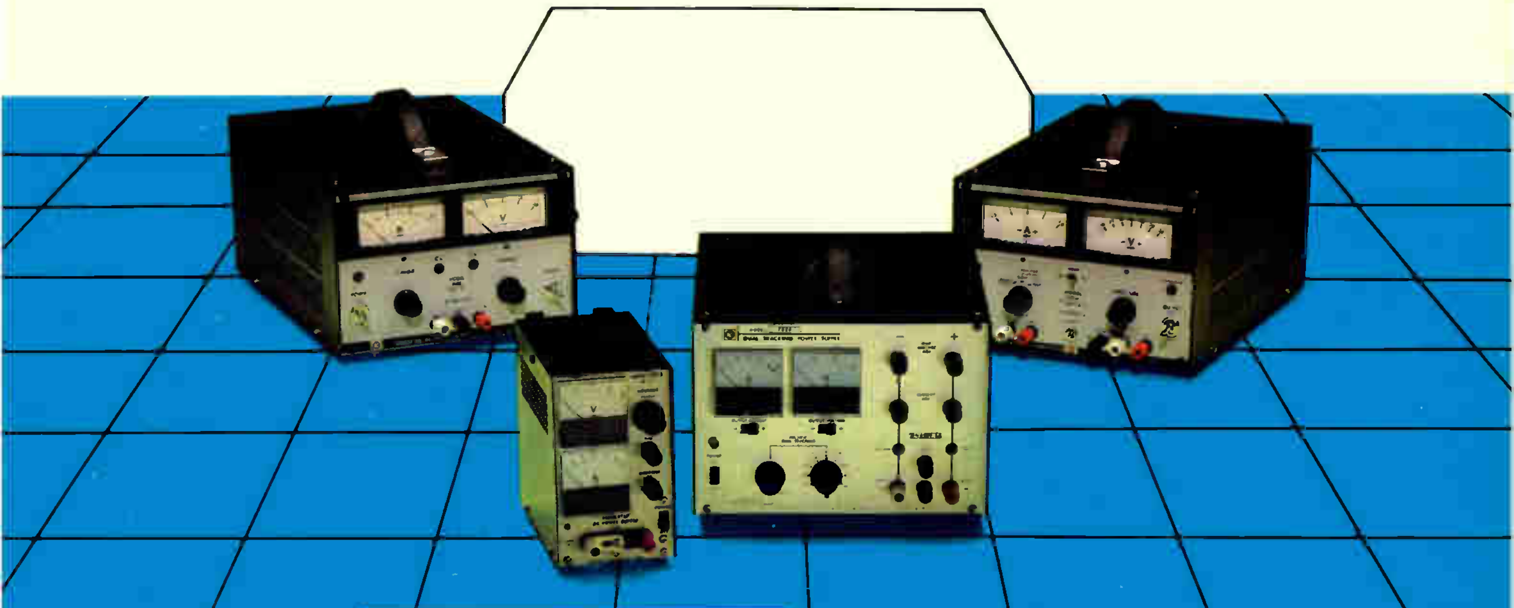

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Telecommunications

# IC makers turn to telecommunications

Switchover to digital techniques makes market attractive, with systems houses expected to rely less on in-house work

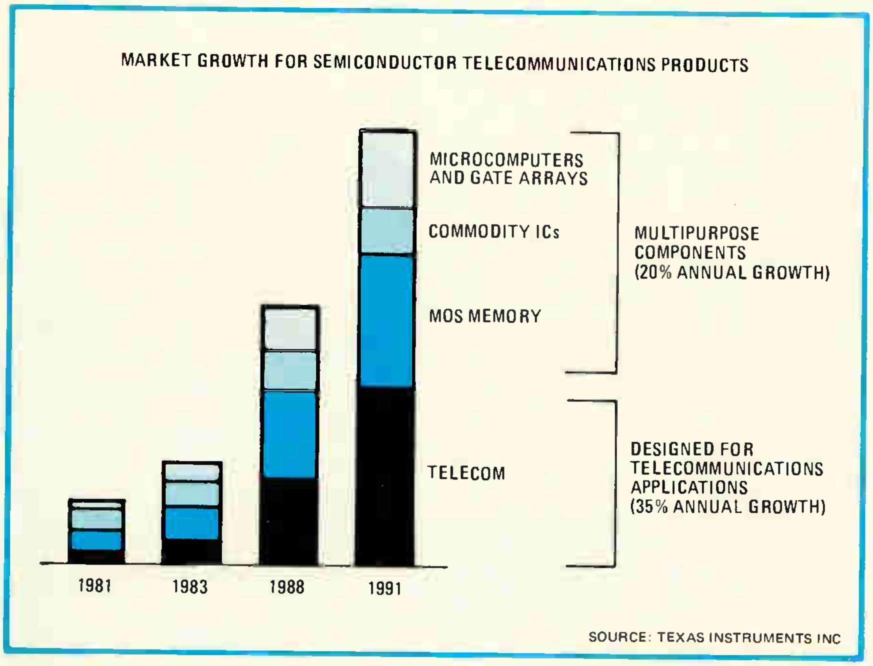
*by J. Robert Lineback, Dallas bureau*

**While semiconductor activity** remains in a slump, many integrated-circuit manufacturers are shifting more of their attention to telecommunications markets—which by some estimates will be ringing up nearly $10 billion in worldwide noncaptive IC sales at the end of the decade. And as these volumes grow and prices drop, telecom system giants, which currently rely heavily on in-house design and production, are expected to bring more of their business to the merchant market.

Although it has been relatively slow in coming over the past two decades, a good portion of telecom's analog-to-digital evolution will be completed by 1990. By then, digital phone sets will be the rage—each unit loaded with very large-scale ICs. Many of these phones will resemble today's computer terminals with video display screens and data-communication capabilities. But the telephone evolution is currently hung up on the analog nature of voice itself and on the herculean task of replacing thousands of miles of existing analog networks and their associated switches.

In the interim, the tricky job of interfacing analog and digital worlds together over phone lines has resulted in a whole new breed of ICs dedicated strictly to telecommunication functions—such as coder-decoders, filters, and subscriber-loop interface circuits.

Currently, these dedicated components make up only a small fraction of semiconductor sales to telecom firms. But system manufacturers and IC houses agree that the rate of growth will be much greater than the increasing consumption of multipurpose components, like microprocessors and memories.




Predicting a 35% annual growth rate for dedicated telecom devices (see chart), Texas Instruments Inc. recently announced entry into the field. TI, which already is a leading supplier of multipurpose devices to the market, predicts that sales of ICs specifically designed for telecom applications will be well over $3 billion in 10 years.

The Dallas firm also believes these dedicated parts will be crucial in capturing future multipurpose-component business in the telecom market. Although the growth rate is lower (20%), multipurpose ICs will continue to form the bulk of semiconductor activity in the market, with sales hitting $7 billion in 1991, according to TI forecasts.

In Chandler, Ariz., Intel Corp.'s telecommunications marketing manager, Anthony Livingston, places total noncaptive telecom sales "at a little less than 20% of the entire IC market." He also agrees that the dedicated-component segments are showing the highest growth potential. Currently, Livingston estimates that the dedicated telecom device market stands at a little less than $100 million.

**Top five.** Motorola Inc.'s Semiconductor Operation has identified telecommunications circuits as being one of its top five IC business priorities according to Robert Karasch, who heads up the marketing efforts of the dedicated parts in Austin, Texas. "I think what you see is a lot of companies with products just coming on the market. So we have very high growth, 40%-to-50% type of numbers, but starting from a low

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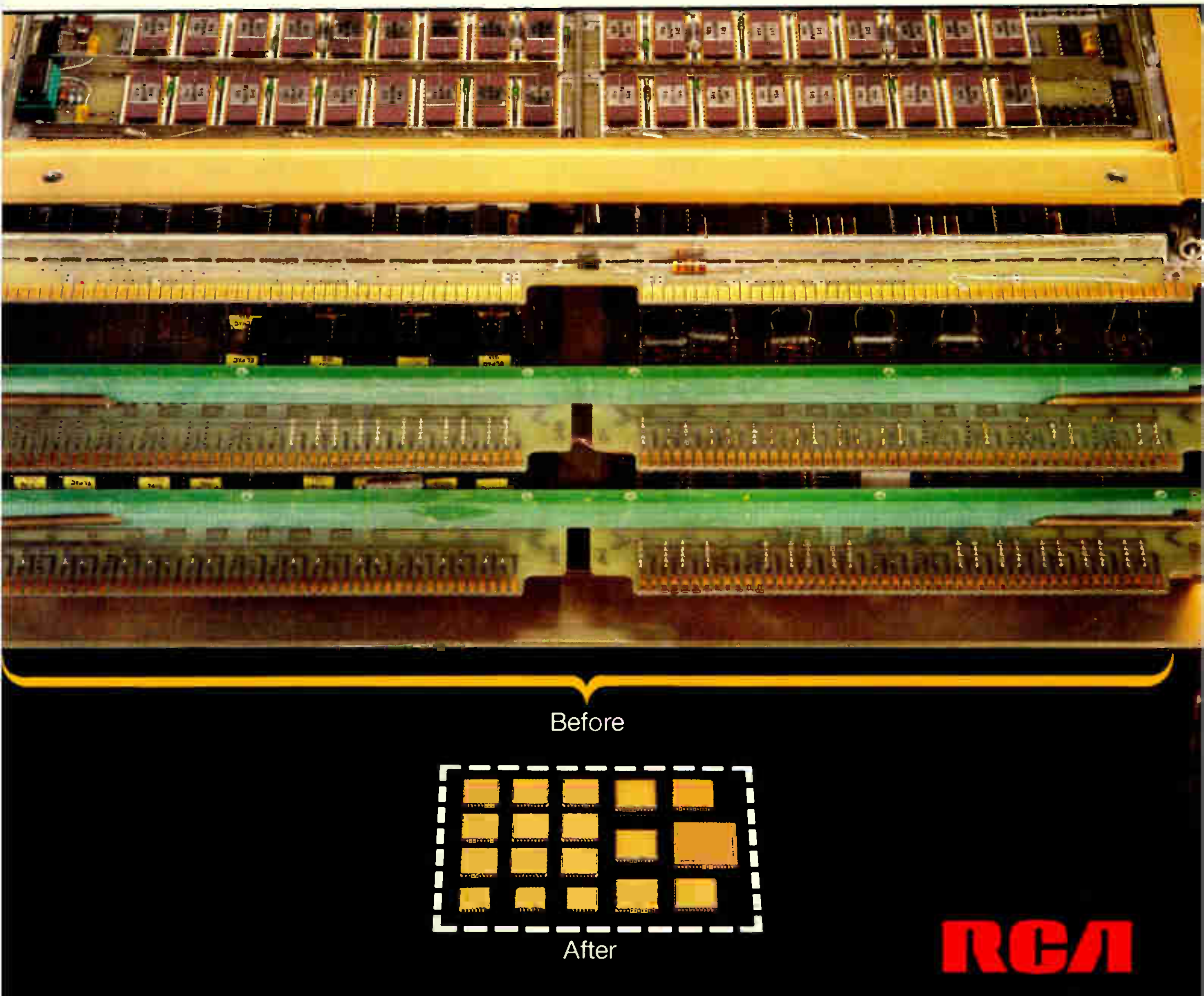


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## TI rings the bell

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The ringers are part of a series of products bringing TI into the dedicated telecommunication integrated-circuit business. In addition to these chips, the Dallas firm will be unveiling six other telecommunications devices in December, including: two bipolar-FET speech amplifiers; one bipolar speech amp; a bipolar bridge IC; a metal-gate complementary-MOS tone encoder; and a silicon-gate n-MOS codec. TI has introduced nine telecom ICs in the past two months. Rounding out the first of these announcements will be a silicon-gate n-MOS switch capacitor to be available in January [*Electronics*, Oct. 6, p. 44].

In mid-1982 and 1983, TI plans to add to the line of dedicated parts with the introduction of several new devices such as subscriber-loop interface circuits and modem chips—made from scaled n-MOS, advanced silicon-gate C-MOS, and 250-V Bid-FET technologies. **-J. R. B.**

base," Karasch explains. "Because many telecom products are just now going into production, I think you've got a new business that is really taking off."

The story is the same at Mostek Corp. in Carrollton, Texas, which has been particularly hard hit by eroding prices in worldwide MOS memory markets. "Although 1981 has not been as good as we anticipated, we are still showing strong growth and we are looking for a very, very strong year in 1982," says Robert Merritt, marketing manager of the company's telecommunications department.

Merritt agrees with projections that the total telecom semiconductor market could hit $10 billion by 1990, but cautions, "It can be hard to say how fast telecommunications will grow because it has a number of variables: how fast will electronic funds transfer grow? Or, what's going to be the impact of videotex markets? What's going to be the impact of telephone deregulation? And so on."

While there is broad agreement that dedicated ICs for telecom will experience a market boom in the 1980s, there is also the belief that programmable components will begin to play a growing role in the last half of the decade. With software, signal processors can do filtering and other telephony functions.

Meanwhile, many participants in the telecom market anticipate a possible shift in production philosophy at many of the large equipment houses. In the past decade, many of these systems houses invested in research and development labs and fabrication facilities to produce their own semiconductors, which at the time were virtually nonexistent on the merchant market.

They also sought to gain a competitive edge. In an attempt to protect their own IC designs, many established semiconductor lines. But the cost of maintaining state-of-the-art processing is apparently driving some back to IC vendors.

**Another source.** "Anytime that you get into high-volume usage—which of course is of interest to the IC manufacturers—we certainly want a second source for supplies," admits John C. Redmond, vice president of research and development for GTE's Communications Products group. "But one of the keys to this industry is how well we adopt uniform standards. The more things become standard across the industry, the more there will be opportunities for high-volume production of circuits by IC manufacturers."

The Bell System, which began its move toward a nationwide digital network in the early 1960s, indicates it will continue to study the capabilities of outside components. But there are indications that many telecommunication systems houses are already feeling the burden of fabricating high volumes of ICs, says Intel's Livingston.

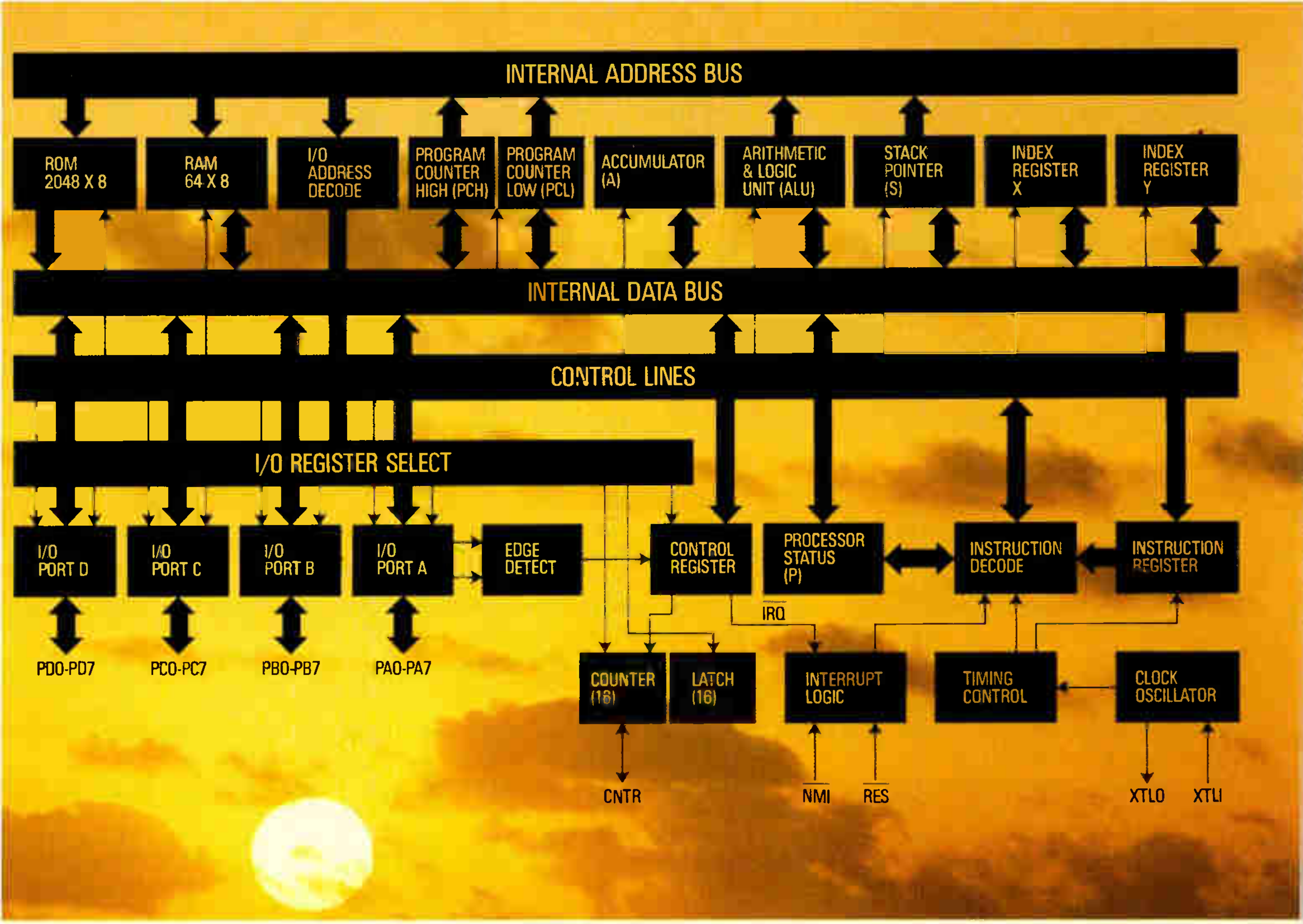
"VLSI is increasingly becoming a key strategic element and some manufacturers are committed to an in-house capability. But now some are turning back to the merchant market, which can provide the kinds of capacity that will be needed," he explains. "I think you will see increasing joint efforts between vendors and equipment designers of future generations of special ICs and an increase in the use of silicon foundries" (see p. 81).

Industry analyst James Barlage of Smith Barney, Harris Upham & Co. in New York observes, "What these companies are finding out is that to keep up with process technology is much harder than they thought."

**Moving away.** But on the other side of the coin, says Livingston, a new wave of telecom firms is beginning to invest in limited in-house manufacturing lines for prototyping and production of parts that are not available on the market. "The trend seems to be that those that have invested in the past are now turning back to merchant markets," he adds. "But, there are those who are just now investing in fabs as a key strategic element in market plans," says the Intel marketer.

Mostek's Merritt agrees that more telecom IC business will be moving to vendors and away from in-house production facilities. However, he still sees some apprehension. "I think that one of the problems is that even though these parts are off the shelf, customer specifications often cause the end product to be different from others—codec-filter chips must be coupled to systems."

Karasch at Motorola believes in-house production operations are normally less cost-efficient because of "economies of scale. They also don't have things like offshore facilities to hold costs down," he notes. "I can see them maintaining their design expertise and maintaining some of their in-house capabilities, but they will work with major semiconductor manufacturers in doing mask-provided circuits." □

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Data communications

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## But the analyses saying Xerox's digital network will fail to dominate the market draw quick rebuttals

by Martin Marshall, San Francisco regional bureau

**Earlier this month,** the president of a small industry-analysis firm in San Jose, Calif., called Strategic Inc. summoned his researchers into his office. He told them that the firm had completed and was about to publicize a study that concludes that Xerox Corp. is headed for the worst failure in its history.

"Xerox's Office Products division strategy, based on Ethernet, will fail, and it will happen within two years," asserts Michael Killen. "The failure will be of greater magnitude than Xerox's previous failures with Daconics, Xten, and even the SDS bath." Realizing that his report, entitled "Xerox—the Key Issues," may be regarded as spitting against the wind of Xerox's movements and those of the community of Ethernet suppliers, Killen further underlined his belief by saying, "I would bet my company on it, and I'd bet my future on it."

Meanwhile, a second study was emerging independently at Venture Development Corp. in Wellesley, Mass. Titled "Local Area Networks, 1981 to 1990: a Strategic Analysis," it reached conclusions that were not as extreme as Strategic's. It did warn, however, that "some large companies may be hitching their wagon to the wrong star. Ethernet has limited growth potential."

VDC drew three scenarios for the future of local-networking schemes, but the one it considers the most probable is that of "a technological jungle in which the marketplace is filled with different, innovative products, each fighting for its share on the basis of improved price-performance ratios." Says Edward A. Ross, manager of VDC's Communications division: "We expect a shakeout to occur in the 1983–85 timeframe, and probably several designs will be prevalent after that shakeout."

As Killen sees it, "by the time that Xerox and [its Ethernet partners], DEC and Intel, build up a significant Ethernet capability, the world will have changed. There will be a million non-Ethernet competitors out there." Surprisingly, Killen says that the factors that persuaded him to make such strong statements about Ethernet were the Xerox sales organization and customer base. "The copier sales force doesn't count on products of this nature, and beyond the copier base Xerox does not have a sufficient customer base in office equipment to leverage upward migration."

Penetration of the Fortune 1,000 companies is the key, he asserts, and he believes those companies will opt for networks including voice and video capabilities. "Today, voice is not an issue, but in 1982 it will become a major issue. A few years after that, video conferencing will become important," he predicts. The net result, he believes, is that some customers will go on a holding pattern rather

### Puncturing some Ethernet myths

William Krause, president of 3Com Corp., a Mountain View, Calif., vendor of Ethernet-networking equipment, believes that four myths that have grown up around Ethernet can be dispelled by a closer look.

The first is that, if Ethernet is not a dominant standard, it will not penetrate the large buildings of large companies. "The answer to that is that there will be no single standard and there will be lots of cables coexisting in the building," he says. Krause believes that Ethernet will be one of the set of wires in a building, but will not exclude others.

A second myth is that Ethernet cannot carry voice. Krause notes that at the 64-kilohertz bandwidth used for high-quality voice, the 10-megabit bandwidth of Ethernet could carry 150 real-time conversations. Xerox's Donald J. Massaro, president of the Office Products division, lends further credence to this by promising that by 1983, Xerox will provide a gateway to integrating the telephone into Ethernet. Krause adds that Bell Telephone is currently conducting experiments on a real-time voice system using Ethernet.

The third myth is the need for continuous video in the office. "There will not be a video camera per work station," he asserts. "If someone needs a video conference, he will go to the video-conference room."

Yet another myth is that Ethernet is suitable only for the office environment and that it is too expensive. "Fully 50% of our customers are in the manufacturing environment with CAD, ATE, and CAM [computer-aided design, automatic test equipment, and computer-aided manufacturing] systems," says Krause. "This is where huge files must be transferred back and forth." As for the cost factor, he points to the fact that Intel, Advanced Micro Devices, Mostek, and Fujitsu have announced that they will manufacture Ethernet large-scale integrated circuits. "These will be the UARTs [universal asynchronous receiver-transmitters] of the 1980s, and they will make cost-effectiveness Ethernet's biggest asset," Krause declares. **-M. M.**


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## Probing the news

than buy Ethernet systems, some will buy systems based on private branch exchanges, and some will buy broadband networks like Wangnet.

**Quick reaction.** The reaction from Xerox was immediate. At the Nov. 17 introduction of its Ethernet-connected Memorywriters, one spokesman retorted that "that's the sort of thing you have to do to sell reports. No one wants to buy a report that says that Xerox or IBM is doing the right thing." At an American Electronics Association meeting the next day, Donald J. Massaro, president of Xerox Office Products division, addressed the question of wiring large buildings of Fortune 1,000 companies with Ethernet.

"You would not need the network in every area of the building at first," he cautioned. He revealed that the Pentagon has asked to be completely wired for Ethernet and that Xerox's advice was that it not do the entire building. "We recommended that areas be networked first, and then they could add to the system when needed," said Massaro.

**No video.** Massaro acknowledges that "Ethernet will never be able to do video, but there is little use for that in the office." He declined to forecast a dollar volume for the local-network market, however, saying, "We have not placed a figure on the network itself because that is not what will make money. It's the equipment that you will be attaching to the networks that manufacturers are interested in."

It may be that the differences of opinion result from the question not of whether Ethernet will do well, but of whether it will dominate the local network market. VDC itself projects that local-networking equipment for local networks will be a $1 billion market by 1990, while William Krause, president of 3Com Corp. of Mountain View, Calif., an Ethernet-networking equipment vendor, predicts that by 1985 there will be $3 billion worth of automation equipment connected to Ethernet. The huge spread between the two projections is partly due to the fact that, for example, the price of a terminal connected to Ethernet would be included in the 3Com projection, but not in the projection from VDC.

Dataquest Inc. of Cupertino, Calif., has its own predictions about local networks. "We separate it into two types, the high-cost systems that will connect mainframe computers and the lower-cost ones such as Ethernet and Datapoint," says Martin Fletcher, vice president of Dataquest in charge of its telecommunications service. "We expect to see higher-cost networking equipment at $75 million in 1985, and lower-cost networking equipment at $175 million in 1985."

VDC's Ross points to the "limited growth potential" of Ethernet as a drawback, noting that "Ethernet has no access control and no prioritizing, which means that a long message can hold up a short, important one." Moreover, delays due to distance on the cable could result in a significant number of data-packet collisions as the traffic on the net got heavy. He admits, though, that these would not be a problem at the 1% to 3% utilization rate used by many designers.

He also points out that Ethernet is "not suitable for synchronous transmission" of the kind that characterizes computer exchanges. "The problem is not with the Xerox marketing muscle. It's that the Ethernet system is suboptimal. For small systems and office-automation equipment, Ethernet may be just what the doctor ordered, but for the kind of thing the Fortune 500 companies want, it will require broadband and some access control," he asserts.

**Good enough.** Dataquest's Fletcher agrees that Ethernet is an imperfect system, but says that "a standard does not have to be optimum. It must have adequate capability. It must handle the majority of requirements in an adequate and cost-effective manner. It must be timely, in that it must be available before too many other systems have secured a foothold. And it must have the sponsorship of major manufacturers." Ethernet, Fletcher believes, can be made to fit the standards mold. "It will become, at very least, a *de facto* standard, although there will continue to be several networks. Ethernet will be the dominant noncaptive system, with significant penetration by people like IBM and Wang." ☐

training but few business skills," Hodges notes. "We'd like to help them avoid the managerial pitfalls that can wreck technological ideas."

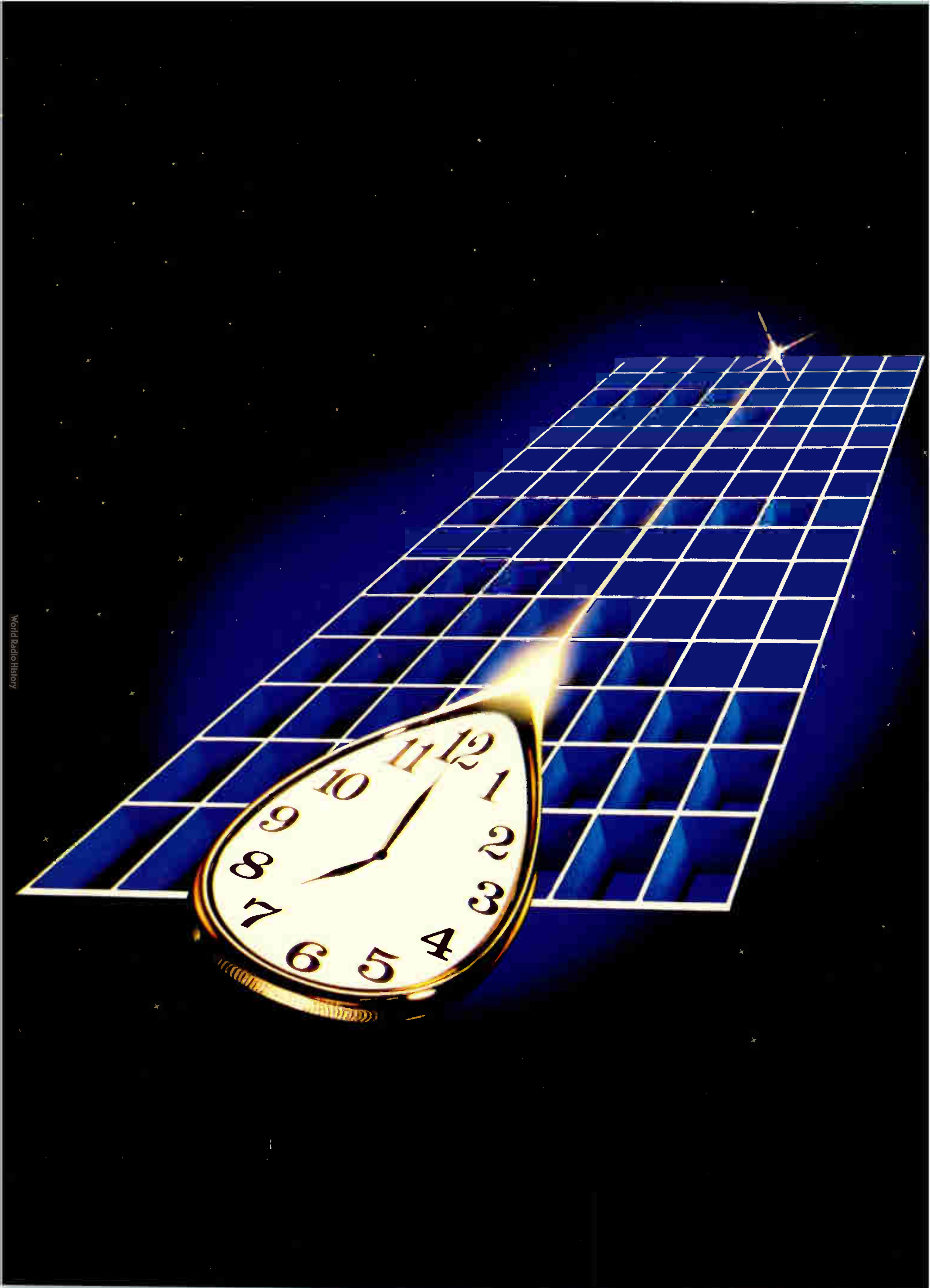
One such advisory committee has already come together. The beneficiary is MicroCompatible Inc., a year-old venture renting temporary space at Georgia Tech. MicroCompatible's consulting group consists of a corporate attorney, a marketing expert, and the president of a local software firm. Meetings with the start-up's founders occur monthly to review company progress and suggest future strategy.

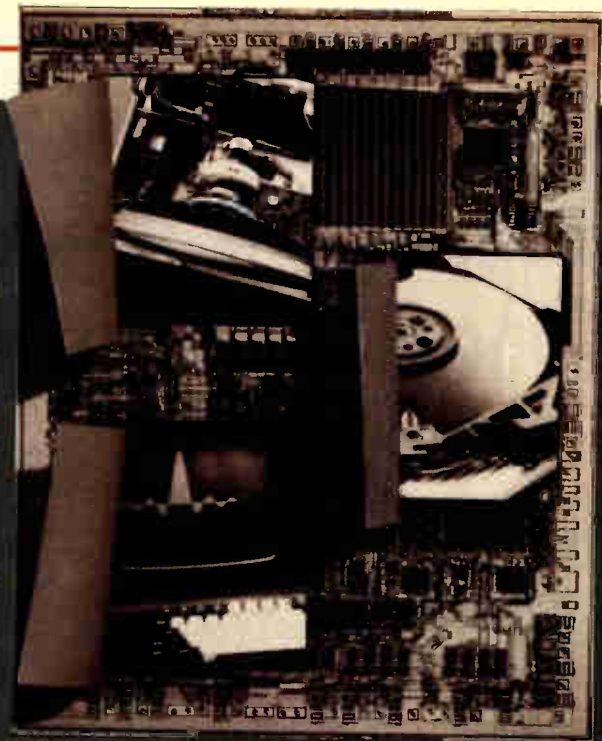
**Profit seen.** The first of its type, Control Data's co-op program, initially tried out in 1979, serves as a model for projects like RPI's and Georgia Tech's. But beyond its commitment to helping new ventures, CDC believes its business and technology centers can also be moneymaking propositions. The company establishes BTC services on such a large scale that it can rent them very widely, not just to start-ups occupying space in the centers, says Walter Bruning, vice president of retail marketing. Further, he adds, CDC may invite outside-investors' participation in future such centers.

Besides those already in operation, CDC plans other centers for Boston, Philadelphia, Miami, Baltimore, San Antonio, Texas, and Charleston, S. C. They can be located in new or renovated buildings with room for dozens of small firms.

Not only high-technology companies find their way to BTCs—according to Bruning, any new venture is a candidate for housing and services, including shared secretarial help, laboratory and light-manufacturing facilities, technical libraries, financial and legal advice, and access to CDC's vast computer network.

The large cooperative program's glittering array of resources brings sighs of envy back at the makeshift Cambridge co-op. "I'd sure like to see MIT have a program like that," says Dezmelyk. At CDC, RPI, and Georgia Tech, no one is complaining of difficulties finding enough struggling, interested entrepreneurs to make the effort worthwhile. □





# Bipolar VLSI builds 16-bit controller handling many fast peripherals at once

Special-purpose microprocessor has controller instruction set in microcode, manipulates three operands in one cycle

by Sunil Joshi, Deepak Mithani, and Steve Stephansen
*Advanced Micro Devices Inc., Sunnyvale, Calif.*

☐ In the last decade, peripheral controllers have evolved from little more than simple input/output ports into highly sophisticated dedicated processors that command the level of performance necessary for handling high data rates. They also must now provide intelligent pre- and post-processing of data to offload from the host computer the specialized tasks intelligent controllers perform.

Recognizing the need for such a processor, Advanced Micro Devices has combined its proprietary Imox processing technology with a bipolar circuit design of scaled emitter-coupled logic based on very large-scale integration to produce the Am29116 16-bit bipolar microprocessor. The largest and the most complex bipolar device ever produced, the 29116 has an architecture and an instruction set specifically designed for high-performance, intelligent peripheral controllers. The high performance is a result of its unique architecture, microprogrammable instruction set, and processing technology; its requisite high speed is achieved by designing the part in ECL with TTL-compatible levels at the pins (see "What is microprogramming?" p. 100).

The instruction set of the 29116 has extensive data and bit manipulation capability to mask, rotate-and-merge, or rotate-and-compare, data in one microcycle—functions that are useful for field extraction, field insertion, and data alignment, which are frequently encountered in controllers. The architecture provides flexibility and parallelism in the data paths so that the device can perform in one microcycle a complex function that would take other processors several cycles to execute. One such feature is the barrel shifter, which rotates a 16-bit word by up to 15 places in one microcycle before the arithmetic operation is performed. The part also has an on-chip priority encoder and cyclic-redundancy-checking logic for specialized functions.

Created for a microprogrammed environment, the 29116 gives the user the flexibility to tailor the controller architecture for a specific application. MOS microprocessors, with their fixed architecture and instruction set, are limited in this respect. The performance is at least an order of magnitude higher than that of any available MOS device (see "Imox: a union of TTL and ECL," p. 102).

The 52-pin device has a microcycle time of 100 nanoseconds. In one cycle, the three-input arithmetic-and-logic unit operates on one, two, or three operands, while the barrel shifter is rotating one of the operands before it is used for an operation. The part also has a single-port register file that is 32 words deep by 16 bits wide and a dedicated accumulator to store temporary results. In this way, the advantages of both register-based and accumulator-based machines can be obtained (Fig. 1).

### Bidirectional busing

The bidirectional 16-bit Y-bus is the primary off-chip data input and output port. The 16-bit D-latch at the input allows the data to be presented directly to the ALU, or be latched and used in the next cycle. This latch can thus be used as a pipeline for prefetching data while the ALU is performing a different function. It is also possible to bring data onto the chip on the Y-bus, perform some function on it, and then send it out again on the same bus without even having to store it.

The priority encoder generates a binary coded number, indicating the most significant bit in the operand that is a one. This special-purpose hardware module saves a significant amount of time, since a subroutine is ordinarily required to perform this often-used operation.

The status register is clocked with the ALU every cycle and can even contain user-defined status bits whose function is defined by the microcode. Using microinstructions, it is also possible to provide a condition-test output based on the status. The bidirectional T-bus, when used as an input, exploits the device's parallelism further by allowing the user to select a condition for branching, while simultaneously executing an instruction in the ALU. The user can also select separate read and write addresses for the same instruction in both the byte and 16-bit word modes.

In addition to having full-carry lookahead across all 16 bits, the ALU executes all the conventional one- and two-operand instructions, such as move, complement, 2's complement, add, subtract, AND, NAND, OR, NOR, exclusive-OR, and exclusive-NOR.

### Masking in a microcycle

Where the 29116 departs from convention is in its ability to operate on three operands simultaneously in a single microcycle. Thus a bit field can be selected from the two data operands with a masking operand all in a single microcycle.

The ALU produces three status outputs: overflow, negative, and carry. The zero flag, although not generated by the ALU, detects zero at both the byte and word level. The carry input to the ALU selects an input of 0, 1, or the stored carry bit from the status register, QC. Using QC as the carry input allows efficient execution of multiprecision addition and subtraction.

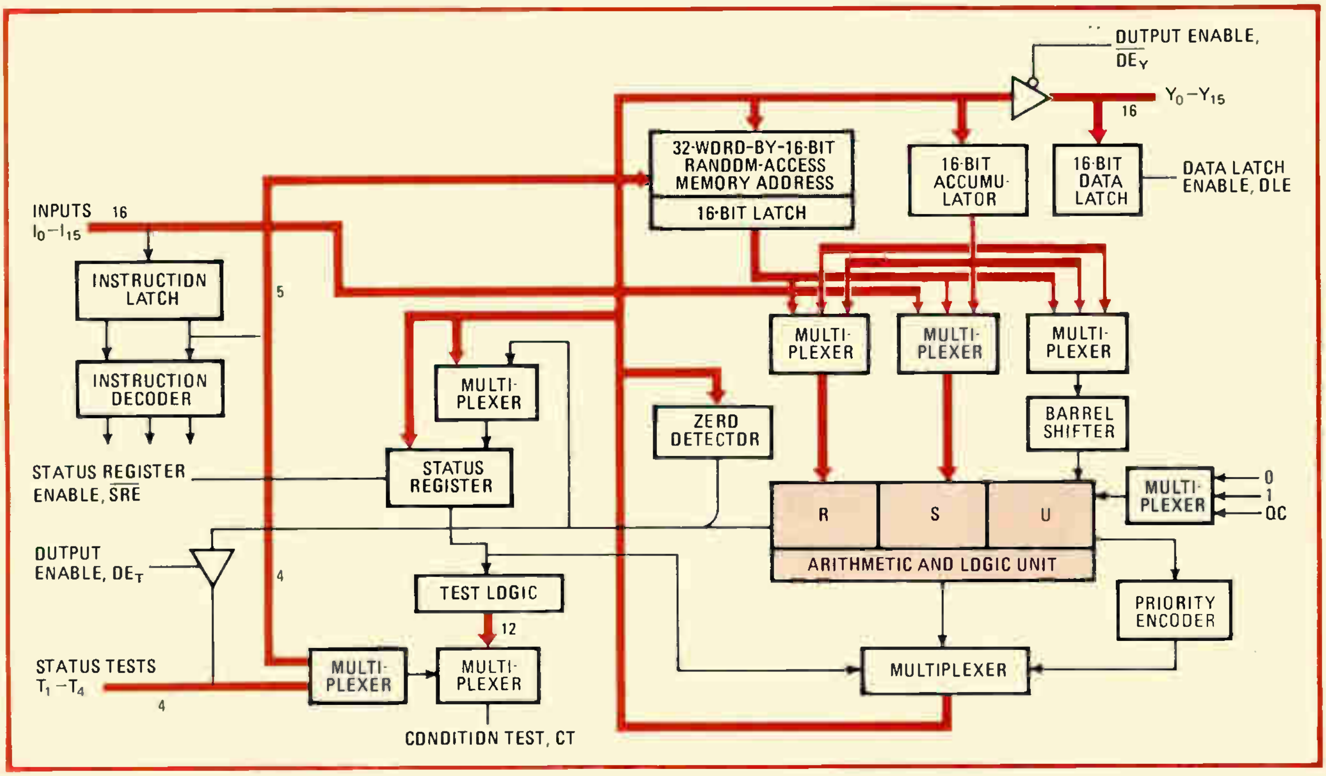
The condition-code generator contains the logic necessary to develop the 12 condition-code test signals. The condition-code multiplexer selects one of these test signals and places it on the CT condition-test output for use by the microprogram sequencer. The multiplexer may be addressed in two different ways. In the first, a test instruction specifies the test condition to be placed on the CT output but does not allow an ALU operation at the same time. The second method uses the bidirectional T-bus as an input, which requires extra microcode but lets the controller simultaneously test and execute.

### Specialized instructions

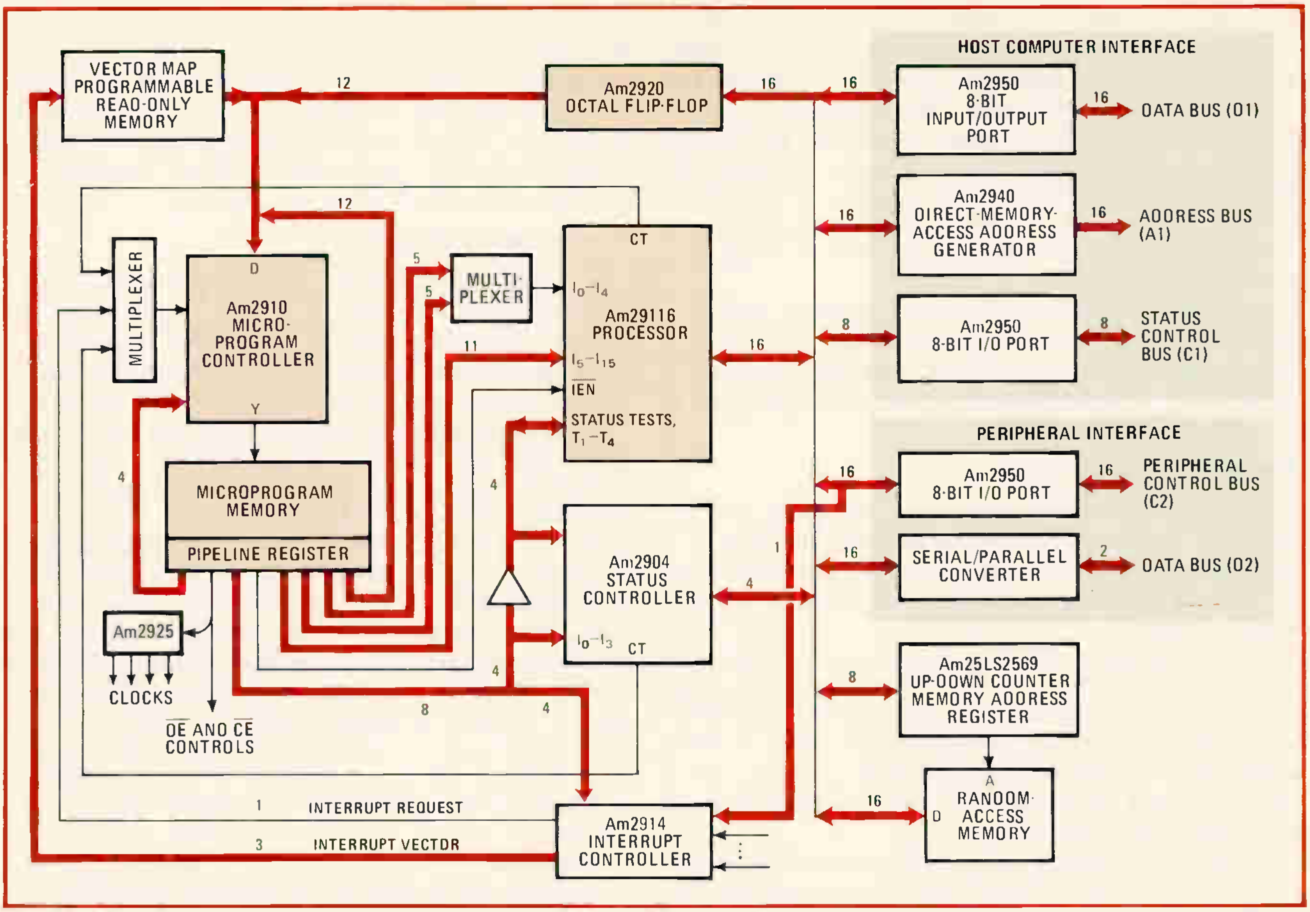
Immediate instructions are executed in two clock cycles. During the first clock cycle, the instruction decoder recognizes that an immediate instruction is being specified and captures the data on the inputs in the instruction latch. In the second clock cycle, the data on the instruction inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the instruction latch is returned to its transparent state.

Since the 29116 is optimized for intelligent controllers, it has extensive bit manipulation instructions operating in either the byte or the word mode. These instructions allow operations such as setting, resetting, and testing of any particular bit without affecting the rest of the bits. Single-bit masks can also be created, such as a single 1 in a field of 0s or a single 0 in a field of 1s in a single microcycle. In addition, the instructions can generate memory addresses in powers of 2 by incrementing or decrementing a number by $2^n$, where n can vary from 0 to 15.

The rotate-by-n instruction uses the barrel shifter with n specifying the number of bit positions the source is to be rotated. In the word mode, a specified number of bits are wrapped around over the 16-bit boundary; in the




**1. Novel architecture.** The arithmetic-and-logic unit on the 29116 16-bit bipolar microprocessor has three inputs so that a masking operation can be performed simultaneously with another instruction. The barrel shifter and priority encoder further optimize it for control.




**2. Maximum system.** If the highest speeds are required, then the 29116 can be assisted by support chips from the 2900 family. However, a minimum system configuration can be realized by using only the shaded components, though system throughput will be slightly degraded.

byte mode, the bits are rotated around the 8-bit boundary of the least significant byte.

The rotate-and-merge instruction can merge two operands on a bit-by-bit basis, under the control of the mask as a third operand. Thus, in one microcycle, translation from one code to another, such as from ASCII to hexadecimal, can be done with this instruction. This sort of operation would require at least three instructions with a conventional ALU.

The rotate-and-compare instruction compares a rotated operand with a nonrotated operand. A 1 at the mask input (third operand) eliminates that bit from the

## What is microprogramming?

Most instructions execute a fixed sequence of steps to perform their function. This control sequence may be realized as a hardwired random-logic state machine that provides the necessary outputs for controlling the different functions. The disadvantage of this approach is that it leads to a design that is irregular and inflexible.

An alternative is the microprogrammed approach, where the control information is obtained from a regular structure, such as a programmable array or a read-only memory. A sequence of controls is obtained by accessing different words in the array. This access is usually obtained by cycling through consecutive words in the array until the instruction is completed. The action is performed by a sequencer that selects the microsubroutines that execute instructions.

Thus, a microprogrammed control mechanism consists of a memory and a sequencer. The memory can be a ROM, programmable ROM or random-access memory, and the information residing in it is referred to as the microcode. The sequencer controls the order of execution of the microcode words. In a microprogrammed system, the output of that microcode memory, however it is stored, directly controls the machine's hardware. This memory in essence replaces the random-logic control mechanism of a machine.

The modularity of this scheme results in a design that is easy to upgrade or modify, since programming a PROM takes much less time than redesigning a random-logic state machine. In the same way that assemblers simplify machine language programming, programs called meta-assemblers can aid in the writing of microcode. A development system called System 29 aids the design of microprogrammed systems. It also contains a meta-assembler called Amdasm for assembling the firmware portion of a system. Using Amdasm, it is possible to write microcode using user-definable mnemonics and the other facilities provided by System 29 help in the development and debugging of this firmware.

comparison. The result of the comparison is loaded in the 0 bit of the status register. If the comparison passes, the 0 bit is set.

The 29116 can also prioritize a masked operand, which is ideal for performing n-way jumps as well as for normalizing numbers. The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest-priority active bit. If none of the bits is active, the output is 0. Such an operation requires a separate subroutine when carried out on conventional microprocessors.

## Forward and reverse

For reliable data transmission, the cyclic-redundancy-check instructions permit generation and comparison of the CRC check bits using any 16-bit polynomial. Since the CRC code standard does not indicate which data bit must be transmitted first, the 29116 supplies both forward and reverse CRC instructions, each of which consumes only two microcycles per bit—perfect for bidirectional tape drives.

In the first cycle, the data bit is shifted from one of the registers into the link bit of the status register. During the second cycle, check bits are generated by executing either the CRC forward or reverse instructions. The result is stored back into the check-sum register.

The part also includes such niceties as exclusive-NOR sign extention for converting 8-bit integers into 16-bit ones and a single-bit shift directly on a register.

A typical system configuration for the 29116 consists of a host computer, memory, and peripheral controller interfaced through three buses. The peripheral controller and the peripheral devices are interfaced with a separate data bus, which may be either serial or parallel, and a control bus. Information on the control buses comprises status, command, and timing signals.

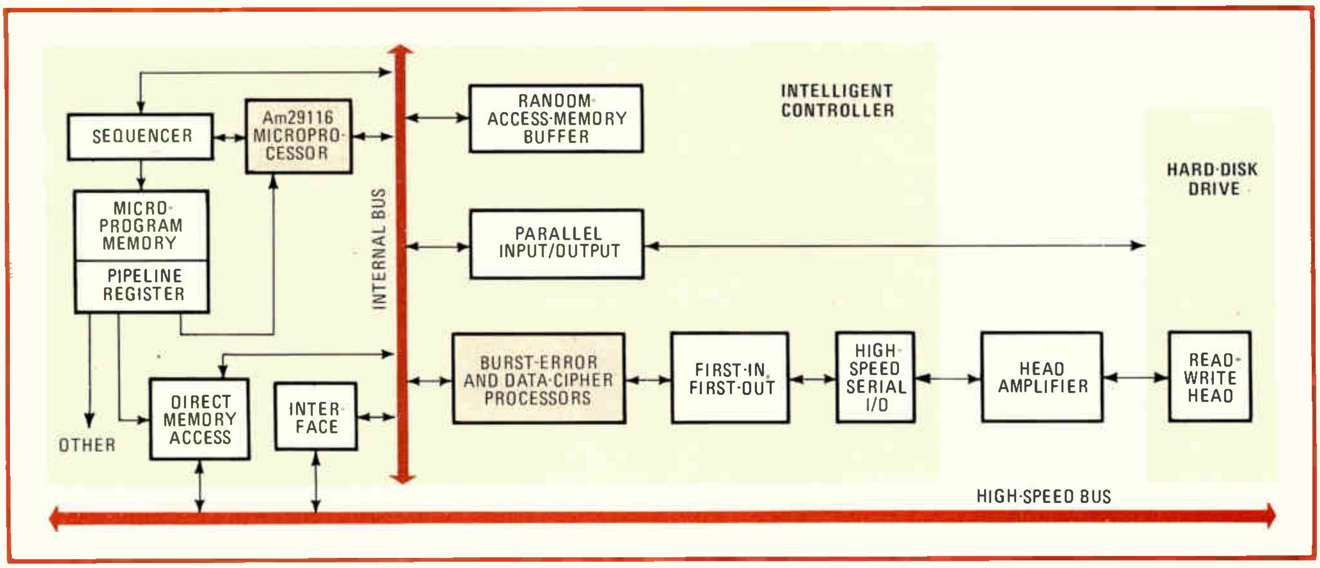
In a typical implementation of the peripheral controller portion of a system, the bidirectional interface to the host's data bus is via two Am2950 8-bit parallel I/O ports. Two Am2940 8-bit direct-memory-access address generators drive the associated address bus, and another 2950 interfaces with the bidirectional control bus. The interface to the serial peripheral data bus in this case is serial. The interface between these bus-interface units and the 29116 is a 16-bit bidirectional bus that connects to its Y port. A 256-word random-access memory for temporary data storage and a 12-bit interface to the microprogram controller connect to the D inputs of the AM2910 microprogram sequencer. The bus-control and clock-enable signals for these devices are generated by the pipeline register at the output of the microprogram memory.

The 29116, 2910, and the microprogram memory perform the data manipulation and routing; command and status generation and testing; and the timing-signal generation functions. This implementation minimizes the amount of hardware necessary to implement a controller, which is accomplished by sharing the instruction-inputs to the 29116 with the inputs to the 2910; by generating all the necessary test conditions within the 29116, which permits connecting the CT output of the 29116 directly to the condition code ($\overline{CC}$) inputs of the 2910; by performing all the necessary status manipulations within the 29116; and by using the same RAM address for reading and writing.

## A tradeoff

Although the peripheral-controller implementation described above minimizes the amount of required hardware, it does limit the throughput. The architecture shown in Fig. 2 uses the same bus interface circuits but maximizes the throughput of the controller at the expense of additional hardware. In this implementation, the instruction inputs of the 29116 and the D inputs of the 2910 are driven from separate microcode bits, making possible simultaneous instruction execution in the 29116 and direct jumping in the 2910.

The multiplexer at the $\overline{CC}$ input of the 2910 allows conditions to be tested without loading the signals into the 29116. Four additional bits of microcode drive the T




**3. Typical application.** The 29116 is ideal for controlling Winchester disk drives. It can handle up to eight such drives simultaneously and, with the addition of a burst-error processor and data-ciphering processor, it can be made very reliable as well.

## Imox: A union of TTL and ECL

The Imox process is an advanced oxide-isolated structure developed by Advanced Micro Devices to address the reproducibility requirements of die sizes in excess of 50,000 square mils. It employs fully ion-implanted transistors, walled emitters, and two layers of metal interconnections. Assuming the same feature sizes, Imox can produce devices with less than half the base area and two thirds the collector substrate area of a diffused-isolation washed-emitter low-power Schottky transistor. Smaller sizes and inert isolation regions significantly reduce device capacitances and increase potential speed.

The approach selected was to combine an oxide-isolated device structure with emitter-coupled-logic internal and TTL input/output circuitry. The technique enabled engineers at AMD to pack the equivalent of over 2,500 TTL gates into 78,000 square mils of silicon, using 3-micrometer minimum features and an 8-$\mu$m metal pitch.

As with all large-scale integrated processes, Imox is a marriage of circuit and process approaches. The reason that the internal circuitry of the 29116 is implemented in ECL, while the inputs and outputs are all standard TTL levels with translators to the ECL interior, is because ECL possesses the ability to create dense structures with an excellent speed-power product through series gating.

The barrel shifter in the 29116 is an excellent example of how ECL can be applied to a complex LSI device. This function performs a selectable n-bit shift or rotate. It is the equivalent of 276 gates and is implemented with 526 components, consumes 92 milliwatts, and exhibits delays of less than 7 nanoseconds.

inputs of the 29116, permitting simultaneous conditional testing and execution of an instruction in the controller. In addition, the ALU status bits can be selectively loaded into the 2904 to reduce the number of cycles necessary to perform status manipulation.

By adding five additional microcode bits and a multiplexer at the I inputs of the part, separate source and destination addresses can be used in the same microcycle. For example, the contents of the third register can be added to the contents of the accumulator and the results can be stored in register 7.

In addition to supplying the basic oscillator and clock driver functions, the 2925 system-clock generator and driver lets the user dynamically alter the length of the microcycle and, thus, interface the 29116 with slower bus-interface and peripheral circuits. The 2914 handles high-speed interrupts from the peripheral controllers.

The 29116 functions as a superior disk controller because its bipolar technology enables it to perform at much higher speeds than MOS processors and, therefore, handle as many as eight Winchester disk drives simultaneously (Fig. 3). Its microprogrammability lets it be tailored to the requirements of a specific application. Efficient data movement and data compression is possible using instructions, such as rotate-and-merge.

### Major application areas

The unit's bit manipulation instructions are useful for checking control and status bits. A microprogrammed system allows the controller to initiate a task such as positioning the disk head while performing other tasks until notified that the head is in position.

Fast response to interrupts as well as other speed enhancements can be designed in, using other 2900 bit-slice–family components. The CRC instructions can be used for the checking and generating the file header CRC bits; the CRC reverse instruction is included for systems (such as with magnetic tape) in which reading data in a forward and in a reverse direction is desirable to avoid time-wasting back-space and reread operations.

Graphics processors vary in complexity based on the performance required from them, but sophisticated image processors require very high-speed controllers. The 29116 is well-suited for systems that include character and vector display or partition the screen into various regions that may need independent scrolling, cursor control, zoom and pan, scaling, and translation and transfer of data between various sections of the memory.

If the part is used for address generation, the arithmetic instructions using $2^n$ are useful. For example, in a windowing operation, there are certain bits in every horizontal scan that must be selected. The next line is displaced in the memory by a fixed address equal to the number of pixels in the horizontal line.

Thus, address generation is simplified considerably. In addition, vectors can be generated from the coordinates of two points to be connected can be done easily using algorithms that generate the intermediate points and require only additions and subtractions for interpolation.

### Saving cycles

The rotate, rotate-and-merge, and other specialized instructions of the 29116 let the user perform the functions in one cycle that would take several cycles on conventional processors. For example, when a copying operation is performed on the display, a section of the area that was previously aligned with the 16-bit word boundary of the controller may no longer be aligned. The realigning may require rotation with a mask to leave the area outside the window unchanged.

Another excellent application for the 29116 is as a cluster controller that manages a group of devices requiring service on a statistical basis. These devices could be terminals or printers or specialized I/O ports. The controller can dynamically alter device priorities to assure a fast response to the active devices at the expense of the inactive ones.

The kinds of functions that a cluster controller may have to perform are data transfers between the devices themselves or between a memory and the devices, checking of device status, diagnostics, and assigning of service priorities. The priorities can be of different kinds and may be dynamically alterable. For example, when all devices are of equal priority, then a round-robin scheme can be used so that the device just serviced gets the last priority for the next service. □

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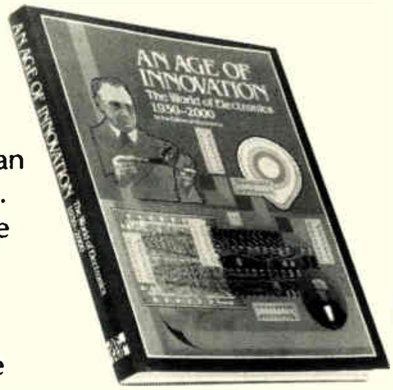


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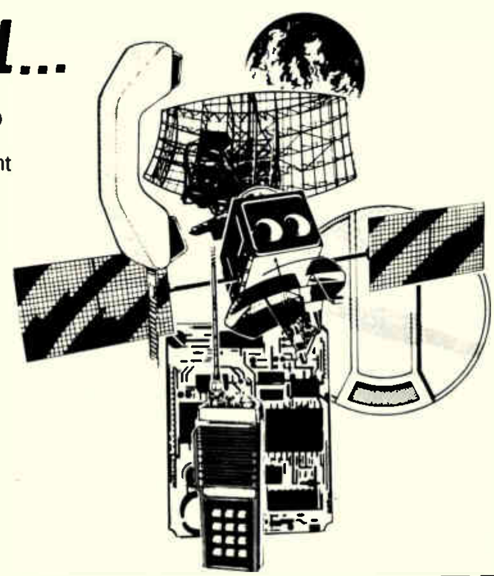

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IEDM SPECIAL REPORT

# Devices meeting heralds new processes and materials to enhance future systems

by John G. Posa, *Solid State Editor*

Creative new techniques continue to better the performance ratings and integration levels of digital MOS and bipolar chips, though the former is getting the lion's share of attention in Washington, D.C., Dec 7–9, at the International Electron Devices Meeting [*Electronics*, Sept. 22, p. 97].

Sapphire is still being pushed as a starting material, but silicon dioxide for device isolation and as an insulating substrate is seen as more cost-effective. A deeper understanding of how alpha radiation affects ICs has brought about a wave of unique solutions to the problem. New device models, some of which track transistor action in three dimensions, now allow engineers to predict the behavior of submicrometer devices.

Polysilicon is being augmented with metal and metal silicides to truncate signal delays, and all these improvements are bringing very large-scale integrated circuits like the 256-K random-access memory that much closer to production.

Complementary-MOS technology, nearly neck and neck with n-channel processes for VLSI, is benefiting further from knowledge gained about scaled-down p-channel devices. For a new level of compaction, some arrangements have C-MOS's p-channel device stacked on top of the n-MOS transistor, or vice versa.

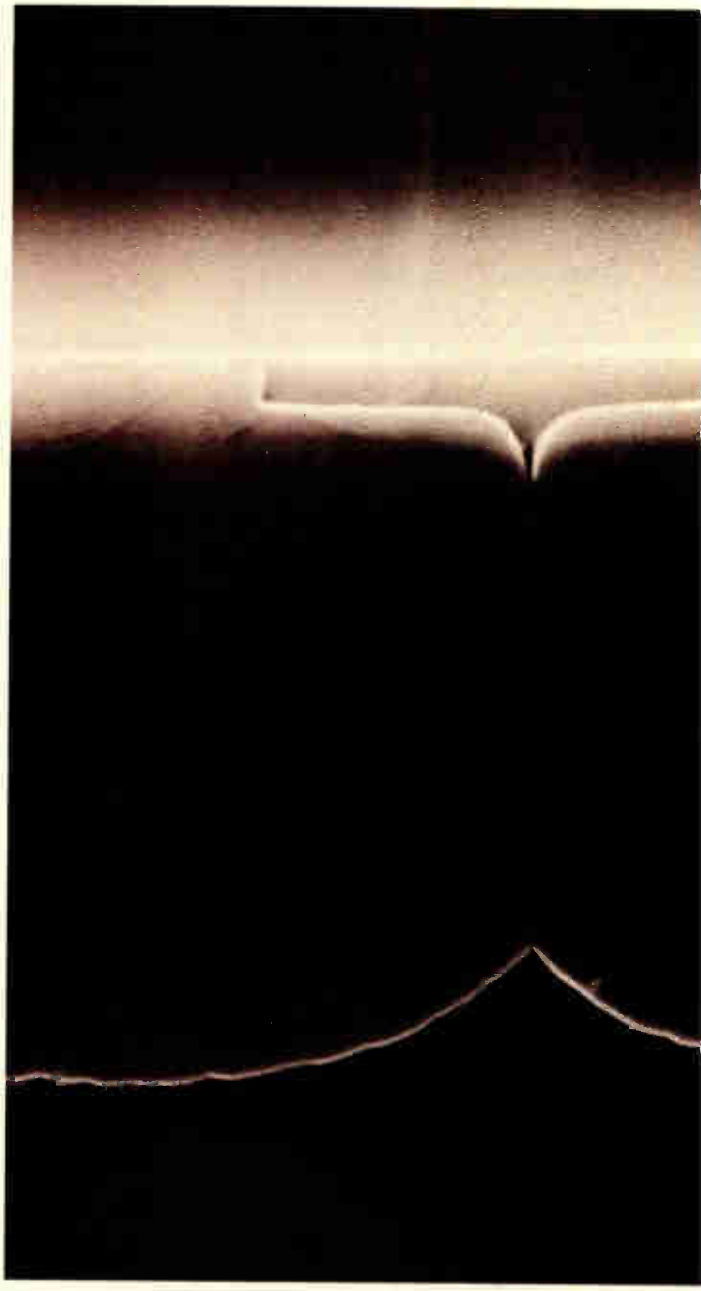
Methods abound on how to optimize the storage and retention capabilities of electrically erasable programmable read-only memories. At least two of the techniques promise the multiplicity in density afforded by requiring only one transistor per bit of EE-PROM.

### Substrate improvements

Mechanisms to enhance the action of MOS transistors are being attempted above and below the substrate. Below the substrate, efforts center on ways to isolate devices from one another and to shelter them from noise.

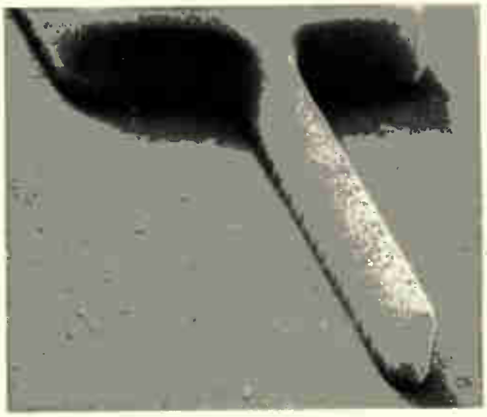
At Nippon Telegraph & Telephone Public Corp.'s Musashino (Japan) Laboratory, a process called full isolation by porous oxidized silicon, or Fipos, is being used to separate active devices with a thick dielectric *Electronics*, Jan. 27, 1981, p. 77]. The lab is applying the technique to C-MOS circuits and has so far built a 1,300-gate logic array that is 20% faster than a bulk C-MOS version would be.

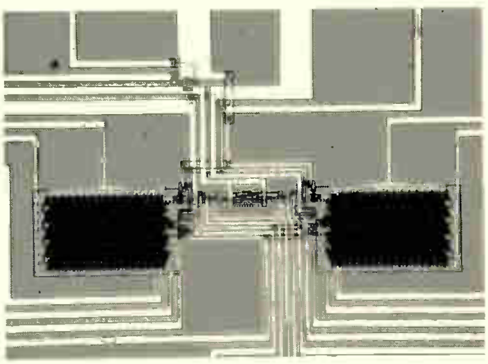
To help neutralize carriers generated by alpha particles, International Business Machines Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y., buries a perforated n-type grid about 2 $\mu$m below the surface of a p-type substrate (Fig. 1). The grid and an intervening p-type implant to subdue punch-through

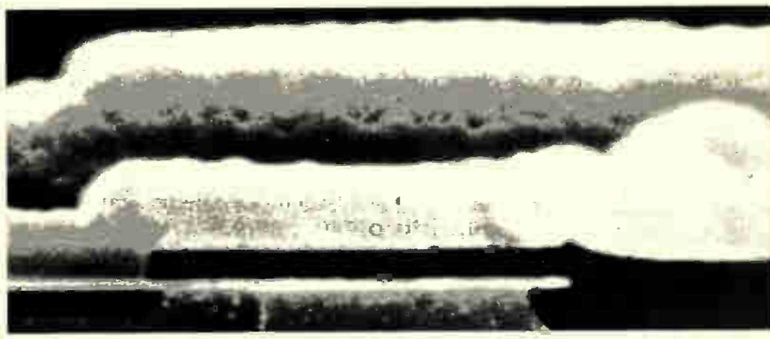


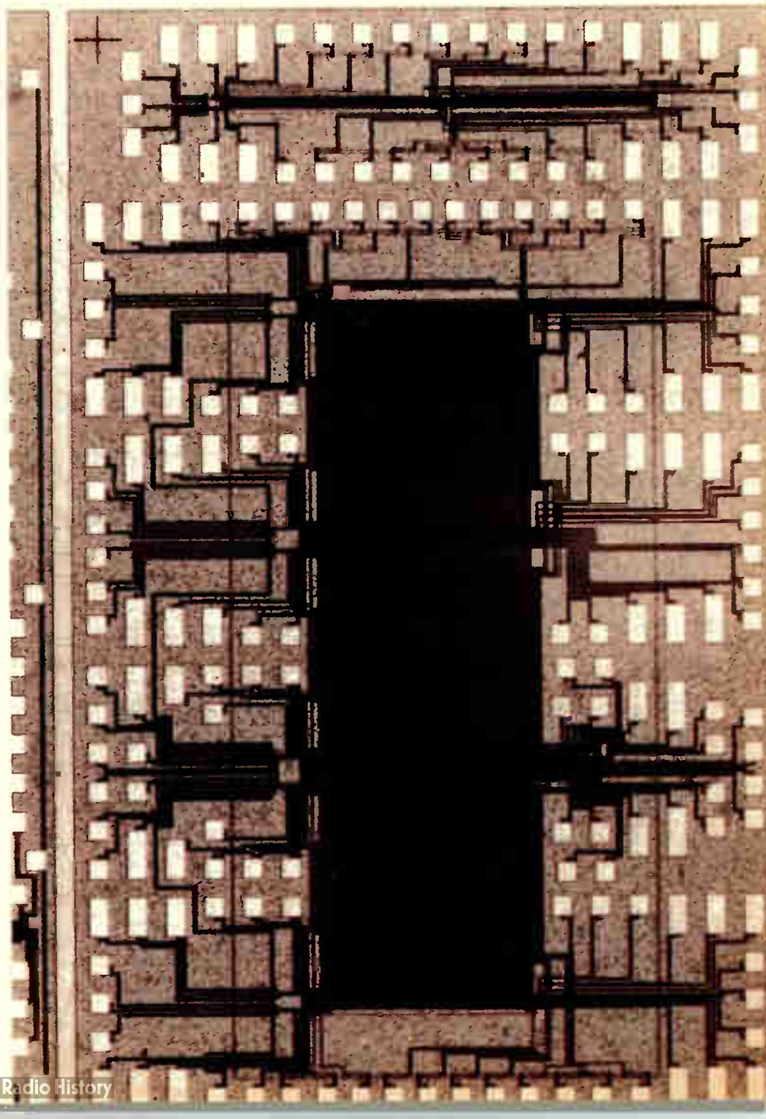
**For MOS.** An island of single-crystal silicon is isolated (above) using NTT's Fipos process. In the middle set of photographs, the thin finger is a titanium disilicide gate etched by Texas Instruments; below that are two 256-bit memory arrays used by Fujitsu to test nitride storage capacitors, and the MOS cross section at bottom was passivated

*Isolation schemes and silicides are helping perfect MOS integrated circuits; solid-state imagers will be followed by flat displays that will be fed by high-power chips; GaAs parts and fiber optics raise bandwidth of communications*









with a very low-temperature process from Hughes. At far right, the top photograph shows a molybdenum gate in a 4-K static memory from NEC and NTT, and the larger photo below contains a new Toshiba sense amplifier that compensates for the threshold voltage of array transistors in MOS dynamic RAMs.

IEDM

may be built with one mask and two implants. The combination blocks up to 85% of the charge that would be collected by a very large electrode, and when the grid is implanted so as to line up with a memory array, soft error rates can be reduced by a factor of five.

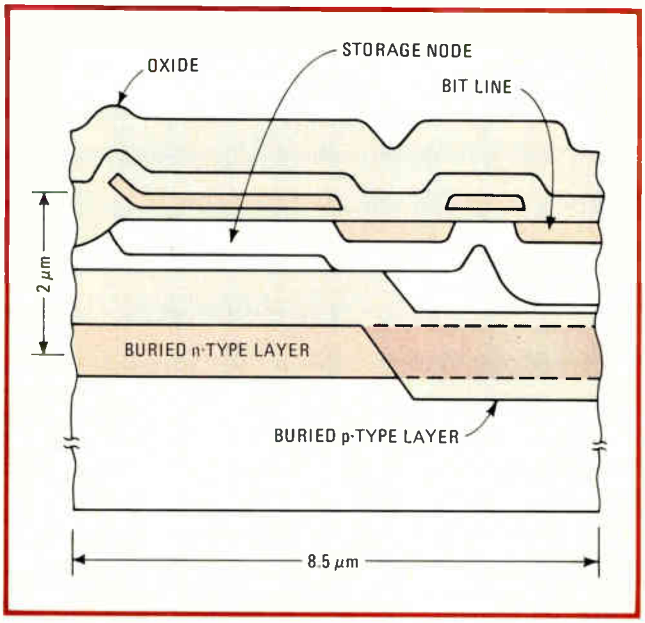
To improve the storage characteristics of MOS dynamic RAMs in particular, Toshiba Corp.'s Semiconductor Device Engineering Laboratory in Kawasaki, Japan, has designed and tested a sense amplifier that compensates for the threshold voltage of cell-selection transistors. Fujitsu Ltd.'s laboratories, also in Kawasaki, are replacing the oxide dielectric present in today's storage capacitors with plasma-deposited silicon nitride. The dielectric constant of $Si_3N_4$ is 30% higher than that of silicon dioxide, and it can be shaved down to 70 angstroms yet still block ions and impurities.

Toshiba and Fujitsu both say their ideas are inspired by the goals of 256-K and 1-megabit dynamic RAMs. Indeed, Toshiba goes on to describe a 256-K RAM based on buried-channel MOS field-effect transistors and molybdenum disilicide gates [*Electronics*, Sept. 22, p. 78]. NTT's Musashino lab has improved the producibility of its 256-K RAM through parallel-plate plasma etching of its molybdenum-on-polysilicon gates [*Electronics*, Feb. 14, 1980, p. 140].

The fact is, numerous efforts are under way to replace doped polysilicon with metal silicides or pure metals to speed signal propagation in VLSI circuits [*Electronics*, Nov. 3, 1981, p. 101]. These higher-conductivity materials bolster the performance of shrinking interconnection paths and contact vias. Elsewhere at NTT's lab, an 18-nanosecond MOS 4-K static RAM with pure molybdenum gates and interconnects has been executed, with $MoSi_2$ used for direct contacts between the metal and diffused $n^+$ regions.

At Intel Corp.'s Livermore, Calif., facility, pure tungsten also is being used for gates and direct contacts. Texas Instruments Inc. prefers titanium disilicide and has etched 1-$\mu$m gates out of the material.

Besides modern dry-etching techniques, the use of metal and silicide gates is made possible by low-temperature passivation techniques such as the 50°-to-300°C Photox process pioneered at Hughes Aircraft Co.'s Technology Support division in Culver City, Calif.




**1. Buried alpha-stopper.** To block the ill effects wrought by alpha particles, IBM Corp. buries an n-type grid and an intervening p-type implant about 2 micrometers below the surface of a p-type substrate. Together, they can reduce soft error rates by 80%.

Now that complementary-MOS technology has established itself as a viable contender for VLSI, research is under way to determine how the n- and p-channel devices in C-MOS circuits will behave as geometries are scaled down. Since fine-line n-channel MOS FETs have already been extensively characterized, interest in submicrometer p-channel MOS FETs is on rise.

## Scaled-down C-MOS

Exploiting capabilities in X-ray lithography and reactive sputter etching, researchers at Bell Laboratories, Murray Hill, N. J., have patterned p-MOS FETs with channels as short as 0.5 $\mu$m. With high gate voltages, behavior of the transistors is dominated by velocity saturation, as it is with extremely small n-MOS FETs. As such, Bell found the drain currents of submicrometer n- and p-channel devices are comparable, given equal geometries, oxide thicknesses, and threshold voltages.

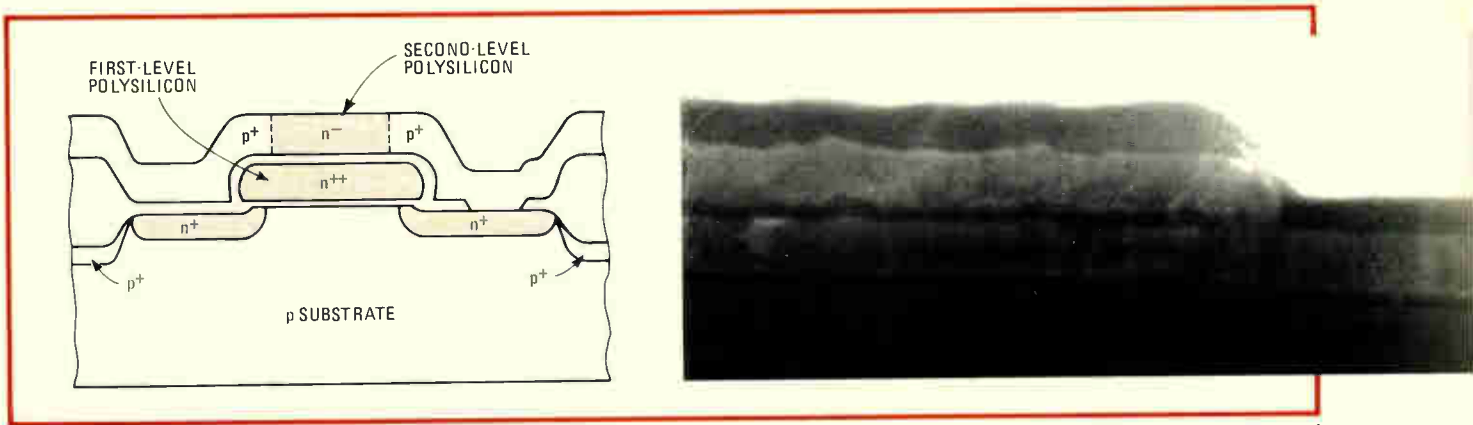
By shrinking effective channel lengths on its n-MOS FETs to 0.25 $\mu$m, Bell has already demonstrated remarkable stage delays in unloaded devices [*Electronics*, Dec. 18, 1980, p. 40]. P-channel FETs of a similarly high caliber open the door at Bell to C-MOS circuits with picosecond delays at microwatt power levels.

Texas Instruments, now getting into C-MOS in a big way, is also investigating scaled-down n- and p-MOS FETs and, in particular, the effects of reduced C-MOS source and drain regions. Modeling transistors with channels as short as 0.2 $\mu$m, scientists at TI's Central Research Laboratories in Dallas have found that the gain of n- and p-MOS devices peaks at channel lengths of about 0.4 and 1.4 $\mu$m, respectively, primarily because of contact resistance. The problem is much more pronounced in the p-channel FETs because of the higher sheet resistivity of the boron junctions.

Because the p-type boron diffuses more quickly in silicon than does n-type arsenic, TI suggests that the boron source-drain implant dose be reduced from that predicted by conventional scaling theory. This reduction results in a beneficial side effect: the previously-implanted $n^+$ source-drain regions can be boron-counter-doped without a shift in threshold voltage. In other words, the entire chip can be blanketed with boron, thus saving one masking step.

Interestingly, cross-sectional diagrams in one of TI's papers show a twin-tub C-MOS process—built in an epitaxial layer—much like the one Bell Labs is using for its 32-bit microprocessor and other applications [*Electronics*, Oct. 6, 1981, p. 106].

Two research concerns, the Lincoln Laboratory of the Massachusetts Institute of Technology in Lexington and the Centre National d'Etudes des Télécommunications of Meylan, France, have come up with vertically stacked




**2. Stacked C-MOS.** Both the Centre National d'Etudes des Télécommunications and the Lincoln Laboratory of the Massachusetts Institute of Technology have come up with structures that stack the n- and p-channel devices of C-MOS circuits atop one another. CNET's version is shown, but both laser-anneal the upper of two polysilicon layers, allowing the gate to control channels above and below.

C-MOS inverters with an uncanny similarity. Both commence with a standard double-polysilicon MOS structure but laser-anneal and dope the upper layer so that it can act as a channel. With this arrangement, first-level–polysilicon gates can control current above and below them, as CNET's construction in Fig. 2 illustrates.

MIT's stacked C-MOS gates are nearly identical in principle, except that all doping polarities are reversed (it begins with an n- rather than a p-type substrate). Using 4-$\mu$m channels, MIT's inverter measures 320 $\mu m^2$.

New applications of C-MOS technology include the fabrication of a 4-K-by-4-bit clocked RAM on a sapphire substrate at Hughes Aircraft Co.'s Newport Beach, Calif., Research Center. The chip's typical access time is 150 ns (or 110 ns with tantalum silicide gates); power dissipation is 20 milliwatts at 3 megahertz and a mere 35 microwatts on standby.

To arrive at such performance specifications, Hughes used planar plasma etching for highly vertical gate-electrode walls, thus eliminating edge leakage and low gate-oxide breakdown. Preliminary testing demonstrated that the memory can withstand a radiation dose of $10^5$ rads (silicon).

### Improving EE-PROMs

Efforts to reduce the size and operating voltage of electrically erasable programmable read-only memories are paying off. Unlike other floating-gate EE-PROM transistors that employ a separate tunnel oxide for cell programming and erasure, a compact cell developed at Motorola Inc.'s MOS IC division in Austin, Texas, uses the entire channel as the tunneling area.

With 3-$\mu$m feature sizes, Motorola's memory cells measure 261 $\mu m^2$ and the 32-K chip in which they are used, only 33,400 square mils. For comparison, cells in Intel Corp.'s 27,225-$mil^2$ 16-K EE-PROM measure 548 $\mu m^2$. Motorola's EE-PROM process is compatible with conventional double-polysilicon technology with the addition of one mask. Thus, the company's microcomputer line could easily be fitted with nonvolatile electrically erasable storage.

Whereas Motorola's EE-PROM features byte erasure, a triple-level polysilicon cell from Toshiba Corp.'s Semiconductor division in Kawasaki offers this plus erasure on a bit-for-bit basis. Charge on the second-level floating gate is monitored with the application of a sensing voltage to the first-level erase gate to prevent overerasure into depletion. Toshiba has built a 64-K EE-PROM with 150-$\mu m^2$ cells that measure 41,500 $mil^2$.

Like Toshiba's memory, an EE-PROM under development at Fujitsu Ltd.'s IC division in Kawasaki gets by with a single transistor per bit. Programming in Fujitsu's cell is accomplished by means of avalanche injection from the channel, as with E-PROM cells. Erasure, however, is carried out through avalanche injection from a $p^+n$ junction embedded in the floating gate. A big advantage of the assembly, says Fujitsu, is the lack of a thin tunnel oxide, which can degrade retention.

### Bipolar's prospects

Members of Hitachi Ltd.'s Device Development Center in Tokyo feel that silicon bipolar transistors are not only competitive with gallium arsenide metal-semiconductor FETs in terms of speed, but they are more reliable and can be integrated more densely and at lower cost. Their studies indicate that 500-Å transistor base widths are possible; and if these are coupled with 0.5-$\mu$m emitters, 75-picosecond emitter-coupled-logic gates would result. GaAs MES FETs, they say, have achieved propagation delays of 62 ps using 1-$\mu$m line widths.

Work is underway at Fairchild Camera & Instrument Corp.'s Advanced Research and Development Laboratory in Palo Alto, Calif., to ascertain the effects of geometry reductions on the Schottky diodes used in bipolar technology. Their results suggest that the voltage-barrier height must be trimmed along with physical dimensions to the point where today's platinum and palladium silicide diodes will no longer deliver optimum performance. Solutions include the use of other transition metals and new structures, on both of which Fairchild is collecting data.

Workers from the NTT's Musashino Laboratory and its Ibaraki Laboratory are using Van de Graaff accelerators to implant bipolar devices. The high energy of the implants allows channel-stop and buried-layer ions to be shot right through thick-field and thin-gate oxides, respectively. The upshot is a much simpler process flow that includes no epitaxy.

# Sensors sharpen their images; logic chips reach high voltages

by Roderic Beresford
*Components Editor*

The next generation of image sensors will be seeing less noise and more color, and doing it faster. Array architecture and isolation techniques open the doors to capture of fast transients and higher sensitivity. The pictures captured will go to flatter displays, like those based on plasma panels or thin-film transistor arrays.

To interface directly with peripheral devices like displays and electrostatic printers, logic chips are integrating high-voltage MOS devices with uncompromised performance. Several new processes are demonstrating the relative merits of field-plate structures, drift regions, and buried layers in controlling strong surface electric fields.

Discrete MOS power devices, meanwhile, reach for ever higher current and voltage capabilities with advanced processes. Also, thyristor experts look for more control over switching dynamics. Thus this year's International Electron Devices Meeting will feature wide-ranging advances in components.

Small, lightweight video cameras using silicon imaging arrays are already a commercial reality; researchers are refining fabrication techniques and designs in order to home in on better-yielding processes, sharper images, color, and high-speed capabilities.

Hitachi Ltd.'s Central Research Laboratory in Kokubunji, Japan has demonstrated the first use of an amorphous silicon film for the photoconductive layer in a color imager. The silicon marks an improvement over its previous imager, which used a chalcogenide glass photoconductor: it leaves the scanning array free of defects and stands up better to the heat during subsequent formation of the color filters on top of the chip.

A top electrode of indium tin oxide forms a Schottky barrier on the amorphous silicon, limiting the dark-current density to a very low 30 picoamperes per square centimeter. With a sensitivity of 40 nanoamperes per lux and a saturation level of 130 lux, the array therefore has a wide dynamic range of more than 60 decibels.

Maintaining even a 50-dB range in a high-speed imager took Eastman Kodak Co. up to some fundamental limits of present array technology. The Research Laboratories in Rochester, N. Y. has designed a monochrome imager for recording transient phenomena at 2,000 frames per second. Conventional serial readout of the 192-by-248 array of photocapacitors would have required a 100-megahertz data rate—far beyond the capabilities of present sensor elements. So the rows of the array are instead addressed in blocks of 32. By addressing one block continuously, a partial frame can stop the action at about 80-microsecond intervals.

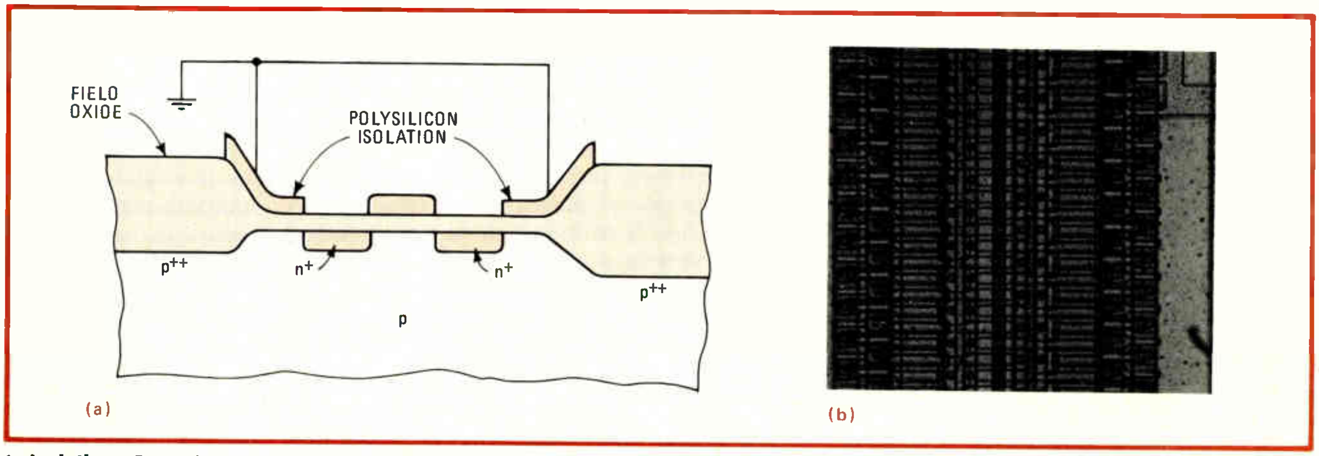
To reduce dark-current noise, Xerox Corp.'s Microelectronics Center, El Segundo, Calif., has separated the active sensor regions from the field-oxide isolation and implants with grounded polysilicon gates. By thus reducing the leakage current that bleeds into the storage area from the stacking faults in the channel-stop regions and from the dislocations in the bird's beak, dark current is reduced almost 3:1, to an average of 0.3 nA/cm².

Figure 1 shows the polysilicon isolation technique and a portion of the linear photodiode array. The technique could help out any other analog circuits that are plagued by dark-current noise.

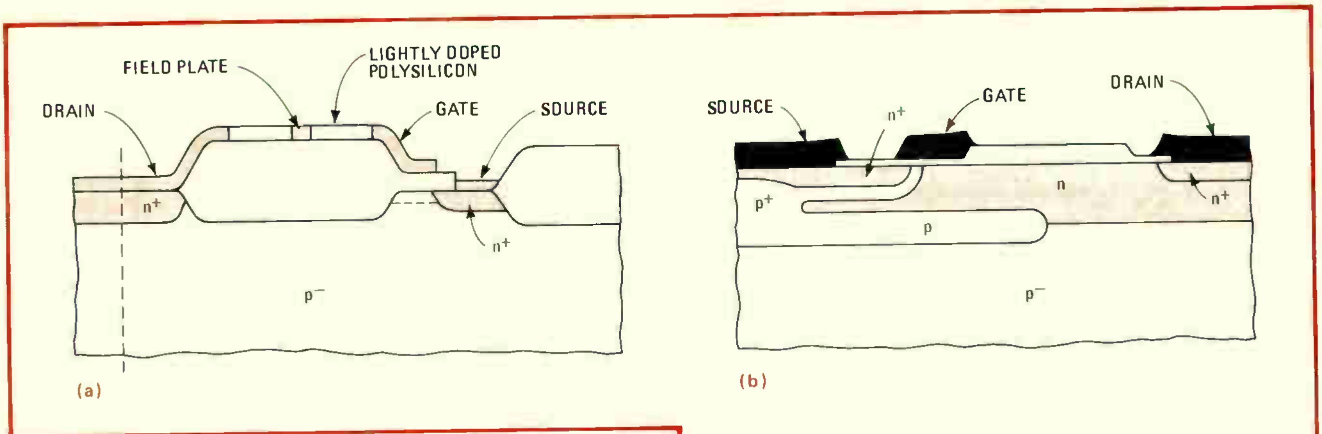
## Thin films for displays

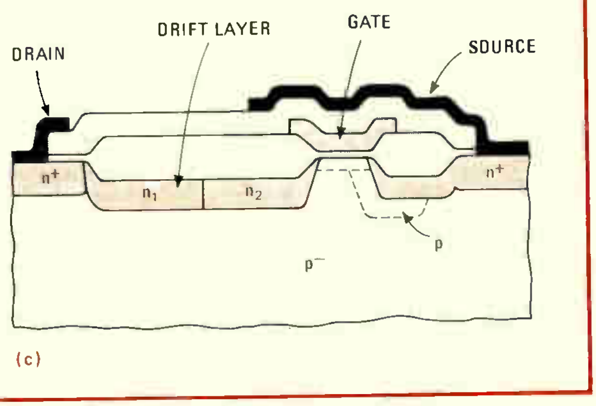
On the display side of electronic image manipulation, solid-state units have yet to see successful commercialization, although attempts abound worldwide. The proposed systems with the greatest potential are based on thin-film–transistor arrays; the difficulty of controlling the properties of compound semiconductors like cadmium selenide has led to the use of polysilicon material in these devices.

Now Hitachi Ltd.'s Mobara, Japan, Works has demonstrated polysilicon thin-film transistors suitable for display driving that are fabricated in a low-temperature, high-vacuum deposition process. Staying below about 550°C enables expensive quartz or sapphire substrates to be replaced with ordinary glass. To do this, the gate insulator must be formed in a low-temperature process also—sputtered aluminum oxide following an oxygen




**1. Isolation.** Grounded gates between field-oxide isolation and active regions (a) keeps leakage currents from interfering with device operation. Xerox applies this polysilicon isolation technique to the linear imaging array in (b) for a threefold reduction in dark current.




**2. The choice is yours.** Three proposed techniques for integrating high-voltage MOS devices on logic chips come from Xerox (a), Philips (b), and Tektronix (c). Extended field plates or extra implants are used to control the electric field at the chip's surface.

plasma treatment gives more stable and reproducible device characteristics than sputtered silicon dioxide. The source and drain contacts are formed by depositing aluminum on substrates held at 150°C.

When viable thin-film processes finally do turn out integrated display drivers on glass substrates, liquid crystals will likely be eligible partners for the long-awaited marriage that will produce solid-state flat-panel displays. In the meantime, however, to judge by the substantial achievements at Burroughs and IBM, plasma panel technology will be capable of information densities approaching those of the cathode-ray tube.

Burroughs OEM Corp. in Plainfield, N. J., cuts the drive electronics required for conventional ac plasma displays by an order of magnitude in a panel that merges ac and dc operation in each cell [*Electronics*, April 21, 1981, p. 39]. International Business Machines Corp.'s System Communications division in Kingston, N. Y., has come up with a 960-by-768-line panel—big enough for scanning multiple pages of text.

## Integrating high-voltage devices

With the cost of the discrete drive electronics apparently the only remaining obstacle to the widespread use of plasma panel displays, papers from Xerox and North American Philips Corp. are particularly timely. Taken together, they show that integration of high-voltage lateral MOS devices in a standard logic-chip processing sequence is clearly feasible and that some of the competing approaches may even rival discrete vertical MOS FETs in performance.

At the Xerox Microelectronics Center, sixteen 500-V MOS devices that use a refinement of the field-plate structures previously developed were integrated with n-channel MOS addressing logic to produce a 170-square-mil driver chip for plasma displays. In the high-voltage device (Fig. 2a), the field plate is a continuous polysilicon layer extending from a central drain diffusion over the field oxide to the usual gate region. The highly resistive polysilicon connecting the plate to the gate and drain electrodes eliminates the risk of breakdown in the oxide or silicon beneath a field-plate edge. The structure requires only one more implant than do the standard logic devices—and this is simply to form contacts to the polysilicon for the gate, drain, and field-plate electrodes. The process thus has high yield.

The usual drawbacks of a lateral device—higher on-resistance and input capacitance—make it slower and more power-hungry than comparable vertical field-effect transistors. But researchers at Philips Laboratories in Briarcliff Manor, N. Y., overcome these limitations by implanting a p-type region deep in the epitaxial layer (Fig. 2b), thereby reducing the electric field in the channel—a move that requires at most one additional processing step. With a reduced surface field, the epitaxial layer's thickness can be increased or its resistivity decreased without lowering the breakdown voltage. Either way, the on-resistance drops.

A more complicated process that combines a source field plate with an implanted drift layer lets Tektronix Inc., Beaverton, Ore., reach 1 kilovolt on the same chip with logic circuits. In fact, the process has so many variables (Fig. 2c) that the researchers can optimize leakage current, on-resistance and saturation current.

## Reducing leakage

The extra p-type implanted region surrounding the source keeps leakage current low. High drain saturation current and low on-resistance require higher drift-layer doping, but this increases the leakage, so the drift layer is doped in sections at two different levels. After all the tuning, the device has leakage as low as 30 nA, on-resistance down to 300 ohms, and still up to 84 milliamperes saturation current in an area about 0.7 square millimeter. Coming at a time when discrete FETs are just reaching the 1-kV level, these results should bode well for the future of high-voltage integrated circuits.

Without the constraint of compatibility with logic devices, processing expertise can bring still further rounds of improvement in discrete MOS FET current and voltage capabilities. Researchers at General Electric Co.'s Corporate Research and Development Center, Schenectady, N. Y., point out that processing techniques like dry etching and ion implantation have as much to offer to power devices as to logic ICs. They have designed a 90,000-mil² vertical FET—the largest such device reported—for use as a synchronous rectifier in switching power supplies [*Electronics*, Oct. 20, 1981, p. 93].

**Discrete charm of the MOS FET**

Extrapolating the results with 4-micrometer lithography, they find that for low-voltage FETs, the on-resistance can be halved by going down to 1-$\mu$m ground rules. In a thin epitaxial layer, the drain current cannot spread out effectively under the p-type wells that form the channel, so making them narrower gives the current more room. The 60-v device conducts 60 amperes with a resistance of just 14 milliohms.

In its high-voltage work, Siemens AG of Munich, West Germany, has concentrated on design of the chip edges, where premature breakdown in a vertical FET occurs. An extended field plate on the source side and a channel-stopper ring on the drain side are separated by an amorphous silicon layer that stops ions migrating along the surface. In this way, the Sipmos process [*Electronics*, March 13, 1980, p. 92] allows a 36-mm² die to have an on-resistance of 2 Ω and a blocking voltage of 1 kv.

The focus of work on thyristor switches is greater understanding of and control over failure mechanisms—a little finesse goes a long way toward increasing reliability in these bipolar behemoths. The elusive gate-turn-off capability comes under scrutiny at Toshiba Corp., and GE softens the blow of turn-on stresses with a novel multistage design.

GE's Schenectady R&D Center split a light-triggered 5-kv thyristor into three stages, coupling them together with integrated resistors formed in the p-type base region of the npnp structures. In this way, the small area of the semiconductor that can be turned on by a light input of 5 nanojoules or less is not melted by the large system currents. Instead, the main stage is turned on gradually, with the resistive elements dissipating the extra power.

At Toshiba's Research and Development Center, Kawasaki, Japan, infrared recombination radiation is monitored to gather evidence of the failure of the gate-turn-off process. The researchers experimentally related the turn-off failure to a critical anode current density—above about 400 A/cm²—given in terms of the n-type base's thickness and the rate of anode voltage rise. Device and circuit design thus jointly determine a safe operating area for gate-turn-off applications.

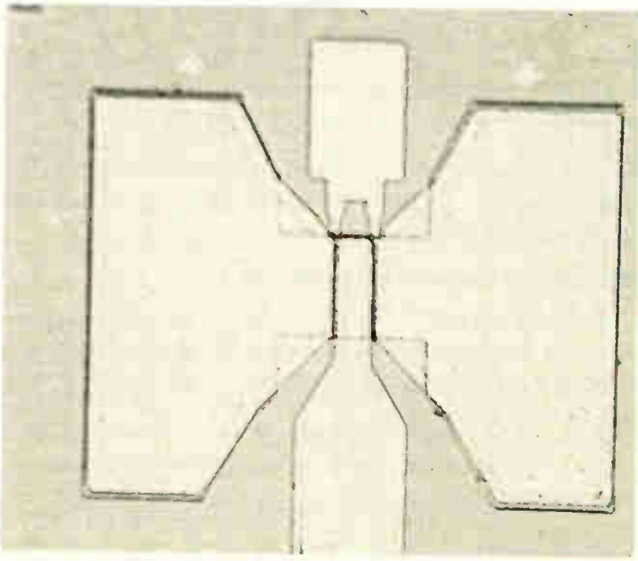
# GaAs FETs drop noise, up gain; optical devices boost power

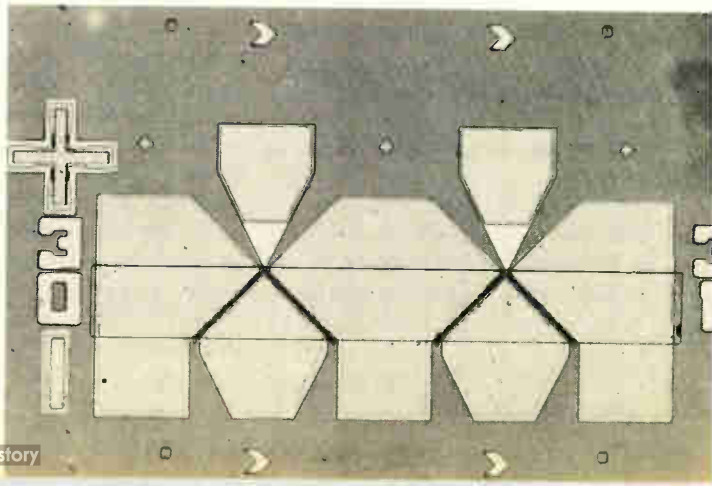
by Harvey J. Hindin
*Communications & Microwave Editor*

There is no doubt that communications systems of the future will operate at higher and higher frequencies. The ever-increasing need for spectrum space will see to that. Design activity centers about the X-band frequencies of 8 to 12 gigahertz, which are coming into active use, and the Q-band frequencies of 26 to 40 GHz, which are still experimental.

Hence many of the landmark papers at this year's International Electron Devices Meeting deal with the technologies that make communications at these and higher optical frequencies possible. Much attention will be focused on gallium arsenide field-effect transistors and fiber-optic components.

In the microwave frequencies, GaAs FETs configured as amplifiers are closing the gaps that exist in low-noise capability, reliability, and gain, compared with their older electron-tube and parametric-diode amplifier cous-





**1. Two choices.** Either the 0.3-$\mu$m-gate-length single-cell design (top) using irregularly shaped source pads for low inductance or the angled-gate geometry (bottom) is employed by Plessey Research to design its 40-GHz gallium arsenide FET amplifiers.

ins. At still higher frequencies, in the optical region of the spectrum (where wavelength is specified instead of frequency), fiber-optic communications systems are appearing at a rapid rate. Like their microwave system counterparts, they need high power sources and sensitive receivers.

### Low-noise GaAs FETS

Low noise and reliability are of particular importance in the amplifiers that work in earth-satellite ground stations. It is no wonder then, that the International Telecommunications Satellite organization (Intelsat) is one of the sponsors of the work performed at Plessey Research Ltd. in Caswell, England.

There, a research team has combined photolithographic and electron-beam technologies to come up with a GaAs FET amplifier with 4 decibels of gain at 40 GHz. The part features a 0.3-micrometer gate length and minimum parasitic inductance and capacitance, and it shows a 3.6-dB noise figure at 26 GHz, even when the losses in its substrate are included. This noise figure is achieved with a gain of 5 dB.

If these figures are not impressive enough, as a bonus, at 77K, the amplifier has a 0.3-dB noise figure at 14 GHz. Such a cooled device could eventually provide competition for those firms making parametric amplifiers—the traditional method of dropping noise figures below 1 dB.

Practically speaking, the Plessey amplifier is not yet developed sufficiently to displace earth-station parametric amplifiers. But the need for low-cost, reliable solid-state devices for future satellite systems ensures its continual development in one form or another.

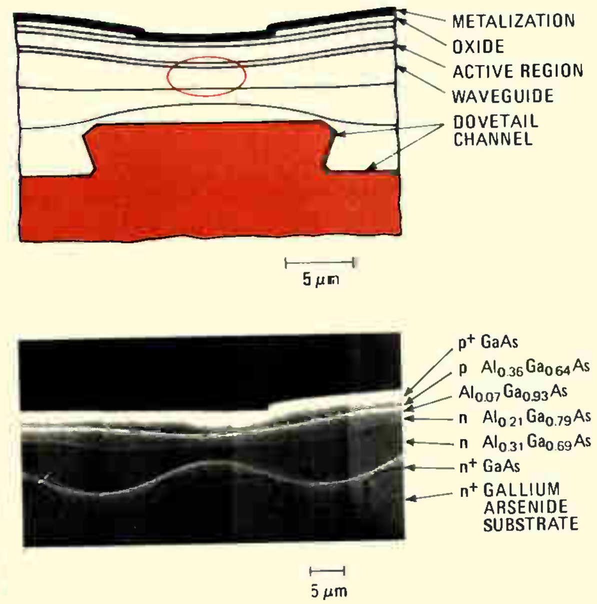
Key to the success of this and other high-frequency GaAs FET amplifiers is the reduction of the transistor's source inductance. Unfortunately, unlike the gate and drain inductance, it cannot be tuned out by the amplifier's input and output matching networks.

Figure 1 (top) is a Plessey approach to this problem. It is an orthogonal single cell with 0.3-μm gate lengths and irregularly shaped source pads ideal for low-inductance bonding of wide tapes when the amplifier is mounted. An alternate Plessey structure, which uses angled gates to minimize feedback capacitance and other parasitics, is also available (Fig. 1, bottom).

To characterize the GaAs FET amplifier, the researchers developed a model that permits *a priori* predictions about the amplifier's behavior. It was constructed after a series of device measurements at 18 GHz using a Hewlett-Packard automatic network analyzer.

With the use of the model, the amplifier's characterization was extended to 40 GHz with reasonable success, meaning that experimental results could be correlated with the 26- and 40-GHz predictions for both the orthogonal and angled geometries. This, in turn, signifies that design parameters such as substrate type and thickness, transistor line sizes, and parasitics could, at least in theory, be optimized.

Future refinements of the amplifier, which has a more-than-adequate predicted mean time before failure of $10^7$ hours at room temperature, will take these results into account. But, at the very least, the feasibility of using GaAs FETs as low-noise Q-band amplifiers has been established.




**2. Complex.** The RCA Laboratories' high-power, single-mode laser diode needs a complex geometry to allow oscillation in a relatively large spot. Discrimination against higher-order modes is provided by incorporating mode-dependent losses in the structure.

While the Plessey amplifiers will eventually make dandy earth-station low-noise amplifiers, the GaAs FETs developed at Microwave Semiconductor Corp. in Somerset, N. J., are designed to accommodate the need for high-reliability, power amplifiers to fly in X-band satellites. Internally matched and hermetically sealed, these FETs compete aggressively with the efficiencies of the medium-power tubes still used in satellites.

### Satellite GaAs FETs

For example, it is possible to obtain a 42% efficiency for 1- and 2-watt power output devices at 8.5 GHz. A 4-W device at the same frequency can achieve 41% efficiency. In power-hungry satellites where fractions of a watt count, such efficiencies are a requirement not met in a FET until now. They were accomplished by paying particular attention to the GaAs FET's construction, material, matching networks, and packaging.

The company spent considerable research effort on GaAs chips that had good power efficiency. Typical of the effects studied by the researchers was ohmic contact resistance. This parameter affects the FET's gain which, in turn, is related to its efficiency. The ohmic contacts were modified until they had less than 50% of the previous resistance values. This modification resulted in a 5% improvement in transistor efficiency that could not otherwise be obtained.

As part of the attention paid to packaging, the grounding, feedthrough terminals, and microwave seals were designed to minimize the coupling of power out of the amplifier's signal path. Finally, since the input and output matching networks were incorporated into the amplifier, power losses due to reflections at the amplifier's terminals were kept to a minimum. Even though the matching networks contributed some 0.3 dB of loss themselves, more efficiency was gained than lost.

## Better fiber optics

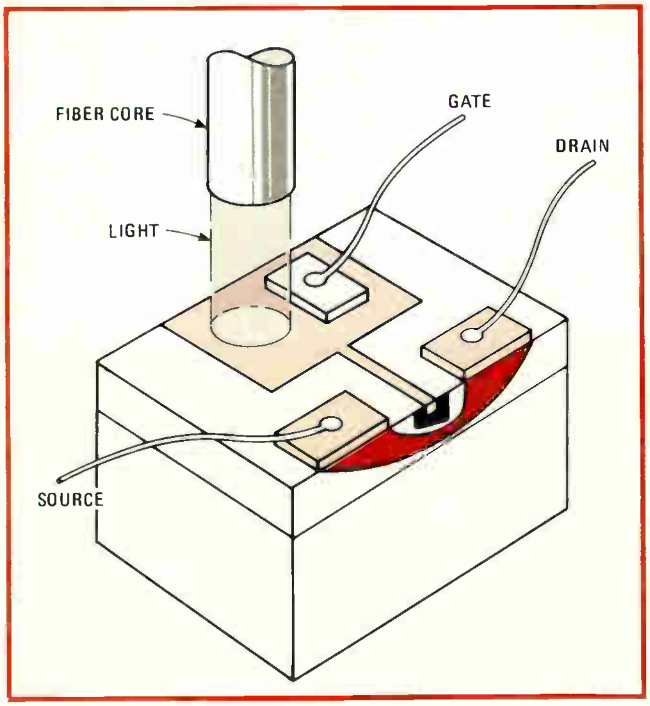
There are three subsystems in a fiber-optic communications system: the light source, the fiber cable, and the light receiver. To make any communications link as cost-effective as possible, the light source, typically a laser diode, should emit as much power as possible.

At the same time, the fiber should have as low an attenuation as can be achieved, and the receiver should be as sensitive as is practical. Although the IEDM will not deal with low-loss fibers, it will address the latest in laser diodes and photoreceivers.

Work at RCA Laboratories in Princeton, N. J., is a first-class example of the studies going on with laser diodes. Researchers there have concentrated on new laser diodes that can generate a large lasing spot size (useful for easy coupling into hair-thin fibers) while operating in substantially one mode (the laser's radiated electromagnetic field pattern). Single-mode operation makes coupling the generated energy into the fiber easier and designing a receiver less of a chore.

Until now, single-mode devices have tended to damage themselves unless their power outputs were constrained to a few milliwatts. The RCA devices, known as constricted double-heterojunction, large-optical-cavity (CHH-LOC) diodes do not have this limitation.

The price paid for the order-of-magnitude improvement in output power is a complex geometry (Fig. 2).




**3. Exotic.** The Bell Laboratories' combination of p-i-n and FET requires InGaAs n-layers grown by liquid-phase epitaxy on semi-insulating InP:Fe substrates. The p-layer for the p-i-n photodiode and the 20-$\mu$m wide FET gate were formed with a Zn diffusion.

Still, 40 milliwatts of single-mode, continuous-wave power has been produced—the highest ever. In fact, for a 50% duty cycle, 100 mW may be had. Unlike some diodes with exceptional output but no practical lifetime, the RCA devices operate more than 10,000 hours at 40 mW with only small changes in their characteristics.

Even though the CHH-LOC diodes appear to be the only practical diode sources suitable for the 20-to-100-mW range, their mere existence is not sufficient. They must function in practical communications systems and be capable of modulating information onto their light outputs at suitable data rates.

This performance imperative has not been ignored. Coupling the diodes to graded-index fiber—a commonly used type—data transmission at 450 megabits a second in both return-to-zero and nonreturn-to-zero formats is obtainable. Most importantly, the CHH-LOC diodes can do this while delivering an order-of-magnitude more power to the receiver than competing diodes. Analog signal transmission is also possible. Here, signal-to-noise ratios can be achieved that are as much as 20 dB better than those of conventional diodes.

## An integrated receiver

At the other end of the communications link, the receiver must do its best with weak signals, neither distorting them nor adding noise. One of the solutions to this problem is the integrated detector-amplifier.

Conventional wisdom holds that the avalanche photodiode is better than the p-i-n diode for the detection function because it is more sensitive. However, it is difficult to achieve low-noise operation of avalanche photodiodes in the 1.3-$\mu$m region of the spectrum where fiber attenuation is at a minimum. So researchers at Bell Laboratories in Holmdel, N. J., have designed an integrated p-i-n and FET photoreceiver, since p-i-n diodes show sufficient sensitivity at 1.3 $\mu$m for the device to perform satisfactorily.

It is not just integration's economies of size and cost that attracted the Bell labs researchers. The input capacitance of the photoreceiver can be minimized, thus allowing high data-rate inputs without distortion. Also, the transistor itself, made from unusual ratios of indium, gallium, and arsenic promises to work better than more conventionally made FETs.

In the Bell design, the p-i-n diode is made as an extension of the gate junction of the FET in order to optimize the integration of both devices (Fig. 3). With this approach, it is possible to achieve an input capacitance of less than 1 picofarad—a very low figure.

Like the Plessey researchers, the Bell team has modeled its photoreceiver in order to predict its behavior. The model indicates that it is possible to reduce the 1-pF capacitance even further if the diode is reduced to the minimum size required for compatibility with the associated optical fiber and if the contact pad is removed.

In this case, an order-of-magnitude reduction in area would be possible, with a corresponding decrease in input capacitance. System operating specifications are not yet available for the photoreceiver. On the other hand, its long-term potential for low-noise, high-data-rate optical reception is clear. □

## Two-chip VCO linearly controls ramp's amplitude and frequency

by Forrest P. Clay Jr. and Mark S. Eaton
*Department of Physics, Old Dominion University, Norfolk, Va.*

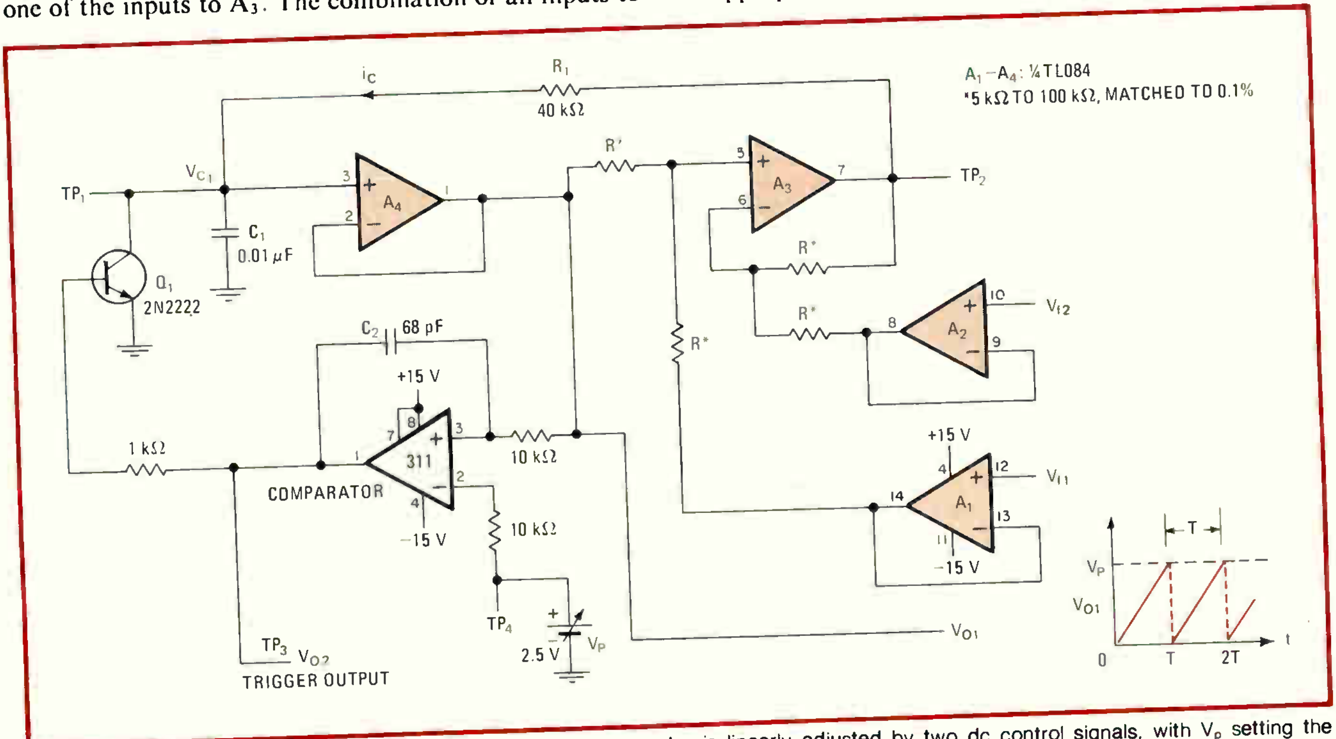
This inexpensive ramp generator provides a proportional voltage control of both the period and amplitude of a waveform over a wide range and thus doubles as a linear voltage-to-frequency converter. Only a few active devices are needed: two operational amplifiers and a transistor.

Two dc differential control signals, $V_{f_1}$ and $V_{f_2}$, are applied to op amps $A_1$ and $A_2$. The output from $A_3$ is $V_{C_1} + (V_{f_1} - V_{f_2}) = V_{C_1} + V_f$, where $V_{C_1}$ is the voltage across ramp capacitor $C_1$ and after buffering becomes one of the inputs to $A_3$. The combination of all inputs to $A_3$ yields a dc bootstrap circuit with a controlled offset voltage. Thus, current $i_c = (V_{C_1} + V_f - V_{C_1})/R_1 = V_f/R_1$, and the voltage across the capacitor is:

$$V_{C_1} = \int_0^t (i_c/C_1)dt = (V_f/R_1C_1)t$$

$C_1$ is discharged through transistor $Q_1$ at time T when $V_{C_1}$ equals the control voltage $V_p$, which is adjustable from 0 to 2.5 volts. thus $[V_{C1}]_{max} = V_p = (V_f/R_1C_1)\,T$ and $f = 1/T = V_f/V_pR_1C_1$. The 311 comparator has a trigger output to synchronize external circuitry for easy operation.

The slope of the control voltage versus frequency in kilohertz is 1 for $1 < V_f < 10$ volts. This linear relationship holds even for slow ramps (increasing the value of $C_1$) with small values of $V_f$. Capacitor $C_2$ is selected to maintain the 311's output in a high state long enough so that $C_1$ may be completely discharged through $Q_1$ during the appropriate portion of the cycle. □




**Potentially proportioned.** A two-chip, one-transistor ramp generator is linearly adjusted by two dc control signals, with $V_p$ setting the amplitude from 0 to 2.5 volts and $V_f$ and $V_p$ setting the frequency over the range of 0 to 10 kilohertz. Proportional control is achieved by placing ramp capacitor $C_1$ in the dc bootstrap circuit of $A_3$ and $A_4$, which ensures that constant current $i_c$ is a function of only $V_f$ and $R_1$.

## Interleaving decoder simplifies serial-to-parallel conversion

by A. J. Bryant
*Manelco Electronics Ltd., Winnipeg, Manitoba, Canada*

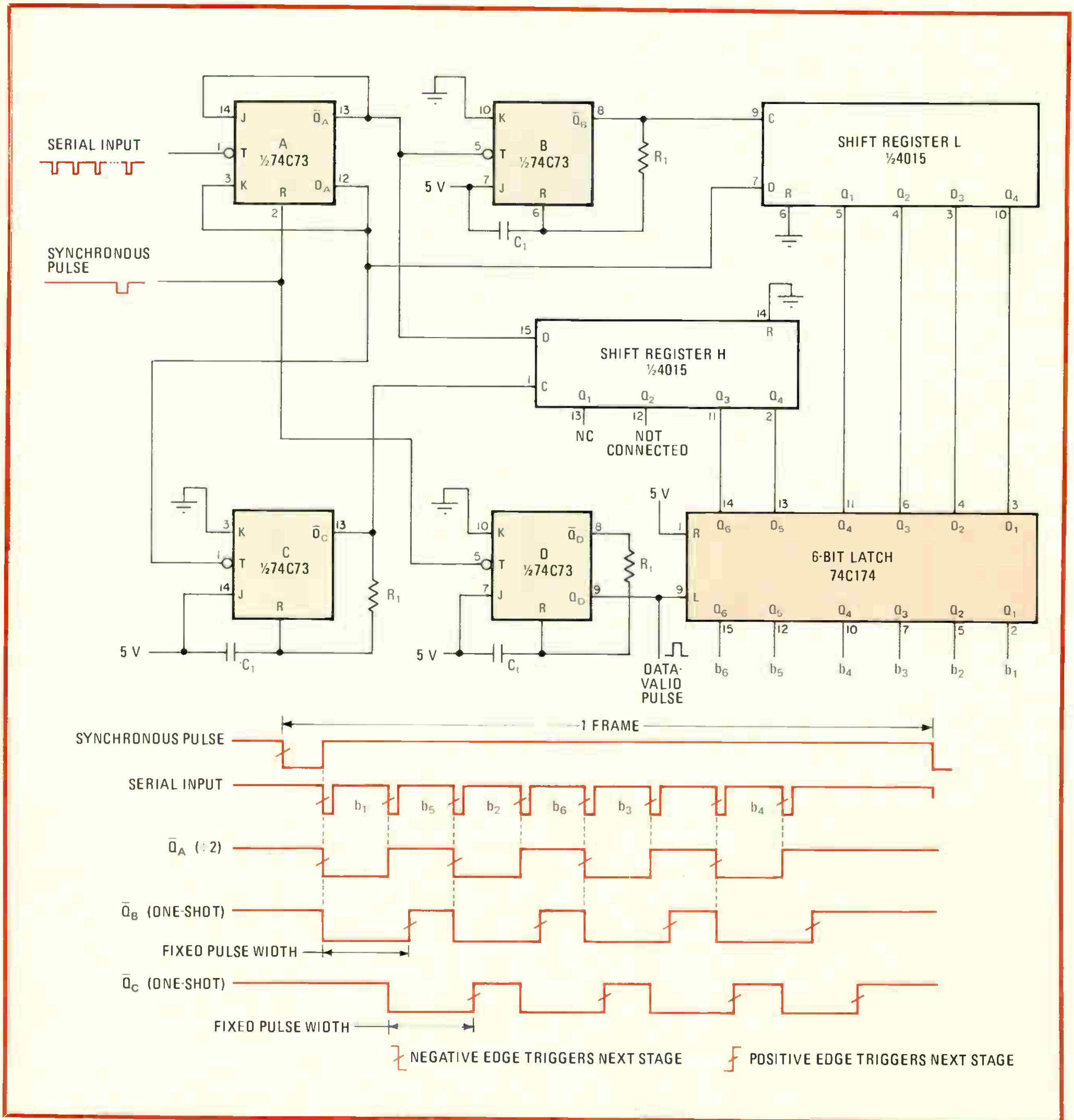
Four low-cost chips combine to convert a 6-bit serial pulse train into its parallel equivalent in this decoder. Its circuitry is simplified because the bits are broken into two data streams so that it takes only two 4-bit shift registers and a latch to do the conversion.

A synchronous pulse (derived from a pulse detector that is not shown in the figure) is applied to flip-flops A and D (½74C73), initiating the conversion. The serial stream of negative-going pulses that will be decoded is also applied to flip-flop A, which serves as a divide-by-2 counter.

Both outputs of flip-flop A are then applied to two 4-bit shift registers (4015)—one through one-shot B, which serves as a clock for stepping the corresponding complementary signal of A to register L, and the other through one-shot C, which performs the same function of loading data into shift register H. As seen from the timing diagram, this asynchronous loading arrangement permits the 6-bit input stream to be split and then interlaced, with shift register L receiving low-order bits $b_1$ to $b_4$, and shift register H taking bits $b_5$ to $b_6$.

All 6 bits are then positioned onto the lines of the 74C174 6-bit latch and strobed onto the latch by one-shot D on the next recurring synchronous pulse. The pulse width of D must be thinner than the synchronous pulse so that its use as the data-valid output does not overlap a new frame. □

*Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $75 for each item published.*




**Scrambled.** Separating 6-bit data into two streams enables serial-to-parallel conversion with only four chips. The timing diagram clarifies the bit-interleaving method used and details circuit operation. Timing components $R_1$ and $C_1$ for one-shots B and C should be selected to ensure that their on-time exceeds two data bits; $R_1$ and $C_1$ should be chosen to ensure there is no overlap with synchronous pulse into a new frame.

# Electronic-music generator retriggers waveforms

by Thomas Henry
*Electronic Music Studios, University of Iowa, Iowa City*

Only three chips, one transistor, and a few passive components make up a circuit that produces the control signals needed by voltage-controlled oscillators and amplifiers in order to modulate musical parameters like loudness, timbre, and pitch in an electronic synthesizer. The circuit retains the simplicity and compactness of an exponential generator [*Electronics*, July 17, 1980, p. 123], and it also permits retriggerable operation.

This envelope generator controls the attack, decay and release times of a waveform and its sustained level. The circuit, however, also responds independently to the trigger and gate input signals of a keyboard, thereby creating a continuously repeating attack-decay portion of the waveform.

The synthesizer's keyboard initiates trigger and gate signals that control circuit timing. The gate pulse is produced if at least one key is pushed, and the trigger pulse is produced whenever the lowest note desired is changed by selecting a new key.

Thus a gate and a trigger pulse is generated when a key is pushed. Pressing a second key lower on the keyboard while holding the first key down generates a new trigger pulse, but there is no change in the gate pulse because it remains high.

In the circuit's quiescent state, the charge on timing capacitor $C_3$ is zero. When a single key is pressed, the 555 timer, which contains a comparator and R-S flip-flop, is enabled by the gate signal.

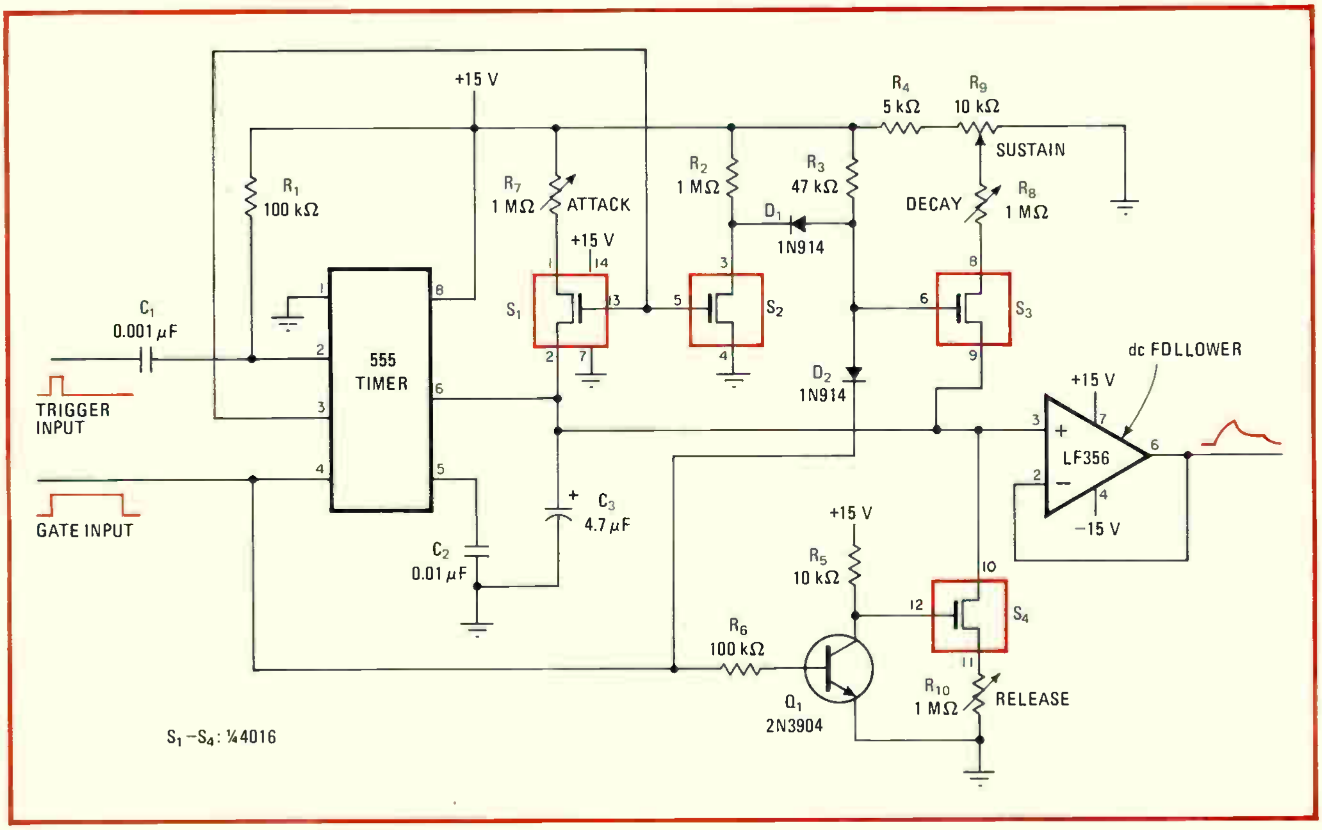
Following this action, the trigger signal is differentiated by the resistor-capacitor combination $R_1C_1$ and is applied to pin 2 of the timer to set its internal flip-flop and bring pin 3 high. Analog switch $S_1$ is thus turned on and current flows through resistor $R_7$ to charge $C_3$, initiating the attack portion of the waveform.

When the voltage across $C_3$ reaches 10 volts, the 555's flip-flop is reset. Pin 3 moves low and $S_1$ is turned off, thus terminating the cycle's attack portion.

At this time, the AND gate formed by $D_1$, $D_2$, and $R_3$ goes high, and analog switch $S_3$ is turned on. This switching permits $C_3$ to discharge through $R_8$, the decay-control potentiometer, to a voltage level specified by $R_9$, the sustain control. Resistor $R_4$ limits the range of sustain voltage from 0 to 10 V.

When the gate signal is removed, the AND gate goes low and $S_3$ is turned off. Transistor $Q_1$ is also turned off, which permits $S_4$ to turn on and $C_3$ to discharge through $R_{10}$ for the release portion of the waveform.

If the generator is in the sustain portion of its output cycle, and a new trigger occurs, the flip-flop will be set again and the attack and decay portions of the cycle will recur. Coupling the gate signal to pin 4 of the 555 ensures retriggering even if the wave is not permitted to reach the conclusion of its attack cycle. □




**Repeating repertoire.** The three-chip generator provides a four-step waveform, each cycle of which is adjustable, for modulating voltage-controlled oscillators in music synthesizers. Thus loudness, timbre, and pitch may be adjusted. The circuit costs under $8.

Design AUTOMATION

# Gate-array development system speeds designs to market

## Software package generates circuit patterns electronically with remote or local access

by James S. Koford, Edwin R. Jones, and Rob Walker, *LSI Logic Corp., Santa Clara, Calif.*

☐ Logic arrays would be even more appealing to systems companies if it were possible to personalize them faster. A new design-automation program that speeds up the process is available either on line by phone to customers of LSI Logic or as a package to those who have the right equipment. Besides generating an array's unique set of interconnections, it checks their timing and breadboards them electronically, reducing the risks of error.

This begins a second set of four articles on the automated design of integrated circuits, a series that began in the last issue. The focus is the new hardware and software tools available to the IC designer. The last issue contained an overview, plus articles on a MOS structure, cell library, and simulation system for chip development. This instalment covers systems for gate-array and custom-chip design as well as automated testing.

The attraction of logic arrays is that they offer an alternative to flexible, but lower-performance, standard logic families on the one hand and inflexible, and sometimes unsuitable, standard large-scale integrated devices on the other. They also provide considerably higher performance and speed-power product than their counterparts in standard small- and medium-scale integration because of their much lower interconnection capacitance and reduced on-chip noise-immunity requirements.

The larger arrays can replace a board or more of standard logic and substantially reduce the size and complexity of the final product. This also helps trim inventory and simplify maintenance. The replacement of tens to hundreds of SSI and MSI ICs and their attendant printed-circuit–board interconnections, solder joints, power supplies, and decoupling capacitors adds significantly to system reliability. All this means lower system costs when production requirements are sufficient to amortize design charges.

Yet there are obstacles to the widespread use of these devices. Almost any change to a logic-array design requires that new masks and prototypes be fabricated, entailing minimum costs of two weeks time and thousands of dollars. Other musts are good computer aids to achieve testing sequences that are able to detect potential faults, as well as standard design languages.

These obstacles are the same the industry faced a decade ago with microprocessors, and it will take many of the same tools and methodologies to exploit the full market potential of logic arrays. A significant step has been taken toward answering these demands by the LDS I universal development system for logic arrays.

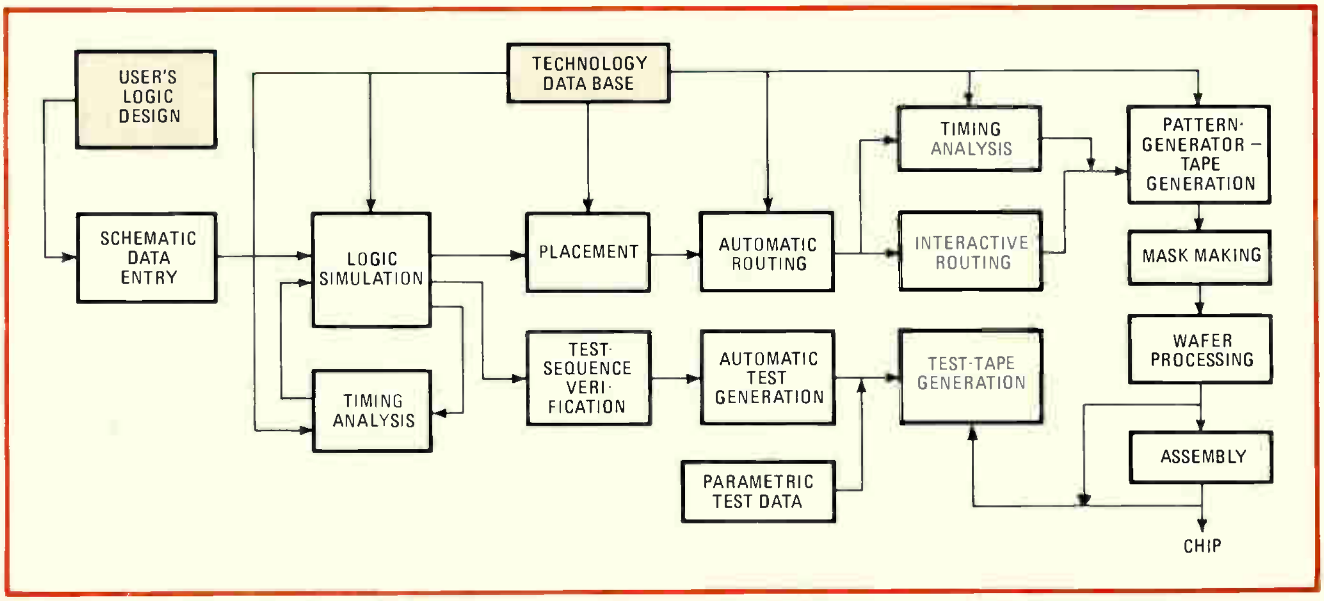
The LDS I was designed to meet a number of important objectives. First, it permits logic to be specified at the gate level as well as in a hierarchy of higher-level descriptions, including the common 7400 and 4000 logic family functions. Also, logic may be entered either graphically using a schematic diagram or alphanumerically using a wiring list. In addition, the system must perform digital function simulation and performance analysis, obviating the need to breadboard the circuit.

To achieve these goals, a variety of interactive and automatic design aids had to be incorporated into the LDS I. Also, verified circuits need automatic placement and routing with interactive modification and automatic generation of production documentation.

### More design goals

Ideally, the system should provide easy-to-use interactive techniques and should support both local and remote design terminals. Moreover, it itself should not be exclusive to any technology or array design, and array-specific information should be kept in specific data sets known as technology libraries. A fully integrated data base is also necessary to ensure that data be entered only once.

And finally, there was a deadline—the system had to




**1. The whole picture.** From start to finish, all design steps are depicted here. The user enters his logic design into a schematic entry program and from there the automatic steps speed along the design until the final task, when the mask set and chip are made.

be developed and be made available by the fourth quarter of this year, just eight months after its inception. This last restraint made it imperative to buy as much software as possible, as opposed to writing it all in house.

## System configuration

The company spent two months evaluating available software packages. The final selections were the SDS schematic data entry and the EDA automatic/interactive-placement and -routing program from Silvar-Lisco. The CC-TDL Tegas V logic-simulator program from Comsat General Information Systems of Austin, Texas, was selected, along with the Spice circuit simulation program from the University of California at Berkeley.

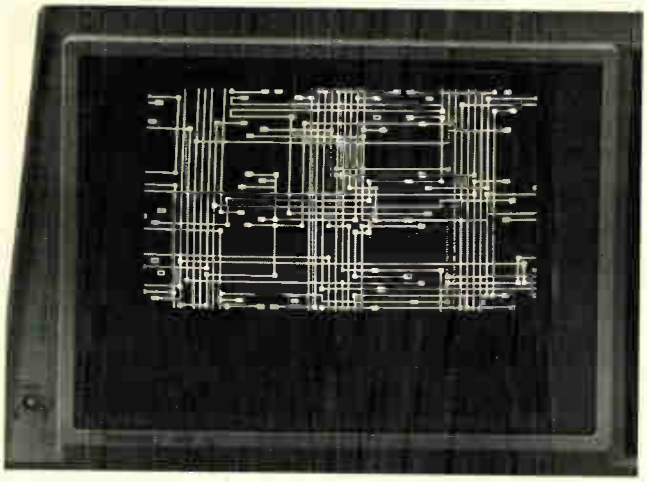
These programs handle about 60% of the company's requirements—the remaining programs and all the technology libraries had to be developed internally. A block diagram of the final system is shown in Fig. 1.

The simulation, test generation, and automatic routing of complex logic arrays require a large host computer, and analysis indicated a 32-bit virtual machine of 0.5 million to 1.0 million instructions per second and a minimum of 3 megabytes of physical memory. The VAX 780, Prime 750, or an IBM (or plug-compatible) machine in the 4341 class offers these capabilities. The IBM plug-compatible National Advanced Systems AS5000N was selected for the initial installation.

Since LDS I is designed to be accessed either locally or remotely over relatively slow telephone lines, several schemes were considered to increase communication throughput. The bulk of the simulation output consists of thousands of 1s and 0s; clearly, several simulation-output figures can be encoded into a single ASCII character. These outputs also tend to change infrequently, so that if signal changes only are sent, throughput can be significantly increased. Such techniques increase effective transmission speed by a factor of 10.

The effective data rate could also be boosted with local terminal storage. When a portion of a logic simulation or mask layout is requested, it may be transmitted in a compressed format by the host at 1,200 bits per second and displayed in real time. After a screenful of data is sent, the LDS I will continue to transmit more data into the terminals' local storage. Using a concept similar to cache memory, the extra data that is transmitted is that which the operator is most likely to need next. Because

**2. Graphics terminal.** The LDS I uses a Tektronix 4112 or 4113 graphics terminal as its interface with the designer. The terminal's power greatly enhances the total system. It uses a 16-bit 8086 with 500-K bytes of memory and a floppy disk, and it is programmable.



3. **Route and place.** The LDS I uses a combination of automatic and manual routing and placement. First the critical paths are manually placed and then the autorouting functions turned on. The user has full interactive editing capability during autorouting.

this data is in local storage, it is available at a very high effective rate.

For these reasons, the remote terminal required to handle the computation and storage must be powerful—hence the choice of the Tektronix 4112 or 4113 (Fig. 2), which uses dual 8086 microprocessors and supports 1 megabyte of local storage plus a diskette. Perhaps its greatest advantage here, the terminal is programmable by the host computer, so that any 4112 or 4113 is convertible to an LDS I terminal in a matter of seconds.

Special terminal software to support these LDS I functions is included in the portions of the LDS I system that are being developed internally.

The LDS I uses the Silvar-Lisco interface with the industry-standard Spice circuit-simulation program. Models include complementary-MOS structures, bipolar junction transistors, and diodes. Spice is used principally in setting up technology libraries and is not usually required for each specific design in an array family.

The LDS I uses a schematic entry system for creating and modifying schematic diagrams and entering them into the system. Starting from a rough sketch, the designer creates his schematics on an interactive graphics terminal like the Tektronix 4112 or 4113. He calls up logic elements from the LDS I library of logic-array macrocells. The logic elements, whether they are complex MSI functions or simple gates, are immediately displayed at all the locations requested, along with a standard text block.

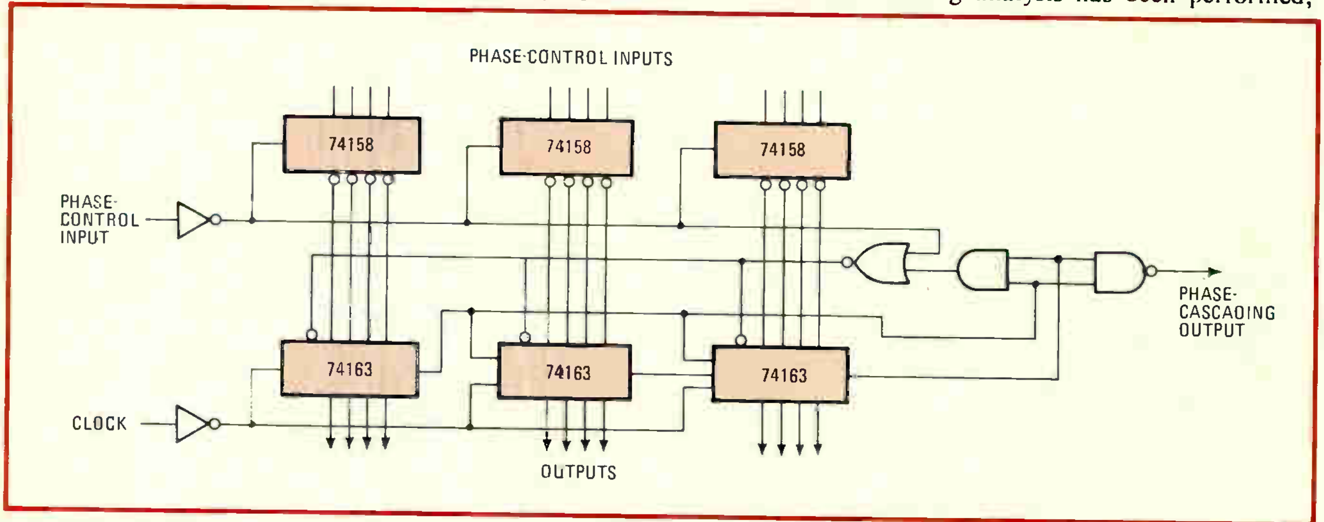
## Network description

Then, still working interactively through the terminal, the designer adds cell names and connecting lines. Once the schematic has been drawn and stored, the data is compiled into the Tegas V format so as to become the network description.

The simulation and test-generation system in the Tegas V software package contains a control-language processor, an automatic test generator, several postprocessors, and a family of simulators. The simulators that form the heart of the system contain a full complement of networks and digital devices.

With the family concept of simulators, a designer can first verify the functionality of his logic-array design. After the logic has been verified, he or she can add timing information. Nominal-delay timing analysis can be performed until the array's behavior has been verified on the basis of the typical device characteristics. Later, with little additional effort, the designer can perform a worst-case timing analysis.

When the final timing analysis has been performed,




4. **A typical example.** This modulo-4000 counter with phase control is shown here implemented using standard 7400 series parts. The LDS I has predefined macrocell wiring information for all 7400 parts in its data base. Discrete wiring could have been used as well.

the designer or test engineer will take the test patterns generated for verification of the array design and determine, through the fault-simulation mode, their fault-detection and -diagnostic capabilities. If these patterns are not sufficient, the user will add more tests and continue to perform fault simulation until the test pattern detects the required percentage of faults. He or she can also make use of the system's automatic test-generation capabilities.

Initially, LDS I supports automatic tape-format generation for Fairchild Sentry VII, Sentry VIII, and Sentry model 20 LSI testers. Other testers for LSI devices will be supported as they come into general use.

**PROGRAM TO DEFINE MODULO 4000 COUNTER**

```
COMPLIE S
DIRECTORY TNET S
OPTIONS REPLACE,XREF S
MODULE DVD4K//1/TNET S
INPUTS CP,IFAZN,I0,I1,I2,I3,I4,I5,I6,I7,I8,I9,I10,I11,ZIP,ONE $
OUTPUTS 0FAZN,O0,O1,O2,O3,O4,O5,O6,O7,O8,O9,O10,O11 S
USE C01 = C01//1/TCELL ,
    C03 = C03//1/TCELL ,
    C09 = C09//1/TCELL ,
    MS1158 = MSI158//1/TCELL ,
    MSI163 = MSI163//1/TCELL S
DEFINE REF = C01 (IFAZN) S
        CPN = C01 (CP) S
        M1 (A,B,C,D) = MSI158 (ONE,I0,ONE,I1,ONE,I2,ONE,I3,ZIP,REF) S
        M3 (E,F,G,H) = MSI158 (ONE,I4,ZIP,I5, ZIP,I6,ONE,I7,ZIP,REF) S
        M5 (I,J,K,L) = MSI158 (ONE,I8,ONE,I9,ONE,I10,ONE,I11,ZIP,REF) $
        M2 (O0,O1,O2,O3,TC0) = MSI163 (CPN,LOAD,ONE,A,B,C,D,ONE,ONE) $
        M4 (O4,O5,O6,O7,TC1)= MSI163 (CPN,LOAD,ONE,E,F,G,H,TC0,ONE) S
        M6 (O8,O9,O10,C11,TC2) = MSI163 (CPN,LOAD,ONE,I,J,K,L,TC0,TC1) S
        LOAD = C09 (TC0,TC2,REF) S
        OFAZN = C03 (TC0,TC2) S
END MODULE S
END COMPILE S
LOAD DVD4K//1/TNET S
END TDL S
```

A unique feature, also undergoing internal development, is the LDPS (for LSI delay path specification) program. Circuit simulators like the Spice program are suitable for simulating transistors, logic cells, macrocells, or a small number of logic elements. However, there are thousands of logic paths in an array, all of which are layout-dependent. It would be impractical to run Spice on all these paths, and yet complete delay specification of all paths is necessary to guarantee the chip will function within design restraints.

LDPS will calculate all pertinent logic paths and provide tabulations of worst-case positive- and negative-going delays for these paths. A technology library for each array type provides the necessary parameters. Prior to actual layout, these delays are based on typical interconnection loading. If a path is declared critical—requiring special care in the layout—the delay is calculated on the assumption of a more optimized interconnection loading. After layout is complete, LDPS is run again with actual interconnection loading to provide final worst-case delays.

**FAULT-ANALYSIS OUTPUT**

```
MODE 2  SIMULATION COMMENCED.
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME        442 ON ELEMENT - M2/D2/2
        - DUE TO A CHANGE ON ITS INPUTS AT TIME         437
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME        442 ON ELEMENT - M2/B2/2
        - DUE TO A CHANGE ON ITS INPUTS AT TIME         437
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME        446 ON ELEMENT - M2/D1/E
        - DUE TO A CHANGE ON ITS INPUTS AT TIME         443
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME        446 ON ELEMENT - M2/B1/E
        - DUE TO A CHANGE ON ITS INPUTS AT TIME         443
NET IS FIRST INITIALIZED AT TIME              476
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME        639 ON ELEMENT - M6/C3/2
        - DUE TO A CHANGE ON ITS INPUTS AT TIME         638
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME        639 ON ELEMENT - M2/C3/2
        - DUE TO A CHANGE ON ITS INPUTS AT TIME         638
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME       2235 ON ELEMENT - M2/C0/2
        - DUE TO A CHANGE ON ITS INPUTS AT TIME        2233
        DELSCH SPP
        A SPIKE WILL BE PRODUCED AT TIME       2239 ON ELEMENT - M2/C3/2
        - DUE TO A CHANGE ON ITS INPUTS AT TIME        2238
```

## Mask design

The LDS I utilizes the Silvar-Lisco EDA system for metal mask design. The input to the EDA system has three parts: the logical information that describes the connectivity of the design (the network description from Tegas), the topological characteristics of the cells, and the interconnection rules of the specific logic array.

With this information, the EDA system aids the user with placement, routing, and subsequent mask-making. Cell placement is created interactively and allows the user either to invoke automatic-placement algorithms or enter a placement manually, as shown in Fig. 3.

## Guided paths

A routing program guides intermacrocell connection patterns—the intramacrocell metal is predefined for each specific function. On arrays using 70% or less of the available cells, an automatic router may achieve 100% completion. In cases of higher utilization, a manual modification of the placement, followed by another attempt at autorouting, is usually attempted. LDS I includes an internally developed color-graphics layout editor for manual modifications.

Throughout the manual modifications, the editor checks any changes against the network data base and disallows interconnections that could change the function of the design. The editor is currently operating on locally attached Megatek 6250 terminals, and it will also be supported on remote Tektronix 4113 terminals. The output system is a data-base tape suitable for pattern generation. Composite drawings may be produced using Versatec, Calcomp, or similar plotters.

LDS I supports logical, topological, and parametric cell libraries for all arrays designed by LSI Logic Corp. All macrocell topological descriptions for a given array family are maintained in unique layout libraries. For each cell, a plot showing the logic symbol and cell interconnections is stored. After layout and checking, pattern-generator tapes incorporating the selected cells are derived from library information.

### A typical design

Figure 4 shows a phase-controlled modulo-4000 binary counter. This function, of approximately 300-gate complexity, will be implemented as a portion of a C-MOS logic array. While this function can be designed at the gate level, an MSI implementation design is much faster and also more natural for many logicians who are familiar with the standard logic families. MSI, however, suffers in efficiency compared with an all-optimized discrete logic design, which could reduce the number of gates to an absolute minimum.

The first step is to enter the network into the LDS I. Altogether, 25 TDL input lines are needed to define the logic elements and their interconnection. Alternatively, a schematic entry scheme could have been used. The coding efficiency of the MSI design is apparent from the fact that over 300 gates were defined in only 25 lines (see top program, p. 119). The MSI representations are called macrofunctions. Most 7400 and 4000 functions are predesigned and available from an LDS I library.

The next step is to apply inputs to a simulation model. In this example, 19 lines of code were used to define an input sequence. The functional simulation output is displayed as a report, with time displayed on the vertical axis and the selected outputs labeled horizontally.

The speed of the proposed design can be analyzed and the logic hazards, races, and spikes checked. If spikes are transmitted to memory elements, such as latches, the circuit could malfunction (see lower program, p. 119).

The Tegas program also analyzes the timing aspects of the design such as delays from clock transition to outputs or the minimum clock-pulse width. However, final values cannot be determined until after layout, because delays are also a function of interconnection capacitance.

### Test score

Next, test patterns for an LSI tester are generated. The simulation inputs used to verify the design make a good starting point, so Tegas is run in the test-verification mode. Here individual faults, such as a node stalled at 1 or 0, are introduced and the input sequences applied to the bad array. When an output signal on the bad network is noted to be different from that on the good one, that particular fault is deemed detected. After all the possible networks containing a single stuck node have been simulated, the overall test score is determined. In this case, the initial simulation picked up 58% of the potential faults (see printout, bottom left).

At this point, more input patterns may be described or the automatic test-generation option used. After a certain level of fault detection is reached, typically 90% to 95%, a Sentry or GenRad test tape is produced and the prototypes are ready for testing.

The interconnection mask is designed in parallel with test verification and generation. The interconnections previously entered, simulated, and verified correct are used as the data base. All macrofunctions are automatically decomposed into macrocells, which have predesigned metal interconnection patterns that have been stored in layout technology libraries.

Using the Silvar-Lisco EDA cell-placement and -routing package, some macrocells are first placed by hand. Pads and their associated input/output circuitry are placed to achieve the required package pinouts. Next, macrocells having tight delay specifications like critical paths are placed closely together. After the manual placement of some macrocells is complete, the EDA program generates placement of the remainder by using an automatic iterative procedure. Placement modifications may be made manually as required.

After the array is wired, the propagation delays can be rechecked. Since actual circuit loading is now known, more accurate delay values may be obtained. A path delay that is out of specification will necessitate logic modifications or a new placement and routing.

Once all path delays are within specification, the procedure calls for generating pattern-generator tapes, making masks and wafer metal, probing testing, assembling, and performing a final test—about a two-week task. If LDS I has been used correctly and a sound design practice followed, the design should be right the first time. □

**PERCENTAGE OF DETECTED FAULTS**

| | THIS PASS | | TOTALS | |
|---|---|---|---|---|
| | NUMBER | PERCENT | NUMBER | PERCENT |
| FAULTS DETECTED | 9. OF 17. | 52.94 | 350. OF 606. | 57.76 |
| FAULTS NOT DETECTED | 8. OF 17. | 47.06 | 250. OF 606. | 42.24 |

# Graphics editor constructs standard cells, symbolizes subsystems

## Work station aids cell placement with user-defined commands and symbols, interfaces with mainframes for data analysis

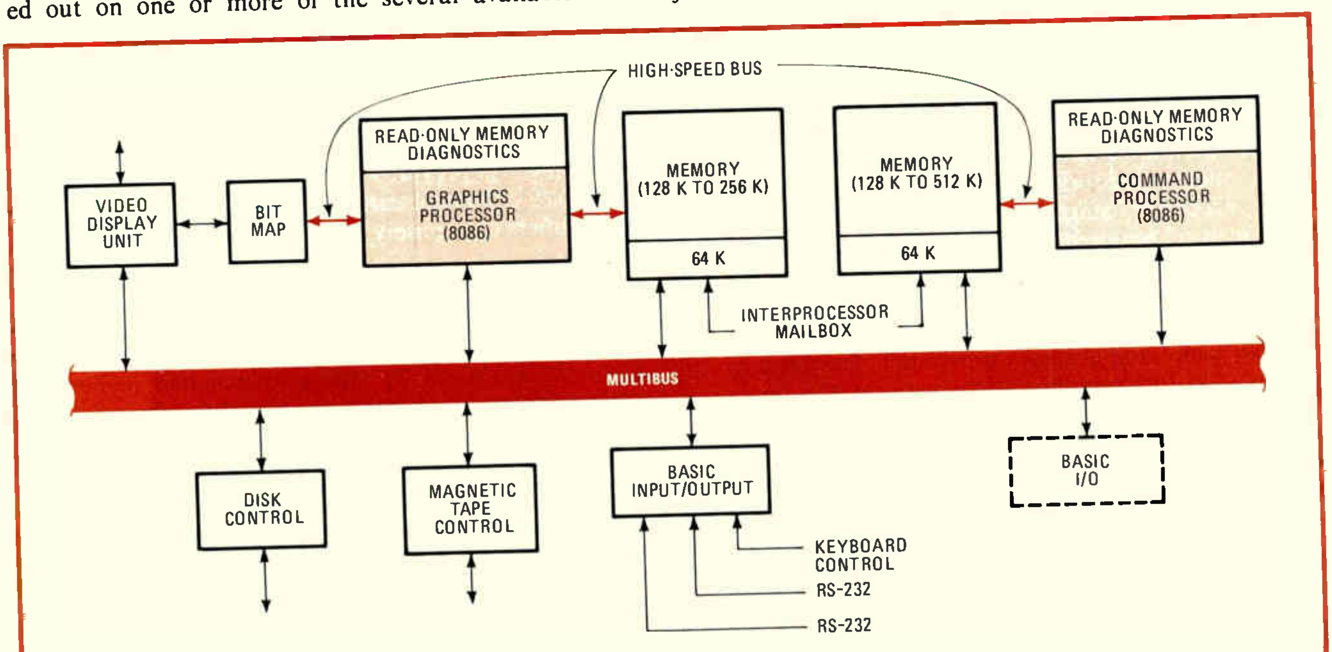
by Michael Dickens and Larry Dorie, *Avera Corp., Scotts Valley, Calif.*

☐ The virtue of very large-scale integration—fantastic complexity—is also its design challenge. However, the problem can be conquered by dividing it up. Once partitioned into independent blocks, the system may then be integrated sequentially by one designer or in parallel by a design team.

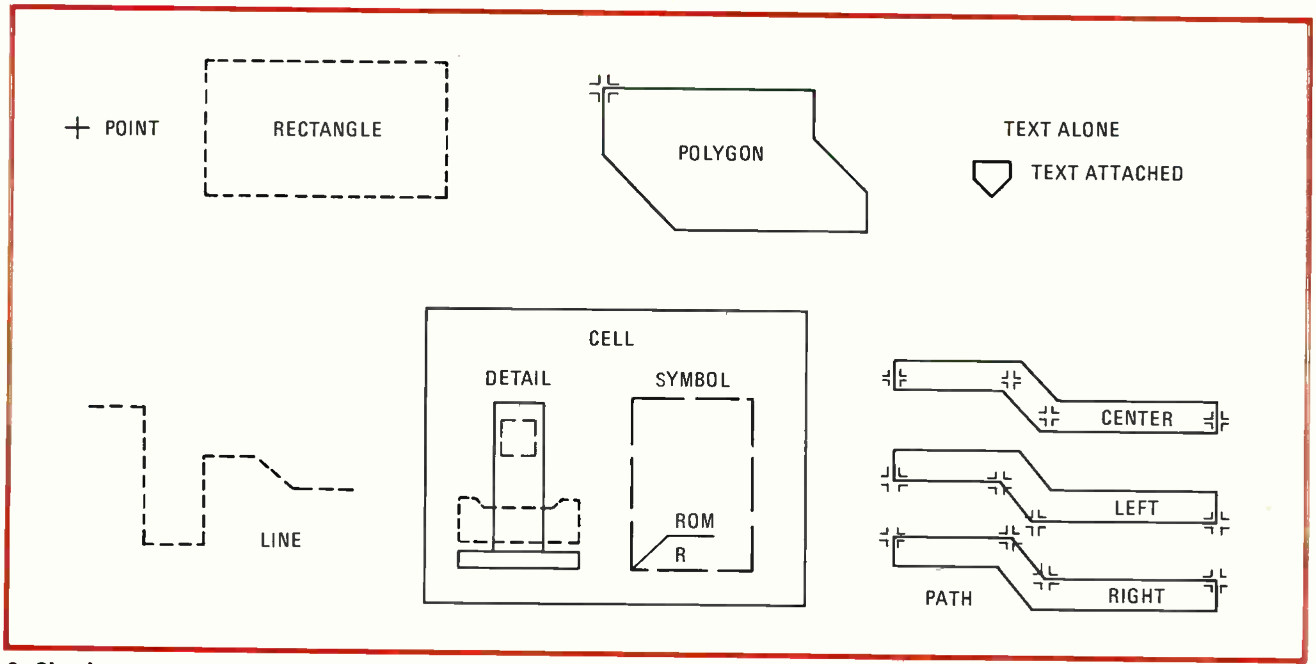
Such a hierarchical methodology requires various design-automation tools—and the tools must be hierarchically balanced in terms of their scope and power. In this sense, at least three levels of capability can be identified: full graphics manipulation, data analysis, and graphics editing. Graphics manipulation is usually carried out on one or more of the several available work stations costing about $280,000, whereas data analysis is reserved for a mainframe or superminicomputer.

While these tools have been assigned more or less properly, the graphics editing function has been given short shrift. This function, which involves the manipulation of symbolic cells to build up higher-level chip functions, has been addressed by everything from hand sketches to specialized programs designed to run on the work station intended for graphics manipulation.

Specifically tailored for editing integrated-circuit graphics, the Avera GS-1100 graphics work station aims to stop this misappropriation of resources. Its low cost is justified by the increase in productivity over manual




**1. Two-for-one system.** The Avera GS1100 graphics work station incorporates two 8086 microprocessors—one for display control and another for manipulating data structures. Several buses are used in the system, including serial links to computers and peripherals.




**2. Simple geometry.** With the GS-1100, geometric components are assembled into drawings. The components, which include polygons, rectangles, paths, lines, points, and textual information, can appear on any of 64 black and white or color layers similar to overlays.

methods. With the addition of this design tool, the three levels of chip design are matched with low-, medium-, and high-priced systems to do the work. Even if smaller companies cannot afford the machines for graphics manipulation and data analysis, they can get started with the GS-1100 to create a data base for a design and then let one of a growing number of service facilities execute the actual design.

### Dual-processor architecture

To achieve the objectives of high speed, low cost, and small size, the Avera GS-1100 incorporates two 16-bit 8086 microprocessors (Fig. 1). Memory capacity for each processor starts at 128-K bytes and can be expanded, if required, to 512-K bytes on one processor and 256-K bytes on the other.

The processors are functionally divided between data-structure–oriented tasks (the command processor) and display tasks (the graphics processor). The Intel Multibus is used for communications between the processors and peripheral devices, whereas a proprietary high-speed bus is used for communicating graphics data to the display subsystem.

The display allows either high-resolution black and white or color graphics plus selective-erasure and split-screen functions. The color display mode features automatic color filling, as well as color area outlining and overlaying—all of which prove useful in VLSI circuit development. Up to 256 colors can be displayed at a time from the 4,096-color palette.

The system employs 8-inch disk drives—either floppy diskette or Winchester types—plus two RS-232 ports for peripheral support and linking to a mainframe. Data tablets and hard-copy devices can be attached to these ports, as can modems or local links. With the Multibus, the work station can be expanded to include Ethernet interfaces or other specialized functions.

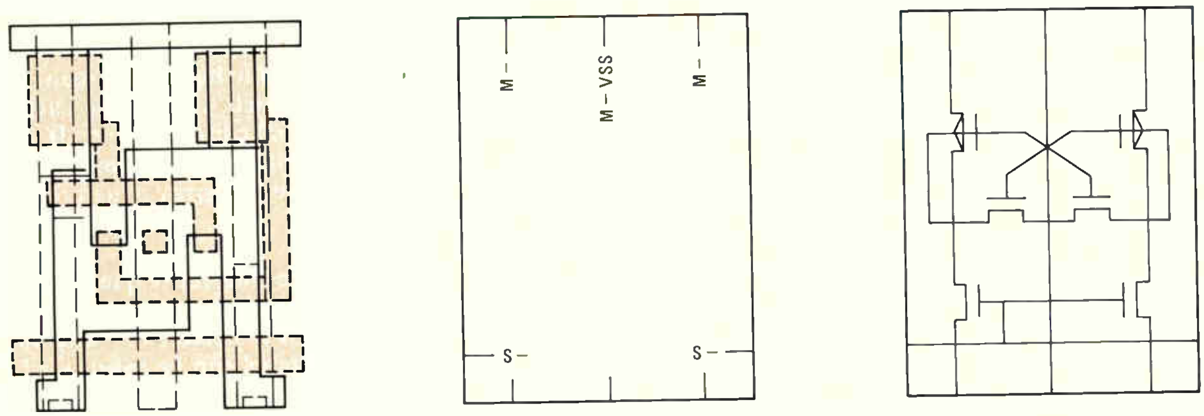
To accommodate the needs of diverse users, the system employs a language that is consistent, English-oriented, and limited in its command types (see table). Flexibility and power are achieved through command modifiers, which substantially reduce the number of commands yet provide hundreds of options. For example, the MOVE command can be followed by any combination of modifiers to precisely specify the desired operation.

### Software is the key

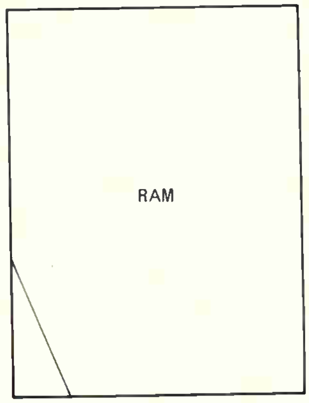
The command language also lets the user easily build new commands and macrofunctions that can be invoked from the keyboard by typing abbreviated names. The commands or macrofunctions may be assigned to programmable function keys, displayed on the screen in menu boxes, or entered as user-defined symbols from the graphics cursor-control device.

As a result, a user can quickly and easily build a dictionary of 50 or more frequently used functions and assign them to the most comfortable input mechanism. The on-screen menus and user-defined symbols let the user concentrate on the display screen at all times, removing the distraction of having to search for a particular button.

Besides a consistent, easy-to-use graphics command




DETAIL SYMBOL    INTERCONNECT SYMBOL    SCHEMATIC SYMBOL




OUTLINE SYMBOL

**3. The same but different.** With hierarchical partitioning, a cell in the data structure can have different representations. All four drawings here depict a random-access memory cell.

**COMMANDS AVAILABLE ON THE AVERA GS-1100 DESIGN SYSTEM**

| Commands | Actions taken |
| --- | --- |
| Manipulate | Maneuvers and acts upon components; enables the designer to initiate such actions as add, move, delete, and rotate. |
| View | Controls the movement of the viewing window. |
| Control | Checks drawings for data correctness; allows saved commands to be repeated; reverses the effects of incorrect commands. |
| Edit | Allows the user to define and modify macrofunctions, function buttons, and symbols. |
| Status | Enables the designer to display and set the current values of many system conditions. |

language, the system simplifies the entering of graphics data. To ease the transition from the drafting board to the on-line design function, the GS-1100 incorporates a gridding system resembling the familiar Mylar surface. It includes a working grid and a counting, or major, grid, both of which are found on Mylar sheets. The system can also force components to align themselves with the grid points (grid-snapping), much as is achieved with manual drafting operations.

The graphics editor on the GS-1100 required software tools not previously available. A multitasking operating system was adapted to the dual-processor environment, with Pascal used for development.

A native compiler was not initially available, so compiled minicomputer code was translated into the microprocessor-based system. This approach allows existing user-generated Pascal programs to be interfaced with the graphics system, with on-system compilation remaining possible at a later date.

The graphics data structure of the GS-1100 provides the IC designer with basic geometric building blocks, called components, to assemble drawings. The components, which include polygons, rectangles, paths, lines, points, and text, can appear on any of 64 drawing layers similar to overlays (Fig. 2). For black and white displays, there are four cross-hatch patterns and eight different outline types to aid in layer differentiation.

## Hierarchical data structures

Any combination of components can be grouped together and called a cell, enabling the designer to create drawings of great complexity. Besides being hierarchical, the data structure features a unique associative capability that adds flexibility by nesting one associated item within the other.

Another software feature helpful in hierarchical partitioning is the ability to carry different representations of a cell in the data structure (Fig. 3). Often in IC design, a cell showing all mask layers in detail is used to derive a symbol for the cell. The symbol may show important interconnection points and schematic data, but may not contain any mask information. The designer can use the symbol to show the function of the cell and how to interconnect it, but once a basic design is completed, the cells can be independently shown in detail, if desired, to allow further handcrafting in the traditional manner.

Several designers thus may work on the same basic layout, or they may develop similar layouts using different drawing diskettes. Typically, the cells of related drawings are standardized and shared.

The GS-1100 isolates cells from layouts by storing cell definitions in a library. This protects designers from inadvertently using the wrong revisions of cells in drawing sections. Whenever a drawing diskette is loaded, the system checks whether the cells it requires are present in the library. If a drawing from an unrelated application (such as a printed-circuit layout) were loaded with integrated-circuit cells, an error would occur. Each required cell not available in the library would be listed and the loading sequence could be started over again by replacing the cell library with the correct one.

### Symbol recognition

Commands are entered into the GS-1100 by moving a cursor over symbols on the display screen. The cursor is a visual marker that locates the position of the graphics input device. Each hand-drawn symbol can be assigned a simple command or a complex macrofunction. This symbol recognition provides a form of command entry that is typically faster than through a keyboard.

For manual drafting approaches, the input medium using standard digitizing techniques is composite sheets of gridded Mylar, each square representing 1 square millimeter. After formulating a plan for the chip and determining the location of important circuit elements, the next step is to pick up a sheet of Mylar and start arbitrarily drawing some portion of the circuit at full scale—1,000 times its actual size. Typically, a circuit will require about 60 Mylar sheets, each with 10 to 20 overlays to represent circuit details.

### Precise partitioning

Although the chip plan is a rough partitioning according to function, each functional portion may require several sheets of Mylar. At each sheet boundary, the various logic cells and portions of memory arrays have to be precisely matched. To enter this information into a computer, each and every location must be digitized, plotted, and then manually checked, often on 30 to 60 sheets of Mylar.

With traditional methods, no matter what the designer is working on at a particular moment, the entire circuit is displayed. If the process has been computerized, the entire device, repeated elements and all, is stored as a whole. The designer, placing larger and larger functional blocks, is essentially working with two levels of nesting: the basic cell, nested within the next larger level, the array. Arrays are then placed to build the circuit.

In the hierarchical approach, the chip is partitioned along the lines of the original chip plan (Fig. 4). Memory cells and other basic units may be repeated as many times as necessary to build up an array structure.

### Superior nesting

A more sophisticated nesting technique can also be used. Once a particular structure has been defined as the smallest unit in an array, it is stored as a basic building block, and a simplified symbol can be substituted for it on the larger array. This symbol, together with all pertinent interconnection information, can be used to build up the displayed array. When finally completed, the array can also be stored in its own separate file on disk, given a symbol, and then used at the next level in the hierarchy. Up to 16 levels can be nested in a hierarchical manner using the GS-1100.

With this technique, only the information appropriate to a particular level is displayed. In a read-only-memory array, for example, only the ROM cell symbol—with appropriate interconnection lines displayed—would be repeated. The detail of the cell is off-loaded to tape storage or transmitted over a communication link for storage on a mainframe computer disk. If some alteration is required on the cell, the detail is fetched from the disk and the appropriate changes made.

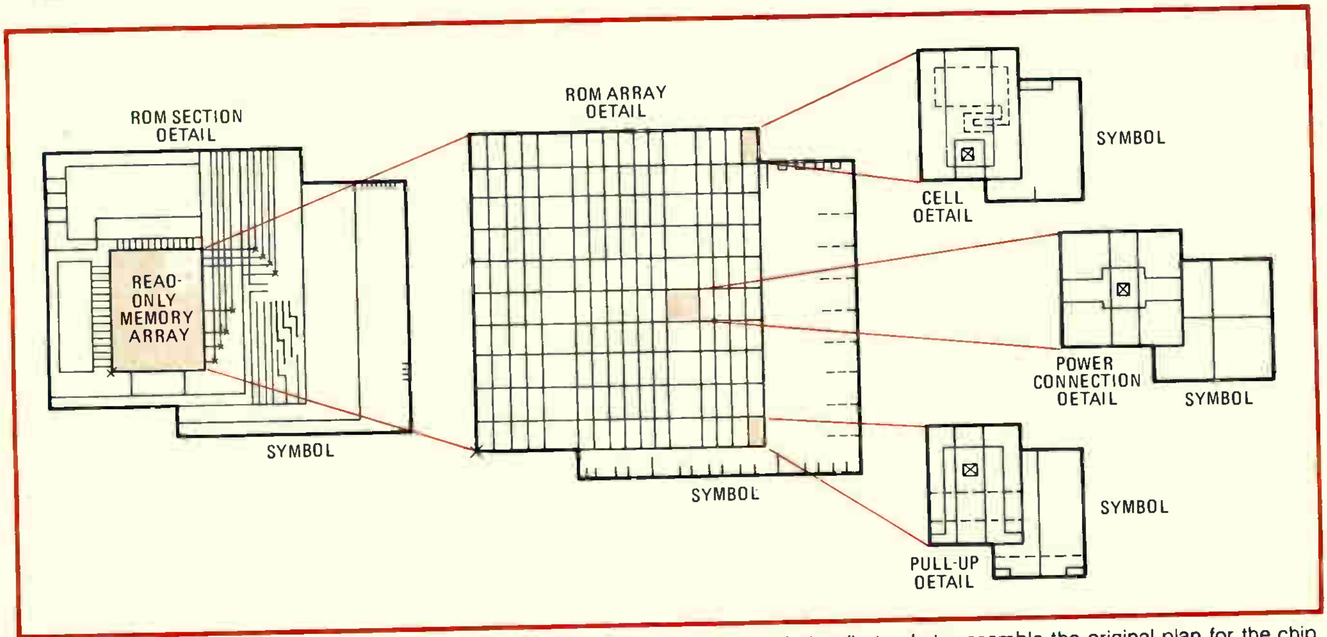
### Linking up

The chip can be built up even further—as much as a quarter of the die could go on cell placement. At any step along the sequence, the full amount of data is available from the mainframe or tape, but without penalty in work-station disk space or access time.

Although graphics work stations are vital links in the hierarchy of computer-aided design, the most computation-intensive functions—design rule-checking, logic or circuit simulation, and mask-pattern generation—are best left for a more powerful mainframe. This means that the desktop work station must be able to link to such computers conveniently.

While the future promises high-speed local networks such as Ethernet, there are at present few such elegant solutions. Although adaptable to Ethernet, the GS-1100 has been designed with a comprehensive RS-232 interface for immediate use. The hardware can support synchronous or asynchronous data transmission under software control. A straightforward protocol has been developed that allows the transmission of ASCII data with full error-checking and re-send capabilities, thus allowing compatibility with virtually any computer.

Source code, supplied by Avera, is brought up on the mainframe to establish the protocol link for the transfer




**4. Regularized.** When a hierarchical approach to integrated-circuit design is used, the die tends to resemble the original plan for the chip. Only three different cells—a memory bit, and details for power and pull-up connections—need to be pulled from the library and replicated.

of files to and from the work station. This will allow the use of local networks with similar ease.

Besides standard components, the design of custom and semicustom circuits can benefit greatly from hierarchical structuring. If the layout design is done manually, early completion depends on conservative—if not generous—design rules and estimates of area in the chip plan. It also means the extensive use of standard cells and higher-level functional blocks.

### A general-purpose VLSI design tool

An interactive graphics station eases the development of the standard-cell library—especially the production of cell variations given a copy of an existing cell. Such work stations also aid in the initial placement of critical paths, the completion of interconnections not done by the mainframe computer, and the display and correction of design-rule errors.

Most important of all, perhaps, is the adherence to the partition interface points located in the chip plan. An interactive graphics system incorporating low-cost work stations like the GS-1100 can simplify compliance by displaying a chip-plan section as a reference framework for doing detailed layout work.

Primitive cells—in this case consisting solely of interconnection patterns—can be developed for functional blocks such as flip-flops, NAND gates, registers, and counters. From these, the size and shape of larger partitions can be estimated. Working top down with these estimates, partitions can then be arranged on the chip. In the majority of cases, the shape and arrangement of upper- and middle-level partitions will need several iterations before a satisfactory chip plan can be obtained.

The most common semicustom IC is the gate array or uncommitted logic array. While automated techniques are sometimes employed, semicustom design is most frequently done manually. A microprocessor-based graphics work station fits well into the semicustom environment because the power and expense of high-capacity systems cannot be justified. Once a cell or partition is laid out, design-rule checking can be done on that section by communicating the graphics information to a larger computer—even one located at an off-site service bureau. Error reports and layout corrections can then be displayed at the work station to finish the design.

### Custom tailoring

An interactive graphics work station can also play an important role when computer-aided placement and routing are used to interconnect the semicustom chip. Any critical paths may be laid out manually, as a first step. Functional blocks can then be specified to increase the program's success level. Finally, a display of the program's results can be used to complete the design manually, which typically requires considerable editing effort as well as the addition of final interconnections.

Used in an on-line design mode, an interactive graphics work station also serves detailed layout well. Cell placements and interconnections can be directly entered and modified. Furthermore, an area logically similar to one that has been already completed can be produced by copying and modifying the existing area. This is both faster and less prone to errors than drawing the new area from scratch. □

# Cell-library system accommodates any degree of design expertise

## Circuit collection catalogs standard functions for efficient semicustom chip layout

by Donald E. Farina, John R. Duffy, and Tore L. Kellgren, *Alphatron Inc., Cupertino, Calif.*

☐ Although the gate array marked a first step to systems companies' participation in the design of large-scale integrated circuits, many product designers are beginning to want more. The cell-library method of computer-aided design represents a leap beyond the gate array that forges a close partnership between the engineer and CAD tools—the human being supplies the intelligence, the computers perform the routine tasks.

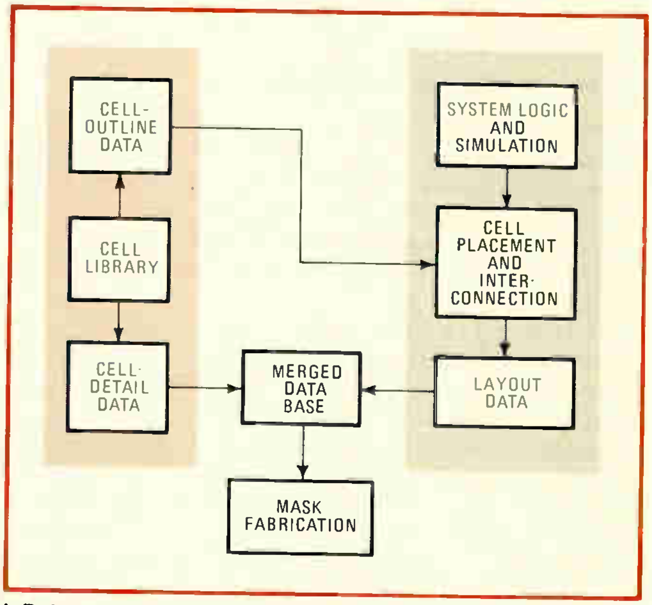
The gate-array method, popularized in the late 1970s, provides an alternative to fully custom chips, offering a fixed layouts of devices that are interconnected by the user. But the approach still requires considerable expertise in device technology because design proceeds at the level of individual circuit elements. In contrast, cells—larger, more complex circuit blocks—make a semicustom IC layout available to more users and with a lower cost and level of expertise. In another improvement over gate arrays, cell-library CAD permits memory and analog circuits to be integrated, greatly enhancing the capabilities of dedicated chips.

Systems companies are especially attracted to the cell library for several reasons. Because the method is accessible to users without special knowledge of semiconductors, the division charged to develop a new product can participate directly in its birth, thus learning its particular foibles and tradeoffs.

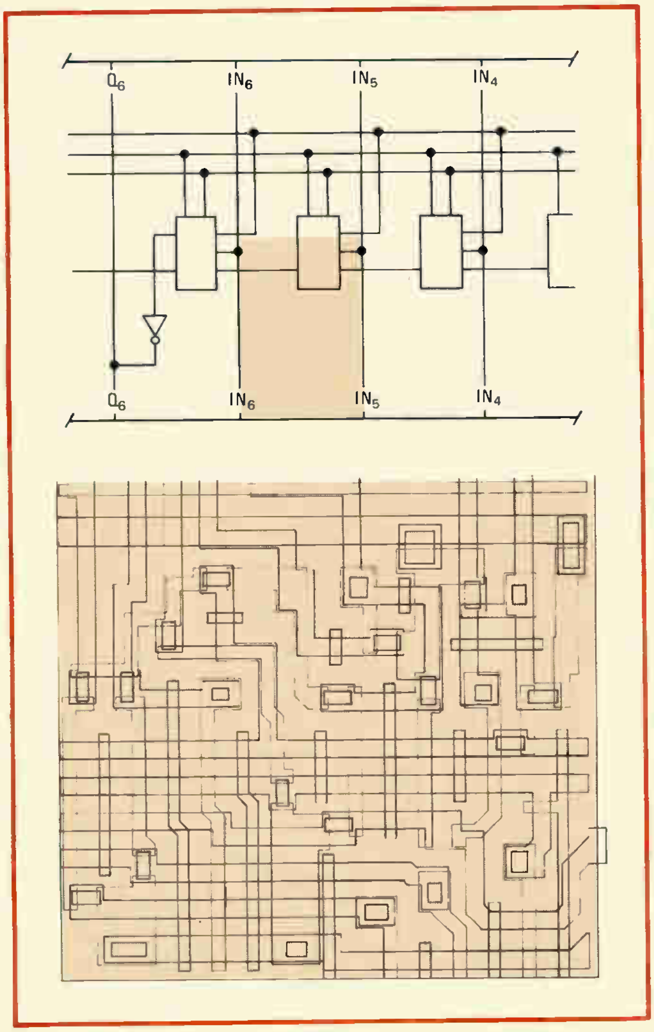
Further, because the standard cells contained in the library already have been made and tested, prototype development proceeds at exceptionally low risk. And whereas gate arrays often waste space with unused devices, the densely designed cell-library chip is more efficient and thus cost-effective. Moreover, the resulting chip design will be compatible with the processing capabilities of many wafer manufacturers.

Typical of this new breed of semicustom design is the cell-library system marketed as Alphamap. Like the traditional cell library of the custom IC designer, Alphamap uses previously designed and proven circuit elements that are representative of generally useful logical functions. The design task thus is reduced to selecting the appropriate logical functions from the library and making the necessary interconnections. If a new function is needed and promises to be popular, it will be added to the library. Or, if users have some IC design expertise themselves, they can lay out their own specialized cells to be used in conjunction with the standard functions that are already available.

Alphamap's strength is its versatility—it can accommodate any degree of CAD know-how on the user's part. The cells can be arranged and connected by hand, using scaled Mylar decals that represent the library functions.




**1. Data merger.** Detailed device layouts from the company and cell placement and routing specifications from the user are merged to complete the data base required for mask making. The cell-outline data is provided to the user either as Mylar decals or in software.




2. **Hidden structure.** Cell outlines—such as this section of an 8-bit shift register—show only the information needed by a logic designer. Complex device technology (tinted areas) need not concern the user and is added to the layout at a later stage.

At this level, it is possible to proceed without having to resort to any CAD tools at all.

In this situation, after the chip layout has been depicted, Alphatron Inc. creates a data base by copying the cell placements and interconnections from the user's drawing, following the requisite design rules. Cell detail is then merged into the data base, with software automatically checking interconnection design rules, loading, and continuity. Finally, from this verified base, the mask tooling is generated.

### Versatile

However, there is a computerized alternative to this design method. For users with some access to CAD equipment, the sequence of events is similar, but the cells are provided on a magnetic tape or floppy disk, to be called up and assembled at the CAD station.

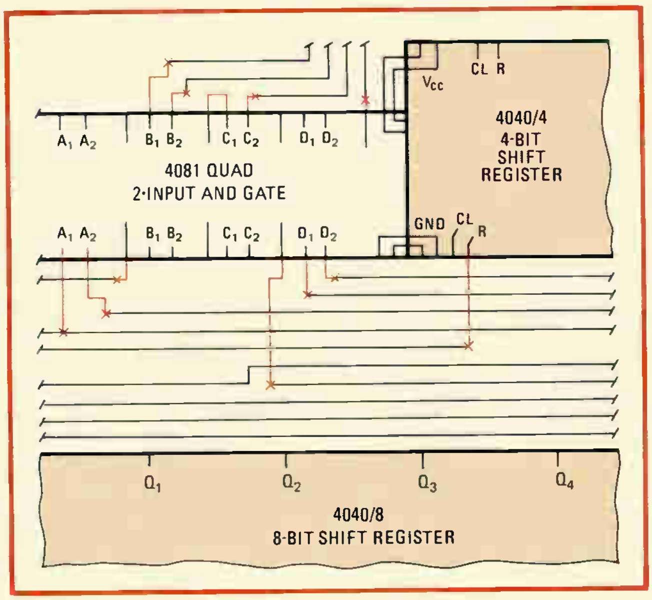
The functions required are available with the Alphamap on-line design system. Or, an automatic placement and routing program such as MP2D, PRF, or Gaelic could assemble the scaled cells into an IC layout. Then a layout data base is created and shipped to Alphatron, to be merged with the cell-detail data and checked before masks are tooled for wafer fabrication (Fig. 1).

Computer aids, in the Alphamap approach, thus serve users' needs in two ways. Indirectly, systems designers reap the benefits of Alphatron's CAD expertise as it is applied to the design, checking, and production of the standard cells. In addition, information supplied by Alphatron will give the designer with access to a graphics-display terminal simple means to optimize chip partitioning. A handbook provides formulas for evaluating system performance and expected development and production costs. With a computer to handle the repetitive calculations, the designer can rapidly check out many possible solutions to the problems at hand.

### How it's done

The cells provided to the systems engineer are scaled-up outlines of the actual silicon area occupied by the circuit blocks. The outlines are 180 times actual size and indicate the input and output connections, ground and supply-voltage locations, and the logical functions.

Thus supplied with the specifications of the logic function, electrical characteristics, and physical location of connection points, the designer can treat the elements




3. **Chip traces.** Board-level designers lay out a semicustom chip in much the same way as a printed-circuit board. Standard cells play the role of integrated-circuit packages and two levels of interconnections route signals among these circuit blocks.

of the cell library just like the standard ICs of a board-level design. In fact, much of the library is composed of compact cells that emulate the complementary-MOS 4000 and 74C series of small-scale ICs. Besides these popular gates and flip-flops, the library includes many common medium-scale IC functions, such as shift registers, counters, multiplexers, decoders, and analog switches. Cells for input and output pads meet the 4000-series specifications, with Schmitt-trigger inputs and three-state, push-pull, or open-drain output buffers.

Other more complex functions are being added to the library, including read-only and random-access memory, operational amplifiers, analog-to-digital converters, and switched-capacitor filters. In all cases the systems engineer uses data sheets included with the Alphamap U/PAC kit to organize a chip layout without concern for the details of the MOS-device topology.

A number of utility cells are also included, providing testing devices for verifying that the wafers meet process parameters, alignment marks for the masking steps of wafer processing, reduction marks for the mask-making process, a scribeline to facilitate cutting the wafer into individual die, and identification letters and digits.

**Design ground rules**

A portion of an eight-stage shift-register cell's outline is shown in Fig. 2, along with a section of the cell detail provided by Alphatron. All inputs and outputs are accessible from both sides of the cell, greatly increasing flexibility in connecting the cells together. Service terminals (supply voltage and ground) are provided in all four corners, allowing power to be connected to the cells after the cells have simply been stacked together.

Design rules are few and easy to follow. Power connections are 14 micrometers wide and are always made on the metal interconnection layer. Signal-line connections to the cells are made on the diffusion layer and are spaced 21 $\mu$m apart. Thus the terminals of adjacent cells can make contact with metal lines without angling the diffusion interconnection for the contact.

The two interconnection levels, metal and diffusion, are drawn with only the center line of the desired path. A space of two grid units—14 $\mu$m—separates these lines on each layer. When drawn by hand, the metal and diffusion layers are in different colors. A metal-to-diffusion interconnection is shown with the symbol X. The placement accuracy of the decals, or cell outlines, is not critical since the layout will be captured on a CAD system either by the systems company or by Alphatron.

Whether hand- or computer-drawn, the layout data base will be merged with the topological detail of the cells at a later stage in the sequence, to allow as much of the design as possible to proceed at the simpler level of the cell outlines and single-line interconnections (Fig. 3).

It is not necessary to redo most of the CAD operations on the detailed cell topologies because these have been completed prior to being installed in the library. This permits very fast and inexpensive logic simulation, test-pattern generation, and data-handling and -checking routines because the amount of coding and data manipulation is relatively small. From the cell-placement diagram, the systems engineer can estimate capacitive loading of critical speed paths, measure exact chip size, and calculate costs for development and production.

With this CAD approach, the time to design and lay out an IC is simply what is required to commit an interconnection diagram to a data-base tape for mask tooling—a matter of weeks. The data base created is compatible with all the traditional checking routines used on custom layouts.

Alphatron, which supplies gate-array, cell-library, and fully custom chips, has compared the costs of these methods. The table illustrates a typical comparison between the gate-array and Alphamap cell-library systems when the customer lays out the chip. It is assumed that the gate array is 75% efficient, so that a 1,000-gate chip is needed to provide 750 usable gates. The development times shown do not include the time taken by the user to lay out the chip. Although the direct development cost of the gate array is almost half that of Alphamap, the production prices—or, correspondingly, the chip areas—are so disparate, that only 840 chips need be produced in order for the cell-library approach to become the more economical.

A similar comparison may be made with fully custom designs by assuming the chip layouts are completed by the design service from logic drawings supplied by the customer. In this case, the much higher development costs to the user—$63,000 compared with $35,000—for a custom design and the modest decrease in production prices—about 15%—make the cell-library approach the better buy until production exceeds 40,000 units. □

**GATE-ARRAY VERSUS CELL-LIBRARY DEVELOPMENT COSTS**

| | Gate array | Alphamap library |
|---|---|---|
| Chip specifications | | |
| Number of gates | 1,000 | 750 |
| Chip area (mil²) | 67,600 | 22,500 |
| Development costs ($ thousands) | | |
| Engineering | $0.5 | $0.5 |
| Layout | 0 | 0.5 |
| Artwork, tooling, and wafers | 4 | 11 |
| Prototype evaluation | 1 | 1 |
| Simulation and test generation | 3 | 3 |
| Total direct costs | 8.5 | 16 |
| Typical cost to user | $ 14,000 | $ 27,000 |
| Development time (months) | 1 – 2 | 2 – 3 |
| Production price ($) (up to 25,000 in plastic DIPs) | $ 20 | $ 4.50 |
| Break-even volume | 840 | |

# Automating test generation closes the design loop

Missing CAD elements—automatic vector generators and high-level languages for test and network description—will soon be added

by Robert Hickling and Glenn Case, *Fairchild Camera & Instrument Corp., Test Systems Group, San Jose, Calif.*

☐ Techniques used in automatic testing of very large-scale integrated circuits are beginning to converge with those used in VLSI design. Although the integration of these two disciplines has already begun, considerable work remains before manufacturers obtain a unified system such as that of Fig. 1. As a result, researchers in computer-aided design are compelled to produce new aids for testing and test generation.

Fundamental to satisfying these requirements is the development of high-level network simulation and of test-vector–generation languages, as well as the evolution of new automatic test-vector–generation algorithms. To understand the relevance of these developments and the ways in which they are likely to come about, the status of both testing and CAD must be reviewed.

## Today's test

Four basic approaches to component testing are widely used today: self-testing, comparison testing, algorithmic testing, and stored-vector testing. They leave the creation of test vectors to the user, and this is a time-consuming process at present. Also, an uncertainty always remains as to how well the device has been tested and how many faults remain undetected. It is the goal of the integrators of CAD and automated testing both to automate test-vector generation and to provide a means of ensuring as close to 100% fault coverage as possible for VLSI.

To overcome uncertainty in the testing of VLSI parts, test-pattern generation based on logic-model coding is potentially the best solution. In this approach, all internal nodal faults are simulated, and functional exercises are developed to propagate such faults to output pins where they can be detected. The basic drawback to this approach is the accuracy of the simulation and of the models needed.

Researchers and designers of VLSI circuits have had to face much the same problems in coming up with the software and systems that they are using. Consequently, current VLSI CAD techniques may provide some insight into automated-testing techniques.

## Today's CAD

In principle, the operation of a semiconductor circuit of any size may be simulated through the integration of the differential equations that govern diffusion and drift of carriers. However, for a large computer to, in effect, analyze itself at this level would probably take more time than the useful life of the machine.

The method used in practice is a graduated approach, in which detailed simulations are performed on small chip sections, then followed by more general simulations—faster and less accurate—from the physical to the logic level. This design effort requires tools that enable the process engineer and the device physicist to predict impurity profiles, physical parameters, and electrical parameters before the device is fabricated. To aid in the simulation of the system, a variety of process, device, circuit, and timing software packages are available to the designer (see Table 1 on p. 131).

To use such tools, the process engineer first makes an educated guess as to the nature of the process that will be used to fabricate the final device. He or she then creates a file of commands for a program like Suprem, which describe the series of diffusions and implantations. Suprem is one of the easiest programs to learn and to use because its input syntax is straightforward and its grammar proceeds according to common-sense rules.

Suprem generates an output file, which can be plotted as a graph of the concentration of different impurity atoms in silicon as a function of depth from the surface. Theoretically, the entire behavior of the device is determined by its concentration profile. The program generates this file in seconds, whereas actual fabrication of the wafer takes several weeks.

The device physicist then uses the concentration profile and a device-simulation code to determine the behavior of a particular device under certain conditions. The physicist wants answers to such questions as the voltage at which a breakdown occurs between the source and drain regions of an MOS gate and the collector current level at which rolloff of the transistor beta is detectable.

The first type of question can be answered using Minimos, one of the few two-dimensional programs. It solves both the current-continuity equation and Poisson's equation by using sophisticated numerical techniques for handling partial differential equations. The second type of question may be answered using Sedan, a one-dimensional Poisson solver.

In the design of a series of devices, the designer is like an architect with a reliable supply of bricks; he is ready to plan the building. The designer gets the bricks by setting up a collection of logic gates, such as OR and AND gates, registers, flip-flops, programmable logic arrays, memory cells, and arithmetic and logic units. From these, the designer must construct a network or circuit to implement a specific logic function.

Circuit-simulation programs do this essentially by reducing the equations that embody Kirchoff's law into a linear matrix equation. Spice is one of the most widely used programs to accomplish this, and it includes a number of built-in models for different kinds of semiconductor devices, including MOS, complementary-MOS, TTL, and junction field-effect–transistor devices. These models are called distributed-network models because an electrical network is used to approximate the partial differential equations that more precisely describe the behavior of the device.

Circuit simulators are able to look at the individual gates in much more detail than logic simulators, but they also consume more time and memory than the latter. On the other hand, logic simulators tend typically to oversimplify the problem of timing and race conditions.

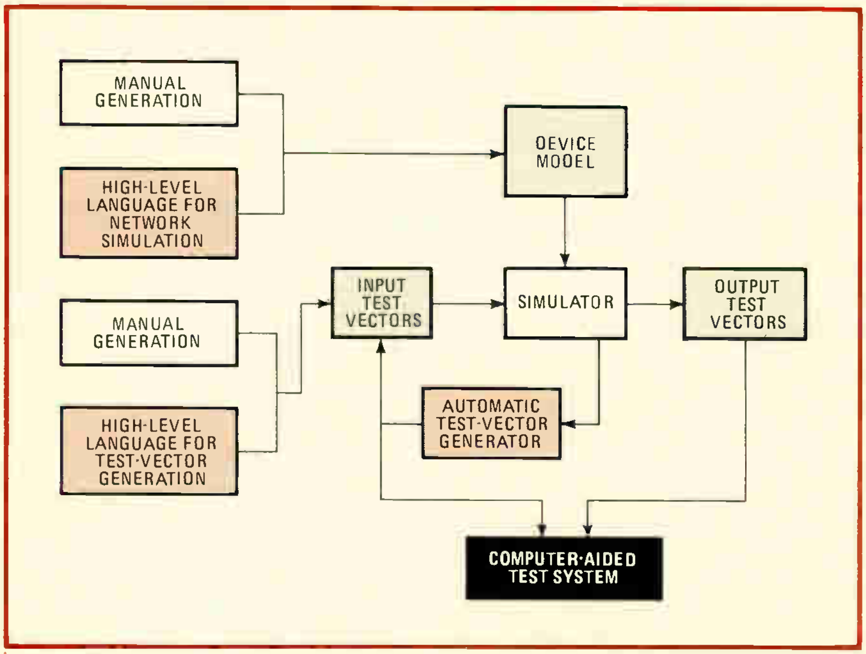
The basic function of a logic simulator is to imitate the behavior of a circuit whose various physical parameters (device, circuit, and timing) have been described to it. That is, given a sequence of input signals to the circuit, it predicts what the output signals should be. In addition, the logic simulator provides the means of inspecting logic values on internal components in the circuit. A design is considered verified if the circuit behavior predicted by the simulator agrees with the original design intent.

The function of a timing simulator is to help bridge the gap between circuit simulators and logic simulators. In Splice, the designer uses circuit, timing, and logic simulation at the same time within the same design. This mixed-mode approach is most effective when the designer needs to model a large circuit.

### Forcing faults

In fault simulation, the true-value behavior of a circuit and the behavior of each possible faulty circuit are simulated. This type of simulation is carried out to grade a test or determine the set of faults detected, to determine a fault not detected and tested, and to construct a fault dictionary.

Typically, faults that are modeled are the set of all possible single stuck-at faults in the circuit. If the response of the simulated circuit changes when some fault is being simulated, then the test is said to detect that fault. The fault simulator tells the user automati-




**1. Integrated test.** The goal of much CAD effort is a system like that at left, in which test generation is an integral part of the design process. The colored areas have yet to be fully developed, while the other elements must be improved to meet the goal.

cally which faults have or have not been detected by the test sequence, without actually having to insert the faults into a prototype circuit.

Three kinds of fault simulation are used: deductive, parallel, and concurrent. In deductive simulation an unfaulted, or true-value, simulation is performed, and faulty behavior deduced from the results. Fault lists associated with each circuit element record the faults that would cause the element's output to differ from the true value. Each time an element's input changes, its true value is determined and then its fault list is updated.

In the parallel approach, several faulty circuits are modeled along with the single correct one. The logic value at each node is represented both by 1 or 2 bits; a single byte is used to represent both a good circuit and several faulty ones. In this way, good signals and faulty ones propagate through the circuit in parallel.

In concurrent simulation, the newest of the techniques, good and faulty circuits are simulated at the same time by creating multiple copies of circuit elements. A circuit element is copied and simulated if some fault makes its output differ from a good circuit. The processing is similar to deductive simulation, since it works with lists attached to circuit elements.

For small circuits, run times for concurrent simulation are faster than for other methods, but storage requirements are higher. However, for very large circuits, a concurrent simulation would require much paging to and from disk storage, thus eliminating its speed advantage. At present, therefore, the parallel approach is considered the most effective one.

Fairlog, a four-part logic and fault simulator developed by Fairchild, is an example of the parallel approach. It consists of Fairnet, a network-description preprocessor; Faircom, a simulation control language; Fairlog, the logic simulator; and Fairflt, the fault simulator. Fairnet expands network macrodefinitions and produces a network interconnection list for Fairlog. Fairlog runs the simulations under the control of commands compiled by Faircom and this netlist.

Using Fairlog, a simulation can be carried out in one of two modes, either the four- or eight-state mode. The four-state mode uses four stable states: logic-0, logic-1, high-impedance, and undefined. To these, the eight-state mode adds four transient states: upward-transition, downward-transition, transition-to-high-impedance, and transient-undefined.

The simulator also generates an applied-states analysis to determine the controlability of the network and an upper boundary on the test coverage of the input sequence. Fairflt determines the precise test coverage or fault grading with this analysis.

### Fairnet input

Fairnet processes an input file that is a macrocell description of the electrical network proposed for circuits based on gate arrays. After the circuit has been placed, routed, and checked by Fairnet, it is resimulated by a separate section of Fairlog with the delays, resistances, and capacitances calculated from the actual geometries. Resimulation provides a much more accurate model of the chip than was possible before layout and thus saves time by avoiding delays caused by the discovery of problems during the actual fabrication process.

Fairnet's input file can be coded by a programmer from the chip's logic diagram. It also can be automatically generated by other means—for example, by an interactive schematics drawing system. Each line of Fairnet code represents a cell with uniquely named inputs and outputs. Each output is named as an input to another cell or an external pin; therefore, the program reading the code can connect the individual cells described to form the complete network.

The logic-simulation module, Fairlog, has built-in log-

**TABLE 1: DEVICE MODELING AND SIMULATION SOFTWARE**

| Program name | Technologies handled | Function | Input required | Output produced |
|---|---|---|---|---|
| Suprem | MOS, TTL, ECL, $I^3L$ | process modeling | process runsheet for particular process | impurity profile distribution |
| Minimos | MOS | process and device simulation | Suprem profile data | physical, electrical, and timing behavior of the device |
| Sedan | MOS, TTL, ECL, $I^3L$ | device modeling | impurity profile distribution from Suprem | physical, electrical, and timing behavior of the device |
| Spice | MOS, TTL, ECL, $I^3L$ | electrical network simulation | electrical network description of circuit | electrical and timing behavior of circuit |
| Simple | bipolar — primarily $I^3L$ | device modeling and network simulation | transistor test measurements and layout description | electrical and timing behavior of circuit |
| Splice | MOS | network and logic simulation | description of logic network and electrical circuitry | logic verification with electrical and timing information |

ic-gate definitions for the operations of AND, OR, NAND, NOR, exclusive-OR, inversion, wired-OR, transmission gates buffers, and multiplexers. The chip description can be made with these primitives, or with user-defined primitives, library logic models, or user-defined logic and functional models.

A complete system-design tool, Fairlog extends from functional definition to gate-level simulation for all gate-array and custom technologies. Ultimately it will provide up to 256 levels of logic, more than enough for any conceivable future application.

To perform fault simulation and grading, and to aid in test sequence generation, Fairflt uses four basic analyses: controllability-observability, applied-states, gate-activity, and fault-insertion. In controllability-observability analysis, the distances from a circuit's input or output to the individual gates that make up that circuit are measured. Thus the analysis is a measure of testability—an index of how difficult it is to toggle internal nodes with stimuli applied at the primary inputs and of how difficult it is to transmit or observe those changes on the primary outputs.

Applied-states analysis gives information about the actual states applied, the percentage of faults potentially detectable from running a given test sequence, and the faults that cannot be detected by the input sequence. To illustrate the principle of applied-states analysis, there is the simple case of a three-input AND gate. Table 2 (below) shows the eight possible input states and the normal and the faulty responses.

The first case is where the gate is stuck at 1. If input state 7 is applied, no difference in response between the normal and faulty gate would be noted. The output would be 1 in either case. The application of any other state, on the other hand, would cause there to be a difference in response.

In a similar way, the condition of the gate input A at 1 can only be detected if state 6 is applied. Application of the proper input state is a necessary condition to the ability to detect a given fault in a gate. In this instance, application of only half the possible states, 4 through 7, is sufficient to find all of the possible stuck-at faults.

Gate-activity analysis counts the number of times a gate output changes state. The designer can then find how effective the input test vectors are in exercising parts of a circuit and can modify the test strategy to include more activity in those areas where needed.

Fault-insertion analysis consists of faulting a given gate during a test sequence to see if the fault causes an incorrect signal that changes the device response. If different responses are noted between faulted and unfaulted networks, the faults are deemed detectable.

From the faults that are potentially detectable as determined by the applied-states analysis, the user can specify which ones he desires to simulate. Fairflt will give the grading of the input test sequence with respect to the potentially detectable faults.

These current CAD techniques need to be enhanced to cope with the requirements of the next generation of VLSI devices. These enhancements will make it possible to integrate the CAD and automated-testing functions to a much greater degree. The enhancements that are needed include:

- More powerful automatic test-vector–generation algorithms that speedily and efficiently aid in the simulation of circuit models.
- High-level test-vector–generation languages that are easier to use and that are more powerful than the assembly-level languages and manual techniques now used to generate test sequences for CAD simulations and in automated-testing systems.
- System-level languages that provide the designer with a set of powerful commands to allow circuits to be modeled, simulated, and routed quickly.
- An integrated data base that will serve for CAD and automated testing.

Fundamental to the operation of CAD simulators and to the quick and efficient generation of test vectors is the development of algorithms capable of dealing with VLSI circuits. The whole area of automatic test-vector generation has been investigated extensively in the past, but difficulties arise when the number of gates on a chip

**TABLE 2: NORMAL AND FAULT RESPONSES FOR A THREE-INPUT AND GATE**

| State No. | Inputs | | | Normal response | Fault response | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Gate stuck at: | | Input stuck at 1 | | |
| | A | B | C | | 1 | 0 | A | B | C |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 4 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 7 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

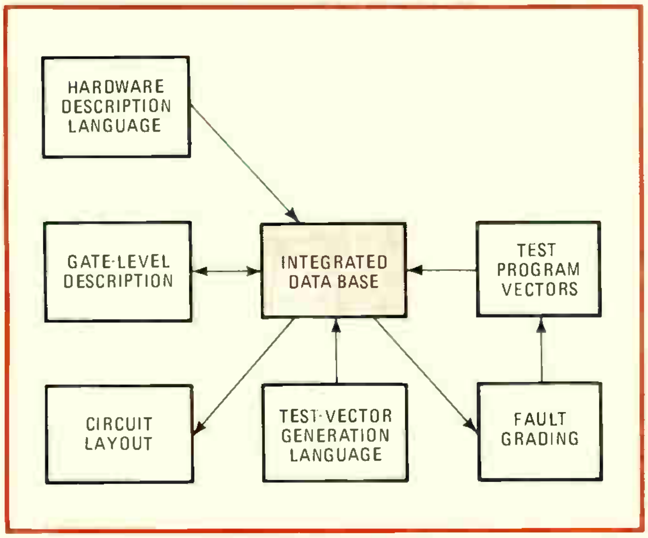
increases, thereby increasing the number of potential failures and complicating the problem.

Highly structured and testable chip designs are essential as circuits get larger. Software tools can then be developed to take advantage of the methodologies employed in the process of designing for testability. While these software tools are still in design, certain attributes can at this point be described.

The tools will be easy for the user to learn and employ and will produce programs for a variety of testers, along with the ac- and dc-parameter descriptions needed for a full device test. Test-program generation will be controllable in accordance with the layout and technology used to fabricate a design; failures peculiar to a particular technology can be added to the fault dictionary.

The software will be able to estimate and indicate graphically the fault coverage, test-pattern length, and test-execution time, along with the confidence bounds of the test before and after actual test runs. Other attributes of the software will be the ability to recognize scan-in/out registers for improved testability and, optionally, to grade nodes according to their contribution to fault isolation for wafer-probe testing. Also, the programs will be able to control fault-isolation resolution and optimization levels, to let the user define failure modes with gate- or function-level descriptions, and to accept suggested test patterns from the user.

It also should be able to select test-pattern–generation strategies and perform automatic switching between them (for example, for the first 50% of the failures use a random pattern generator, and thereafter a nine-valued algorithm). Another possibility is the production of test programs that can collect data for generating product profile analysis, for test-pattern–generation feedback, and for effect-cause analysis when test-pattern inadequacy is observed.




**2. Software structure.** The software elements of a computer-aided design and test system will provide inputs to and receive them from an integrated data base. Such a data base will appear as a single entity to system users, although it may be physically distributed.

With high-level languages, a similar situation exists at both the simulation and test stages. The enormous demands of VLSI make present approaches no longer suitable and require the development of high-level test-vector–generation languages that allow the user to generate test-vector inputs in groups of functions rather than one at a time. Present languages are cumbersome and not suited for large circuits.

Considering VLSI requirements, such languages should be based on an easy-to-use and solidly structured language, such as Pascal, that will permit easy generation of hundreds of thousands of vectors, each of which can be several hundred bits in length. It should also be capable of being compiled into a form useful on either a logic simulator or automatic test equipment.

### Language needed

The design and fabrication of VLSI circuits also requires some sort of high-level language for describing hardware. The language should make it possible to describe complex circuits speedily and to reduce these designs automatically to silicon.

A first step in this direction is Fairsys, a high-level simulation language that assists in the design of a chip from the top down, from design specifications down to a level short of logic, timing, and fault simulation. Registers, memories, buses, inputs, and outputs are described in a manner similar to the declaration of variables in programming languages such as Pascal.

These system elements are combined and manipulated through the use of connection statements and register-transfer statements, which are roughly analogous to the assignment statement found in most programming languages. Like the assignment statement, the right-hand side of connection and register-transfer statements is an expression that combines basic elements using a set of operators such as AND, OR, exclusive-OR, or negation. These operators may be applied to individual bits or to vectors of bits (a register) or of signals (a bus).

Integrating CAD and automated testing by tying together all the key elements in the two environments with a common data base will solve two of the major disadvantages of the logical-model coding approach to device testing: that is, getting data to the tester, and no real-time interaction when the device designer wants to change pattern or instruction sequences quickly in order to analyze the devices.

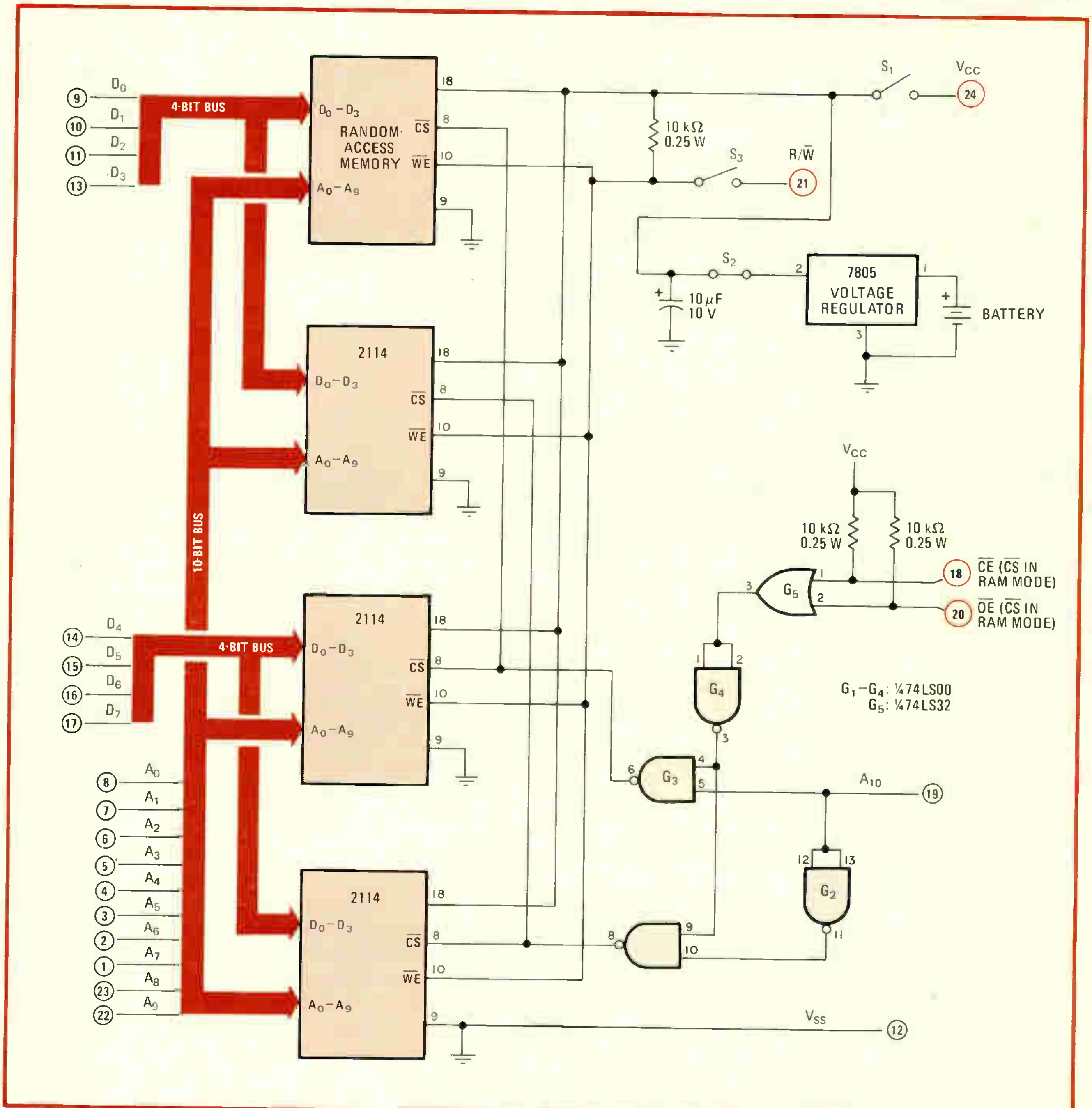
Figure 2 shows how such an integrated data base may be organized. Such a data base is a software system of information storage and retrieval whereby information is accessible to all programs in the system. It would be characterized by a standardized terminology that is common to most of the system's languages and programs. □

## Random-access memories form E-PROM emulator

by David J. Kramer
*Sunnyvale, Calif.*

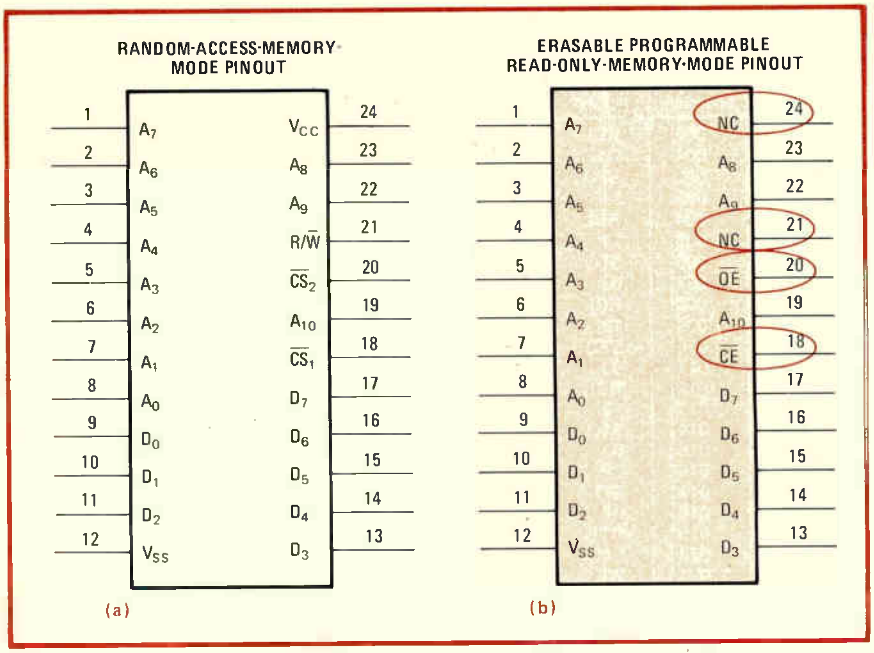
Many low-cost microprocessor kits that are used as educational tools possess a relatively small amount of on-board random-access memory and are incapable of transferring programs to erasable programmable read-only memories. This E-PROM emulator overcomes both of these limitations.

Four 2114 RAMs are connected in a 2-K-by-8-bit configuration (Fig. 1). To emulate an E-PROM, this memory




**1. Emulator.** Four 2114 RAMs are wired on a separate board to simulate a 2-K-by-8-bit E-PROM. Using switches $S_1$ and $S_2$, power supply $V_{CC}$ for the emulator can be taken either from a trainer's kit or a battery. Numbers within circles denote pinouts for the 24-pin DIP.

**2. Package.** The pinouts of the emulator in both its modes—random-access memory and erasable programmable read-only memory—are as shown in (a) and (b). The only differences are in pins 18, 20, 21, and 24—in the E-PROM mode, pins 18 and 20 function as chip and output enable.




circuit is built on a separate board and has its leads terminating in a 24-pin dual in-line package. The power supply for the emulator is either from the microprocessor training kit ($V_{cc}$) or a battery and is coupled to the emulator by using switches $S_1$ or $S_2$. The $\overline{WE}$ line may be disconnected from the plug with $S_3$.

To function as an emulator, the 24-pin DIP must be connected to the appropriate address-decoding circuitry in the trainer. The memory is then plugged in and either $S_1$ or $S_2$ is closed (depending on the selected power supply). This puts the circuit in its RAM mode (Fig. 2a). In this mode, pins 18 and 20 function as chip-select controls. Pin 21 is the read-write input.

Once the data to be preserved is in the RAM, the battery should be (if not already) connected to the 7805 voltage regulator, and $S_2$ closed and then $S_1$ and $S_3$ opened. The circuit is now in its E-PROM mode (Fig.2b) and may be inserted in the master socket of any programmer that will handle a 2716 E-PROM.

The emulator will remain to be powered while the programming occurs. The type of keep-alive battery needed depends on the power requirements of the 2114 RAMs and the length of time the emulator is to remain in the E-PROM mode. □

## Calculator notes

# TI-59's reverse-Polish routine simplifies complex arithmetic


by John Bunk
*University of Pittsburgh, Johnstown, Pa.*


Solving complex arithmetic equations by hand is both tedious and subject to errors. However, by using a system of reverse-Polish notation (RPN) similar to that used in the Hewlett-Packard series of calculators, this Texas Instruments-59 program performs this task easily. A six-register stack stores intermediate results automatically, and equations can therefore be solved with a minimum of keystrokes. The real and imaginary components of the equation are displayed separately.

The 224 step program is a collection of simple subroutines that are joined to perform the complex mathematical calculations. The subroutines, which perform all the mathematical operations required for the calculations, are the addition, subtraction, multiplication, division, exponentiation, and inverse functions. The functions corresponding to their subroutine names are listed in the table.

Calculators using the RPN system require a specific memory-stack structure. Each stack register occupies two data registers that store the real and imaginary parts of any input number. The arithmetic is solved with the aid of both the A and Z registers, which contain the data that is keyed into the stack by means of the SBR =

**TI-59's OPERATIONAL ROUTINES FOR COMPLEX MATH**

| Subroutine | Function |
|---|---|
| SBR + | A + Z |
| SBR − | A − Z |
| SBR × | A × Z |
| SBR ÷ | A ÷ Z |
| SBR $Y^X$ | $A^Z$ |
| SBR = | enter display/t-register into stack |
| SBR CLR | clear stack |
| SBR lnx | $e^Z$ |
| SBR 1/X | 1/Z |

## TI-59 PRINTER LISTING: SIMPLIFYING COMPLEX MATH USING REVERSE-POLISH NOTATION

| Location | Key | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 | RCL | 044 | EXC | 089 | X ⇌ T | 134 | + | 179 | 20 |
| 001 | 20 | 045 | 26 | 090 | RCL | 135 | SBR | 180 | RTN |
| 002 | STO | 046 | EXC | 091 | 19 | 136 | 00 | 181 | LBL |
| 003 | 01 | 047 | 24 | 092 | RTN | 137 | 00 | 182 | $Y^X$ |
| 004 | RCL | 048 | EXC | 093 | LBL | 138 | PGM | 183 | SBR |
| 005 | 21 | 049 | 22 | 094 | CLR | 139 | 04 | 184 | 00 |
| 006 | STO | 050 | EXC | 095 | 1 | 140 | B | 185 | 00 |
| 007 | 02 | 051 | 20 | 096 | 9 | 141 | SBR | 186 | PGM |
| 008 | RCL | 052 | STO | 097 | STO | 142 | 00 | 187 | 04 |
| 009 | 18 | 053 | 18 | 098 | 18 | 143 | 20 | 188 | E′ |
| 010 | STO | 054 | X ⇌ T | 099 | 0 | 144 | RTN | 189 | PGM |
| 011 | 03 | 055 | RTN | 100 | ST* | 145 | LBL | 190 | 04 |
| 012 | RCL | 056 | LBL | 101 | 18 | 146 | − | 191 | D |
| 013 | 19 | 057 | = | 102 | RCL | 147 | SBR | 192 | SBR |
| 014 | STO | 058 | EXC | 103 | 18 | 148 | 00 | 193 | 00 |
| 015 | 04 | 059 | 19 | 104 | X ⇌ T | 149 | 00 | 194 | 20 |
| 016 | CP | 060 | EXC | 105 | 2 | 150 | PGM | 195 | RTN |
| 017 | STF | 061 | 21 | 106 | 9 | 151 | 04 | 196 | LBL |
| 018 | 01 | 062 | EXC | 107 | EQ | 152 | B′ | 197 | LNX |
| 019 | RTN | 063 | 23 | 108 | 01 | 153 | SBR | 198 | SBR |
| 020 | STO | 064 | EXC | 109 | 16 | 154 | 00 | 199 | 01 |
| 021 | 20 | 065 | 25 | 110 | 1 | 155 | 20 | 200 | 20 |
| 022 | X ⇌ T | 066 | EXC | 111 | SUM | 156 | RTN | 201 | PGM |
| 023 | STO | 067 | 27 | 112 | 18 | 157 | LBL | 202 | 05 |
| 024 | 21 | 068 | STO | 113 | GTO | 158 | × | 203 | B′ |
| 025 | NOP | 069 | 29 | 114 | 00 | 159 | SBR | 204 | STO |
| 026 | NOP | 070 | NOP | 115 | 99 | 160 | 00 | 205 | 18 |
| 027 | RCL | 071 | NOP | 116 | 0 | 161 | 00 | 206 | X ⇌ T |
| 028 | 29 | 072 | X ⇌ T | 117 | STO | 162 | PGM | 207 | STO |
| 029 | EXC | 073 | EXC | 118 | 18 | 163 | 04 | 208 | 19 |
| 030 | 27 | 074 | 18 | 119 | RTN | 164 | C | 209 | RTN |
| 031 | EXC | 075 | EXC | 120 | RCL | 165 | SBR | 210 | LBL |
| 032 | 25 | 076 | 20 | 121 | 19 | 166 | 00 | 211 | 1/X |
| 033 | EXC | 077 | EXC | 122 | STO | 167 | 20 | 212 | SBR |
| 034 | 23 | 078 | 22 | 123 | 02 | 168 | RTN | 213 | 01 |
| 035 | EXC | 079 | EXC | 124 | X ⇌ T | 169 | LBL | 214 | 20 |
| 036 | 21 | 080 | 24 | 125 | RCL | 170 | ÷ | 215 | PGM |
| 037 | STO | 081 | EXC | 126 | 18 | 171 | SBR | 216 | 05 |
| 038 | 19 | 082 | 26 | 127 | STO | 172 | 00 | 217 | E |
| 039 | X ⇌ T | 083 | STO | 128 | 01 | 173 | 00 | 218 | STO |
| 040 | NOP | 084 | 28 | 129 | STF | 174 | PGM | 219 | 18 |
| 041 | NOP | 085 | NOP | 130 | 01 | 175 | 04 | 220 | X ⇌ T |
| 042 | RCL | 086 | NOP | 131 | CP | 176 | C′ | 221 | STO |
| 043 | 28 | 087 | RCL | 132 | RTN | 177 | SBR | 222 | 19 |
| | | 088 | 18 | 133 | LBL | 178 | 00 | 223 | RTN |

### Instructions

- Key in program
- Given the algebraic expression, key in the variables corresponding to their real and imaginary magnitudes and their mathematical operations

  Place all real quantities in the t register

  Enter all imaginary quantities into the stack by means of the SBR = function

  If multiplication or division of two terms is necessary, press SBR × or SBR ÷ keys after entering the last term

  If addition or subtraction is desired, press the SBR + or SBR − keys after entering the last term

  If quantities must be multiplied exponentially, press either the $y^x$ or lnx key, depending on the application

  If the inverse of an algebraic quantity is required, press the 1/x key

  Stack may be cleared by pressing the SBR CLR keys

- Imaginary quantities that result from a given algebraic operation will be displayed directly. Real quantities may be recovered from the t register (press the x ⇌ t key)

operation. After the data is entered, the complex equation is solved by pressing the appropriate function keys. In this program all stack entering is manual.

As an example of the program's usefulness, consider $x+jy = (2+j2)(3+j5)-(9-j15)+(1.4+j3)$. The solution to this equation may be found by entering: 2, x ⇌ t, 2, SBR =, 3, x ⇌ t, 5, SBR =, SBR ×, 9, x ⇌ t, 15, ±, SBR =, SBR −, 1.4, x ⇌ t, 3, SBR =, SBR +. The imaginary part of the result, y = 34, appears on the display. The real part of the result, x = −11.6, may be found by pressing the x ⇌ t key. □

# Engineer's newsletter

**Glossary lifts veil on pc terminology**

Aspect ratio, B-stage material, electroless deposition, vias—these are just a few of the terms used throughout the printed-circuit–board industry that are foreign to the great majority of electronics engineers. However, as packaging goes from an inexact technique to a true technology, **all EEs need to have a firm understanding of pc-board technology.** An aid to this goal is a free 16-page glossary recently published by National Technology Corp., 1801 Newport Circle, Santa Ana, Calif. 92705. It contains 158 frequently encountered pc-board terms and their meanings and should be a good reference for the design engineer.

**Dc biasing methods help measurement of in-circuit inductance**

To measure in-circuit inductance correctly, it is necessary to have dc biasing, making sure to avoid the unwanted impedance of the test fixture that will contribute to erroneous readings. A recent short article by Dale Mack in the summer issue of Electro & Scientific Industries' newsletter, "Bridge," **describes both voltage- and current-source techniques for dc biasing of inductors.** The voltage-source method uses a dc voltage source, a resistor, and bypass capacitors to remove unwanted impedances like those of the source and ammeter. The more sophisticated current-source technique uses an external voltage source, a three-transistor current mirror for a high-impedance current source, and a solid-state surge protector to suppress inductive-current surges. For more details on these methods, write Electro & Scientific Industries Inc., 13900 NW Science Park Drive, Portland, Ore. 97229.

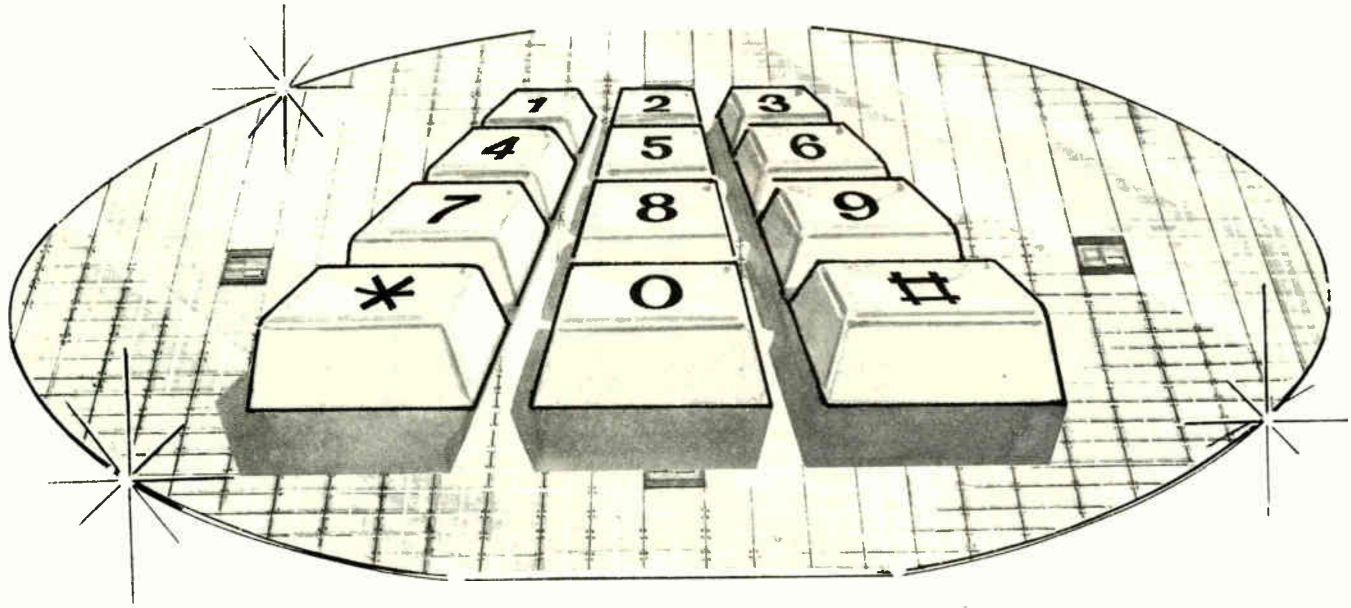
**IC maker finds tape bonding reliable**

Is tape automated bonding a reliable method of bonding? A recent National Semiconductor Corp. study based on 2½ years' integrated-circuit production and 450 million plastic dual in-line packages disclosed an exceptional performance rate. Only eight customer complaints on a total of 99 parts were received. Tests showed 72 of the 99 to be good, and **in the case of the 27 bad DIP circuits, none had malfunctioned because of lead or bond failures.** All of the 450 million circuits were produced using 3M beam tape for bonding of the ICs to the DIP lead frames. National committed itself to beam-tape assembly in the mid-1970s, adopting 3M's two-layer tape in an automated bonding process for IC interconnection. Supplied in an 11-mm-wide, sprocketed format, the tape is composed of 1-oz rolled annealed copper foil and 0.5-mil cast polyimide film.

**Bulletin lists more modifications to Casiotone musicmakers**

Robin Whittle of 42 Yeneda St., North Balwyn, Melbourne, Australia 3104, has come up with yet an other group of circuitry modifications for Casio's electronic music instruments [*Electronics*, June 16, p. 192]. **These include: modifications to the M-10's digital-to-analog converter to reduce quantization noise; suggestions for improving the new CT-202 keyboard;** coupling two instruments together as master and slave; and interfacing with computers. These, and other modifications, and much descriptive material about the Casio family of keyboard instruments are in Whittle's technical bulletin, which can be obtained by sending the author $6 in U.S. currency.

**-Jerry Lyman**




# TELEPHONE KEYPAD LOGIC THAT'S VERSATILE BUT MEAN

A whole family of pulse dialler and DTMF circuits in fact, that combine outstanding performance with exceptionally low power dissipation.

The pulse diallers (MV4320 – MV4326) have all the logic for loop-disconnect push-button telephones.

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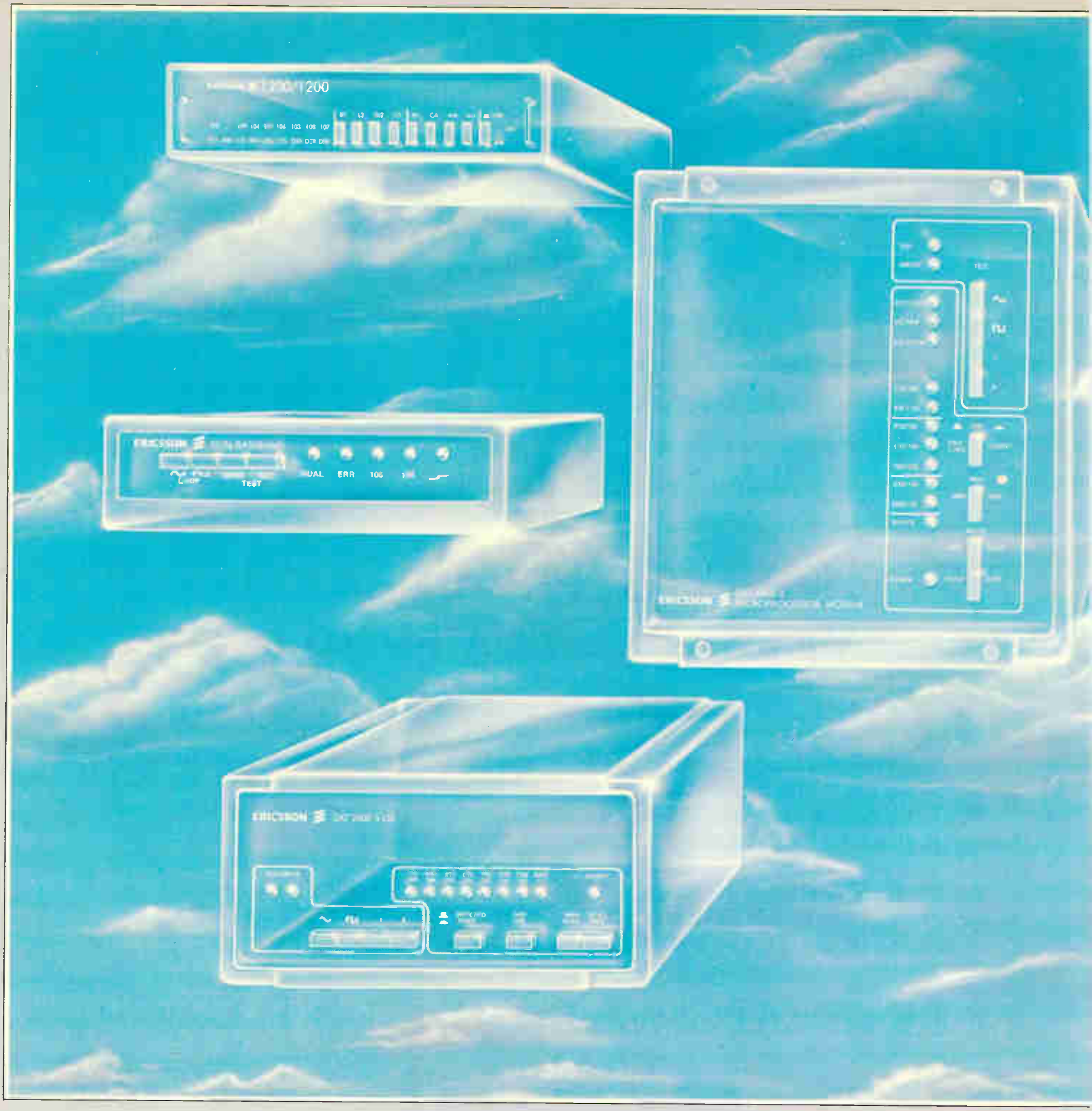
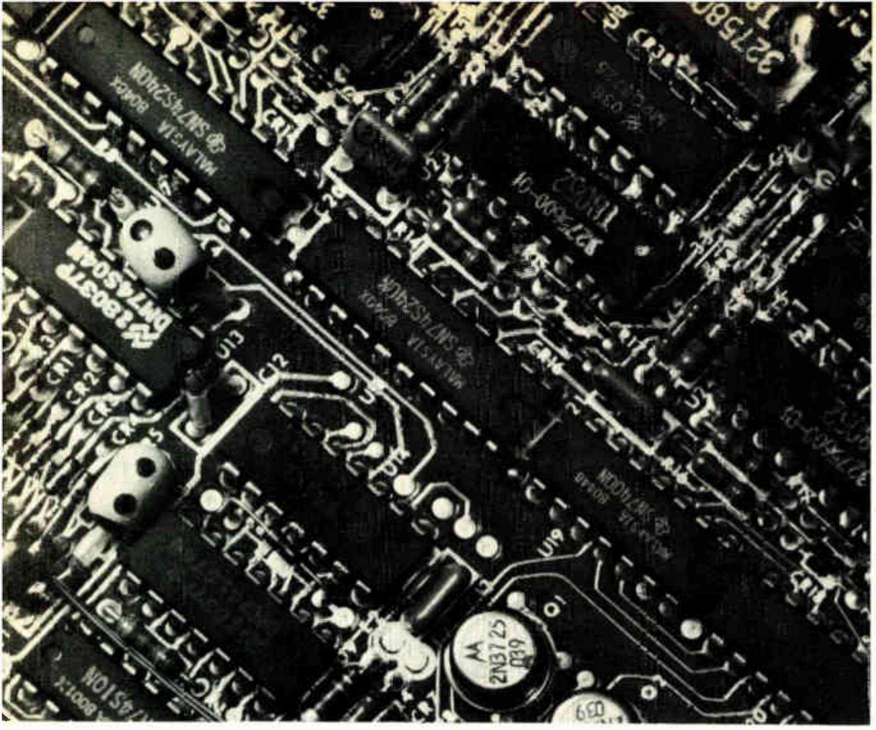
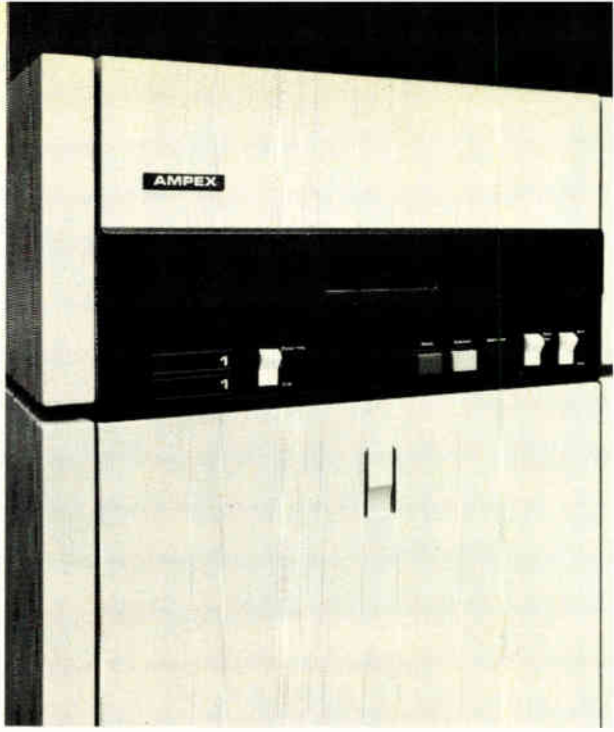



# 7 reasons why ERICSSON is the coming name in modems.



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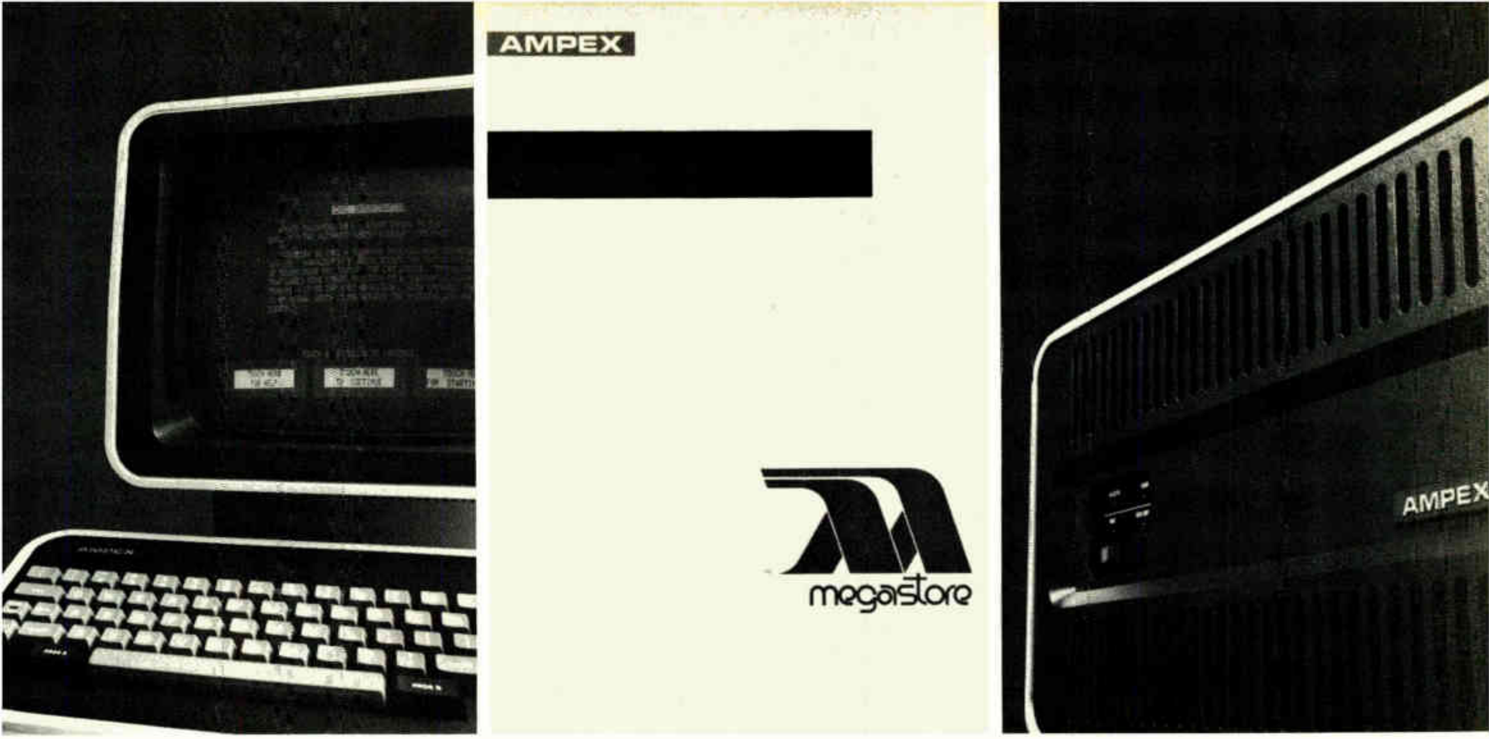
Responsiveness to designer demands has also brought about many innovative product improvements. Not just in core memory where Ampex is the recognized world leader, but also in new technologies like the Megastore® Memory data storage device, our all-electronic peripheral alternative to rotating memories. We've introduced new product concepts, too, in non-memory devices such as our touch-operated video display terminal, TouchTerm™ 80. The proof of this continuing emphasis on meeting designer needs is a full line of high-performance core and semiconductor memory systems, disk drives, disk and drum replacement devices, video display terminals and minicomputers.




**Memory.** The UNIBIT™ temperature-independent ferrite core is only one of many significant product improvements generated by Ampex in memory technology. Other products include: Megastore® Memory solid-state peripheral memories for DEC, Data General and Honeywell CPU's; Multibus-compatible memory modules; add-in core memories; semiconductor MOS RAM modules; and DEC System 10, 20 and 1170-compatible main memories.

**Disks.** Ampex manufactures a full line of disk drives in round and flat ribbon cable SMD interfaces. Our Winchester technology includes our "Superwinchester" series of 32, 64 and 96 megabyte systems, with 16 megabytes of removable media. Our Capricorn 14" Winchester disk drives come in 165 or 330 megabyte formats, with SMD interface compatibility, and our 8" drives offer 48 or 80 megabyte capacities. We also offer the designer disk storage modules in rack or free-standing formats, as well as DEC or Data General-compatible disk controllers.

**Tape.** Our design expertise in the field of tape drives has produced our Streamer-Type Magnetic Tape Transport (TMS), which can be mounted vertically or horizontally, with unmatched MTBF and 1600 BPI density. We also offer tension arm and vacuum column tape drives with either 7 or 9 track heads, all with standard P-type interface, common electronics and embedded formatter.

**Terminals.** The newest addition to our terminal family, the TouchTerm 80 video display unit provides fast and accurate interaction with most computers by simply touching the screen. A gloved workman in a production environment, or an executive in his office can both operate the terminal with the same benefits such as fully buffered memory, self-diagnostics, and selectable baud rate found in our D80 series.
We also offer the OEM market our D30 terminal for basic data communications applications.

**Computers.** Ampex, in addition to its peripheral devices, also offers the OEM market a single processor board CPU in two versions: complete minicomputers with controllers, terminals, and memory capacity from 128 to 256K bytes, and OEM versions, designed to help systems integrators in building specially-tailored computer systems for business and industry.

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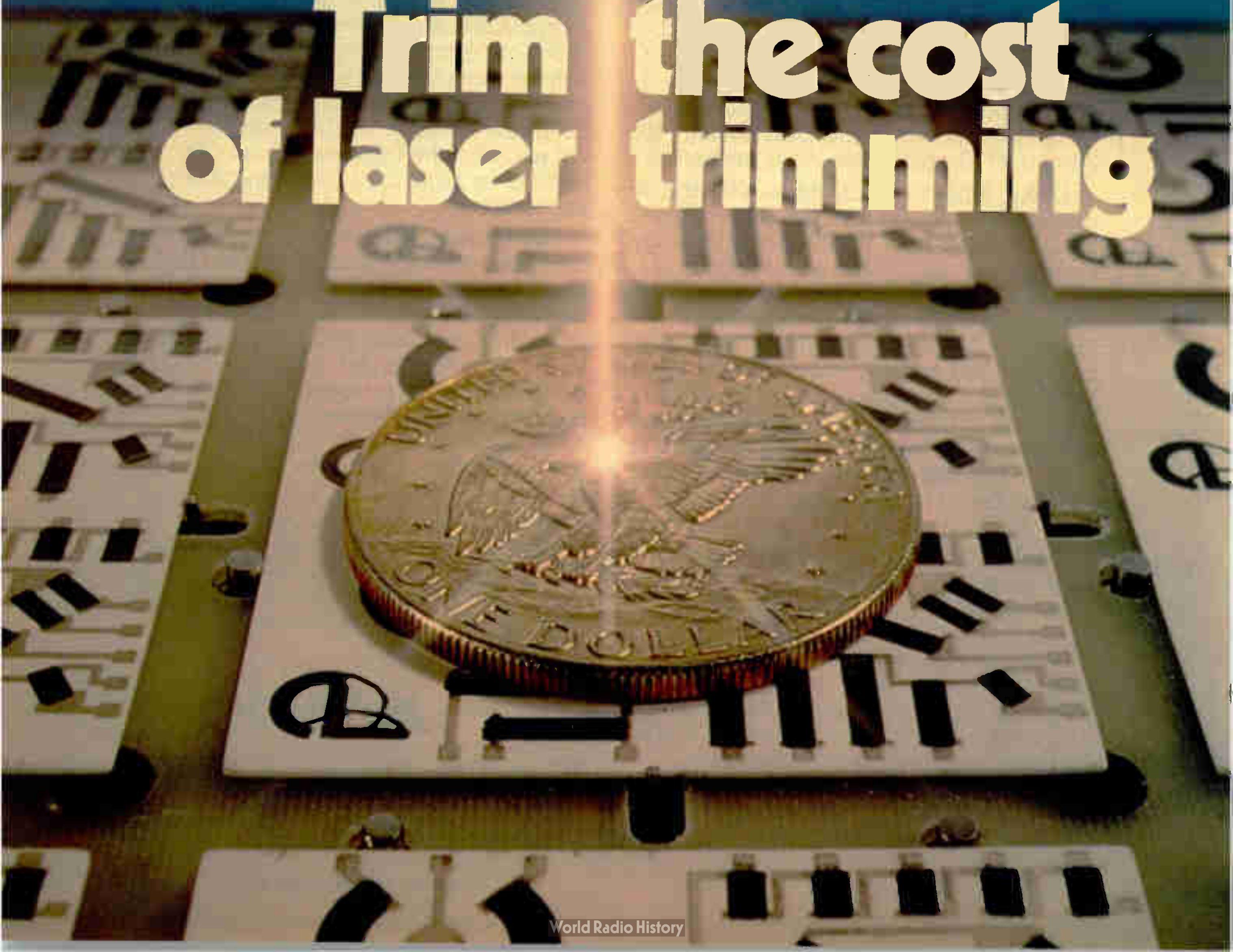

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# Productivity: Driving Force for the 1980s


This special advertising section on production equipment was paid for by the advertisers in it and was written by freelance journalist John Joss.

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# BETTER PRODUCTIVITY IS KEY TO INDUSTRIAL SURVIVAL

## As a New World Order Emerges, High Technology Takes Center Stage, With the Electronics Industries Clearly in the Spotlight

A new world of industrial power is in the making, with hundred billion dollar markets at stake. The competition primarily concerns high-technology industries, and companies around the world are recognizing that the difference between growth and extinction lies in the leverage they may gain from productivity improvement.

The electronics industries are crucial to this struggle. Not only are they the leading edge in high technology, but they provide many of the tools that other industries need to optimize factory and office productivity.

Automation and robotics will assume an increasing share of the burden. Designing, implementing, and testing products and production processes for highest quality and reliability will be essential. At the bottom line, however, productivity is emerging as the test of corporate success or failure for the high-technology industries and their burgeoning customer base.

With so widespread an interest in productivity, it is not surprising that the term embraces a multitude of activities. Productivity is a computer-aided design system that cuts months and millions from product design and development. It is a testing strategy that slashes defects and rework. It is new office automation, including data and word processing and networking. It is automation via robotics and computer-aided manufacturing. It is factory data management and gathering. It is radical approaches to software.

**Advanced electronics paves the way for two-member flight crews in the Boeing 757/67, vs. three crew members in earlier commercial craft.**

*John Joss, author of this special advertising section of productivity, has written and edited numerous articles and books on a wide range of scientific and technological subjects. He also has covered these subjects for many radio and TV features.*

### No Place to Hide

Top managements in every sector of the electronics industries are unanimous in saying that productivity or its lack will make or break their companies in the 1980s. In fact, the semiconductor industry is swiftly becoming the pivot on which world industry hinges, with silicon its fundamental deflation engine.

Very large-scale integrated circuits designed by CAD systems form the next generation of computers, a wide range of CAD/CAM tools, and communications systems that work harder at lower cost. Those same systems help aggressive multinational firms to create more competitive products and services of every kind.

One high-visibility example is the new generation of avionics in jetliner cockpits, which are safe and efficient with two, not three, crew members. Made possible by advanced electronics, this productivity improvement is holding down airline costs in the competitive international transportation industry to the benefit of travelers and air-freight users.

Productivity—basically higher yields of increasingly complex VLSI circuitry of higher quality and lower cost—is the semiconductor industry's driving force. Its products are the only world

commodity, producing higher performance at lower cost. Economists see it as the best deflation game in the industrial world.

The potential improvements in productivity are enormous, as two advances from Canon and Siltec suggest. "Automated handling and alignment is coming—over 70% of our contact/proximity aligners include it," says Brian Allsop, national sales manager for Canon USA. "We use a laser to scan the mask and wafer through a microscope, and we've adapted it to the mirror-projection aligner and wafer stepper. We also provide buffers that let our machines communicate with future automated process controllers."

Each of the hundreds of steps from raw material to finished product is getting productivity emphasis. Siltec has placed its new microprocessor-controlled crystal-growing furnaces at six major silicon-wafer manufacturing sites. "Removing 'personality' from ingots means better ICs, and getting labor out cuts costs," says Tony Bonora, Equipment division vice president. "Our new furnace monitors eight vital ingot parameters under closed-loop control and lets users tailor chemistry like carbon concentration and radial/axial oxygen distribution for wafers to go into specific processes, at higher yields."

## Automation's Tradeoffs

Chuck Wood, executive vice president of NEC Electronics USA and general manager of the Electronic Arrays production facilities, operates one of the industry's most highly automated plants. "Automation is inevitable," he says. "But it calls for a series of subtle compromises.

"We've virtually eliminated people from the assembly process, but many considerations feed back all the way to circuit design. For example, we settle for conservative cell size and wider inter-die spacings to make room for the automatic handling equipment."

"Less dice per wafer? Yes. But the higher yields more than make up the difference. But then, our fully automated pattern-recognition bonders are 12 times faster than humans. In VLSI, local control versus long pipelines to Southeast Asia more than make up for the highest costs."


**Automated parts-supply systems, such as this one from Eaton-Kenway, can improve material-handling productivity by as much as 50%.**

The silicon factory of tomorrow, as envisaged by Applied Materials' vice president Bob Graham, aims at improving quality and yields despite more complex circuits and shrinking geometry. "We must remove the people from inside the process," he says. "They are the prime cause of dirt and damage. They should be used solely as intelligent prostheses outside the process, for maintenance.

"I predict, not a [production] line which was the old way, but a ring-shaped tunnel structure with its own Class-10-or-better clean environment for processing parts all the way from wafer to die without human intervention. The 'silicon tunnel' will be essential if submicrometer-linewidth devices are to be achieved repeatably and with economical yields."

Some problems still await engineering breakthrough, he admits. "We will have to do a lot of inventing. For example, we need a new way to move wafers down the line. Nothing we have or can visualize today can work at sufficiently high cleanliness better than Class 10" [10 submicrometer-sized particles per million].

Productivity via automation is exemplified by a broad series of attacks on conventional plant design and management. The attacks are interrelated and emanate from leading-edge electronics technologies—CAD/CAM, factory data management, and various forms of robotics.

All aim to raise the production rates of consistently high-quality, reliable end products, using the fewest numbers of people on the least floor space for the lowest capital investment.

## CAD/CAM: Prime Tool

CAD/CAM is one of the most useful new tools of high technology. A score of companies, primarily in the U. S., Japan, Germany, and the UK, is configuring continually more powerful systems.

Basically these new tools are versatile computer systems with input via digitizing table or data stream, the ability to display and manipulate color graphics and symbols flexibly, and the capability to simulate and model temperature and mechanical stress. They can store and manage large, complex, and interrelated data bases,

plus precision plotter ouput, and, in some cases, numerical-control tapes and product-testing programs.

In the end-user world, CAD is used by architects, engineers, and builders for mechanical engineering, drafting, and simulation, all the way to finite-element modeling and analysis, as well as for city, plant, office, piping, and wiring layouts with associated materials calculations. The major fabrication industries are buying CAD/CAM at an increasing clip—a bright spot in a time of overall industry sluggishness: aircraft and automobile makers, the electrical industries, and the makers of heavy equipment for earth moving and agriculture all are buying.

Already, the big million-dollar machines are being challenged by smaller systems selling in five figures that deliver a large measure of the power of their big brothers and lack only ultimate speed and memory capacity. Managers husbanding costly capital for financial productivity are looking closely at these smaller systems. The computer industry's record of more power at lower cost is a precise analogy.

The newly arrived CAD/CAM specialist at industry analyst Dataquest, Tim Gauhan, provides a valuable perspective: "The old management-information-system role has expanded into CAD and CAM and is reaching forward into CIM—computer-integrated manufacturing. The new applications that create CIM include process planning, materials management, and production scheduling.

"The classical computer pattern is repeating in CAD/CAM: more capable 32-bit machines using SEL, DEC, Data General, and Perkin-Elmer processors and microprocessor-based machines. There are stumbling blocks; in large companies there is a power struggle between the classical data-processing operations and manufacturing for control of CAD/CAM in complex political-financial-bureaucratic environments. But the future looks bright: the $800 million business of 1981 will be a $5 billion giant by 1986."

Typical of the aggressive technology arena is the recent introduction by Gerber of a low-cost CAD system that generates artwork for pc boards. Dave Ryan, vice president of marketing, predicts that "in five years the large, centralized CAD systems will be obsolete, since they are merely prototypes for determining the functions that need implementation in the new wave of equipment tuned to perform discrete functions at vastly reduced cost. These new systems will be usable without extensive training or costly overhead staff and will cost 10% to 30% of today's big prototypes."

### Tough Talk

CAD/CAM users today expect and get productivity increases measured at up to five times and more in many applications. This means that they get layouts, drawings, and production results in weeks instead of months, months instead of years. Without these systems, no VLSI circuits could be designed, few aircraft or cars built. As a way to remain competitive in an increasingly competitive world, CAD/CAM is the most important productivity tool since the computer.

An increasingly popular tool, handling people as CAD/CAM handles designs, is the factory data-management system involving suppliers such as HP, IBM, NCR, and Texas Instruments. These are tools for managing men and materials on the shop floor and for using a company's computer power for real-time data collection and management decision-making.

Important to the factory of the future will be increasing use of robotics and other computerized manufacturing tools. One pioneering company that expects a surge of activity in this area is Dyna/Pert, which introduced automation to the electronics industries in 1955 with its automatic component-insertion machinery for pc boards. "Probably without exception, all of the industry's giants have invested extensively in this technology," says marketing manager Neil McClean. But

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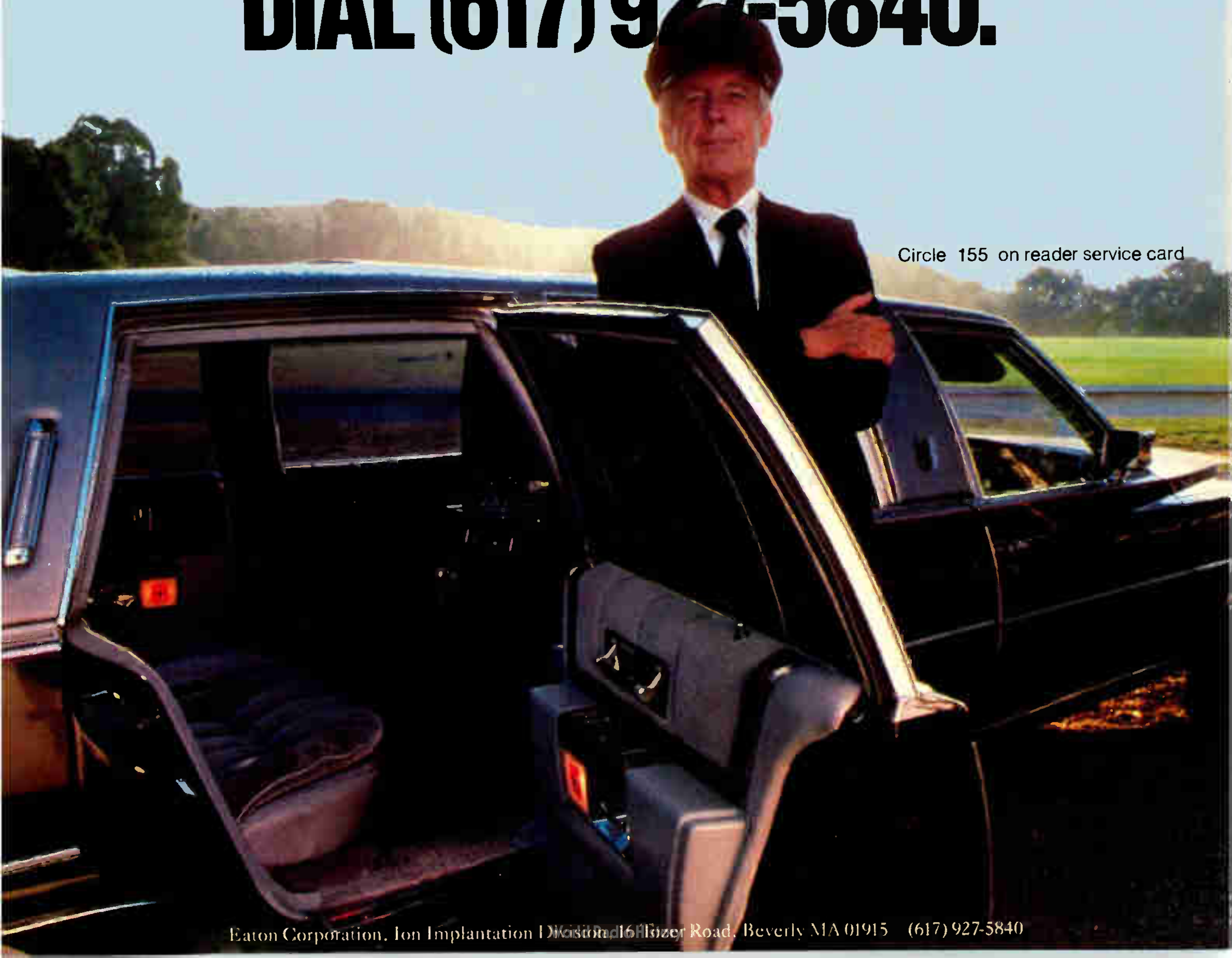

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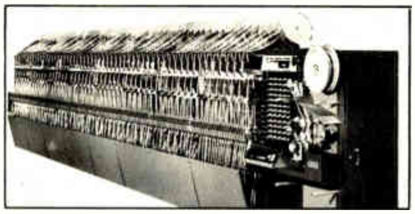
# Universal Automation in Electronics

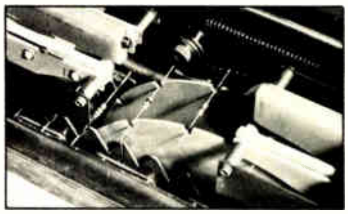
There's a labor-saving Universal Instruments machine or system for almost every electronic assembly manufacturing need. Not just one machine that will do the job for you better and faster, but a whole array of machines, systems and peripheral equipment. They range from table-top manual units that help the operator increase output, to complete production lines. Many of these systems are modular in design, so that you can increase production capability as your volume grows. Among them you'll find the perfect match for your particular need, whether your problem involves increasing productivity, improving quality, or reducing per unit cost.

**Model 2425/2315 Axial Lead Straightener-Taping Machine.** Automatically straightens leads of axial components and tapes them at a rate of 15,000/hr.

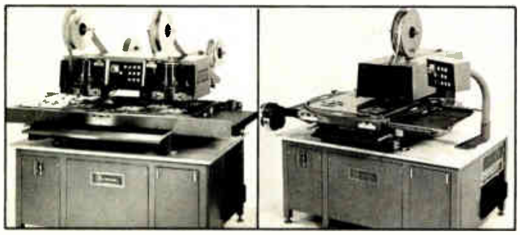


**Model 2596 Expandable Component Sequencer.** Sequences axial lead components, including jumper wires at rates up to 25,000 an hour for programmed insertion. Modules can expand from 20 to 160 input stations.

**Model 2863 Off-Line Tester.** Can be used for inspection of incoming components, or sequenced components at up to 36,000 an hour.

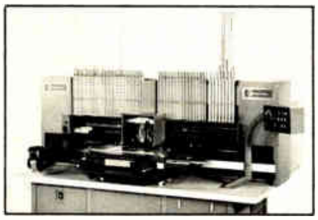


**Model 2862 On-Line Sequence Tester.** Mounts on Model 2596 Sequencer and detects missing, out-of-sequence and faulty components, and stops machine cycle for correction of error at up to 22,500 components an hour.

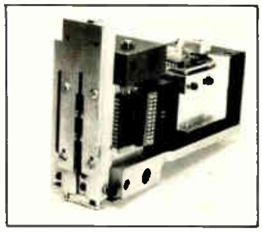


**Model 6285/6295 High-Speed VCD Axial Lead Insertion Machines.** The ultimate in automatic insertion of axial lead components. Cycle rates of 12,500 insertions an hour on single head Model 6285, 25,000 an hour with dual head Model 6295.

**Model 6345 Radial Lead Sequencer/Inserter.** Cycles at insertion rates of over 7,000/hr. Will insert a broad variety of radial lead devices, including capacitors, peaking coils, and "hairpin" axials.



**Model 6792 Multi-Module™ DIP Insertion Machine.** High-speed automatic insertion of two different DIPs selected from .300", .400", .600" sizes, sockets, and small 2- and 4-lead .300", sizes.



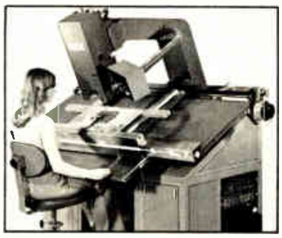
**Model 2866 DIP Verifier.** Verifies that each integrated circuit module is the correct type, functional and correctly oriented.

**Pass-Thru™ Automatic Board Handling System** eliminates manual board feeding and removal. System accepts boards in stack or magazine input, moves them through the machine and accumulates inserted boards in a magazine loader for automatic movement to the next machine.

**Model 6911 Auto Load™ Board Handler** permits hands-free automatic circuit card loading and unloading of VCD type machines.

**Model 6232 Man-U-Sert™ Manual Assembly Machine.** Machine automatically positions board, shows operator exact location for each insertion, cuts and clinches leads after insertion.

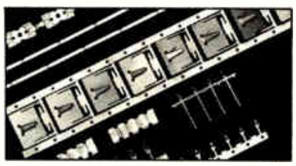
**Model 4611 Hybrid Microelectronic Assembly Machine.** Automatically places chip capacitors, integrated circuits and other microelectronic devices as small as 030" on substrates at cycle rates up to 3,600/hr.



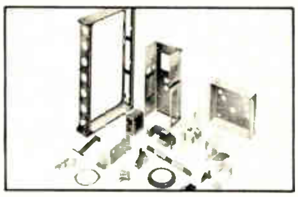
**Model 3986/3991 Wire Termination Machines.** Panels are positioned under termination gun and indicate wire to operator, for termination rates of 600 to 1200 wires/hr.

**Model 8212 Satellite Controller™ System.** Multi-machine capability and centralized program generation and storage make this the world's most productive computer-based machine control system.

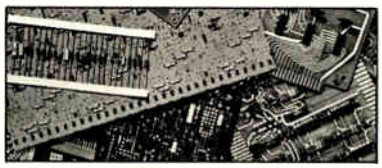
**Model 6731 Mod-U-Sert® Manual DIP Insertion Machine.** Easily-programmed built-in memory automatically feeds .300", .400" or 600" DIPs from 12- or 16-magazine feed rack.



**Circuit Board Terminals and Insertion Machines.** Stamped pins and receptacles in quantity, in strips, on reels or loose—your design or ours—plus Universal's automatic pin and terminal insertion equipment at rates up to 10,000 per hour.



**Sheet Metal Stamping and Fabrication.** Including prototype stamping, short run stamping; high speed long-run and secondary operations such as welding, EDM and NC machining.



**MEA Mechanized Electronic Assembly Service.** Any degree of electronic assembly manufacturing service from component preparation to assembled circuit boards to finished end products, including extensive test and quality control.

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Its optimum printed line resolution and complete modular versatility give you the best of two worlds.

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| Contact Printing Performance | <2 Micron Features | <2 Micron Features |
| Proximity Printing Performance | 3 Micron Features at 20 Micron Gap | 3 Micron Features at 20 Micron Gap |
| Viewing Optics Resolution | 1 Micron | 1 Micron |
| Prealign Accuracy | ±0.0025" X,Y | ±0.012" X,Y |
| Motorized X,Y,θ | Available | Available |
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**LEXIDATA CORPORATION**

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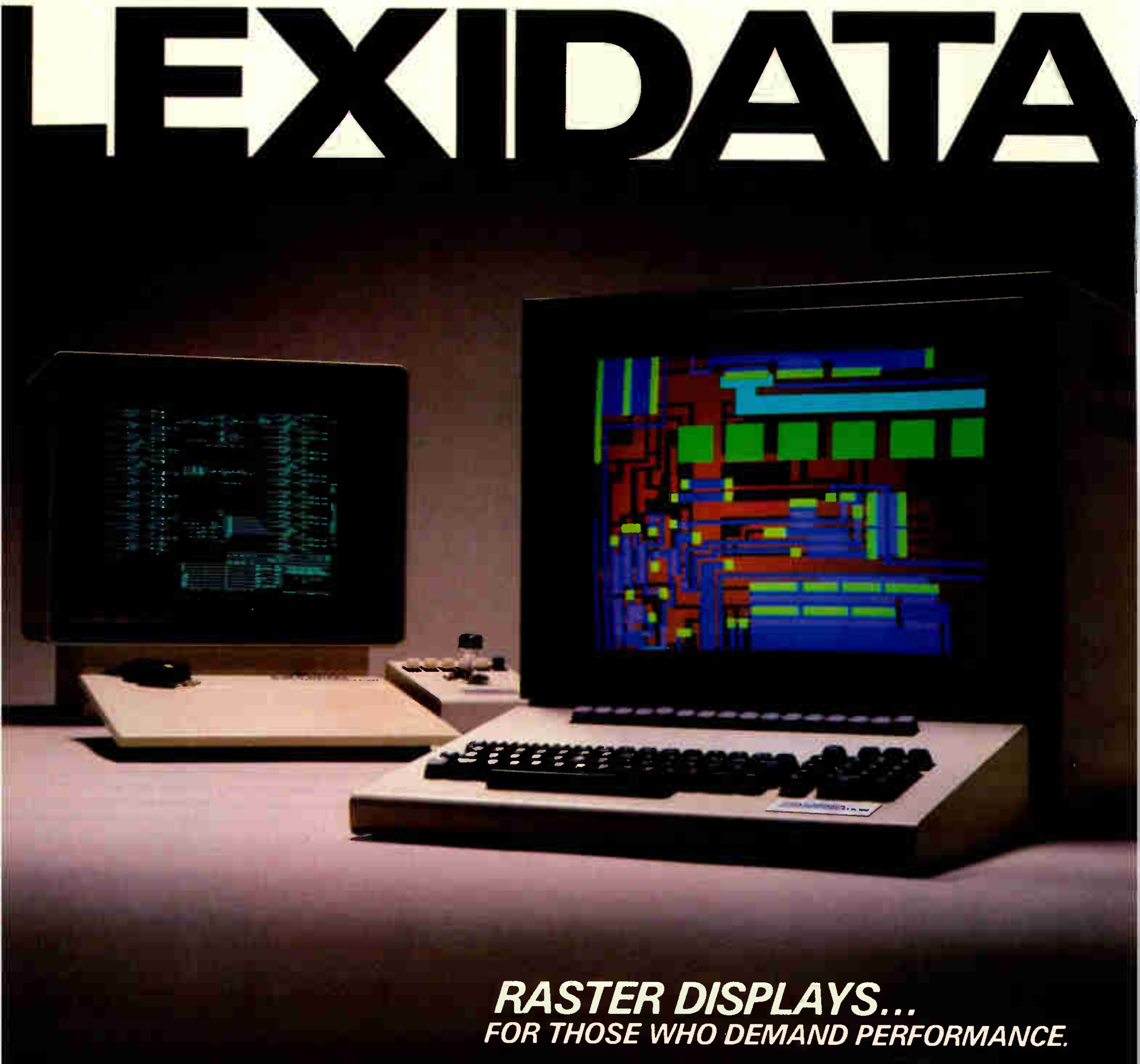


regardless of the CAD/CAM, CIM, or robotics used, control of production-line variables is crucial. For example, electronics manufacturers making more and more complex, sensitive systems are reporting severe static surges that kill products and wreak production-line havoc. Topical antistat can control this, says Steven A. Halperin, executive vice president at Analytical Chemical Laboratories. For example, "ITT-Courier in Phoenix which ships about $250 million yearly in terminals, has cut pc board defects 80%, eliminated over 15,000 manhours of rework annually, and reduced inventories by several hundred thousand dollars."

Materials-handling automation in the factory of the future concerns Eaton-Kenway in Salt Lake City. Senior vice president and general manager Jim Allred calls this industry segment "the best opportunity for American industry to make major improvements in productivity. We've integrated automatic inventory storing, transportation and tracking, numerical control, and robotics under the control of up to five hierarchical levels of computers, from a central large machine to local microprocessor intelligence in handling equipment."

## Testing: a Partner

Leading manufacturers of test-and-measurement and automatic-test equipment, such as Fluke, Teradyne, and HP, all see testing as a productivity tool, but each sees it differently. Jim Bowen is vice president for operations for Eaton Corp.'s semiconductor-industry activities, including the Test Systems division. "The drive for productivity in testing is quite clear," he says. "But quality and reliability in end products are just as important and are tightly linked to testing in the 1980s.

"The basic economics of IC manufacture are coming to a head over the issues of quality, reliability, burn-in, and test. Today at least two thirds of the problem is in the software. We must address the current generation of testing issues before we attempt the next. For example, [I believe that] 64-K RAMS are being slowed in acceptance because testing them is too costly and slow.

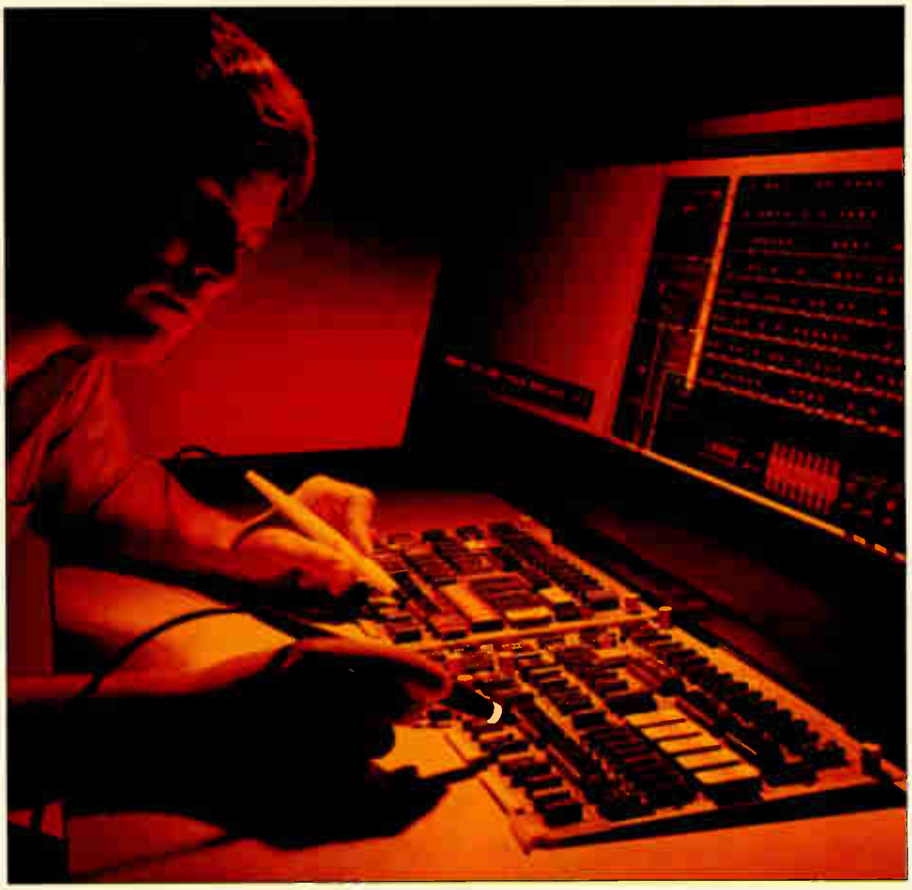
At Hewlett-Packard, Merrill Brooksby has what he calls "broad responsibility within HP" to promote productivity tools, and he asserts that "productivity at the end of the line results from a deliberate intention to create quality products. The two are virtually synonymous and must be designed in from the start. DOAs in final test, or even worse, at our customers' receiving dock, kill company productivity.

## Simplicity the Key

"Any functional productivity system, for design through production and in all testing phases must be simple. Big, elaborate systems won't work. We emphasize down-to-earth solutions usable by as many engineers as possible." The HP viewpoint carries weight; they are makers or users of virtually every type of test-and-measurement and ATE equipment in the industry.

Productivity numbers may come hard, but only cost-benefit data can justify specific testing strategies. U.S. Instrument Rentals' president Tony Schiavo emphasizes test-equipment rentals and leases to improve a company's financial productivity. "Today the pressure on earnings per share and the cost of money, plus its increasing impact on the balance sheet, forces more aggressive leveraging," he says. "Instrument rental and lease—from as short as a week to as long as 4 to 6 years—is part of the solution."

Productivity—both personal and corporate—has been improved more by the computer than by any other



**More capable test systems like Fluke's 3050A digital/analog tester can check out a variety of circuitry and permit full test-program generation.**

element in technology. Today the computer is not discrete, but integral to almost everything men and machines can do.

The link between electronics, computing, and communications has become so tight that there is almost seamless continuity. Every discipline in the industry makes an important contribution down to the component and materials level, and each area of technology is pushed to deliver cost-effective results. By 1999, these links will be forged even more tightly.

Order-of-magnitude increases in performance, coupled with similar reductions in cost that most computers have delivered each decade since their inception, constitute the industry's most notable contributions. Peripherals of every type have shared powerfully in the overall achievement. Indications are that this technological double play will continue. Fifth-generation machines, using voice recognition and voice output and incorporating huge, low-cost optical memories, will bring personal-computing power to almost any citizen in the industrialized world who needs or wants it.

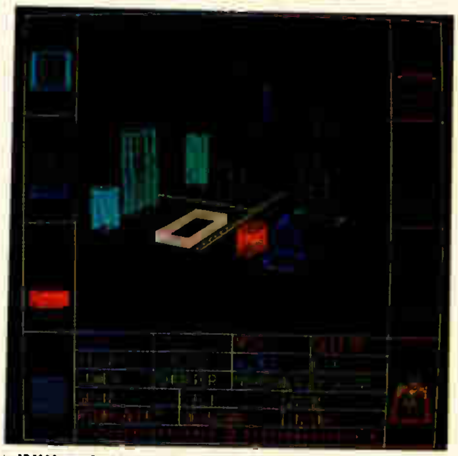
## The Productivity Influence

By the late 1960s, leading computer makers had already established electronic data processing as a basic productivity tool for business, industry, government, medicine, finance, and science. Their influence is hard to overstate.

Minicomputer makers established a strong middle ground. They did it through cost reduction, massive and cheap main and peripheral memory, and networking—essentially emulating and competing with big-machine features.

Then the microcomputer invasion launched by Intel dragged the semiconductor industry into new levels of vertical integration. Intel—and other companies such as National, Texas Instruments, Motorola, AMD, Signetics, and Zilog—are progressing from 4- to 32-bit machines in a decade.

In the process, they are driving digital



**With advanced display techniques and sophisticated software, Evans & Sutherland computer graphics are reaching new heights.**

computing concepts into millions of new applications rooted basically in the relentless demand for industrial productivity. Personal applications have proliferated, but the personal computer is still in its infancy.

Progressive peripherals are revolutionizing data and word processing, CAD/CAM, and office-system productivity. For example, "technological and price-performance advances in computing, VLSI memories, and microprocessor-based architecture will make raster-scan graphics the dominant display technique of the 1980s, and quality will improve as costs decline," says Lexidata president Ralph Linslata. He foresees wide use of these in integrated form for facsimile, electronic mail, and graphics-plus-data processing.

Machine linkup was yet another stimulus. The advent of much less expensive and more reliable digital data communications, including satellite links, notched computing's productivity thrust upward still further in the 1970s. The question for managements in the Fortune 500 companies and their peers worldwide is not whether but when to implement fully integrated computer-communications systems for data and words. The challenge is how to configure them for maximum possible cost-effectiveness and minimum reasonable obsolescence.

Yet none of these advances would have been possible without software to guide the machines. Today, software looms as the productivity barrier to be broken if progress is to continue.

Sometimes dubbed the 'infinite task,' the problem of matching the explosion of microcomputers, minicomputers, and mainframes with operating and applications software is assuming high priority in the data- and word-processing community. Programmer shortfall—estimated variously by observers at 100,000 to 1 million by decade's end—is close to crisis. Cost is another problem: software already consumes 80% of a system's lifetime cost and is predicted to exceed 90% by 1990, as hardware costs declined and labor costs in programming rise.

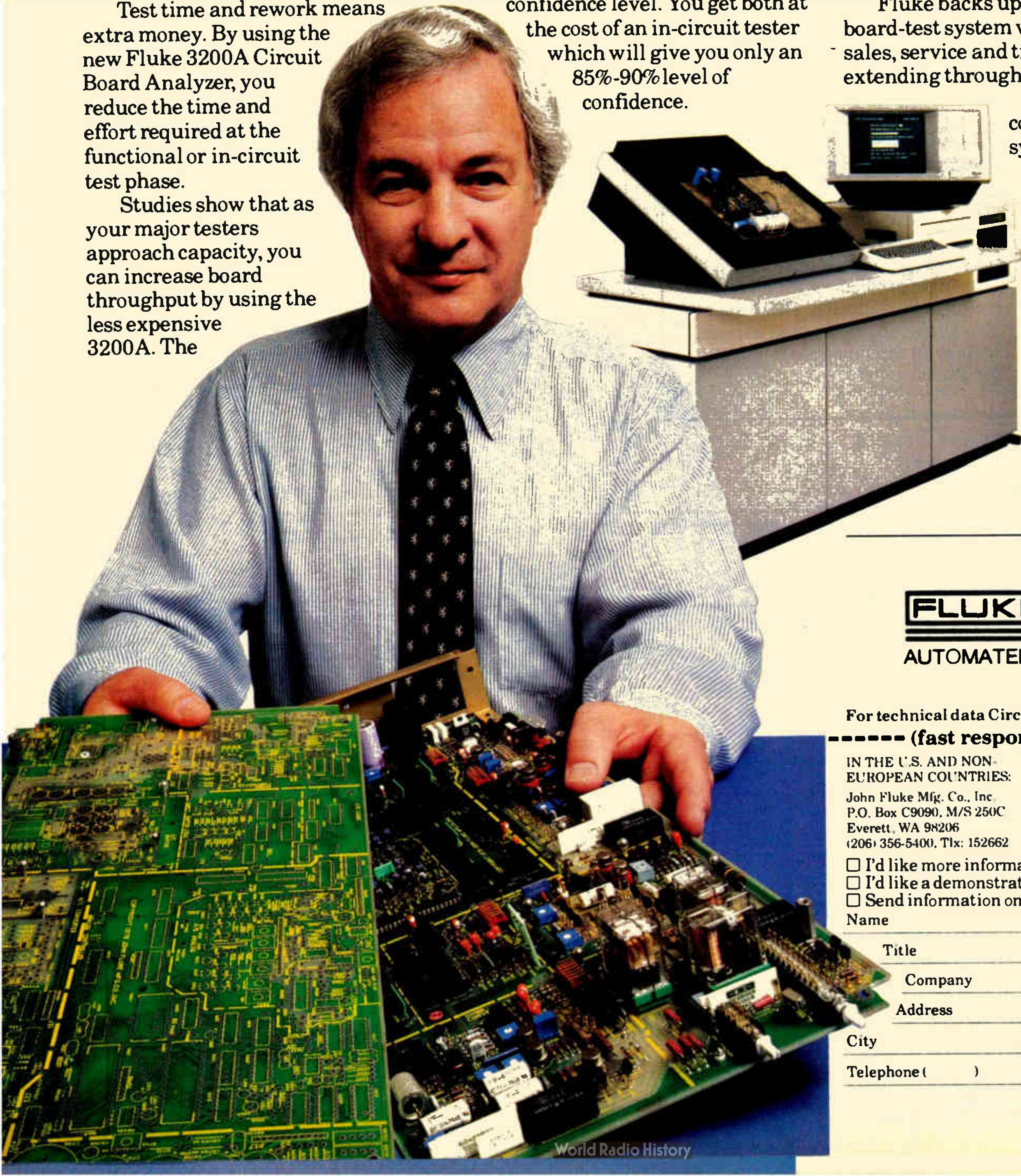
## Software's Productivity Crisis

The development of software that requires minimal programming skill to use it is crucial. It is noteworthy that when HP introduced an ambitious range of office-automation products last month, the hardware was coupled with emphasis on new user-friendly software-automation tools. They will enable people without programming experience to process words, graphics, and numbers, according to HP Business Computer Group general manager Ed McCracken. What's more, for software pros, he promises a factor-of-4-to-10 improvement in programmer productivity with the Rapid program-prototyping concept.

Off-the-shelf, packaged programs often fail to meet users' needs, and the built-in inefficiences and cost to customize deter many users. Now the role of automatic program generation is becoming accepted.

Modules addressing specific functions are coded automatically once the user has specified the kind of program desired, thus saving time and manpower. More than 10 companies are already active in automatic program generation; the programmer gap is expected to stimulate more entries.

Operating systems resident in a



# REDUCE ALIGNMENT COST/WAFER

In these days of rising capital equipment costs, Canon gives you outstanding cost per wafer advantage. The concept is "MIX and MATCH." Today's devices do not require alignment on the finest resolution mask aligner at every level. Such aligners are expensive and comparatively slow in throughput.

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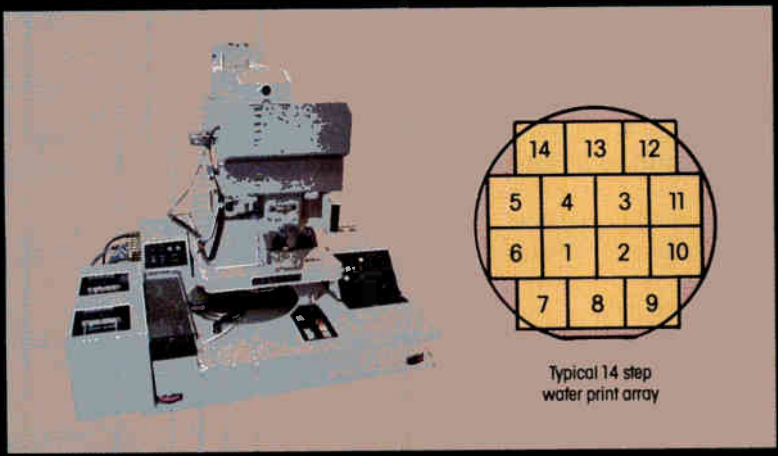


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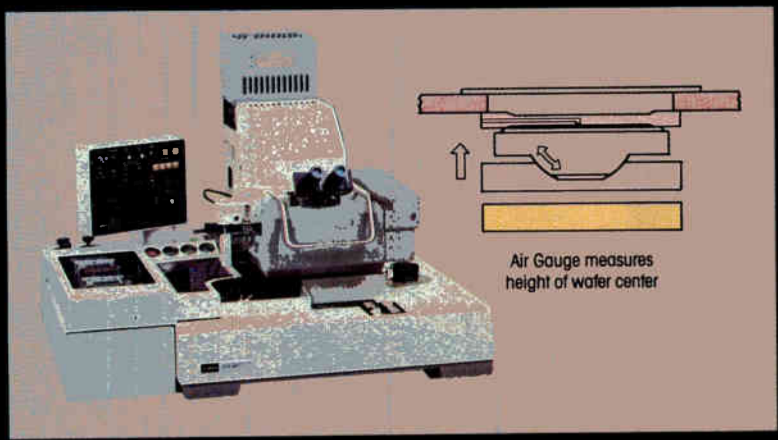


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silicon chip are the first elements of silicon software available. Soon, subroutines are expected to be available on chip, callable by the programmer on demand, to accelerate program development. Standard applications functions—especially where the application is fully understood and reliably coded—are anticipated in newer microprocessors under development.

"Most professionals who need computers have neither the time nor the inclination to learn programming," says John Peers, chairman of the newly formed Technology Industries and a pioneer in programmerless programming with Logical Machines' ADAM in 1974. Peers wants to go far beyond automatic program generation, silicon software, or other aids.

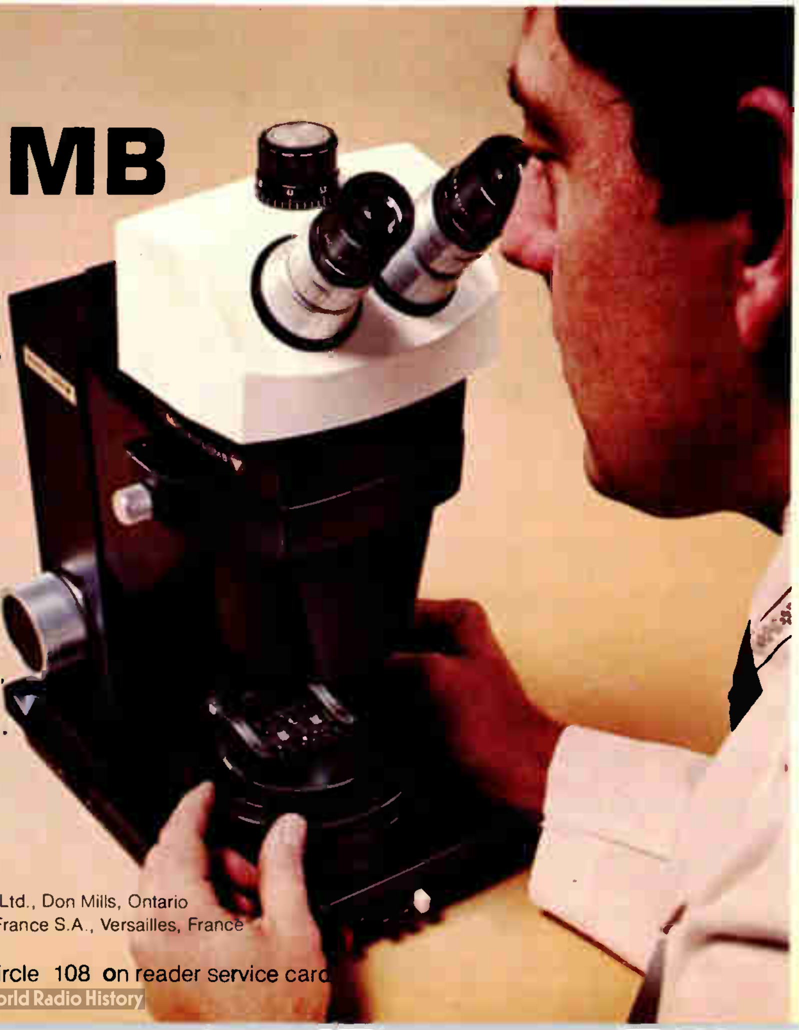
"Computer power must be transparent, instinctual if it is to become the 1980's true productivity tool," he says. "Our goal is to permit anyone to put data into a computer, manipulate it, and inquire from data bases, without any nonEnglish or nonroutine programming or other action. The machine should be able to accept essentially any form of input that can be digitized, including voice and images."

**Personal Computing's Role**

Mike Markkula, president and chief executive officer of Apple, expects ultimately to see personal computers on every desk. "These machines are all about individual productivity," he states. "I can do in minutes on my Apple what used to take hours by hand—or was so laborious I wouldn't attempt it. I get my own data now, not in a week via a subordinate."

"The personal computer will be for the 1980s and 1990s what hand-held calculators were for the 1960s and 1970s," he says. "Based on history, we will be able to deliver 10 times as much personal computing power for a tenth the cost. As important, we will make our machines learnable in 20 minutes, versus today's 20 hours, without having to program. Then [the personal computer] will be pervasive—no one will be able to work productively without it."

Still, the manpower shortage looms, as profound for hardware engineers as it is for programmers. Recent AEA predictions of six-figure manpower shortfall by 1986 in all key professional engineering and software areas underscore the problem—which is insoluble, based on current college enrollments. □



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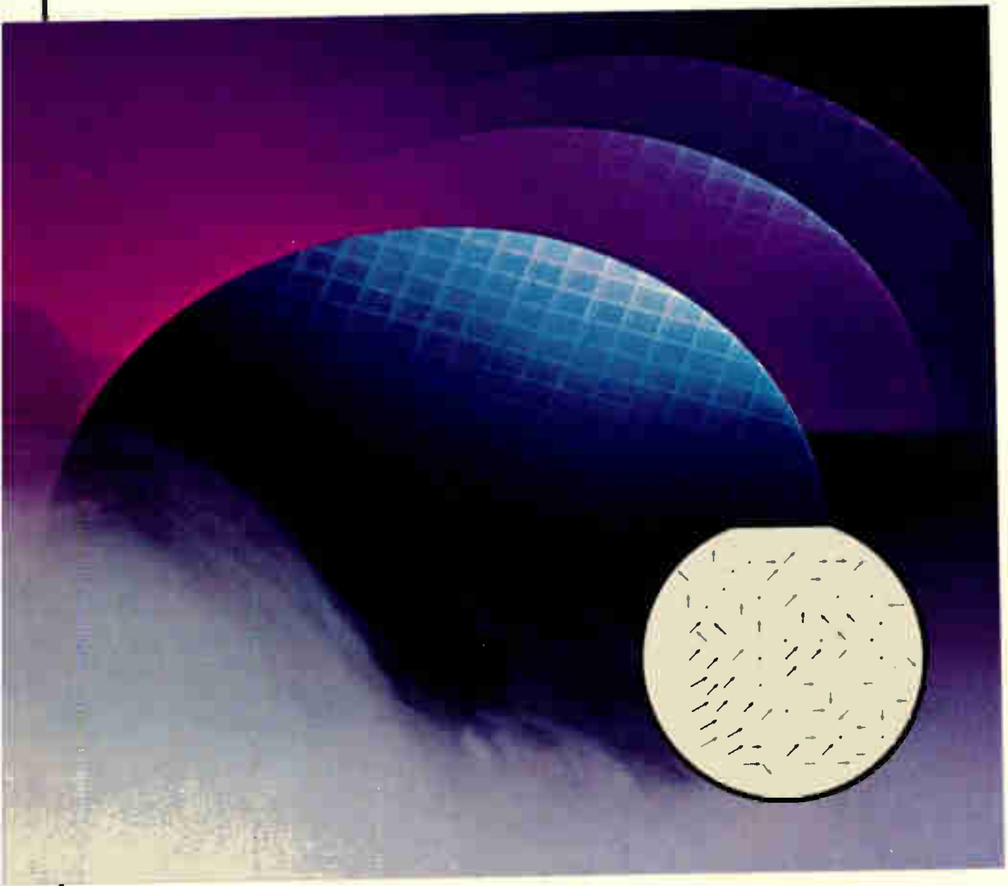

OVERLAY SCALE

0.50 μm

**The inset shows a vector map of the Model 300 overlay performance measured against a contact-printed, first-level using electrical patterns distributed over a four inch wafer. Combined magnification/distortion and alignment errors are measured using this technique.**

Perkin-Elmer now offers a cost effective route to higher packing densities, higher yields, greater production economies ...utilizing the same process, the same floor space, the same personnel, the same spare parts and the same tooling.

It's all made possible by the new Micralign Model 300 with a specified overlay accuracy of 0.5μm, machine stability of 0.25μm and resolution of 1⅛μm at 300nm.

Dramatic improvements in optical fabrication techniques are incorporated in the Model 300. To take full advantage of this, the 300 also incorporates improved optical mounting techniques, vibration isolation, air flow and internal temperature control, wafer-cassette protective cover, and pellicle protected mask capability.

These improvements provide overall stability measured in months, not days.

To find out what else the Micralign Model 300 can do for you, and to take advantage of equipment trade-in policies and Model 200 to Model 300 retrofits, contact Perkin-Elmer, Semiconductor Operations, 50 Danbury Road, Wilton, Connecticut 06897.

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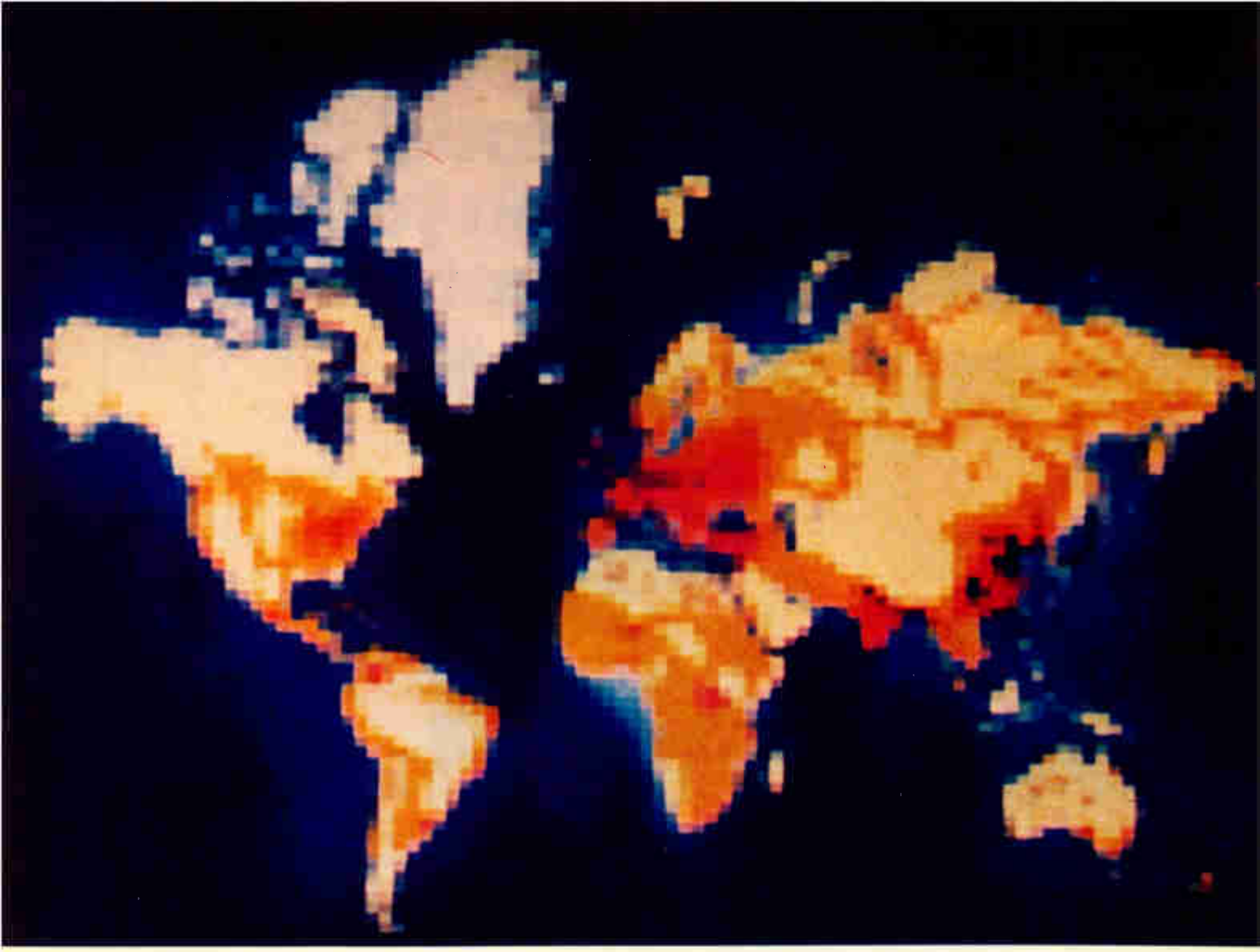


# Resource manager coordinates testing

## In-circuit board-testing station joins existing functional testers in networked system with distributed computing

by Richard W. Comerford, Test, Measurement & Control Editor

**Test-system networks, which** usually centralize their computer power in a large automated test system or host, have paved the way for networks in the factory. But "they do not provide an optimum utilization of computing power," says James Keener, vice president of sales and marketing for Computer Automation's Industrial Products division.

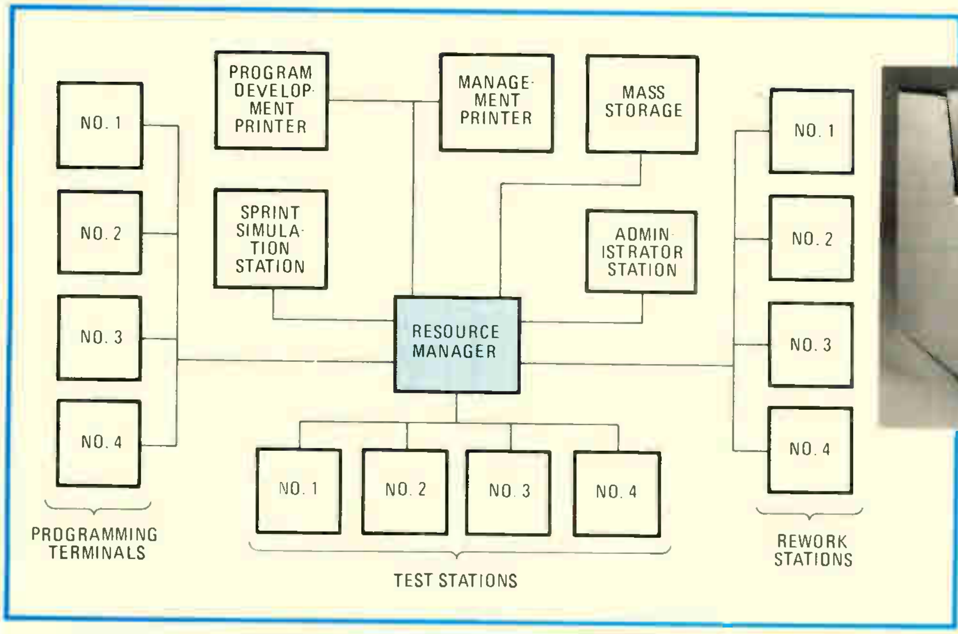
Thus about a year and a half ago, the company started to develop a network system targeted at using distributed processing to efficiently manage board flow in the production arena. Though separate elements of the total system have since been introduced, now the company is unveiling the total scheme, called Marathon [*Electronics*, Nov. 3, p. 33], and is adding two elements with a third promised by mid-1982.

The two new elements that complete the test line are what the company has dubbed a resource manager and a prefunctional tester. The resource manager ties together all test activity, including program development and checkout, testing and reworking of production boards, board-flow management, and also corporate reporting.

**Multitask approach.** For the resource manager, Computer Automation leveraged work done by its Naked-Mini division and employed an LSI-4/95 computer with an operating system resembling Bell Laboratories' Unix. The unit does not serve as a data integrator, performing all the test-generation, simulation, and data-analysis functions a host would in other systems, but instead uses multitasking software to manage and allocate the computer resources in the rest of the system. For example, it allows four programmers to share a Sprint board-simulation computer. In the previous stand-alone configuration [*Electronics*, Jan. 13, p. 276], the allocation was one programmer per Sprint.

The resource manager also takes care of archiving test programs—using a hierarchical data-base–management system—once they have been generated using the Majic test language [*Electronics*, Feb. 10, p. 40] and debugged using Sprint. Test libraries as well as test data can be stored on a 300-megabyte disk system, which can be doubled in size.

When test-station operators are ready to run a test, they can call for programs using a board part number or some other management-defined descriptor. The resource manager will download the appropriate software using a high-speed serial local link called Acorn. Acorn differs from other local nets such as Ethernet, according to Irwin Pfister,




**Test sharing.** The Marathon network (left) relies on an LSI-4/95 to manage distributed computers in a multitasking mode. A test station may be a prefunctional tester (above) or a functional unit.

vice president of engineering, in its "more sophisticated computer protocol. Ethernet doesn't have the data-verification capability built into Acorn, which is a must for valid testing and reporting."

**One source.** So that it can serve as a single source for board-testing systems, Computer Automation is adding the prefunctional tester. This 4,096-pin station "is basically what the industry has been calling an in-circuit tester," Pfister explains, "but since our Capable series of functional testers has always used in-circuit techniques to find faulty components, we think it's more important to emphasize the methodology angle of testing." A prefunctional tester checks to find assembly faults before the functional tester ensures that all the components work together.

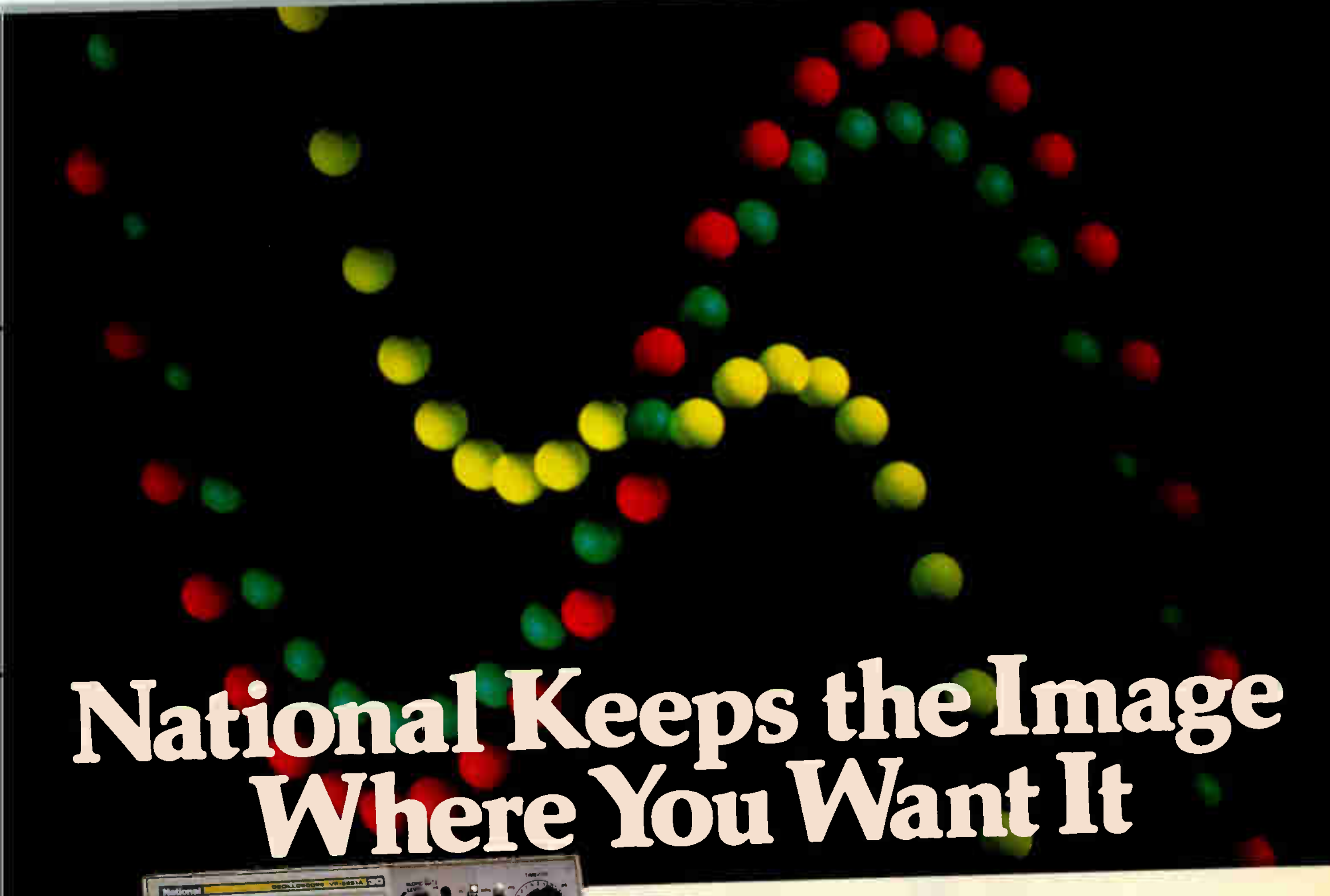
The Marathon functional testers are derived from the Capable 4900 series, and existing 4900s can be tied into the system. But those testers do not require the software development and management-oriented functions when linked to Marathon, and thus are dedicated only to testing functions.

Because of the current frugal approach to capital investment, Keener emphasizes that "Marathon is not only for big users—a small user can get a programming station, resource manager, and prefunctional tester for $230,000." For that price, he adds, the user also gets the management-reporting capability now, and with time can expand to a system such as the one diagrammed, which would cost about $1.5 million.

One of the items a user may add later is a paperless rework station, which will use board-failure data to tell a board fixer what component needs replacement. To be formally unveiled in mid-1982, it "will not have the full graphics capability of the Marconi unit [*Electronics*, Oct. 20, p. 264] but it will get the information needed and talk back to the resource manager," says Pfister.

Marathon deliveries, starting in April, will take 90 days.

Computer Automation Inc., Industrial Products Division, 2181 Dupont Dr., Irvine, Calif. 92713. Phone (714) 833-8830 [338]



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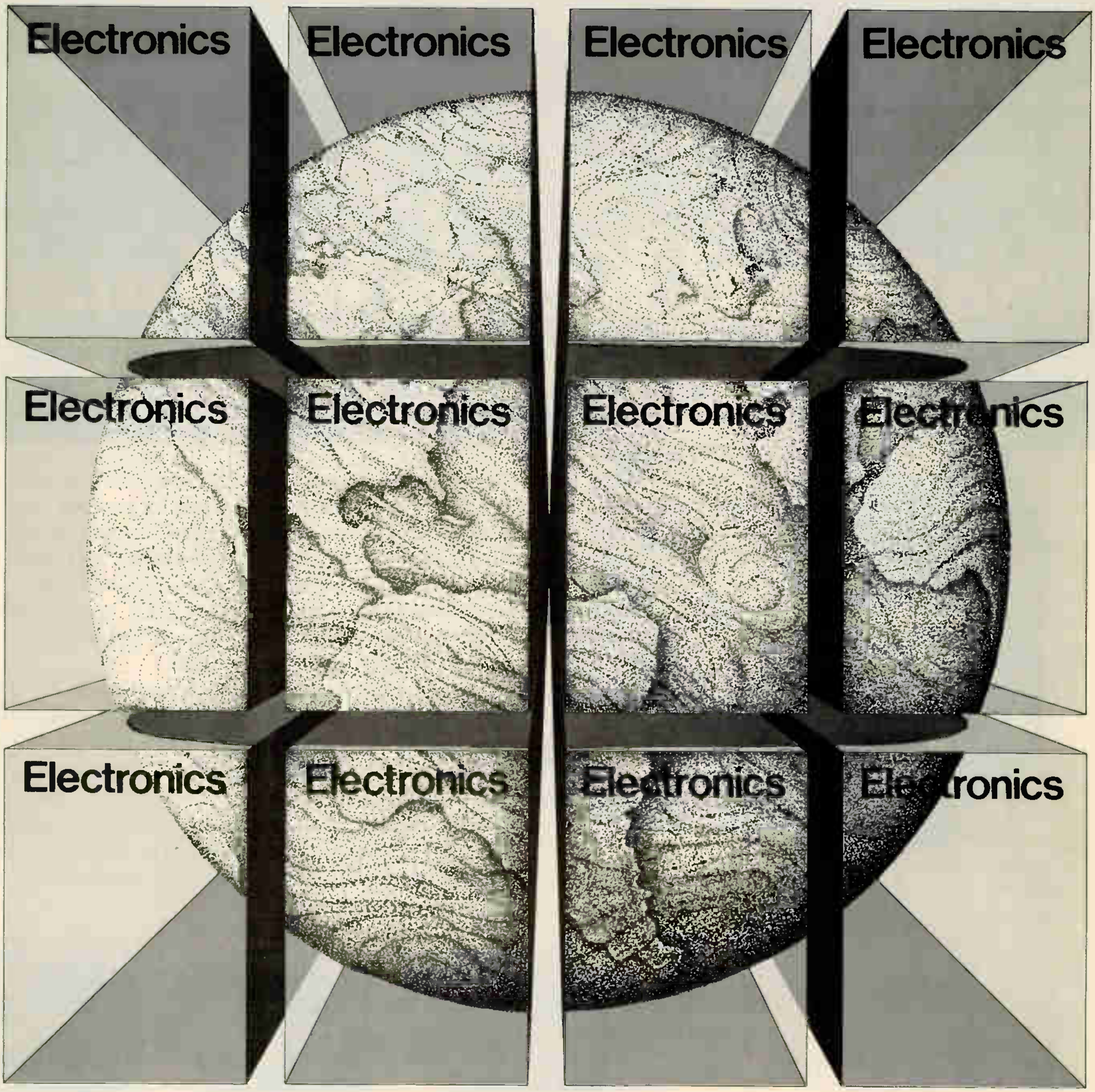
# examine...
## a worldwide perspective.



# Boards hook DEC machines to Ethernet

## Controllers buffer host from network, performing tasks for first two layers of protocol and collecting net statistics

*by James B. Brinton, Boston bureau manager*

**For a user** to get the most out of a local network, his equipment must interface with it gracefully and operate with minimal host-processor overhead. Those two factors are reflected in the first products from Interlan Inc. [*Electronics*, July 28, p. 97], microprocessor-based board subsystems that handle many aspects of local-network interfacing.

The firm's communications controllers directly connect the bus of Digital Equipment Corp. LSI-11, PDP-11, or VAX computers with Ethernet. The interfacing subsystems include a Z80 control microprocessor, input/output buffer storage, and all hardware and software needed to conform with Ethernet version 1.0 protocols.

According to president Paul J. Severino, Interlan's products differ from earlier offerings in this area in that they have both local intelligence and a direct connection to the computer bus. The few other systems available either operate via RS-232-C, IEEE-488, or other ports, or make interface control operations the province of the host, resulting in undesirable overhead.

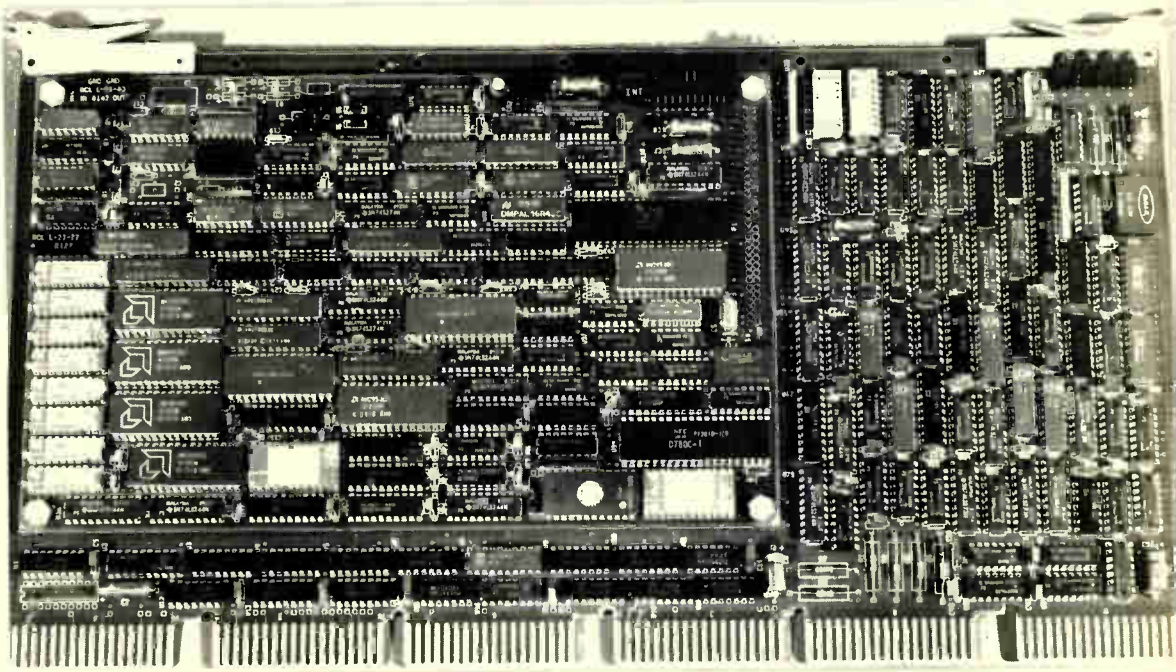
Users with a PDP-11 or VAX computer can purchase the company's NI1010 Unibus communications controller, priced at $2,940 in lots of 25. The NI1010 comes complete on a single circuit board, taking one Unibus slot. LSI-11 users would buy the NI2010 at $1,625 in quantities of 25; the 2010 takes two quad-height slots.

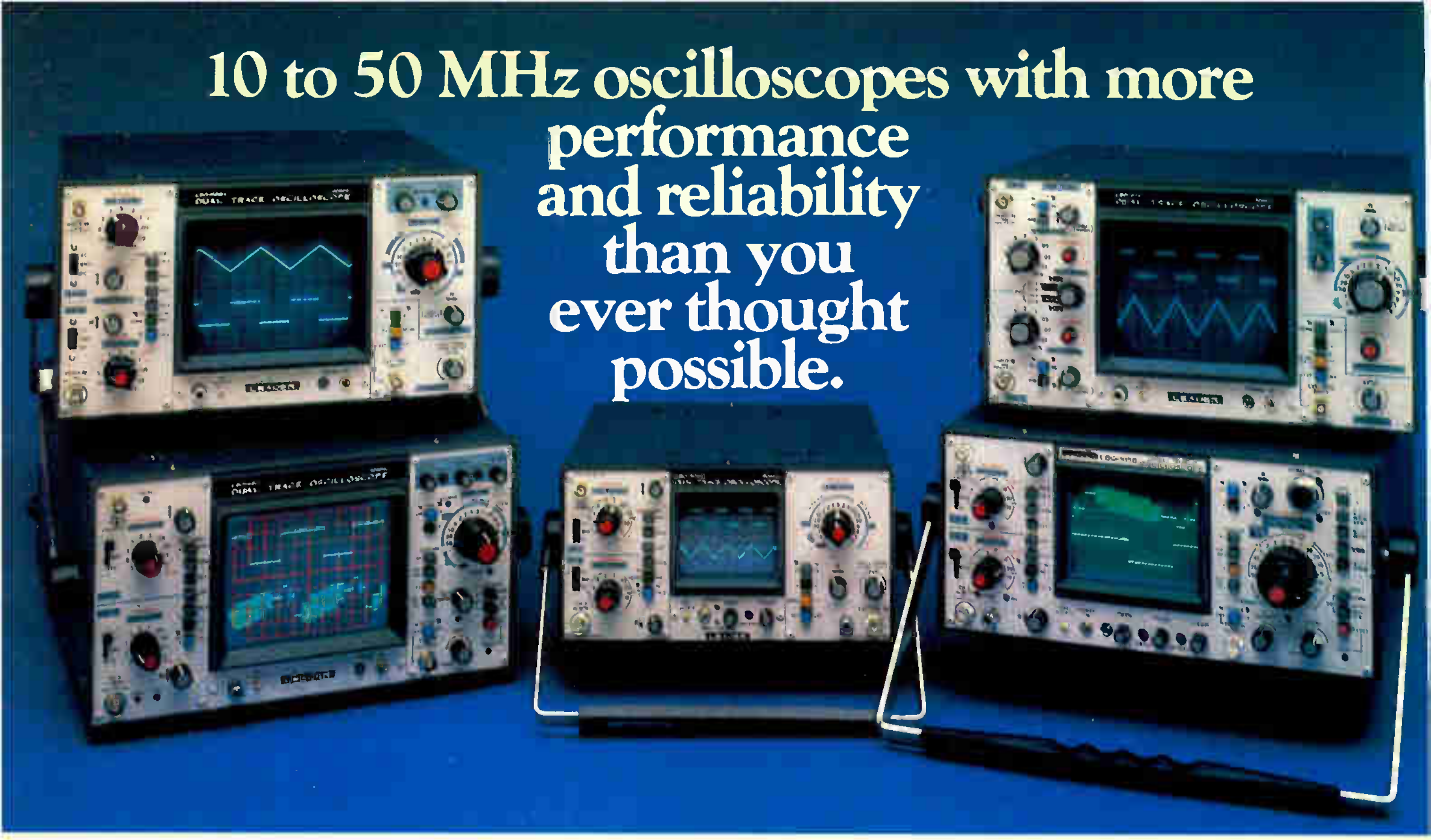
Interlan-supplied device drivers can be interleaved with DEC's RSX-11M and -11S operating systems, and with connection to an Ethernet cable, operation can begin. The company will sell its customers an Ethernet transceiver if they need one, the model UN-NA1010; using this transceiver, the host computer can be up to 50 m from the Ethernet cable, and stations can be up to 1,500 m distant on the cable before repeaters are required.

**Framed.** Ethernet uses a packet or frame format to transmit data. A frame consists of a 64-bit synchronization preamble, 48-bit destination and source addresses, 16 bits of data-type information telling receiving nodes how the data is to be used, 46 to 1,500 bytes of data, a cyclic-redundancy-check sequence 32 bits long, and a 9.6-$\mu$s frame gap.

The Interlan devices perform the functions needed to transmit and receive data in this form. They also collect statistics on network and node performance, the latter a feature common in large network monitors. These jobs correspond to layers 1 and 2 of the Ethernet interconnection protocol, the physical layer and the data-link layer. With these tasks properly performed, Ethernet nodes can communicate at a half-duplex rate of 10 Mb/s.

Physical-link functions are simplest. During transmission, they include generation of the 64-bit syn-





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LEADER's oscilloscope line includes 12 models, single and dual trace versions, for bench or field use. All models offer comprehensive triggering controls, TTL compatible Z-axis modulation, front panel trace alignment control and convenient, color-keyed front panel layout. Probes are furnished with every oscilloscope and options include probe pouches, carrying cases and front panel covers.

## 50 MHz alternate time base.

LBO-517 gives you complex analysis capability with alternate/composite triggering and simultaneous main/delayed time base display on its dome-mesh CRT with 20 kV accelerating potential. Has 7 ns rise time, 5 mV/cm sensitivity with X5 multiplier for 1 mV/cm up to 10 MHz, 5 ns sweep speed with X10 magnifier, and two trigger view channels.

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LBO-515B is a dual trace oscilloscope with 4-inch CRT and parallax-free internal graticule, 5 mV sensitivity, 120 ns signal delay, trigger hold-off, delayed sweep and x-y operation at full sensitivity.

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The dual trace LBO-520A combines 10 ns rise time with 5 mV sensitivity and 120 ns signal delay lines. Has 5.6 kV PDA CRT with internal graticule.

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LBO-308S gives lab performance and high reliability in field service. Sensitivity is 2 mV with complete triggering controls and 18 sweep ranges to 0.1 µs/div. with X5 magnifier. Dual trace, compact, lightweight with 3-inch, internal graticule CRT. Optional internal, rechargeable battery pack available.

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Circle 112 for product literature

Circle 113 for product demonstration

chronization preamble, parallel-to-serial data conversion, calculation of the CRC value and its insertion into the frame, and Manchester encoding of the bit stream. It also seeks to avoid collision through monitoring of other stations' frame transmissions and sensing collision signals from its local transceiver.

Physical-link receiving functions include synchronization with the incoming bit stream and removal of the synch preamble, decoding of the incoming bit stream, and serial-to-parallel conversion of the stream.

Within the data-link layer, the Interlan subsystems perform transmit-data encapsulation and transmit-link management. They also do data decapsulation and receive-link management.

Transmit-link management consists of carrier deference (delaying transmission until the network is silent) or collision detection in the event of simultaneous transmissions, and of back-off and retransmission in the event of collision. In Ethernet, collisions are common, so the receive side of the subsystem is designed to filter collision fragments from valid frames—an important aid in maximizing link throughput.

When not transmitting, the subsystem monitors traffic continuously. Usually, the unit processes a frame up to the destination address. It accepts frames either if they are addressed to it, if they are broadcast to all nodes in a system, or if the address matches one of the 63 multicast-group logical addresses the user may assign to the board. This last capability allows users to send data to from 2 to 63 nodes selectively without broadcasting to all nodes or repeating the transmissions.

**Net monitor.** If a node is to perform network management or diagnosis, its controller can operate in what is called the promiscuous receive mode, bypassing its address-filter logic and accepting all undamaged frames. It will flag its host with network performance data when desired. Net statistics collected include: frames received, frames received with CRC error, frames received with alignment error, frames with out-of-window error, frames transmitted, and collisions.

Interlan's subsystems buffer the host bus from the unpredictable frame arrival and departure times characteristic of Ethernet. The boards have a 16-K-byte first-in, first-out buffer for received frames, so few time-critical demands are made of the host bus. For transmission, the subsystems have a 2-K-byte FIFO buffer, enough for one frame.

All data transfers between the controllers and bus memory are supervised by an on-board direct-memory-access controller. The user can preload as many as 16 buffer-address and byte-count values for DMA received frames.

On power-up, the communication controllers perform tests of on-board memory, registers, and data paths; light-emitting-diode indicators show the state of the board. If there is a failure, the user can resort to diagnostic software supplied by Interlan.

There also are network-related testing and diagnostic features. The user can exercise the controller in an internal or external loopback mode; this makes it possible to isolate trouble to the Ethernet cable, the transceiver, or to within the controller.

For users who wish to build their own controllers to suit computers Interlan has not yet addressed, the NM10 Ethernet protocol module is available at $1,725 in quantities of 25. It is equipped to interface with most available 8- and 16-bit microprocessors and buses and performs almost all of the communications controller's functions.

Software is unbundled; the NS-2010 RSX-11M/S device driver software has an initial license fee of $1,000; copies cost $100.

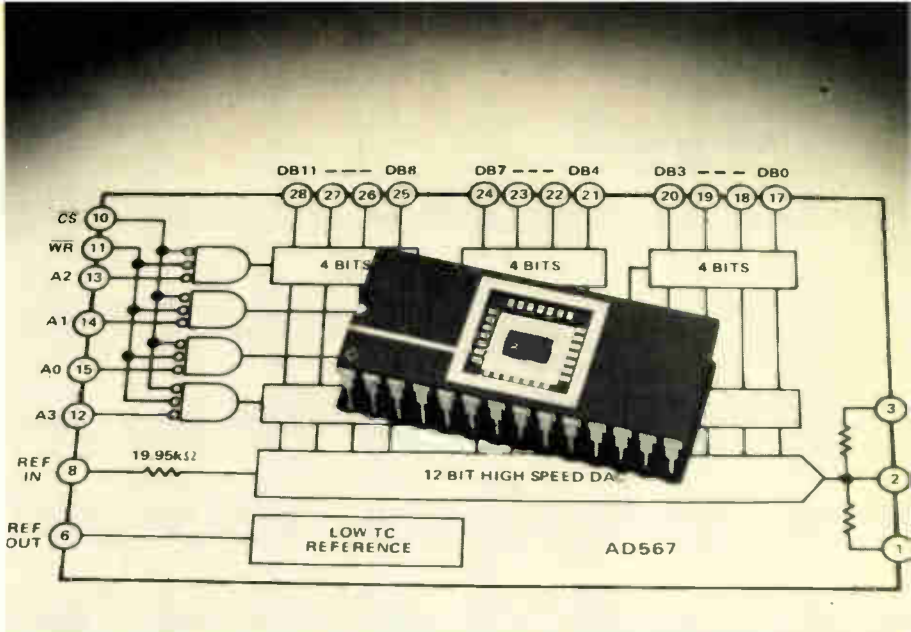
Units are scheduled to enter beta test immediately; full-scale shipments are to begin in January.

Interlan Inc., 160 Turnpike Rd., Chelmsford, Mass. 01824. Phone (617) 256-5888 [339]

Data acquisition

# D-a converter is double-buffered

## 12-bit monolithic converter works on fast bus, has on-chip laser-trimmed reference




"We want this to be the standard digital-to-analog converter of the mid-1980s," says David W. Kress, marketing manager at Analog Devices' Semiconductor division. He is talking about the firm's AD567 monolithic d-a converter, a 12-bit current-output unit with double-buffering input latches that make possible operation with any current or foreseen microprocessor.

Analog Devices has introduced several latched d-a converters in the past year, but none has the speed or applications flexibility of the new AD567, says Kress. Nor do they have its aggressive pricing—less than $15 per piece in hundred-unit quantities.

"We have other converters available now that can load data in several word lengths, but all impose some restrictions on use, whether in word length, right or left justification, or other parameter. The AD567 does not," says Kress. "It can take parallel loads from almost any microprocessor or bus at rates up to 10 or 12 MHz." Naturally, since it is a 12-bit part, the AD567 has latches 12 bits wide, but it can work with 16-bit buses, says Kress. In conversion, the last four bits are ignored.

A key advantage in applying the AD567 is the speed lent it by its double buffering. Using two latches in series allows the unit to grab data during the increasingly brief periods during which that data is available on today's increasingly fast microprocessor buses; the processing system need not be slowed to accommodate the converter.

Nor is there a need to add outboard input circuitry, according to company applications engineers. With an 8-bit microprocessor, for example, the required latches might mean the addition of three more logic chips, at a cost of about $3. Of course, the added chips increase board size and cut reliability; with the AD567 they are not needed.

**Extra resistors.** As a further convenience to the user, the chip also contains silicon-chrome thin-film "application" resistors, which can be used either with an external operational amplifer to supply precise output voltages, or as input resistors for an analog-to-digital converter. These resistors are also laser-trimmed for minimum offset error; typical bipolar offset error is 0.05% of full scale and 0.15% maximum. Unipolar offset error is typically 0.01% of full scale and 0.05% maximum. Data-hold time in the latch system is rated at zero, and write pulse width can be as short as 100 ns.

Thus, the unit should drop into systems with minimal inconvenience to the design engineer. The analog portion of the system also is speedy, with the bipolar current-steering converter settling to ½ least significant bit in 500 ns at most, and typically in 400 ns. Part of this speed is due to the unit's current-output design, but some users deem it a convenience to be able to select the appropriate output amplifier for their application.

The AD567 includes an on-chip reference. In this case, the 10-V reference is accurate to better than ±1% maximum. The voltage also is available at pin 6 for use elsewhere in the system. The reference uses a buried-zener design combined with on-chip thin-film resistors that are laser-trimmed to the final reference-voltage value.

Laser trimming also is used to maximize linearity. The chip's thin-film resistor overlay is trimmed to assure ±½-LSB maximum linearity error, and monotonicity is guaranteed over the unit's full 0°-to-70°C operating temperature range. Its typical full-scale gain temperature coefficient is 10 ppm/°C.

The AD567 is offered in a 28-pin ceramic dual in-line package. It is compatible with both ±12- and ±15-V power supplies, dissipating a maximum of 495 mW, and typically only 300 mW. Input levels are compatible with TTL and complementary-MOS logic.

But to some users, price will be the most important aspect of Analog's introduction. In hundreds, the AD567JD is priced at only $14.95 and its companion AD567KD costs only $22.95 in like quantities; the latter unit offers slightly tighter accuracy—and temperature—coefficient specifications. Both parts are available from stock.

Analog Devices Inc., Semiconductor Division, 804 Woburn St., Wilmington, Mass. 01887. Phone (617) 935-5565 [381]

## Remote interface adapter expands acquisition system

An industrial-control and data-acquisition network, the Remote Input/Output System operates over a single cable of up to 5,000 ft in the full-duplex, bit-serial communications mode. The cable consists of three shielded-wire pairs, including one in reserve as a spare.

Working either downstream from the user's central processing unit or as a stand-alone system, the RIOS master station communicates with up to 127 individually addressable, intelligent remote stations, which may be configured hierarchically to support several thousand analog and digital sensing inputs and outputs.

Introduced last year, RIOS has since been augmented by an STD-Bus–compatible controller that comprises a serial communications board and a Z80-based processor board. The controller is priced at $349.50, with delivery in four weeks.

The RIA-8201, a remote interface adapter that uses a Z80 microprocessor along with expanded user read-only memory and on-board random-access memory, is available immediately for $299.50. Each RIA functions as a remotely located peripheral interface adapter that has 16 input/output lines and four control lines. Other additions include a latch board that allows mixed analog and digital I/O at any remote station and an analog-to-digital-to-analog board that performs bidirectional a-d conversions with up to 10 bits of resolution. These are priced at $99.50 and $379.50, respectively, with immediate delivery.

International Rectifier, Crydom Division, 1521 Grand Ave., El Segundo, Calif. 90245. Phone (213) 322-4987 [383]

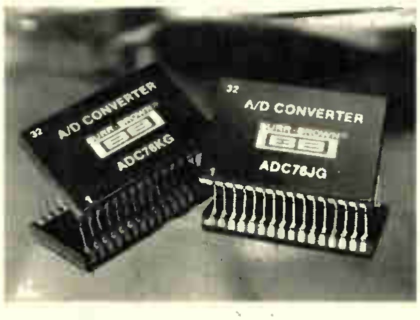
## A-d converter gives 14-bit accuracy, 16-bit resolution

The successive-approximation technique enables the ADC76 analog-to-digital converter to offer 14-bit accuracy with 16-bit resolution for such applications as high-resolution analytical instruments, analyzers, and test instruments. The ADC76 makes 16-bit a-d conversions at a rate of 59 kHz and 14-bit conversions at a rate of 67 kHz, with a maximum full-scale linearity error of ±0.003%. For 14-bit resolution, conversion time is 15 µs.

The device's gain drift is ±15 ppm/°C and its offset drift is ±10 ppm/°C of full scale (bipolar). Performance is specified for 0° to 70°C, with no missing codes from +10° to +40°C. Users can select analog input ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10, and 0 to +20 V.

The complete ADC76 packs a comparator, a clock, a reference, and laser-trimmed thin-film components into a 32-pin bottom-brazed ceramic package. The two available models are the ADC76JG, which offers 13-bit linearity and is priced at $165 in 100-unit lots, and the ADC76KG, a 14-bit linear device, which is priced at $191 in like quantities. Delivery is four weeks after receipt of order.

Burr-Brown, International Airport Industrial Park, Box 11400, Tucson, Ariz. 85734. Phone (602) 746-1111 [385]




## Control or acquisition system offers speech output

Synthesized speech output is just one of the machine-to-operator interfaces possible with the Datalogger 3500, a process-control or data-acquisition system. Users select from a standard 300-word vocabulary to form phrases, and, as a second interface, a built-in cathode-ray tube displays interactive menu programming, data, messages, and graphics for quick data analysis.

The Datalogger offers up to 1,000 analog outputs that provide both 4-to-20-mA and 0-to-10-V dc signals. The output values are computed by a high-speed processor incorporatng algebraic, trigonometric, and logarithmic functions.

An easily interchangeable 3M-DC100A cartridge stores over 6,000 data readings from both the operating system and the application program. Read-after-write techniques ensure the integrity of the cartridge's data. The Datalogger 3500 mainframe is priced under $10,000, with delivery in 8 to 10 weeks.

United Systems Corp., P. O. Box 458, Dayton, Ohio 45403. Phone (513) 254-6251 [384]

## 12-bit d-a converter is packaged for hybrid designers

Available in die form, the HI-DAC801 is the 12-bit current-output digital-to-analog converter that provides the base for such critical hybrid applications as the ADC-80 family or—supplemented by two components—the voltage-output DAC-80 family.

Two laser-trimmed versions are the DAC801A, which accepts a +6.2-V reference, and the DAC801B, which accepts a +10.24-V reference. The d-a converter accepts one of three digital input codes: complementary, complementary-offset, or 2's complement.

Laser-trimmed resistors are provided on chip for use with an external-output amplifier. With an output-current settling time of 260 ns, achieved using dielectric isolation, and a maximum ½-least-significant-bit linearity error at 25°C, the DAC801 is suitable for high-speed successive-approximation analog-to-digital converters.

Priced at $13.69 for 100-unit lots, the converter chip is available from stock.

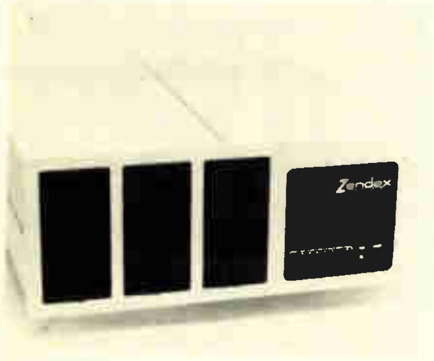
Harris Corp., Semiconductor Group, P. O. Box 883, Melbourne, Fla. 32901 [386]

Microcomputers & systems

# System has hard removable disk

## Storage-drive options for 8085-based system include removable-media Winchester

The 8-bit microcomputer market has matured to the point where systems integration, warranty, availability, and software are key components of the buying decision. Optimizing this critical combination is the ideal of the Quota series 900, a family of 8085A-2- and 8088-based systems from a small systems company in northern California. With prices




ranging from $15,800 to $28,230 in single-unit quantities and with immediate availability, the series 900 competes with 8-bit systems from Cromemco, Altos, and Dynabyte.

The series 900 is a packaged system, including either an 8085A-2–based processor board or two central-processing-unit boards, one with an 8085A-2 and one using an 8088. These CPU boards are packaged with one of three types of hard-disk systems. The first is a Shugart Associates SA1004 8-in. Winchester disk drive that has 11 megabytes of unformatted storage; it is packaged as the model 935 system for the 8085A-2 version and as the model 938 for the version including the 8088 board. These systems also include two Shugart SA801R floppy-disk drives.

The second storage configuration replaces one of the floppy-disk drives with a 10-megabyte removable-media Winchester drive, the DP 100 Lynx drive from Data Peripherals Inc. These systems are designated the model 955, using the 8085A-2 board, and model 958, including the 8088 CPU board.

The third type of storage has no floppy-disk drives. Instead it uses the three 8-in. slots in the system package for one Lynx drive and two Shugart SA1004 drives, thus providing 20 megabytes of fixed storage and 10 megabytes of removable media. If floppy drives are needed with the larger-capacity system, a model 710 or 720 extender chassis can be used.

**Adding memory.** The basic configuration for random-access memory on the 8085A-2 CPU versions is 64-K bytes. Since the system can be multiplexed to support up to eight terminals, however, additional memory is likely to be required. Up to 320-K bytes of this memory can be supplied by a separate card that manages the bank switching of up to five banks of memory, each with 64-K bytes. On the 8088-based system, the basic configuration uses 192-K bytes of memory, but the board has the capability to address up to the 1-megabyte limitation of the 8088.

Both CPU boards contain 4-K bytes of read-only memory, including a 2-K-byte bootstrap routine and a 2-K-byte monitor. This 4-K bytes of ROM does not take up user memory space in normal operation.

The disk controllers for the series 900 systems are the Data Technology DTC-1403D, for the fixed-only storage configurations, and the DTC 900, for the fixed and removable combinations. These provide error checking and correction, overlapped seeks, automatic seek and verify, and an integral data separator.

Pricing, including a one-year warranty, is $14,500 for the system 935, $15,900 for the system 938, $20,500 for the system 955, $21,900 for the system 958, $24,500 for the system 965, and $25,900 for the system 968.

In the first quarter of next year, Zendex will add an 8086-based CPU to its offerings, and in the second quarter the company will add an Intel-based Ethernet board.

Zendex Corp., Quota Systems Division, 6680 Sierra La., Dublin, Calif. 94566. Phone (415)829-1284 [371]

## 5-megabyte disk storage expands Apple's capabilities

A companion to the soon-to-be-delivered 128-K-byte Apple III is ProFile, a self-contained unit featuring an intelligent controller, a 5¼-in. Winchester disk drive, a power supply, an interface card, and driver software. With a 5-megabyte capacity and an average seek time of 95 ms, ProFile brings true data-base-management capabilities to the personal computer.

ProFile has four disk surfaces, two read and write heads, and an actuator mechanism, all integrated in a sealed, protected unit. The intelligent controller ensures data integrity by automatically scanning for errors and relocating marginal data blocks.

ProFile can be used with an Apple III with 128-K bytes of memory and the revised Sophisticated Operating System 1.1. Already being delivered, ProFile sells for $3,495.

Apple Computer Inc., 10260 Banley Dr., Cupertino, Calif. 95014 [373]

## High-speed microcontroller gets in-circuit emulation

Signetics has adapted the microprocessor development system of Tustin, Calif.–based American Automation to support Signetics' model 8X300, a bipolar 8-bit microprogrammed microcontroller. EZ-PRO has two microprocessors, each with its own memory and control circuitry, in a master-slave configuration. In-circuit emulation is provided by the combination of the 8X300's 8-K of memory, the slave processor, and the Address Control Board. EZ-PRO may be configured for as little as $7,495.

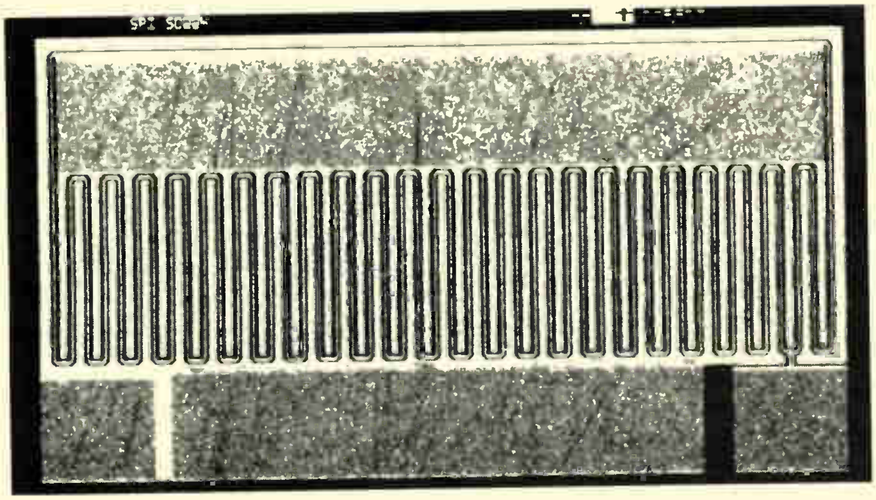
Signetics, 811 East Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086 [377]

Components

# Power FETs gain rf bandwidth

## Lateral design cuts gate capacitance for 2.5-GHz gain-bandwidth product

Semi Processes Inc. is exploiting the lower gate capacitance of lateral MOS field-effect transistors in medium-power devices that switch several times faster than comparable vertical parts. The SD220 product family is made in a diffused lateral process



in which the channel length—and hence the transconductance—is comparable to that of vertical devices. Since the gate overlaps only one highly doped diffusion, the gate capacitance is about half that of vertical transistors with the same on-resistance.

The devices are designed for use in radio-frequency power amplifiers, high-speed switches, and logic-to-high-current interfaces. Their turn-on delay is 2 ns, and they are rated at 60 V maximum drain-source potential. The 220H and 222DC carry typically 0.75 A with a maximum on-resistance of 10 Ω, whereas the 226 is rated for 3 A and 1.5 Ω. With an input capacitance of 12 pF, typically, and a transconductance close to 0.2 mho, the devices' gain-bandwidth product is 2.5 GHz.

"Another key advantage of the lateral process," comments F. Bruce Watson, double-diffused MOS marketing manager, "is that the substrate contact can be brought out in a four-lead package, so the parasitic diode inherent in vertical FETs is eliminated." As a result, a single power transistor can be used as a bidirectional switch.

The devices are available from stock in 100s, at $3.50 for the 226 in a TO-39 package. The 220H is $3, and the 222DC in a TO-72 case is $2.75. All can be supplied in chip form for custom assembly.

Semi Processes Inc., 1885 Norman Ave., Santa Clara, Calif. 95050. Phone (408) 988-4004 [341]

## V-groove laser emits 20-mW continuous-wave power

The CQL 12, a double-heterostructure gallium-aluminum-arsenide laser, employs V-groove technology to produce a 20-mW continuous-wave power output, with a 10,000-h minimum lifetime. The device's light-current output is extremely linear, making it suitable for fast analog optical-transmission links.

Specifically, the laser, which can operate in both the continuous-wave and pulse-code–modulated mode, may be used in fiber-optic links running at up to 520 Mb/s, in digital and analog optical disks, and in laser printers. Unlike many other semiconductor lasers, it is not destroyed at excessive current levels, but keeps a constant power density by increasing its active emission area.

The CQL 12 operates in a single transverse and multiple longitudinal modes. Its beam is nearly totally polarized in the plane parallel to the junction. Available in wavelengths of 780 and 850 nm with a typical spectral half-bandwidth of 2.5 nm, it has a typical threshold current of 100 mA at 25°C. The device is priced at $650 each in quantities of 10 to 49, with delivery from stock.

AEG-Telefunken Corp., Rte. 22, Somerville, N. J. 08876. Phone (201) 722-9800 [343]

## 8- and 16-A rectifiers recover in 35 ns

Switchmode has added to its power-rectifier product line Ultrafast devices that feature a 35-ns recovery time. These 8-A single- and 16-A dual-chip versions in TO-220 packages have an operating junction temperature rating of 175°C.

Primarily for switching power supplies with greater than a 5-V output, the rectifiers may also be used as inverters and protection diodes. The 8-A versions, MUR-805, -810, and -815, are replacements for the European BYW29 series, and the 16-A MUR-1605CT, -1610CT, and -1615CT will replace the European BYV32 series for most applications.

The devices' forward voltage drop is less than 0.85 V at 8 A. The 250-μA leakage current at a 150°C case temperature allows safe operation without fear of thermal runaway. Each 8- and 16-A device is offered in versions with a 50-, 100-, or 150-V peak reverse voltage. The 16-A units have dual-chip center taps.

The 8-A units start at $1.50 and 16-A devices start at $1.90 in quantities of 100 to 999. The 8- and 16-A units run 63¢ and 88¢ in lots of 25,000 or more. Samples are available immediately, with large deliveries taking four to six weeks.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036. Phone (602) 244-4624 [344]

Industrial

## $100 controller has 32 I/O lines

### 6508-based control card's interface chip provides for five interrupt lines, handshaking

By orienting its product strictly as a controller and not a general-purpose computer, by packaging it on a compact 5-by-7-in. board, and by implementing a new three-port interface chip in its design, Commodore Semiconductor has come up with a very inexpensive yet powerful microcontroller. The product is the 6508-1, a $99 microcontroller ($75 in lots of 25) that uses Commodore's 6508 microprocessor, which has the same instruction set as the 6502. In addition, it has 1,280 bytes of random-access memory on board and sockets for up to 16-K bytes of read-only memory or programmable ROM, as well as four 8-bit input/output ports.

This last feature is made possible by Commodore's new 6525 three-port interface chip, which allows the ports to be configured either as 32 I/O lines or as 24 I/O lines with two handshake lines and five priority-interrupt lines, each of which can be individually enabled or disabled. The handshake lines can operate in any of three modes. The first mode consists of simply setting each line high or low under program control. In this mode, the lines can be used to signal peripheral devices that data is available on an I/O port, or that the processor is ready to receive data.

The second mode is used in conjunction with an interrupt line. In this mode, the handshake line goes high automatically whenever its associated interrupt line is activated, and it goes low whenever the processor services the interrupt by reading from or writing to the port. The handshake line is, in effect, toggled by peripheral and processor action.

In the third mode, a pulse is generated on the handshake line whenever the processor reads from or writes to the associated port. The line is normally high, and it pulses low for 1 $\mu s$ when the processor accesses the port. The pulse can be used as a data strobe or as an acknowledgment to the peripheral.

The edge connector interface to the 6508-1 includes the four 8-bit I/O ports, as well as four pins for 5-V dc input power, four ground pins, and a reset line. In addition, the two clock phases are brought to the edge connector in case they are needed for synchronizing peripheral devices to the processor. Delivery is from stock.

Commodore Semiconductor Group, 950 Rittenhouse Rd., Norristown, Pa. 19403. Phone (215) 666-7950 [417]

## Converter hooks to resolver directly

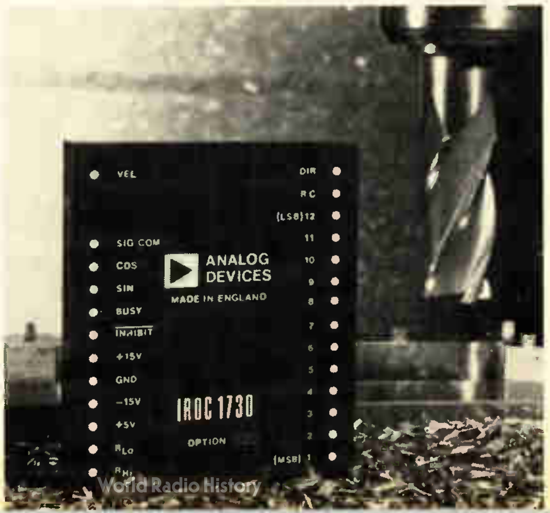
### Isolated resolver-to-digital unit accepts 10-kHz input, can be used with Inductosyn

A tracking converter module from Analog Devices Inc. for position control of robots, machine tools, and process-control equipment, the IRDC1730 translates analog signals from standard resolvers into 12-bit digital data. Besides data conversion, the parallel-output device's internal circuitry handles several related chores that normally require external parts, according to Edward H. Friedman, synchro-converter specialist at the firm.

"As far as I know, we're addressing applications for which there are no competitive devices on the market," Friedman points out. "Designers of positioning systems have been building their own conversion schemes from a variety of parts, for which the IRDC1730 substitutes a single module."

The module interfaces with the resolver, a common position transducer fitted, for instance, on lead screws in machine-tool environments. A central rotor shaft in the resolver rotates in response to machine-tool movement, and the resolver puts out signals with voltages proportional to sine and cosine values of the shaft's angle of rotation.

**Variations.** The converter also works with a variation on the resolver, Farrand Controls Inc.'s Inductosyn. Linear and rotary Inductosyns, according to Friedman, are the most accurate and widely used position transducers for numerical-control and machine-tool applications. The device consists of a slider and a scale. These inductively coupled parts bear printed-circuit tracks formed in continuous rectangular waveforms. The scale attaches to the axis where position measurement takes place and the slider moves with the device being measured. The Inductosyn's output represents the sine and cosine of the distance moved by the slider through any waveform cycle, or pitch, on the scale.




The IRDC1730 accepts resolver or Inductosyn signals at input frequencies of 400 Hz or 2.6, 5, or 10 kHz. Transformer-isolated to 500 V, these inputs can be received by the converter as voltages of 2.5 V rms, but the IRDC1730 permits external resistive scaling for interfacing with any resolver or Inductosyn.

Each 12-bit word generated by the IRDC1730 expresses a sine-to-cosine ratio rather than an absolute amplitude, thus canceling out the effect of noise or of voltage drops between transducer and converter, Friedman notes. The converter's 12-bit resolution divides a resolver's full 360° revolution into 0.0879° intervals, or an Inductosyn's standard 2-mm pitch into 0.5-$\mu$m steps.

**Tracking.** Maximum tracking rate (at 5- and 10-kHz input frequencies) is 170 revolutions or 170 pitches per second. At that rate, accuracy is ±14 min of arc; accuracy increases to ±10.5 min at one-half tracking speed. Maximum bit-update rate is nearly 700 kHz.

The IRDC1730 tracks continuously using a type 2 servo loop, in which a second integrator automatically compensates for following errors at high speed by maintaining a zero-position-error output to a voltage-controlled oscillator. The converter's output includes a dc voltage proportional to the rate of change in a position. This signal provides feedback for loop stabilization, without the need for bulky external tachometers, says Friedman.

The IRDC1730 also puts out a signal indicating the direction of a resolver's rotation. A ripple clock tracks the number of completed revolutions or pitches by emitting a pulse each time the converter's output passes through electrical zero.

Packaged in a module only 0.4 in. high, the IRDC1730's low profile allows mounting in standard card cages; the converter module measures 3.125 by 2.625 in. The unit operates at from 0° to 70°C or from −55 to +105° C. It runs on +15-, −15-, and +5-V power supplies, typically drawing 1.33 W. It sells for $255, with quantity discounts available. Delivery is from stock.

Analog Devices Inc., Route 1 Industrial Park, Box 280, Norwood, Mass. 02062. Phone (617) 329-4700 [411]

## Distributed processing system controls up to 254 elements

The Westinghouse Distributed Processing Family (WDPF), for steel mills, power plants, and other complex industrial applications, allows as many as 254 microcomputers to be connected to it by way of a data highway system. This data highway setup makes the WDPF 10 times faster than other systems used at present, according to its manufacturer. It can broadcast up to 10,000 data variables and 6,000 messages every second and provides the plant operator with up-to-the-second process information from anywhere in the mill or plant.

The WDPF includes a 16-bit microcomputer at each highway unit to control, scan, monitor, and compute and report data through color graphics implemented on cathode-ray tubes or printers.

Other features include a high-level language that provides a simple, direct means for developing and loading control logic, graphic process diagrams, and log reports; components that use the same hardware, thereby reducing the cost of installation, maintenance, spare parts, and training; an independent drop to handle short- and long-term data storage and on-line retrieval; and separate data-computing drop, programmed in a high-level general-purpose language (as are the individual microcomputers) to perform system-wide complex calculations.

Westinghouse Electric Corp., Industry Systems Division, 200 Beta Dr., Pittsburgh, Pa. 15238 [412]

## Unit prevents brownouts in response to radio signal

Using the R703 smart duty cycler, developed by Honeywell's Energy Products Center, utility companies now have the ability to prevent brownouts and blackouts. The microprocessor-based device stops air conditioners from increasing their energy consumption levels if temperatures continue rising. According to the manufacturer, the unit is expected to reduce electricity demand by 15% to 30%.

The R703 is activated by a radio signal transmitted by the public utility. A similar signal is used to deactivate the device as soon as the critical period has ended. The unit can be installed outdoors on air conditioners of both residences and small commercial buildings.

It sells for $175 in quantities of 25 to 999 or as little as $97.50 in lots of 10,000. Delivery takes six weeks.

Honeywell Inc., 10400 Yellow Circle Dr., Minnetonka, Minn. 55343. Phone (612) 931-4396 [414]

## Motor and amplifier are geared for robotics uses

The International Scientific Industries Inc. has introduced two new products to the robotics industry, a brushless dc motor and an amplifier. The motor uses high-energy cobalt magnets and is offered either as rotor and stator components or as a unit packaged with a standout output shaft containing position- and velocity-feedback devices with or without brakes and reducers. Prototype quantities of devices with peak torques from 30 to 18,000 oz-in. and with outside diameters ranging from 1.4 to 5.0 in. are available in 30 days, priced from $300 to $700.

The amplifier is designed to drive the motor and is configured to produce either a six-switch square-wave three-phase output or three-phase sinusoidal outputs with a frequency range from 0 to 200 Hz. The units have static stiffness up to 10,000 ft-lb/radian and dc forward gain up to $10^6$ with no deadband. They are available in four to eight weeks in prototype quantities ranging in price from $400 to $1,200.

International Scientific Industries Inc., 135 Scattergood Dr., Christiansburg, Va. 24073. Phone (703) 382-1473 [415]

Communications

# Light source tests with pulses

## Low-cost fiber-optic generator has output variable to 100 $\mu$W, pulsing at 5 to 100 kHz

The Fotec S fiber-optic signal source enters a low-cost market consisting in main of dc optical sources. The Fotec source's output is a digitally generated square-wave pulse train with a 50% duty cycle. That makes it able to test not only for cable attenuation, but also for splice or connector loss, receiver sensitivity, and satisfactory transmission over data links using repeaters. The pulse energy needed to trigger a receiver or repeater, both of which normally ignore dc input, can be determined using the unit.


"The Fotec S is an optical analog of electrical pulse generators, and designers and field-service technicians can use it as easily as they do electrical test equipment," asserts company president James E. Hayes. When equipped with a fiber-optic converter such as the Fotec C, an optical receiver with a linear electrical output, it can work with power meters, digital multimeters, photometers, X-Y recorders, and data-acquisition equipment.

**Wavelength options.** Driven by an internal oscillator, a light-emitting diode in the standard Fotec S model produces light with a 940-nm wavelength. Wavelengths of 700, 820, and 880 nm are optional. Employing front-panel potentiometers, users can vary output amplitude over a 150:1 range and output-pulse repetition rate from 5 to 100 kHz.

A single BNC connector on the Fotec S can also link the devices to an external pulse generator, which then can control both pulse width and frequency. Output frequency under external control can range from dc to 100 kHz. When the Fotec S is operating independently, the BNC connector functions as a pulse output to oscillators or frequency counters, with which the pulse rate can be measured.

Set at maximum power, the Fotec S can couple 100 $\mu$W average, 200 $\mu$W peak, into a 1,000-$\mu$m fiber. The unit measures 1.5 by 3.0 by 5.25 in. and weighs less than a pound. Further enhancing its portability is its availability in both an ac-only model and a rechargeable-battery model (which can also run on ac line power).

The Fotec S is priced at $295 to $375, depending on model and connector type. Delivery is from stock to four weeks.

Fotec Inc., Box 246, Boston, Mass. 02129. Phone (617) 242-0863 [401]

## Device gives computers access to TWX, Telex

Dispensing with hardware and software considerations, the Telex-Plug connects any computer with the Western Union Telex network as well as with other common carriers, so that users may send and receive messages directly through their word processor or computer. Placed between a word processor or computer and a printer without tying up a communication port, the Telex-Plug listens for activating codes that indicate a message is available to send.

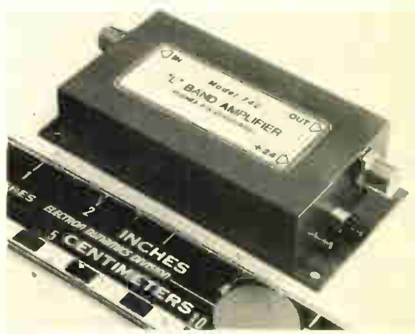
The unit dials, establishes a connection, and sends the message, returning answer-backs or busy signals. The host is responsible only for sending a block of text, including the telex number of the destination; the Telex-Plug handles the rest.

If the host is unattended or involved with other tasks, the unit will sense an incoming message and automatically store it or route it to the printer. In January, an $800 option that is retrofittable will provide message coding and decoding according to the data-encryption standard. The basic unit can be delivered 30 days after receipt of order and sells for $1,700.

Teleface Corp., 176 Ludlow St., New York, N. Y. 10002. Phone (212) 477-6802 [403]

## Amp lets satellite receiver be ½ mile from antenna

The IFLA 463 post-amplifier is for use in satellite video receiving terminals where the antenna must be



located at distances of up to ½ mile from the receiver electronics. The unit operates over a frequency range of 950 to 1,450 MHz and has a 40-dB gain and a 5-dB noise figure.

The model IFLA 463 is compatible with Hughes' model SVR 463 receiver and other block downconversion receivers using the 1-GHz interface. It is available as a single unit or as part of a redundant panel with single or redundant power supply. Delivered from stock, the amplifier sells for $600.

Hughes Microwave Communications Products, P. O. Box 2999, Torrance, Calif., 90509. Phone (213) 517-6100 [404]

## Bidirectional T-splitter keeps crosstalk below 30 dB

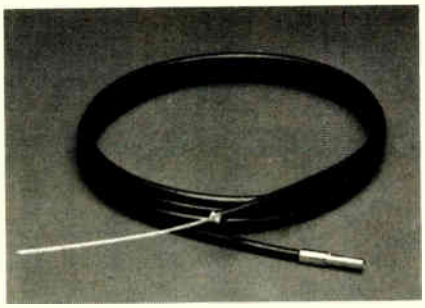
Suitable for developing loop networks, single-fiber multiplexing, and branching with graded-index fibers, the bidirectional optical T-splitter employs advanced proprietary technology featuring low excess losses. Supplied with either 50-, 62.5-, or 100-μm fiber core diameter, the TSI-1 provides a nominal 1:1 splitting ratio of the input signal with crosstalk below 30 dB. Other splitting ratios, such as 10:1 are also available.

Housed in a 100-by-60-by-16-mm aluminum casing that weighs 0.1 kg, the splitter is supplied with unterminated fiber pigtails 50 cm long. The TSI-1 operates over the −20° to +70°C temperature range in 0% to 95% humidity. The unit sells for $225, with delivery from stock to eight weeks.

Plainview Electronics Corp., 28 Cain Dr., Plainview, N. Y. 11803. Phone (516) 249-6677 [408]

## Refraction lens reduces collimator's insertion loss

The Selfoc micro lens, a graded-index-of-refraction lens with which a variety of optical characteristics can be obtained, forms the heart of an optical collimator and an electrical-



to-optical converter.

The collimators in the OPCL 56 series have both optical axes of a fiber and a Selfoc micro lens aligned. With this coupling, a typical insertion loss for a lens separation of less than 20 mm is less than 2 dB, and for a 50-mm lens separation, it is less than 4 dB. The OPCL assembly is available in one graded-index fiber (OPCL-5G) and two step-index fibers (OPCL-10A and OLCL-20H). The numerical apertures for these fibers are 0.19°, 0.28°, and 0.50°, and the divergence angles are 1°, 2.5°, and 5° respectively. On small orders, the collimator prices range from $65 to $110.

The electrical-to-optical converter consists of a light-emitting diode and a step-index-of-refraction fiber. The six standard devices available afford a variety of output power levels and terminations. Typical output power ranges from 80 μW to 1 mW. The converter series varies in price from $240 to $290. Delivery on either item is five to six weeks.

NSG America, 136 Central Ave., Clark, N. J. 07066. Phone (201) 499-0939 [406]

## Optical receiver has threshold of 1 μW/cm² in full sunlight

The TD200 optical receiver detects the threshold of pulsed lightwave radiation, producing standard TTL outputs from optical inputs of less than 1 μW/cm². Threshold sensitivity is a function of pulse width: at a pulse width of 150 ns in full sunlight, the unit's threshold power is 1.0 μW. Its relative sensitivity peaks at about 0.9 μm, but sharp cutoff filters for enhanced sensitivity at shorter wavelengths to 0.79 μm are available.

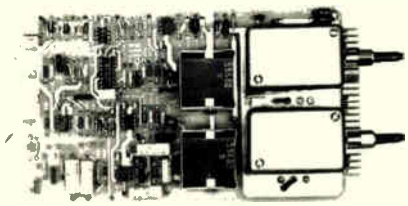
The TD200 module contains an electromagnetic interference shield, wide field-of-view optical filter, and the necessary signal-conditioning circuits in a stainless steel, hermetically sealed package. It employs a photodiode 1 cm² in area, a transimpedance amplifier, a video amplifier, and a comparator. The module has three pins—B+, ground, and output.

A single +12-V supply powers the TD200, which operates from −35° to +75°C. Its current drain is 16 mA in full sunlight. In 100s, it is $186, with delivery from stock.

Meret Inc., 1815 24th St., Santa Monica, Calif. 90404. Phone (213) 828-7496 [405]

## Narrow-bandpass filter enhances signal-to-noise ratio

The model 67 fiber-optic audio link can be used to interface audio signals from a frequency-shift transmitter-receiver terminal or voice with a four-wire optical cable. With high- and low-pass filters, the circuit may



respond at 300 Hz to 4 kHz, but without filtering, it may achieve a response bandwidth extending from 5 Hz to 100 kHz.

The predistortion circuit and the 300-Hz-to-4-kHz narrow bandwidth enable the audio-tone, transfer-trip system to operate over 55 dB of optical-cable system losses and still maintain an 18-dB signal-to-noise ratio. The link operates directly from an internal ±12-V dc power supply and may be used either to dedicate one channel or to multiplex several channels. The unit operates from −20° to +60°C and has built-in line-surge protection. The model 67 sells for $600 and is available 30 days after receipt of order.

RFL Industries, Powerville Road, Boonton, N. J. 07005. Phone (201) 334-3100 [407]

# Products Newsletter

**Separator enables 5¼-in. Winchester to store 27 megabytes**

Look for the capacity of 5¼-in. Winchester disk drives to extend to 27 megabytes with the introduction of a four-platter drive and data separator from Rotating Memory Systems Inc. of Milpitas, Calif. The basic drives have unformatted capacities of 4.5, 9, 13.5, and 18 megabytes for the one-platter to four-platter versions, respectively. But **the Data Express II, a $250 optional data separator, increases capacities by 50%.** It also boosts the data-transfer rate to 7.5 MHz using a controller chip set that RMS offers for $60. Models 504, 509, 513, and 518 will be delivered in January, with 100-unit pricing at $910, $1,140, $1,305, and $1,460.

**Microwave plug-in sweeps wide range**

To achieve its widest-range sweeper yet—from 10 MHz to 26.5 GHz—the model 83595A from **Hewlett-Packard combines heterodyne and multiplication techniques using a 2-to-7-GHz yttrium-iron-garnet oscillator.** The $27,000 unit, which plugs in to HP's 8350A mainframe, mixes YIG- and cavity-oscillator outputs to obtain its low-band sweep of 10 MHz to 2.4 GHz. Then it amplifies, multiplies, and filters YIG oscillator harmonic frequencies to obtain the higher bands.

**Color graphics enhances CAD system**

The PC-800 color-graphics option from Gerber Scientific Instrument Co., Hartford, Conn., upgrades the PC-800 system by helping designers differentiate among the layers of multilayer boards. **The color-graphics package uses a 19-in. cathode-ray tube with seven-color display ability** (blue, red, cyan, yellow, green, white, and magenta). The price is $12,000 and delivery takes 90 days.

**Add-in memory doubles 3031 storage**

With the Stor/3000 Mod 31E from Cambex Corp., Waltham, Mass., users can increase the main-memory capacity of IBM 3031 computers to 16 megabytes—twice the physical-memory limit announced for that machine by IBM and equal to its virtual-memory capability. **The key is 64-K memory chips,** according to the company, making possible memory cards eight times denser than IBM's. Each megabyte sells for about $30,000—approximately 60% of IBM's price; delivery takes 60 days.

**Nonvolatile RAM is word-alterable**

NCR Corp.'s Microelectronics division, Dayton, Ohio, is adding the NCR7033 to its p-channel metal-nitride-oxide-semiconductor nonvolatile random-access memories. Words can be altered in the 21-by-16-bit part, which is built under a cross-licensing agreement with Nitron Inc., Cupertino, Calif., and **priced at about $1.95 in 10,000-unit quantities.** Samples will be available in January, with production in March.

**Xerox 820 is given software support**

Unveiled at last week's Comdex show in Las Vegas by Digital Research Inc. of Pacific Grove, Calif., were a number of software offerings targeted at the Xerox 820 personal computer. They include CBasic, a Basic language compiler and interpreter, **as well as CB-80, a much faster compiler version of the CBasic program.** Also included is the PL/1-80, based on the ANSI subset G of PL/1 and compatible with minicomputer and mainframe environments. Deliveries begin next month and exact pricing is forthcoming.

# Career outlook

## The numbers game

Whether the publicized engineer shortage really exists now in the early stages of recession is a pointed question even for electrical engineers with stable jobs. As a practical matter, company planning and new programs often hinge on the availability of people in the job market, not to mention raises and promotions. So the opinions of a veteran with a longer perspective on this "numbers game" could be illuminating.

The bedrock advice of Robert J. Kuntz is that all predictions about critical shortages of engineers should be viewed skeptically—and his experiences stretch back into the 1960s. As executive director of the nonprofit California Engineering Foundation, he often grapples with the numbers game riddle in working toward a goal of improvements in engineering education.

"We don't have to go back very far in the past to see the trouble this numbers game gets us into," he notes. In 1968, for example, the goals study on engineering education, sponsored by the American Society for Engineering Education, predicted a shortfall of nearly 300,000 engineers by 1975. Six months later, however, then-President Richard M. Nixon chopped Federal research and development by 30%. "Suddenly, there were over 100,000 engineers unemployed and another 200,000 underemployed," says Kuntz. The job market for EEs stayed flat for many years, not really taking off until the end of the 1974–75 recession.

"It's clear the engineering job market responds more closely to Federal spending than to the economic cycle," he warns. This is a fact often misunderstood or not recognized, as was the case during the most recent boom. Kuntz's advice is that another cycle of Federal budget cutting is starting, so even previously high-demand EEs could see opportunities dry up faster than anyone expected.

Kuntz's organization, based in Sacramento, believes "the real problem in engineering is qualitative, not quantitative" and has a program to deal with it. This week, the foundation convenes a two-day conference of California leaders in industry, engineering education, and Government to hammer out a consensus on specific improvements that can be made in training undergraduate engineers. While representatives of the three groups often call individually for such things as much more laboratory experience for engineering students and voice them in trade associations, no substantial changes have taken place.

**Face to face.** "There has been very poor communication between the parties responsible," Kuntz continues. "Solutions can best be effected by bringing together the decision makers, and that's what the conference will do."

The goals of the Pomona, Calif., conference are not just to map changes in engineering education, but to provide a working framework for continuing the upgrading.

In this direction, the conference will address some pertinent questions and present some leaders in the fields of Government, engineering, and engineering education. For example, F. Allen Cleveland, Lockheed Corp.'s corporate engineering vice president, will deliver the keynote address from industry, "Industries' Perspectives on Engineering Education." Looking at the problem from the universities' side will be Warren Baker, president of California State Polytechnic University at San Luis Obispo, with "Educational Institutions' Perspectives on Engineering Education." In addition, there will be work sessions covering undergraduate curricula; faculty development, laboratories, technology, and applied education; and administration and finance of education.

The foundation itself will serve to coordinate an ongoing program, which if successful can serve as a model for other states or regions, Kuntz points out. Strong support from California electronics and aerospace firms looks certain in view of the number of top-level engineering and personnel officials already committed to attend. **-Larry Waller**

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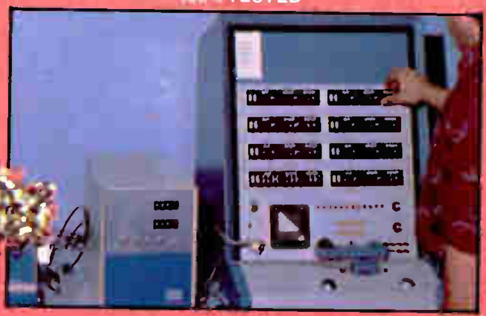

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