Asymmetrical Parasitic Inductance Utilized for Switching Loss Reduction in Power Modules

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High efficiency of power conversion circuits is a design goal on its own. At the top end competing solar inverter manufacturer to develop the most efficient topologies using components with the lowest power dissipation. But high efficiency is also the key for other approaches. The reduction of switching losses is the basis for higher switching frequencies which lead to a reduction of the size and weight of the passive components. The improvement from 96% to 99% efficiency will reduce the effort for cooling by factor four. It is obvious that high efficient circuits are the smartest way to achieve compact design and highest power density. With the utilization of parasitic inductance and consequent execution of basic rules of power electronics is a new power electronics solution based on standard Si components disclosed which extends the traditional designs. The presented new power module concept combines a low inductive turn off with the utilization of the parasitic inductance for a reduction of the turn on losses and the usage of three level switching circuits with the paralleling of fast switching components with components with low forward voltage drop.

1 Introduction

The goal of this development project is the reduction of switching losses in power applications >100kW with screw type modules. The limitations in such applications are mainly parasitic effects as stray inductance [7][8] and reverse recovery behavior of the diodes [5]. The overvoltage spike caused by the parasitic inductance will limit the turn off switching speed. The losses and the increased electromagnetic influence (EMI) caused by the reverse recovery behavior of the freewheeling diode is the drawback for increased turn on switching speed. In a first step, the parasitic inductance is reduced to a minimum to solve the issue with turn-off. In a second step are the turn on losses reduced. This is achieved with the utilization of the parasitic inductance for turn-on by keeping the low inductive turn-off behavior. The third activity for a switching loss reduction is the introduction of a neutral point clamped (NPC) inverter topology. Finally a special topology for paralleling MOSFET with IGBT is introduced to show the advanced prospects of the idea. The feasibility of the new concept is proven with a power module concept incorporating all the discussed arrangements.

2 Theory about Switching Losses (Inductive Load)

The power dissipation in power electronics is caused by conductive losses and switching losses. The conductive losses are defined by the forward voltage drop in the semiconductor. The switching losses are dependent on:

- the switching speed of the transistor
- the reverse recovery behavior of the diode
- serial inductance
- additional parasitic effects

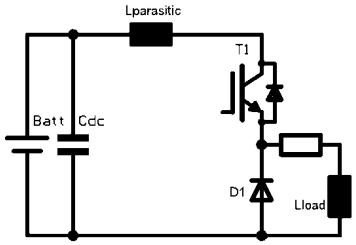

Figure 1: switching circuit with inductive load

2.1 Turn-On

In a system with inductive load (see Figure 1) is the freewheeling diode conducting at turn on and the output voltage equals the negative DC-bus voltage (DC-). The transistor starts now to conduct. As soon the transistor takes over the complete output current, the output voltage will develop to the positive DC-bus voltage (DC+). The diode faces reverse voltage and will conduct in reverse direction. This will cause losses in the diode (E_{REC}) and it will increase the current in the transistor. This current peak is often the root cause of EMI in the system. After the diode is completely recovered and blocking, the current in the transistor will fall back to the level of the output current. The turn-on process is now complete. An increased serial inductance with the transistor will reduce the turn on losses. The energy stored in the serial inductance is calculated according [9]:

$$E_L = ½ * L * I^2$$

2.2 Turn-Off

At turn off will the voltage at the transistor develop up to the DC-bus voltage level. The diode will take over the output current. The overvoltage will cause additional losses and it endangers the transistor to be destroyed. The usage of fast transistors is limited on the inductance and the maximum current, as the voltage peak is dependent on

the turn off speed. The stored energy in the serial inductance of the DC-input causes a voltage overshooting according [1]: $\mathbf{V_{CE}(peak) = V_{CE} + L \times di/dt}$

3 Low Inductive Module Technology

With the new low inductive module technology [3] we achieve:

- Fast and reliable turn-off of high current power modules
- Switching loss reduction (turn off)
  The reduced voltage overshot at turn off allows the usage of fast components.

The reduced inductance will not reduce the switching losses at turn-on. The turn-off losses will decrease but the turn-on losses of the transistor and the reverse recovery losses in the diode will increase even more [4]. The efficiency of low inductive circuits will increase with the utilization of fast components. The goal of low turn on losses without increasing EMI requires ultra fast freewheeling diodes.

4 Asymmetrical Inductance

Increased inductance at turn on and ultra low inductance at turn off is the new goal. This approach is named "Asymmetrical Inductance". The way to achieve the new switching behavior, is the utilization of the parasitic inductance $L_{parasitic}$ at turn-on and bypassing it during turn-off. The diode D_{tran} (see Figure 2) assigns the stored energy of the parasitic inductance during turn off to the integrated capacitor C_{tran}.

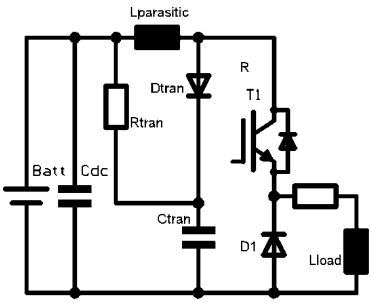

Figure 2: Asymmetrical Inductance in a switching circuit with feedback to the main DC-link.

The stored energy circulates in $L_{parasitic}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. With this circuit we are able to release the semiconductor from switching losses but some energy has to be dissipated in passive components. The regeneration of the stored energy with a DC-DC circuit (see Figure 3) is an option to increase the efficiency.

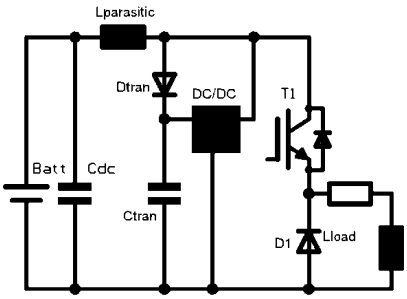

Figure 3: Asymmetrical Inductance in a switching circuit with regeneration of the stored energy.

4.1 Verification of the new Idea of Asymmetrical Inductance

The idea is verified with the comparison of different parasitic inductance on a traditional power module setup and asymmetrical setup with integrated snubber capacitors.
Test conditions:
$R_G = 2\Omega$ (+/- 15V), $V_{DC} = 600V$, $I_{OUT} = 400A$
Component: Infineon HS 3 / 1200V / 400A

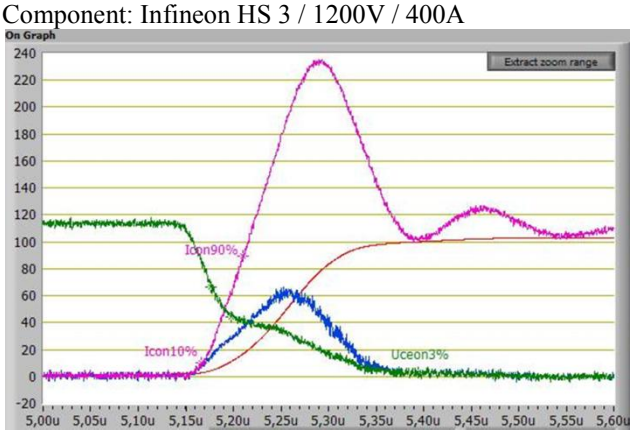

Figure 4: IGBT-Turn-On characteristics with symmetrical inductance. L[ON] = L[OFF] = 50nH

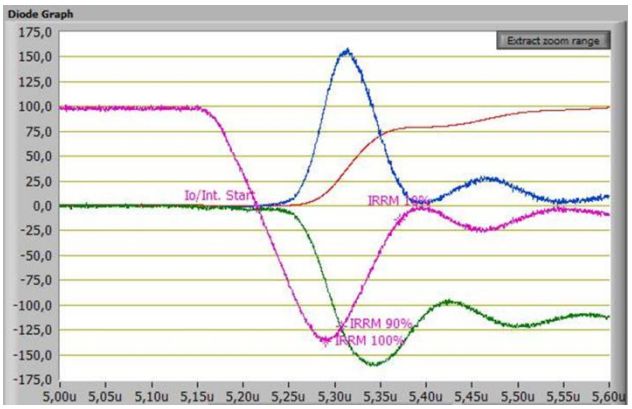

Figure 5: Diode-characteristics with symmetrical inductance. L[ON] = L[OFF] = 50nH

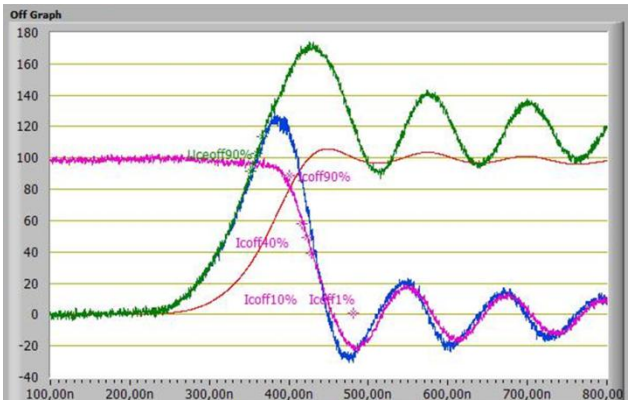

Figure 6: IGBT-Turn-Off characteristics with symmetrical inductance. L[ON] = L[OFF] = 50nH

Results:
E_{ON}=16,92mJ, E_{OFF}=27,78mJ, E_{REC}=31,78mJ
The switching losses are fine but more important is the voltage overshooting at turn off. The most critical case is turn-off at low temperatures. At 25°C is an overvoltage of ca. 180% measured which limits the usage to 650V. Save turn off at over current conditions is not anymore possible. In our test the module failed at 720A / 600V / T_J=25°C.

The identical measurement is now performed with asymmetrical inductance of 50nH at turn on and 5nH at turn-off:

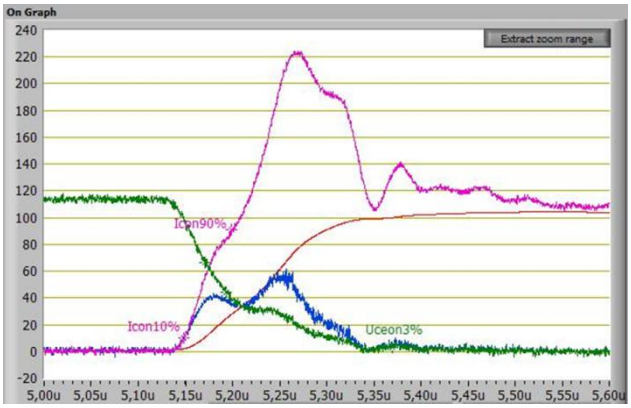

Figure 7: IGBT-Turn-On characteristics with asymmetrical inductance. L[ON] = 50nH, L[OFF] = 5nH

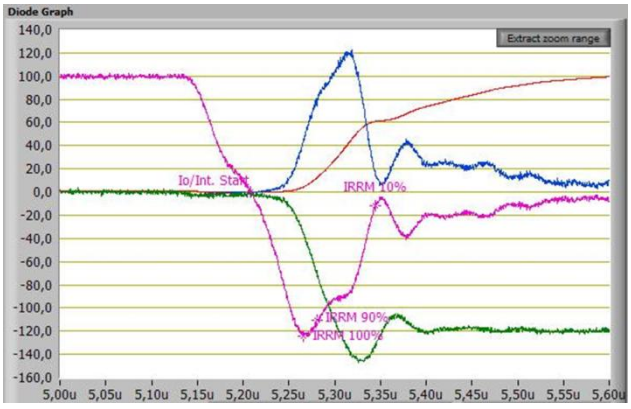

Figure 8: Diode-characteristics with asymmetrical inductance. L[ON] = 50nH, L[OFF] = 5nH

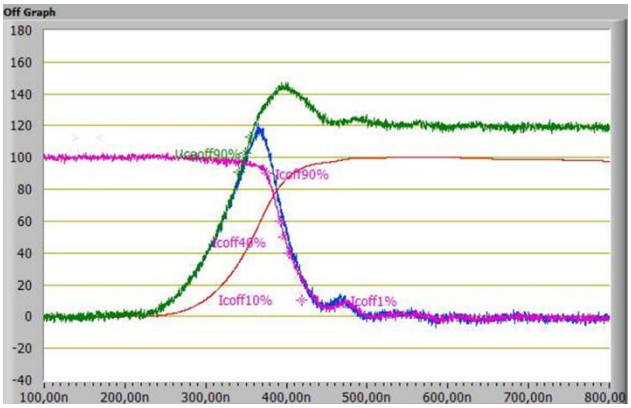

Figure 9: IGBT-Turn-Off characteristics with asymmetrical inductance. L[ON] = 50nH, L[OFF] = 5nH

Results:
E_{ON}=15,487mJ, E_{OFF}=25,66mJ, E_{REC}= 28,27mJ
The switching losses of the new asymmetrical setup are lower. Surprisingly are not only the turn off losses reduced, all switching losses are reduced. The reason for the turn on loss reduction is the reverse recovery behavior of the circuit. At turn on is the current of the transistor T_1 increased by the reverse recovery current through the diode D_1. After completed recovery is the current reduced but in the parasitic inductance $L_{parasitic}$ is the additional energy stored which causes an overvoltage at the collector of the transistor compared with the positive voltage in the transient capacitor $C_{tran.}$
=> The energy will flow into the capacitor.
This will reduce the reverse current in the diode and the voltage drop in the transistor which results in a significant reduction of the switching losses.

With the asymmetrical inductance circuit, it is possible to increase the inductance further to take advantage out of the turn-on loss reduction.
In a setup with $L_{parasitic}$[ON] = 90nH, $L_{parasitic}$[OFF] = 5nH
We get the following results:
E_{ON}=12,44mJ, E_{OFF}=25,77mJ, E_{REC}=26,70mJ

4.2 Advantages of the Asymmetrical Inductance

- Superior switching performance with standard components:
  The new circuit improves the efficiency without investing in special components. It is possible to reduce the switching losses with standard components.
- Reduced EMI:
  The increased turn on inductance reduces the peak current in the transistor. This is the major source of EMI.
- No bus bars required:
  Inductance in the DC-input is now welcome and will cause a further loss reduction at turn-on. In consequence the expensive laminated bus bars for a low inductive connection with the DC-capacitor bank are not required anymore. This might be the most significant advantage of the new approach.

- Reduced voltage swing of the onboard capacitors. The onboard capacitors will not get discharged during turn on, the voltage swing and the dissipation in the capacitors is reduced.

5 Decoupling of Upper and Lower Transistor

This following circuit (see Figure 10) is a solution for reducing the turn-on losses due to the output capacitance of the complementary switching device and the elimination of cross conduction during turn-on. The goal of this idea is the decoupling of the output transistors. In the following circuit is the output divided into two branches and the parasitic inductance of the output connection is utilized to decouple the components. The corresponding diodes are direct connected for achieving a low inductive commutation loop.

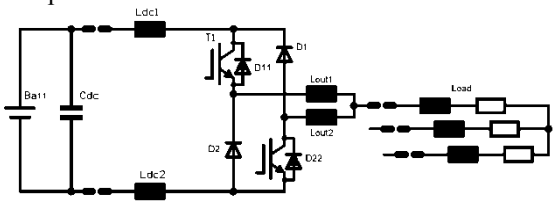

Figure 10: Pseudo half bridge topology with decoupled branches for improved switching behavior

6 Multi Level Topology

The usage of multi level topology as neutral point clamped inverter (NPC) or mixed voltage NPC inverter cuts the voltage at the switching transistor into half which reduces the switching losses accordingly [2]. On top on this loss reduction have the freewheeling diodes to be sized only for half of the voltage e.g. 600V instead of 1200V. But for 600V are many components with ultra fast reverse recovery behavior available.

7 Advanced Paralleling

The target is to merge the advantages of:

- Standard NPC.
  In the NPC topology are components with the half voltage rating required. At low voltage are faster components available.
- Mixed voltage NPC [6] (see Figure 11: Mixed voltage NPC circuit). The output current faces only one junction, this leads to reduced static losses.

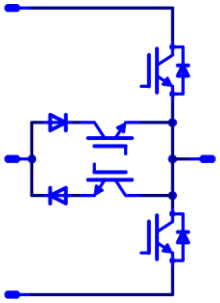

Figure 11: Mixed voltage NPC circuit

- Parallel Switch:
  This is the paralleling of a fast component (e.g. MOSFET) and a component with low voltage drop (e.g. IGBT). The loss reduction is achieved by rendering the static losses of the switch to the IGBT and the dynamic losses to the MOSFET. Even smarter is to use a so called mixed voltage NPC topology and to parallel with just 600V MOSFET´s a 1200V IGBT (see Figure 12).

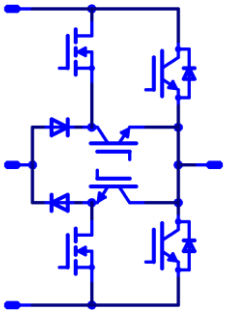

Figure 12: Advanced paralleled NPC circuit

7.1 Function

In the advanced paralleled NPC is the original idea of paralleling MOSFET with IGBT maintained (see Figure 13). The MOSFET and the IGBT are turned on simultaneously. The MOSFET as the faster device will take over the current at turn on. The IGBT will turn on with zero voltage. The voltage drop in the IGBT is lower so the IGBT will take over the major share of the current. At turn off is the gate signal of the MOSFET delayed. The IGBT will turn off, the MOSFET will take over the current and will turn off with a delay of some 100ns.

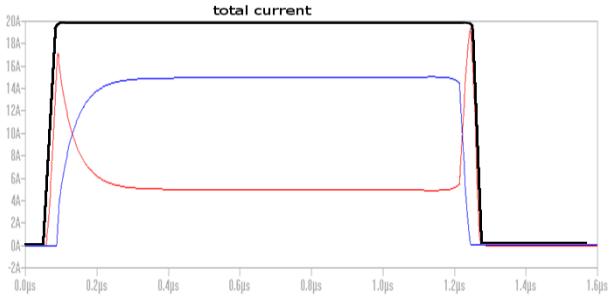

Figure 13: current sharing in the parallel switch system. Current in the MOSFET (red), current in the IGBT (blue)

7.2 Performance Verification of the Advanced Paralleled Topology

The measurements are showing that the advanced paralleled NPC topology is able to cut the switching losses into half.

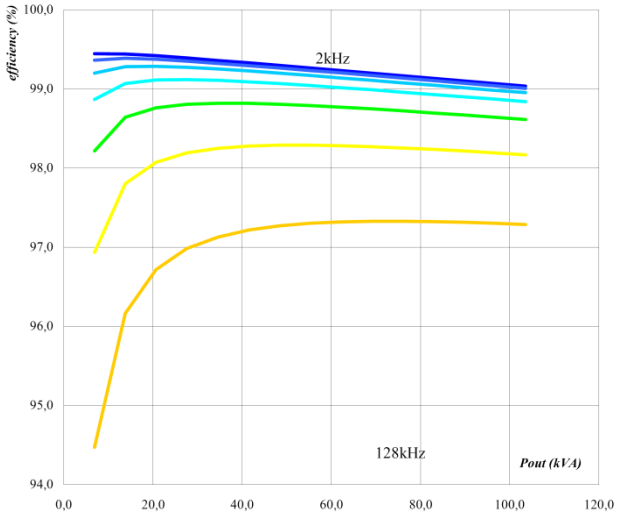

Figure 14: Advanced paralleled NPC: Efficiency vs. switching frequency in steps from 2kHz to 128kH doubling in each step – 2 (blue), 4, 8, 16, 32 (green), 64 (yellow), 128kHz (orange)

The inverter reaches now more than 99% efficiency with a PWM switching frequency of 16kHz. At 64kHz switching frequency is the efficiency still above 98% (see Figure 14)!

7.3 Advantages of the Advanced Paralleled NPC Topology

With the advanced paralleled NPC topology it is possible to cut the switching losses into half compared with mixed voltage NPC.

8 Power Module Definition

The combination of all this ideas leads to the following power module specification:

- 200kVA output power at 20kHz
- Asymmetrical parasitic inductance with energy regeneration.
- Decoupling of low side and high side switches.
- Three level topology
- Paralleling of fast MOSFET or IGBT´s with components having low static losses

9 Power Module Concept

- 1200V/500A power rating
- Asymmetrical parasitic inductance with onboard snubber capacitors (5nH turn-off inductance) and DC-DC regeneration circuit
- Separated outputs for high- and low-side circuit for decoupling of the corresponding switches.
- 3 phase advanced paralleled mixed voltage NPC topology.

The result is shown in Figure 15 and Figure 16. The inductance shown in the schematics is the parasitic inductance of the power module setup.

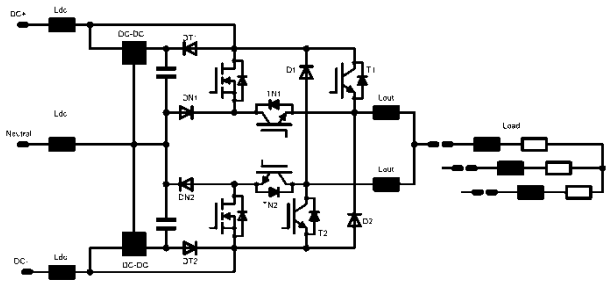

Figure 15: Power module concept for a 3 phase advanced paralleled NPC with asymmetrical inductance and regeneration circuit.

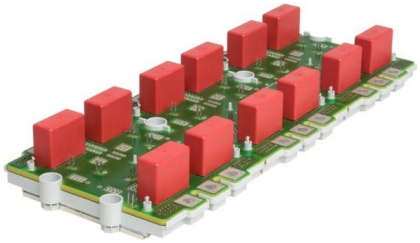

Figure 16: Power module with integrated snubber capacitors and asymmetrical inductance.

10 Conclusion

Beside the advantages of new technologies as SiC or GaN switching components it is still possible to increase the efficiency with standard Si Components. To extend traditional power designs we have to remember the basics of power electronics.

- The low inductive module concept ensures the fast and reliable turn-off in high current power modules and reduces the voltage overshot.
- The power module setup with very low internal parasitic elements it is able to utilize the external stray inductance for a reduction of switching losses without investing in expensive high-speed semiconductor technology. The asymmetrical inductance leads to lower switching losses, reduced EMC and minimized effort for the inverter mechanics. Low inductive bus bars are not needed anymore. A flexible low cost cable connection in the DC link can be used. The increased serial inductance will just cause additional reduction of the turn-on losses.
- The parallel switch technology achieves highest efficiency at elevated switching frequencies of 50kHz and more.

11 References

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