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Datasheet

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# UFirebird-UC6226

## GNSS Positioning Chip

# Contents

# Revision History

| Version | Revision History | Date |
|---|---|---|
| Ver. 1.0 | First Edition | Aug. 2017 |
| Ver. 2.0 | Add WLCSP | April. 2019 |
| R3.0 | Two options of VDDIO input voltage are clarified is chapter 10.4 | Oct. 2019 |

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# Foreword

This <User Manual> offers you information in the features of the hardware, the installation, specification and use of Unicore UC6226 product.

**Readers it applies to**

This <User Manual> is applied to the technicists who know GNSS Receiver to some extent but not to the general readers.

Chapter 1

# 1. Functional Characteristics

## 1.1. Overview


QFN40 WLCSP

Figure 1-1 UFirebird-UC6226 chip

Unicore UFirebird™ (UC6226) is designed with 28nm process and efficient PMU, features low power consumption and ultimate compact size, which significantly increase the battery life of user equipment.

UC6226 is suitable for global applications, supports GPS, GLONASS, BDS, Galileo and multi-system positioning, as well as supports a variety of SBAS signal reception processing, thus providing users with fast and accurate high-performance positioning experience.

Through the built-in Sensor Hub, UC6226 can connect with the gyroscope, accelerometer, magnetometer, barometer and other sensors to realize fusion positioning. With the accurate scenes and pattern recognition, in the harsh signal environment, UC6226 can still ensure fast and accurate positioning effect, and significantly reduce the average operating power consumption, substantially increase the standby time of devices, such as mobile phones, wearing devices and Internet of Things devices.

What's more, UC6226 has adopted the high integration design, and the chip has provided built-in DC/DC, LDO, LNA and RTC, etc. With the simple peripheral devices, it can achieve a complete GNSS receiver function, which can significantly reduce the PCB area and save hardware costs for users.

UC6226 QFN40 package is AEC-Q100-Compliant, is compatible with mainstream package; WLCSP package meets the requirements of industrial application. What's more, the small footprint is suitable for applications requiring compact dimensions.

## 1.2. Feature Advantages

UC6226 has the following features:

- Positioning engine features
  - 64-channel simultaneous tracking;
  - Less than 1 second hot start time;
  - -147 dBm cold start sensitivity, -160 dBm tracking sensitivity;
  - Up to 10Hz data update rate
- Support GPS, BDS, GLONASS and Galileo
- Support 26MHz crystal and TCXO;
- External 32.768kHz crystal is optional;
- Built-in DC/DC and power management unit;
- Built-in Sensor Hub, support PDR, VDR and another fusion algorithm
- SOC adopts ultra-low power design, PDR can further lower the power consumption
- Support three starting modes: ROM built-in firmware, Flash expansion firmware and AP load firmware
- Automotive grade 5.0mm x 5.0mm QFN40 package, 0.4mm pitch

- Industrial grade 1.73mm x 2.87mm WLCSP package, small footprint
- Under the simplified BOM conditions, the complete receiver PCB area <30mm$^2$

## 1.3. Performance Specifications

GNSS performance specifications of UC6226 are as follows:

Table 1-1 UC6226 GNSS Performance

| Item | Description | | |
|---|---|---|---|
| **Positioning accuracy** | | | |
| Single point positioning | <2.0m CEP | | |
| D-GNSS | <1.0m CEP | | |
| **Velocity accuracy** | 0.1m/s | | |
| **Sensitivity[1]** | | | |
| | GPS | BDS | GLONASS |
| Cold Start[2] | -147dBm | -146dBm | -140dBm |
| Tracking | -160dBm | -159dBm | -158dBm |
| Hot start | -151dBm | -150dBm | -151dBm |
| Reacquisition | -158dBm | -157dBm | -156dBm |
| **TTFF[3]** | | | |
| Cold start | <28s | | |
| AGNSS | <4s[4] | | |
| Hot start | <1s | | |
| Reacquisition | <1s | | |

[1] The sensitivity index needs C/N0 attain 41dB

[2] Externally matches LNA and ensure superior performance

[3] Satellite signal strength is up to -130dBm

[4] Assisted Ephemeris Information

# 1.4. System Block Diagram

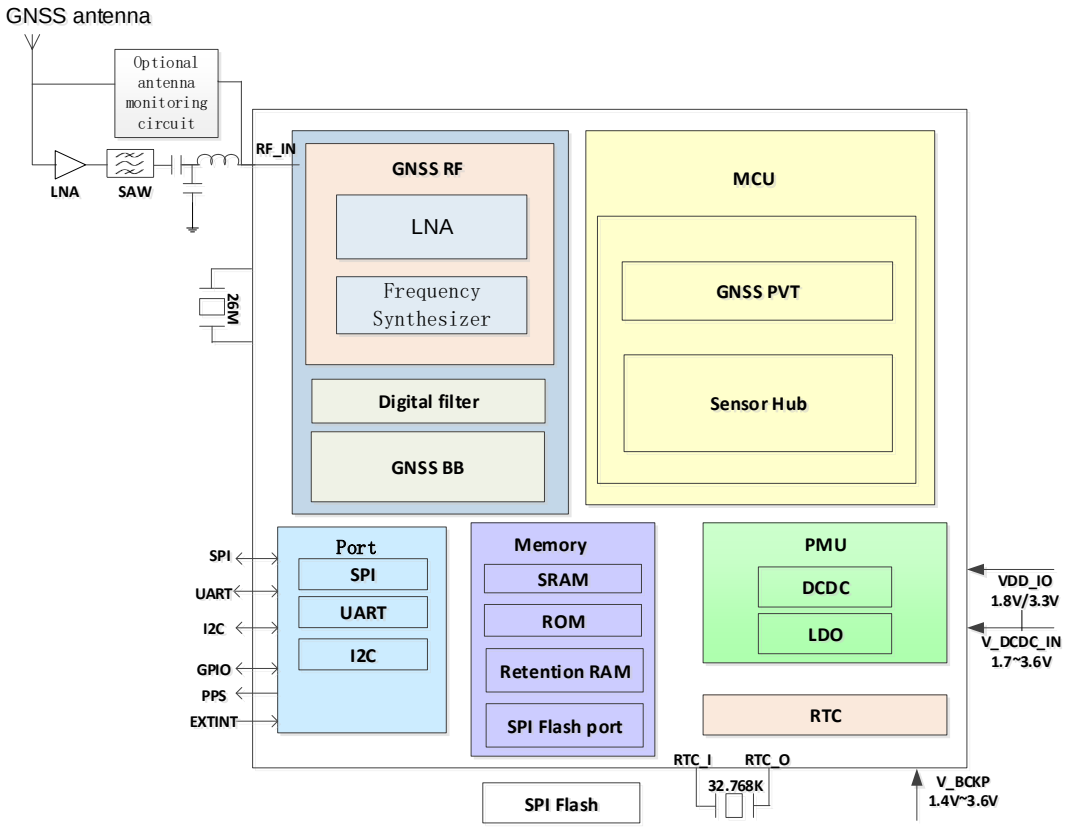



Figure 1-1 UC6226 chip block diagram

# 1.5. Satellite Navigation Systems

UC6226 supports multiple GNSS systems, including GPS, BDS, GLONASS, Galileo and SBAS. RF uses a broadband design that simultaneously receives and processes satellite signals from four satellite systems, including GPS L1, BDS B1, GLONASS L1 and Galileo E1, which can receive or process two or three of them in parallel.

By default, the UC226 is configured to receive GPS and BDS signals simultaneously. If the user has higher requirements on power consumption, single system is configured to operate via the command, i.e. use either GPS or BDS. For other systems' configuration, please contact Unicore FAE to obtain GNSS firmware.

### 1.5.1. GPS

The UC6226 can receive and track GPS's 1575.42 MHz L1 signal.

### 1.5.2. GLONASS

UC6226 can receive and track GLONASS's L1 signal, the signal frequency is 1602 MHz + k * 562.5 kHz, k = -7 ~ +6. Users can design GLONASS receivers in compliance with regulatory requirements.

### 1.5.3. BDS

UC6226 can receive and track the BDS satellite navigation system's 1561.098 MHz B1 signal. It can combine with GPS to receive and track the BDS B1 satellite signal, increase the coverage, improve reliability and improve accuracy.

### 1.5.4. Galileo

UC6226 can simultaneously receive and track GPS and Galileo signals, as well as enhance accuracy and coverage.

## 1.6. Protocols and Interfaces

UC6226 data protocol complies with "Unicore Protocol" specification. By default, UC6226 communicates with host device via UART, and performs data communication via configuring to $I^2C$ and SPI. For the technical parameters of the various protocols, supported communication interfaces and firmware versions, please refer to the *Unicore Protocol* documentation.

### 1.6.1. Terms and Abbreviations

The following table lists the terms and abbreviations involved or used in this document:

Table 1-2 List of terms and abbreviations

| Abbreviations | Complete description or name |
|---|---|
| A/D | Analog/Digital |
| ADC | Analog Digital Convertor |
| AGC | Automatic Gain Control |

| Abbreviations | Complete description or name |
|---|---|
| AGNSS | Assisted GNSS |
| BB | Baseband |
| CP | Chip Probing |
| DC/DC | Direct Current to Direct Current |
| DGNSS | Differential GNSS |
| FT | Final Test |
| Galileo | Galileo Navigation Satellite System |
| GLONASS | GLONASS Navigation Satellite System |
| GNSS | Global Navigation Satellite System |
| GPS | GPS Navigation Satellite System |
| LDO | Low DropOut regulator |
| LNA | Low Noise Amplifier |
| PDR | Pedestrian Dead Reckoning |
| PGA | Programmable Gain Amplifier |
| PIO | Programming Input/Output |
| PLL | Phase Locked Loop |
| PMU | Power Management Unit |
| POR | Power On Reset |
| RAM | Random Access Memory |
| RF | Radio Frequency |
| RTC | Real-Time Clock |
| SBAS | Satellite-Based Augmentation System |
| SAW | Surface Acoustic Wave |
| SPI | Serial Peripheral Interface |
| SQI | Serial Quad I/O |
| TCXO | Temperature Compensate Crystal Oscillator |
| VDR | Vehicle Dead Reckoning |

Chapter 2

# 2. RF Subsystem

RF subsystem adopts broadband design. The input signal is centered at about 1575MHz with a 100 MHz band width. The received GNSS signals are amplified by a Low Noise Amplifier (LNA), and then fed to a gain block, which offers further amplification, thus reducing the noise figure requirements for the mixer. The gain block also provides a single-ended to differential conversion.

After the complex down-conversion, the multi-GNSS signals are split up into I and Q channels. Afterwards both channels are I/Q low-pass filtered and amplified by separate Programmable Gain Amplifiers (PGA). The amplified I and Q signals will do the A/D conversion to get 6-bits I/Q digital signals that are then sent to baseband section, where signal processing and final image rejection takes place.

## 2.1. LNA

The low noise amplifier (LNA) makes use of a single stage configuration and requires external matching to function satisfactorily. For improved performance an external LNA should be added. Depending on the application, it might be useful to consider additional SAW to improve robustness against interference.

## 2.2. Gain Block

A single stage differential amplifier follows the LNA providing further amplification and conversion from single-ended to differential signaling.

## 2.3. Mixer

UC6226 uses the active I/Q mixer to first convert the multi-GNSS signals to an intermediate frequency. At this stage the signals are split into two similar IF channels. Both channels are further amplified and converted into different GNSS signal band.

## 2.4. I/Q Low-Pass Filter (LFP)

The low-pass filter removes any high-frequency from the desired signal. For single GNSS system signal reception, their cut-off frequency and band width are adjusted lower to reduce power consumption.

## 2.5. PGA

The programmable gain amplifiers (PGA) are used to provide the ADCs with appropriate input IF signals. The PGA gain can be automatically closed looped according to the ADC output signal to provide automatic gain control (AGC) for the receiver. The PGA gain is automatically looped and adjusted based on the ADC output signal values, providing an automatic gain control (AGC) for the receiver.

PGA gain can be configured as a fixed value via GPIO to improve system's robustness, which is suitable for applications that integrate with mobile communication functions.

## 2.6. ADC

Two 6-bit ADCs are used for A/D conversion in the UC6226. I and Q-branch ADC output 6-bit signal respectively, and then enter into baseband subsystem for processing.

Chapter 3

# 3. Baseband Subsystem

## 3.1. Interfaces

A number of interfaces are provided by UC6226 either for data communication or Flash access. The embedded firmware uses these interfaces according to their respective protocol specifications. For specific applications, the firmware also supports the connection of peripheral devices, such as external Flash or sensors, to some of the interfaces.

The digital I/O of the baseband section is powered by VDD_IO, and the VDD_IO level is the same as applied logic voltage level. Without supplying VDD_IO, the UC6226 will be kept in reset state.

As the UC6226's selected digital IO does not support anti-current backflush function, IO interface should not be supplied power separately in the case of power down in the actual application. Please see the note in 3.2 for details.

### 3.1.1. UART

The UC6226 makes use of two UART interfaces, UART1 and UART2, which can be used for communication with a host. Both of them support configurable baud rates up to 921600bps.

By default, PIO6/PIO7 corresponds with UART1, which is the main UART port in standard firmware version. The communication interface of the UC6226 can be mapped to a different PIO interface via D_SEL. PIO6/PIO7 can also be used as an SPI, at which point UART1 will be mapped to PIO15/PIO16. Refer to the note in 3.2 for D_SEL usage and corresponding communication interface mapping.

UART2 can use PIO17/PIO18, or PIO10/PIO12, or PIO2/PIO3. By default, UART2 will use PIO17/PIO18 in the standard firmware. UART2 is mainly used for transmitting or debugging auxiliary information.

### 3.1.2. Debug Interface

The UC6226 provides two dedicated pins for debug purpose, including chip probing (CP) and final test (FT). The interface consists of two dedicated pins: TCK and TMS.

When designing the UC6226 application, the chip test interface TCK and TMS must be kept open.

## 3.2. PIO

The PIO module may be configured as a GPIO or as the aforementioned communication interface. The following table describes all PIO functions and multiplexing.

Table 3-1 PIO function and multiplexing

| PIO # | Default function | I/O | Description | Multiplexing function |
|---|---|---|---|---|
| 0 | GPIO | I/O | NC | SPI slave MOSI,<br>SPI slave MISO |
| 1 | GPIO | I/O | NC | SPI slave MISO,<br>SPI slave MOSI |
| 2 | GPIO | I/O | NC | TIMEPULSE, UART2 TX |
| 3 | GPIO | I/O | NC | TIMEPULSE, UART2 RX |
| 4 | GPIO | I/O | NC | SPI slave clock |
| 5 | GPIO | I/O | NC | SPI chip select |
| 6 | TX1 | O | UART1 TX (if D_SEL is high at startup) | GPIO |
| 7 | RX1 | I | UART1 RX (if D_SEL is high at startup) | GPIO |
| 8 | GPIO | I/O | NC | SCL |
| 9 | GPIO | I/O | NC | SDA |
| 10 | D_SEL | I | Communication interface selection | |

| PIO # | Default function | I/O | Description | Multiplexing function |
|---|---|---|---|---|
| | | | pin.<br>This pin forces a pull up by default | |
| 11 | PPS | O | 1PPS output | EVENT<br>CPU_CLK |
| 12 | BOOT_MODE | I | Bootstrap mode selection pin.<br>This pin forces a pull up by default | UART1 TX,<br>UART2 TX |
| 13 | - | I | No function by default | EVENT,<br>UART1 CTS,<br>SCL or SCK |
| 14 | No function | I | Can be configured as antenna detection input | EVENT,<br>ANT_DET |
| 15 | ANT_OK | I | Antenna status detection input | ANT_SHORT, |
| 16 | ANT_OFF | O | Antenna power supply control output and output state is related to the PIO15 state | SPD_PULSE |
| 17 | UART2 RX | I | UART2 RX | SCL or SCK |
| 18 | UART2 TX | O | UART2 TX | UART2 TX<br>SDA |

☞ *As the digital IO selected by UC6226 does not support anti-current backflush function, please pay attention to the following points in development and application:*

*1) When VDDIO and V_DCDC_IN/Vcore use the same power supply: it should indicate signal state of host port that communicates with UART, SPI. I²C when power down. If host computer wants to control the chip power down, users should first set the ports that connect with UC6226 to high impedance state so as to prevent UC6226 from consuming host computer's power.*

*2) In case VDDIO and V_DCDC_IN/Vcore do not use the same power supply, users can cut off V_DCDC_IN/Vcore power supply to achieve the purpose of chip power-down.*

## 3.3. Watchdog

The UC6226 includes a watchdog timer, which prevents system-lockups caused when the software gets trapped in a deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before timer overflow occurs.

## 3.4. Timer Counter

The timer counter has one TIMEMARK input and one TIMEPULSE output. TIMEMARK can be input via PIO11, PIO13 or PIO14, but only be input through one of the PIOs. TIMEMARK inputs (routed through EXTINT0 and EXTINT1) is timestamp events relative to GPS time.

TIMEPULSE can be output via PIO2, PIO3 or PIO11, but only one TIMEPULSE can be output at one time. TIMEPULSE outputs generate pulse sequence synchronized with GPS or UTC time grid, time intervals can be configured over a wide frequency range.

## 3.5. Clock

### 3.5.1. TCXO

The UC6226 requires an external 26MHz clock, which can be provided by TCXO or crystal, providing reference frequency for RF and baseband PLLs.

### 3.5.2. PLL

The fully integrated, low-power PLL generates the system clock from the 26MHz reference frequencies supplied by crystal or TCXO oscillators.

### 3.5.3. RTC

The RTC is driven internally by a 32768 Hz oscillator, which makes use of an external 32768Hz crystal.

If the main supply voltage and IO power supply fail and a backup battery is connected to V_BCKP, the baseband, RF, CPU will switch off, but the RTC still runs providing a timing reference for the receiver. This operating mode is called RTC puncturing mode. Under the RTC puncturing mode, the relevant data for GNSS hot start is still saved in the Retention RAM.

The RTC puncturing mode is required for GNSS hot start function, under this mode, time information is maintained in the RTC and the ephemeris and calendar are kept in the

Retention RAM or Flash. In an A-GNSS-based system, RTC is not required if time information and ephemeris can be provided through the network.

If Retention RAM and RTC are not used, UC6226 does not require a backup battery.

The standard firmware supports 32768HZ by default. And UC6226 also support digital clock signal of external 32768HZ directly into the RTC_I pin to replace the crystal. When the external digital clock signal is used to input RTC_I, please note that its signal amplitude should be less than 1.1V, otherwise the UC6226 may be burnt.

### 3.5.4. Clock Source Combination

Table 3-2 clock source combination

| Main clock input | RTC clock input | Description |
|---|---|---|
| **26MHz TCXO provides clock connection to XTAL_I** | 32768Hz crystal provides clock connection to RTC_I and RTC_O | Normal use<br>V_BCKP must be provided by battery to keep RTC running |
| **26M TCXO provides clock connection to XTAL_I** | 32768Hz external digital signal to RTC_I | Normal use<br>V_BCKP must be provided by battery to keep RTC running |
| **26M TCXO provides clock connection to XTAL_I** | | GNSS hot-start function is disabled under this condition. |

For the application of the above clock source combination, the following should be noted in the design:

- When using 26M TCXO, the TCXO can be powered by LDO_X or external power supply, XTAL_O should be kept floating
- In case 32768Hz external digital signal is used as the RTC clock, its waveform amplitude must be attenuated to 0.9V~1.1V, The clock drift should between ± 0.6Hz, 20ppm.

# 3.6. Power Management Unit (PMU)

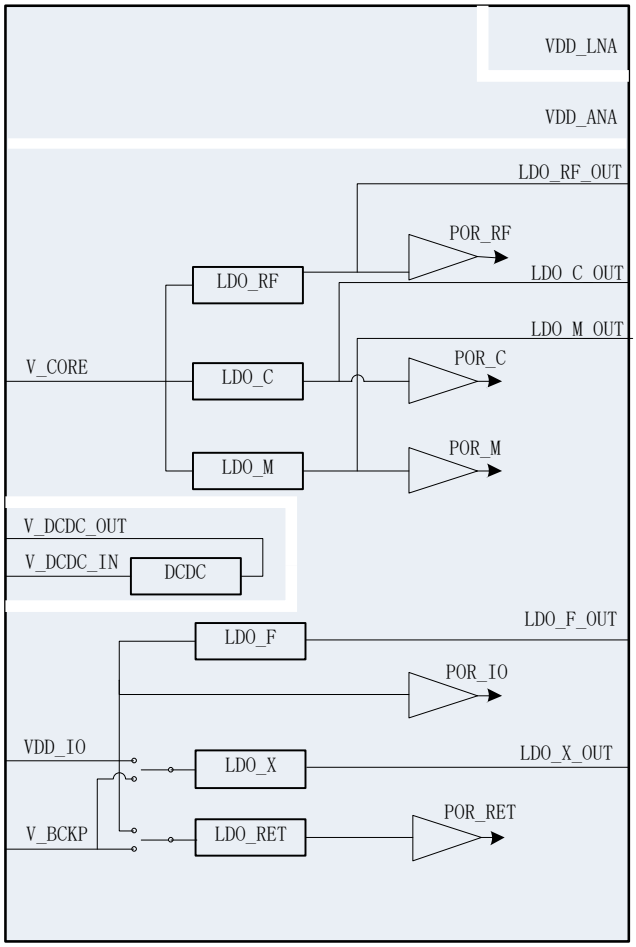



Table 3-1 Power Management Unit (PMU)

The PMU provides four power domains that are internally generated by LDOs and supervised by several voltage monitors:

- Core (Core)

The core domain is the main power domain for the RF and logic inside the chip. Two subsequent LDOs (LDO_C and LDO_RF) convert V_CORE source, and convert V_CORE to respective voltages, which must be decoupled through LDO_C_OUT and LDO_RF_OUT pins respectively the LDO_C drives the digital logic parts, and the LDO_RF drives the RF and analog circuits.

LDO_RF_OUT does not directly connect or drive RF circuits on-chip. Instead, users should connect it to the VDD_LNA and VDD_ANA on PCB to feed the supply into the on-

chip RF circuits. It is recommended that users should use noise-resistant connections to improve RF performance, such as using magnetic beads.

In the case UC6226 is powered by on-chip DC/DC, voltage range for V_CORE pin is 1.0V-1.1V; in DC/DC bypass mode, V_CORE allows the input voltage range of 1.2V-1.98V.

- IO

The IO power domain is powered by VDD_IO, including chip IO devices, on-chip Flash, ADC converters and eFuse. The supply voltage of VDD_IO could be 1.8V centered (1.7V-1.9V) or 3.3V centered (2.8V – 3.6V). Except IO pads, the other devices are powered by a dedicated LDO_F to ensure 1.8V supply voltage for on-chip flash, ADC and eFuse. The LDO_F must be connected with a decoupling capacitor through LDO_F_OUT pin.

- Backup

The backup domain runs the RTC section and the Retention RAM. This domain uses the voltage sources of VDD_IO and V_BCKP. In case VDD_IO voltage is inside the normal range, it uses VDD_IO, otherwise use V_BCKP. The allowed voltage range of V_BCKP is 1.4V-3.6V. Therefore, a common lithium battery or other battery could be directly connected to this pin.

- Crystal

If it is being used 26M TCXO and TCXO powered by LDO_X, LDO_X_OUT should be connected to the power pin of TCXO and decoupling capacitance. And user can also choose an external power source other than LDO_X to make TCXO work. Note that if TCXO used as the main clock source, and the clock source is used to drive RTC, do not design the hardware backup function, V_BCKP can’ t provide the working current required by TCXO.

### 3.6.1. DC/DC Converter

UC6226 integrates a DC/DC converter, allowing reduced power consumption and cost, especially when using a single supply voltage. To use the chip DC/DC converter, the main power supply must be connected to V_DCDC_IN and a capacitor and an inductor must be added to connect V_DCDC_OUT to V_CORE. If a DC/DC converter is not used, connect V_DCDC_IN/V_DCDC_OUT to V_CORE.

If a DC/DC converter is used, the allowable input voltage range for V_DCDC_IN is from 1.7V to 3.6V. If the DC/DC converter is not used, the allowable input voltage range for V_DCDC_IN/V_CORE is from 1.2V to 1.98V. The UC6226 chip will be damaged if power supply exceeds maximum allowable voltage range.

# 3.7. RAM

## 3.7.1. Backup RAM

UC6226 has a built-in 32k Bytes backup RAM powered by the battery, which enables all relevant data to be saved in case of a power failure. The Backup RAM is powered inside backup domain, so the V_BCKP can automatically take over the supply once VDD_IO gets lost.

## 3.7.2. System RAM

The UC6226 chip includes 768k Bytes system RAM and 512k Bytes system ROM, which is shared by the processor for data access, the UART, $I^2C$ and SPI DMA.

## 3.7.3. GNSS RAM

The UC6226 chip uses a 256k Bytes GNSS RAM, which is used by the tracking engine. This memory can also be used by the processor with less efficiency.

## 3.7.4. Acquisition RAM

The UC6226 chip includes a 384kByte dedicated RAM for the GNSS acquisition engine.

## 3.7.5. eFuse Memory

The UC6226 chip includes an integrated 256bit eFuse, which permanently saves chip production information and configuration settings.

Chapter 4

# 4. Operating Modes

## 4.1. Continuous Tracking Mode

Under the full-speed operation mode, the chip's hardware tracking channel will uninterruptedly process satellite signals, to ensure the accuracy of positioning, velocity, and TTFF through high-quality signal acquisition and tracking.

## 4.2. Sleep Mode

The chip is powered off except for the RTC punctual unit and Backup RAM. Users can easily wake up according to actual needs. Under the sleep mode, the chip operates at very low power levels and can realize hot start quickly after waking up.

Chapter 5

# 5. System Configuration

## 5.1. Configure the Communication Interface

The standard communication interface of UC6226 includes two UART serial.

## 5.2. Configuration Pins

There are two configuration pins: BOOT_MODE (PIO12) and D_SEL (PIO10).

The BOOT_MODE pin decides which Boot mode the chip will enter: the standalone mode or SPI slave mode. Please check the next section for the descriptions for these two modes.

The D_SEL pin is used to choose the communication interface set. When D_SEL pin is left open or connected to VDD_IO, UART1 and I²C use PIO6/PIO7/PIO8/PIO9. The SPI slave interface is disabled by default and should be configured respectively if it is required to be enabled. If the D_SEL pin is connected to GND, the SPI slave uses PIO6/PIO7/PIO8/PIO9, while UART1 and I²C are mapped to PIO15/PIO16/PIO17/PIO18. Moreover, PIO14 is used as an auxiliary SRDY signal to help SPI communication. The brief schematic diagram is shown in the following table:

Table 5-1 D_SEL pin configuration

| D_SEL configuration | Pin function | Description |
|---|---|---|
| 1 | UART1 TX/RX：PIO6/PIO7<br>I²C SCL/SDA：PIO8/9 | |

| D_SEL configuration | Pin function | Description |
|---|---|---|
| 0 | SPI Slave MISO/MOSI/clk/CS：<br>PIO6/PIO7/PIO8/PIO9<br>UART1 TX/RX：PIO15/PIO16<br>I²C SCL/SDA：PIO17/PIO18 or PIO13/PIO14 | PIO14 acts as an auxiliary SRDY for the SPI interface |

All the configurations above are for UC6226' s standard functions, or standard firmware versions. Please be noted that I2C can either be mapped to PIO17/PIO18 or mapped to PIO13/PIO14, depending on the firmware. Actually, the interface configuration of UC6226 is quite flexible, and the configuration mode more complex accordingly, depending on the firmware. For details, please check the PIO configuration table for details and follow the release notes for the firmware you are using.

The D_SEL is only valid before the power-on or RESETN is released. After the RESETN is released, the D_SEL pin can be used as an ordinary PIO pin.

## 5.3. Boot Modes

There are two major Boot modes of UC6226 controlled by BOOT_MODE (PIO12) pin: standalone mode and SPI slave mode.

When the UC6226 boots from the standalone mode, its internal CPU sequentially checks valid firmware in the external flash, the embedded flash in package and the ROM. In case the external flash is not detected or the firmware in the external flash is absent, the CPU then tries to read the firmware in the embedded flash in package. If it fails again, the CPU then turns to use the ROM firmware.

If the UC6226 boots from the SPI slave mode, CPU waits for firmware transmission initiated by the host through SPI slave interface. The host then starts the transmission with Unicore' s dedicated protocol. After the firmware transmission is over, the UC6226' s internal CPU starts to execute the firmware.

If it boots from the stand-alone mode, the internal CPU will monitor the firmware upgrade request of UART1 port. If the CPU detects an upgrade request within 20ms after power-on or reset, the CPU starts to adapt the baud rate and upgrades the firmware; otherwise, it follows the Boot sequence described above.

The BOOT_MODE is only valid before the power-on or CHIP_RSTN is released. After the CHIP_RSTN is released, the BOOT_MODE pin can be used as an ordinary PIO pin.

## 5.4. System Reset

According to the power structure of UC6226 chip, there are two reset domains: the core domain and the Backup domain. The Core domain contains all circuits clocked by 26M clock, and Backup domain contains RTC circuits and Retention RAM.

The main RESET controls the reset of the Core domain, and the main RESET domain has the following reset source:

- POR_IO is used to detect IO voltage. When the IO voltage is lower than 1.62V (1.8V IO supply), it sends the resetting signal of core domain; then the core domain reset signal; When the IO voltage is lower than 2.6V (3.0V/3.3V IO supply), it sends the resetting signal of Core domain;
- POR_DCDC is used to detect DC/DC input voltage. In the DC/DC condition, the Core domain resetting signal is sent when the DC/DC voltage is less than 1.6V; under DC/DC bypass condition, the Core domain resetting signal is sent when the voltage is less than 1.0V.
- POR_C is used to detect the core voltage. When the core voltage is less than 90% of the firmware preset voltage, the Core domain reset signal is sent;
- POR_RET is used to detect the voltage of the backup power domain. When the voltage of backup power domain is less than 0.6V, the Core domain resetting signal is sent;
- RESET_N is the reset pin of chip, when its level is low, the Core field resetting signal is sent;
- The software system resetting signal of Chip is, controlled by firmware;
- Watchdog RESET.

If any of the above resetting sources issues a Core domain resetting signal, the Core domain will be reset.

The Backup RESET domain has the following reset sources:

- POR_RET is used to detect the supply voltage of backup power domain. When the voltage is lower than 0.6V, then the backup domain resetting signal is sent;
- The RTC RESET signal controlled by software controls is controlled by the

firmware.

If any of the above resetting sources issues a backup domain reset signal, the backup domain will be reset.

## 5.5. Power on Sequence

In general, there are two scenarios for UC6226 power supply: to use the internal DC/DC, or bypass the internal DC/DC. The RTC region and VDD_IO region are independent with the main power supply, and power-on sequences do not affect or depend on each other.

### 5.5.1. DC/DC Power-on and Sequence

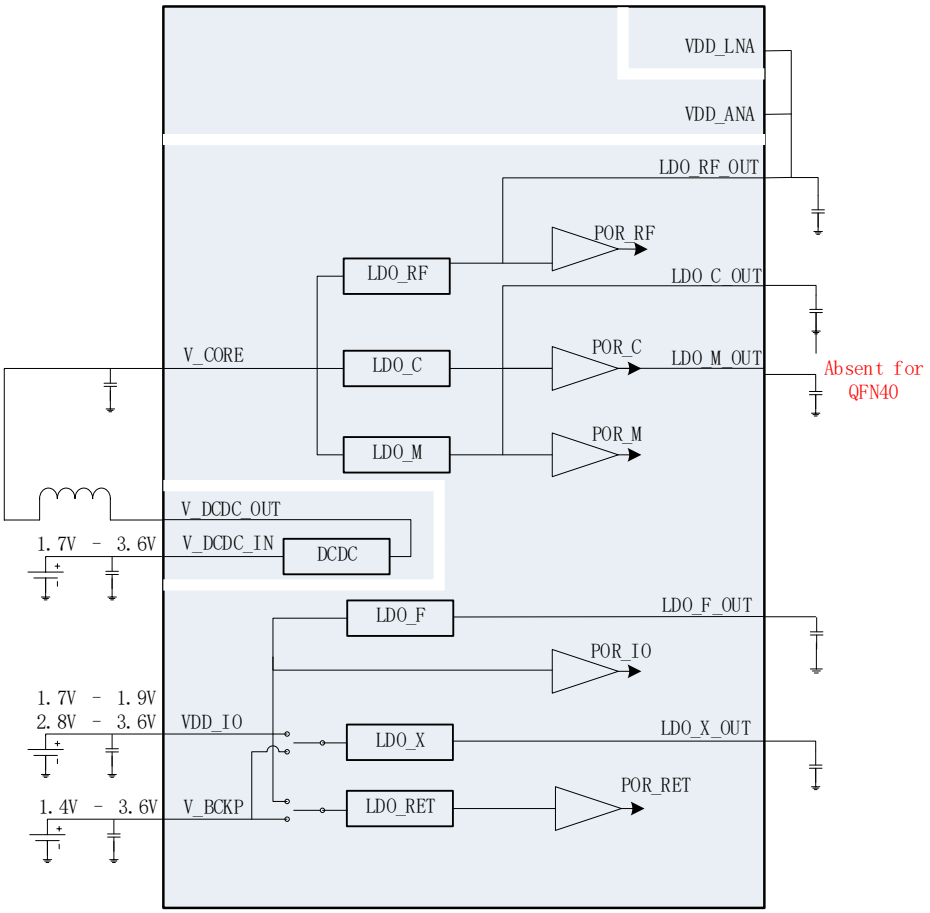



Figure 5-1 DC/DC power-on and sequence

With the internal DC/DC, the supply efficiency is maximized. The main supply is

connected to V_DCDC_IN pin, which is independent with VDD_IO.

The power on time for main supply and the VDD_IO should be shorter than 10ms. But there is no sequence requirement between the main supply and the VDD_IO. However, the missing of any of these two supplies will keep the main circuit in reset state.

When V_BCKP continues to power, the status of the main supply or VDD_IO does not affect the status of RTC region.

## 5.5.2. DC/DC Bypass Power-on and Sequence

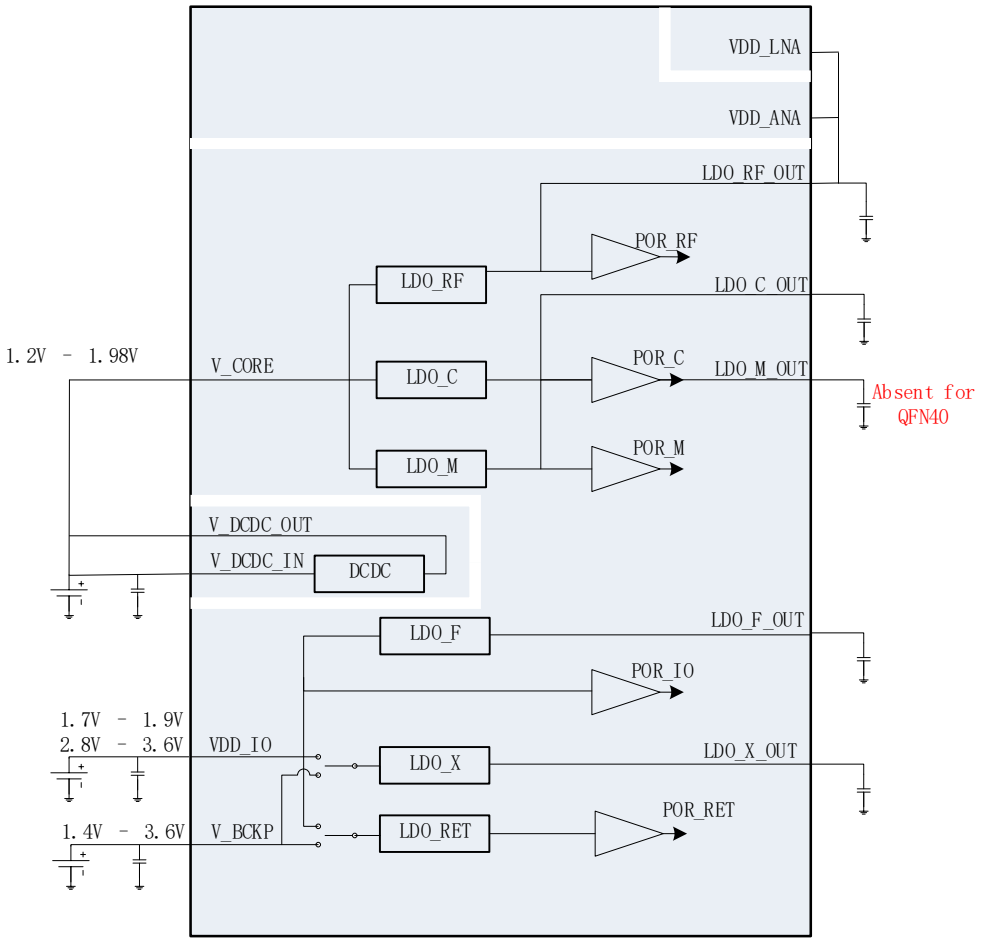



Figure 5-2 DC/DC bypass power-on and sequence (Main Supply is 1.2V ~ 1.98V)

Without the internal DC/DC, the number and cost of external components are minimized. In this case, the main supply is connected to V_DCDC_IN, V_DCDC_OUT and

V_CORE pins, which is independent with VDD_IO.

> ☞ *Please be attention that the allowed input voltage of main supply in this mode is limited to 1.2V –1.98V. The supply voltage higher than 1.98V will cause permanent damage of UC6226 chip.*

The power on time for main supply and the VDD_IO should be shorter than 10ms. But there is no sequence requirement between the main supply and the VDD_IO. However, the missing of any of these two supplies will keep the chip in reset state.

When V_BCKP continues to power, the status of the main supply or VDD_IO does not affect the status of RTC region.

### 5.5.3. Power on Sequence for Backup Region

The Backup region is powered by the output of an internal power switch, which switches between the IO supply from VDD_IO pin and the backup supply from V_BCKP pin. In order to minimize the backup battery consumption, only when the VDD_IO supply drops to a voltage below 1.6V, the switch changes to V_BCKP supply.

If neither VDD_IO nor V_BCKP is powered, the backup region does not work. If any one of pins is supplied, the backup region will be reset and soon start to be functional.

Chapter 6

# 6. Pin Definitions

## 6.1. Pin Distribution

### 6.1.1. QFN40

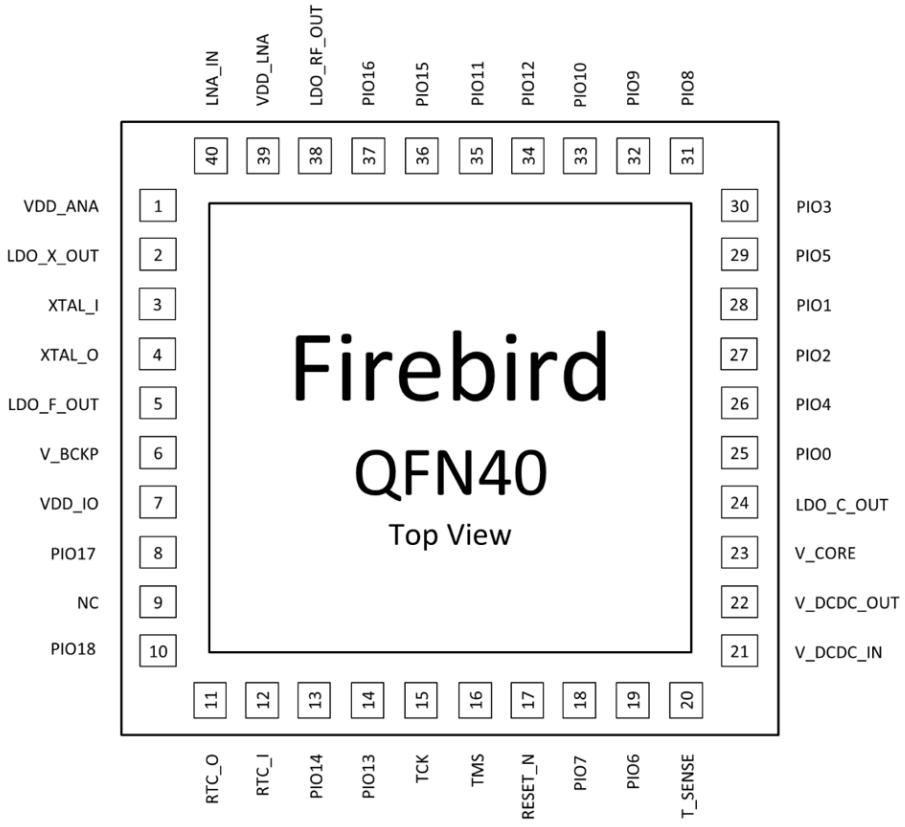



Figure 6-1 QFN40 pin diagram

### 6.1.2. WLCSP27

| ● | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | | GND_RF | LDO_X_OUT | NC | CLK_I | VDD_IO | RTC_O |
| B | LNA_IN | 1PPS* | NC | TMS | NC | NC | RTC_I |
| C | LDO_RF_OUT | NC | NC | RSTN | TCK | HUART_RXD | V_BCKP |
| D | NC | LDO_C_OUT | NC | NC | GND | V_CORE | HUART_TXD |

Remark: *ROM firmware does not support

## 6.2. Pin Description

### 6.2.1. QFN40 Pin Description

Table 6-1 Description of QFN40 Power Supply Pin

| Name | Pin QFN40 | Power Domain | Description |
|---|---|---|---|
| V_DCDC_IN | 21 | DC/DC | DC/DC input |
| V_DCDC_OUT | 22 | DC/DC | DC/DC output |
| V_CORE | 23 | Core | Core supply |
| V_BCKP | 6 | Backup | Backup cell supply |
| VDD_IO | 7 | IO | I/O, TCXO and Flash power supply |
| VDD_ANA | 1 | Core/RF | Power supply of analog section |
| VDD_LNA | 39 | Core/RF | LNA power supply |
| LDO_RF_OUT | 38 | Core/RF | RF power output |
| LDO_C_OUT | 24 | Core/Logic | Core power output |
| LDO_X_OUT | 2 | Clock | TCXO/crystal power output |
| LDO_F_OUT | 5 | Flash | Flash power output |
| PADDLE | paddle | | Ground |

Table 6-2 Description of QFN40 Analog Pin

| Name | Pin QFN40 | Power Domain | Description |
|---|---|---|---|
| LNA_IN | 40 | RF | LNA input (LNA requires an external input matching) |
| XTAL_I | 3 | Clock | 26M TCXO or crystal input |

| Name | Pin QFN40 | Power Domain | Description |
|---|---|---|---|
| XTAL_O | 4 | Clock | 26M crystal output |
| RTC_I | 12 | Backup | 32k crystal or digital clock signal input (amplitude range of 0.9V ~ 1.1V!) |
| RTC_O | 11 | Backup | 32k clock output |
| T_SENSE | 20 | IO | ADC input (required to be <1.8Vp-p) |
| RESET_N | 17 | IO | System reset |
| TCK | 15 | IO | Debug interface |
| TMS | 16 | IO | Debug interface |
| DNC | / | N/A | NC, please keep float |
| NC | 9 | N/A | NC<br>NC |

Table 6-3 Description of QFN40 PIO Pin

| Name | Pin QFN40 | Power Domain | I/O Reset | I/O Core off | Description |
|---|---|---|---|---|---|
| PIO0 | 25 | IO | I/pull-up | I/pull-up | IO PIO0 |
| PIO1 | 28 | IO | I/pull-up | I/pull-up | IO PIO1 |
| PIO2 | 27 | IO | I/pull-up | I/pull-up | IO PIO2 |
| PIO3 | 30 | IO | I/pull-up | I/pull-up | IO PIO3 |
| PIO4 | 26 | IO | I/pull-up | I/pull-up | IO PIO4 |
| PIO5 | 29 | IO | I/pull-up | I/pull-up | IO PIO5 |
| PIO6 | 19 | IO | O/pull-up | I/pull-up | IO PIO6 |
| PIO7 | 18 | IO | I/pull-up | I/pull-up | IO PIO7 |
| PIO8 | 31 | IO | I/pull-up | I/pull-up | IO PIO8 |
| PIO9 | 32 | IO | I/pull-up | I/pull-up | IO PIO9 |
| PIO10 | 33 | IO | I/pull-up | I/pull-up | IO PIO10<br>Or D_SEL |
| PIO11 | 35 | IO | I/pull-up | I/pull-up | IO PIO11 |
| PIO12 | 34 | IO | I/pull-up | I/pull-up | IO PIO12 or BOOT_MODE |
| PIO13 | 14 | IO | I/pull-down | I/pull-down | IO PIO13 |
| PIO14 | 13 | IO | I/pull-down | I/pull-down | IO PIO14 |
| PIO15 | 36 | IO | I/pull-up | I/pull-up | IO PIO15 |
| PIO16 | 37 | IO | I/pull-up | I/pull-up | IO PIO16 |
| PIO17 | 8 | IO | I/pull-up | I/pull-up | IO PIO17 |
| PIO18 | 10 | IO | I/pull-up | I/pull-up | IO PIO18 |

| Name | Pin QFN40 | Power Domain | I/O Reset | I/O Core off | Description |
|---|---|---|---|---|---|
| | | | | | |

## 6.2.2. WLCSP27 Pin Description

Table 6-4 description of WLCSP27 power supply pin

| Name | Pin WLCSP27 | Power Domain | Description |
|---|---|---|---|
| V_CORE | D6 | Core | Core supply |
| V_BCKP | C7 | Backup | Backup cell supply |
| VDD_IO | A6 | IO | I/O, TCXO power supply |
| LDO_RF_OUT | C1 | Core/RF | RF power output |
| LDO_C_OUT | D2 | Core/Logic | Core power output |
| LDO_X_OUT | A3 | Clock | TCXO/crystal power output |

Table 6-5 Description of WLCSP27 Analog Pin

| Name | Pin WLCSP27 | Power Domain | Description |
|---|---|---|---|
| LNA_IN | B1 | RF | LNA input (LNA requires an external input matching) |
| CLK_I | A5 | Clock | 26M TCXO or crystal input |
| NC | A4 | | NC |
| RTC_I | B7 | Backup | 32k crystal or digital clock signal input (amplitude range of 0.9V~1.1V！) |
| RTC_O | A7 | Backup | 32k clock input |
| RSTN | C4 | IO | System reset |
| TCK | C5 | IO | Debug interface |
| TMS | B4 | IO | Debug interface |

Table 6-6 Description of WLCSP27 IO pin

| Name | Pin WLCSP27 | Power Domain | I/O Reset | I/O Core off | Description |
|---|---|---|---|---|---|
| UART_RXD | C6 | IO | I/pull-up | I/pull-up | Serial data input |
| UART_TXD | D7 | IO | O/- | I/pull-up | Serial data output |
| NC | C3 | | | | NC |

| Name | Pin WLCSP27 | Power Domain | I/O Reset | I/O Core off | Description |
|---|---|---|---|---|---|
| NC | D3 | | | | NC |
| NC | D4 | IO | | | NC |
| PPS | B2 | IO | I/pull-up | I/pull-up | PPS output，the power on state is strictly prohibited to be at low level |
| NC | B3 | IO | | | NC |
| NC | B5 | IO | | | NC |
| NC | B6 | IO | | | NC |
| NC | D1 | IO | | | NC |
| NC | C2 | IO | | | NC |

Chapter 7

# 7. Electrical Specifications

## 7.1. Maximum Absolute Rating

Table 7-1 Maximum absolute rating

| Symbol | Parameter | | Min. | Max. | unit |
|---|---|---|---|---|---|
| V_DCDC_IN | Input voltage of the internal DC/DC converter<br>WLCSP without the pin | | -0.2 | 3.6 | V |
| V_CORE,<br>V_DCDC_OUT | Supply voltage of baseband main core and RF LDOs inputs<br>Output voltage of the internal DC/DC converter | | -0.2 | 1.98 | V |
| VDD_IO | VDDIO_3.3V | VIL | -0.2 | 0.7 | V |
| | | VIH | 1.2 | 3.6 | |
| | VDDIO_1.8V | VIL | -0.2 | 0.6 | |
| | | VIH | 1.2 | 1.9 | |
| V_BCKP | Supply voltage of backup domain and LDO_X inputs | | -0.2 | 3.6 | V |
| VDD_ANA,<br>VDD_LNA | Supply voltage RF domain | | -0.2 | 0.99 | V |
| Vi | Input voltage on XTAL_I | | -0.2 | 1.1 | V |
| $Vi_{ana}$ | Input voltage on RTC_I | | -0.2 | 1.1 | V |
| $Vi_{dig}$ | Input voltage on PIO0-18, RESET_N, TCK and TMS | | -0.2 | 3.6 | V |
| $Vi_{adc}$ | Input voltage on T_SENSE | | -0.2 | 1.98 | V |

| Symbol | Parameter | Min. | Max. | unit |
|---|---|---|---|---|
| $P_{rfin}$ | RF input power on LNA_IN | | +15 | dBm |
| $P_{tot}$ | Total power | | 100 | mW |
| $T_{jun}$ | Junction temperature | -40 | +125 | °C |
| $T_s$ | Storage temperature | -50 | +150 | °C |

## 7.2. Working Conditions

Table 7-2 QNF40 working conditions

| Symbol | Parameter | Condition | Min. | Typical | Max. | unit |
|---|---|---|---|---|---|---|
| $T_{amb}$ | Environment temperature | | -40 | +25 | +85 | °C |
| V_DCDC_IN | Input voltage of the internal DC/DC converter; WLSCP without this pin | | 1.7 | | 3.6 | V |
| V_CORE[5] | Supply voltage of baseband main core and RF LDO inputs | | 1.2 | 1.2 | 1.98 | V |
| VDD_IO | Supply voltage of I/O, LDO_X and flash; | 1.8V centered<br>3.0V/3.3V centered | 1.7<br>2.8 | 1.8<br>3.0/3.3 | 1.9<br>3.6 | V |
| | WLSCP | | 1.7 | 1.8 | 1.9 | |
| V_BCKP | Supply voltage of backup domain and LDO_X inputs | | 1.4 | | 3.6 | V |
| | WLSCP | | 1.4 | 1.8 | 3.6 | |
| VDD_ANA[6], | Supply voltage of | | 0.69 | 0.8 | 0.95 | V |

[5] If V_CORE is used to power the chip directly, V_DCDC_IN and V_DCDC_OUT must be connected to V_CORE

[6] If V_CORE is used to power the chip directly, V_DCDC_IN and V_DCDC_OUT must be connected to V_CORE

| Symbol | Parameter | Condition | Min. | Typical | Max. | unit |
|---|---|---|---|---|---|---|
| VDD_LNA | RF domain | | | | | |
| $F_{ref}$ | Reference clock | | | 26 | | MHz |

## 7.2.1. DC Electrical Characteristics

Table 7-3 DC electrical characteristics

| Symbol | Parameter | Min. | Typical | Max. | unit |
|---|---|---|---|---|---|
| VDD_IO | Supply voltage for PIOs and input voltage for LDO_F and LDO_X | 1.7<br>2.8 | 1.8<br>3.3 | 1.9<br>3.6 | V |
| V_DCDC_IN | Input voltage for DC/DC converter | 1.7 | | 3.6 | V |
| V_CORE (Internal DC/DC power supply) | Input voltage for LDO_C and LDO_RF | 1.0 | 1.1 | 1.1 | V |
| V_CORE (Internal DC/DC is not used) | Input voltage for LDO_C and LDO_RF | 1.2 | 1.2 | 1.98 | V |
| V_BCKP | Input voltage for LDO_B and LDO_X (backup mode) | 1.4 | 3.3 | 3.6 | V |
| | WLCSP | 1.4 | 1.8 | 3.6 | |
| $I_{LDO\_X\_OUT}$ | LDO_X output current | | | 5 | mA |
| LDO_X_OUT | LDO_X output voltage<br>(With 26M crystal)<br>(For 1.6V TCXO)<br>(For 1.9V TCXO) default<br>(For 2.6V TCXO)<br>(For 3.0V TCXO) | | -<br><br>1.6<br>1.9<br>2.6<br>3.0 | | V |
| LDO_RF_OUT | LDO_RF output voltage | 0.69 | 0.8 | 0.85 | V |
| LDO_F_OUT | LDO_F output voltage | 1.78 | 1.8 | 1.85 | V |
| LDO_C_OUT | LDO_C output voltage | 0.7 | 0.8 | 0.9 | V |

sign, please contact Unicore to obtain technical support.

| | | | | | |
|---|---|---|---|---|---|
| VDD_ANA | Power supply pin | 0.69 | 0.8 | 0.95 | V |
| VDD_LNA | Power supply pin | 0.69 | 0.8 | 0.95 | V |

## 7.2.2. Analog Parameters

Table 7-4 Analog parameters

| Symbol | Parameter | Condition | Min. | Typical | Max. | unit |
|---|---|---|---|---|---|---|
| RTC_Fxtal | RTC crystal resonant frequency | | | 32768 | | Hz |
| RTC_T_start | RTC startup time | | 0.2 | 1 | 2 | s |
| RTC_Iosc | 32768 Hz OSC current source | | | 3 | | μA |
| RTC_Amp | 32768 Hz OSC amplitude | ESR = 80 kΩ | 50 | | 350 | mVpp |
| RTC_ESR | 32768 Hz Xtal equivalent series resistance | | | | 90 | kΩ |
| RTC_CL | RTC integrated load capacitance | ESR = 80 kΩ | 7 | 7 | 12.5 | pF |
| RTC_Vil | RTC low level input voltage | Shared RTC oscillator input | 0.0 | | 0.2 | V |
| RTC_Vih | RTC high level input voltage | Shared RTC oscillator input | 0.7 | | 0.9 | V |
| DCDC_eff | DC/DC efficiency | Input 3.3V, 2mA-40mA, external components L = 4.7μH, C = 10uF | | 82 | | % |

## 7.2.3. RF Parameters

Table 7-5 RF parameters

| Symbol | Parameter | Condition | Min. | Typical | Max. | unit |
|---|---|---|---|---|---|---|
| Fin | Receiver input frequency | | 1550 | 1575.42 | 1620 | MHz |
| LNA_IN | LNA input impedance | Require matching devices | | 50 | | Ω |

| Symbol | Parameter | Condition | Min. | Typical | Max. | unit |
|---|---|---|---|---|---|---|
| | | and DC blocking capacitors.<br>Matching device typical value: series inductance L = 7.5nH, ground capacitance C = 3pF.<br>The typical value of DC blocking capacitor is 47pF. | | | | |
| LNA_S11 | LNA input return loss | 50Ω environment | | -10 | | dB |
| NFtot | Receiver chain noise figure | 50Ω environment | | 2.5 | | dB |
| Ext_Gain | External gain before matching | 50Ω environment | | | 45 | dB |
| TCXO_Freq | TCXO frequency | | | 26 | | MHz |
| TCXO_IN_Vpp | TCXO input peak-to-peak voltage | | | 0.6 | | $V_{pp}$ |
| XTAL_Freq | XTO frequency | | | 26 | | MHz |
| XTAL_Drive | XTAL drive level | @ 26MHz, 15Ω <ESR <60Ω | | | 100 | μW |

## 7.2.4. Current Consumption

Table 7-6 current consumption

| Symbol | Parameter | Condition | Typical | unit |
|---|---|---|---|---|
| $I_{BCKP}$ | V_BCKP backup current using the RTC crystal | Retention RAM powered (V_BCKP = 3.6V, VDD_IO = V_CORE = 0V)) | 45 | μA |
| $I_{BCKP}$ | V_BCKP backup current using the RTC crystal | Retention RAM power down (internal Flash chip) (V_BCKP = 3.7V, | 35 | μA |

| Symbol | Parameter | Condition | Typical | unit |
|---|---|---|---|---|
| | | VDD_IO = V_CORE = 0V)) | | |

## 7.3. Reference Power Requirements

The table below lists examples of the total system supply current including RF and baseband section for a possible application.

Values listed below are provided for customer information only as an example of typical current requirements (the basic frequency of system is 66MHz). Values are characterized on samples – actual power requirements can vary depending on Firmware version used, external circuitry, number of SVs tracked, signal strength, type and time of start, duration, and conditions of test.

Table 7-7 Indicative power requirements

| Symbol | Parameter | Condition | Typical | unit |
|---|---|---|---|---|
| Ivdd_io | IO current | Vcore=0V<br>No external peripherals | 200@3.3V<br>100@1.8V | uA |
| $I_{V\_DCDC\_IN}$ | V_DCDC_IN current<br>@ 3.3V, V_CORE = 1.1V | Acquisition (GPS and BDS or GLONASS) | 18.2 | mA |
| | | Tracking (GPS, BDS or GLONASS single mode tracking, continuous mode) | 8.5 | |
| | | Tracking (GPS and BDS or GLONASS dual mode simultaneous tracking, continuous mode) | 9 | |

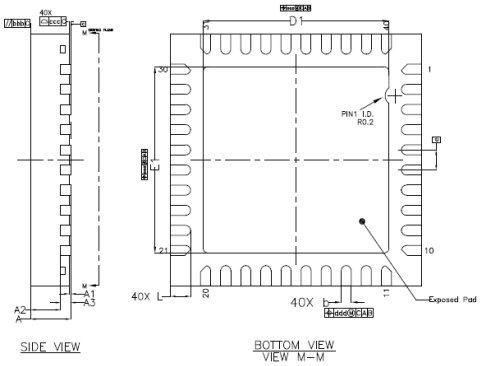
☞ *GNSS dual mode, support GPS+BDS or GPS+GLONASS to system dual mode; GNSS single mode, support GPS, BDS or GLONASS.*

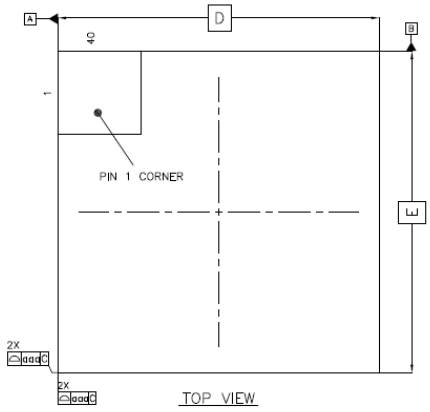
☞ *UC6226 operating current is related to firmware characteristics, including operating frequency, voltage, GNSS software strategy, etc. The above parameters are measured at 66MHZ system frequency. For further details, please refer to relevant test report.*

Chapter 8

# 8. Mechanical Specifications

## 8.1. QFN40




| DESCRIPTION | | SYMBOL | MILLIMETER | | |
|---|---|---|---|---|---|
| | | | MIN | NOM | MAX |
| TOTAL THICKNESS | | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | | A1 | 0.00 | --- | 0.05 |
| MOLD THICKNESS | | A2 | 0.50 | 0.55 | 0.60 |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.15 | 0.20 | 0.25 |
| BODY SIZE | X | D | 4.90 | 5.00 | 5.10 |
| | Y | E | 4.90 | 5.00 | 5.10 |
| LEAD PITCH | | e | 0.40 BSC | | |
| EP SIZE | X | D1 | 3.65 | 3.70 | 3.75 |
| | Y | E1 | 3.65 | 3.70 | 3.75 |
| LEAD LENGTH | | L | 0.35 | 0.40 | 0.45 |
| Tolerance of form and position | | | | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.1 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

Figure 8-1 QFN40 Mechanical Parameters

# 8.2. WLCSP27

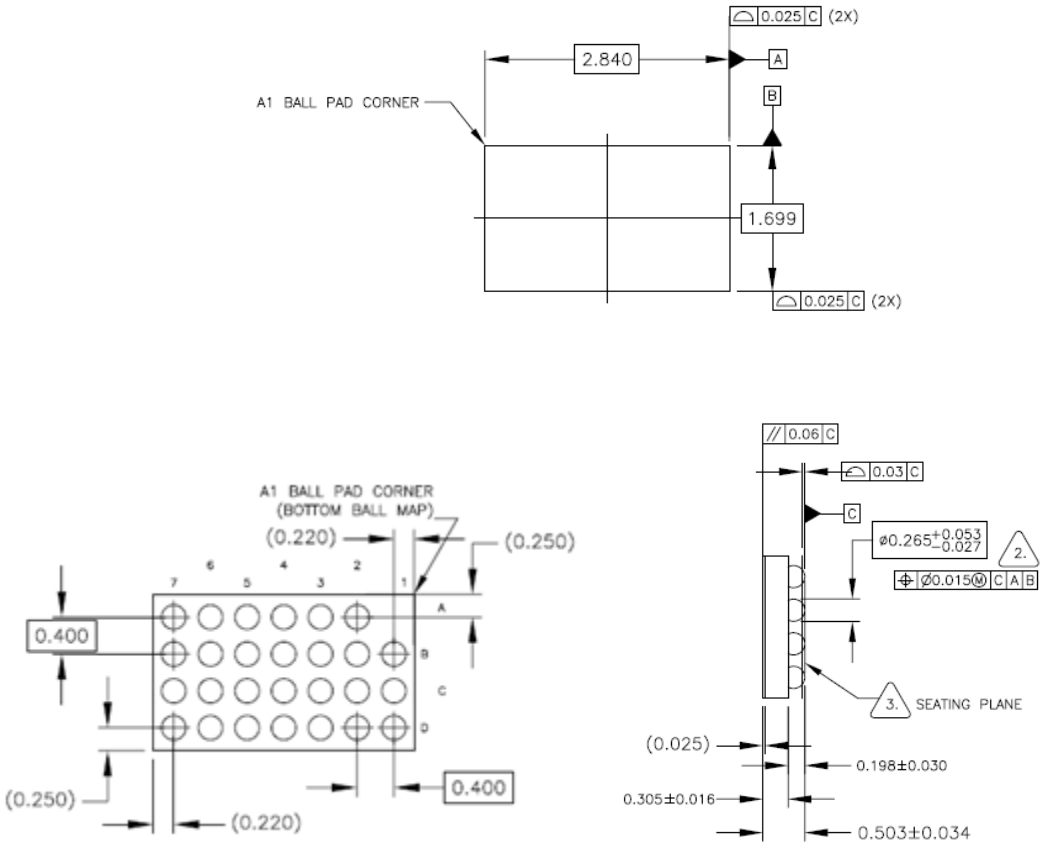



Figure 8-2 WLCSP Mechanical Parameters

WLCSP mechanical parameters description:

1. Ball pitch 0.4mm;

2. Raw ball diameter is 0.25mm;

Chapter 9

# 9. Reliability Test and Certificate

## 9.1. Reliability Test

UC6226 chips are qualified with standard according to appropriate JEDEC standards, e.g. JESD47 Stress-Test-Driven Qualification of Integrated Circuits.

UC6226 chips that meet automotive reliability test standards are qualified according to AEC-Q100 (Grade 3) *Failure Mechanism Based Stress Test Qualification for Integrated Circuits*. Please refer to 11 for the specific order model.

## 9.2. Certificate

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS). UC6226 chips are RoHS compliant and green (no halogens).

Chapter 10

# 10. Product Appearance, Packaging and Transportation

## 10.1. Appearance


Figure 10-1 QFN product appearance

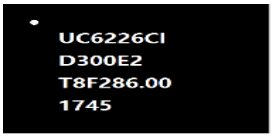



Figure 10-2 WLCSP product appearance

UC6226 chip's appearance is shown in above picture, the marking information may vary from customer order code, please follow the actual order.

## 10.2. Label

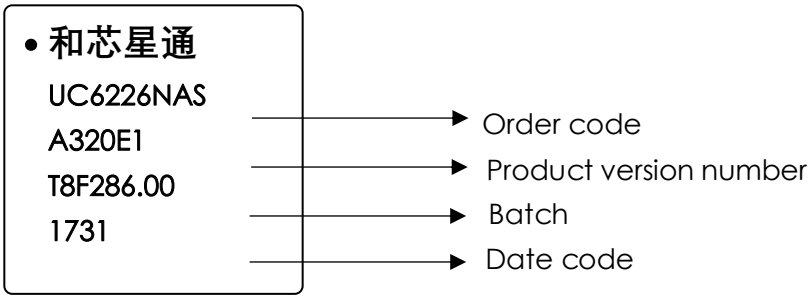



Figure 10-3 QFN product marking description

Table 10-1 Specific description of product label

| Code | Description |
|---|---|
| UC6226 | Main model of product |
| N | Package type code: N - QFN Package, C-WLCSP Package |
| A | Level: A – Automotive grade; I - Industrial grade |
| S | Whether to contain built-in Flash: S-Flash built-in; R - only supports on-chip ROM version firmware, not built-in Flash |
| A | Hardware version, s/n letter |
| 320 | GNSS firmware version number |
| E1 | Efuse configuration number |
| 1731 | Production date |

## 10.3. Package

UC6226 adopts tape packaging, QFN40 contains 3000 pieces in each package. The packaging is as follows:

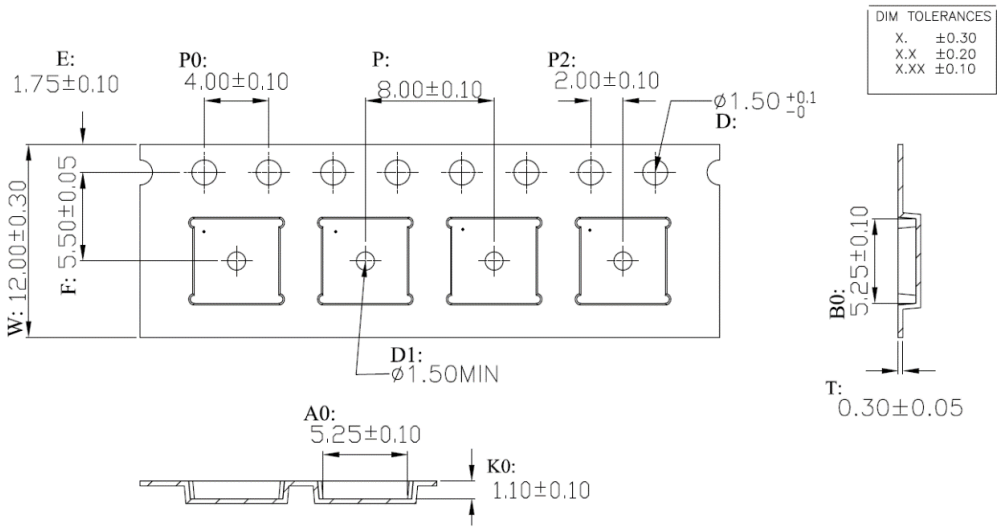



Figure 10-4 UC6226 Tape packaging

Tape specifications are as follows:

1. 10-hole spacing cumulative tolerance is ± 0.20mm;
2. All dimension sizes meet EIA-481-C requirements;
3. Thickness: 0.3 ± 0.05mm

WLCSP contains 5000 pieces in each package.

## 10.4. Ordering Codes

Table 10-2 Ordering Codes

| Order Number | Description |
|---|---|
| UC6226NIS | QFN40 package, industrial grade, built in Flash, support firmware update. Two options of VDDIO input voltage are supported as shown below |
| -E/B310E1 | VDDIO input voltage: 3.3V |
| -E/B310E2 | VDDIO input voltage: 1.8V |
| UC6226NIR | QFN40 package, industrial grade, non-built in Flash, support ROM version firmware or AP load firmware |
| UC6226NAS | QFN40 package, automotive grade, compliant with AEC-Q100, built in Flash, support firmware update |
| UC6226CI | WLCSP package, industrial grade, non-built in Flash, support ROM version firmware or AP load firmware |

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