

# WIRELESS INFRASTRUCTURE SOLUTIONS GUIDE

Digital Signal Processors, ASIC, Digital Upconverters/Downconverters, Data Converters, Amplifiers, Microcontrollers, Clock Distribution, Serial Gigabit, Interface, Logic, Power Management

4Q 2003



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## TI WORLDWIDE TECHNICAL SUPPORT

### Internet

TI Semiconductor Product Information Center Home Page  
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### Product Information Centers

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 Spain +34 902 35 40 28  
 Sweden (English) +46 (0) 8587 555 22  
 United Kingdom +44 (0) 1604 66 33 99  
 Fax +(49) (0) 8161 80 2045  
 E-mail [epic@ti.com](mailto:epic@ti.com)  
 Internet [support.ti.com/sc/pic/euro.htm](http://support.ti.com/sc/pic/euro.htm)

#### Japan

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 Domestic 0120-81-0036  
 Internet/E-mail International [support.ti.com/sc/pic/japan.htm](http://support.ti.com/sc/pic/japan.htm)  
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## GENERAL OVERVIEW

### TI'S HIGH-PERFORMANCE, FLEXIBLE SOLUTIONS ENABLE LOWEST COST/CHANNEL IN WIRELESS NETWORKS

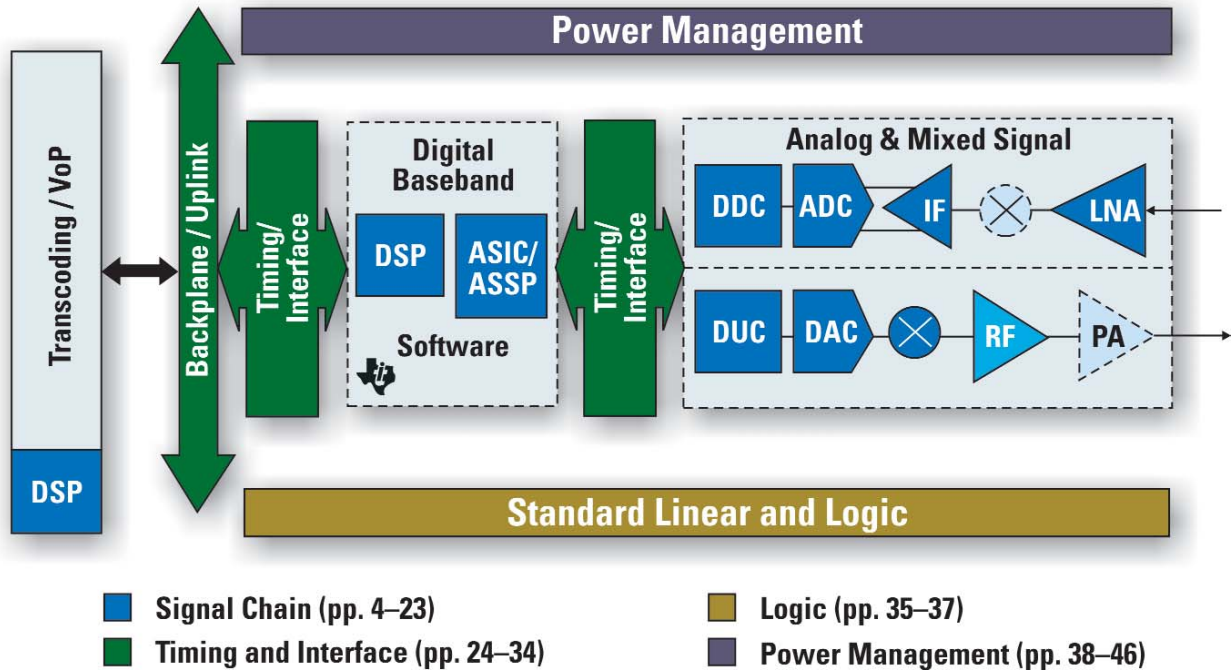
Transitioning from the voice-centric services of a 2G network to the multimedia-dominated data of 2.5G and 3G presents designers of wireless infrastructure systems with a number of challenges, such as how to reduce cost per channel while effectively increasing capacity, processing higher data rates and supporting several multimedia standards simultaneously. At the same time though, designers must address the usual engineering questions of size, cost and power consumption.

Base station manufacturers need a broad portfolio of flexible products to provide a large degree of freedom when it comes to partitioning and migrating various critical tasks within systems as they evolve. Successful manufacturers will be able to efficiently customize their system offerings for each cellular technology and

standard, thus enabling network evolution for service providers in a cost-effective manner.

TI's high-performance solutions enable more simultaneous voice and data calls so that **base station manufacturers** can support more user terminals including cell phones, smartphones, wireless PDAs, Internet appliances and other types of devices. This results in improved profitability for the service provider, which ensures customer satisfaction for the infrastructure system manufacturer. With higher capacity systems capable of higher data rates, service providers will be able to reduce subscriber churn and generate more revenue. In addition, TI's unmatched system expertise will help manufacturers lower development costs and rapidly deliver new 2.5G and 3G systems to market.

Generic Wireless Infrastructure System



## COMPLETE WIRELESS SIGNAL CHAIN SOLUTIONS

In wireless infrastructure (WI) systems, designers must address several cross-disciplinary issues in the signal chain or that partition of the system where signals are processed. These challenging issues involve analog, mixed-signal, DSP, and chip-rate solutions, such as operational amplifiers (op amps). Highly flexible solutions provide system designers with the right level of hardware/software partitioning for cost-effective system-level products that can be brought to market quickly. In addition, highly flexible WI systems will better protect the manufacturer's investment in software.

For 3G base station architectures and Voice-over-Packet (VoP) applications, the combination of TI's high-performance TMS320C64x™ DSP generation and its leading-edge ASIC capability provides customers with a winning wireless infrastructure solution. And, TI's unparalleled silicon expertise ensures that system designers receive state-of-the-art ASIC capability.

TI's digital upconverters (DUCs) and digital downconverters (DDCs) lead the industry in performance. These DDCs and DUCs can support multiple standards from 2G to 2.5G and 3G. With the recent introduction of the industry's best performing 14-bit 400-MSPS DAC, TI supports high-intermediate frequencies and 3G multi-carrier applications like the four-carrier W-CDMA.

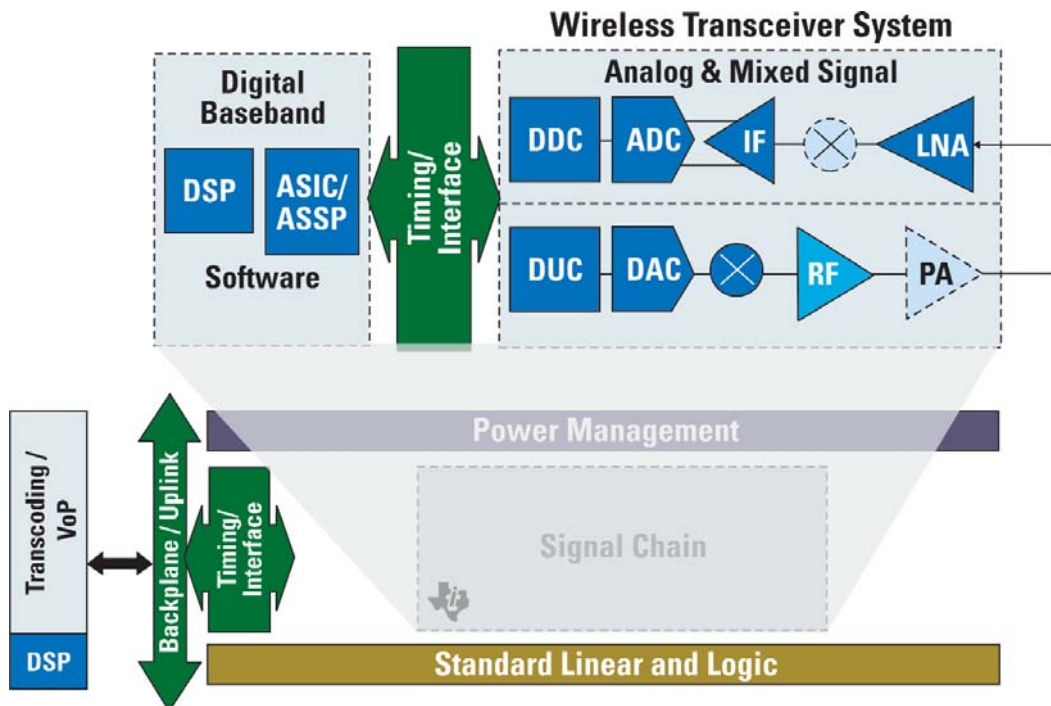
Innovative architectures and technology have made TI's operational amplifiers some of the leading solutions in the industry. For example, the patented architecture of the THS4271 makes it the only op amp to achieve low noise, low distortion, and high slew rate with unity gain stability.

And the THS4302 leverages a new fully complimentary bipolar silicon-germanium fabrication process to deliver the first op amp with over 10 GHz of gain bandwidth. These devices and a wide selection of fully differential op amps give TI the most comprehensive array of high-speed, high-performance amplifiers for wireless infrastructure applications.

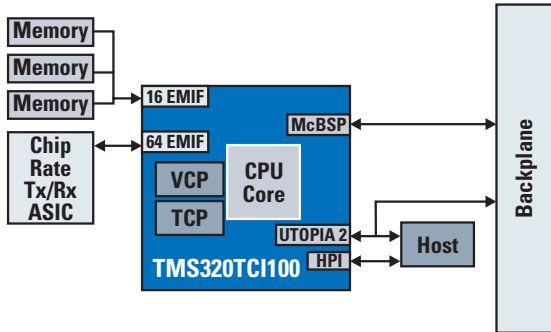
### TO KNOW MORE ►

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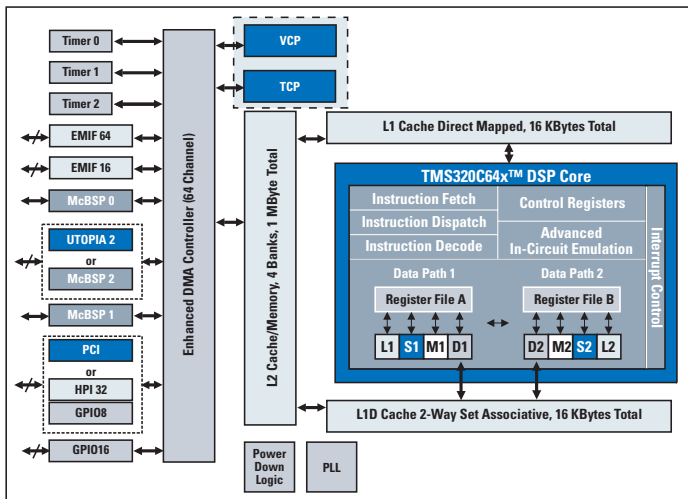
TMS320TC1100 DSP in Symbol-Rate Processing for 2G, 2.5G, and 3G Applications



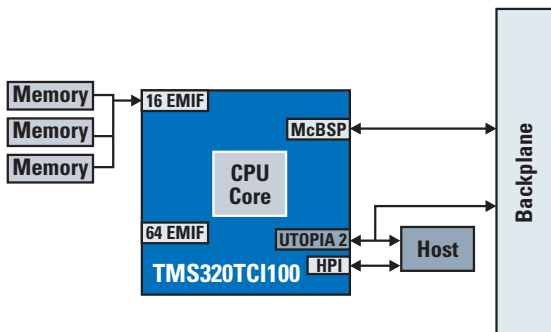
**Applications:**

- Symbol-rate processing for 2G, 2.5G, and 3G (shown above)
- Assist in chip-rate processing
- Layer 2 processing in RNC

DSP Block Diagram – TMS320TC1100 DSP



TMS320TC1100 DSP in a Voice Encode and Decode Application



**Applications:**

- Voice encode and decode (shown above)
- Network control processing
- Data formatting and routing

## HIGH-PERFORMANCE DSPs INCREASE BASE STATION SYSTEM EFFICIENCY

TMS320TC1100 DSP

Get samples and application reports at:  
[www.ti.com/sc/device/tms320tci100](http://www.ti.com/sc/device/tms320tci100)

**Key Features:**

- Industry-leading 90-nanometer process node
  - 720 MHz core performance
  - Power-efficient design (~600-mW core power)
  - High integration through state-of-the-art CMOS manufacturing process
- DSP designed for wireless infrastructure applications
  - Integrated Viterbi (VCP) and Turbo (TCP) coprocessors
  - TCP supports over 35 data (384 kbps) channels
  - VCP enables over 600 voice (7.95 kbps AMR) channels
- Complements TCI110 and TCI120 receive and transmit accelerators for wideband CDMA
- Rich mix of robust peripherals
  - Two high-bandwidth (up to 10 Gbps), flexible interfaces to external memory
  - Host port with glueless interface to most GPP
  - UTOPIA II port for interface to communication network
  - PCI for high-performance standard local bus
- Object-code compatible with all TMS320C6000™ DSPs
- Pin compatible with TMS3206415 and TMS320C6416 DSPs

## HIGH-DENSITY SOLUTIONS FOR VOICE-OVER-PACKET (VoP) AND DATA TRANSCODING

TMS320C55x™/TMS320C64x™ DSP Generations + Telogy Software

Get samples and application reports at:  
[www.ti.com/wisolutions\\_vop](http://www.ti.com/wisolutions_vop)

The TMS320TC1100 DSP also fits well in voice-transcoding, mobile switching-center, and media-gateway applications. Combining the optimized TCI100 solution with TI's high-density, field-hardened voice-over-packet (VoP) gateway solutions addresses the tough challenges facing service providers deploying packet-based networks.

**Key Features:**

- Flexible, carrier-grade solution
  - Field-proven Telogy software with over 50 million total ports shipped
  - Carrier-certified echo cancellation
- Telogy software framework optimized for the TMS320C64x and TMS320C55x DSP generations
- Extensive voice CODEC suite
  - Includes wireless codecs such as SMV, EVRC, AMR, WB-AMR and QCELP

## COMPREHENSIVE AND CUSTOMIZABLE UMTS BASEBAND SOLUTION

### UMTS Baseband Platform

TI's UMTS wireless infrastructure digital baseband platform is a comprehensive silicon and software product offering that enables the design of low-cost, high-density UMTS channel cards. The TCI1x platform supports the 3GPP FDD Release 99 standard as well as the HSDPA channels as per Release 5 of the 3GPP FDD standard. The platform consists of a high-performance wireless infrastructure tailored DSP and tightly coupled programmable accelerators. The design achieves a low cost-per-channel solution by leveraging an efficient pooling of silicon and memory resources on the chip-rate accelerators and optimally partitioning the symbol rate and chip rate functions between the DSP and accelerators.

The UMTS platform offering includes:

#### TMS320TCI100 DSP

- Industry leading 720 MHz core
- VCP and TCP coprocessors
- Pin and code compatible with TMS320C64x™ DSPs

#### TMS320TCI110

- Single device for de-spreading, RACH and searching
- Configured and controlled via DSP
- The device is highly customizable with parameters such as number of users, number of fingers per user, correlation lengths and accumulation lengths configured via DSP software
- Efficient host interface between the TCI110 and the TCI100 DSP resulting in a high-channel-density solution

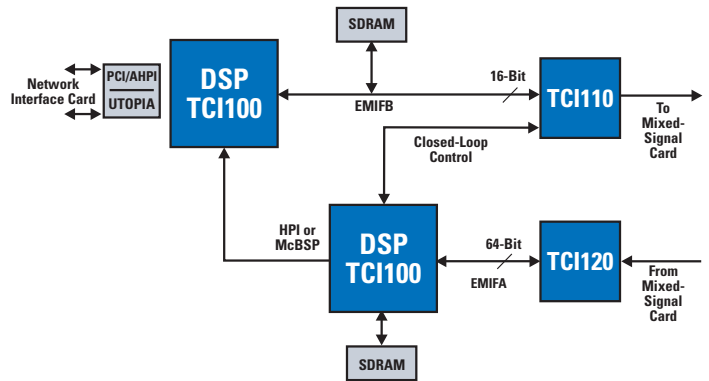
#### TMS320TCI120

- The TCI120 is a highly configurable downlink chip-rate accelerator
- Configured and controlled by the DSP
- The channel block is made up of 9 channel groups and supports a total of 288 downlink channel elements that can be configured as common or dedicated channels
- The TCI120 supports HSDPA as per Release 5 of the 3GPP standard
- Support for all the common channels, variable-rate dedicated channels, shared channels and compressed mode as per Release 99 of the 3GPP standard

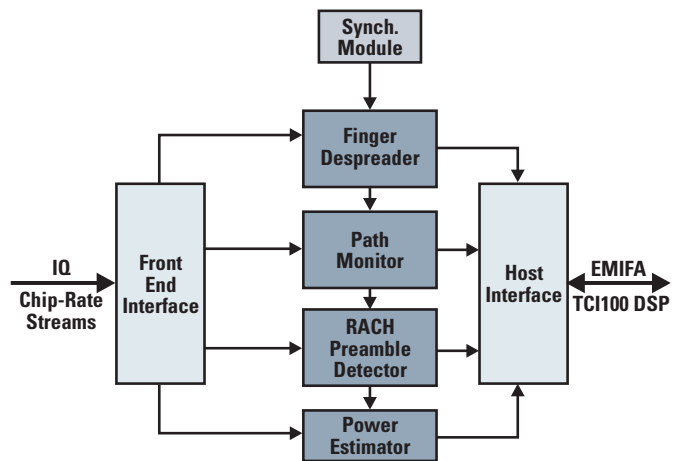
#### TCI1x Platform Software

- Physical layer reference design which includes layer 1 application and physical layer services manager
- The TCI1x hardware abstraction layer abstracts the hardware implementation details
- Highly optimized symbol- and chip-rate software modules
- TCI110 and TCI120 device control software

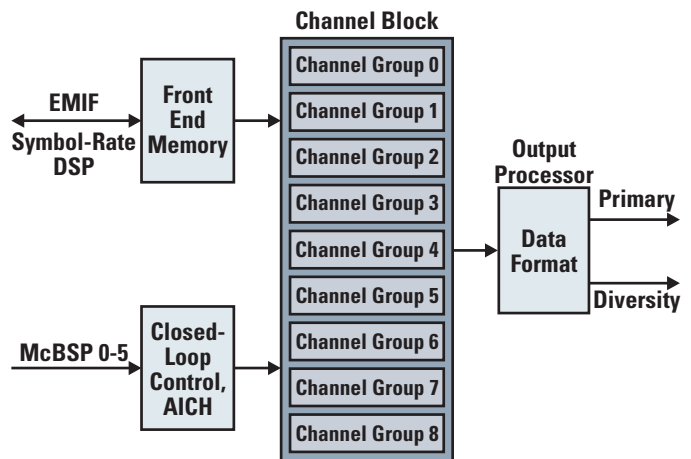
UMTS Platform-Based Channel Card



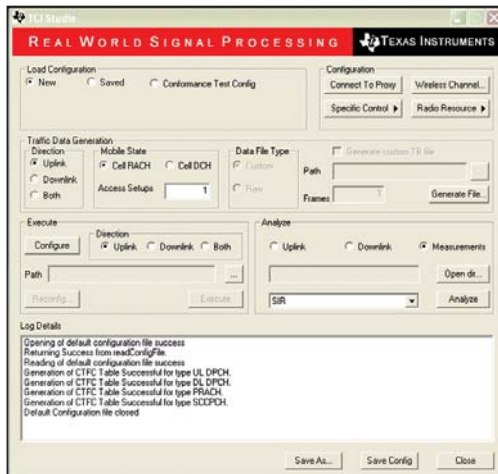
TCI110



TCI120



## TCIStudio



## TCI1x Development and Evaluation Tools

- The familiar Code Composer Studio (CCStudio) suite of development tools including the debug, profiling, and tuning tools allows for faster software development
- TCIStudio suite of evaluation and analysis tools includes accelerator probes and performance analysis tools
- The TCIStudio along with the TCI1x Evaluation Module (EVM) help carry out the evaluation and performance analysis of the TCI1x accelerators and software
- The EVM also allows for initial code development before the customer's channel card is ready

## Key Features:

- Customizable and flexible hardware configured and controlled through DSP software
- Comprehensive silicon and software UMTS baseband product offering
- TCI1x hardware abstraction layer provides a higher level of device abstraction to the user enabling them to develop a hardware independent application
- CCStudio, TCIStudio and EVM reduce the time-to-market by making software development quicker and easier

## Applications:

- Low-cost, high-channel-density UMTS channel card

# ASIC SOLUTIONS ENABLE NEXT-GENERATION WIRELESS INFRASTRUCTURE (WI)

## ASIC

For detailed information, visit:

[www.ti.com/sc/asic](http://www.ti.com/sc/asic)

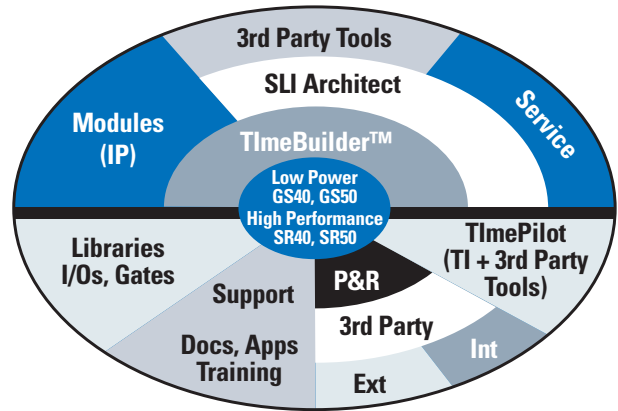
For further information, please contact your local TI Sales Representative (see page 2)

- Global leadership in semiconductor manufacturing
  - 0.18  $\mu\text{m}$  – 55 nm (Ldrawn) nodes. 95-nm (Ldrawn) Cu product 15% faster than competition
  - High-performance/density library, I/O, and memory for varying wireless infrastructure ASIC needs
  - Packaging: High-performance flip chip
- Experienced, flexible, and global design services
  - Worldwide design center staff for on-site support
  - Experienced WI applications team for system-level support
  - Collaborative design, traditional floor planning, place and route
  - Design kit with online documentation and full application notes
- System-level integration
  - Proven success on numerous multi-million gate designs
  - IP targeting WI, high-speed interfaces, and I/O (RapidIO / SerDes)
  - IP-Ethernet, DSP, microprocessor cores, broad array of peripherals
- Comprehensive ASIC cells and tool support
  - Robust module library/rich core library
  - Open EDA tool/flow support
  - Analog converter functions

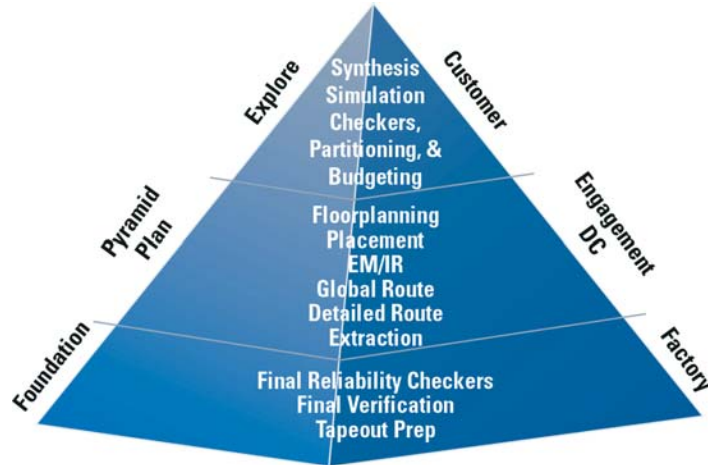
### Wireless Infrastructure Applications:

- Application-specific digital downconverter/digital upconverter
- Base-band processing
  - Chip-rate and symbol-rate processing for CDMA systems
  - Combining/decombining/bridge chips
- Specialized applications
  - Viterbi/turbo decoding
  - Switching matrix
- Network control and interface processing
  - Base station uplink
  - RNC control and protocol processor
- Transcoding/echo canceller
  - Customized applications
- Embedded SOC designs
  - High performance
  - Low peak power
- PA linearization

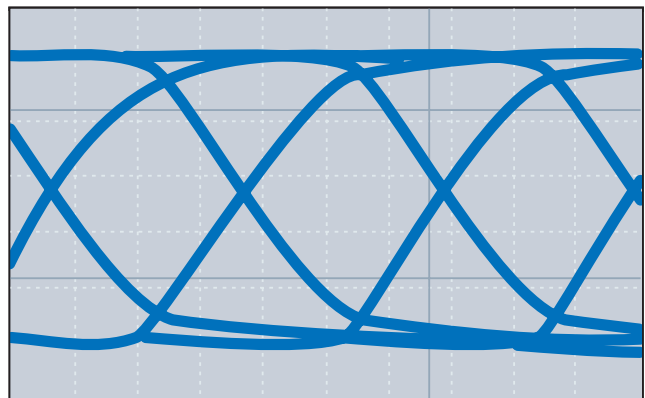
Twenty Years of ASIC Leadership



Leading-Edge EDA Tools



Leading-Edge IP: SoC with Multiple High-Performance SerDes Links at 3.2-Gbps



Measure	Current	Mean	Std Dev	Markers	X	Y
V p-p (1)	263.95 mW	266.13 mW	1.6868 mW	----- (1)	24.587 ns	-66.00 mV
Frequency (1)	114 GHz	? 220.5 GHz ?	131.9 GHz ?	----- (1)	24.852 ns	69.80 mV
V base (1)	-105.43 mW	-103.81 mW	7.1021 mW	Δ	265.26 ps	135.80 mV
V base (2)	Source off	-----	-----	1/ΔX	3.770 GHz	

(1) Scale: 44.8 mV/div    (2) Scale: 1.0 mV/div    Time: 100.0 ps/div    Trigger Level: -380 mV  
 Offset: -27.5 mV    Offset: 0.0 mV    Delay: 24.1876 ns

General Overview

Signal Chain

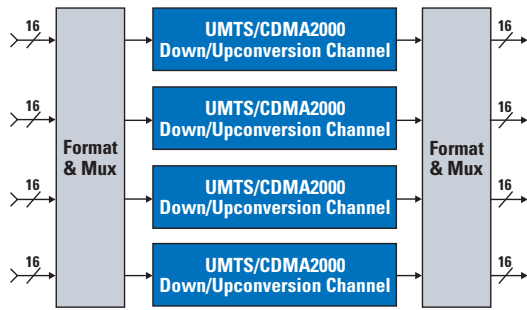
Timing & Interface

Logic

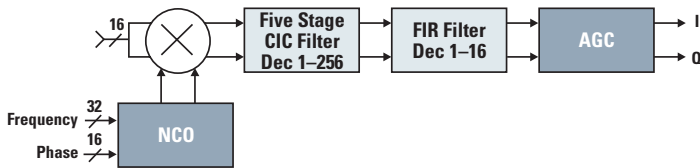
Power Management



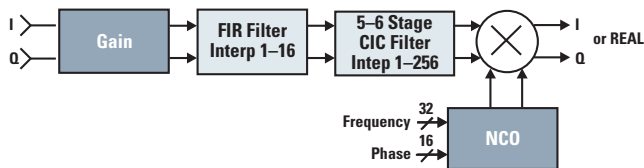
GC5016 Internal Block Diagram



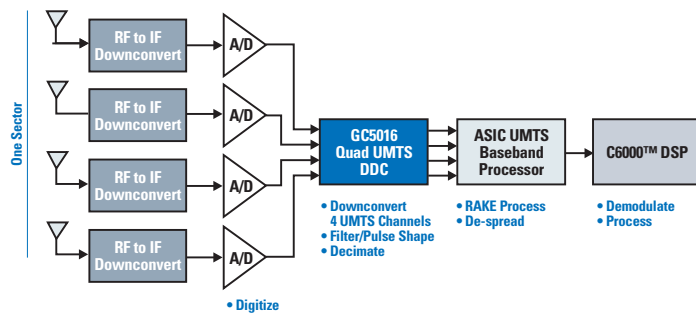
Downconversion Mode Channel Detail



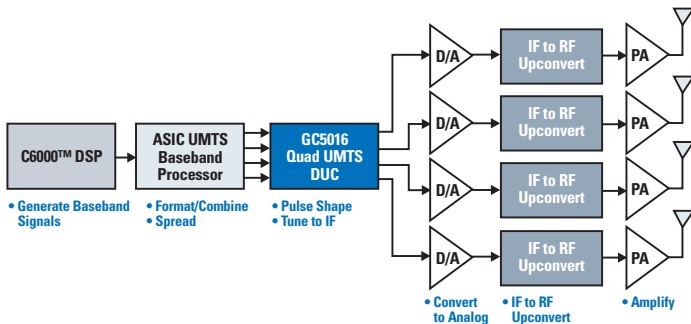
Upconversion Mode Channel Detail



GC5016 UMTS Four-Element Beamform Base Station Receiver



GC5016 UMTS Four-Element Beamform Base Station Transmitter



## PROGRAMMABLE QUAD DDC OR DUC FOR 3G SYSTEMS



GC5016

Get samples, datasheets, application reports, and EVMs at: [www.ti.com/sc/device/gc5016](http://www.ti.com/sc/device/gc5016)

Each one of the GC5016's four channels can be independently programmed to perform digital upconversion or downconversion of 3G systems such as W-CDMA or CDMA2000. Customers can choose to use the device as a programmable digital upconverter or downconverter. Alternatively, they can use the device to implement a two-channel upconversion and a two-channel downconversion simultaneously on a single chip.

As with its predecessors, the GC5016 continues to offer the best performance in the industry by delivering better than 115 dB of spurious-free dynamic range, exceeding industry requirements. While the maximum input data rate for each channel is the fastest in the industry (at 150 MSPS) by more than 35%, it can provide even faster input data rates of up to 300 MSPS by combining two channels for even wider bandwidth applications.

In the upconversion mode, the GC5016 accepts real or complex signals, interpolates them, and modulates them to selected intermediate frequencies that are then output to a digital-to-analog converter, such as the DAC904, DAC2904, or DAC5686. In the downconversion mode, the GC5016 accepts digital signals from an analog-to-digital converter, such as the ADS5410.

### Key Features:

- Input clock rates
  - Up to 150 MSPS
  - Up to 300 MSPS in two-channel even/odd mode
- SFDR: 115 dB
- Integrated AGC
- FIR filter block consists of 16 cells providing up to 256 filter taps per channel
- 64 parallel input bits and 64 parallel output bits provide flexible I/O options
- Multiple multiplex output options
- Future-proof filter performance, clock rate, and bandwidth
- Power dissipation: 1 W at 100 MHz with all four channels in operation

### Applications:

- Process four-channel UMTS in both downconvert or upconvert modes, as well as combination upconvert and downconvert mode
- Efficient and economic beamforming
- Low power is ideal for micro and pico base stations

## QUAD DIGITAL UPCONVERTER PROVIDES TWO 3G W-CDMA CHANNELS

### GC4116

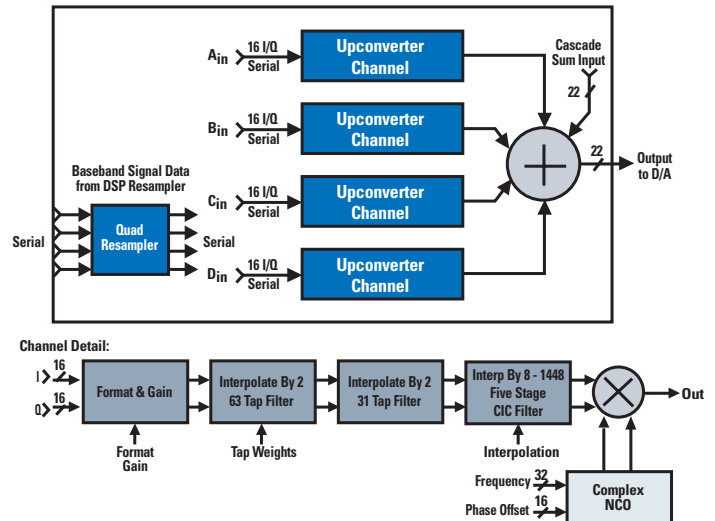
Get samples, datasheets, and IBIS models at: [www.ti.com/sc/device/gc4116](http://www.ti.com/sc/device/gc4116)

The GC4116 is the first digital upconverter (DUC) to support multiple standards. The chip can upconvert four narrowband channels and up to two UMTS/CDMA2000-3x channels. The GC4116 also can directly accept QPSK, GMSK, or QAM symbols for transmit filtering or pulse shaping.

#### Key Features:

- Output rates up to 106 MSPS
- Four identical upconvert channels
- 16-bit real or complex inputs, with summed output
- Independent frequency, phase and gain controls
- Serial interface controller simplifies interfacing with ASICs or DSPs
- Low power: 117 mW (per GSM channel), up to 305 mW (per UMTS channel)

GC4116 DUC Block Diagram



#### Applications:

- Wireless base transceiver stations: macro, micro, and pico
- Repeaters
- Wireless local loop
- Cable headend and customer premise equipment

## QUAD DIGITAL DOWNCONVERTER ENABLES UMTS, MULTI-STANDARD DOWNCONVERSION

### GC4016

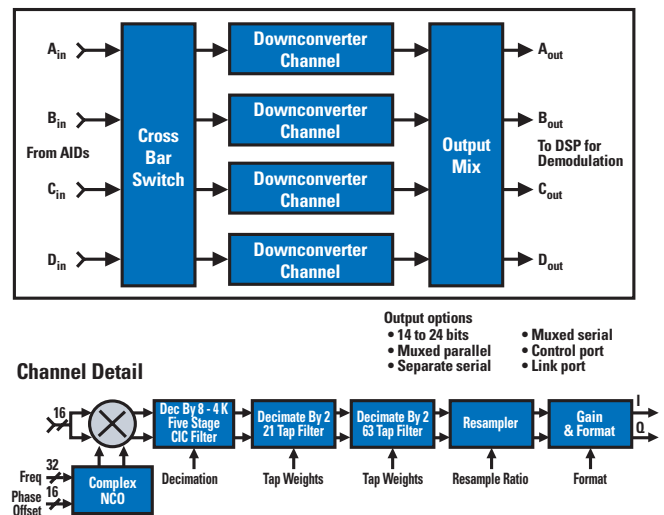
Get samples, datasheets, and IBIS models at: [www.ti.com/sc/device/gc4016](http://www.ti.com/sc/device/gc4016)

The GC4016 is the first digital downconverter (DDC) supporting multiple wireless standards, including 3G standards. The GC4016 can downconvert two UMTS/CDMA2000-3x with 2x oversampling or one channel with 4x oversampling.

#### Key Features:

- Input rates up to 100 MSPS
- Four independent Digital Down Convert (DDC) channels
- Independent decimation and resampling, tuning, phase and gain controls
- Built-in diagnostics
- > -115 dBc spurious free dynamic range
- Low power: 115 mW (per GSM channel), up to 620 mW (per 3.84-MB UMTS channel)

GC4016 DUC Block Diagram



#### Applications:

- Cellular base transceiver stations: macro, micro, and pico
- Repeaters
- Wireless local loop
- Cable headend and customer premise equipment

General Overview

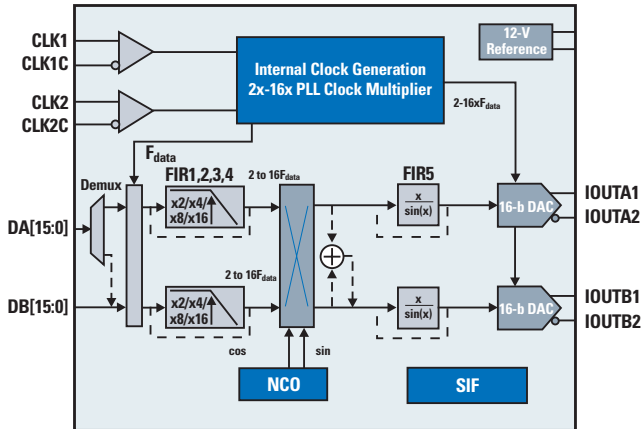
Signal Chain

Timing & Interface

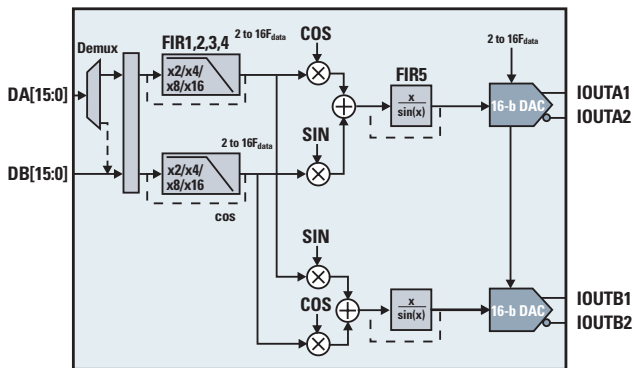
Logic

Power Management

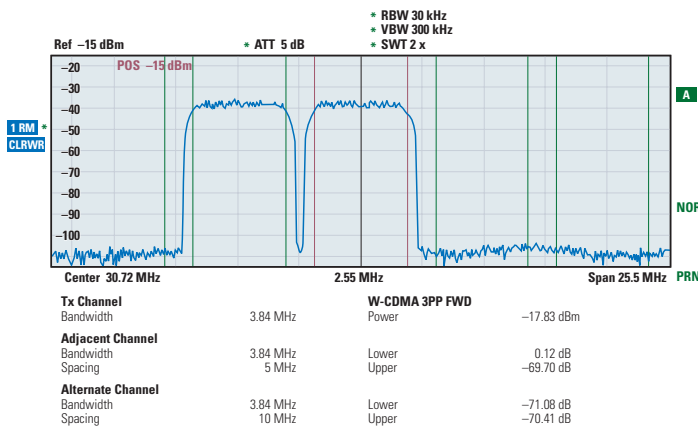
DAC5686 Internal Block Diagram



DAC5686 in Single Sideband Mode



DAC5686 Performance Plot



**Applications:**

- Cellular BTS
  - CDMA: W-CDMA, CDMA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/UWC-136
- Baseband I&Q transmit
- Low-data-rate interface for quadrature modulation
- Single sideband upconversion
- Diversity transmit

**16-BIT, 500-MSPS PROGRAMMABLE DUAL DAC**



**DAC5686**

Get datasheets at:  
[www.ti.com/sc/device/dac5686](http://www.ti.com/sc/device/dac5686)

DAC5686 is designed to allow low data rate transfer from the ASIC to the DAC. The DAC5686's superior performance enables transmissions of up to four W-CDMA carriers at high intermediate frequencies. The DAC5686 can be used in three modes of operation.

**A. Dual-Channel**

The interpolation filters increase the DAC update rate, resulting in reduced  $\sin x / x$  roll off. This greatly relaxes the requirements for analog-post filtering.

**B. Quadrature Modulation Mode**

This mode is used for baseband modulation or a two-channel digital IF system. While channel selection is done through complex mixing in the ASIC, the DAC5686 interpolates this incoming low-data-rate signal into higher-data rates. Then, on-chip mixing using a flexible 32-bit programmable NCO provides the final IF upconversion. Optional  $f_s/4$  mixing is available for lower power operation.

**C. Single Sideband Upconversion Mode**

This mode gives users the best interface to an analog upconverter, such as the TRF3701, for low-cost transmit solution. Complex mixing using the NCO can be used to offset the baseband signal from the LO frequency. The LO feed through an unwanted side band can then be attenuated by IF filtering at RF.

**Key Features:**

- 500-MSPS maximum DAC update rate
- 71 dBc SNR in 100-kHz BW for  $f_{OUT} \leq 40$  MHz
- 82 dB IMD for four-tone CW input signal, each tone at -12 dBFS ( $f_{OUT} = 15.6, 15.8, 16.2, 16.4$  MHz)
- Low power dissipation: 440 mW (SSB mode)
- Selectable 2x to 16x interpolation, dual-channel
- On-chip 2x-16x PLL clock multiplier, PLL bypass mode
- Differential scalable current outputs: 2 mA to 20 mA
- 1.8-V digital / 3.3-V analog supply
- 1.8-V / 3.3-V CMOS-compatible interface
- Packaging: 100-HTQFP (PowerPAD™)

**W-CDMA ACPR Performance:**

- W-CDMA 1 carrier:
  - 74-dBc baseband, 245.76 MSPS
  - 77-dBc IF = 30.72 MHz, 245.76 MSPS
  - 71-dBc IF = 61.44 MHz, 245.76 MSPS
- W-CDMA 2 carrier:
  - 74-dBc IF = 30.72 MHz, 245.76 MSPS
  - 71-dBc IF = 61.44 MHz, 245.76 MSPS
  - 67-dBc IF = 122.88 MHz, 491.52 MSPS
- W-CDMA 4 carrier:
  - 67-dBc IF = 61.44 MHz, 245.76 MSPS
  - 64-dBc IF = 122.88 MHz, 491.52 MSPS

## 14-BIT, 400-MSPS DAC WITH 2X/4X INTERPOLATION

### DAC5674

Get samples, datasheets, app reports and EVMs at: [www.ti.com/sc/device/dac5674](http://www.ti.com/sc/device/dac5674)

The DAC5674 is a digital-to-analog converter integrated with a cascade of up to two 2x interpolation filters. The digital filtering option allows either a low pass or high pass mode which enables users to select the higher-order image for increased output frequency, potentially reducing an IF mixer stage. The low-pass interpolation mode provides excellent SFDR performance that enables multi-carrier architectures in the first Nyquist zone of up to 40-MHz IF with relaxed filter requirements.

#### Key Features:

- High W-CDMA ACPR:
  - 73 dB @ 15.36-MHz single carrier
  - 70 dB @ 46.08-MHz single carrier and 19.2-MHz dual carrier
- 2x or 4x interpolation with configurable low-pass/high-pass mode
- On-chip PLL with bypass option
- 1.8-V Digital and 3.3-V Analog supply operation
- 1.8-V/3.3-V CMOS-compatible interface
- Packaging: 48-lead PowerPAD™ HTQFP

## DUAL DACS FOR I & Q PROCESSING

### DAC2900, DAC2902, DAC2904

Get samples, datasheets, and EVMs at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

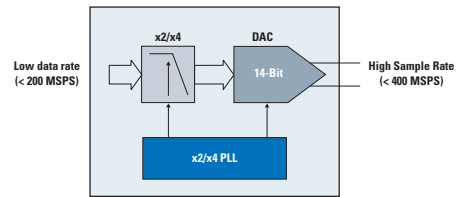
Replace partnumber in URL with *dac2900*, *dac2902*, or *dac2904*

The two integrated DAC channels of the DAC290x family enable the I and Q channels to have close gain matching to maintain low error-vector magnitudes. These channels also provide high performance at low cost and low power. The 10-, 12-, and 14-bit family is pin compatible, allowing easy resolution upgrades.

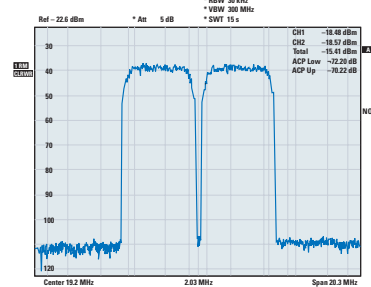
#### Key Features:

- High SFDR:
  - DAC2900: 68 dB at  $f_{OUT} = 20$  MHz
  - DAC2902: 70 dB at  $f_{OUT} = 20$  MHz
  - DAC2904: 78 dB at  $f_{OUT} = 10$  MHz
- Power: 310 mW
- Power-down mode: 23 mW
- Low glitch: 2 pVs
- Internal reference
- Packaging: 48-lead TQFP

DAC5674 Internal Block Diagram



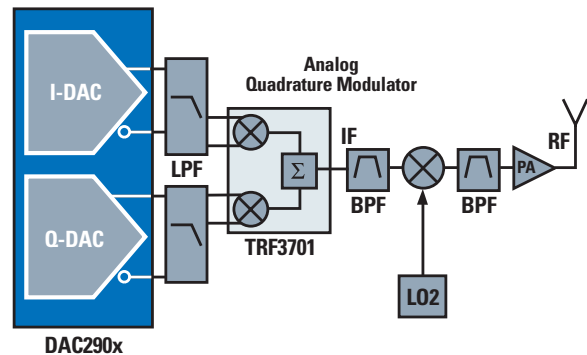
Dual-Carrier W-CDMA with ACPR of 70 dB @ 19.2 MHz



#### Applications:

- Cellular BTS:
  - CDMA: W-CDMA, CMDA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/UWC-136
- Low-data-rate interface
- Wireless local loop

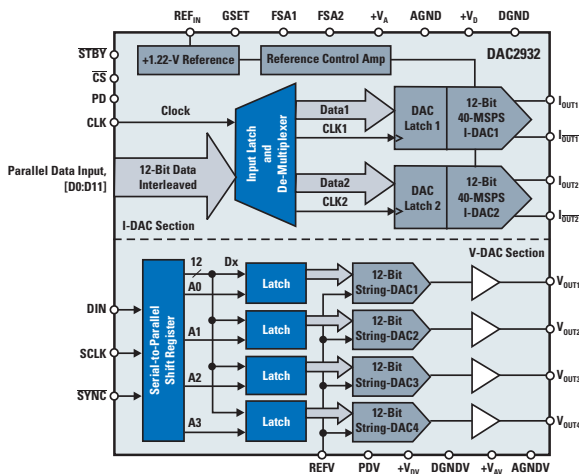
DAC290x in Baseband Sampling Transmitter System



#### Applications:

- Base stations, WLL, WLAN
- Direct digital synthesis (DDS)
- Baseband sampling transmitter
- Diversity transmitter

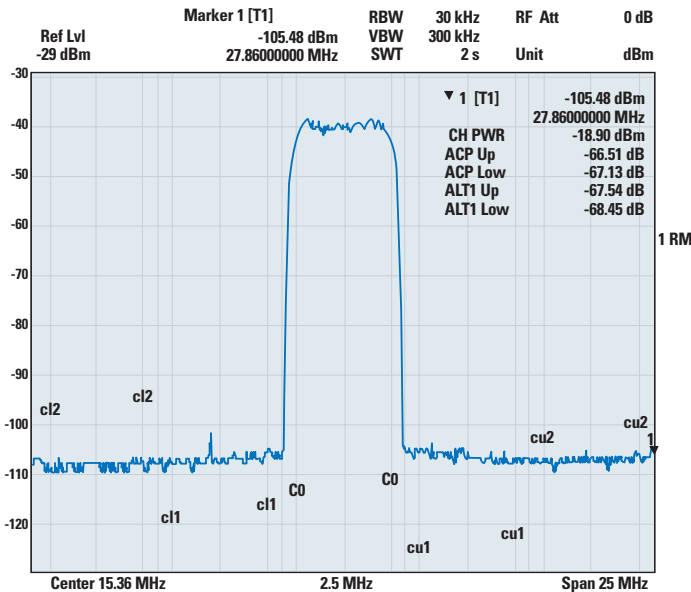
DAC2932 Functional Block Diagram



**Applications:**

- Transmit channels
  - I and Q
  - PC card modems: GPRS, CDMA
  - Wireless network cards (NICs)
- Signal synthesis (DDS)
- Portable medical instrumentation
- Arbitrary waveform generation (AWG)

Single-Channel W-CDMA Signal on DAC904 with 15.36-MHz Input @ 122.88 MSPS



**Applications:**

- Transmit channel
  - Wireless base station
  - Wireless local loop
  - Digital microwave

## ULTRA-LOW-POWER 12-BIT, 40-MSPS DUAL DAC

### DAC2932

Get samples, datasheets, app reports and EVMs at: [www.ti.com/sc/device/dac2932](http://www.ti.com/sc/device/dac2932)

The DAC2932 is a 12-bit 40-MSPS dual DAC with four integrated voltage output control DACs. This DAC can be used for I and Q in wireless applications. The additional four voltage output control DACs provide wireless system cost savings by allowing the designer to control transmit and receive path gain and adjust filter and local oscillator frequencies. The use of these four control DACs simplifies the system design, provides flexibility and can provide overall system cost savings.

**Key Features:**

- Dual 12-bit, 40-MSPS current output DACs
- Four 12-bit  $V_{out}$  DACs for signal path control
- Ultra low power: 29 mW
- Adjustable full-scale output: 0.5 mA to 2 mA
- 3.3-V supplies
- Power down mode: 25  $\mu$ W
- Budgetary pricing: U.S. \$7.95/1 KU
- Packaging: 48-lead TQFP

## LOW-COST, SINGLE DAC FAMILY

### DAC904/DAC902/THS5671A/THS5661A

Get samples, datasheets, and EVMs at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace *partnumber* in URL with *dac904*, *dac902*, *ths5671a*, or *ths5661a*

The DAC90x and THS56x1A families are pin-compatible, single DACs with 8-bit, 10-bit, 12-bit, and 14-bit options. These are the lowest-cost DACs available on the market.

**Key Features:**

- Update rate of 165 MSPS (DAC90x); 125 MSPS (THS56x1A)
- Analog supply of 5 V; digital supply of 3 V or 5 V
- On-chip, 1.2-V reference
- Set-up and hold times of 1 ns
- Twos complement or binary input code format (THS56x1A)
- Differential current outputs of 2 mA to 20 mA
- SFDR > 60 dBc at 27.4 MHz IF at 165 MSPS
- Low power: 175 mW at 5 V
- Packaging: 28-pin SOIC, 28-pin TSSOP (10- and 8-bit versions are also available for both families)

## QUADRATURE MODULATORS

TRF3701/TRF3702

**Product Preview**

Get datasheets at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

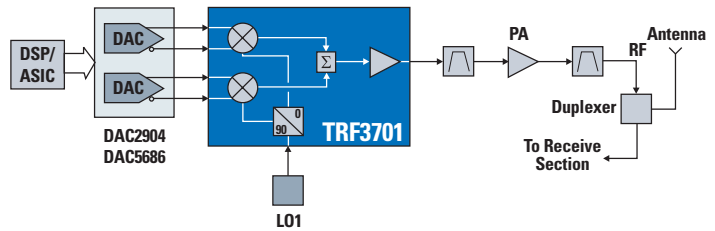
Replace partnumber in URL with trf3701 or trf3702

TRF3701 and TRF 3702 are low-noise quadrature-direct modulators capable of converting complex input signals from 0–250 MHz IF up to RF. An internal analog combiner sums the real and imaginary components of the RF output. The modulators are implemented as a double-balanced mixer. An internal LO phase splitter accommodates a single LO input.

**Key Features:**

- TRF3701: IF to 900 MHz
- TRF3702: IF to 2 GHz
- Typical optimized carrier suppression > 50 dBc
- Typical optimized sideband suppression > 50 dBc
- Typical noise floor; -157 dBm/Hz at 700 to 900 MHz
- 5-V single supply

TRF3701 and TRF3702 in Direct Upconversion Architecture



**Applications:**

- Cellular BTS
  - CDMA: W-CDMA, CDMA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/UWC-136
- Wireless local loop
- Wireless LAN 802.11
- LMDS, MMDS

## INTEGER-N RF PLL SYNTHESIZER

TRF3750

**Product Preview**

Get samples, datasheets, app reports and EVMs at:

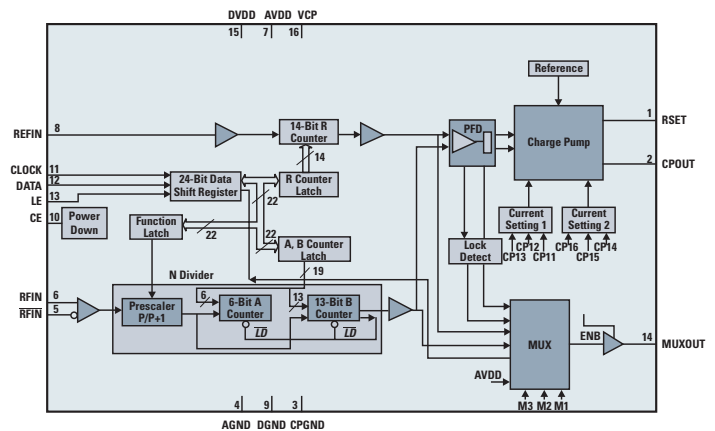
[www.ti.com/sc/device/trf3750](http://www.ti.com/sc/device/trf3750)

The TRF3750 is frequency synthesizer that can be used to implement local oscillators (LO) up to 3 GHz in the RF upconversion and downconversion chains of wireless transmitters and receivers. A complete Phase Locked Loop (PLL) can be implemented using an external loop filter and a Voltage-Controlled Oscillator (VCO) together with the TRF3750. The very wide frequency range simplifies system complexity and reduces cost.

**Key Features:**

- Supports operation up to 3 GHz
- Supply voltage of 2.7 V to 5.5 V
- Programmable charge pump currents
- Programmable anti-backlash pulse width
- Analog and digital lock detect
- Low phase noise
- Extended VCO control range through independent VCP supply
- Hardware and software power down
- Packaging: 16-lead TSSOP

TRF3750 Internal Block Diagram



**Applications:**

- Cellular BTS:
  - CDMA: W-CDMA, CMDA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/UWC-136
- Portable wireless communications equipment
- Wireless local loop
- Communications test equipment

General Overview

Signal Chain

Timing & Interface

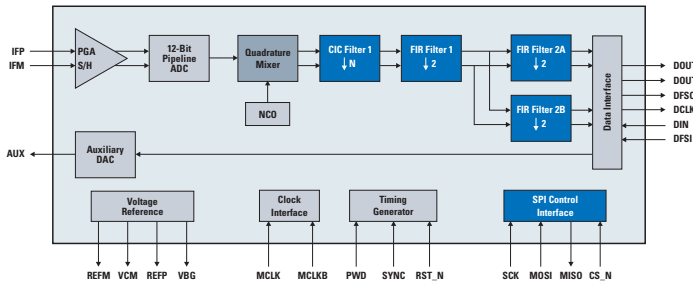
Logic

Power Management

IF Sampled Receive Channel



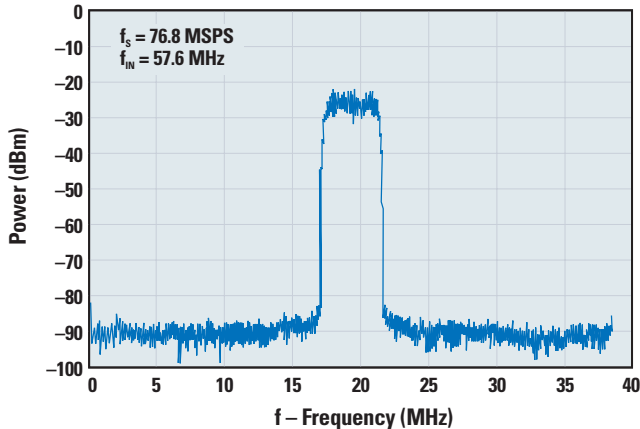
Detailed AFE8201 Block Diagram



Applications:

- Receivers

W-CDMA Single-Carrier Measurement



Applications:

- Performance supports across cellular standards
  - W-CDMA / CDMA2000 / GPRS / EDGE / GSM / IS-95
- Wireless local loop / LMDS / MMDS
- Point-to-point microwave

## 12-BIT ADC WITH INTEGRATED DDC

### AFE8201

Get samples, datasheets, app reports and EVMs at:

[www.ti.com/sc/device/afe8201](http://www.ti.com/sc/device/afe8201)

The AFE8201 is an 80-MSPS, 12-bit ADC that includes a digital downconverter (DDC) and user-programmable digital filters. It is designed to sample IF signals and digitally mix, filter, and decimate the signals to baseband. An integrated 12-bit DAC is included to control the gain of the IF block. This highly integrated device simplifies and reduces costs for receiver applications.

Key Features:

- 12-bit, 80-MSPS ADC
- Integrated digital down converter
- 32-bit NCO
- Digital filters
- User-programmable coefficients
- McBSP interface for TI DSPs
- 12-bit control DAC
- Budgetary pricing: U.S. \$25/1 KU

## LOWEST-POWER, LOWEST-COST ADC FOR BTS RECEIVERS

### ADS5410

Get samples, datasheets, and EVMs at:

[www.ti.com/sc/device/ads5410](http://www.ti.com/sc/device/ads5410)

The 12-bit, 80-MSPS ADC offers the lowest power at this performance level. It is a low-cost alternative to expensive 14-bit ADCs and can be implemented in cost-reduction programs for existing systems or startup of 3G systems.

Key Features:

- 12 bit, 80 MSPS
- SFDR: 75 dB at 100-MHz IF
- SNR: 60 dB at 70-MHz IF
- Digital outputs from 1.6 V – 3.3 V in 2s complement
- Flexible clocking: Single-ended or differential
- Power: 360 mW

## 50-MHz TO 400-MHz CASCADEABLE IF AMPLIFIERS

### THS9000/THS9001

Get samples, datasheets, app reports and EVMs at:

[www.ti.com/partnumber](http://www.ti.com/partnumber)

Replace partnumber in URL with *ths9000* or *ths9001*

The THS9000 and THS9001 are medium power, cascadeable, gain block optimized for 50-MHz to 400-MHz IF frequencies. The amplifiers incorporate internal impedance matching to 50  $\Omega$ . The part mounted on the standard EVM achieves greater than 15 dB input and output return loss from 50 MHz to 325 MHz with  $V_S = 5$  V,  $R_{BIAS} = 237$   $\Omega$ ,  $L_{COL} = 470$  nH. Design requires only 2 dc blocking capacitors, 1 power supply bypass capacitor, 1 RF choke, and 1 bias resistor. The THS9000 comes in a very small 2x2-mm leadless MSOP package, and the THS9001 comes in a 6-pin SOT23 package. These devices make excellent choices for driving SAW filters, buffering LOs, or general-purpose IF amplifiers.

#### Key Features:

- OIP<sub>3</sub>: 37 dBm at 300 MHz
- Gain: 15.5 dB
- Noise figure: 4.0 dB at 300 MHz
- 1 dB compression: 20.6 dBm

## HIGH-SPEED, FULLY DIFFERENTIAL OP AMP

### THS4502/THS4503

Get samples, datasheets, and EVMs at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

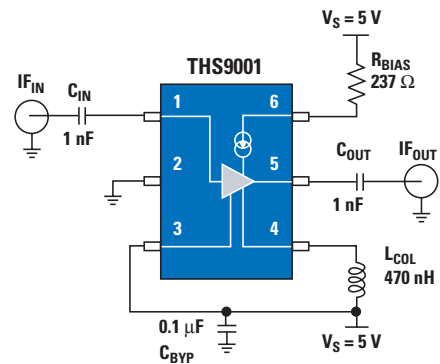
Replace partnumber in URL with *ths4502* or *ths4503*

The THS4502, featuring power-down capability, and the THS4503, without power-down capability, set new performance standards for fully differential amplifiers with unsurpassed linearity, supporting 14-bit operation through 40 MHz.

#### Key Features:

- 370-MHz bandwidth ( $V_{CC} = \pm 5$  V,  $R_f = 392$   $\Omega$ ,  $G = 0$  dB)
- Slew rate: 2800 V/ $\mu$ s
- OIP<sub>3</sub> = +38 dBm at 30 MHz ( $G = 12$  dB)
- NF = 25 dB ( $G = 12$  dB)
- Differential input/differential output
- Output common-mode voltage control
- Balanced architecture rejects common-mode noise and reduces even order harmonic distortion

THS9001 Block Diagram

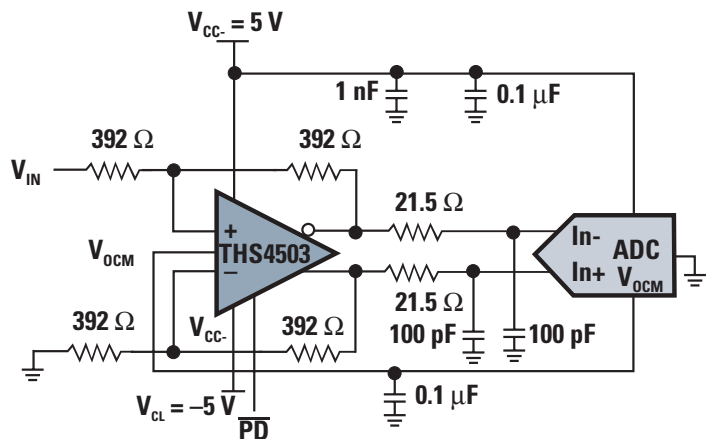


- $V_S = 3$  V to 5 V
- $I_S$  is adjustable
- Packaging: 6-lead (leadless) MSOP, SOT23-6

#### Applications:

- IF amplifier
- TDMA: GSM, IS-136, EDGE/UWE-136
- CDMA: IS-95, UMTS, CDMA2000
- Wireless local loop
- Wireless LAN: IEEE 802.11
- Radio links

THS4503 Block Diagram

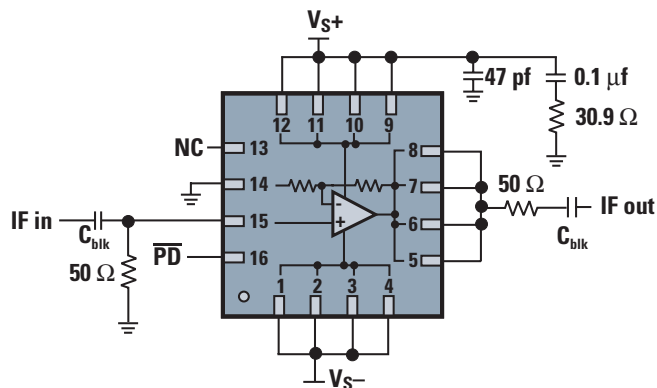


#### Applications:

- Single-ended to differential conversion
- Differential ADC driver
- Active differential anti-alias filter



THS4302 Block Diagram

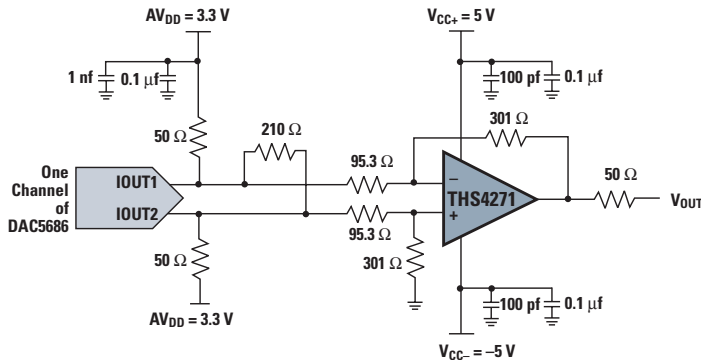


### Single-Supply IF Amplifier Application Circuit, $G = 8$ dB into 50- $\Omega$ Load

#### Applications:

- High-frequency signal processing
- LO drive
- High-frequency ADC drivers
- High-speed DAC buffers

Differential to Single-Ended Conversion of High-Speed DAC Output



For test data, see DAC5686 graph, page 11

#### Applications:

- Low-noise differential to single-ended conversion
- Differential line receiver
- Active anti-alias filtering

## FIXED-GAIN, HIGH-SPEED OP AMP WITH POWER DOWN

### THS4302

Get samples, datasheets, and EVMs at:

[www.ti.com/sc/device/thS4302](http://www.ti.com/sc/device/thS4302)

The THS4302 is an ultra-low-distortion, single-supply-operation, wide-bandwidth, high-speed amplifier ideal for use with high-resolution data converters. These voltage feedback amplifiers can operate from a single 5-V power supply while delivering a performance level of -88 dBc third-order intermodulation distortion (IMD<sub>3</sub>) at 100 MHz.

#### Key Features:

- 2.4-GHz bandwidth
- $G = 14$  dB (non-inverting)
- Slew rate: 5500 V/ $\mu$ s
- NF = 16 dB
- OIP<sub>3</sub> = 39 dBm at 100 MHz ( $R_L = 100 \Omega$ )
- High output drive,  $I_O = \pm 180$  mA (typ)
- $V_S = 3$  V to 5 V
- Evaluation module available
- Packaging: Leadless packages

## ULTRA-LOW-DISTORTION, HIGH-SPEED OP AMPS WITH SHUTDOWN

### THS4271/THS4275

Get samples, datasheets, and EVMs at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with *ths4271* or *ths4275*

The THS4271 and THS4275 are ultra-low distortion and noise, single-ended 5-V operation, wide-bandwidth, high-speed amplifiers. They are ideal for use with high-resolution data converters. These voltage-feedback amplifiers have a power supply range of 4.5 V to 15 V while delivering a performance level of -90 dB of harmonic distortion (THD) at 30 MHz.

#### Key Features:

- HD<sub>2</sub> = -92 dBc ( $f = 30$  MHz,  $R_L = 150 \Omega$ ,  $V_O = I_{VPP}$ )
- HD<sub>3</sub> = -95 dBc ( $f = 30$  MHz,  $R_L = 150 \Omega$ ,  $V_O = I_{VPP}$ )
- 3-nV/ $\sqrt{\text{Hz}}$  input noise voltage
- 1.4-GHz bandwidth (-3 dB,  $G = +1$ )
- Slew rate: 1000 V/ $\mu$ s
- 25-ns settling time (0.1%)
- High output drive,  $I_O = 160$  mA (typ)
- Wide range of power supplies:  $\pm 2.5$  V to  $\pm 7.5$  V

## 2-GHz, LOW DISTORTION, CURRENT FEEDBACK AMPLIFIER

### THS3202

Get samples, datasheets, app reports and EVMs at: [www.ti.com/sc/device/ths3202](http://www.ti.com/sc/device/ths3202)

The THS3202 is a low-distortion, high slew rate op amp ideally suited for applications driving loads sensitive to distortion at high frequencies. It provides well-regulated AC performance characteristics with a power supply range of 6.6 to 15 V. The device's low differential gain/phase error makes it ideal for video line driver applications, test and measurement systems and RF and IF amplifier stages.

#### Key Features:

- Unity-gain bandwidth: 2 GHz
- High slew rate: 9000 V/ $\mu$ s
- IMD<sub>3</sub> at 120 MHz: -89 dBc (ref measurement circuit)
- OIP<sub>3</sub> at 120 MHz: 43 dBm (ref measurement circuit)
- NF = 17.5 dB (ref measurement circuit)
- High output current:  $\pm$ 115 mA into 20  $\Omega$  R<sub>L</sub>
- Power supply voltage range: 6.6 V to 15 V
- Packaging: 8-lead SO, 8-lead MSOP

## 3–9-GHz GBW, ULTRA-LOW NOISE, VOLTAGE FEEDBACK OP AMPS

### OPA846/OPA847

Get samples and datasheets at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

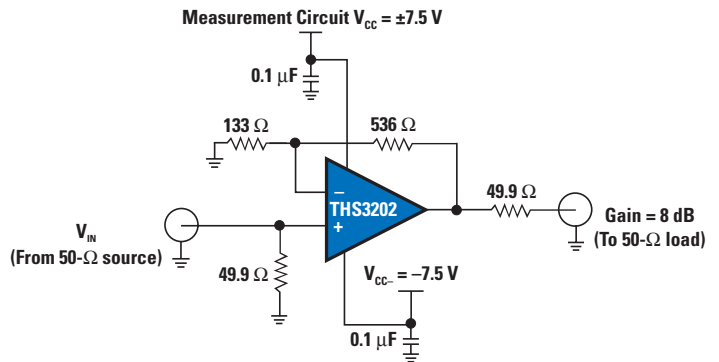
Replace partnumber in URL with opa846 or opa847

The OPA847 combines very-high-gain bandwidth and large signal performance with an ultra-low input noise voltage (0.85 nV/ $\sqrt{\text{Hz}}$ ), while using only 18 mA of supply current. As a voltage gain stage, the OPA847 is optimized for a flat frequency response at a gain of +20 V/V and is stable down to gain as low as +12 V/V. New external compensation techniques allow the OPA847 to be used at any inverting gain with excellent frequency response control. Using this technique in a differential ADC interface application, as shown, can deliver one of the highest dynamic range interfaces available.

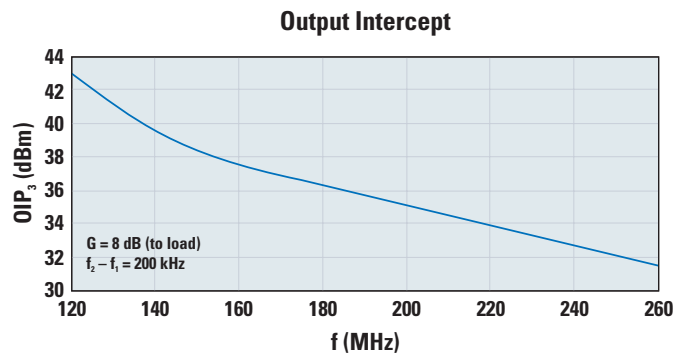
Device	Minimum Operating Gain (V/V)	GBW (MHz)	Input Noise Voltage nV/ $\sqrt{\text{Hz}}$	Offset Voltage Drift (0 to 70°C) max (mV/°C)	Offset Current Drift (0 to 70°C) max (nA/°C)	Price Starts at 1K
OPA842	1	200	2.60	4	2	\$1.45
OPA843	3	800	2.00	4	2	\$1.49
OPA846	7	1750	1.20	1.5	2	\$1.59
OPA847 <sup>†</sup>	14	3800	0.85	1.5	2	\$1.89
OPA656*	1	230	7.00	12	0.9	\$3.19
OPA657*	7	1600	4.80	12	0.9	\$3.59

\*JFET input trimmed offset drift low grade specifications shown. High grade available with <math><6 \mu\text{V}/^\circ\text{C}</math> max. drift.

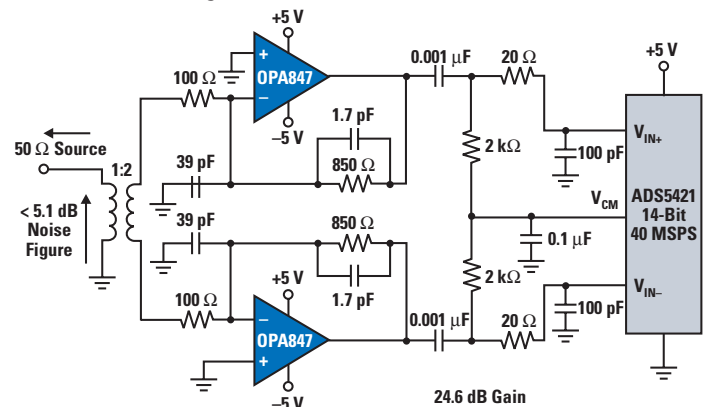
THS3202 Block Diagram



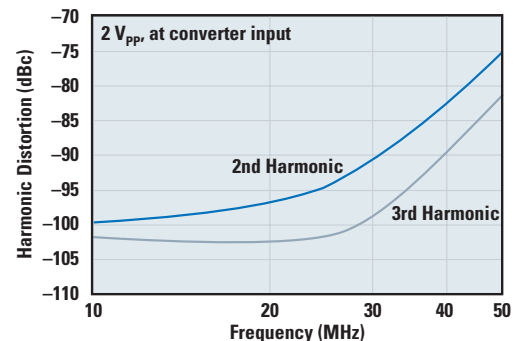
THS3202 Performance Characteristics



OPA847 Block Diagram



Differential OPA847 Driver Distortion



#### Applications:

- High dynamic range ADC preamps
- Wideband, high gain amplifiers

General Overview

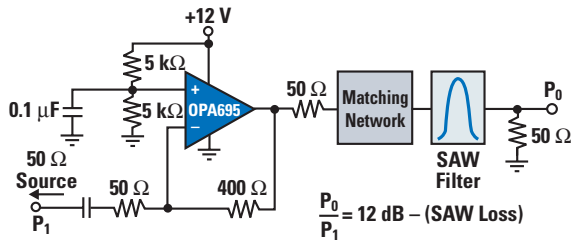
Signal Chain

Timing & Interface

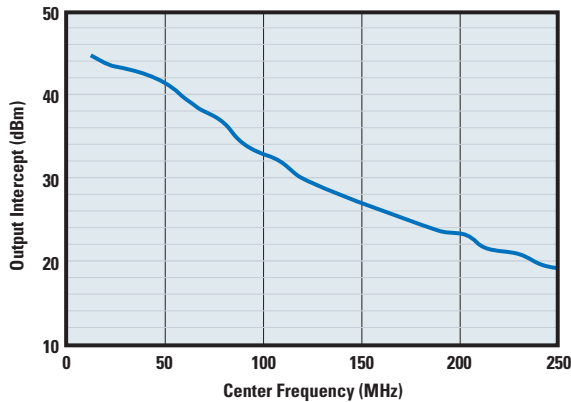
Logic

Power Management

Low Distortion, 12-dB Gain SAW Driver



2-Tone 3rd-Order Intermodulation Intercept



## ULTRA-WIDE BAND, CURRENT FEEDBACK OP AMP WITH DISABLE OPA695

Get samples and datasheets at: [www.ti.com/sc/device/opa695](http://www.ti.com/sc/device/opa695)

The OPA695 is a very-high bandwidth, current-feedback op amp that combines 4200-V/μs slew rate and low-input voltage noise to deliver a precision, low-cost, high-dynamic range IF amplifier. Optimized for high-gain operation, the OPA695 is ideally suited to buffering SAW filters.

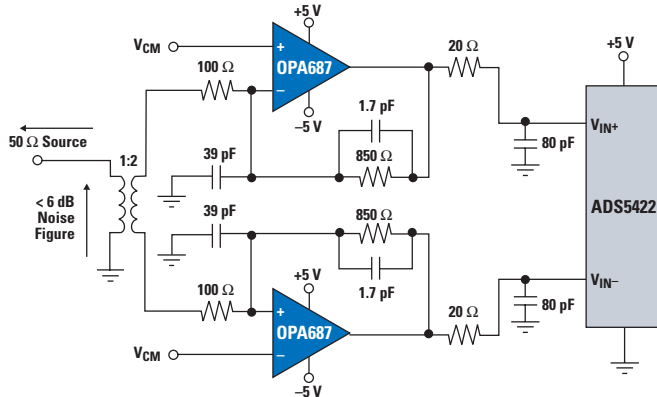
### Key Features:

- Gain = +2 bandwidth: 900 MHz
- Gain = +8 bandwidth: 420 MHz
- Ultra-high slew rate: 4200 V/μs
- 3rd order intercept: > 40 dBm (f < 50 MHz)

### Applications:

- Very wideband ADC driver
- Video line driver
- ARB waveform output driver

Ultra-High Dynamic Range Differential Input ADC Driver



## WIDEBAND, ULTRA-LOW-NOISE, VOLTAGE FEEDBACK AMPLIFIER OPA687

Get samples and datasheets at: [www.ti.com/sc/device/opa687](http://www.ti.com/sc/device/opa687)

The OPA687 combines a very high gain bandwidth and large signal performance with an ultra-low input noise voltage while dissipating only 18-mA supply current. The low input noise voltage and its very-high, two-tone intercept can be used as a fixed-gain IF amplifier.

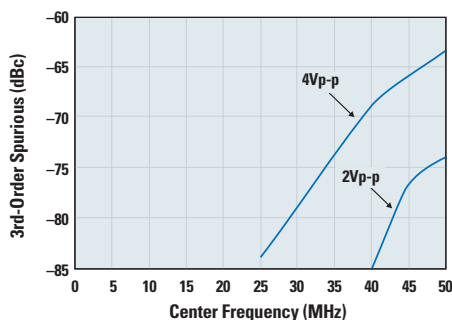
### Key Features:

- High gain bandwidth: 3.8 GHz
- Low input voltage noise: 0.95 nV/√Hz
- Stable for G ≥ 12
- Two-tone, 3rd-order intercept: 43 dBm

### Applications:

- RF/IF amplifier
- Low-distortion ADC driver

Measured 2-Tone, 3rd-Order Distortion for Differential ADC Driver



## 16-BIT RISC FLASH MCU FOR ONLY \$0.99

### MSP430F11x1

Get samples, datasheet, application reports, and EVMs at: [www.ti.com/sc/msp430](http://www.ti.com/sc/msp430)

A new class of low-power, advanced RISC-architecture MCUs, TI's family of Flash-based MSP430 MCUs consume just 250 micro-amps at 1 MHz and feature TI's analog and digital signal processing expertise.

#### Key Features:

- Ultra-low-power consumption, 250- $\mu$ A active, 0.8- $\mu$ A standby at 2.2 V (typ)
- 16-bit RISC architecture enables new applications at a fraction of the code size
- Integrated analog comparator is ideal for precise mixed-signal measurement
- Multifunctional, 16-bit multichannel timer with PWM, capture, and compare capability
- In-system programmable Flash permits last-minute code changes, field upgrades, and data logging to Flash
- The MSP-FET430X110 offers a completely integrated development environment for only U.S. \$49
- New, small 4x4-mm QFN packaging available 4Q 2003

## 16-BIT RISC FLASH MCU WITH INTEGRATED 12-BIT ADC, MULTIPLIER, AND USARTs

### MSP430F14x

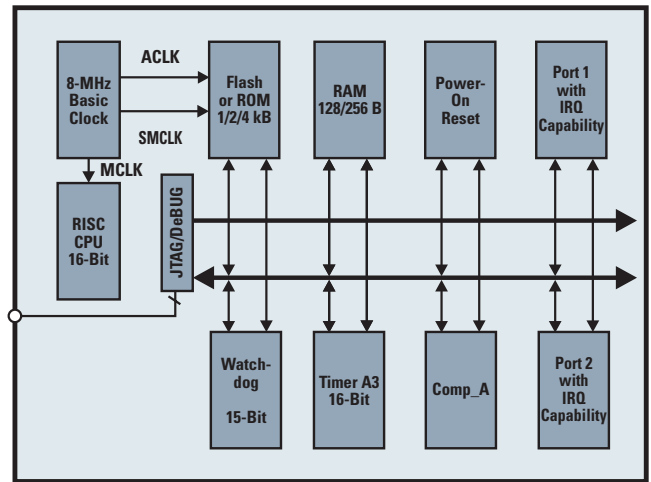
Get samples, datasheets, application reports, and EVMs at: [www.ti.com/sc/msp430](http://www.ti.com/sc/msp430)

Experience the ultimate SoC solution for low-power applications. The MSP430F14x features the combination of ultra-low power consumption and integrated high-performance analog peripherals ideal for cost, power, and space-sensitive applications.

#### Key Features:

- Ultra-low power consumption: 250- $\mu$ A active mode, 0.8- $\mu$ A standby mode at 2.2 V (typ)
- 16-bit RISC architecture enables new applications at a fraction of the code size
- High-performance integrated analog and digital peripherals including a 200-kSPS, 12-bit A/D converter, to reduce system cost and speed time-to-market
- Serial communication interface (USART) functions as asynchronous UART or synchronous SPI interface
- Two 16-bit PWM timers allow highly flexible multichannel capture and compare
- In-system programmable Flash permits last-minute code changes, field upgrades, and data logging to Flash
- The MSP-FET430P140 offers a completely integrated development environment for only U.S. \$99

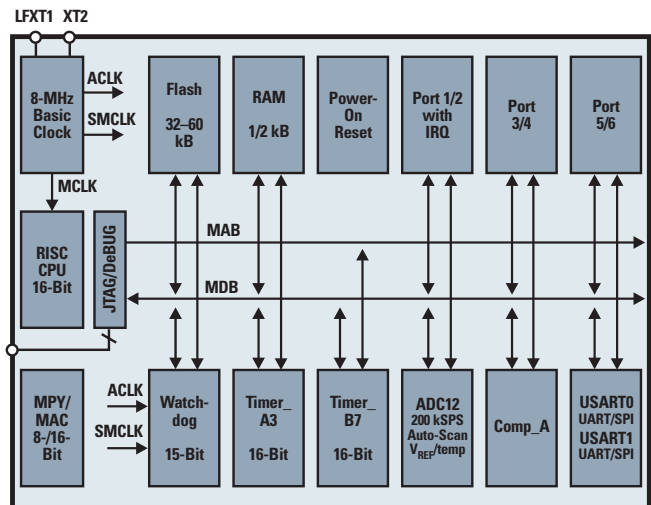
MSP430F11x1 Block Diagram



#### Applications:

- Monitoring and control
- Can support initialization of CDC7005 clock synchronizer

MSP430F14x Block Diagram



#### Applications:

- Monitoring and control

General Overview

Signal Chain

Timing & Interface

Logic

Power Management

# HIGH-SPEED AMPLIFIERS

Part Number		Architecture								Supply Voltage	A <sub>CL</sub> Min	BW MHz	Slew Rate V/μs	Settling Time to 0.1% / 0.01% ns (typ)	THD 1 MHz dBc (typ)	Differential Gain/Phase %/°	V <sub>N</sub> V/√Hz	V <sub>OS</sub> mV (max)	I <sub>b</sub> μA (max)	I <sub>s/amp</sub> mA (typ)	I <sub>OUT</sub> mA (typ)	Price <sup>1</sup>				
		Single	Dual	Triple	Quad	VFB	CFB	Diff I/O	FET														PGA	C-Stable	Shutdown	3 V
<b>Voltage-Feedback Op Amps</b>																										
THS4001					•					•	•	•	1	270	400	40	–	-72	0.04	0.15	12.5	8	5	7.8	100	2.19
THS4011	THS4012				•					•	•	•	1	290	310	37	90	-80	0.01	0.01	7.5	6	6	7.8	110	2.29/3.81
THS4021	THS4022				•					•	•	•	10	350	470	40	145	-72	0.02	0.08	1.5	2	6	7.8	100	1.67/2.79
THS4031	THS4032				•					•	•	•	2	100	100	60	90	-90	0.015	0.025	1.6	2	6	8.5	90	2.23/3.68
THS4041	THS4042				•					•	•	•	1	165	400	120	250	-89	0.01	0.01	14	10	6	8	100	1.25/2.49
THS4051	THS4052				•					•	•	•	1	70	240	60	130	-89	0.01	0.01	14	10	6	8.5	100	1.20/1.55
THS4061	THS4062				•					•	•	•	1	180	400	40	140	-72	0.02	0.02	14.5	8	6	7.8	115	1.52/1.92
THS4081	THS4082				•					•	•	•	1	175	230	43	233	-79	0.01	0.05	10	7	6	3.4	85	1.79/2.78
THS4271					•								1	1400	970	25	38	<-120	0.007	0.004	2.8	10	18	22	90	2.69
THS4275					•					*	*	*	1	1400	970	25	38	<-120	0.007	0.004	2.8	10	18	22	90	2.69
THS4601					•					•	•	•	1	440	100	135	170	-77			5.4	4	100 pA	10	80	9.95
OPA355	OPA2355	OPA3355			•					•	•	•	1	450	300	30	120	-81	0.02	0.05	5.8	9	50 pA	8.3	60	1.20/1.99/2.82
OPA356	OPA2356				•					•	•	•	1	450	300	30	120	-81	0.02	0.05	5.8	9	50 pA	8.3	60	1.10/1.90
OPA627					•					•	•	•	1	16	55	450	550	–	–	–	4.5	0.1	5 pA	7	45	8.28
OPA637					•					•	•	•	2	80	135	300	450	–	–	–	4.5	0.1	5 pA	7	45	8.28
OPA642					•					•	•	•	1	450	380	11.5	13	-95	0.007	0.008	2.3	1	45	22	60	3.75
	OPA2652				•					•	•	•	1	700	335	–	–	-77	0.05	0.03	8	7	15	11	140	1.19
OPA655					•					•	•	•	1	400	290	8	17	-92	0.006	0.009	6	2	125 pA	25	60	9.13
OPA656					•					•	•	•	1	500	290	10	–	-85	0.02	0.05	7	1.8	20 pA	14	70	5.85
OPA657					•					•	•	•	7	350	700	10	–	-78	–	–	4.8	1.8	20 pA	14	70	7.29
OPA686	OPA2686				•					•	•	•	7	250	600	16	18	-83	0.02	0.02	1.3	1	17	12.4	80	2.89
OPA687					•					•	•	•	12	600	900	15	17	-85	–	–	0.95	1	33	18.5	80	3.49
OPA688					•					•	•	•	1	530	1000	–	7	–	0.02	0.01	6.3	6	12	15.8	100	2.65
OPA689					•					•	•	•	4	280	1600	–	7	-64	0.02	0.01	4.6	5	12	15.8	100	2.95
OPA690	OPA2690	OPA3690			•					•	•	•	1	500	1700	8	–	-83	0.06	0.01	4.5	4	8	5.5	190	1.50/2.32/3.19
	OPA2822				•					•	•	•	1	400	170	32	–	-95	0.02	0.03	2	1.2	12	4.8	150	2.17
<b>THS4303</b>										•	•	•	<b>5</b>	<b>2500</b>	<b>1000</b>	<b>5</b>		<b>-92</b>	–	–	<b>2.4</b>	<b>0.5</b>	<b>6</b>	<b>34</b>	<b>100</b>	–
<b>THS4304</b>										•	•	•	<b>1</b>	<b>2500</b>	<b>1000</b>	<b>5</b>		<b>-92</b>	–	–	<b>2.4</b>	<b>0.5</b>	<b>6</b>	<b>18</b>	<b>100</b>	–
<b>OPA842</b>										•	•	•	<b>1</b>	<b>350</b>	<b>400</b>	<b>15 ns</b>		–	<b>0.003</b>	<b>0.006</b>	<b>2.6</b>	<b>0.3</b>	<b>20</b>	<b>20.2</b>	<b>±100</b>	<b>1.35</b>
<b>OPA843</b>										•	•	•	<b>3</b>	<b>500</b>	<b>1000</b>	<b>7.5 ns</b>		–	<b>0.001</b>	<b>0.012</b>	<b>2</b>	<b>0.3</b>	<b>20</b>	<b>20.2</b>	<b>±100</b>	<b>1.39</b>
<b>OPA846</b>										•	•	•	<b>7</b>	<b>500</b>	<b>625</b>	<b>10 ns</b>		–	<b>0.02</b>	<b>0.02</b>	<b>1.2</b>	<b>0.15</b>	<b>10</b>	<b>12.6</b>	<b>±80</b>	<b>1.59</b>
<b>OPA847</b>										•	•	•	<b>12</b>	<b>600</b>	<b>950</b>	<b>10 ns</b>		–	–	–	<b>0.85</b>	<b>0.1</b>	<b>19</b>	<b>18.1</b>	<b>100/-75</b>	<b>1.49</b>
<b>THS9000</b>										•	•	•	<b>5.8</b>	<b>500</b>	–	–	–	–	–	–	<b>0.6</b>	–	–	<b>100</b>	–	–
<b>THS9001</b>										•	•	•	<b>5.8</b>	<b>500</b>	–	–	–	–	–	–	<b>0.6</b>	–	–	<b>100</b>	–	–
<b>OPA698</b>										•	•	•	<b>1</b>	<b>450</b>	<b>1100</b>	<b>8 ns</b>		–	<b>0.012</b>	<b>0.008</b>	<b>5.6</b>	<b>2</b>	<b>3</b>	<b>15.5</b>	<b>±120</b>	<b>1.79</b>
<b>OPA699</b>										•	•	•	<b>6</b>	<b>285</b>	<b>1500</b>	<b>7 ns</b>		–	–	–	<b>4.1</b>	<b>0.5</b>	<b>8</b>	<b>15.5</b>	<b>±100</b>	<b>1.85</b>
<b>Current-Feedback Op Amps</b>																										
THS3001					•					•	•	•	1	420	6500	40	–	-96	0.01	0.02	1.6	3	10	7.5	120	3.37
THS3061	THS3062				•					•	•	•	1	300	7000	30	125	–	0.02	0.01	2.6	0.7	2	8.3	145	2.95/4.25
	THS3112				•					•	•	•	1	110	1550	63	–	-78	0.01	0.011	2.2	8	23	4.9	270	3.03
	THS3115				•					•	•	•	1	110	1550	63	–	-78	0.01	0.011	2.2	8	23	4.9	270	3.03
	THS3122				•					•	•	•	1	160	1550	64	–	-80	0.01	0.011	2.2	6	23	8.4	440	3.75
	THS3125				•					•	•	•	1	160	1550	64	–	-80	0.01	0.011	2.2	6	23	8.4	440	3.75
OPA658	OPA2658				•					•	•	•	1	900	1700	11.5	15	-82	0.025	0.02	2.7	4.5	18	4.5	80	1.95/3.12/4.99
OPA684	OPA2684	OPA3684/ OPA4684			•					•	•	•	1	170	780	–	–	-82	0.04	0.02	3.7	1.5	5	3.4	160	1.3/1.97

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

Preview devices are listed in blue.  
New devices are listed in red.  
Continued on next page

## HIGH-SPEED AMPLIFIERS (CONTINUED)

Part Number		Architecture								Supply Voltage				A <sub>CL</sub> Min	BW MHz	Slew Rate V/μs	Settling Time to 0.1% / 0.01%		THD 1 MHz dBc (typ)	Differential Gain/Phase %/°		V <sub>N</sub> V/√Hz	V <sub>OS</sub> mV (max)	I <sub>b</sub> μA (max)	I <sub>s/amp</sub> mA (typ)	I <sub>OUT</sub> mA (typ)	Price <sup>1</sup>	
		Single	Dual	Triple	Quad	VFB	CFB	Diff I/O	FET	PGA	C-Stable	Shutdown	3 V				5 V	± 5 V		± 15 V	V/V							ns (typ)
<b>Current-Feedback Op Amps (Continued)</b>																												
THS3201/	THS3202																										1.87/2.89	
OPA685																											1.89	
OPA691	OPA2691	OPA3691																									1.45/2.32/3.15	
<b>OPA693</b>																											<b>1.35</b>	
<b>OPA695</b>																											-	
<b>THS3201</b>																											<b>1.59</b>	
<b>Fixed-Gain Amplifiers</b>																												
<b>THS4302</b>																												<b>1.97</b>
BUF634																											2.84	
OPA633																											5.15	
OPA692		OPA3692																									1.35/2.98	
THS9000																											1.00	
THS9001																											1.00	
<b>Variable-Gain Amplifiers</b>																												
<b>THS7530</b>																											<b>3.65</b>	

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

Preview devices are listed in blue.  
New devices are listed in red.

## D/A CONVERTERS

Device Name	Resolution (Bits)	Supply (V)	Update Rate (MSPS)	Settling Time (ns)	Number of DACs	Power Typ (mW)	DNL Max (±LSB)	INL Max (±LSB)	Pin/Package	Price <sup>1</sup>
DAC904	14	3.0 to 5.0	165	30	1	170	1.75	2.5	28 SOP 28 TSSOP	6.25
THS5671A	14	3.0 to 5.0	125	35	1	175	3.5	7	28 SOP 28 TSSOP	8.00
DAC902	12	3.0 to 5.0	165	30	1	170	1.75	2.5	28 SOP 28 TSSOP	6.25
THS5661A	12	3.0 to 5.0	125	35	1	175	2.0	4	28 SOP 28 TSSOP	6.25
DAC900	10	3.0 to 5.0	165	30	1	170	0.5	1	28 SOP 28 TSSOP	4.25
THS5651A	10	3.0 to 5.0	125	35	1	175	0.5	1	28 SOP 28 TSSOP	4.25
DAC2904	14	3.3 to 5.0	125	30	2	310			48TQFP	20.19
DAC2902	12	3.3 to 5.0	125	30	2	310	2.5	3	48 TQFP	15.41
DAC2900	10	3.3 to 5.0	125	30	2	310	1	1	48 TQFP	9.19
DAC5675	14	3	400	5	1	820	2	4	48 HTQFP	29.75
<b>DAC5686</b>	<b>14</b>	<b>1.8/3.3</b>	<b>500</b>	<b>12</b>	<b>2</b>	<b>400</b>	<b>TBD</b>	<b>TBD</b>	<b>100 HTQFP</b>	<b>42.00</b>
DAC2932	12	2.7 to 3.3	40	25	2	29	0.5	2	48 TQFP	7.95
DAC5674	12	1.8/3.3	400	20	1	420	2	3.5	48 HTQFP	21.00

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

Preview devices are listed in blue.

## A/D CONVERTERS

Device Name	Resolution (Bits)	Sample Rate (MSPS)	Supply (V)	Analog Inputs	Power Typ (mW)	Analog Input BW (MHz)	DNL Max (±LSB)	INL Max (±LSB)	SNR (dB)	Pin/Package	Price <sup>1</sup>
ADS5410	12	80		1	360	1000	1	2	67	48 TQFP	23.00
ADS5422	14	62	5	1	1200	300	1		72	64 TQFP 64 LQFP	29.00
ADS809	12	80	5	1	880	1000	1.7	6	65	48 TQFP	23.75
AFE8201*	12	80	2.7 to 3.3	1	450	1000	1	2	67	48 TQFP	25.00

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

\*AFE8201 integrates programmable DDC, PG4, and Control DAC. Directly interfaces to TI TMS320C5000™ and TMS320C6000™ DSP platforms with McBSP port.

General Overview

Signal Chain

Timing & Interface

Logic

Power Management

## DIGITAL DOWNCONVERTERS/UPCONVERTERS (DDC/DUC)

Device	Max Clock Rate	Conversion Type	Narrowband Channels <sup>2</sup>	Wideband Channels <sup>3</sup>	Automatic Gain Control	Input Resolution	Output Resolution	SFDR	Power (max) / Channel	Special Features	Price <sup>1</sup>
GC5016	150	Up and/or down	4	4	✓	16	16	115	250	RSSI meters, programmable filters, real or complex data formats	65.00
GC4016	100	Down	4	2		16	24	115	115	Resampler, serial, or parallel output formats	48.00
GC4116	105	Up	4	2	NA	16	22	115	150	Resampler, IS-95/CDMA phase equalization	48.00
GC1012B	100	Down	–	1		12	16	75	850	Fixed decimate by 2, 4, 8, 16, 32, or 64	–

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

<sup>2</sup>DAMPS, GSM, IS-95, CDMA2001X

<sup>3</sup>UMTS, DOCSIS, QAM

## MSP430 ULTRA-LOW-POWER MICROCONTROLLERS

Device <sup>1</sup>	Program (kB)	SRAM	I/O	WDT	Timer A	Timer B	USART	I <sup>2</sup> C	SVS	BOR	MPY	Comp A	ADC	DAC	Pins/Package	Price <sup>2</sup>
<b>Flash-Based F1xx Family<sup>3</sup> (V<sub>CC</sub> 1.8 to 3.6 V)</b>																
MSP430F1101A	1	128	14	✓	✓							✓	Slope		20 DGV, DW, PW, 24 RGE	0.99
MSP430C1101	1	128	14	✓	✓							✓	Slope		20 DW, PW, 24 RGE	0.60
MSP430F1111A	2	128	14	✓	✓							✓	Slope		20 DGV, DW, PW, 24 RGE	1.34
MSP430C1111	2	128	14	✓	✓							✓	Slope		20 DW, PW, 24 RGE	1.10
MSP430F1121A	4	256	14	✓	✓							✓	Slope		20 DGV, DW, PW, 24 RGE	1.66
MSP430C1121	4	256	14	✓	✓							✓	Slope		20 DW, PW, 24 RGE	1.34
MSP430F1122	4	256	14	✓	✓								5-ch ADC10		20 DW, PW, 32 RHB	1.99
MSP430F1132	8	256	14	✓	✓								5-ch ADC10		20 DW, PW, 32 RHB	2.23
MSP430F122	4	256	22	✓	✓		1					✓	Slope		28 DW, PW, 32 RHB	2.11
MSP430F123	8	256	22	✓	✓		1					✓	Slope		28 DW, PW, 32 RHB	2.26
MSP430F1222	4	256	22	✓	✓		1						8-ch ADC10		28 DW, PW, 32 RHB	2.36
MSP430F1232	8	256	22	✓	✓		1						8-ch ADC10		28 DW, PW, 32 RHB	2.49
MSP430F133	8	256	48	✓	✓	✓	1					✓	8-ch ADC12		64 PM, RTD, PAG	2.98
MSP430F135	16	512	48	✓	✓	✓	1					✓	8-ch ADC12		64 PM, RTD, PAG	3.59
MSP430C1331	8	256	48	✓	✓	✓	1					✓	Slope		64 PM, RTD	1.97
MSP430C1351	16	512	48	✓	✓	✓	1					✓	Slope		64 PM, RTD	2.27
MSP430F147	32	1024	48	✓	✓	✓	2					✓	8-ch ADC12		64 PM, RTD, PAG	5.01
MSP430F1471	32	1024	48	✓	✓	✓	2					✓	Slope		64 PM, RTD, PAG	4.60
MSP430F148	48	2048	48	✓	✓	✓	2					✓	8-ch ADC12		64 PM, RTD, PAG	5.71
MSP430F1481	48	2048	48	✓	✓	✓	2					✓	Slope		64 PM, RTD	5.30
MSP430F149	60	2048	48	✓	✓	✓	2					✓	8-ch ADC12		64 PM, RTD, PAG	6.03
MSP430F1491	60	2048	48	✓	✓	✓	2					✓	Slope		64 PM, RTD	5.60
MSP430F155 <sup>4</sup>	16	512	48	✓	✓	✓	1	✓	✓	✓		✓	8-ch ADC12	2-ch DAC12	64 PM	4.95
MSP430F156 <sup>4</sup>	24	1024	48	✓	✓	✓	1	✓	✓	✓		✓	8-ch ADC12	2-ch DAC12	64 PM	5.65
MSP430F157 <sup>4</sup>	32	1024	48	✓	✓	✓	1	✓	✓	✓		✓	8-ch ADC12	2-ch DAC12	64 PM	5.85
MSP430F167 <sup>4</sup>	32	1024	48	✓	✓	✓	2	✓	✓	✓	✓	✓	8-ch ADC12	2-ch DAC12	64 PM	6.73
MSP430F168 <sup>4</sup>	48	2048	48	✓	✓	✓	2	✓	✓	✓	✓	✓	8-ch ADC12	2-ch DAC12	64 PM	7.45
MSP430F169 <sup>4</sup>	60	2048	48	✓	✓	✓	2	✓	✓	✓	✓	✓	8-ch ADC12	2-ch DAC12	64 PM	7.95
MSP430F1610 <sup>4</sup>	32	5120	48	✓	✓	✓	2	✓	✓	✓	✓	✓	8-ch ADC12	2-ch DAC12	64 PM	8.45
MSP430F1611 <sup>4</sup>	48	10240	48	✓	✓	✓	2	✓	✓	✓	✓	✓	8-ch ADC12	2-ch DAC12	64 PM	8.95

<sup>1</sup>C = ROM, F = Flash

<sup>2</sup>Suggested resale unit price in U.S. dollars in quantities of 1,000.

<sup>3</sup>All devices support industrial temperature range.

<sup>4</sup>Planned release 1Q 2004.

## TIMING AND INTERFACE PRODUCTS

Wireless Infrastructure (WI) systems will accommodate a wider range of technologies than ever before as the industry moves from 2G to 2.5G and 3G. Advanced wireless technologies like Bluetooth™ personal area networking (PAN), wireless local area networking (WLAN) with IEEE 802.11 technology, and leading wireless protocols like GSM, CDMA, and UMTS all place higher demands on WI systems for greater processing performance without jeopardizing power consumption or cost characteristics.

Designers realize that the increased data rates must be supported by base station and controller backplanes and the interconnections between these systems. Typically, this means the standard backplane either has to speed up or become wider, moving from 16-bit to 32-bit and beyond.

TI's timing and interface components simplify the generation of timing signals that are used to synchronize system activity and meet today's stringent clock-signal timing requirements. A wide selection of high-fan-out drivers, repeaters, and translators provide benefits like low propagation delay, low jitter, and reduced skew, in addition to driving high-performance clocking systems.

TI timing and interface products that support wireless infrastructure applications include:

- Serializer/Deserializer (SerDes) devices ranging from 100 Mbps to 3.125 Gbps, based on LVDS or LVPECL technology
- Repeaters, translators, and multiplexers transmitting at speeds up to 2.0 Gbps with less than 65-ps total jitter
- Single-ended and differential bi-directional transceivers supporting multipoint topologies
- Clock solutions that buffer, synchronize, divide, and multiply with low-phase noise
- PHY and link 1394 (FireWire™) solutions\*
- Low-noise GTLP solutions

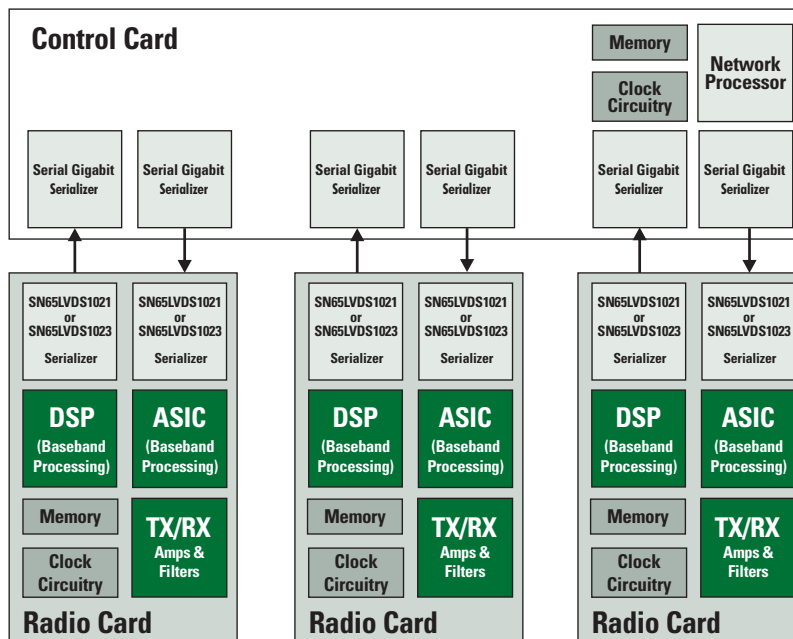
\*See [www.ti.com/connectivity](http://www.ti.com/connectivity) for information

### TO KNOW MORE ►

For detailed information about timing and interface ICs for wireless infrastructure:

Transceivers and receivers	25
Clock drivers	28
GTLP	30
Product selection guides	31

100-MHz to 600-MHz, 10-Bit LVDS Serializer/Deserializer (SerDes) Chipsets







## LVDS SerDes BACKPLANE TRANSMITTER/RECEIVER CHIPSETS

SN65LV1021, SN65LV1023, SN65LV1212, SN65LV1224

Get datasheet and samples at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with *sn65lv1021*, *sv65lv1023*, *sn65lv1212*, or *sn65lv1224*

TI's SN65LV1021/1023 transmitter and SN65LV1212/1224 receiver family of devices is designed to provide BTS backplane solutions between 100 Mbps and 660 Mbps. The chipset has a 10-bit LVTTTL parallel-side input/output and a high-speed LVDS serial-side input/output.

### Key Features:

- 100-Mbps to 400-Mbps serial LVDS data payload bandwidth at 10-MHz to 40-MHz system clock (SN65LV1021/23)
- 300-Mbps to 660-Mbps serial LVDS data payload bandwidth at 30-MHz to 66-MHz system clock (SN65LV1212/24)
- Pin-compatible superset of NSM DS92LV1021/1212, NSM DS92LV1023/1224
- Chipset (serializer/deserializer) power consumption: <250 mW (typ) (Tx) and <400 mW (typ) (Rx)
- Synchronization mode for faster lock

## 16:1 SERIALIZER/DESERIALIZER TRANSCEIVERS WITH PRBS TESTABILITY

TLK1501, TLK2501, TLK2701, TLK2711, TLK3101, TLK4015

Get datasheets, samples, EVMs, and application reports at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

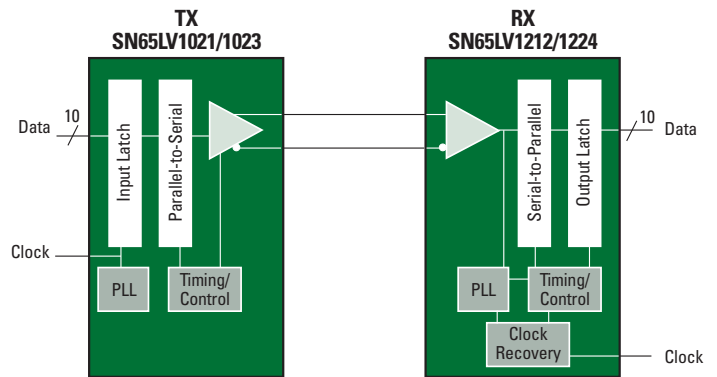
Replace partnumber in URL with *tlk1501*, *tlk2501*, *tlk2701*, *tlk2711*, *tlk3101*, or *tlk4015*

TI's TLK1501, TLK2501, TLK2701, TLK2711, TLK3101, and TLK4015 provide a 16-to-1 serializer/deserializer (SerDes) function with supported data rates from 600 Mbps to 3.125 Gbps. The devices feature built-in 8-B/10-B encoding/decoding for easier design.

### Key Features:

- Hot-plug protection
- 2.5-V power supply for low-power operation
- Programmable voltage output swing on serial output
- Interfaces to backplane, copper cables, or optical converters
- Rated for industrial temperature range
- On-chip 8-bit/10-bit encoding/decoding
- On-chip PLL provides clock synthesis from low-speed reference
- Receiver differential input thresholds 200 mV (min)
- Loss-of-signal (LOS) detection
- Packaging: 64-pin VQFP (PowerPAD™) (TLK1501, TLK2501, TLK2701, TLK3101), 80-pin Microstar Junior™ BGA (GQE) (TLK2711), BGA (TLK4015)

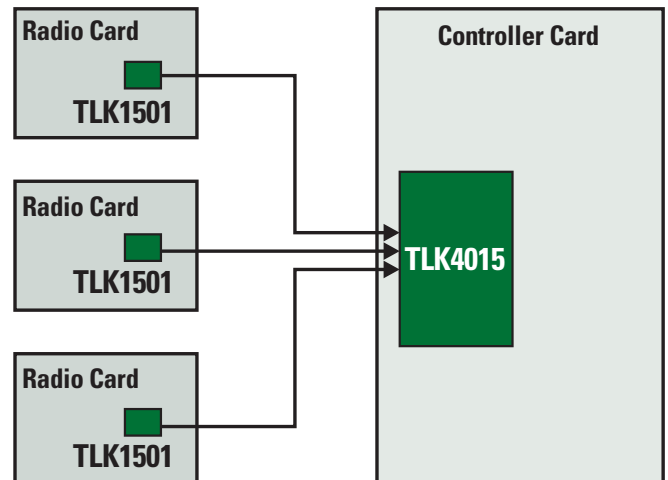
SN65LV1021 Block Diagram



### Applications:

- Radio-to-controller card links
- Antenna-to-receiver link
- BTS backplane

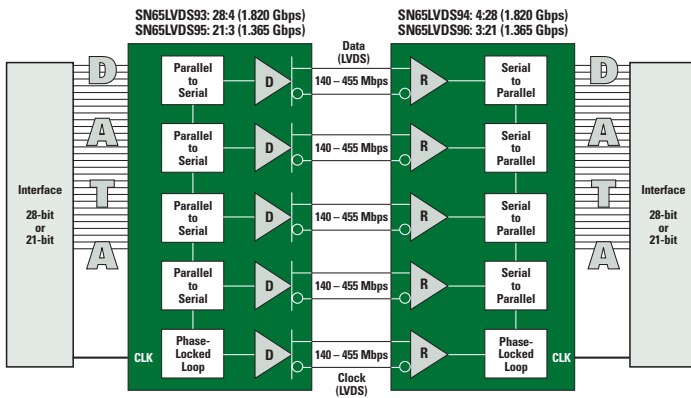
Single-Channel and Multichannel Devices for Radio-to-Controller Card Interfaces



### Applications:

- Radio-to-controller card
- Antenna-to-receiver card
- BTS backplane

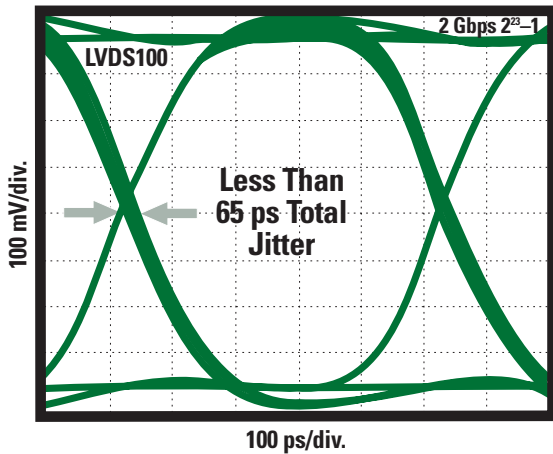
SN65LVDS9x Block Diagram



**Applications:**

- Base station backplane
- Radio-to-controller card links

Eye Pattern of LVDS100



**Applications:**

- CML/LVPECL-to-LVDS translator
- LVDS/CML-to-LVPECL translator
- 2x2 Crosspoint and 2:1 Mux
- 4x4 Crosspoint, 4:1 Mux

### 3- OR 4-CHANNEL, POINT-TO-POINT TRANSMITTER AND RECEIVER PAIR

SN65LVDS96, SN65LVDS95, SN65LVDS93, SN65LVDS94

Get datasheet, samples, EVMs, and application reports at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with *sn65lvds96*, *sn65lvds95*, *sn65lvds93*, or *sn65lvds94*

The SN65LVDS9x family of devices is a 3- or 4-channel (3 or 4 data channels, plus 1 clock channel) point-to-point transmitter and receiver pair which supports up to 1.365/1.820 Gbps of data throughput. It accepts 21/28 LVTTTL inputs and outputs 3 or 4 LVDS lines in parallel with a clock signal.

**Key Features:**

- Operates with a single 3.3-V supply
- 5-V tolerant input
- Rising-clock-edge-triggered outputs
- Wide phase-lock input frequency range
- Low-voltage TTL (LVTTTL) logic output levels
- Pin compatible with NSC:
  - DS90CR213 → SN65LVDS95      DS90CR214 → SN65LVDS96
  - DS90CR285 → SN65LVDS93      DS90CR286 → SN65LVDS94
- Industrial temperature qualified: T<sub>A</sub> = -40°C to 85°C

### LVPECL/CML/LVDS REPEATERS/TRANSLATORS AND CROSSPOINT SWITCHES

SN65LVDS100, SN65LVDS101, SN65CML100

SN65LVDS122, SN65LVDS125, SN65LVCP22, SN65LVCP23

Get samples, datasheets, and EVMs at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in URL with *sn65lvds100*, *sn65lvds101*, *sn65cml100*, *sn65lvds122*, *sn65lvds125*, *sn65lvcp22*, or *sn65lvcp23*

These high-speed repeaters/translators and crosspoint switches feature internal differential signal paths maintain for very low pulse and channel-to-channel skews.

**Key Features:**

- Total jitter < 65 ps
- Pulse skew < 50 ps
- All devices accept LVDS, CML, and LVPECL inputs
- 1:1 Translator repeaters
  - LVDS100 with LVDS output
  - LVDS101 with LVPECL output
  - CML100 with CML output
- Crosspoints
  - LVDS122 2x2 – LVDS output
  - LVDS125 4x4 – LVDS output
  - LVCP22 2x2 – LVDS output
  - LVCP23 2x2 – LVPECL output

## MULTIPOINT-LVDS FOR BACKPLANES AND CABLES

SN65MLVD080, SN65MLVD082, SN65MLVD200, SN65MLVD201, SN65MLVD202, SN65MLVD203, SN65MLVD204, SN65MLVD205, SN65MLVD206, SN65MLVD207

Get samples, datasheets, application notes, and EVMs at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)  
 Replace partnumber in the URL with *sn65mlvd080*, *sn65mlvd082*, *sn65mlvd200*, *sn65mlvd201*, *sn65mlvd202*, *sn65mlvd203*, *sn65mlvd204*, *sn65mlvd205*, *sn65mlvd206*, or *sn65mlvd207*

TI introduces the industry's first family of transceivers compliant with the Multipoint Low-Voltage Differential Signaling (M-LVDS) specification TIA/EIA-899. The SN65MLVD20x parts are half- and full-duplex single-channel transceivers. The SN65MLVD08x devices are 8-channel half-duplex transceivers that can operate at 125 MHz with up to 32 devices.

### Key Features:

- Half power, 10x speed of RS-485
- Complies with M-LVDS Standard (TIA/EIA-899) – also supported by alternative vendors
- Supports wired-OR configuration – ideal for control lines
- Hot-plugging capability enhances reliability and robustness
- Controlled rise times for longer stub lengths

## LOW-VOLTAGE CLOCK DRIVERS FOR CLOCK-DISTRIBUTION APPLICATIONS

CDCLVP110/CDCLVD110

Get datasheets and application reports at: [www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)  
 Replace partnumber in the URL with *cdclvp110* or *cdclvd110*

TI's CDCLVP110 and CDCLVD110 low-voltage clock drivers support low-skew, low-jitter differential LVDS/LVPECL or HSTL (selectable) inputs (CLK0, CLK1) to 10 pairs of differential LVPECL clock outputs with minimum skew.

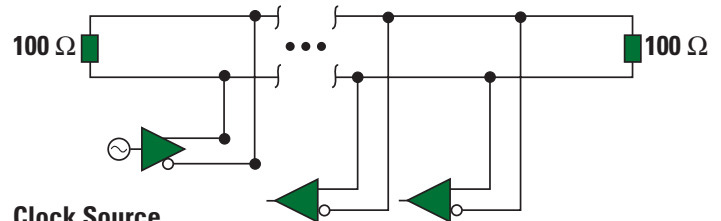
### Key Features:

- 2.5-V or 3.3-V support
- Selectable clock input through CLK\_SEL
- Low-output skew (15 ps) max
- Cycle-to-cycle jitter less than 1 ps (rms)
- Packaging: 32-pin TQFP

### CDCLVD110

- Accepts LVDS, LVTTIL, HSTL, CML, or LVPECL signaling levels
- Signaling-rate capability up to 1.1 GHz
- Full rail-to-rail common-mode range
- Low output skew (30 ps)
- Packaging: 32-pin LQFP (VF)

M-LVDS for Clock Distribution Over a Backplane

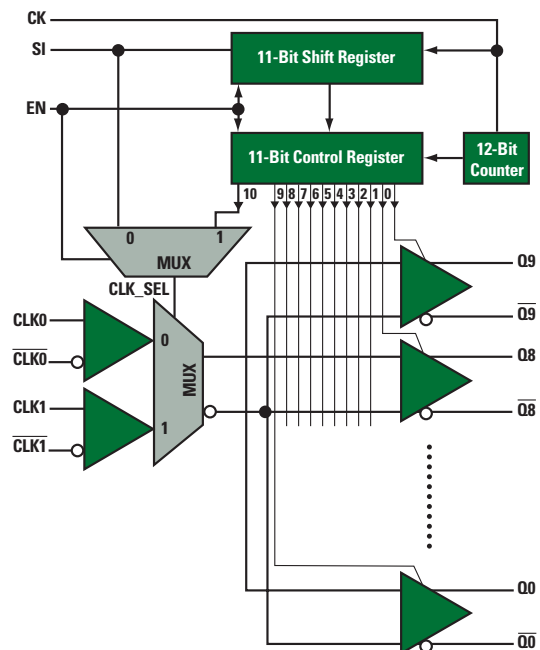


**Clock Source**  
 e.g., 8 kHz, 19 MHz ... X < 100 MHz

### Applications:

- Clock distribution
- Base station control and data bus
- Synchronization signals
- PICMG 3.0 ATCA telephony clock interface

CDCLVxx Block Diagram



### Applications:

- Base stations, BB card, LTU
- Cable modem headend

General Overview

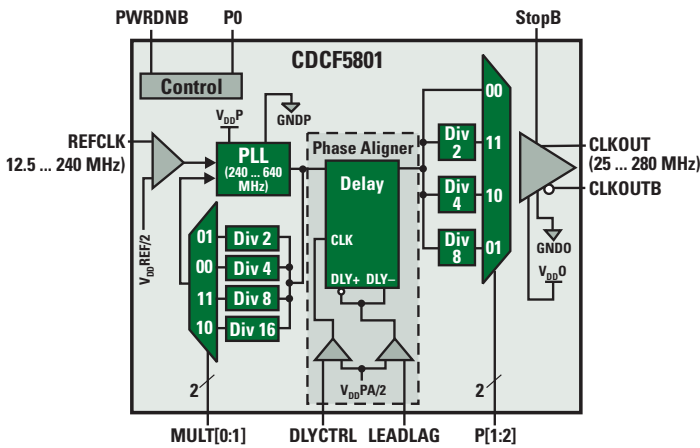
Signal Chain

Timing & Interface

Logic

Power Management

CDCF5801 Functional Diagram



**Applications:**

- Phase adjustment
- Low-jitter multiplier

## LOW-JITTER CLOCK MULTIPLIER WITH PROGRAMMABLE DELAY AND PHASE ALIGNMENT

### CDCF5801

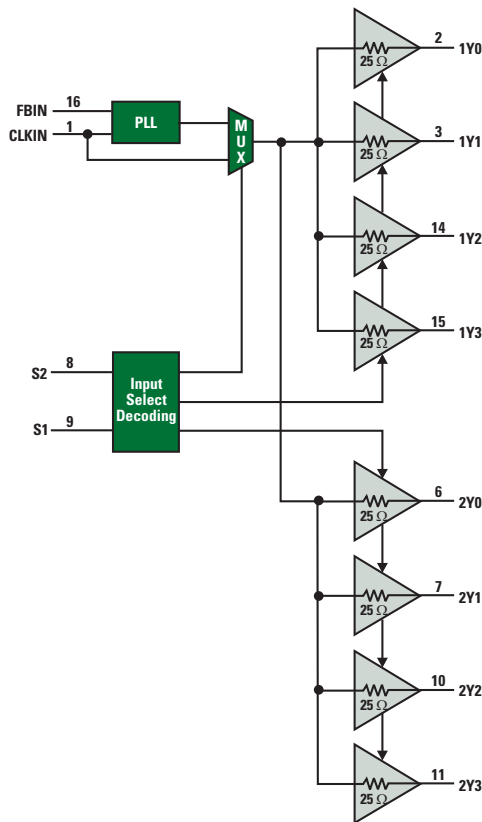
Get application notes and datasheets at: [www.ti.com/sc/device/cdcf5801](http://www.ti.com/sc/device/cdcf5801)

The CDCF5801 provides clock multiplication from a reference clock (REFCLK) signal. It also allows delay or advance of the CLKOUT/CLKOUTB with steps of 2.6 mUI through a unique aligner.

**Key Features:**

- Low-jitter clock multiplier x1, x2, x4 or x8
  - Input frequency: 12.5 to 240 MHz
  - Output frequency: 25 to 280 MHz
- Low-jitter clock divider /2, /4 or /8
  - Input frequency: 12.5 to 240 MHz
  - Output frequency: 25 to 280 MHz
- 2.6-mUI programmable bidirectional delay steps
- One single-ended input and one differential output pair
- Output can drive LVPECL, LVDS and LVTTTL
- Spread spectrum clock tracking ability to reduce EMI
- Industrial temperature range: -40°C to 85°C

CDCVF25084 Block Diagram



## 3.3-V X4 CLOCK MULTIPLIER WITH 8 OUTPUTS

### CDCVF25084

Get application notes and datasheets at: [www.ti.com/sc/device/cdcvf25084](http://www.ti.com/sc/device/cdcvf25084)

The CDCVF25084 is a high-performance, low-skew, low-jitter, phase-locked loop clock multiplier. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal including a multiplication factor of four. The CDCVF25084 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

**Key Features:**

- Phase-locked loop-based zero-delay buffer
- Operating frequency range: 10 MHz to 200 MHz
- Low jitter (cycle-cycle)
- Distributes one clock input to two banks of four outputs
- Auto frequency detection to disable device (power-down mode)
- Consumes less than 20 μA in power-down mode
- Packaging: 16-pin TSSOP

**Applications:**

- Telecom
- Datacom

## GUNNING TRANSCEIVER LOGIC PLUS

### GTLP Family

Get samples, datasheets, and application reports at:  
[www.ti.com/sc/gtlp](http://www.ti.com/sc/gtlp)

TI provides backplane interface solutions for telecom/datacomm end equipment with the open-drain GTLP technology, which provides better signal integrity and overall system improvement over traditional logic, allowing you to drive heavily loaded backplanes.

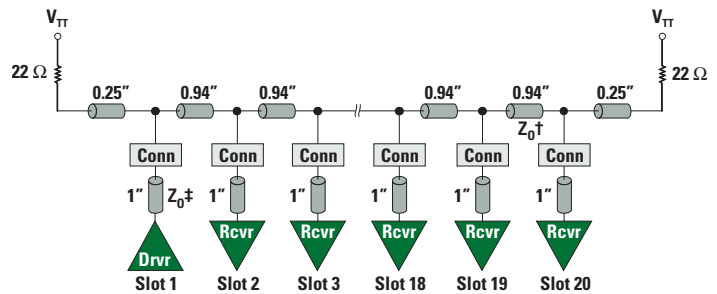
#### Key Features:

- GTLP low-output-voltage swing reduces EMI
- Reduced-input GTLP threshold provides adequate noise margin
- TI-OPC and OEC circuitry provide improved signal integrity
- $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$  support live insertion
- Bi-directional interface between GTLP and LVTTTL signal levels
- 5-V tolerant LVTTTL I/Os allow mixed-voltage systems
- Up to 100-mA drive capability to drive heavily loaded backplanes
- Packaging: Space-saving TSSOP (DGG), TVSOP (DGV), and LFBGA (GKE/GKF) packages

#### Applications:

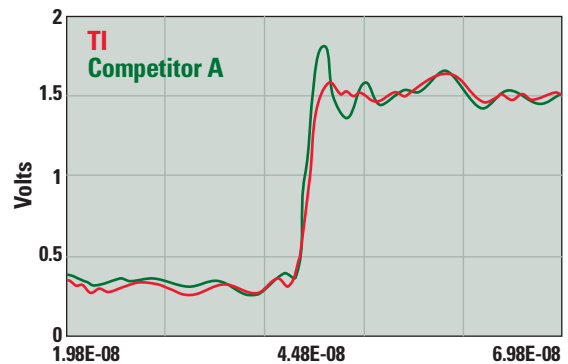
- Base stations
- Networking

Single-Bit Representation of a Multipoint Parallel Backplane



† Unloaded backplane trace natural impedance ( $Z_0$ ) is 45  $\Omega$ . 45 to 60  $\Omega$  is allowed with 50  $\Omega$  being ideal.  
 ‡ Card stub natural impedance ( $Z_0$ ) is 60  $\Omega$ .

Signal Integrity: TI vs. Competition



## SERIAL GIGABIT SOLUTIONS

Device	Function	Data Rate	Serial I/F	Parallel I/F	Power	Special Features	Price <sup>1</sup>
TLK1501	Single-ch. 16:1 SerDes	0.6–1.5 Gbps	1 CML ch.	16 LVTTTL lines	200 mW	Built-in testability	Web
TLK2501	Single-ch. 16:1 SerDes	1.6–2.5 Gbps	1 CML ch.	16 LVTTTL lines	300 mW	Built-in testability	Web
TLK2701	Single-ch. 16:1 SerDes	1.6–2.5 Gbps	1 CML ch.	16 LVTTTL lines	300 mW	Built-in testability and K character control	Web
TLK2711	Single-ch. 16:1 SerDes	1.6–2.5 Gbps	VML	16 LVTTTL lines	350 mW	MicroStar Jr.™ BGA packaging	Web
TLK3101	Single-ch. 16:1 SerDes	2.5–3.125 Gbps	1 VML ch.	16 LVTTTL lines	350 mW	Built-in testability	Web
TLK1201	Single-ch. 10:1 gigabit Ethernet xcvr	0.6–1.3 Gbps	1 LVPECL ch.	10 LVTTTL lines	200 mW	Industrial temperature	Web
TLK2201	Single-ch.	1.0–1.6 Gbps	1 LVPECL ch.	10 LVTTTL lines	200 mW	JTAG; 5-bit DDR mode	Web
TLK22011	Single-ch. 10:1 gigabit Ethernet xcvr	1.2–1.6 Gbps	1 LVPECL ch.	10 LVTTTL lines	200 mW	JTAG; 5-bit DDR mode, industrial temp. qualified	Web
TLK2201JR	Single-ch. 10:1 gigabit Ethernet xcvr	1.0–1.6 Gbps	1 LVPECL ch.	10 LVTTTL lines	200 mW	MicroStar Jr. 5 × 5 Land Grid Array (LGA)	Web
TLK2208	Eight-ch. of 10:1 or 8:1 gigabit Ethernet xcvr	1.0–1.3 Gbps	8 CML ch.	4/5-bit/ch (nibble DDR mode), 8/10- bit/ch (multiplex ch. mode)	1 W	JTAG, MDIO supported	Web
TLK4015	Four ch. of 16:1 xcvr	0.8–1.56 Gbps	4 CML ch.	16 LVTTTL/ channel	1 W	Four-channel version of TLK1501	Web
SN65LVDS93/94	Four-ch. 28:4 TX/RX chipset	140–455 Mbps/ch.	4 LVDS	28 × LVTTTL	250 mW/ chip	Supports up to 1.82-Gbps throughput	Web
SN65LVDS95/96	Four-ch. 21:3 TX/RX chipset	140–455 Mbps/ch.	4 LVDS	28 × LVTTTL	250 mW/ chip	Supports up to 1.3-Gbps throughput	Web
SN65LV1021/ SN65LV1212	Single-ch. 10:1 TX/RX chipset	100–400 Mbps	1 LVDS	10 × LVTTTL	<400 mW/ total	Low-power solution	Web
SN65LV1023/ SN65LV1224	Single-ch. 10:1 TX/RX chipset	300–660 Mbps	1 LVDS	10 × LVTTTL	<400 mW/ total	Low-power solution	Web
SLK2501/ SLK2511	Single-ch. 4:1 multirate SONET xcvr with CDR	OC-3/12/24/48	1 LVPECL	4 × 622 LVDS	900 mW	Auto-rate detection, local and remote loop back	Web
SLK2701/ SLK2721	Single-ch. 4:1 multirate SONET xcvr with CDR	OC-3/12/24/48	PECL	4 × LVDS	900 mW	FEC rate is compatible, SLK2721 is optimized for jitter tolerance	Web

<sup>1</sup>Please check [www.ti.com](http://www.ti.com) for current pricing on these products.

## LVDS LINE DRIVERS AND RECEIVERS

Device	Max Drvr/Rcvr $t_{pd}$ (ns)	Max Speed (Mbps)	Max Supply Current (mA)	HBM ESD Protection (kV)	# Inputs	# Outputs	Output Skew (ps) <sup>2</sup>	Pulse Skew (ps) <sup>2</sup>	Package Options	Comments	Price <sup>1</sup>
SN65LVDS1	3.1	630	8	15	1 LVTTTL	1 LVDS	–	300 typ	5-pin SOT-23, 8-pin SOIC	Single driver	0.66
SN65LVDS2	3.6	400	7	15	1 LVDS	1 LVTTTL	–	600 max	5-pin SOT-23, 8-pin SOIC	Single receiver	0.66
SN65LVDS22	6	400	20	12	2 LVDS	2 LVDS	–	200 typ	16-pin SOIC 16-pin TSSOP	2:2 MUX (crosspoint)	3.01
SN65LVDS31	2.5	400	35	8	4 LVTTTL	4 LVDS	300 max	300 max	16-pin SOIC 16-pin TSSOP	Quad driver	1.85
SN65LVDS32 <sup>3</sup>	3	400	18	8	4 LVDS	4 LVTTTL	300 max	400 max	16-pin SOIC 16-pin TSSOP	Quad receiver	1.85
SN65LVDS33 <sup>3</sup>	6	400	23	15	4 LVDS	4 LVTTTL	150 typ	200 typ	16-pin SOIC, 16-pin TSSOP	Quad receiver	2.22
SN65LVDS047	2.8	400	26	8	4 LVTTTL	4 LVDS	300 max	300 max	16-pin SOIC, 16-pin TSSOP	Quad driver	1.83
SN65LVDS048A	3.7	400	15	10	4 LVDS	4 LVTTTL	500 max	450 max	16-pin SOIC, 16-pin TSSOP	Quad receiver	1.83
SN65LVDS386 <sup>3</sup>	4	300	70	4	16 LVDS	16 LVTTTL	400 max	600 max	64-pin TSSOP	16-ch. receiver	5.55
SN65LVDS387	2.9	630	95	15	16 LVTTTL	16 LVDS	150 max	500 max	64-pin TSSOP	16-ch. receiver	5.55
SN75LVDS388A <sup>3</sup>	4	300	40	4	8 LVDS	8 LVTTTL	400 max	600 max	38-pin TSSOP	Octal receiver	3.25
SN65LVDS389	2.9	300	70	4	8 LVTTTL	8 LVDS	150 max	500 max	38-pin TSSOP	Octal driver	3.25

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

<sup>2</sup> $R_L = 100 \Omega$ ,  $C_L = 10 \text{ pF}$  with max. spec.

<sup>3</sup>Integrated termination option.

## LVDS/LVPECL/CML REPEATERS/TRANSLATORS AND CROSSPOINTS

Device	Max Drvr/Rcvr $t_{pd}$ (ns)	Max Speed (Mbps)	Max Supply Current (mA)	HBM ESD Protection (kV)	# Inputs	# Outputs	Output Skew (ps)	Pulse Skew (ps)	Packaging	Comments	Price <sup>1</sup>
SN65LVDS100	0.9	2000	90	5	1 LVDS/CML/LVPECL	1 LVDS	–	50	8-pin SOIC, VSSOP	Translator/Repeater	2.52
SN65LVDS101	0.9	2000	90	5	1 LVDS/CML/LVPECL	1 LVPECL	–	50	8-pin SOIC, VSSOP	Translator/Repeater	2.52
SN65CML100	0.8	1500	30	5	1 LVDS/CML/LVPECL	1 CML	–	50	8-pin SOIC, VSSOP	Translator/Repeater	2.52
SN65LVDS122	0.9	1500	100	4	2 LVDS/CML/LVPECL	2 LVDS	40	50	16-pin SOIC, TSSOP	2x2 Crosspoint	4.75
SN65LVCP22	0.8	1000	85	8	2 LVDS/CML/LVPECL	2 LVDS	20	20	16-pin SOIC, TSSOP	2x2 Crosspoint	3.89
SN65LVCP23	1	2000	65	5	2 LVDS/CML/LVPECL	2 LVPECL	20	20	16-pin SOIC, TSSOP	2x2 Crosspoint	4.95
SN65LVDS125	1	1500	100	8	4 LVDS/CML/LVPECL	4 LVDS	50	50	38-pin TSSOP	4x4 Crosspoint	8.70

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.



## GTLT TRANSCIVERS

Device	Description	Status	Price <sup>1</sup>
SN74GTL1394	2-bit LVTTTL-to-GTLP adjustable-edge-rate bus Xcvt w/ split LVTTTL port, feedback path, and selectable polarity	Active	2.73
SN74GTL1395	Two 1-bit LVTTTL/GTLP adjustable-edge-rate bus Xcvrs w/ split LVTTTL port, feedback path, and selectable polarity	Active	1.75
SN74GTL2033	8-bit LVTTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTTL port and feedback path	Active	3.85
SN74GTL2034	8-bit LVTTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTTL port and feedback path	Active	3.85
SN74GTL21395	Two 1-bit LVTTTL/GTLP adjustable-edge-rate bus Xcvrs with split LVTTTL port, feedback path, and selectable polarity	Active	1.75
SN74GTL22033	8-bit LVTTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTTL port and feedback path	Active	3.85
SN74GTL22034	8-bit LVTTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTTL port and feedback path	Active	3.85
SN74GTL817	GTLP-to-LVTTTL 1-to-6 fanout driver	Active	2.45
SN74GTLPH1612	18-bit LVTTTL-to-GTLP adjustable-edge-rate universal bus transceiver	Active	5.95
SN74GTLPH1616	17-bit LVTTTL-to-GTLP adjustable-edge-rate universal bus transceiver with buffered clock outputs	Active	5.95
SN74GTLPH1645	16-bit LVTTTL-to-GTLP adjustable-edge-rate bus transceiver	Active	2.45
SN74GTLPH1655	16-bit LVTTTL-to-GTLP adjustable-edge-rate universal bus transceiver	Active	5.95
SN74GTLPH16612	18-bit LVTTTL-to-GTLP universal bus transceiver	Active	4.62
SN74GTLPH16912	18-bit LVTTTL-to-GTLP universal bus transceiver	Active	4.90
SN74GTLPH16916	17-bit LVTTTL-to-GTLP universal bus transceiver with buffered clock outputs	Active	4.90
SN74GTLPH16945	16-bit LVTTTL-to-GTLP bus transceiver	Active	2.10
SN74GTLPH306	8-bit LVTTTL-to-GTLP bus transceiver	Active	3.08
SN74GTLPH3245	32-bit LVTTTL-to-GTLP adjustable-edge-rate bus transceiver	Active	3.71
SN74GTLPH32912	36-bit LVTTTL-to-GTLP universal bus transceiver	Preview	Call
SN74GTLPH32916	34-bit LVTTTL-to-GTLP universal bus transceiver with buffered clock outputs	Active	7.00
SN74GTLPH32945	32-bit LVTTTL-to-GTLP bus transceiver	Active	3.15

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## M-LVDS TRANSCIVERS

Device Name	Description	No. of Tx	No. of Rx	Input Signal	Output Signal	RX Type 1 or 2	Part-to-Part Skew Max (ps)	Signal-ing Rate (Mbps)	Tx t <sub>pd</sub> Typ (ns)	Rx t <sub>pd</sub> Typ (ns)	I <sub>cc</sub> Max (mA)	ESD HBM (kV)	Supply Voltage (V)	Pin/Package	Price <sup>1</sup>
SN65MLVD200	Half-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	2500	100	2.3	4.6	26	3	3.3	8-pin SOP	1.84
SN65MLVD201	Half-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	1000	200	1.5	4.0	24	3	3.3	8-pin SOP	2.10
SN65MLVD202	Full-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	2500	100	2.3	4.6	26	3	3.3	14-pin SOP	1.84
SN65MLVD203	Full-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	1000	200	1.5	4.0	24	3	3.3	14-pin SOP	2.10
SN65MLVD204	Half-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	2500	100	2.3	4.6	26	3	3.3	8-pin SOP	1.84
SN65MLVD205	Full-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	2500	100	2.3	4.6	26	3	3.3	14-pin SOP	1.84
SN65MLVD206	Half-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	2	1000	200	1.5	4.0	24	3	3.3	8-pin SOP	2.10
SN65MLVD207	Full-duplex M-LVDS xcvt	1	1	LVTTTL, M-LVDS	LVTTTL, M-LVDS	2	1000	200	1.5	4.0	24	3	3.3	14-pin SOP	2.10
SN65MLVD080	Half-duplex M-LVDS xcvt	8	8	LVTTTL, M-LVDS	LVTTTL, M-LVDS	1	600	250	1.5	4	180	8	3.3	64-pin TSSOP	4.50
SN65MLVD082	Half-duplex M-LVDS xcvt	8	8	LVTTTL, M-LVDS	LVTTTL, M-LVDS	2	600	250	1.5	4	180	8	3.3	64-pin TSSOP	4.50

<sup>1</sup>Suggested resale unit price in U.S. dollars in quantities of 1,000. Please check [www.ti.com](http://www.ti.com) for current pricing on these products.

## CLOCK DISTRIBUTION CIRCUITS

Device	Description	Package Options	I/O Levels (Input/Output)	Frequency (MHz)	V <sub>CC</sub> (V)	Output Skew t <sub>sk(o)</sub> max (ns)	Price <sup>1</sup>
<b>Buffer-Based Clock Distribution</b>							
CDCVF111	1:9 diff LVPECL	28-pin PLCC	LVPECL/LVPECL	0–650	3.3	0.05	Web
CDC318A	1:18 clock driver with I <sup>2</sup> C control interface	48-pin SSOP	LVTTTL/LVTTTL, TTL	0–100	3.3	0.25	Web
CDC341	1:8 w/ fast t <sub>pd</sub> fanout	20-pin SOIC	TTL/TTL	0–80	5	0.6	Web
CDC351/2351	1:10 w/ fast t <sub>pd</sub> fanout, 3-state outputs	24-pin SOIC/SSOP	LVTTTL/LVTTTL	0–100	3.3	0.5	Web
CDC391	1:6 clock driver with selectable polarity and 3-state outputs	16-pin SOIC	TTL/TTL	0–100	5	0.5	Web
CDCLVD110	1:10 programmable low-voltage LVDS clock driver	32/TQFP	LVDS/LVDS	900	2.5	30 ps typ	
CDCLVP110	1:10 low-voltage LVPECL HSTL with selectable input clock driver	32/LQFP	LVPECL or HSTL/LVPECL	3.5 GHz	2.5/3.3	30 ps	
CDCV304	1:4 fanout for PCI-X and general apps.	8-pin TSSOP	LVTTTL/CMOS	0–140	3.3	0.17	Web
CDCVF2310	1:10 clock driver w/ 2 banks for general-purpose applications	24-pin TSSOP	LVTTTL/LVTTTL	0–170 (V <sub>DD</sub> =2.3–2.7 V) 0–200 (V <sub>DD</sub> =3–3.6 V)	2.5/3.3	170 ps @ 2.5 V 100 ps @ 3.3 V	Web
<b>CDCM1804</b>	<b>1:3 LVPECL clock buffer and addl. LVCMOS output and programmable divider</b>	<b>24/MLF</b>	<b>LVPECL/LVPECL or LVCMOS</b>	<b>to 800 MHz for LVPECL to 200 MHz for LVCMOS</b>	<b>3.3</b>	<b>–</b>	<b>Web</b>
SN65LVDS104	1:4 diff LVDS	16-pin SOIC/TSSOP	LVDS/LVDS	0–315	3.3	0.1	2.22
SN65LVDS105	1:5 diff LVDS	16-pin SOIC/TSSOP	LVDS/LVDS	0–315	3.3	0.1	2.22
SN65LVDS108	1:8 diff LVDS	38-pin TSSOP	LVDS/LVDS	0–311	3.3	0.3	4.55
SN65LVDS116	1:16 diff LVDS	64-pin TSSOP	LVDS/LVDS	0–311	3.3	0.3	5.97
<b>PLL-Based Clock Distribution</b>							
CDC516/2516 <sup>2</sup>	1:16 PLL clock driver	48-pin TSSOP	LVTTTL/LVTTTL	25–125	3.3	0.2	Web
CDC536/2536 <sup>2</sup>	1:6 PLL clock driver w/ (3) at 1/2× or 2× output, 3-state outputs	28-pin SSOP	LVTTTL/LVTTTL	25–100	3.3	0.5	Web
CDC582/2582 <sup>2</sup>	1:12 LV diff PECL PLL clock driver w/ (9) at 1/2× or 2× output	52-pin TQFP	LVPECL/LVTTTL	25–100	3.3	0.5	Web
CDC586/2586 <sup>2</sup>	1:12 PLL clock driver w/ (9) at 1/2× or 2× output, 3-state outputs	52-pin TQFP	LVTTTL/LVTTTL	25–100	3.3	0.5	Web
CDC5801	Clock multiplier/divider w/ programmable delay and phase alignment	24/SSOP	LVTTTL/LVPECL or LVDS or LVTTTL	150–500 / 12.5–62.5	3.3		
CDC7005	High-performance clock synthesizer	64/BGA	LVTTTL/LVPECL	10–650	3.3	200 ps	
<b>CDCF5801</b>	<b>Multiplier/divider with programmable delay and phase alignment</b>	<b>24/SSOP</b>	<b>LVCMOS/LVPECL or LVDS or LVTTTL</b>	<b>12.5 to 240 25 to 280</b>	<b>3.3</b>	<b>–</b>	<b>Web</b>
CDCVF2505	1:5 PLL clock driver for general purpose, SSC	8-pin TSSOP/SOIC	LVTTTL/LVTTTL	24–200	3.3	0.15	Web
CDCVF2508	1:8 low-power PLL clock driver with two banks, SSC	16-pin TSSOP/SOIC	LVTTTL/LVTTTL	10–170	2.5/3.3	0.15	Web
<b>CDCVF25084</b>	<b>1:8 low-power 4<sup>1</sup> multiplier with two banks, SSC</b>	<b>16-pin TSSOP</b>	<b>LVTTTL/LVTTTL</b>	<b>10 to 180</b>	<b>3.3</b>	<b>150</b>	<b>Web</b>
CDCVF2509	1:9 low-power PLL clock driver for PC 133 and beyond application, SSC	24-pin TSSOP	LVTTTL/LVTTTL	50–175	3.3	0.1	Web
CDCVF2510	1:10 low-power PLL clock driver for PC 133 and beyond application, SSC	24-pin TSSOP	LVTTTL/LVTTTL	50–175	3.3	0.1	Web
<b>PLL-Based Clocks for Memory Applications</b>							
CDCV850	1:10 PLL clock driver for DDR SDRAM application, SSC compatible with two-line serial interface	48-pin TSSOP	HCSSL, Universal (except ECL)/SSTL-II	60–140	2.5/3.3	0.075	Web
CDCV855	1:4 (plus feedback pair) PLL differential clock driver for DDR applications, SSC	28-pin TSSOP	SSTL-II/ SSTL-II, LVTTTL	60–180	2.5	0.075	Web
CDCV857B	1:10 PLL differential clock driver for DDR applications, SSC	48-pin TSSOP	SSTL-II/SSTL-II	60–200	2.5	0.075	Web

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000. Please check [www.ti.com](http://www.ti.com) for current pricing on these products.

<sup>2</sup>With series output resistors.

Notes: For more information regarding test conditions used to obtain measurements, see datasheet.

Converted from V/ns datasheet value to ns value, based on 0.4- to 2-V voltage rise/fall.

Preview devices are listed in blue.

## LOGIC

As wireless infrastructure designers look to increase data throughput, reduce power consumption, and shrink form factors, TI's logic portfolio is constantly advancing while, at the same time, the company is dedicated to providing legacy logic devices.

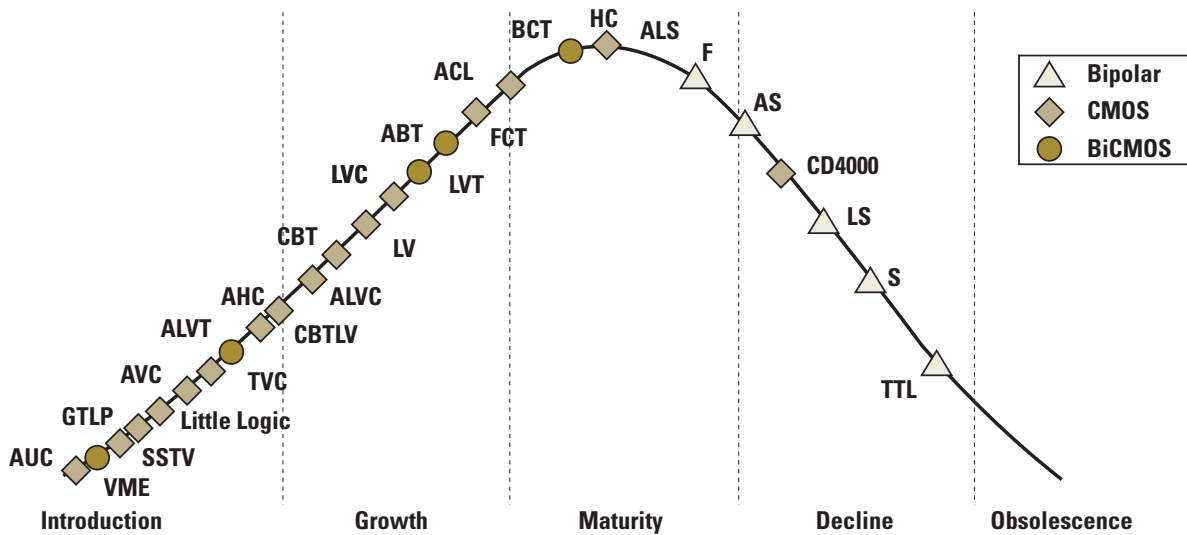
As the leading provider of logic, TI's latest technologies are targeted for the fast moving market of wireless infrastructure systems. Advanced CMOS families and functions, like the LVC and ALVC are optimized at 3.3-V  $V_{CC}$ . And the CBT and CBTLV families of bus switches offer designers a broad portfolio to meet diverse switching needs.

### TO KNOW MORE ▶

For detailed information about logic for wireless infrastructure:

Buffer/driver	36
Bus switch	36
Product selection guides	37

Logic Product Life Cycle



## 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SN74ALVC16244A/SN74LVC16244A

Get samples and datasheets at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in the URL with *sn74alvc16244a* or *sn74lvc16244a*

Ideal for base station and networking applications, both the LVC and ALVC families of logic technologies offer solutions for speed-critical 3.3-V system designs. The LVC family is a high-performance version with 0.8- $\mu$  CMOS process technology. With typical propagation delays of less than 2 ns, ALVC provides 24 mA of current drive and static power consumption.

### Key Features:

- 3.6-ns max  $t_{pd}$  at 3.3 V (ALVC)
- 5.2-ns max  $t_{pd}$  at 3.3 V (LVC)
- $I_{off}$  circuitry (LVC)
- Packaging: BGA

### ALVC PARAMETRICS

Parameter Name	SN74ALVC16244A
Voltage nodes (V)	3.3, 2.7, 2.5, 1.8
$V_{CC}$ range (V)	2.3 to 3.6
Input level	LVTTL
Output level	LVTTL
Output drive (mA)	-24/24
$t_{pd}$ max (ns)	3.6
Static current	0.04

## LOW-VOLTAGE QUADRUPLE-FET BUS SWITCH

SN74CBTLV3125

Get samples and datasheets at:

[www.ti.com/sc/device/sn74cbtlv3125](http://www.ti.com/sc/device/sn74cbtlv3125)

The CBTLV family of bus switches operate at the low-voltage 3.3-V operating node. These high-speed bus-connect devices benefit designs with greater system speed and reduced power consumption. The SN74CBTLV3125 quadruple-FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is high.

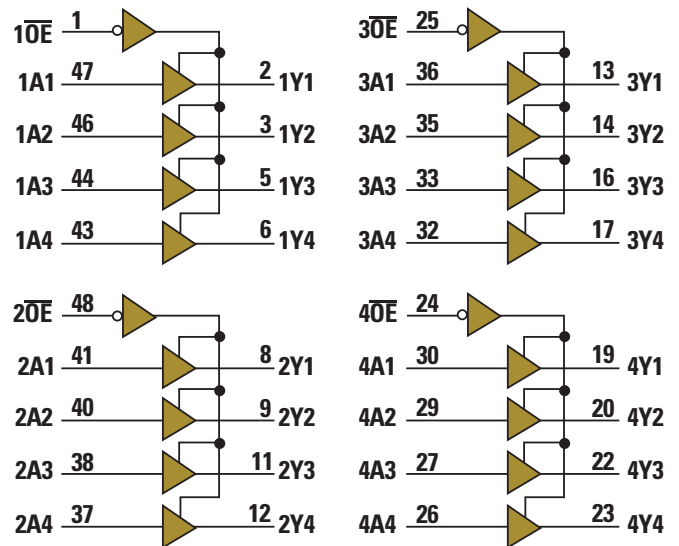
### Key Features:

- Standard SN74CBTLV3125-type pinout
- 5- $\Omega$  switch connection between two ports
- Isolation under power-off conditions
- Latch-up performance exceeds 100 mA per JESD 78, Class II

### Applications:

- Base stations
- Networking

SN75ALVC16244A Logic Diagram (Positive Logic)

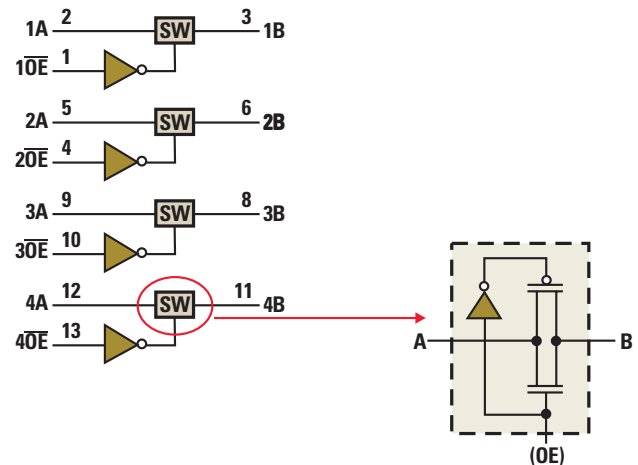


Pin numbers shown are for the DGG and DL packages.

### Applications:

- Base stations
- Networking

SN74CBTLV3125 Block Diagram



### CBTLV3125 PARAMETERS

Parameter Name	SN74CBTLV3125
Voltage nodes (V)	3.3, 2.5
$V_{CC}$ range (V)	2.3 to 3.6
No. of bits	4
$r_{on}$ max (ohms)	7
$t_{pd}$ max (ns)	0.25

General Overview

Signal Chain

Timing & Interface

Logic

Power Management

## SN74CBTLV31x BUS SWITCHES

Orderable Device	Package	Pins	Temp (°C)	Status	Pack Quantity	Price <sup>1</sup>
SN74CBTLV3125D	D	14	-40 to 85	Active	50	0.81
SN74CBTLV3125DBQR	DBQ	16	-40 to 85	Active	2500	0.81
SN74CBTLV3125DGVR	DGV	14	-40 to 85	Active	2000	0.81
SN74CBTLV3125DR	D	14	-40 to 85	Active	2500	0.81
SN74CBTLV3125NSR	NS	14	-40 to 85	Active	2000	0.88
SN74CBTLV3125PWR	PW	14	-40 to 85	Active	2000	0.81

<sup>1</sup>Suggested resale price in U.S. dollars.

## ALVC BUFFER/DRIVERS

Orderable Device	Package	Pins	Temp (°C)	Status	Pack Quantity	Price <sup>1</sup>
SN74ALVC16244ADGGR	DGG	48	-40 to 85	Active	2000	1.12
SN74ALVC16244ADL	DL	48	-40 to 85	Active	25	1.12
SN74ALVC16244ADLR	DL	48	-40 to 85	Active	1000	1.12
SN74ALVC16244AGQLR	GQL	56	-40 to 85	Active	1000	1.23

<sup>1</sup>Suggested resale price in U.S. dollars.

## LVC PRODUCTS

Orderable Device	Package	Pins	Temp (°C)	Status	Pack Quantity	Price <sup>1</sup>
SN74LVC16244ADGGR	DGG	48	-40 to 85	Active	2000	1.01
SN74LVC16244ADGVR	DGV	48	-40 to 85	Active	2000	1.01
SN74LVC16244ADL	DL	48	-40 to 85	Active	25	1.01
SN74LVC16244ADLR	DL	48	-40 to 85	Active	1000	1.01
SN74LVC16244AGQLR	GQL	56	-40 to 85	Active	1000	1.12

<sup>1</sup>Suggested resale price in U.S. dollars.

## POWER MANAGEMENT PRODUCTS

For detailed information, visit:  
power.ti.com

Wireless infrastructure (WI) systems require that designers consider a wide range of power management technology. From discrete devices to modular approaches, WI designers must select technology that addresses the technical challenge of the system and offers ancillary benefits in terms of ease-of-use and supply chain reliability and efficiency.

Much of TI's broad range of power management products has been targeted at wireless infrastructure applications. Based on extensive experience with power technology, TI's solutions address application challenges that designers face daily. With solutions for both portable and board power applications, TI has a comprehensive array of power management solutions. In addition, its market-proven record of expertise has made TI's power technology very easy to use for designers. A wide range of both discrete devices and isolated and non-isolated modular power technology is available.

Some of the products specific to wireless infrastructure applications include the following:

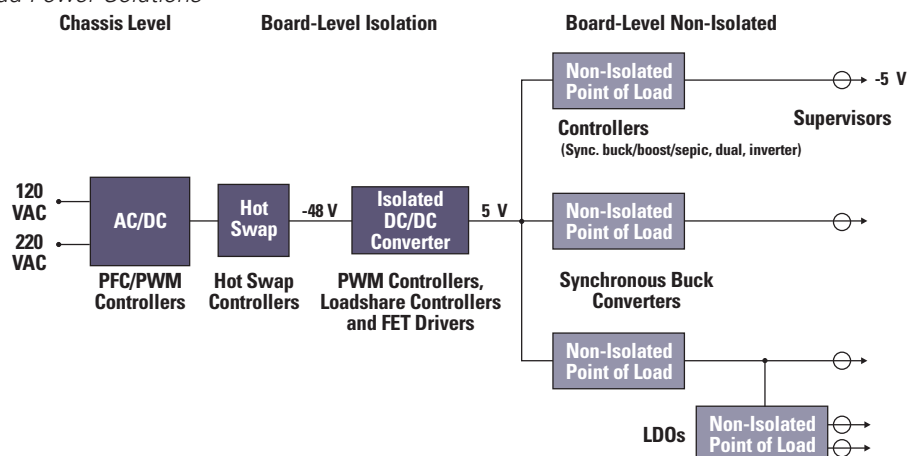
- **DC/DC Controllers and Converters:** These devices will generate regulated supply rails. The TPS54xxx (SWIFT™) family of converters integrates the output FETs to simplify design and the family provides output currents up to 9 A. New controllers, such as the TPS40K™ series, are ideal for a broader range of input voltages and output currents.
- **Isolated Plug-In Modules:** A number of products are specifically designed for 48-V bus applications. Many devices feature multiple channels for improved integration and lower system cost.
- **Non-Isolated Plug-In Modules:** Modules specifically designed for point-of-load applications come in high-performance packaging. A broad range of voltage and current options make these devices ideal for wireless infrastructure systems.
- **Hot Swap Power Managers:** New TPS2490, TPS2491 and TPS2350 hot swap devices are specifically designed for the 48-V bus used in infrastructure systems. These new devices add to the family of TPS239x hot swap devices.
- **MOSFET Gate Drivers:** A powerful family of gate driver ICs, featuring a combined bipolar and MOSFET manufacturing process, delivering fast switching transitions and high current output capability
- **PWM Controllers and Special Functions:** The industry's largest selection of controllers and an extensive selection of support ICs facilitate the efficient design of discrete power supplies.
- **Linear Regulators:** For the lowest-cost power solution, a broad range of LDOs support currents ranging from 10 mA to 7 A.

### TO KNOW MORE ►

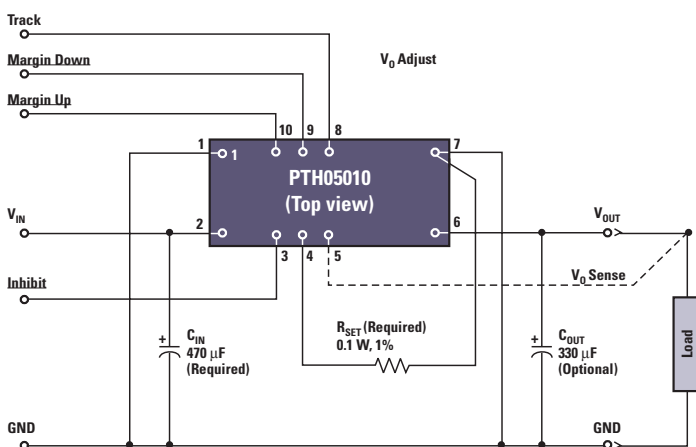
For detailed information about power management ICs for wireless infrastructure:

DC/DC converters	39
Controllers	40
MOSFET driver	43
LoadShare controller	43
LDOs	44
Product selection guides	45

Board Power Point-of-Load Power Solutions

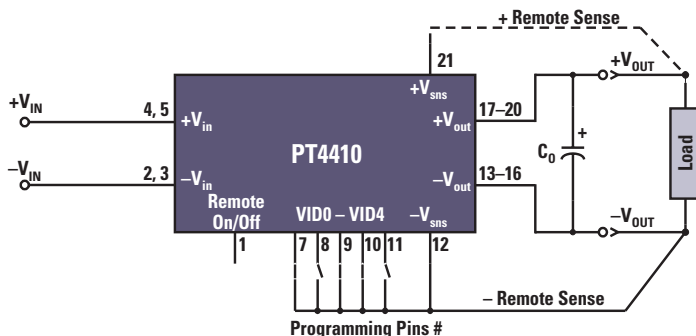


PTH05010 Block Diagram

**Applications:**

- Wireless infrastructure
- Telecom
- Networking
- Servers

PT4410 Block Diagram

**Applications:**

- Wireless infrastructure
- Telecom
- Networking

## POINT-OF-LOAD POWER MODULES OFFER AUTO-TRACK™ SEQUENCING

### PTH Series of Point-of-Load Modules

Get samples and datasheets at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in the URL with *pthxx000*, *pthxx050*, *pthxx060*, *pthxx010*, *pthxx0020*, *pthxx030* where *xx* = input voltage = 03, 05, or 12

The PTHxx series of plug-in power modules will support step-down DC/DC conversion from a 3.3 V, 5 V or 12 V input with adjustable output voltages from 0.8 V to 5.5 V at output currents up to 30 A. The power modules incorporate an innovative new Auto-Track sequencing technology, which allows multiple modules to be powered up and down in sequence without external circuitry.

**Key Features:**

- Auto-Track sequencing
- Margin-up/down controls
- Pre-bias startup capability
- Output current up to 30 A
- Efficiencies up to 96%
- Point-of-Load Alliance (POLA) compatible
- Packaging: Low-profile DIP module

## 75-W/100-W CONVERTERS OFFER 90% EFFICIENCY

### PT4410

Get samples and datasheets at:

[www.ti.com/sc/device/pt4410](http://www.ti.com/sc/device/pt4410)

The PT4410 series of power modules are single-output isolated DC/DC converters housed in a compact 21-pin low-profile (12-mm) package. These modules are rated up to 75 W with load currents as high as 30 A. The output voltage is set within a pre-defined range via a 5-bit input code and is adjustable.

**Key Features:**

- 90% efficiency
- Output power: 75 W or 100 W
- 36-V to 75-V input
- 5-bit programmable output voltage
- 1500-V DC isolation
- On/off control
- Over-current protection
- Differential remote sense
- Output over-voltage protection
- Over-temperature shutdown
- Under-voltage lockout
- Space-saving solderable copper case
- Packaging: Low profile, 12 mm

## TRIPLE-OUTPUT MODULES FEATURE 50% SMALLER FOOTPRINT PLUS SEQUENCING

### PT4820/PT4850

Get samples and datasheets at:  
[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

Replace partnumber in the URL with *pt4820* or *pt4850*

The PT4820 and PT4850 Excalibur™ power modules are a series of isolated triple-output DC/DC converters that operate from a standard (-48 V) central office supply. These modules are rated for a combined output of up to 12 A or 25 A and are designed for powering mixed-logic applications. Output voltage options include a low-voltage output for a DSP or ASIC core and two additional supply voltages for the I/O and other functions.

#### Key Features:

- Three independently regulated outputs
- Internal power-up and power-down sequencing
- Output power: 35 W or 75 W
- Input voltage range: 36 V to 75 V
- 1500-V DC isolation
- Dual logic-on/off control
- Short-circuit protection (all outputs)
- Over-temperature shutdown

## -48 V, 8-PIN, HOT SWAP CONTROLLERS

### TPS2390/TPS2391

Get samples and datasheets at:  
[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

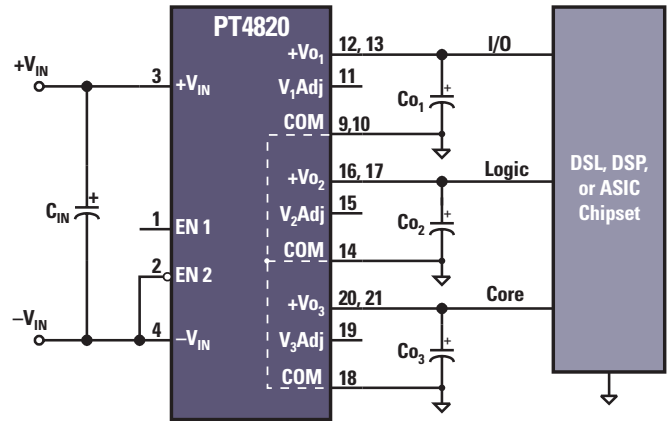
Replace partnumber in the URL with *tps2390* or *tps2391*

The TPS2390 and TPS2391 Hot Swap power managers are optimized for use in nominal -48-V systems. Designed for supply voltage ranges up to -80 V, they are rated to withstand spikes to -100 V. In conjunction with an external N-channel FET and sense resistor, these controllers can be used to enable the live insertion of plug-in cards and modules in powered systems.

#### Key Features:

- Wide input supply range: -36 V to -80 V
- Transient rating to -100 V
- Programmable current limit and current slew rate
- Enable input (EN)
- Fault timer to eliminate nuisance trips
- Open-drain fault output
- Requires few external components
- Packaging: 8-pin MSOP

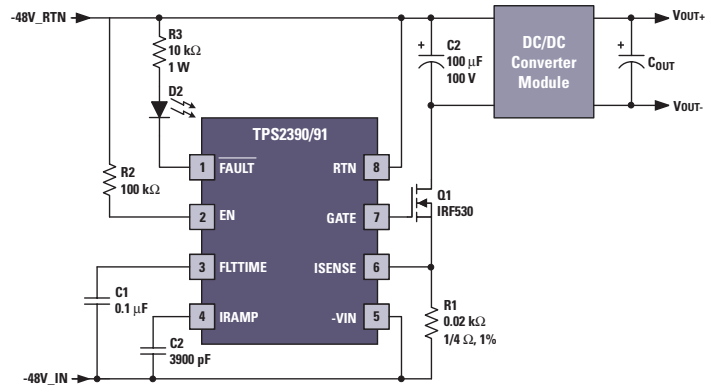
PT4820/50 Block Diagram



#### Applications:

- Wireless infrastructure
- Telecom
- Networking

TPS2390/91 Block Diagram



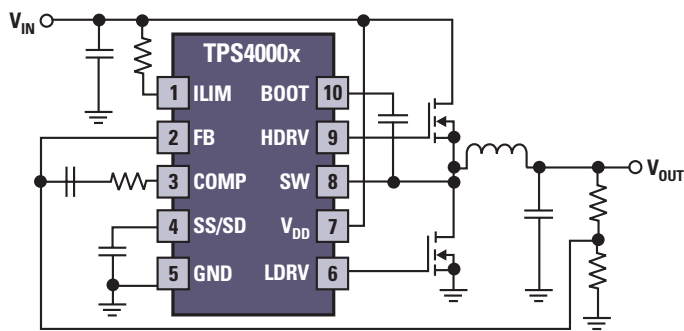
#### Applications:

- On-card hot swap
- -48-V distributed power systems

Device	Auto-Retry	Output
TPS2350	Yes	PG
TPS2390	No	Fault
TPS2391	Yes	Fault
TPS2392	No	PG/Fault
TPS2393	Yes	PG/Fault
TPS2398	No	PG
TPS2399	Yes	PG
TPS2490	No	PG
TPS2491	Yes	PG



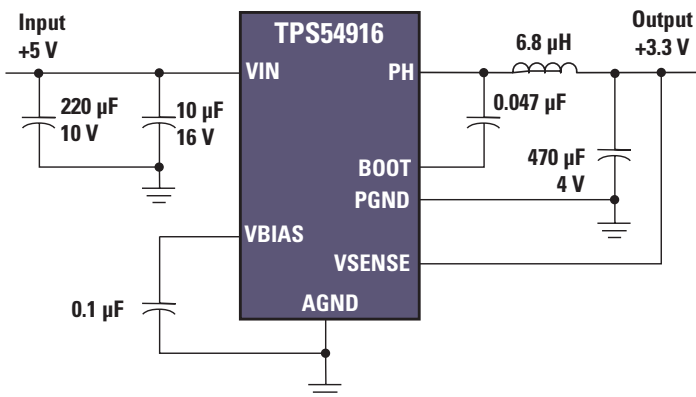
TPS4000x Block Diagram



**Applications:**

- Wireless infrastructure
- Networking equipment
- Telecom equipment
- Base stations
- DSP power

TPS54916 Block Diagram



Part Number	I <sub>OUT</sub> (A)	V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	Price <sup>1</sup>
TPS54910	9	3–4	Adj. to 0.9 V	5.20
TPS54810	8	4–6	Adj. to 0.9 V	4.90
TPS5461x	6	3–6	0.9, 1.2, 1.5, 1.8, 2.5, 3.3 V adj.	4.65
TPS5431x*	3	3–6	0.9, 1.2, 1.5, 1.8, 2.5, 3.3 V adj.	3.45

\*20-pin HTSSOP package

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## HIGH-EFFICIENCY SYNCHRONOUS BUCK DC/DC CONTROLLERS

### TPS4000x

Get samples and datasheets at: [power.ti.com](http://power.ti.com)

The TPS4000x are controllers for low-voltage, non-isolated synchronous buck regulators and drive N-channel power MOSFETs. They control the delays from main switch-off to rectifier turn-on and from rectifier turn-off to main switch turn-on, minimizing diode losses (both conduction and recovery) in the synchronous rectifier with TI's proprietary Predictive Gate Drive™ technology.

**Key Features:**

- Input voltage range: 2.25 V to 5.5 V
- Output voltage as low as 0.7 V
- 1% internal 0.7-V reference
- Predictive Gate Drive N-channel MOSFET drivers for higher efficiency
- Externally adjustable soft-start and overcurrent limit
- Fixed-frequency, 300-kHz or 600-kHz voltage-mode control
- Packaging: 10-lead MSOP PowerPAD™ for higher performance

## SYNCHRONOUS BUCK DC/DC CONVERTERS WITH INTEGRATED MOSFETS

### TPS54916

For datasheets, samples, app notes, EVMs, and software, go to: [power.ti.com/swift](http://power.ti.com/swift)

**Key Features:**

- Input voltage range: 3.0 V to 6.0 V
- Internal MOSFET switches for high efficiency at full load output current
- Adjustable output voltage range down to 0.9 V with 1.0% accuracy
- Wide PWM frequency: Fixed 350 kHz, 550 kHz, or adjustable 280 kHz to 700 kHz
- Load protected by peak current limit and thermal shutdown
- PowerGood, enable, and slow-start
- Reduces board area and component count
- Packaging: 28-pin HTSSOP

**Applications:**

- Low-voltage, high-density distributed power
- Point-of-load regulation for high-performance DSPs, FPGAs, ASICs, and microprocessors
- Broadband, networking, and optical communications infrastructure

## TRACKING SWITCHER WITH INTEGRATED FETS FOR SEQUENCING

### TPS54680

Get datasheets, EVMs, samples, application notes, and software tools at:

[www.ti.com/sc/device/tps54680](http://www.ti.com/sc/device/tps54680)

System designers must consider the timing and voltage differences between core and I/O power supplies (i.e., power supply sequencing) during power up and power down. The TPS54680 solution easily accomplishes simultaneous power-up and power-down without the need of additional complex sequencing circuitry.

#### Key Features:

- Power-up/down tracking
- Input voltage range: 3.0 V to 6.0 V
- Internal 30-m $\Omega$ , 12-A peak MOSFET switches for high efficiency at 6-A continuous output
- Switching frequency fixed at 350 kHz or adjustable from 280 kHz to 700 kHz
- PowerGood and enable functions
- Load protected by peak current limit and thermal shutdown
- Packaging: 28-pin HTSSOP PowerPAD™

## 95% EFFICIENT, 600-mA, STEP-DOWN CONVERTERS

### TPS6200x

Get datasheets and samples at:

[www.ti.com/sc/device/partnumber](http://www.ti.com/sc/device/partnumber)

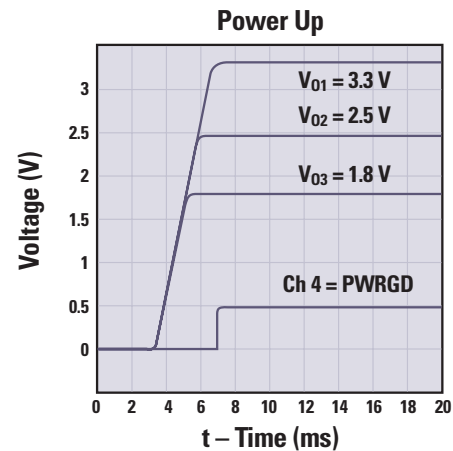
Replace partnumber in URL with *tps62000*, *tps62001*, *tps62002*, *tps62003*, *tps62004*, *tps62005*, *tps62006*, *tps62007*, or *tps62008*

The TPS6200x high-efficiency, synchronous step-down converters are ideal for high-efficiency power conversion in sub-systems with input voltages between 2.0 V and 5.5 V.

#### Key Features:

- 2.0-V to 6.0-V input voltage range
- Adjustable-output voltage range from 0.8 V to  $V_I$
- Fixed-output voltage options available
- Up to 600-mA output current
- Synchronizable to external clock signal up to 1 MHz
- Highest efficiency over wide-load current range due to PFM power-save mode
- 50- $\mu$ A quiescent current (typ)
- Packaging: 3  $\times$  5 mm<sup>2</sup> MSOP-10

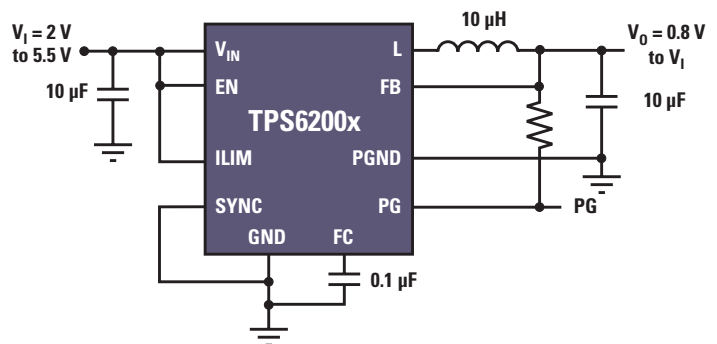
Sequential Startup Waveform



#### Applications:

- DSPs, FPGAs, ASICs, and microprocessors that require simultaneous start up
- Broadband, datacom, and optical communications infrastructure
- Precision point-of-load regulation

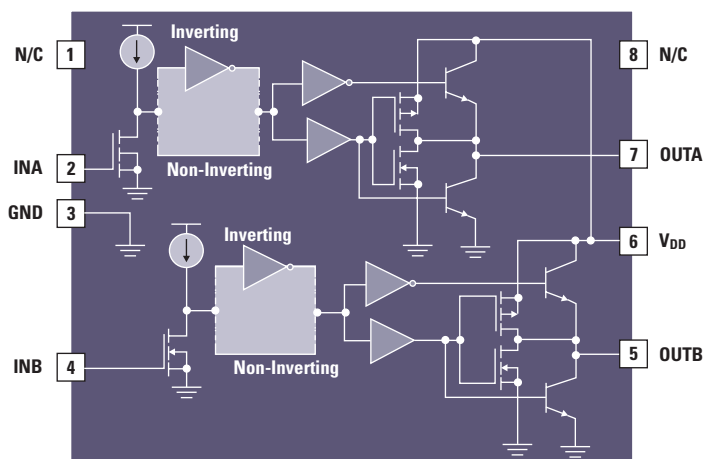
TPS6200x Application Diagram



#### Applications:

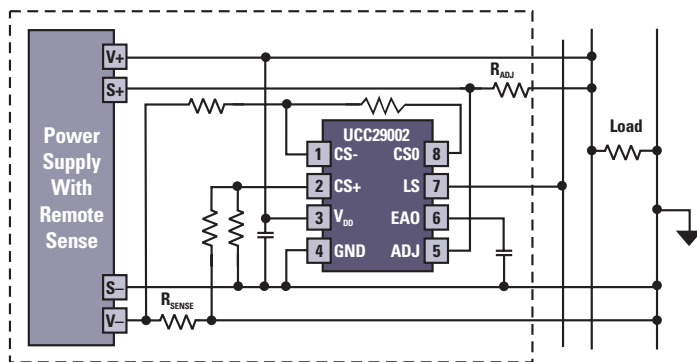
- DSP
- $\mu$ C processor core
- System voltage supply

UCC27323 Block Diagram

**Applications:**

- Switch-mode power supplies:
  - Off-line power supplies
  - DC/DC converters
  - Board mount power supplies

UCC29002 Typical Low-Side Current-Sensing Application

**System Configurations:**

- Modules with remote sense capability
- Modules with adjust input
- Modules with both remote sense and adjust input
- In conjunction with the internal feedback E/A of OEM power supply units

**Applications:**

- Paralleled solution for DC/DC distribution
  - Redundant power supplies
  - SMPS for (web) servers
  - Server, workstation, and telecom systems

**DUAL, 4-AMP, MOSFET GATE DRIVER****UCC27323**

Get samples and datasheets at:  
[www.ti.com/sc/device/ucc27323](http://www.ti.com/sc/device/ucc27323)

The UCC27323/4/5 family of high-speed dual-MOSFET drivers can deliver large peak currents into capacitive loads, typical of a power MOSFET gate. Three standard logic options are offered – dual-inverting, dual-noninverting, and one inverting and one non-inverting driver.

**Key Features:**

- High current drive capability of  $\pm 4$  A at the Miller Plateau region
- Industry-standard pin-out
- Efficient constant-current sourcing using a unique bipolar and CMOS output stage
- TTL-/CMOS-compatible inputs independent of supply voltage
- 4-V to 15-V supply voltage
- Packaging: Thermally enhanced MSOP PowerPAD™ with 4.7 C/W  $\theta_{jc}$

**LOADSHARE CONTROLLER FOR PARALLEL POWER SUPPLIES****UCC29002**

Get samples and datasheets at:  
[www.ti.com/sc/device/ucc29002](http://www.ti.com/sc/device/ucc29002)

The UCC29002 is an advanced, high-performance, low-cost LoadShare controller that provides all necessary functions to parallel multiple independent power supplies or DC-to-DC modules. Targeted for high-reliability applications in telecom distributed-power systems, the controller is suitable for N+1 redundant systems or high-current applications where off-the-shelf power supplies need to be paralleled.

**Key Features:**

- High accuracy, better than 1% current share error at full load
- High-side or low-side (GND reference) current-sense capability
- Ultra-low offset current-sense amplifier
- Single-wire LoadShare bus
- Full scale adjustability
- Intel® SSI LoadShare specification compliant
- Disconnect from LoadShare bus at stand-by
- LoadShare bus protection against shorts to GND or to the supply rail
- Packaging: 8-pin MSOP minimizes space
- Lead-free assembly

## LOW-INPUT-VOLTAGE, OUTPUT-CAP-FREE, 1-A LDO FOR SIMPLE, HIGHLY EFFICIENT REGULATION

TPS725xx/TPS726xx

Get samples, datasheets, and EVMs at: [power.ti.com](http://power.ti.com)

The TPS725xx/726xx families of Low-Dropout Regulators (LDOs) help you achieve as high as 83% efficiency with the low-input-voltage feature, rivaling a switch-mode solution. These devices offer simplicity, minimized component count, and low-noise performance in post-regulation applications, as shown in the diagram.

### Key Features:

- Supports input voltages as low as 1.8 V (and up to 5.5 V), allowing up to 83% efficiency
- No output capacitor required for stability
- 1-A LDO with integrated SVS (50-ms delay), TPS725xx
- 1-A LDO with integrated SVS (200-ms delay), TPS726xx
- 1.5-/1.6-/1.8-/2.5-V fixed-output, and adjustable-output versions available
- Dropout voltage typically 170 mV at 1 A
- Less than 1- $\mu$ A quiescent current in shutdown mode
- Packaging: SOT-223-5, DDPAK

## ULTRA-LOW-NOISE, HIGH-PSRR, FAST-RF LDO IN SOT-23

TPS791xx/TPS792xx/TPS793xx/TPS794xx/TPS795xx/TPS796xx/TPS786xx

Get samples, datasheets, and EVMs at: [power.ti.com](http://power.ti.com)

The TPS79xxx family of Low-Dropout Regulators (LDOs) features extremely high PSRR and ultra-low-noise performance to support noise-sensitive applications such as powering RF amplifiers.

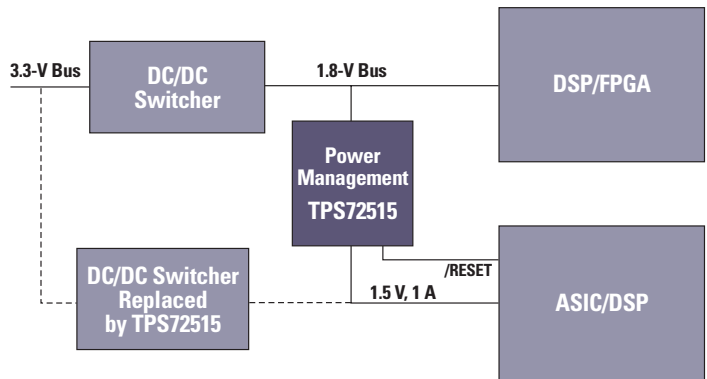
### Key Features:

- Output current: 100 mA to 1.5 A (see table at right)
- Input voltage: 2.7 V to 5.5 V
- Output capacitor: 1.0- $\mu$ F or 2.2- $\mu$ F ceramic
- High PSRR: 70 dB at 10 kHz
- Ultra-low noise: 15  $\mu$ VRMS (TPS791xx)
- Fast start time: 50  $\mu$ s (TPS792xx)
- Dropout voltage: 38 mV at 100 mA (TPS791xx)
- Packaging: SOT-23-5, MSOP-8, SOT-223-5, DDPAK

### Applications:

- RF
- VCOs
- DSP/FPGA/ASIC/microprocessor supplies

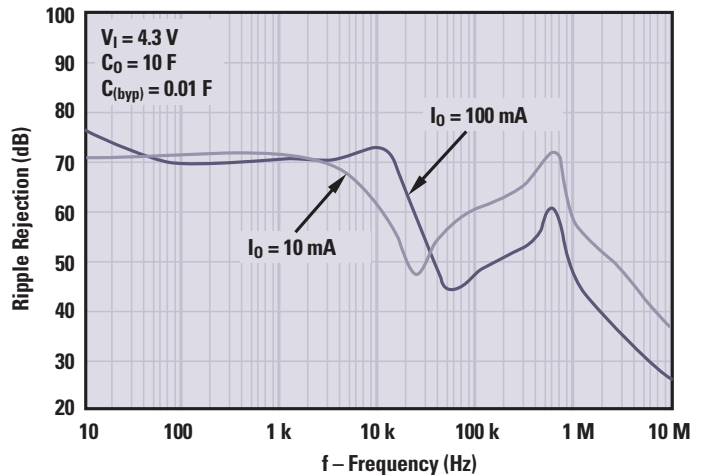
TPS725xx Application Diagram



### Applications:

- Post-regulation of switch-mode supplies
- Powering core voltages of DSPs, FPGAs, ASICs, and microprocessors

TPS791xx PSRR Performance



Device <sup>1</sup>	I <sub>o</sub> (mA)	V <sub>o</sub> (V)	Peak Current (mA)
TPS791xx	100	1.8/3.3/4.7/adj.	285
TPS792xx	100	2.5/2.8/3.0/adj.	285
TPS793xx	200	1.8/2.5/2.8/2.85/ 3.0/3.3/4.75/adj.	285
TPS794xx	250	1.8/2.5/2.8/3.0/3.3/adj.	700
TPS795xx	500	1.6/1.8/2.5/3.0/3.3/adj.	2400
TPS796xx	1000	1.8/2.5/2.8/3.0/3.3/adj.	2400
TPS786xx	1500	1.8/2.5/2.8/3.0/3.3/adj.	2400

<sup>1</sup>xx represents the 2 digits of output voltage.

## DC/DC CONVERTERS (INTEGRATED SWITCH)

Device	I <sub>OUT</sub> (mA)	Switch Current Limit (max) (mA)	V <sub>IN</sub> (V)	V <sub>OUT</sub> Adj (V)	V <sub>OUT</sub> Fix (V)	Efficiency (%)	Switching Frequency (max) (kHz)	Quiescent Current (typ) (mA)	Shutdown Current (typ) (µA)	Features										Packaging					Price <sup>2</sup>
										Shutdown	LDO (mA)	Low Battery	Power Good	Power Sequencing	Dual Input Bus (3.3, 2.5 V)	Undervoltage Lockout	DDR Memory	DSDS <sup>1</sup>	Current Limit	Thermal Limit	SOT-23	MSOP	QFN	TSSOP	
<b>Low Power Step Down (Buck) Converters — up to 1.2 A</b>																									
TPS62200	300	670	2.5 to 6.0	0.7 to 6.0	—	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62201	300	670	2.5 to 6.0	—	1.5	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62202	300	670	2.5 to 6.0	—	1.8	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62203	300	670	2.5 to 6.0	—	3.3	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62204	300	670	2.5 to 6.0	—	1.6	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62205	300	670	2.5 to 6.0	—	2.5	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62206	300	670	2.5 to 6.0	—	2.6	97	1000	0.015	0.1	✓						✓		✓	✓	6			✓	1.29	
TPS62000	600	1600	2.0 to 5.5	0.8 to 5.0	—	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62001	600	1600	2.0 to 5.5	—	0.9	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62002	600	1600	2.0 to 5.5	—	1.0	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62003	600	1600	2.0 to 5.5	—	1.2	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62004	600	1600	2.0 to 5.5	—	1.5	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62005	600	1600	2.0 to 5.5	—	1.8	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62006	600	1600	2.0 to 5.5	—	2.5	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62007	600	1600	2.0 to 5.5	—	3.3	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
TPS62008	600	1600	2.0 to 5.5	—	1.9	95	1000	0.05	0.1	✓		✓	✓			✓		✓		10			✓	1.49	
<b>SWIFT™ Step Down (Buck) Converters — up to 9 A</b>																									
TPS54310	3000	6500	3.0 to 6.0	0.9 to 4.5	—	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54311	3000	6500	3.0 to 6.0	—	0.9	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54312	3000	6500	3.0 to 6.0	—	1.2	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54313	3000	6500	3.0 to 6.0	—	1.5	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54314	3000	6500	3.0 to 6.0	—	1.8	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54315	3000	6500	3.0 to 6.0	—	2.5	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54316	3000	6500	3.0 to 6.0	—	3.3	90	700	6.2	1000	✓		✓				✓		✓		20			✓	3.45	
TPS54372	3000	6500	3.0 to 6.0	0.2 to 4.5	—	90	700	6.2	1000	✓					✓		✓		✓	20			✓	3.45	
TPS54610	6000	10000	3.0 to 6.0	0.9 to 4.5	—	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54611	6000	10000	3.0 to 6.0	—	0.9	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54612	6000	10000	3.0 to 6.0	—	1.2	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54613	6000	10000	3.0 to 6.0	—	1.5	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54614	6000	10000	3.0 to 6.0	—	1.8	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54615	6000	10000	3.0 to 6.0	—	2.5	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54616	6000	10000	3.0 to 6.0	—	3.3	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
TPS54672	6000	10000	3.0 to 6.0	0.2 to 4.5	—	90	700	11	1000	✓					✓		✓		✓	28			✓	4.65	
TPS54673	6000	10000	3.0 to 6.0	0.9 to 4.5	—	90	700	11	1000	✓		✓				✓		✓		28			✓	4.65	
<b>TPS54680</b>	<b>6000</b>	<b>10000</b>	<b>3.0 to 6.0</b>	<b>0.9 to 4.5</b>	<b>—</b>	<b>90</b>	<b>700</b>	<b>11</b>	<b>1000</b>	✓		✓	✓			✓		✓		<b>28</b>			✓	<b>4.65</b>	
TPS54810	8000	11000	4.0 to 6.0	0.9 to 4.5	—	85	700	11	1000	✓		✓				✓		✓		28			✓	4.90	
TPS54872	8000	11000	4.0 to 6.0	0.2 to 4.5	—	85	700	11	1000	✓					✓		✓		✓	28			✓	4.90	
TPS54873	8000	11000	4.0 to 6.0	0.9 to 4.5	—	85	700	11	1000	✓		✓				✓		✓		28			✓	4.90	
<b>TPS54880</b>	<b>8000</b>	<b>11000</b>	<b>4.0 to 6.0</b>	<b>0.9 to 4.5</b>	<b>—</b>	<b>85</b>	<b>700</b>	<b>11</b>	<b>1000</b>	✓		✓	✓			✓		✓		<b>28</b>			✓	<b>4.90</b>	
TPS54910	9000	15000	3.0 to 4.0	0.9 to 2.5	—	90	700	11	1000	✓		✓				✓		✓		28			✓	5.20	
TPS54972	9000	15000	3.0 to 4.0	0.2 to 2.5	—	90	700	11	1000	✓					✓		✓		✓	28			✓	5.20	
TPS54973	9000	15000	3.0 to 4.0	0.9 to 2.5	—	90	700	11	1000	✓		✓				✓		✓		28			✓	5.20	
<b>TPS54974</b>	<b>9000</b>	<b>15000</b>	<b>2.2 to 4.0</b>	<b>0.2 to 2.5</b>	<b>—</b>	<b>90</b>	<b>700</b>	<b>11</b>	<b>1000</b>	✓					✓		✓		✓	<b>28</b>			✓	<b>5.20</b>	
<b>TPS54980</b>	<b>9000</b>	<b>15000</b>	<b>3.0 to 4.0</b>	<b>0.9 to 2.5</b>	<b>—</b>	<b>90</b>	<b>700</b>	<b>11</b>	<b>1000</b>	✓		✓	✓			✓		✓		<b>28</b>			✓	<b>5.20</b>	

<sup>1</sup>Disabled sinking during start-up.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

*New devices are listed in red.*

## PLUG-IN POWER SOLUTIONS

Device <sup>1</sup>	Input Bus Voltage (V)	P <sub>OUT</sub> or I <sub>OUT</sub>	Isolated Outputs	V <sub>O</sub> Range (V)	V <sub>O</sub> Adjustable	Price <sup>2</sup>
<b>Non-Isolated Single Positive Output</b>						
<b>PTH03010/20/30/50/60</b>	<b>3.3</b>	<b>15 A, 22 A, 30 A, 6 A, 10 A</b>	<b>No</b>	<b>0.8 to 2.5</b>	<b>Yes</b>	<b>14.00, 18.13, 24.63, 9.10, 11.20</b>
<b>PTH05010/20/30/50/60</b>	<b>5</b>	<b>15 A, 22 A, 30 A, 6 A, 10 A</b>	<b>No</b>	<b>0.8 to 3.6</b>	<b>Yes</b>	<b>14.00, 18.13, 24.63, 9.10, 11.20</b>
<b>PTH12010/20/30/50/60</b>	<b>12</b>	<b>12 A, 18 A, 26 A, 6 A, 8 A</b>	<b>No</b>	<b>1.2 to 5.5</b>	<b>Yes</b>	<b>14.00, 18.13, 24.63, 9.10, 11.20</b>

<sup>1</sup>See [power.ti.com](http://power.ti.com) for a complete product offering.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

*New devices are listed in red.*

## LOW DROPOUT REGULATORS (LDOs)

Device	I <sub>O</sub> (mA)	V <sub>DO</sub> @ I <sub>O</sub> (mV)	I <sub>q</sub> @ I <sub>O</sub> (µA)	Output Options			Min V <sub>IN</sub>	Max V <sub>IN</sub>	Accuracy (%)	Packages										Features <sup>1</sup>	C <sub>0</sub> <sup>2</sup>	Comments	Price <sup>3</sup>
				Negative Out	Voltage (V)	Adj.																	
										SC70	SOT23	MSOP	S08	SOT23	PWP	T0263	T0220	PW	DDPAK				
TPS797xx	10	105	1.2		1.8, 3, 3.3		1.8	5.5	4	✓									PG	0.47 µF C	MSP430; lowest I <sub>q</sub>	0.32	
TPS715xx	50	415	3.2		2.5, 3, 3.3, 5	✓	2.5	24	4	✓										0.47 µF C	Ultra-low I <sub>q</sub>	0.32	
TPS770xx	50	35	17		1.2, 1.5, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 5	✓	2.7	10	3		✓								/EN	4.7 µF T	Low I <sub>q</sub>	0.34	
TPS722xx	50	50	80		1.5, 1.6, 1.8	✓	1.8	5.5	3		✓								EN	0.1 µF C	Low noise & low V <sub>IN</sub>	0.39	
TPS760xx	50	120	90		3, 3.2, 3.3, 3.8, 5.0		3.2	16	2		✓								EN	2.2 µF T	Bipolar, low cost	0.34	
TPS769xx	100	70	18		1.2, 1.5, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 5	✓	2.7	10	3		✓								/EN	4.7 µF T	Low cost	0.29	
REG101	100	60	400		2.5, 2.8, 2.85, 3, 3.3, 5	✓	2.6	10	1.5		✓		✓						EN, BP	No Cap	Low noise	0.88	
TPS791xx	100	38	185		1.8, 3.3, 4.7	✓	2.7	5.5	2		✓								/EN, BP	1 µF C	RF low noise, high PSRR	0.38	
TPS792xx	100	38	185		2.5, 2.8, 3	✓	2.7	5.5	2		✓								EN, BP	1 µF C	RF low noise, high PSRR	0.38	
TPS761xx	100	170	90		3, 3.2, 3.3, 3.8, 5		3.4	16	2		✓								EN	4.7 µF T	Bipolar, low cost	0.35	
TPS763xx	150	180	85		1.6, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 3.8, 5	✓	2.7	10	3		✓								EN	4.7 µF T	Low cost	0.29	
TPS764xx	150	300	85		2.5, 2.7, 2.8, 3, 3.3		2.7	10	3		✓								EN, BP	4.7 µF T	TPS763xx + low noise	0.29	
TPS771xx	150	75	90		1.5, 1.8, 2.7, 2.8, 3.3, 5	✓	2.7	10	2			✓							/EN, SVS	10 µF T	Low noise	0.56	
<b>TPS731xx</b>	<b>150</b>	<b>60</b>	<b>450</b>		<b>1.5, 1.8, 2.5, 3.0, 3.3, 5.0</b>	<b>✓</b>	<b>1.8</b>	<b>5.5</b>	<b>2</b>		<b>✓</b>								<b>EN, BP</b>	<b>No Cap</b>	<b>Reverse leakage protection</b>	<b>0.45</b>	
<b>SN105125</b>	<b>150</b>	<b>1 V</b>	<b>150</b>		<b>1.2</b>	<b>—</b>	<b>3</b>	<b>5.25</b>	<b>2</b>		<b>✓</b>								<b>EN, PG</b>	<b>1 µF C</b>	<b>Reverse leakage protection</b>	<b>0.29</b>	
TPS788xx	150	150	18		2.5, 3.3		2.7	10	3		✓								/EN	4.7 µF T	USB inrush control	0.36	
TPS721xx	150	150	90		1.5, 1.6, 1.8	✓	1.8	5.5	3		✓								EN	0.1 µF C	Low noise & low V <sub>IN</sub>	0.39	
TL750/1Lxx	150	600	1 mA		5, 10, 12		6	26	4			✓							/EN	10 µF T	60-V load dump	0.45	
TPS793xx	200	77	180		1.8, 2.5, 2.8, 2.85, 3, 3.3, 4.75	✓	2.7	5.5	2		✓								EN, BP	2.2 µF C	RF low noise, high PSRR	0.40	
TPS794xx	250	145	172		1.8, 2.5, 2.8, 3, 3.3	4	2.7	5.5	3			✓		✓					EN, BP	2.2 µF C	RF low noise, high PSRR	0.62	
<b>TPS732xx</b>	<b>250</b>	<b>100</b>	<b>450</b>		<b>1.5, 1.8, 2.5, 3, 3.3, 5.0</b>	<b>✓</b>	<b>1.8</b>	<b>5.5</b>	<b>2</b>		<b>✓</b>				✓				<b>EN, BP</b>	<b>No Cap</b>	<b>Reverse leakage protection</b>	<b>0.65</b>	
TPS773xx	250	125	90		1.5, 1.6, 1.8, 2.7, 2.8, 3.3, 5	✓	2.7	10	2		✓								/EN, SVS	10 µF T	Low noise	0.65	
TPS779xx	250	250	90		1.8, 2.5, 3	✓	2.7	10	2		✓								EN, SVS	10 µF T	Low noise	0.65	
REG102	250	150	400		2.5, 2.8, 2.85, 3, 3.3, 5	✓	2.6	10	1.5		✓		✓	✓					EN, BP	No Cap	Capacitor free, DMOS	1.00	
<b>TPS736xx</b>	<b>400</b>	<b>160</b>	<b>450</b>		<b>1.5, 1.8, 2.5, 3.0, 3.3</b>	<b>✓</b>	<b>1.8</b>	<b>5.5</b>	<b>2</b>		<b>✓</b>			✓					<b>EN, BP</b>	<b>No Cap</b>	<b>Reverse leakage protection</b>	<b>0.80</b>	
REG113	400	250	400		2.5, 2.85, 3, 3.3, 5		2.6	10	1.5		✓	✓							EN, BP	No Cap	Capacitor free, DMOS	1.04	
TPS795xx	500	105	265		1.6, 1.8, 2.5, 3, 3.3	✓	2.7	5.5	3			✓		✓					EN, BP	1 µF C	RF low noise, high PSRR	0.95	
TPS775xx	500	169	87		1.5, 1.6, 1.8, 2.5, 3.3	✓	2.7	10	2			✓		✓					/EN, SVS	10 µF T	Fast transient response	0.87	
TPS776xx	500	169	87		1.5, 1.8, 2.5, 2.8, 3.3	✓	2.7	10	2			✓		✓					/EN, PG	10 µF T	Fast transient response	0.83	
REG103	500	115	500		2.5, 2.7, 3, 3.3, 5	✓	2.6	15	2			✓		✓					EN, PG	No Cap	Capacitor free, DMOS	2.00	
TPS777xx	750	260	85		1.5, 1.8, 2.5, 3.3	✓	2.7	10	2			✓		✓					/EN, SVS	10 µF T	Fast transient response	0.96	
TPS725xx	1000	170	75		1.5, 1.6, 1.8, 2.5	✓	1.8	6	2			✓		✓					EN, SVS	No Cap	Low noise; SVS delay 50 ms	1.04	
TPS726xx	1000	170	75		1.5, 1.6, 1.8, 2.5	—	1.8	6	2			✓		✓					EN, SVS	No Cap	Low noise; SVS delay 200 ms	1.04	
TPS796xx	1000	200	310		1.8, 2.5, 2.8, 3, 3.3	✓	2.7	5.5	2			✓		✓					EN, BP	1 µF C	RF low noise, high PSRR	1.04	
TPS767xx	1000	230	85		1.5, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 5	✓	2.7	10	2			✓		✓					/EN, SVS	10 µF T	Fast transient response	1.04	
TPS768xx	1000	230	80		1.5, 1.8, 2.5, 2.7, 2.8, 3, 3.3, 5	✓	2.7	10	2			✓		✓					/EN, PG	10 µF T	Fast transient response	1.00	
UCCx81-x	1000	500	400		3.3, 5	✓	1.8	9	2.5										EN	2.2 µF T	Reverse leakage protection	1.80	
REG104	1000	230	600		2.5, 2.7, 3, 3.3, 5	✓	2.6	15	2			✓		✓					EN	No Cap	Capacitor free, DMOS	2.22	
<b>TLV1112</b>	<b>1000</b>	<b>1200</b>	<b>5 mA</b>		<b>1.2</b>	<b>—</b>	<b>2.7</b>	<b>18</b>	<b>2.5</b>				✓		✓					<b>10 µF T</b>	<b>Low cost regulator</b>	<b>0.35</b>	
<b>TLV1117</b>	<b>1000</b>	<b>1200</b>	<b>5 mA</b>		<b>1.5, 1.8, 2.5, 2.85, 3.3, 5</b>	<b>✓</b>	<b>2.7</b>	<b>18</b>	<b>2.5</b>				✓		✓					<b>10 µF T</b>	<b>Low cost regulator</b>	<b>0.32</b>	
TPS786xx	1500	390	310		1.8, 2.5, 2.8, 3, 3.3	✓	2.7	5.5	3			✓		✓					EN, BP	1 µF C	RF low noise, high PSRR	1.28	
TPS751xx	1500	160	75		1.5, 1.8, 2.5, 3.3	✓	2.7	5.0	2				✓						/EN, PG	47 µF T	Fast transient response	1.52	
TPS752xx	2000	210	75		1.5, 1.8, 2.5, 3.3	✓	2.7	5.0	2				✓						/EN, SVS	47 µF T	Fast transient response	1.71	
TPS754xx	2000	210	75		1.5, 1.8, 2.5, 3.3	✓	2.7	5.0	2				✓						/EN, PG	47 µF T	Fast transient response	1.65	
UCC382-x	3000	350	6 mA		1.5, 2.1, 2.5	✓	1.7	7.5	1					✓		✓				100 µF T	Fast LDO with reverse leak.	2.57	
UCC383-x	3000	400	400		3.3, 5	✓	1.8	9	2.5					✓		✓			/EN	22 µF T	Reverse leakage protection	2.57	
TPS758xx	3000	150	110		1.5, 1.8, 2.5, 3.3	✓	2.8	5.5	3				✓		✓				EN	47 µF T	Fast transient response	2.57	
UCC385-x	5000	350	8 mA		1.5, 2.1, 2.5	✓	1.7	7.5	1					✓		✓				100 µF T	Fast LDO with reverse leak.	3.00	
TPS756xx	5000	250	110		1.5, 1.8, 2.5, 3.3	✓	2.8	5.5	3				✓		✓				EN	47 µF T	Fast transient response	2.83	
TPS759xx	7500	400	110		1.5, 1.8, 2.5, 3.3	✓	2.8	5.5	3				✓		✓				/EN, PG	47 µF T	Fast transient response	3.04	

<sup>1</sup>PG = PowerGood, EN = Active High Enable, /EN = Active Low Enable, SVS = Supply Voltage Supervisor  
<sup>3</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

<sup>2</sup>C = Ceramic, T = Tantalum, No Cap = Capacitor Free LDO  
*New devices are listed in red.*

## MOSFET DRIVER

Device	No. of Outputs	Output Configuration	Output Type	I <sub>O</sub> Source/Sink (A)	Rise/Fall Time (ns)	V <sub>CC</sub> Range (V)	Prop Delay (ns)	Input Threshold	Enable	Dead Time Control	Protection Features	Internal Regulator	Price <sup>1</sup>
UCC37323	2	Inverting	TrueDrive	4.0/4.0	25/25	4 to 15	35	TTL/CMOS	No	No	—	No	0.99

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## LOADSHARE CONTROLLERS

Device	V <sub>IN</sub> (min)	V <sub>IN</sub> (max)	Reference Accuracy (%)	Share Bus	Pin Count	Supply Current (mA)	Price <sup>1</sup>
UCC29002	4	15	—	Single Ended	8	2.5	0.89

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

General Overview

Signal Chain

Timing & Interface

Logic

Power Management

## DUAL-OUTPUT LDOs

Device	I <sub>O1</sub> (mA)	I <sub>O2</sub> (mA)	V <sub>DO1</sub> @ I <sub>O1</sub> (mV)	V <sub>DO2</sub> @ I <sub>O2</sub> (mV)	I <sub>q</sub> @ I <sub>O</sub> (μA)	Output Options		Accuracy (%)	PWP Package	Min V <sub>O</sub>	Max V <sub>O</sub>	Features							C <sub>O</sub> <sup>1</sup>	Description	Price <sup>2</sup>
						Voltage (V)	Adj.					/EN	PG	SVS	Seq	Low Noise	Min V <sub>IN</sub>	Max V <sub>IN</sub>			
TPS707xx	250	150	83	—	95	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5	✓	✓	✓	✓	✓	2.7	5.5	10 μF T	Dual-output LDO with sequencing	1.91
TPS708xx	250	150	83	—	95	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5	✓	✓	✓		✓	2.7	5.5	10 μF T	Dual-output LDO with independent enable	1.91
TPS701xx	500	250	170	—	95	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5	✓	✓	✓	✓	✓	2.7	5.5	10 μF T	Dual-output LDO with sequencing	2.17
TPS702xx	500	250	170	—	95	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5	✓	✓				2.7	5.5	10 μF T	Dual-output LDO with independent enable	2.17
TPS767D3xx	1000	1000	230	—	170	3.3/2.5, 3.3/1.8	✓	2	✓	1.2	5	✓		✓			2.7	10	10 μF T	Dual-output FAST LDO with integrated SVS	2.17
<b>TPPM0110</b>	<b>1500</b>	<b>300</b>	<b>1000</b>	<b>2500</b>	<b>1000</b>	<b>3.3/1.8</b>		<b>2</b>		<b>1.8</b>	<b>3.3</b>						<b>4.7</b>	<b>5.3</b>	<b>100 μF T</b>	<b>Outputs track within 2 V</b>	<b>1.62</b>
<b>TPPM0111</b>	<b>1500</b>	<b>300</b>	<b>1000</b>	<b>2800</b>	<b>1000</b>	<b>3.3/1.5</b>		<b>2</b>		<b>1.5</b>	<b>3.3</b>						<b>4.7</b>	<b>5.3</b>	<b>100 μF T</b>	<b>Outputs track within 2 V</b>	<b>1.60</b>
TPS703xx	2000	1000	160	—	185	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5	✓	✓	✓	✓	✓	2.7	5.5	22 μF T	Dual-output LDO with sequencing	2.30
TPS704xx	2000	1000	160	—	185	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2	✓	2	✓	1.2	5	✓	✓	✓		✓	2.7	5.5	22 μF T	Dual-output LDO with independent enable	2.30

<sup>1</sup>T = Tantalum

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

*New devices are listed in red.*

## PLUG-IN POWER SOLUTIONS

Device <sup>1</sup>	Input Bus Voltage (V)	Description	P <sub>OUT</sub> or I <sub>OUT</sub>	Isolated Outputs	V <sub>O</sub> Range (V)	V <sub>O</sub> Adjustable	Price <sup>2</sup>
<b>Isolated Multiple Output</b>							
PT4820	48	35-W 48-V Input Triple Low-Voltage Isolated DC/DC Converter	35 W	Yes	1.2 to 5.0	Yes	64.83
PT4850	48	75-W 48-V Input Triple Low-Voltage Isolated DC/DC Converter	75 W	Yes	1.2 to 3.3	Yes	96.64
<b>Isolated Single Output</b>							
PT4410	48	100-W 30-A 48-V Input Isolated Programmable DC/DC Converter	100 W	Yes	1.05 to 5.7	5-bit programmable	70.20

<sup>1</sup>See [power.ti.com](http://power.ti.com) for a complete product offering.

<sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## HOT SWAP CONTROLLERS (EXTERNAL FET)

Device	Target Applications	Channels	V <sub>IN</sub> (V)	Enable/Shutdown	Power Good or UVLO Reporting	Ramp	Automatic Retry/Latch	Average Power Limiting	Price <sup>1</sup>
TPS2390	-48-V Telecom	1	-36 to -80	1H	UVLO	Current	Latch	No	1.15
TPS2391	-48-V Telecom	1	-36 to -80	1H	UVLO	Current	AutoRetry	No	1.15

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## DC/DC CONTROLLERS

Device	V <sub>IN</sub> (V)	V <sub>O</sub> (max) (V)	V <sub>O</sub> (min) (V)	V <sub>ref</sub> Tol (%)	Driver Current (A)	Output Current (A) <sup>1</sup>	Multiple Outputs	Adaptive Voltage Positioning	Protection <sup>2</sup>	Comments	Price <sup>3</sup>
<b>Performance Processor Power Supply Controllers (Synchronous Rectification)</b>											
TPS40000	2.25 to 5.5	4	0.7	1.5	1	15	No	No	OCP, UVLO	300-kHz low input sync buck, source only	0.99
TPS40001	2.25 to 5.5	4	0.7	1.5	1	15	No	No	OCP, UVLO	300-kHz low input sync buck, source/sink except SS	0.99
TPS40002	2.25 to 5.5	4	0.7	1.5	1	15	No	No	OCP, UVLO	600-kHz low input sync buck, source only	0.99
TPS40003	2.25 to 5.5	4	0.7	1.5	1	15	No	No	OCP, UVLO	600-kHz low input sync buck, source/sink except SS	0.99
<b>TPS40050</b>	<b>8 to 40</b>	<b>30</b>	<b>0.7</b>	<b>1</b>	<b>1</b>	<b>20</b>	<b>No</b>	<b>No</b>	<b>OCP, UVLO</b>	<b>Wide input range sync buck, source only</b>	<b>1.32</b>
<b>TPS40051</b>	<b>8 to 40</b>	<b>30</b>	<b>0.7</b>	<b>1</b>	<b>1</b>	<b>20</b>	<b>No</b>	<b>No</b>	<b>OCP, UVLO</b>	<b>Wide input range sync buck, source/sink</b>	<b>1.32</b>
<b>TPS40053</b>	<b>8 to 40</b>	<b>30</b>	<b>0.7</b>	<b>1</b>	<b>1</b>	<b>20</b>	<b>No</b>	<b>No</b>	<b>OCP, UVLO</b>	<b>Wide input range sync buck, source/sink except SS</b>	<b>1.32</b>
<b>TPS40060</b>	<b>10 to 55</b>	<b>40</b>	<b>0.7</b>	<b>1</b>	<b>1</b>	<b>10</b>	<b>No</b>	<b>No</b>	<b>OCP, UVLO</b>	<b>Wide input range sync buck, source only</b>	<b>1.32</b>
<b>TPS40061</b>	<b>10 to 55</b>	<b>40</b>	<b>0.7</b>	<b>1</b>	<b>1</b>	<b>10</b>	<b>No</b>	<b>No</b>	<b>OCP, UVLO</b>	<b>Wide input range sync buck, source/sink</b>	<b>1.32</b>

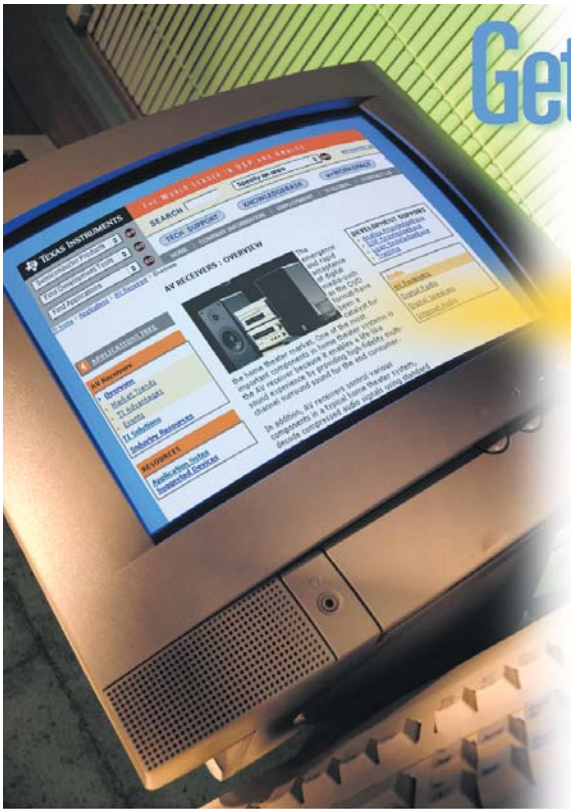
<sup>1</sup>Current levels of this magnitude and beyond can be supported.

<sup>2</sup>OCP — over-current protection; UVLO — under-voltage lockout

<sup>3</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

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