Texas Instruments

Technology for Innovators™

Communications Infrastructure Solutions Guide

Amplifiers, ASIC, Clock Distribution Circuits, Data Converters, Digital Signal Processors, Digital Up/Down Converters, Interface, Logic, Power Management

2Q 2007

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Overview

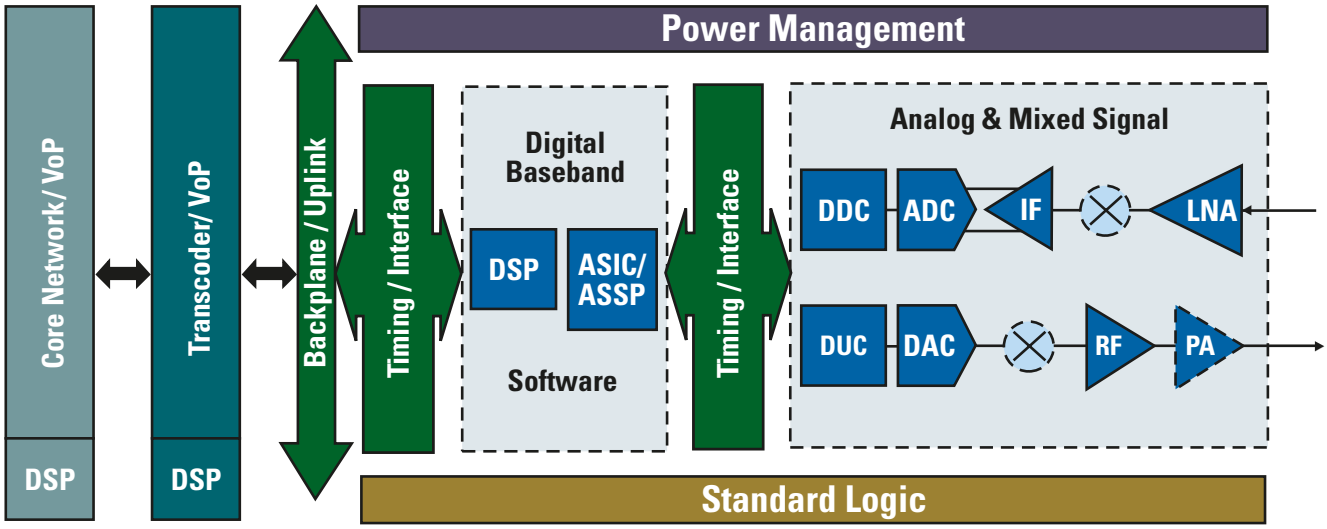
A great change is coming in communications infrastructure. For the consumer, these changes may feel like a natural transition as devices become more integrated and services become more accessible. Global consumers will have the ability to access broadband data and voice services from any device and any network—fixed or mobile—to which they are connected. Internet protocol (IP) will become the pervasive network transport technology, broadband data will become mobile and fixed mobile converged services will become available.

Service providers will leverage these changes to not only offer more services but reduce capital and operational expenditures (CAPEX/OPEX). They will demand products with new capabilities while still maintaining their service quality and reliability. In turn, equipment manufacturers want solution providers that offer system-level products with performance, flexibility and upgradeability.

Choosing the right solution provider is a critical decision. Texas Instruments (TI) takes a system-level approach to communications infrastructure. TI offers a complete portfolio of digital and analog hardware products, optimized software libraries for several air interfaces (including WCDMA, TD-SCDMA, and WiMAX™ development platforms) and evaluation modules that ease design and speed time to market. In addition, TI works with numerous third-party partners and system integrators to offer reference designs and hardware platforms.

TI is the only communications infrastructure solution provider to offer the complete signal chain—both at the board level and application level. From high-density voice media gateways and mobile-switching centers in the core of the network to small form-factor base stations, TI applies its system-level experience to assist customers with equipment architectures and configurations. TI's software libraries are carrier-class, leveraging more than 10 years of Telogy™ software VoIP experience. In fact, TI's PIQUA™ software solution is capable of, not only monitoring call quality in the network, but mitigating some problems in real time.

The *Communications Infrastructure Solutions Guide* offers a number of digital and analog products to help design engineers meet their product requirements. For more information, please go to **www.ti.com/wi**



Complete communications infrastructure system solution.

For more information about communications infrastructure, visit: www.ti.com/wi

Overview

To Know More

For detailed information about DSPs and software for carrier infrastructure:

TI brings a unique system-level perspective to the carrier infrastructure market. Leveraging its leadership in end-to-end VoIP and wireless infrastructure applications, TI aids fixed, cable and mobile service providers and equipment manufacturers to navigate the changing landscape. Targeted applications include existing network equipment, such as Class 4 and Class 5 switches, as well as media gateways in voice networks, packet gateways in broadband applications and transcoding functions in 3G wireless networks.

Service providers worldwide are actively transitioning their existing networks to support all internet-protocol (IP)-based voice, video and data services. The benefits of this transition far outweigh the costs, enabling service providers to deliver new products and services with one-third less equipment and in half the time. Equipment manufacturers will realize an effective, evolutionary path to developing systems capable of delivering multimedia/3G services while streamlining design and development resources. Additionally, consumers will benefit from greater flexibility and access to more sophisticated services, such as mobile video conferencing and video content streaming.

TI's portfolio of single- and multi-core devices are optimized to not only address these new design challenges, but to support existing network requirements. In addition, a robust portfolio of carrier-class software and world-class Telinnovation™ Echo Canceller software are also available. Finally, TI's PIQUA™ technology enables service providers to dramatically improve their quality of service and enhance the subscriber experience.

DSP with Software for Carrier-Class Voice Processing
TNETV3010

Get more information at: **www.ti.com/wi**

TI's TNETV3010 provides a flexible, carrier-grade solution with the highest density of any currently deployed voice-over-packet (VoP) carrier application. The TNETV3010 is a full-featured silicon and software solution with significant worldwide field deployment. It has six fixed-point DSP cores based on TI's TMS320C55x™ DSP. Each of these six DSP cores operates at 300 MHz and shares multiple on-chip resources.

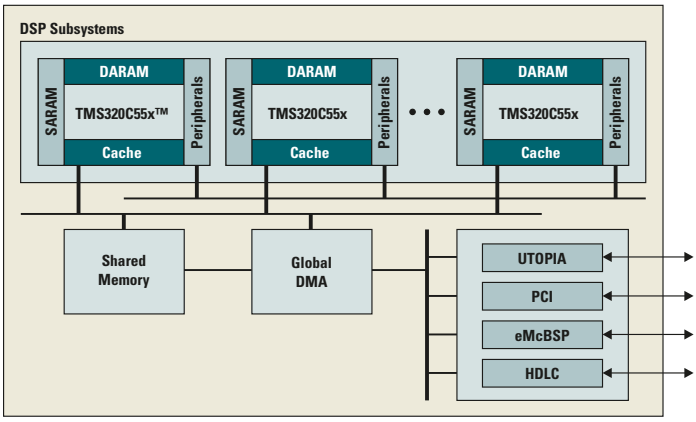
The TNETV3010 has been optimized for high-density VoP applications including VoP media gateways, echo cancellation and transcoding solutions. TI provides industry-leading software solutions including Telogy Software® for full VoP solutions, audio codecs, and the Telinnovation™ Echo Canceller. In addition, users can program their own customized solutions on the TNETV3010.

Key Features

- Fixed-mobile-convergence (FMC) software builds available
- Sufficient internal memory for VoP applications
- Field-proven Telogy Software with more than 150 million ports deployed
- Reference designs provide a complete system solution including backplane aggregation
- Single control/data plane minimizes board complexity
- Extensive voice codec suite
- Available with carrier-certified Telinnovation Echo Canceller

Applications

- VoP media gateways
- Echo cancellation
- Transcoding



TNETV3010 processor architecture.

Dual-Level Memory DSP for Multimedia Applications
TNETV3020

For more information go to: **www.ti.com/wi**

The TNETV3020 has six fixed-point DSP cores based on TI's TMS320C64x+™ DSP subsystems. Each of these cores is capable of operating at 500 MHz and shares multiple on-chip resources. These cores are supported by an internal switch-fabric architecture that accelerates on-chip data movements.

Dual-level memory architecture with extensive on-chip storage capabilities reduces chip count and bills-of-material (BOM) costs. The TNETV3020 also speeds new gateway systems to market while offering the industry's most reliable software. This software also works with TI's previous generations of infrastructure devices such as the TMS320C5x™-based TNETV3010. Users can also program their own customized solutions. TI provides industry-leading software for the TNETV3020, including Telogy Software® for full voice-over-packet (VoP) solutions, audio codecs and video codecs.

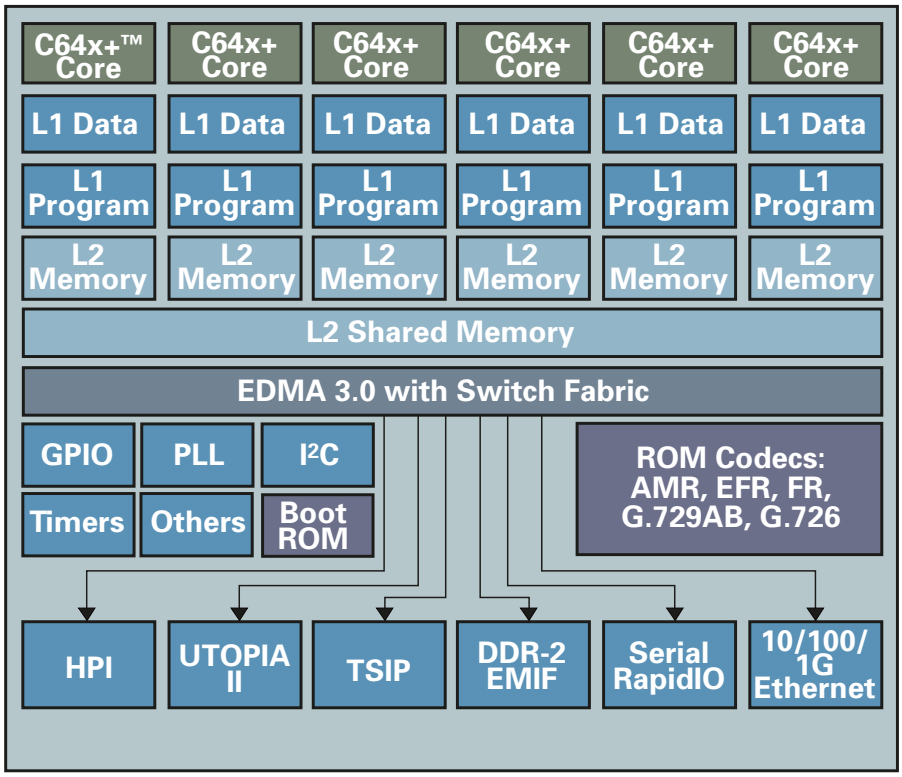
A set of critical communications interfaces, including telecom serial interface ports (TSIPs), Serial RapidIO® (SRIO), UTOPIA and Ethernet, reduces BOM and development costs by slashing component count. This decreases board layers and simplifies implementation. For more memory-intensive applications, the TNETV3020 allows the addition of external memory.

Key Features

- Six fixed-point DSP cores based on TMS320C64x+™ DSP subsystems
- 64-channel, switch-fabric enhanced direct memory access (EDMA) engine
- Shared peripherals and I/O interfaces:
  - Three 8-Mbps TSIP ports
  - DDR2 memory controller
  - Two SRIO links
  - UTOPIA ATM controller
  - Two high-speed Ethernet controllers
  - HPI, I^2C and six 64-bit, general-purpose timers
- Fixed-mobile-convergence software builds and ROM codecs
- Available with Telinnovation™ Echo Canceller
- Support for TI's PIQUA™ technology

Applications

- Advanced multimedia, high-density applications
- Fixed, cable and mobile (VoP) media gateways
- Echo cancellation solutions
- Voice or video transcoding solutions



TNETV3020 delivers 3 GHz of optimized performance.

DSP-Based Software for Echo Cancelling
Telinnovation™ Echo Canceller

Get more information at: **www.ti.com/cis**

TI's Telinnovation™ Echo Canceller is a robust, industry-standard software compatible with a variety of TI DSPs. Telinnovation provides industry-leading channel densities and unparalleled performance. This DSP-based (versus ASIC) solution allows any critical functionality problem to be solved with software while cost effectively adapting to changing network requirements.

Telinnovation Echo Canceller is G.168-2004 compliant and has been certified for use across fixed-carrier, enterprise and wireless telecommunications networks.

Convergence times for today's high-quality echo cancellers range from 150 to 300 ms. Through a patented dual-canceller algorithm, the Telinnovation Echo Canceller can converge and suppress echoes within 25 ms for ninety percent of the time. When this is not possible, the Telinnovation Echo Canceller is comparable to other carrier-class echo cancellers. This same algorithm provides superior double-talk detection.

Key Features

- Field-proven solution with more than 20 years of deployment
- Comprehensive product testing and support
- Breadth of deployment: fixed-carrier, enterprise and wireless networks
- Fast convergence
- Long-tail cancellation (up to 128 ms)
- Fast time to market

Telinnovation Specifications*

Echo Tail Length	128 ms
Industry-Standards Compliant	G.168-2004, G.169 automatic level control (ALC)
High-Level Compensation	Allows for receive-level attenuation where needed
Comfort Noise Generation	Using spectral matching
Tone Detection	Modem disable, midcall trigger (MCT), C7 bypass, C7 generate/detect/measure, C5 bypass, C5 generate/detect
Voice Quality Enhancements (VQEs) for Wireless Infrastructure Support	Adaptive noise reduction (ANR) Acoustic echo control Adaptive listener enhancement Tandem-free operation (TFO) detection A-interface detection

**Available for the following DSPs: C509/49, C5420/21/41, C5510, TNETV3010/20, C64x™ and C64x+™ DSPs*

Standards-Based VoIP Quality-Management Software
PIQUA™ Technology

Get more information at: **www.ti.com/piqua**

TI's PIQUA™ technology is a standards-based system for IP quality management that incorporates TI-developed extensions to measure VoIP performance. These extensions, along with the basic parameter set, provide enhanced statistics and diagnostic capabilities. Together these features allow for a real-time response to service degradation while providing the carrier or service provider with extensive metrics that accurately convey the user experience.

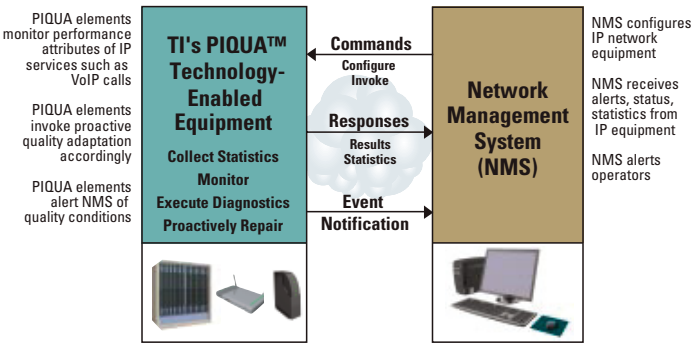
TI's PIQUA system is based on DSP technology and embedded software solutions that provide real-time monitoring and improve the quality of IP-based voice and video services. This unique quality-management tool collects data from a variety of DSP-based endpoints, including user devices, IP set-top boxes and residential and media gateways. The endpoint software encodes voice and performs the signal processing required to transmit voice between various networks.

With TI's PIQUA-embedded elements represented in more endpoints throughout the network and customer premises equipment (CPE) devices, better quality can be delivered with additional information available for monitoring and analysis. Endpoints with TI's PIQUA elements also provide a valuable resource for managing today's complex IP networks.

PIQUA software extends the quality metrics specified in many standards. These extensions have been incorporated into today's leading quality-monitoring and quality-assurance solutions.

Key Features

- Management and control of quality of service (QoS) on IP networks
- Proactive service-impairment remediation
- Real-time diagnostics based on information measured throughout IP networks
- Ability of gathered data to drive analytical tools as well as management and reporting systems
- Based on standards RTCP-XR, RTCP-HR, H.248, SIP and RTSP



TI's PIQUA technology embedded in equipment working with a network management system.

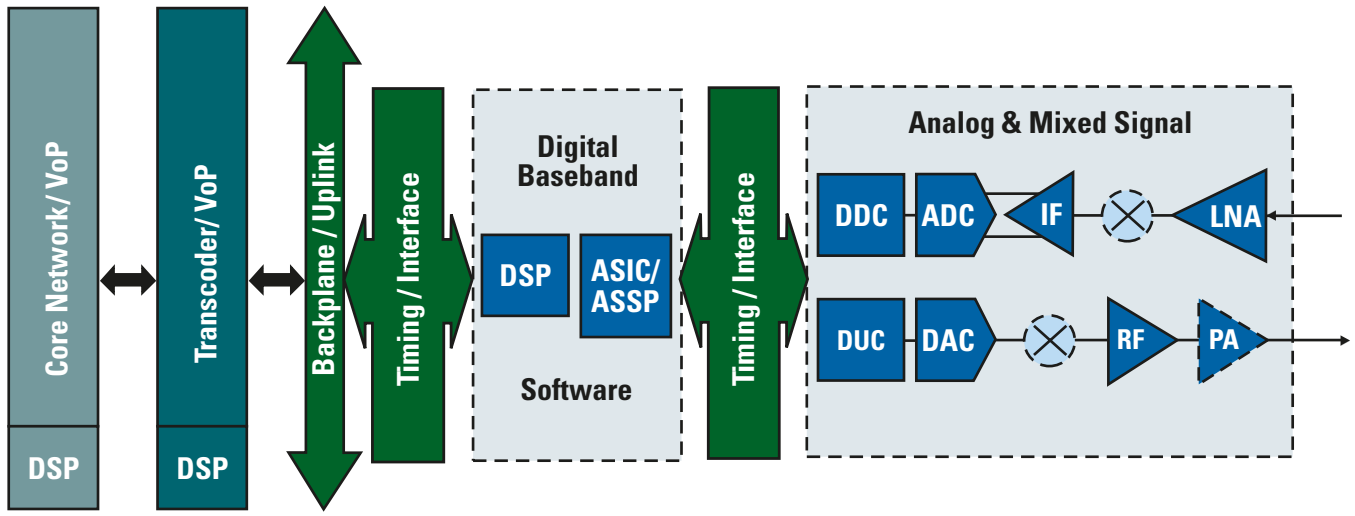
To Know More

For detailed information about wireless signal chain ICs for communications infrastructure:

The cellular network continues to evolve, growing in 2G, 2.5G and 3G deployments as well as emerging air interfaces such as 802.16d/e WiMAX, High-Speed Packet Access plus (HSPA+) and Long-Term Evolution (LTE). In addition, new form factors have been developed, ranging from in-home femto base stations to super macro base stations.

TI matches this progression through continuous innovation of high-performance, low-power, single- and multi-core digital signal processors (DSPs) and optimized software libraries targeting specific applications. These products enable OEMs to add new features and adapt to evolving wireless standards while reducing development costs and time to market.

TI's analog solutions are designed for flexibility and high levels of integration. These solutions—which include RF, data converters, digital up/down converters, interface, clocking, power management and standard logic products—provide the OEM an unparalleled portfolio of solutions spanning the complete radio signal chain.



Wireless infrastructure system signal chain.

Digital Signal Processors

High-Performance DSPs Increase Base Station System Efficiency
TMS320TCI100Q DSP

Get more information at: **www.ti.com/wi**

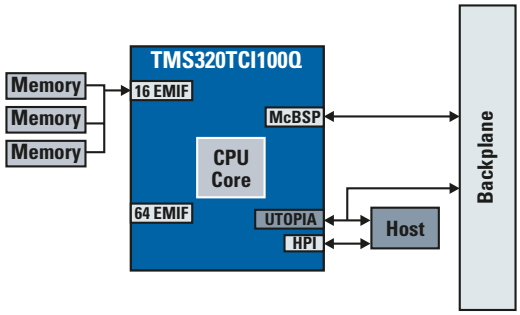
The TMS320TCI100Q DSP offers the heightened bandwidth needed to deliver wider network coverage areas, clearer signals and cutting-edge features like wireless video download and real-time video conferencing over a cellular handset. With low power per channel, this DSP is also highly beneficial for GSM/EDGE and UMTS transceiving applications as well as for transcoding/media gateway designs. Additionally, for TD-SCDMA baseband processing, this product can reduce the number of processors for a full carrier from three to two, which, when combined with device operation at less than 2 W, decreases the overall power per channel by 20%.

Key Features

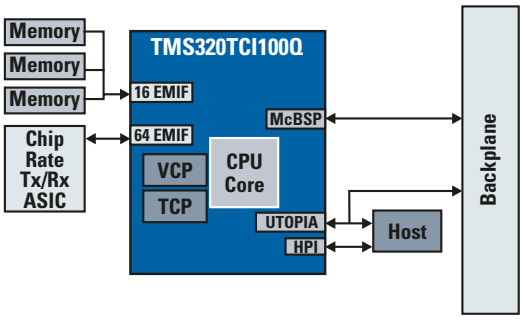
- Industry-leading 90-nm process node:
  - 850-MHz core performance
  - Power-efficient design (less than 2 W in wireless infrastructure applications)
  - High integration through state-of-the-art CMOS manufacturing process
- DSP designed for wireless infrastructure applications:
  - Integrated Viterbi (VCP) and Turbo (TCP) coprocessors
  - TCP supports more than 35 data (384-kbps) channels or seven 2-Mbps channels
  - VCP enables more than 600 voice (7.95-kbps AMR) channels
- Rich mix of robust peripherals:
  - Two high-bandwidth (up to 10 Gbps), flexible interfaces to external memory
  - Host port with glueless interface to most GPP
  - UTOPIA port for interface to communication network
  - PCI for high-performance standard local bus
- Object-code compatible with all TMS320C6000™ DSPs
- Pin-compatible with TMS320C6415, TMS320C6416 and TCI100 DSP devices

Applications

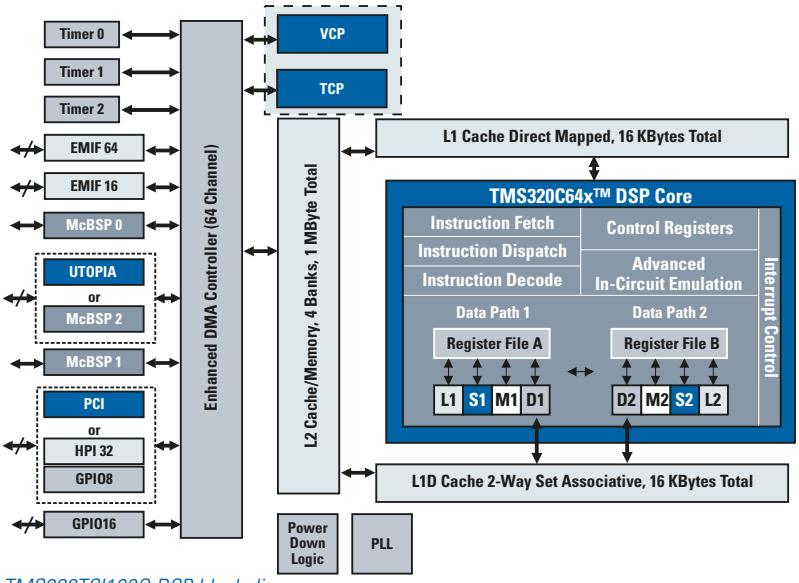
- Symbol-rate processing for 2G, 2.5G and 3G
- Assist in chip-rate processing
- Layer 2 processing in RNC



TMS320TCI100Q DSP in a voice encode and decode application.



TMS320TCI100Q DSP in symbol-rate processing for 2G, 2.5G and 3G applications.



TMS320TCI100Q DSP block diagram.

High-Performance, Low-Power, Programmable DSP
TMS320TCI6482

Get more information at: **www.ti.com/wi**

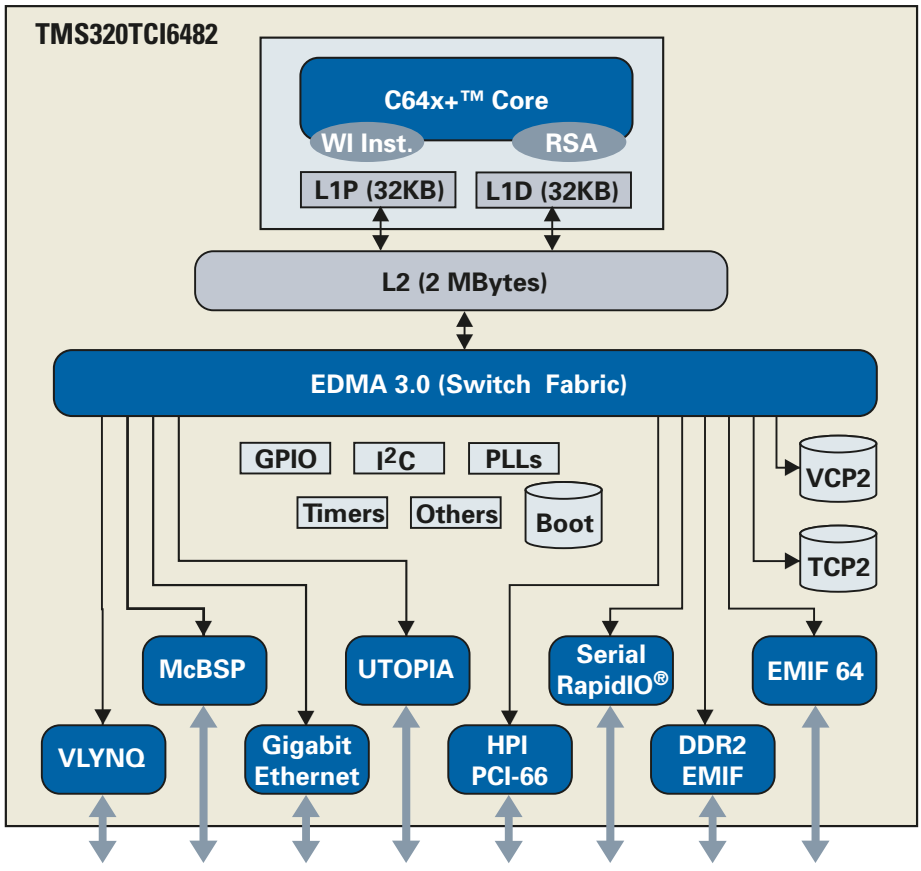
The TMS320TCI6482 DSP device is a high-performance, low-power, easy-to-program DSP optimized for the wireless infrastructure (WI) market. This device is a result of continued innovation on TI's DSP architecture, significant process improvements and a system-level focus on WI applications. With designs based on the TCI6482 DSP, wireless-equipment makers can use a single hardware platform for different applications, saving development time and costs in new designs, as well as upgrading existing products quickly and efficiently.

Key Features

- High-performance DSP TMS320C64x+™ architecture:
  - 1-GHz TMS320C64x DSP core
  - 28 new WI instructions to improve symbol and chip rate processing
  - New complex multiply (CMPY) instructions to improve chip and symbol rate performance
  - New WI DSP instructions for packing, sorting and bit manipulation
  - New Rake, RACH, Search and Spread Assist instruction set extension for complex correlation functions in CDMA base standards
- Power efficient (~3 W) for more on-board functionality in WI applications
- High-performance memory subsystems:
  - 2 Mbytes of L2 memory/32 Kbytes of L1D and L1P memory
  - Double data rate 2 (DDR2) external memory interface
- Second-generation Viterbi (VCP2) and Turbo (TCP2) decoder coprocessors to significantly speed up channel decoding operations
- Seamless, modular and scalable system-level connectivity:
  - Four 1x serial RapidIO® interfaces (12.5-Gbps maximum performance throughput) with low latency and peer-to-peer communications for both data and control planes
  - Integrated 10/100/1000 Ethernet MAC allows glueless network and system connectivity
  - Legacy interfaces UTOPIA, HPI, PCI and McBSP to ease migration
- Industry-leading 90-nm process technology
- Software compatible with existing C64x™ WI software
- Supports software implementation of worldwide wireless standards such as TD-SCDMA, 802.16 (WiMAX™), UMTS (including HSDPA), GSM and CDMA2000®

Applications

- Macro, micro and pico base stations
- MAC-HS



TMS320TCI6482 block diagram.

Digital Signal Processors

High-Performance, Multicore, Programmable DSPs
TMS320TCI6487, TMS320TCI6488

Get more information at: **www.ti.com/wi**

The TMS320TCI6488 is a high-performance DSP targeted specifically for WCDMA wireless infrastructure baseband applications. With high functional integration and high channel density supported on a single device, the TCI6488 DSP offers a modular and scalable design with a small footprint. Its functional integration provides lower system cost and eliminates the need for accelerator ASICs.

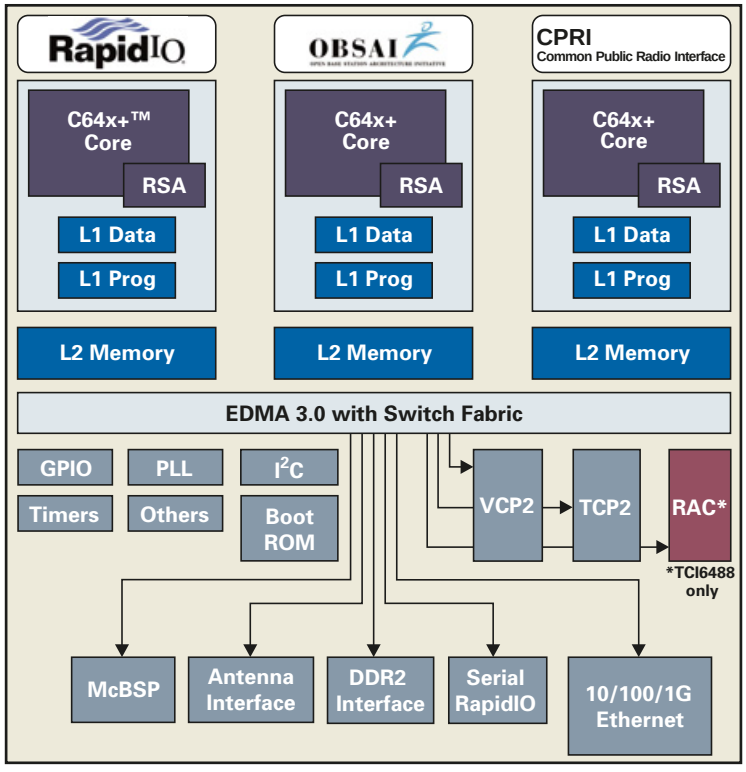
The TCI6488 DSP is an ideal solution for pico, micro and macro BTS and enables a system-on-chip (SoC) baseband solution for WCDMA Tx and Rx applications. The TCI6488 DSP offers a software-programmable solution and allows for the reuse of existing C64x™ and C64x+™ DSP code.

RSA instruction-set extensions are available on all three DSP cores and enable high-performance Rake, Rach Search and Spread Assist.

In the same ways, the TMS320TCI6487 is a highly versatile DSP targeted for the TD-SCDMA, WiMAX and CDMA2000® wireless infrastructure baseband market. Advanced features such as MIMO, beamforming and PIC can be easily supported without the need for any hardware redesign.

Key Features

- Three cores at 1 GHz each
- Total of 3 MB on-chip L2 SRAM/cache
- Standard C64x+ DSP core
- Dedicated receiver accelerator coprocessor (RAC)—TCI6488 only
- Second-generation Viterbi (VCP2) and Turbo (TCP2) decoder coprocessors
- Chip-rate Rx functions (preamble detect, path search and finger despread)
- Industry-leading 65-nm silicon technology
- Scalable platform with modular design for pico, micro and macro BTS
- Software-programmable resources for reuse of MIPS and memory resources
- Standard interfaces for SGMII Gigabit Ethernet, DDR2, two serial RapidIO® (SRIO) links, McBSP, I^2C, GPIO
- Antenna interfaces (6 links):
  - CPRI: 614.4-Mbps, 1.2288-Gbps and 2.4576-Gbps link rates
  - OBSAI: 768-Mbps, 1.536-Gbps and 3.072-Gbps link rates
- Other interfaces:
  - 10/100/1000 Ethernet (SGMII) interdevice communication
  - SRIO: Two 1x lanes at rates of 1.25, 2.5 or 3.125 Gbps each
  - McBSP: Two McBSP links, each at 100 Mbps
  - I^2C: One I^2C link at 400 kbps
  - DDR2-667 support



TMS320TCI6487/8 block diagram.

WiMAX Forum® 802.16e Wave 1, Baseband-Processing Software Library

Targeted for TMS320TCI6482

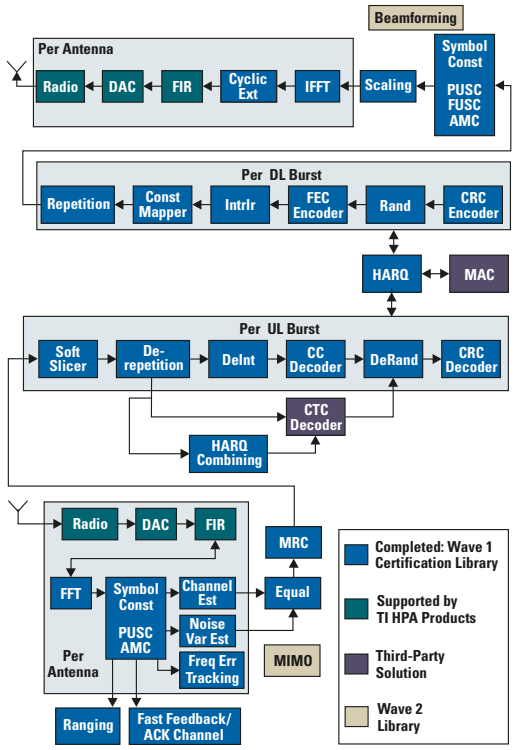
Get more information at: **www.ti.com/wi**

The WiMAX Forum® Wave 1 Certification software library, combined with the TMS320TCI6482 high-performance DSP, provides an ideal start for any 802.16e base-station design. The WiMAX™ software library is an optimized set of functions covering all the basic signal-processing elements needed to build a baseband solution compliant with Wave 1. Using this library, design teams can focus on differentiating features without sacrificing quality or optimal functionality of the baseband processing software.

TI's extensive suite of software development tools, including Code Composer Studio™ integrated development environment, allows rapid integration of the WiMAX library into a complete system.

Key Features

- Complete set of optimized software components for Wave 1 Certification requirements
- Extensive documentation including simulated performance results for receiver functions
- Library supporting TI's 1-GHz TMS320TCI6482 and TMS320TCI6487 DSPs
- Complete demo system available: uses advanced mezzanine cards and includes MAC processing and mobile simulator
- Wave 2 support available in 3Q 2007



WiMAX library block diagram.

WCDMA Baseband-Processing Software Libraries

Targeted for TMS320TCI648x

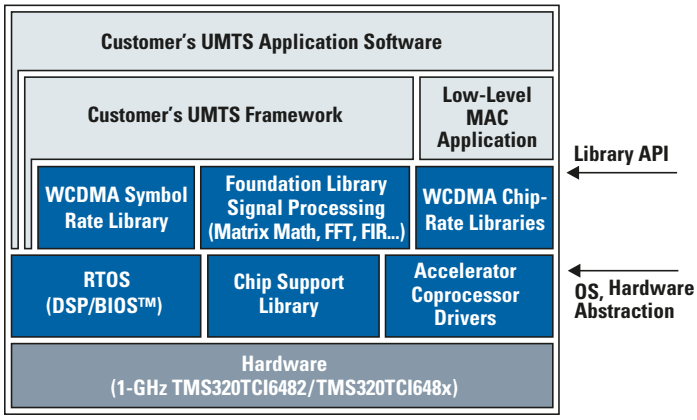
Get more information at: **www.ti.com/wi**

TI's WCDMA software libraries, combined with TI's TMS320TCI648x high-performance DSPs, provide an ideal start for any WCDMA base-station design. The WCDMA software library is an optimized set of functions covering basic elements for implementing both chip-rate and symbol-rate processing. In addition, the software makes use of resident coprocessors on the DSPs to further enhance processing power on the system. Using these libraries, design teams can focus on differentiating features without sacrificing quality or the optimal functionality of the baseband-processing software. The WCDMA libraries cover requirements through the 3GPP Release 6 international standard.

In addition, TI's extensive suite of software development tools, including Code Composer Studio™ integrated development environment, allows rapid integration of the WCDMA libraries into a complete system.

Key Features

- Supports a complete system on a chip for up to 48 users (when used with TMS320TCI6488 DSP)
- Designed to support TI's 1-GHz TMS320TCI6482 and TMS320TCI6487/8 DSPs
- Optimized software components for WCDMA Release 6 symbol-rate processing
- Viterbi (VCD) and Turbo (TCP) decoding using hardware coprocessors on DSP
- Chip-rate processing using hardware coprocessors on DSP
- Complete transmit chip-rate application
- Receiver functions abstract powerful chip-rate despreading hardware engine on the TCI6488
- Rigorous testing and customer support developed using practices compliant with ISO9001



TI software system view for TCI648x, OS and hardware abstraction layer provided and supported by Texas Instruments.

Digital Signal Processors

32-Bit DSP Controller Handles up to 16 DC/DC Channels
TMS320F28044

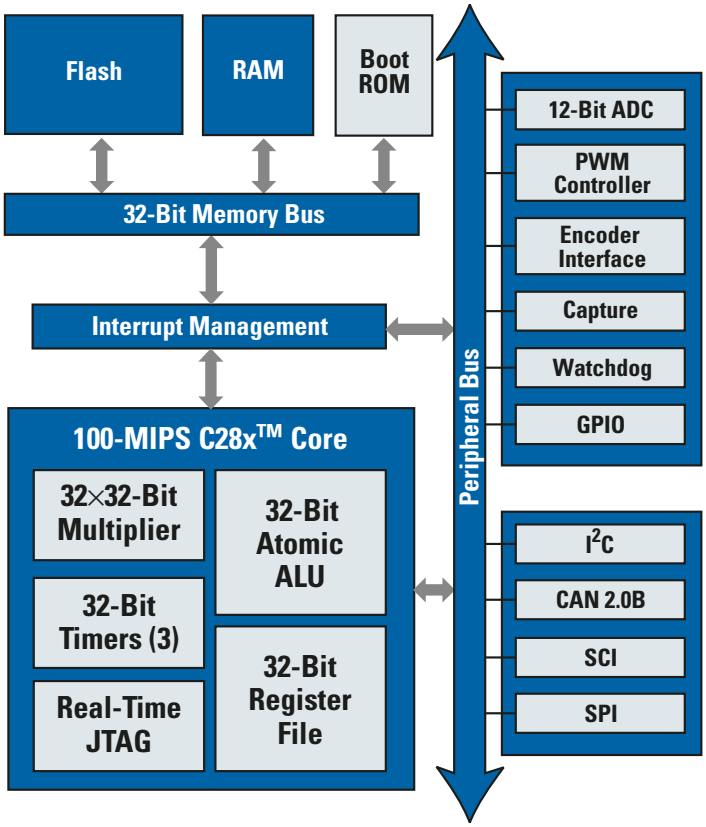
Get more information at: **www.ti.com/f28044**

Allowing designers to transition to software-controlled, digital power management, the F28044 controller is targeted at multi-channel point-of-load (POL) applications such as telecommunications and networking infrastructure equipment, servers, laptop computers and industrial equipment. The F28044 controller is the industry's only device to offer full digital loop control of up to 16 DC/DC converter channels. It can handle multiple outputs, phases, sequencing, margining and soft-start capabilities—as well as system management and communications. The device starts at $5 in volume.

Key Features
- 32-bit DSP core
  - 100-MIPS performance
  - Single-cycle 32 x 32 MAC
  - Ultra-fast interrupt response
- Memory
  - Flash: 128 KB
  - RAM: 20 KB
- High-resolution PWM
  - Sixteen independent PWM channels
  - Resolution capabilities of ~150ps (12+ bits @ 1 MHz)
  - Duty cycle, sequencing and multiple phase shift and compensation
  - Easy event synchronization with on-chip ADC
- ADC
  - High-speed throughput (up to 80 ns/12.5 MSPS)
  - 16-channel, 2 sample-hold, 12-bit resolution
  - Zero wait state results

Tools
1) Digital power supply software
- Free software frameworks and application examples of AC/DC, point-of-load and DC/AC
- Translates engineers' analog experience to digital control
- More information at **www.ti.com/dpslib**

2) Digital power hardware
- Two digital power adapter boards available from Tier Electronics at **www.tierelectronics.com**
- Two-phase boost PFC
- Dual phase-shifted full-bridge
- Easily interfaces to TI's F28044 or F2808 eZdsp™ development kit for initial prototyping and experimentation with digital power



TMS320F280x digital signal controllers.

ASIC Solutions Enable Next-Generation Wireless Infrastructure

ASIC

Get more information at: **www.ti.com/asic**

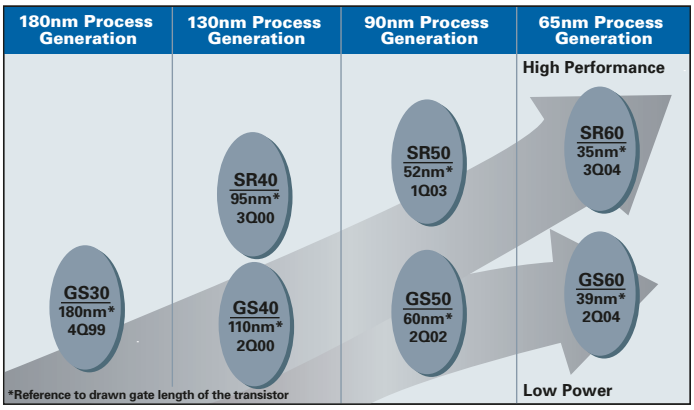
TI's dedicated, worldwide ASIC team builds flexible product platforms enabling customers to deliver differentiated wireless infrastructure (WI) solutions. TI ASIC's in-depth silicon expertise, deep circuit design knowledge and close collaboration with customers have resulted in ASIC platforms addressing system requirements from a performance, power and density perspective. By combining our 90- and 130-nm ASIC platforms with one of the richest portfolios of embeddable IP, TI is taking system-on-chip (SoC) development from the drawing board to reality in customers' products.

Key Features

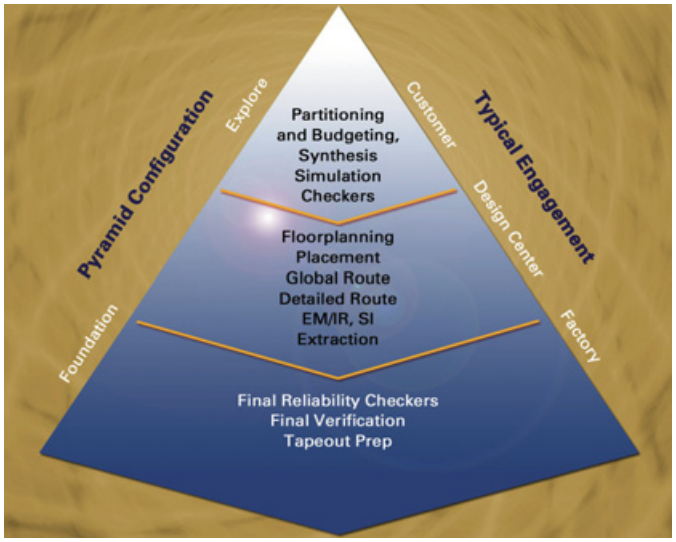
- Global leadership in semiconductor manufacturing:
  - Leading-edge 130- and 90-nm CMOS process technologies
  - High-performance and density-optimized ASIC libraries, I/O and memory for varying WI ASIC needs; can be mixed on chip for best total solution
- Extensive SoC and large-design expertise:
  - Robust IP portfolio:
    - DSP, microprocessor cores (ARM®, MIPs)
    - Broad array of peripheral IP
    - Advanced, silicon proven gigabit SerDes technology leadership
    - Experienced SysApps team for broad-based support in silicon, package and system-level integration
  - Complete range of low-cost and high-performance packages
- Comprehensive ASIC cells and tool support:
  - Robust module library/rich core library
  - Broad portfolio of memory compilers based on industry-leading SRAM-bit cell densities and performance
  - Open, comprehensive design flow based on industry-standard, third-party CAD/CAE tools
- Experienced, flexible and global design services:
  - Worldwide design center staff
  - Experienced WI applications team for system-level support
  - Collaborative design, traditional floor planning, place and route

Applications

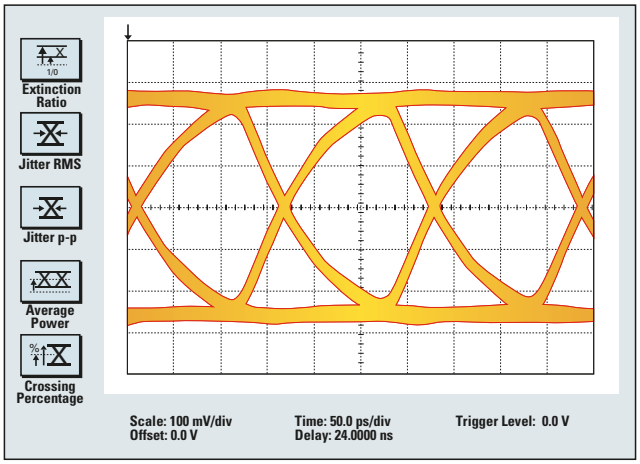
- Application-specific digital up/down converter
- Baseband processing:
  - Chip-rate and symbol-rate processing
  - Combining/decombining/bridge chips
- Specialized applications:
  - Viterbi/Turbo decoding
  - Switching matrix
- Network control and interface processing:
  - Base station uplink
  - RNC control and protocol processor
- Embedded processor SoC designs



TI roadmap of ASIC libraries.



Open design flow delivers flexibility and ease of use.



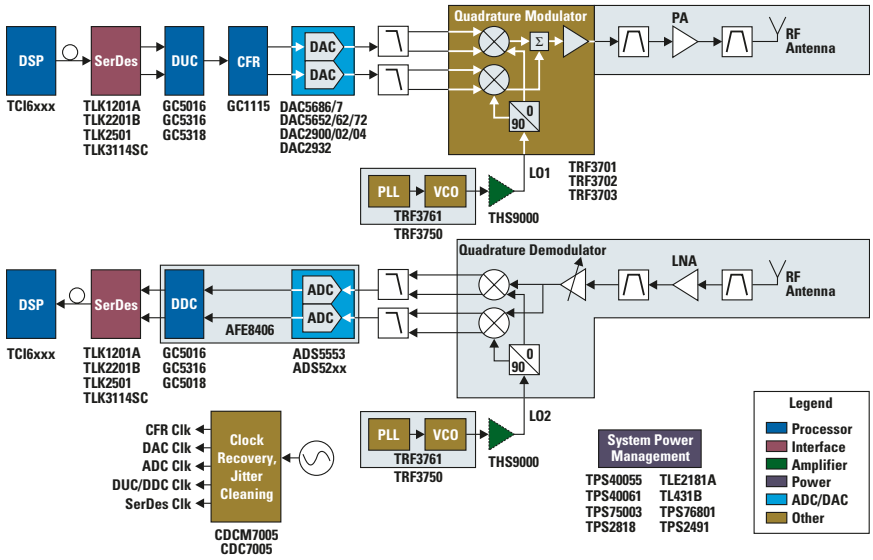
TI waveform 90-nm, SONET-compliant SerDes interface running at 6.25 GSPS.

Wireless Infrastructure Architectures

In this section, four typical signal-chain architectures adopted in wireless infrastructures are discussed: direct-up conversion radio, single-IF heterodyne Tx/Rx with digital up/down conversion, multi-carrier radio PA linearization with direct-up conversion, and high-performance WiMAX™ (2.5- and 3.5-GHz BTS). Each of these architectures has its own benefits and trade-offs. In each diagram, suggested TI devices are listed under each block.

Direct-Up (Zero-IF) Conversion Radio

The digital up-conversion (DUC) process includes pulse shaping and interpolation. Crest-factor reduction (CFR) selectively reduces the peak-to-average ratio (PAR) of the wideband digital signals. A DAC then converts digital I/Q data into analog signals that are sent through low-pass filters to remove multiple images of the DAC clock. The quadrature modulator up converts the I/Q analog signals directly to RF. Integrated monolithic PLL/VCO devices can be used to generate the local-oscillator (LO) frequencies required by the quadrature modulator.



Benefits

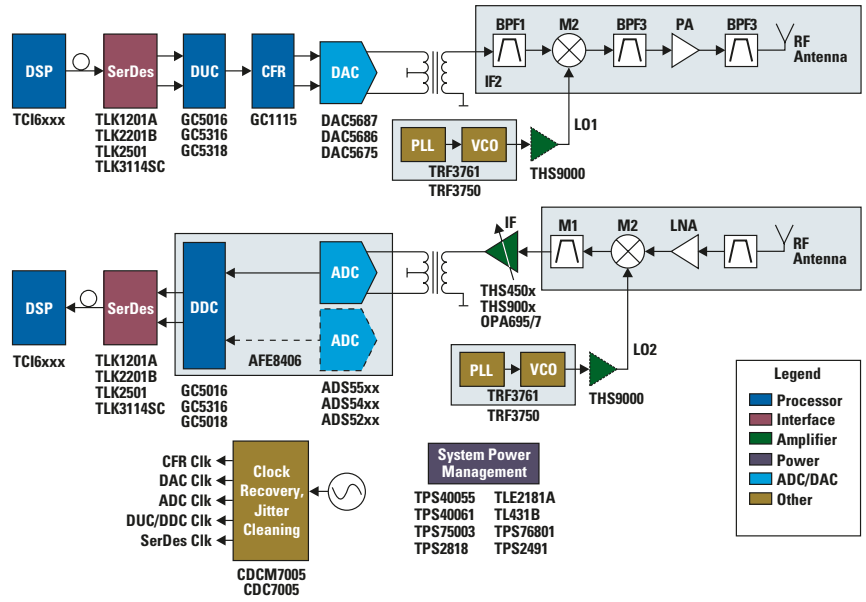
- Direct-up conversion saves RF bills of material (BOM)
- Provides low-cost system

Trade-offs

- Quadrature modulator I/Q imbalance
- I/Q channel gain mismatching, offset
- Noise performance

Single-IF Heterodyne Tx/Rx with Digital Up/Down Conversion

In the single-IF configuration, a digital up converter (DUC)/digital down converter (DDC) replaces the IF analog modulator/demodulator, which means no local-oscillator (LO)/carrier self-mixing at IF obtains perfect gain/phase matching. Carrier or channel selection can be implemented in the digital domain (DUC/DDC). Instead of a low-frequency baseband signal, the single-channel ADC/DAC receives or transmits an intermediate frequency (IF). The IF is defined by the frequency of the digital sine and cosine generator, which is a numerically controlled oscillator (NCO). The IF signal is up/down converted to/from RF through one analog mixing stage, reducing the RF bills of material (BOM). The IF frequency is usually in the 70- to 200-MHz range.



Benefits

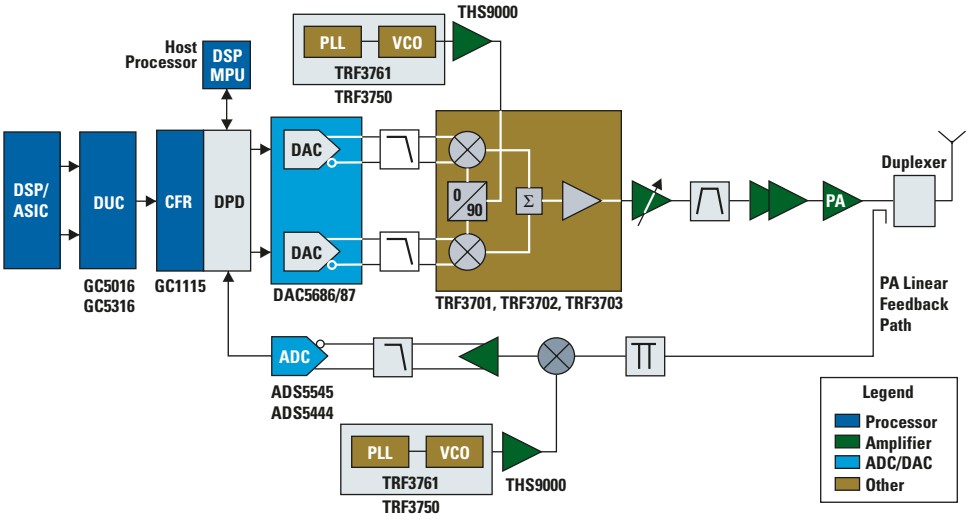
- No LO/carrier self-mixing at IF, perfect gain/phase matching, no offset
- High IF relaxes RF front-end image rejection filter requirement
- Reduces RF BOM

Trade-offs

- High IF requires a wideband data converter, but ADC/DAC performance at such a high IF range limits the performance of such architecture
- Carrier/channel selection can be implemented in the digital domain (DUC/DDC) but requires a high-speed ADC/DAC

Multi-Carrier Radio PA Linearization with Direct-Up Conversion

Power amplifiers (PAs) are one of the most expensive and power-consuming components in 3G base stations. They are inherently non-linear and, when operated near saturation, cause intermodulation that interferes with adjacent channels. Digital predistortion (DPD) uses feedback to measure the nonlinear behavior of the PAs and predistorts the signal to compensate for the nonlinear behavior of PAs near saturation, thus extending the linearity range of PAs.



Benefits

- Both DPD and crest-factor reduction (CFR) technology significantly lower PA requirements
- Overall system cost is greatly reduced

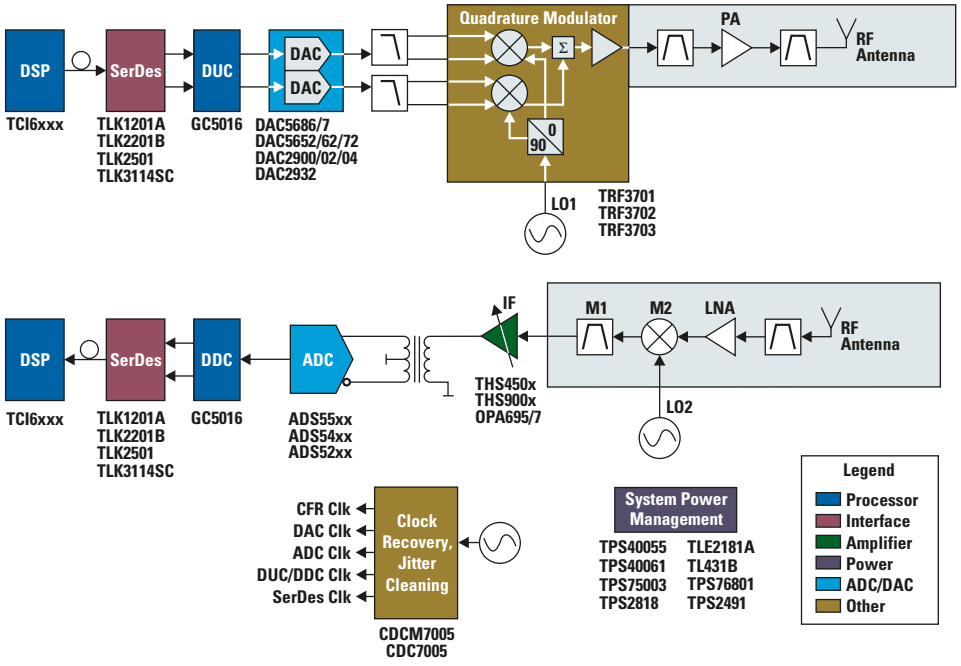
Trade-offs

- More demanding on signal processing capability

High-Performance WiMAX™ (2.5- and 3.5-GHz BTS)

Baseband data is interpolated and filtered in the digital up converter (DUC), which presents parallel I/Q data to the dual DAC. The DAC provides high-speed conversion of the I/Q data along with phase, gain and offset correction of the I/Q imbalance. With a complex baseband input, an interpolating DAC can be used to increase the effective data rate through interpolation.

The I/Q modulator is capable of performing at frequencies from 0.4 to 4 GHz and is therefore suitable for the popular WiMAX frequency bands. The receive chain down-converts RF to IF through one analog mixing stage. The ADC converts the IF to a combined I/Q for the digital down converter (DDC), which provides digital down conversion and carrier/channel selection.



Benefits

- Direct-up-conversion architecture reduces RF bills of material (BOM)
- Supports a wide range of RF frequency bands
- Nonharmonic clock-related spurious signals fall out of band

Trade-offs

- Quadrature modulator I/Q imbalance
- I/Q channel gain mismatching, offset
- Noise performance

Transceiver Signal Chain

High-Density Digital Up/Down Converter
GC5316, GC5318

Get samples, datasheets and evaluation modules at:
www.ti.com/sc/device/GC5316 and **www.ti.com/sc/device/GC5318**

The GC5316 is a high-density, multichannel communications signal processor that provides both digital down conversion and digital up conversion for cellular base-transceiver systems. The device supports both UMTS and CDMA2000® (CDMA) air-interface cellular standards.

The chip provides up to 24 CDMA digital-down-converter (DDC) and digital-up-converter (DUC) channels or 12 UMTS DDC and DUC channels. The GC5316 can also support a combination of CDMA and UMTS channels. The DDC and DUC channels are independent and operate simultaneously.

The chip is ideal for cellular base-transceiver systems requiring a large number of digital radio channels.

Each of the 24 CDMA (or 12 UMTS) channels can operate independently. On the DDC side, four 16-bit input ports can accept real or complex input data. The input ports are driven with parallel data, typically from an A/D converter. Each down-converter channel can be programmed to accept data from any one of the four input ports.

On the DUC side (GC5318), there are four 18-bit output ports. Each output port can sum any of the DUC channels in a daisy-chain fashion, which can create a stack of CDMA or UMTS signals. These ports can output either real or complex data.

Key Features
- Clock rates up to 125 MSPS
- Optimized for CDMA2000-1X and UMTS systems
- Up to 12 UMTS or 24 CDMA up/down-converter channels
- Mixed CDMA2000-1X and UMTS operation
- Any DDC can connect to any of four input ports
- Any DUC can sum into any of four output ports
- Real/complex DDC inputs and DUC outputs
- Programmable AGC on DDC outputs
- Rx filtering: 6-stage CIC, 48-tap CFIR, 64-tap PFIR
- Tx filtering: 6-stage CIC, 47-tap CFIR, 63-tap PFIR
- 115-dB SFDR
- 16-bit DDC inputs, 18-bit DUC outputs
- 1.5-V core, 3.3-V I/O
- Packaging: 388-ball, 27-mm PBGA, 1-mm pitch

Applications
- High-density wireless base-station receiver and transmitter (wideband, multicarrier)
- WCDMA, CDMA2000, TD-SCDMA
- Software radio
- Wireless local loop
- Intelligent antenna systems

Four-Channel Wideband Up/Down Converter
GC5016

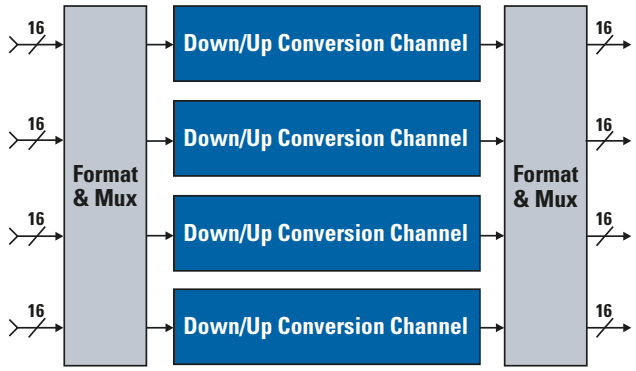
Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/GC5016

The GC5016 is a flexible, wideband, four-channel digital up/down converter. The four identical processing channels can be independently configured for up conversion, down conversion or a combination of two up-conversion and two down-conversion channels.

The device accepts various types of input formats and can output each channel on a separate port, or two or more channels can be summed on a common port.

Key Features
- Flexible input and output options allow seamless connections with TI ADCs and DACs
- Channel flexibility and filtering allows the use in very wideband repeater applications (greater than 30 MHz)
- Efficient resource usage allows for low-delay application
- Four independently configurable wideband down-converter or up-converter channels
- Rates to 160 MSPS for four channels, 320 MSPS for two channels in double-rate mode
- Four wideband channels support UMTS and WiMAX applications
- FIR filter block providing up to 256 taps per channel
- Variable input and output options
- JTAG boundary scan
- 3.3-V I/O, 1.8-V core
- Power dissipation: <1 W for four channels
- Packaging: 252-ball, 17-mm PBGA, 1-mm pitch

Applications
- Cellular base-transceiver-station transmit and receive channels
- WCDMA, CDMA2000®, WiMAX, WiBRO, LTE standards supported
- Radar
- General filtering
- Test and measurement equipment
- Low-power applications
- Single- and multi-carrier repeaters



GC5016 internal block diagram.

Eight-Channel, Wideband Digital Down Converter GC5018

Get samples, datasheets and evaluation modules at:

www.ti.com/sc/device/GC5018

The GC5018 provides up to 8 UMTS, 16 CDMA or 16 TD-SCDMA digital down-converter (DDC) channels. The DDC channels are independent and operate simultaneously.

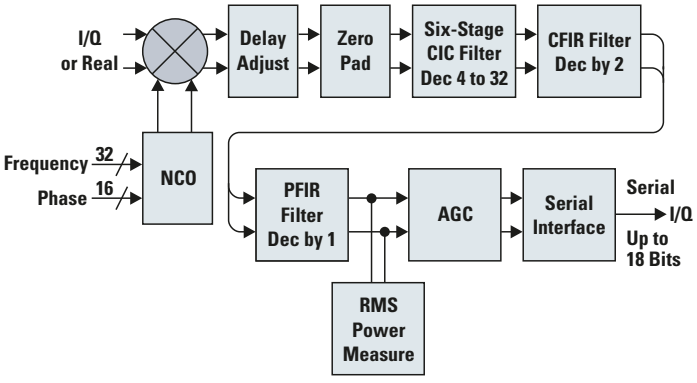
The GC5018 has four 16-bit inputs. Each DDC channel can be programmed to accept data from any one of the four input ports (or two for complex input mode).

Key Features

- Clock rates up to 160 MSPS
- Four 16-bit CMOS ADC input ports
- 8 UMTS, 16 CDMA or 16 TD-SCDMA DDC channels with programmable 18-bit filter coefficients:
  - Real or complex DDC inputs
  - 115-dB SFDR NCO
  - Rx filtering: 6-stage CIC (m = 1 or 2), up to 48-tap CFIR, up to 64-tap PFIR
  - Power-measurement unit
  - Digital AGC
- Programmable closed-loop VGA control with 6-bit outputs for each ADC input port
- 3.3-V I/O, 1.5-V core
- Power dissipation: ~2.5 W max
- Packaging: 305-ball, 19-mm PBGA, 1-mm pitch

Applications

- Wireless base-station receiver (wideband, multicarrier)
- WCDMA, CDMA2000®, TD-SCDMA
- Software radio
- Wireless local loop
- Intelligent antenna systems



GC5018 DDC module detail.

Integer-N PLL with Integrated VCO TRF3761

Get samples, datasheets and application reports at:

www.ti.com/sc/device/PARTnumber

(Replace **PARTnumber** with **TRF3761-A**, **TRF3761-B**, **TRF3761-C**, **TRF3761-D**, **TRF3761-E**, **TRF3761-F**, **TRF3761-G**, **TRF3761-H**, **TRF3761-J** or **TRF3761-K**)

The TRF3761 is a family of high-performance, highly integrated frequency synthesizers optimized for wireless infrastructure applications. The TRF3761 includes a low-noise voltage-controlled oscillator (VCO) and an integer-N PLL. It integrates division options of /2 or /4 for a more flexible output frequency range. It is controlled through a three-wire serial peripheral interface (SPI). It can be powered down when not in use by the SPI or external pin.

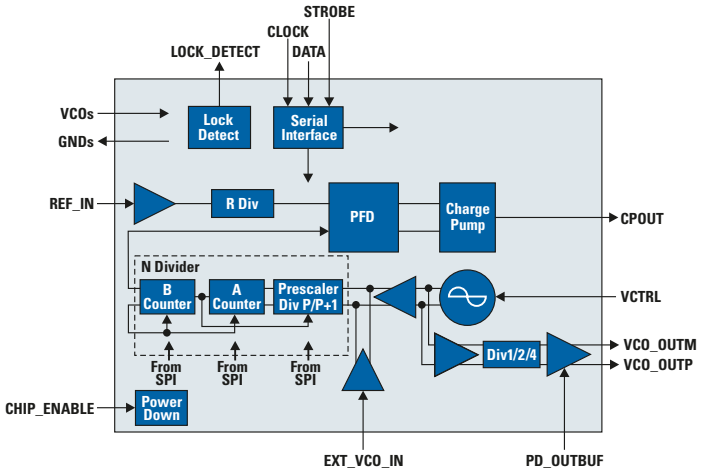
Alternatively, the TRF3750 integer-N PLL frequency synthesizer device can be used in conjunction with an external VCO to implement a local-oscillator (LO) function.

Key Features

- Fully integrated VCO
- Low phase noise: –138 dBc/Hz (at 600 kHz, f_{VCO} of 1.9 GHz)
- Low noise floor: –160 dBc/Hz at 10-MHz offset
- Integer-N PLL
- Input reference frequency range: 10 to 104 MHz
- VCO frequency output divided by 1, 2 or 4
- Output buffer enable pin
- Programmable charge-pump current
- Hardware and software power down
- Three-wire serial interface
- Single supply: 4.5- to 5.25-V operation
- Silicon germanium technology

Applications

- Wireless infrastructure for WCDMA, CDMA and GSM



TRF3761 functional diagram.

Transceiver Signal Chain

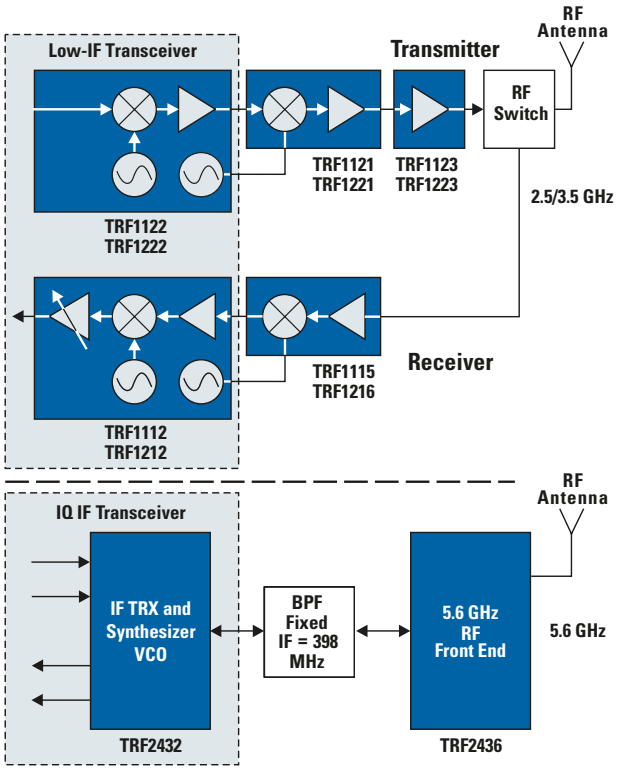
RF Transceiver Chipset Solutions for WiMAX™ Applications
TSW5002, TSW5003, TSW5005

Get more information at: **www.ti.com/tsw5002evm,** **www.ti.com/tsw5003evm** or **www.ti.com/tsw5005evm**

The TRF500x reference designs represent complete design implementations of the TRF11xx/12xx/24xx family of RF front-end solutions for the 2.5/3.5/5.6-GHz WiMAX™ wavebands, respectively. The chipsets have low device counts and offer flexible interface options to implement either low-IF or IQ baseband architecture solutions.

Key Features
- Complete RF reference designs for 2.5/3.5/5.6-GHz wavebands
- Fully compliant with IEEE 802.16d/e
- Supports broadband wireless applications such as WiMAX and WiBro
- Front-end chipsets offer highly integrated, compact RF solutions
- Optimized bill of materials lowers overall system costs

Applications
- Wireless base stations and access points
- Customer premise equipment (CPE)
- Wireless backhaul
- Point-to-point microwave
- Safety band



WiMAX™: 2.5/3.5/5.6-GHz chipset solutions.

High-Performance, Low-Noise, 0.4- to 4-GHz Quadrature Modulator
TRF3703

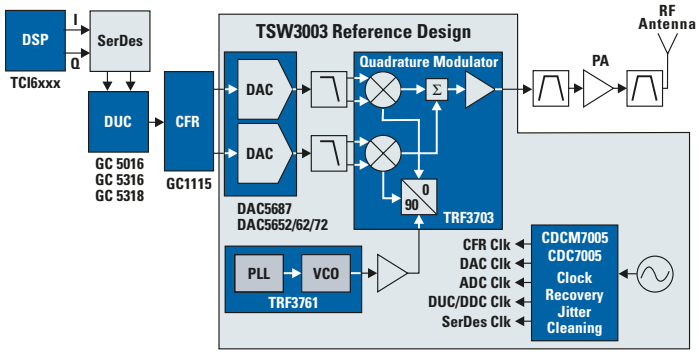
Get samples, datasheets and evaluation modules at:
www.ti.com/sc/device/TRF370315 or **www.ti.com/sc/device/TRF370333**

The TRF3703 is a best-in-class, low-noise, direct quadrature modulator capable of converting complex modulated signals from baseband or IF directly up to RF. It is ideal for high-performance, direct RF modulation from 400 MHz up to 4 GHz. The low noise floor and high linearity eliminate the need for additional filtering and cut down on heat dissipation. The device's wide operating frequency range supports different air-interface standards and is ideal for direct-up conversion.

Together with TI's DAC56x2 family, the TRF370315 provides a cost-effective, direct-up conversion transmitter for GSM. With seamless interface to TI's DAC5687, the TRF3703 provides a universal transmitter platform for WCDMA, TD-SCDMA, CDMA2000®, WiMAX™ or WiBro transmit signals for signal bandwidths up to 350 MHz.

Key Features
- –75-dBc, single-carrier, WCDMA adjacent-channel power ratio (ACPR) at –11-dBm channel power
- Common-mode inputs of –1.5 V and 3.3 V support different types of DAC output
- Noise floor: –163 dBm/Hz
- Linearity: 23-dBm, third-order output intercept point (OIP_3)
- Output compression (P1dB): 9 dB
- Unadjusted carrier leakage: –40 dBm (at 2 GHz)
- Unadjusted sideband suppression: –40 dBc (at 2 GHz)
- Accepts input signals ranging from 0 (dc) to 350 MHz
- RF output modulation: 0.4 to 4 GHz

Applications
- Cellular base station: UMTS, TD-SCDMA, CDMA2000, GSM, EDGE, UWC-136, IS-95, TDMA
- WiMAX 802.16d/e, WiBro
- Wireless local loop
- Wireless metropolitan-area network (MAN)



The TRF3703 in a direct-up conversion transmitter.

16-Bit, 500-MSPS, Dual DAC with Interpolation
DAC5687

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/DAC5687

The DAC5687 is a dual-channel, 16-bit, 500-MSPS DAC that delivers best-in-class linearity, plus low noise and crosstalk. The device has multiple integrated, digital-processing function blocks and interpolation filters (2x, 4x and 8x) that allow higher-output IF at relatively low input rates. It also eases the output filter's requirement for image rejection.

The combination of a 32-bit numerically controlled oscillator (NCO) fine mixer with a coarse mixer of $f_s/4$ and $f_s/2$ allows for a wider range of frequencies with fine resolution, providing more flexibility for frequency planning. The IQ-compensation feature allows optimized phase, gain and offset to maximize sideband rejection and minimize LO feedthrough for better direct-up (or zero-IF) conversion. The on-chip PLL delivers very low phase noise to enable clock multiplication for interpolation.

The DAC5687 has multiple operation and input/output modes to provide the highest flexibility for base-station design. Together with TI's second-generation IQ modulator (TRF3703) and integrated-PLL and VCO-frequency synthesizer (TRF3761), the TSW3003 reference design is the best universal transmitter platform for base stations with WCDMA, CDMA2000®, TD-SCDMA or WiMAX™ that operate from 0.4 to 4 GHz with signal bandwidths up to 200 MHz.

Key Features
- Integrated 2x, 4x and 8x interpolation filters
- I/Q compensation including offset, gain and phase
- Complex 32-bit NCO fine mixer
- Fixed-frequency mixer with $f_s/4$ or $f_s/2$
- On-chip PLL/VCO clock multiplier
- Allows both complex or real output

Applications
- Cellular base station for WCDMA, TD-SCDMA, CDMA2000 or WiMAX transmit channels
- Signal generator/test equipment
- Cable modem termination system
- Soft-defined radio
- WiMAX/WiBro

See TRF3703 diagram on previous page for the TSW3003 Reference Design using the DAC5687.

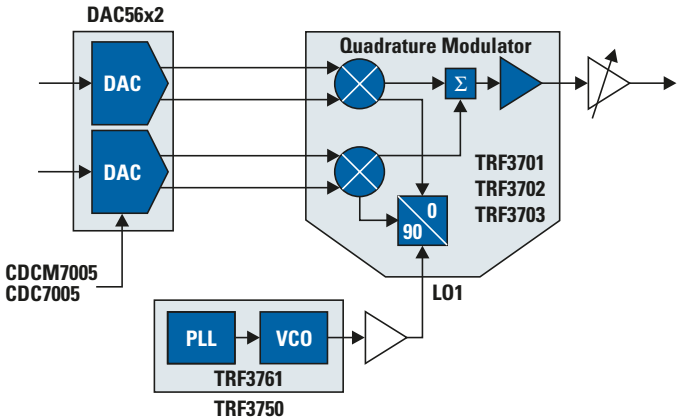
10/12/14-Bit, 275-MSPS Dual DACs
DAC5652, DAC5662, DAC5672

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/PARTnumber
(Replace **PARTnumber** with **DAC5652**, **DAC5662** or **DAC5672**)

The DAC5652, DAC5662 and DAC5672 are dual-channel, 10-/12-/14-bit, high-speed DACs with an on-chip voltage reference. Operating with update rates of up to 275 MSPS, the DAC5652, DAC5662 and DAC5672 offer exceptional dynamic performance and tight gain and offset matching, characteristics that make them suitable in either I/Q baseband or direct IF communication applications. The 10/12/14-bit family is pin-compatible, allowing easy resolution upgrades. The DAC290x, which is pin-compatible with DAC56x2, can be used for 5-V applications.

Key Features
- 275-MSPS update rate
- Single supply: 3.0 V to 3.6 V
- High SFDR: 85 dBc at 5 MHz
- High IMD3: 78 dBc at 15.1 and 16.1 MHz
- WCDMA ACLR: 70 dB at 30.72 MHz; 78 dB at baseband
- Independent or single resistor gain control
- Dual or interleaved data
- On-chip 1.2-V or external reference
- Low power: 330 mW; powerdown: 15 mW
- Packaging: 48-pin TQFP

Applications
- Cellular base station for WCDMA, TD-SCDMA, CDMA2000 or WiMAX transmit channels
- Medical/test instrumentation
- Arbitrary waveform generators (AWG)
- Direct digital synthesis (DDS)
- Cable modem termination systems (CMTS)



Cost-sensitive TI transmitter signal chain allows for direct digital baseband or complex IF to RF.

Transceiver Signal Chain

Ultra-Low-Power, 12-Bit, 40-MSPS Dual DAC
DAC2932

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/DAC2932

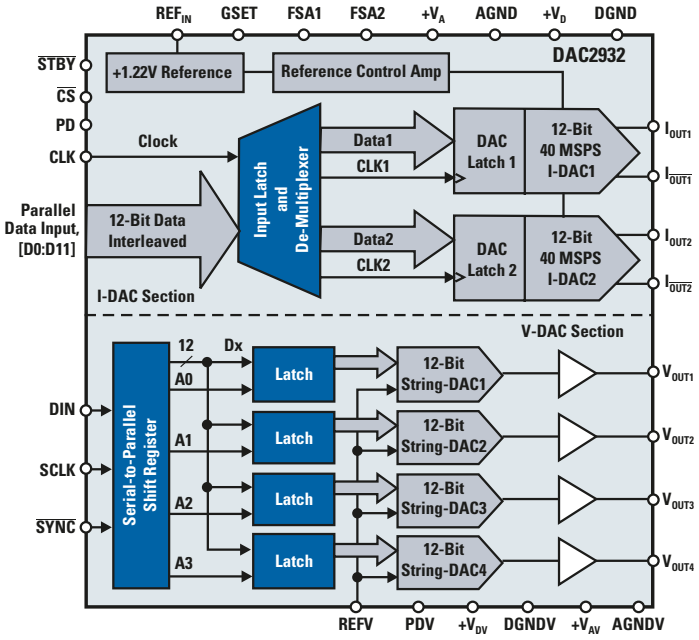
The DAC2932 is a 12-bit, 40-MSPS, dual DAC with four integrated voltage output control DACs. This DAC can be used for I and Q in wireless applications. The additional four voltage output control DACs provide wireless system cost savings by allowing the designer to control transmit and receive path gain, and to adjust filter and local oscillator frequencies. The use of these four control DACs simplifies the system design, provides flexibility and can lower overall system cost.

Key Features

- Dual 12-bit, 40-MSPS current output DACs
- Four 12-bit V_{OUT} DACs for signal path control
- Ultra-low power: 29 mW
- Adjustable full-scale output: 0.5 mA to 2 mA
- Single 3.3-V supply
- Powerdown mode: 25 µW
- Packaging: 48-lead TQFP

Applications

- Transmit channels:
  - I and Q
  - PC card modems: GPRS, CDMA
  - Wireless network cards (typ NICs)
- Signal synthesis (DDS)
- Portable medical instrumentation
- Arbitrary waveform generation (AWG)



DAC2932 functional block diagram.

14-Bit ADCs with LVDS/CMOS Outputs
ADS5545, ADS5546, ADS5547

Get samples, datasheets and evaluation modules at: **www.ti.com/ADS5546**

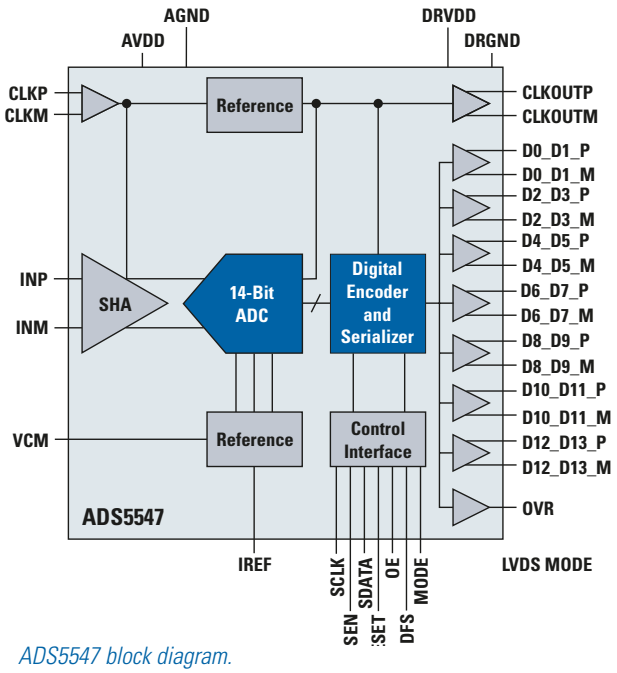
The 14-bit ADS5545, ADS5546 and ADS5547 are, respectively, 170-MSPS, 190-MSPS and 210-MSPS analog-to-digital converters (ADCs). These ADCs operate from a 3.3-V supply and offer unprecedented digital output flexibility with two output options—fully differential double-data-rate (DDR) LVDS or parallel CMOS. Using an internal sample-and-hold and a low-jitter clock buffer, the three devices support high SNR and high SFDR at high IFs. The 12-bit, pin-compatible ADS5525 and ADS5527 are 170-MSPS and 210-MSPS versions of the ADS5545 and ADS5547, respectively.

Key Features

- SNR: 73.2 dBc at 70-MHz IF
- SFDR: 84 dBc at 70-MHz IF
- Total power dissipation: 1.1 W
- DDR-LVDS and parallel-CMOS output options
- Internal/external reference support
- Clock duty cycle stabilizer
- Power-saving modes at lower sample rates
- 3.3-V analog and digital supply
- Packaging: QFN-48 (7 x 7 mm)

Applications

- Wireless communications infrastructure
- Software-defined radio
- Power amplifier linearization
- Test and measurement
- Medical imaging
- Radar systems



ADS5547 block diagram.

13-Bit, 210/250-MSPS ADCs
ADS5440, ADS5444

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/ADS5440 and **www.ti.com/sc/device/ADS5444**

The ADS5440 and ADS5444 are 13-bit ADCs (210-MSPS and 250-MSPS, respectively) that operate from a single 5-V supply and provide LVDS-compatible digital outputs from a 3.3-V supply. Both offer outstanding SNR performance as well as low noise and linearity over input.

Key Features

- SNR: 68.7 dBc at 100-MHz IF and 250 MSPS (ADS5444)
- SFDR: 78 dBc at 230-MHz IF and 250 MSPS (ADS5444)
- Differential input voltage: 2.2 V_{PP}
- Fully buffered analog inputs
- Total power dissipation: 2.1 W
- 2's complement output format
- 3.3-V LVDS-compatible outputs
- Packaging: TQFP-80 PowerPAD™

Applications

- Test and measurement
- Software-defined radio
- Multichannel base-station receivers
- Base-station TX digital predistortion
- Communications instrumentation

Monolithic 12-Bit, 500-MSPS ADC
ADS5463

Get samples, datasheets and evaluation modules at:
www.ti.com/sc/device/ADS5463

The new ADS5463 is TI's highest-performing, 12-bit monolithic ADC with a 500-MSPS sample rate. It provides 65.5-dBFS SNR and 80-dBc SFDR through 100-MHz f_{IN}. The ADS5463 comes in a space-saving 14 x 14-mm, 80-pin TQFP package and is pin-compatible with TI's 13-bit, 210-MSPS ADS5440 and 250-MSPS ADS5444. The new ADC also meets the resolution and speed needs for applications such as communications, amplifier linearization, test and measurement instrumentation, software-defined radio, and radar and imaging systems.

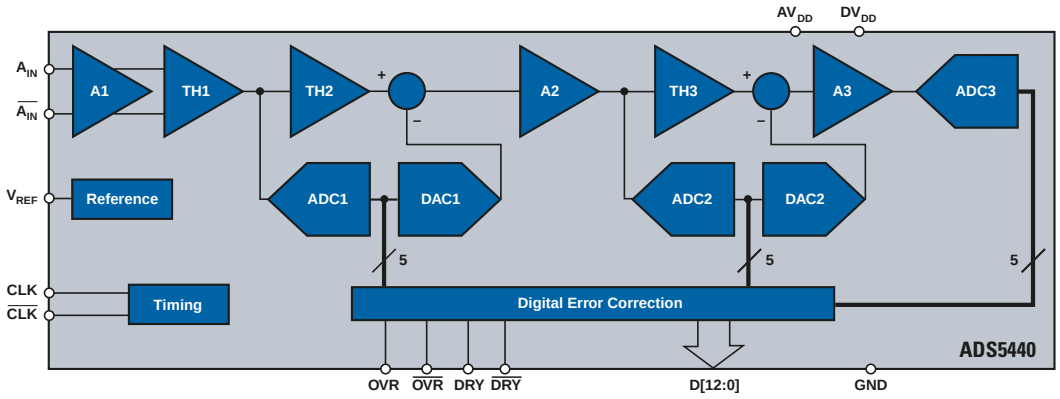
The ADS5463 input buffer isolates the internal switching of the onboard track-and-hold from disturbing the signal source while providing a high-impedance input. An internal reference generator is also provided to simplify the system design.

Key Features

- 12-bit resolution at 500 MSPS
- SNR: 65.5 dBFS at 100-MHz f_{IN} (500 MSPS)
- SFDR: 80 dBc at 100-MHz f_{IN} (500 MSPS)
- 10.5-bit ENOB at 100-MHz f_{IN} (500 MSPS)
- 5-V and 3.3-V analog and 3.3-V digital operation
- Total power dissipation: 2.25 W
- 3.3-V LVDS outputs
- 2.2-V_{PP} input range; 2-GHz input BW
- Pin-compatible with TI's ADS5440/44
- Packaging: 14 x 14-mm, 80-pin, TQFP PowerPAD™ package; available in I-temp, mil-temp, enhanced plastic and space-qualified packages

Applications

- Test and measurement instrumentation
- Multichannel base-station receivers
- Radar systems
- Software-defined radio
- Base-station digital predistortion
- Communications instrumentation



ADS5440/63 functional block diagram.

Transceiver Signal Chain

12-Bit, 40/65-MSPS Dual ADCs
ADS5231, ADS5232

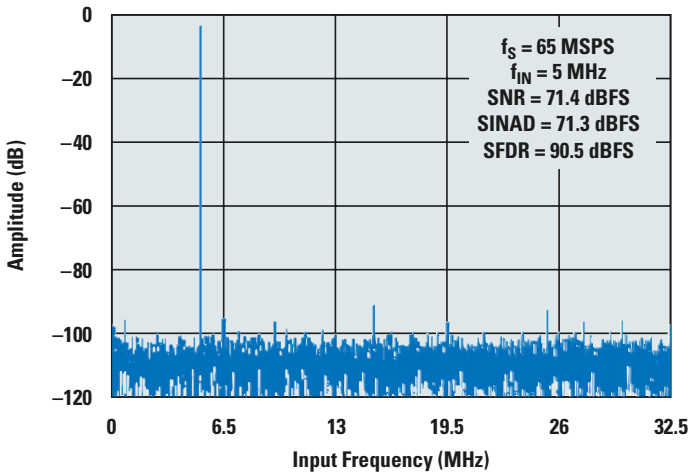
Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/ADS5231 or **www.ti.com/sc/device/ADS5232**

The ADS5231/32 is a dual, high-speed, high-dynamic-range, 12-bit pipelined ADC with very low power. This converter includes a high-bandwidth track-and-hold that gives excellent spurious performance up to and beyond the Nyquist rate.

The ADS5231/32 provides an over-range indicator flag to indicate an input signal that exceeds the full-scale input range of the converter. This flag can be used to reduce the gain of front-end gain control circuitry. An output enable pin allows for multiplexing and testability on a PC board.

Key Features
- Single +3.3-V supply
- High SNR: 70.5 dB
- Low power: 340 mW at 65 MSPS
- Internal or external reference
- Low DLE: 0.3 LSB
- Flexible input range: 1.5 V_{PP} to 2 V_{PP}
- Packaging: 64-pin TQFP

Applications
- Communications IF processing
- Communications base stations
- Test equipment
- Medical imaging
- Video digitizing
- CCD digitizing



Spectral performance.

10/12-Bit, 40/50/65/70-MSPS, Octal/Quad ADCs with Serial LVDS Interface
ADS527x, ADS5240, ADS5242

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/ADS527x, **www.ti.com/sc/device/ADS5240** or **www.ti.com/sc/device/ADS5242**

The ADS527x/ADS5240 is a family of multi-channel ADCs with a serial LVDS interface. This interface dramatically reduces the number of data lines at the output resulting in reduced package size while featuring unparalleled power and performance, allowing for high-density system integration.

Key Features
- 60.5-dB SNR (10-bit) at 10-MHz IF
- 70.5-dB SNR (12-bit) at 10-MHz IF
- 123-mW power per channel at 65 MSPS
- Independent powerdown for each ADC channel
- No missing codes
- Simultaneous sample-and-hold
- Internal and external references
- 3.3-V digital/analog supply
- Serialized LVDS outputs
- Option to double LVDS clock output currents
- Pin- and format-compatible family
- Packaging: 80-pin TQFP PowerPAD™

Applications
- Medical imaging
- Industrial ultrasonics
- Optical networking
- Instrumentation
- Test and measurement

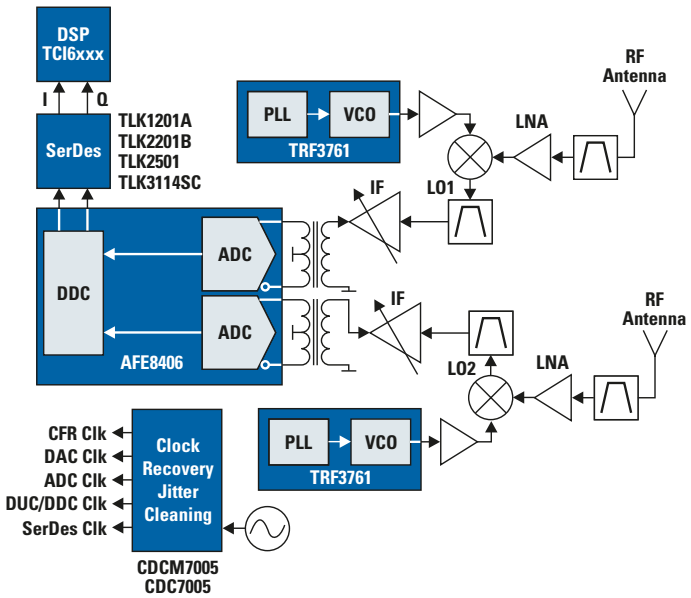
Integrated Wideband 8-Channel IF Receiver with Dual, 14-Bit, 85-MSPS ADC Front End
AFE8406

Get samples, datasheets and evaluation modules at:
www.ti.com/sc/device/AFE8406

The AFE8406 is a mixed-signal, IF-to-baseband receiver consisting of a dual-channel, 14-bit, 85-MSPS ADC and an 8-channel, multimode digital down converter (DDC). The integrated AFE8406 can be used as a single-chip IF solution for a 4-carrier WCDMA receiver with diversity, a 16-carrier TD-SCDMA receiver or an 8-carrier CDMA2000 receiver with diversity. Robust automatic generation control (RAGC) allows close loop control for better dynamic performance when a big-blocking signal is present. Digital automatic generation control (DAGC) automatically adjusts the gain of the DDC output to reach a target value for additional baseband processing.

Key Features
- Improved receiver sensitivity and blocking performance
- 14-bit ADC
- SFDR: 82 dBc at 70-MHz IF; 70 dBc at 140-MHz IF
- SNR: 70 dBc at 70-MHz IF; 68 dBc at 140-MHz IF
- RAGC and DAGC
- Fully programmable cascaded CIC/CFIR/PFIR

Applications
- Cellular base-station receiver
- WCDMA 4-carrier/sector with diversity
- TD-SCDMA 16-carrier/sector without diversity or 8-carrier/sector with diversity
- CDMA2000 8-carrier/sector with diversity
- Software-defined radio
- Intelligent antenna



AFE8406 in a high-IF heterodyne diversity receiver.

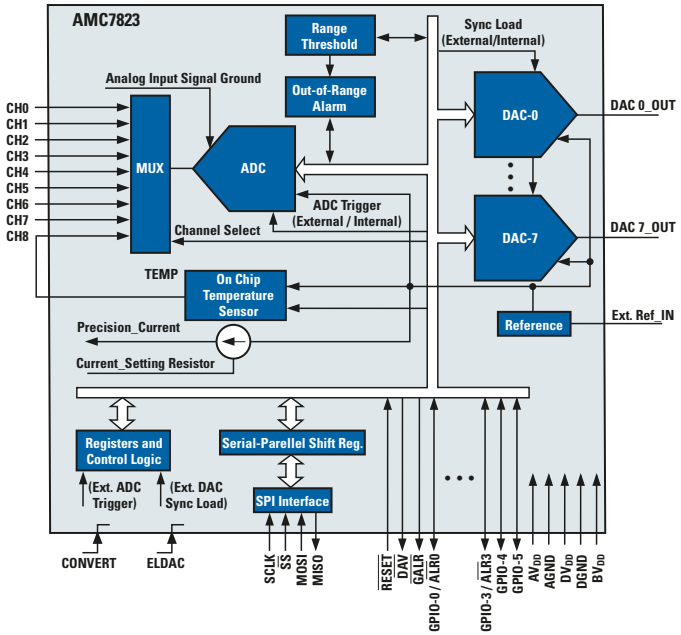
Analog Monitoring and Control Circuit
AMC7823

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/AMC7823

The AMC7823 is a complete analog monitoring and control circuit that includes an 8-channel, 12-bit ADC, eight 12-bit DACs, four analog input out-of-range alarms and six GPIOs to monitor analog signals and to control external devices. Also included are an internal sensor to monitor chip temperature and a precision current source to drive remote thermistors or RTDs to monitor remote temperatures.

Key Features
- 12-bit, 200-kSPS ADC
  - Eight analog inputs
  - Input range: 0 to 2 x V_{REF}
- Programmable V_{REF}, 1.25 V or 2.5 V
- Eight 12-bit DACs (2-µs settling time)
- Internal bandgap reference
- On-chip temperature sensor
- Precision current source
- SPI interface, 3-V or 5-V logic compatible
- Single supply: 3 V to 5 V
- Power-down mode
- Packaging: QFN-40 (6 x 6 mm)

Applications
- Communications equipment
- Optical networks
- ATE
- Industrial control and monitoring
- Medical equipment



AMC7823 functional block diagram.

Transceiver Signal Chain

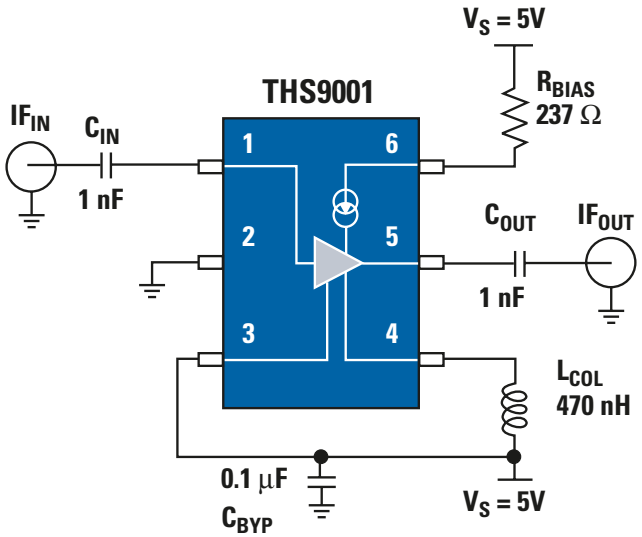
50- to 400-MHz Cascadable IF Amplifiers
THS9000, THS9001

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/THS9000 and **www.ti.com/sc/device/THS9001**

The THS9000 and THS9001 are medium power, cascadable, gain block optimized for 50- to 400-MHz IF frequencies. The amplifiers incorporate internal impedance matching to 50 Ω. The part mounted on the standard evaluation module achieves greater than 15-dB input and output return loss from 50 to 325 MHz with V_S = 5 V, R_{BIAS} = 237 Ω, L_{COL} = 470 nH. Design requires only two dc blocking capacitors, one power supply bypass capacitor, one RF choke and one bias resistor. The THS9000 comes in a very small 2 x 2-mm leadless MSOP package, and the THS9001 comes in a 6-pin SOT23 package. These devices make excellent choices for driving SAW filters, buffering LOs or general-purpose IF amplifiers.

Key Features
- OIP_3: 37 dBm at 300 MHz
- Gain: 15.5 dB
- Noise figure: 4.0 dB at 300 MHz
- 1-dB compression: 20.6 dBm
- V_S = 3 V to 5 V
- I_S is adjustable
- Packaging: 6-lead (leadless) MSOP, SOT23-6

Applications
- IF amplifier
- TDMA: GSM, IS-136, EDGE/UWC-136 standards
- CDMA: IS-95, UMTS, CDMA2000® standards
- Wireless local loop
- Wireless LAN: IEEE 802.11
- Radio links



THS9001 block diagram.

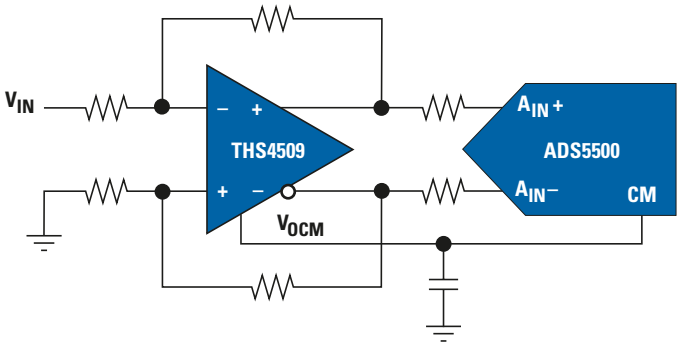
High-Speed, Fully Differential Op Amps
THS4509, THS4513

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/THS4509 and **www.ti.com/sc/device/THS4513**

The THS4509 and THS4513 are low-noise, fully differential amplifiers with unsurpassed linearity. With gains of 2 V/V and 1 V/V, respectively, they support 14-bit operation through 100 MHz. Both amplifiers are available in a small 16-lead QFN package and are characterized for operation above the full industrial temperature range of –40°C to +85°C.

Key Features (G = 10 dB for THS4509)
- Bandwidth: 1900 MHz
- Slew rate: 6600 V/µs
- OIP_3 = +43 dBm at 100 MHz
- NF = 16 dB (50-Ω system)
- Differential input/output
- Output common-mode voltage control
- Balanced architecture rejects common-mode noise and reduces even-order harmonic distortion

Applications
- Single-ended to differential conversion
- Differential ADC drivers
- Active differential anti-alias filters



THS4509 ADC interface block diagram.

Fixed-Gain, High-Speed Op Amps with Powerdown

THS4302, THS4303

Get samples, datasheets and evaluation modules at:
www.ti.com/sc/device/THS4302 and **www.ti.com/sc/device/THS4303**

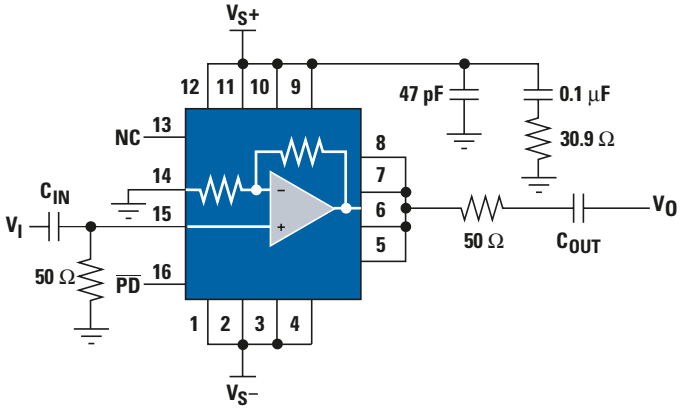
The THS4302 and THS4303 are ultra-low-distortion, single-supply-operation, wide-bandwidth, high-speed amplifiers ideal for use with high-resolution data converters. These voltage feedback amplifiers can operate from a single 5-V power supply while delivering a performance level of –88-dBc third-order intermodulation distortion (IMD3) at 100 MHz.

Key Features

- 2.4-GHz bandwidth (THS4302) and 1.8-GHz bandwidth (THS4303)
- G = 14 dB (THS4302) and G = 20 dB (THS4303)
- Slew rate: 5500 V/µs
- NF = 16 dB
- OIP_3 = 39 dBm at 100 MHz (R_L = 100 Ω)
- High output drive, I_O = ±180 mA (typ)
- V_S = 3 V to 5 V
- Evaluation modules available
- Packaging: Leadless 16-pin QFN

Applications

- High-frequency signal processing
- LO drives
- High-frequency ADC amplifiers



THS4302 and THS4303 block diagram.

Ultra-Wideband, Current-Feedback Op Amp with Disable

OPA695

Get samples and datasheets at: **www.ti.com/OPA695**

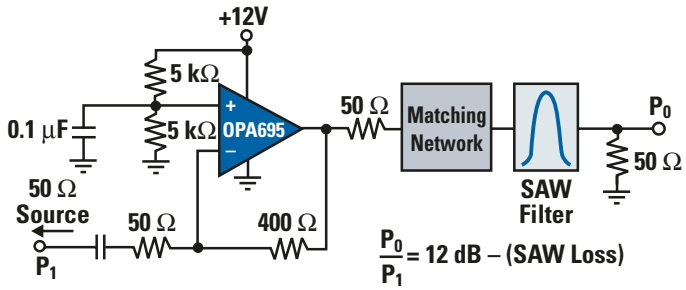
The OPA695 is a very high-bandwidth, current-feedback op amp that combines 4200-V/µs slew rate and low-input voltage noise to deliver a precision, low-cost, high-dynamic-range IF amplifier. Optimized for high-gain operation, the OPA695 is ideally suited to buffering SAW filters.

Key Features

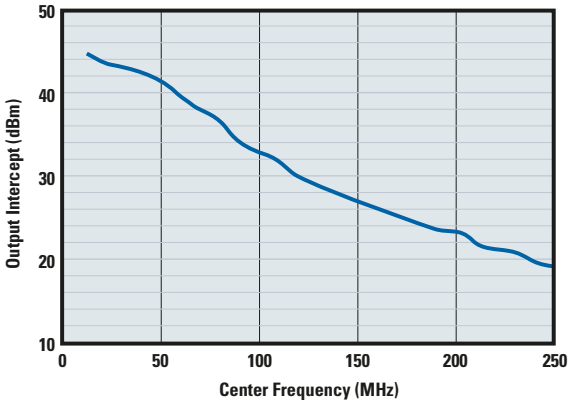
- Gain = +2 bandwidth: 900 MHz
- Gain = +8 bandwidth: 420 MHz
- Ultra-high slew rate: 4200 V/µs
- Third-order intercept: > 40 dBm (f < 50 MHz)

Applications

- Wideband ADC drivers
- Video line drivers
- ARB waveform output drivers



Low-distortion, 12-dB gain SAW driver.



Two-tone third-order intermodulation intercept.

Selection Guides

Digital Signal Processors

Device	Voltage Core (V)	Voltage I/O (V)	MHz	MIPS	Power[1] CPU (W)	Power[1] Total (W)	Internal RAM (Bytes) L1 Program Cache/ L1 Data Cache/ L2 Memory	CDMA Accelerator	Coprocessors	Serial RapidIO®	Communication	McBSP	Timers	Enhanced DMA Channels	Package	Price*
TMS320C6414	1.4	3.3	600	4800	0.6	1.5	16K/16K/1M	—	—	—	PCI/HPI	3	2	64	532 FCBGA, 23 mm	Call
TMS320C6415	1.4	3.3	600	4800	0.6	1.5	16K/16K/1M	—	—	—	PCI/HPI/UTOPIA	3	2	64	532 FCBGA, 23 mm	Call
TMS320C6416	1.4	3.3	600	4800	0.6	1.5	16K/16K/1M	—	VCP/TCP	—	PCI/HPI/UTOPIA	3	2	64	532 FCBGA, 23 mm	Call
TMS320C6414T	1.2	3.3	720	5760	0.44	1.36	16K/16K/1M	—	—	—	PCI/HPI	3	2	64	532 FCBGA, 23 mm	Call
TMS320C6415T	1.2	3.3	720	5760	0.44	1.36	16K/16K/1M	—	—	—	PCI/HPI/UTOPIA	3	2	64	532 FCBGA, 23 mm	Call
TMS320TCI100	1.2	3.3	720	5760	0.44	1.36	16K/16K/1M	—	VCP/TCP	—	PCI/HPI/UTOPIA	3	2	64	532 FCBGA, 23 mm	Call
TMS320TCI100Q	1.2	3.3	850	6800	0.52	1.60	16K/16K/1M	—	VCP/TCP	—	PCI/HPI/UTOPIA	3	2	64	532 FCBGA, 23 mm	Call
TMS320TCI6482	1.2	3.3/1.8	1000	8000	~1.0	~3.0	32K/32K/2M	RSA[2]	VCP2/TCP2	4 x 3.25 Gbps	PCI/HPI/UTOPIA/EMAC	2	2	64	697 FCBGA, 24 mm	Call

[1]Assume 60% CPU utilization, 50% EMIF utilization, 50% writes and bit switching, McBSP and timers at 100% utilization.
[2]Rake, RACH, Search and Spread Assist.
**Customers are advised to obtain the most current and complete pricing information from TI prior to placing orders.*

TMS320C28x™ Controller Generation

Device[1] (F) Flash (R) RAM-Only (C) ROM	MIPS	Boot ROM	RAM	Flash/ ROM	Timers	CAP/ QEP	PWM Channels	# HiRes PWM	12-Bit A/D Chs/ Conversion Time (ns)	EMIF	WD Timer	Comm Ports Other	Comm Ports SPI	Comm Ports SCI	Comm Ports CAN	I/O Pins	Core Voltage (V)	Package	Price*
TMS320**F28015** - PZA/S/Q	60	8 KB	12 KB	32 KB	9	2/0	8 + 2	4	16 ch/267	—	Y	I^2C	1	1	0	35	1.8	100 LQFP	3.25
TMS320**F28016** - PZA/S/Q	60	8 KB	12 KB	32 KB	9	2/0	8 + 2	4	16 ch/267	—	Y	I^2C	1	1	1	35	1.8	100 LQFP	3.50
TMS320**F2801**-60 - PZA/S/Q	60	8 KB	12 KB	32 KB	9	2/1	6 + 2	3	16 ch/267	—	Y	I^2C	2	1	1	35	1.8	100 LQFP	3.95
TMS320**F2802**-60 - PZA/S/Q	60	8 KB	12 KB	64 KB	9	2/1	6 + 2	3	16 ch/267	—	Y	I^2C	2	1	1	35	1.8	100 LQFP	4.75
TMS320F2801-PZA/S/Q	100	8 KB	12 KB	32 KB	9	2/1	6 + 2	3	16 ch/160	—	Y	I^2C	2	1	1	35	1.8	100 LQFP	5.80
TMS320F2801-GGMA/S[2], ZGMA/S	100	8 KB	12 KB	32 KB	9	2/1	6 + 2	3	16 ch/160	—	Y	I^2C	2	1	1	35	1.8	100 BGA	5.80
TMS320F2802-PZA/S/Q	100	8 KB	12 KB	64 KB	9	2/1	6 + 2	3	16 ch/160	—	Y	I^2C	2	1	1	35	1.8	100 LQFP	7.10
TMS320F2802-GGMA/S[2], ZGMA/S	100	8 KB	12 KB	64 KB	9	2/1	6 + 2	3	16 ch/160	—	Y	I^2C	2	1	1	35	1.8	100 BGA	7.10
TMS320F2806-PZA/S/Q	100	8 KB	20 KB	64 KB	15	4/2	12 + 4	4	16 ch/160	—	Y	I^2C	4	2	1	35	1.8	100 LQFP	8.70
TMS320F2806-GGMA/S[2], ZGMA/S	100	8 KB	20 KB	64 KB	15	4/2	12 + 4	4	16 ch/160	—	Y	I^2C	4	2	1	35	1.8	100 BGA	8.70
TMS320**F28044**-PZA/S	100	8 KB	20 KB	128 KB	19	0/0	16	16	16 ch/80	—	Y	I^2C	1	1	0	35	1.8	100 LQFP	9.95
TMS320F2808-PZA/S/Q	100	8 KB	36 KB	128 KB	15	4/2	12 + 4	4	16 ch/160	—	Y	I^2C	4	2	2	35	1.8	100 LQFP	11.60
TMS320F2808-GGMA/S[2], ZGMA/S	100	8 KB	36 KB	128 KB	15	4/2	12 + 4	4	16 ch/160	—	Y	I^2C	4	2	2	35	1.8	100 BGA	11.60
TMS320**F2809**-PZA/S/Q	100	8 KB	36 KB	256 KB	15	4/2	12 + 4	6	16 ch/80	—	Y	I^2C	4	2	2	35	1.8	100 LQFP	12.95
TMS320**F2809**-GGMA/S[2], ZGMA/S	100	8 KB	36 KB	256 KB	15	4/2	12 + 4	6	16 ch/80	—	Y	I^2C	4	2	2	35	1.8	100 BGA	12.95

[1]A = –40° to 85°C; S = –40 to 125°C (10% adder over A); Q = –40 to 125°C, Q100 qualified (15% adder over S).
*New products are listed in **bold red**.*
[2]Non Pb-Free/Green version of MicroStar BGA™. All other devices are Pb-Free/Green.
[3]Minimum volumes for C28x devices are 10 KU with NRE of $11,000.
**Prices are quoted in U.S. dollars and represent year 2007 suggested resale pricing. All prices are subject to change.*
Customers are advised to obtain the most current and complete pricing information from TI prior to placing orders. TI may verify final pricing prior to accepting any order.

Digital Down Converters/Digital Up Converters (DDCs/DUCs)

Device	Clock Rate (MSPS) (max)	Conversion Method	Narrowband Channels	Wideband Channels	Input Resolution (Bits) (max)	Output Resolution (Bits) (max)	SFDR (dB)	Power Channel (mW) (max)	Automatic Gain Control	Package	Price*
GC4016	100	Down	4	2	16	24	115	115	—	160 BGA	40.00
GC4116	105	Up	4	2	16	22	115	150	—	160 BGA	48.00
GC5016	160	Down,Up	4	4	16	16	115	250	Yes	252 BGA	28.75
GC5018	160	Down	16	8	16	16	115	250	Yes	305 BGA	50.00
GC5316	125	Down/Up	24 down/24 up	12/12	16	18	115	225	Yes	388 BGA	165.00
GC5318	125	Up	24	12	16	18	115	225	—	388 BGA	82.50

**Suggested resale price in U.S. dollars in quantities of 1,000.*

D/A Converters

Device	Resolution (Bits)	Update Rate (MSPS)	Power Consumption (mW) (typ)	Current Range (mA)	No. of DAC Channels	Analog Voltage AV/DD (Range) (V)	Analog Voltage AV/DD (V) (max)	SFDR (dB) (typ)	LVDS	Package(s)	Price*
DAC2932	12	40	29	2	2	2.7 to 3.3	3.3	75	—	48 TQFP	8.35
DAC904	14	200	170	20	1	2.7 to 5.5	5.5	76	—	28 SOIC, 28 TSSOP	7.35
DAC902	12	200	170	20	1	2.7 to 5.5	5.5	75	—	28 SOIC, 28 TSSOP	5.95
DAC900	10	200	170	20	1	2.7 to 5.5	5.5	68	—	28 SOIC, 28 TSSOP	4.20
DAC908	8	200	170	20	1	2.7 to 5.5	5.5	67	—	28 SOIC, 28 TSSOP	2.90
DAC5672	14	275	330	2 to 20	2	3 to 3.6	3.6	84	—	48 TQFP	13.25
DAC5662	12	275	330	20	2	3 to 3.6	3.6	81	—	48 TQFP	10.70
DAC5652	10	275	290	2 to 20	2	3 to 3.6	3.6	80	—	48 TQFP	7.60
DAC5675A	14	400	660	2 to 20	1	3.15 to 3.6	3.6	74	Yes	48 HTQFP	25.00
DAC5674	14	400	435	20	1	3 to 3.6	3.6	76	—	48 HTQFP	15.00
DAC5687	16	500	Note 1	2 to 20	2	3 to 3.6	3.6	80	—	100 HTQFP	22.50
DAC5686	16	500	445	20	2	3 to 3.6	3.6	72	—	100 HTQFP	19.75

[1]*Configuration dependent.* **Suggested resale price in U.S. dollars in quantities of 1,000.*

A/D Converters

Device	Resolution (Bits)	Sample Rate (MSPS) (max)	Power Consumption (mW) (typ)	SNR (dB)	SFDR (dB)	ENOB (Bits)	Analog Voltage AV/DD (V)	Number of Input Channels	LVDS	Package	Price*
ADS5270	12	40	907	70.5	85	11.3	3.0 to 3.6	8	Yes	80 HTQFP	44.00
ADS5240	12	40	592	70.5	85	11.3	3.0 to 3.6	4	Yes	80 HTQFP	20.00
ADS5271	12	50	957	70.5	85	11.3	3.0 to 3.6	8	Yes	80 HTQFP	48.00
ADS5232	12	65	335	70.7	86	11.3	3.0 to 3.6	2	—	64 TQFP	16.00
ADS5242	12	65	599	71	85	11.5	3.0 to 3.6	4	Yes	64 HTQFP	30.00
ADS5272	12	65	984	70.5	85	11.3	3.0 to 3.6	8	Yes	80 HTQFP	54.85
ADS5273	12	70	1003	71.1	85	11.5	3.0 to 3.6	8	Yes	80 HTQFP	121.00
ADS5520	12	125	740	69.4	83.6	11.3	3.0 to 3.6	1	—	64 HTQFP	27.50
ADS6425	12	125	1650	70.3	83	11.4	3.0 to 3.6	4	Yes	64 QFN	74.25
ADS5525	12	170	1100	70.5	84	11.3	3.0 to 3.6	1	Yes	48 QFN	35.00
ADS5527	12	210	1230	70.5	84	11.4	3.0 to 3.6	1	Yes	48 QFN	45.00
ADS5463	12	500	2250	65.2	84	10.5	4.75 to 5.25	1	Yes	80 HTQFP	125.00
ADS5440	13	210	2250	69	80	11.1	4.75 to 5.25	1	Yes	80 HTQFP	42.00
ADS5444	13	250	2250	69	73	11.1	4.75 to 5.25	1	Yes	80 HTQFP	59.00
ADS5553	14	65	725	74	84	—	3.0 to 3.6	2	—	80 HTQFP	30.00
ADS5423	14	80	1850	74	94	—	4.75 to 5.25	1	—	52 QFP	40.00
ADS5424	14	105	1900	74	93	12.3	4.75 to 5.25	1	—	52 QFP	56.00
ADS5500	14	125	780	70.5	82	11.3	3.0 to 3.6	1	—	64 HTQFP	49.00
ADS5545	14	170	1100	74	85	12	3.0 to 3.6	1	Yes	48 QFN	62.50
ADS5546	14	190	1130	73.5	87	11.8	3.0 to 3.6	1	Yes	48 QFN	82.50
ADS5547	14	210	1375	73.3	85	11.8	3.0 to 3.6	1	Yes	48 QFN	82.50

**Suggested resale price in U.S. dollars in quantities of 1,000.*

High-Speed Clocking

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Package(s)	Price*
CDCE421	Flexible low-jitter clock generator	Crystal/Single-Ended	LVPECL	11 MHz to 1.1 GHz	3.3	24/QFN	TBD
CDC7005	Clock synchronizer and jitter cleaner	LVCMOS	LVPECL	10 to 800	3.3	64/BGA, 48/QFN	10.00
CDCM7005	Clock synchronizer and jitter cleaner	LVCMOS/LVPECL	LVCMOS/LVPECL	0 to 1500	3.3	64/BGA, 48/QFN	10.75
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3.5 GHz	2.5/3.3	32/LQFP	5.55
CDCL6010	Clock multiplier and jitter cleaner with internal VCO	LVDS	CML	15 to 1250	1.8	48/QFN	7.50
CDCP1803	1:3 buffer with dividers	LVPECL/LVDS	LVPECL	0 to 800	3.3	24/QFN	3.15
CDCV304	1:4 fanout for PCI-X and general apps	LVTTL	LVCMOS	0 to 140	3.3	8/TSSOP	1.10

**Suggested resale price in U.S. dollars in quantities of 1,000.*

*New products are listed in **bold red**. Preview products are listed in **bold blue**.*

Selection Guides

High-Speed Amplifiers

Device				Architecture							Supply Voltage				ACL Min	BW	Slew Rate	Settling Time to 0.1% / 0.01%		THD 1 MHz	Differential Gain/Phase		V_N	V_{OS}	I_b	I_S/amp	I_{OUT}	Price*
Single	Dual	Triple	Quad	VFB	CFB	Diff I/O	FET	PGA	C-Stable	Shutdown	3 V	5 V	±5 V	±15 V	(V/V)	(MHz)	(V/µs)	(ns) (typ)		(dBc) (typ)	(%/°)		(nV/√Hz)	(mV) (max)	(µA) (max)	(mA) (typ)	(mA) (typ)	
Voltage-Feedback Op Amps																												
THS4011	THS4012			✔									✔	✔	1	290	310	37	90	–80	0.01	0.01	7.5	6	6	7.8	110	2.40/3.80
THS4031	THS4032			✔									✔	✔	2	100	100	60	90	–90	0.015	0.025	1.6	2	6	8.5	90	2.00/3.35
THS4041	THS4042			✔					✔				✔	✔	1	165	400	120	250	–89	0.01	0.01	14	10	6	8	100	1.65/3.35
THS4081	THS4082			✔									✔	✔	1	175	230	43	233	–79	0.01	0.05	10	7	6	3.4	85	1.80/2.95
THS4271				✔								✔	✔		1	1400	970	25	38	< –120	0.007	0.004	2.8	10	18	22	90	2.85
THS4275				✔						✔		✔	✔		1	1400	970	25	38	< –120	0.007	0.004	2.8	10	18	22	90	2.85
THS4601				✔			✔						✔	✔	1	440	100	135	170	–77	—	—	5.4	4	100 pA	10	80	9.95
OPA354	OPA2354		OPA4354	✔							✔	✔			1	250	150	30	—	–73	0.02	0.09	6.5	8	50 pA	4.9	100	0.75/1.20/1.80
OPA355	OPA2355	OPA3355		✔			✔		✔		✔	✔			1	450	300	30	120	–81	0.02	0.05	5.8	9	50 pA	8.3	60	0.90/1.50/1.90
OPA356	OPA2356			✔			✔				✔	✔			1	450	300	30	120	–81	0.02	0.05	5.8	9	50 pA	8.3	60	0.90/1.50
OPA357	OPA2357			✔					✔		✔	✔			1	250	150	30	—	–74	0.02	0.09	6.5	8	50 pA	4.9	100	0.75/1.20
OPA358				✔							✔				1	80	70	—	—	—	0.02	0.05	5.8	9	50 pA	6.5	80	0.45
OPA627				✔			✔						✔	✔	1	16	55	450	550	—	—	—	4.5	0.1	5 pA	7	45	12.25
OPA637				✔			✔						✔	✔	2	80	135	300	450	—	—	—	4.5	0.1	5 pA	7	45	12.25
	OPA2652			✔									✔		1	700	335	—	—	–77	0.05	0.03	8	7	15	11	140	1.20
OPA656				✔			✔						✔		1	500	290	10	—	–85	0.02	0.05	7	1.8	20 pA	14	70	3.40
OPA657				✔			✔						✔		7	350	700	10	—	–78	—	—	4.8	1.8	20 pA	14	70	3.80
OPA690	OPA2690	OPA3690		✔					✔			✔	✔		1	500	1700	8	—	–83	0.06	0.01	4.5	4	8	5.5	190	1.60/2.45/3.35
OPA694	OPA2694				✔								✔		1	1500	1700	13	20	—	0.03	0.015	2.1	3	18	5.8	80	1.25/1.90
	OPA2822			✔								✔	✔		1	400	170	32	—	–95	0.02	0.03	2	1.2	12	4.8	150	2.30
THS4303												✔			5	2500	1000	5	—	–92	—	—	2.4	0.5	6	34	100	2.10
THS4304												✔			1	2500	1000	5	—	–92	—	—	2.4	0.5	6	18	100	1.75
OPA842												✔	✔		1	350	400	15	—	—	0.003	0.006	2.6	0.3	20	20.2	±100	1.55
OPA843												✔	✔		3	500	1000	7.5	—	—	0.001	0.012	2	0.3	20	20.2	±100	1.60
OPA846												✔	✔		7	500	625	10	—	—	0.02	0.02	1.2	0.15	10	12.6	±80	1.70
OPA847												✔	✔		12	600	950	10	—	—	—	—	0.85	0.1	19	18.1	100/–75	2.00
THS9000											✔	✔			5.8	400	—	—	—	—	—	—	—	—	—	—	—	1.05
THS9001											✔	✔			5.8	350	—	—	—	—	—	—	—	—	—	—	—	1.05
OPA698												✔	✔		1	450	1100	8	—	—	0.012	0.008	5.6	2	3	15.5	±120	2.00
OPA699												✔	✔		6	285	1500	7	—	—	—	—	4.1	0.5	8	15.5	±100	2.05
Current-Feedback Op Amps																												
THS3061	THS3062				✔								✔	✔	1	300	7000	30	125	—	0.02	0.01	2.6	0.7	2	8.3	145	2.95/4.25
	THS3122				✔								✔	✔	1	160	1550	64	—	–80	0.01	0.011	2.2	6	23	8.4	440	3.75
	THS3125				✔				✔				✔	✔	1	160	1550	64	—	–80	0.01	0.011	2.2	6	23	8.4	440	3.75
OPA684	OPA2684	OPA3684			✔							✔	✔		1	170	780	—	—	–82	0.04	0.02	3.7	1.5	5	3.4	160	1.35/2.10/2.75
			OPA4684																									3.30
OPA691	OPA2691	OPA3691			✔					✔		✔	✔		1	400	2100	10	—	–81	0.001	0.01	2.5	2.5	35	5.1	190	1.55/2.45/3.30
OPA693												✔	✔		2	800	2400	3	—	–85	0.02	0.01	1.6	0.7	10	13	120	1.30
OPA695	**OPA2695**	**OPA3695**										✔	✔		1	1200	2400	3	—	–85	0.02	0.01	1.6	0.7	10	13	120	1.35
Differential I/O Op Amps																												
THS4509						✔					✔	✔			2	2000	6600	2	—	–98	—	—	1.9	5	13	37.7	96	3.75
THS4508						✔					✔	✔			2	2000	6400	2	—	–98	—	—	2.3	5	15.5	39.2	61	3.95
THS4511						✔					✔	✔			1	1400	4900	3.3	—	–97	—	—	2	5.2	15.5	39.2	61	3.45
THS4513						✔					✔	✔			1	1400	5100	16	—	–97	—	—	2.2	5.2	13	37.7	96	3.25
THS4520						✔					✔	✔			1	430	570	6.3	—	–100	—	—	2	5	10	15.3	105	2.35
Fixed-Gain Amplifiers																												
THS4302									✔		✔	✔			5	2400	5500	1.5	6	< –120	—	—	2.8	4.25	10	37	180	1.97
BUF634												✔	✔	✔	1	180	2000	200	—	—	0.4	0.1	4	100	20	15	250	3.05
OPA633													✔	✔	1	260	2500	50	—	—	0.1	0.1	—	15	35	21	100	5.45
OPA692		OPA3692							✔			✔	✔		1	225	2000	8	—	—	0.07	0.02	1.7	0.5	5	5.1	190	1.45/3.15
THS9000											✔	✔			5.8	400	—	—	—	—	—	—	—	—	—	—	—	1.05
THS9001											✔	✔			5.8	350	—	—	—	—	—	—	—	—	—	—	—	1.05

**Suggested resale price in U.S. dollars in quantities of 1,000.*

*New products are listed in **bold red**. Preview products are listed in **bold blue**.*

Overview

To Know More

For detailed information about interface and timing ICs for communications infrastructure:

Communications infrastructure systems are accommodating a wider range of technologies than ever before as the industry moves from 2G to 2.5G and 3G. Advanced wireless technologies like *Bluetooth*®, personal area networking (PAN), wireless local area networking (WLAN) with IEEE 802.11 technology, and leading wireless standards like GSM, CDMA and UMTS all place higher demands on communications systems for greater processing performance without jeopardizing power consumption or cost characteristics.

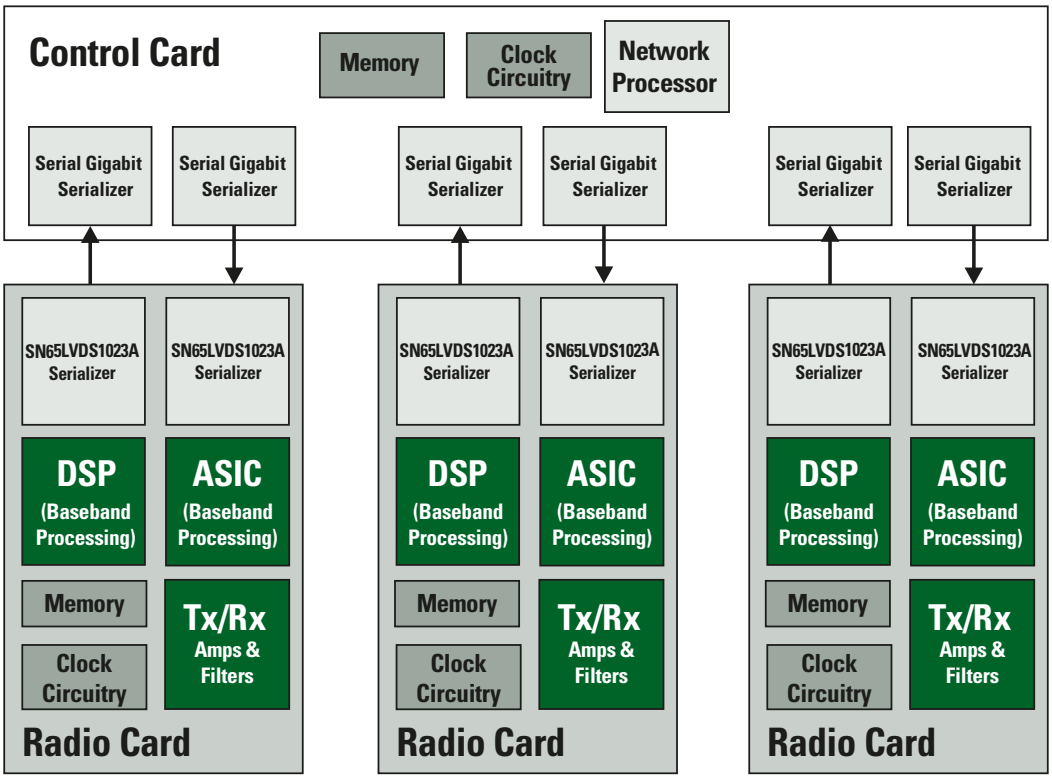
These increased data rates must be supported by base station and controller backplanes and the interconnections between these systems. Typically, this means the standard backplane either has to speed up or become wider, moving from 16-bit to 32-bit and beyond.

TI's interface and timing components simplify the generation of timing signals used to synchronize system activity to meet today's stringent clock-signal timing requirements. A wide selection of high-fanout drivers, repeaters and translators provides benefits such as low propagation delay, low-jitter and reduced skew, in addition to driving high-performance clocking systems.

TI interface and timing products that support wireless infrastructure applications include:

- Serializer/deserializer (SerDes) devices ranging from 100 Mbps to 3.125 Gbps, based on LVDS or LVPECL technology
- Repeaters, translators and multiplexers transmitting at speeds up to 4.0 Gbps
- Single-ended and differential bi-directional transceivers supporting multipoint topologies
- Clock solutions that buffer, synchronize, divide and multiply with low-phase noise
- PHY and link 1394 (FireWire™) solutions*
- Low-noise GTLP solutions

See **www.ti.com/connectivity for information.*



100-MHz to 600-MHz, 10-bit LVDS serializer/deserializer (SerDes) chipsets.

For more information about interface, visit: interface.ti.com

16:1 Serializer/Deserializer Transceivers with PRBS Testability

TLK1501, TLK2226, TLK2501, TLK2701, TLK2711, TLK3101, TLK4015

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/PARTnumber
(Replace **PARTnumber** with **TLK1501**, **TLK2226**, **TLK2501**, **TLK2701**, **TLK2711**, **TLK3101** or **TLK4015**)

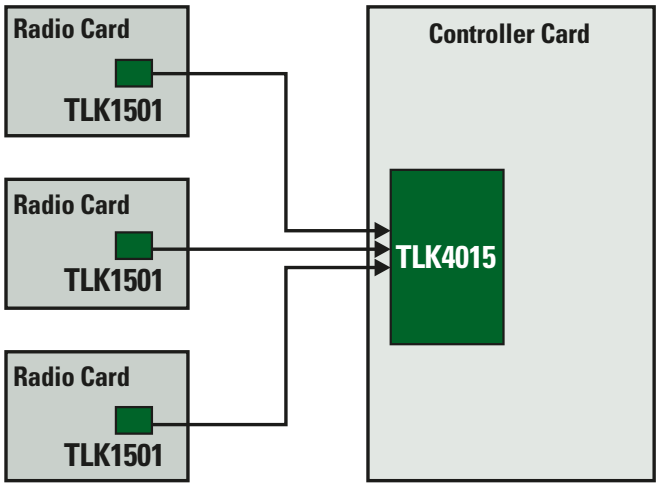
TI's TLK1501, TLK2226, TLK2501, TLK2701, TLK2711, TLK3101 and TLK4015 provide a 16-to-1 serializer/deserializer (SerDes) function with supported data rates from 600 Mbps to 3.125 Gbps. The devices feature built-in 8/10-bit encoding/decoding for easier design.

Key Features

- Hot-plug protection
- 2.5-V power supply for low-power operation
- Programmable voltage output swing on serial output
- Interfaces to backplane, copper cables or optical converters
- Rated for industrial temperature range
- On-chip 8/10-bit encoding/decoding
- On-chip PLL provides clock synthesis from low-speed reference
- Receiver differential input thresholds 200 mV (min)
- Loss-of-signal (LOS) detection
- CPRI data-rate compatible
- Packaging: 64-pin VQFP (PowerPAD™) (TLK1501, TLK2501, TLK2701, TLK3101), 80-pin MicroStar Junior™ BGA (GQE) (TLK2711), BGA (TLK2226, TLK4015)

Applications

- Radio-to-controller cards
- Antenna-to-receiver cards
- Base station backplanes



Single-channel and multichannel devices for radio-to-controller card interfaces.

10:1 LVDS SerDes Backplane Tx and Rx Chipsets

SN65LV1023A, SN65LV1224B

Get samples and datasheets at: **www.ti.com/sc/device/SN65LV1023A** and **www.ti.com/sc/device/SN65LV1224B**

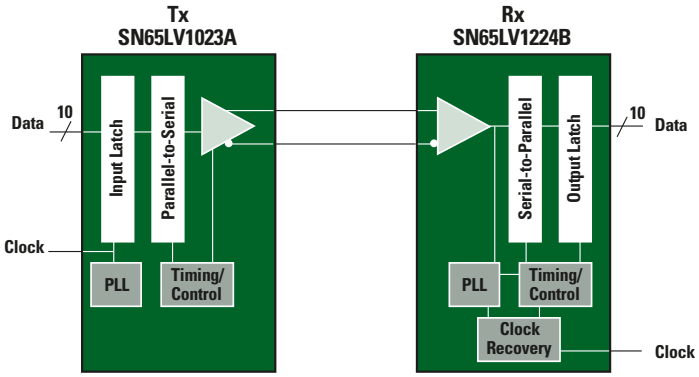
The TI SN65LV1023A transmitter and SN65LV1224B receiver devices provide base station backplane solutions between 100 and 660 Mbps. The chipset has a 10-bit LVTTL parallel-side input/output and a high-speed LVDS serial side input/output.

Key Features

- 100- to 600-Mbps serial LVDS data payload bandwidth at 10- to 66-MHz system clock
- Pin-compatible with other leading suppliers
- Chipset (serializer/deserializer) power consumption: <450 mW (typ) at 66 MHz
- Synchronization mode for faster lock
- Packaging: Standard SOIC and 70% smaller QFN packages

Applications

- Radio-to-controller card links
- Antenna-to-receiver links
- Base station backbones



SN65LV1023A and SN65LV1224B block diagram.

LVPECL/CML/LVDS Repeaters/Translators and Crosspoint Switches

SN65CML100, SN65LVCP22, SN65LVCP23, SN65LVDS20, SN65LVDS100, SN65LVDS101, SN65LVDS122, SN65LVDS250, SN65LVP20, SN65LVCP404

Get samples, datasheets and evaluation modules at:
www.ti.com/sc/device/PARTnumber
(Replace **PARTnumber** with **SN65CML100**, **SN65LVCP22**, **SN65LVCP23**, **SN65LVDS20**, **SN65LVDS100**, **SN65LVDS101**, **SN65LVDS122**, **SN65LVDS250**, **SN65LVP20** or **SN65LVCP404**)

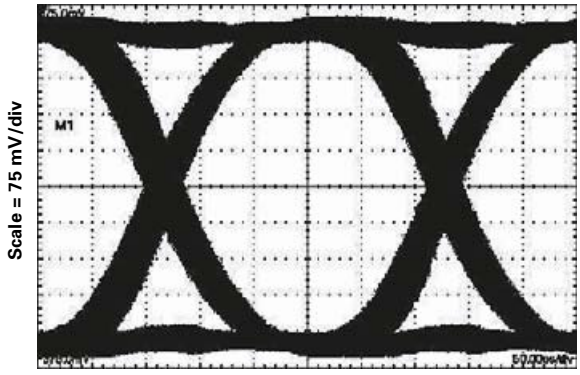
These high-speed repeaters/translators and crosspoint switches feature internal differential signal paths that maintain very low pulse and channel-to-channel skews.

Key Features

- Devices accept LVDS, CML and LVPECL inputs
- 1:1 translator repeaters:
  - LVDS20 and LVDS100 with LVDS output
  - LVP20 and LVDS101 with LVPECL output
  - CML100 with CML output
- Crosspoints:
  - LVDS122 2 x 2 – LVDS output
  - LVDS250 4 x 4 – LVDS output
  - LVCP22 2 x 2 – LVDS ouput
  - LVCP23 2 x 2 – LVPECL ouput
  - LVCP404 4 x 4 – VML ouput

Applications

- CML/LVPECL-to-LVDS translators
- LVDS/CML-to-LVPECL translators
- 2 x 2 Crosspoint and 2:1 Muxes
- 4 x 4 Crosspoint and 4:1 Muxes



SN65LVDS20 output eye pattern with 4-Gbps PRBS input.

Multipoint-LVDS for Clock Distribution Over Backplanes and Cables

SN65MLVD2, SN65MLVD3, SN65MLVD047A, SN65MLVD080, SN65MLVD082, SN65MLVD128, SN65MLVD200A, SN65MLVD201, SN65MLVD202A, SN65MLVD203, SN65MLVD204A, SN65MLVD205A, SN65MLVD206, SN65MLVD207

Get samples, datasheets, evaluation modules and application reports at:
www.ti.com/sc/device/PARTnumber
(Replace **PARTnumber** with **SN65MLVD2**, **SN65MLVD3**, **SN65MLVD047A**, **SN65MLVD080**, **SN65MLVD082**, **SN65MLVD128**, **SN65MLVD200A**, **SN65MLVD201**, **SN65MLVD202A**, **SN65MLVD203**, **SN65MLVD204A**, **SN65MLVD205A**, **SN65MLVD206** or **SN65MLVD207**)

TI introduced the industry's first family of transceivers compliant with the multipoint low-voltage differential signaling (M-LVDS) specification TIA/EIA-899. The SN65MLVD20x parts are half- and full-duplex single-channel transceivers. The SN65MLVD08x devices are 8-channel half-duplex transceivers that can operate at 125 MHz with up to 32 devices. The SN65MLVD047A is a quad M-LVDS driver. The SN65MLVD128 is a 1:8 LVTTL to M-LVDS fanout buffer. The latest releases, SN65MLVD2 and SN65MLVD3, are single-channel receivers.

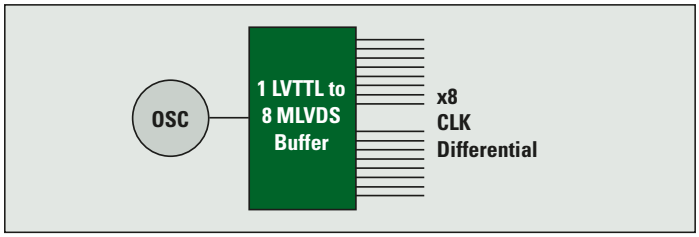
Key Features

- Half power, 10x speed of RS-485
- Complies with M-LVDS Standard (TIA/EIA-899)
- Supports wired-OR configuration – ideal for control lines
- Hot-plugging capability enhances reliability and robustness
- Controlled rise times for longer stub lengths

Applications

- Clock distribution up to 125 MHz
- ATCA PICMG 3.0 synchronous clocks
- Low-power, low-EMI RS-485 replacement

Common solution to date.



M-LVDS solution from TI.

Selection Guides

SerDes (Serial Gigabit Transceivers and LVDS)

Device	Function	Data Rate	Serial I/F[1]	Parallel I/F	Power	Special Features	Price*
General Purpose							
TLK1501	Single-Ch. 16:1 SerDes	0.6-1.5 Gbps	1 CML	16 LVTTL	200 mW	Built-In Testability	8.40
TLK2501	Single-Ch. 16:1 SerDes	1.6-2.5 Gbps	1 CML	16 LVTTL	300 mW	Built-In Testability	12.60
TLK2701	Single-Ch. 16:1 SerDes	1.6-2.5 Gbps	1 CML	16 LVTTL	300 mW	Built-In Testability and K Character Control	12.60
TLK2711	Single-Ch. 16:1 SerDes	1.6-2.5 Gbps	1 VML	16 LVTTL	350 mW	MicroStar Junior™ BGA Packaging	10.50
TLK3101	Single-Ch. 16:1 SerDes	2.5-3.125 Gbps	1 VML	16 LVTTL	350 mW	Built-In Testability	16.85
TLK2521	Single-Ch. 18:1 SerDes	1.0-2.5 Gbps	1 VML	18 LVTTL	<550 mW	Low Power and Built-In Equalization	12.60
TLK1521	Single-Ch. 18:1 SerDes	0.6-1.3 Gbps	1 VML	18 LVTTL	<350 mW	Low Power and Built-In Equalization	10.50
TLK4120	Four-Ch. 18:1 Serdes	0.5-1.3 Gbps	4 VML	18 LVTTL	<350 mW	Four-Channel Version of TLK1521	24.00
TLK4250	Four-Ch. 18:1 Serdes	1.0-2.5 Gbps	4 VML	18 LVTTL	<550 mW	Four-Channel Version of TLK2521	32.00
TLK4015	Four-Ch. of 16:1 Xcvr	0.6-1.5 Gbps/Ch.	4X CML	16 LVTTL/Ch.	1 W	Four-Channel Version of TLK1501	29.40
EPON							
TLK1211	Single-Ch. 10:1 Gigabit Ethernet	0.6-1.3 Gbps	1 LVPECL	10 LVTTL	200 mW	Fast Relock for PON	14.00
Gigabit Ethernet/FibreChannel							
TLK1201AI	Single-Ch. 10:1 Gigabit Ethernet Xcvr Gbps	0.6-1.3	1 LVPECL	10 LVTTL	200 mW	Industrial Temperature	4.85
TLK1221	Single-Ch. 10:1 Gigabit Ethernet Xcvr Gbps	0.6-1.3	1 LVPECL	10 LVTTL	200 mW	6 x 6-mm QFN Package	3.25
TLK2201BI	Single-Ch. 10:1 Gigabit Ethernet Xcvr	1.2-1.6 Gbps	1 LVPECL	10 LVTTL	200 mW	JTAG; 5-Bit DDR Mode, Industrial Temperature Qualified	4.65
TLK2201AJR	Single-Ch. 10:1 Gigabit Ethernet Xcvr	1.0-1.6 Gbps	1 LVPECL	10 LVTTL	200 mW	MicroStar Junior 5 x 5-mm LGA	4.25
TLK2208B	Eight-Ch. of 10:1 Gigabit Ethernet Xcvr	1.0-1.3 Gbps	8 VML	4/5-Bit/Ch. (Nibble DDR Mode), 8/10-Bit/Ch. (Multiplex Ch. Mode)	1 W	JTAG, MDIO Supported	31.50
TLK2226	Six-Ch. 16:1 Gigabit Ethernet Xcvr	1.0-1.3 Gbps	6 VML	4/5-Bit RTBI or RGMII	<1.5 W	MDIO Supported 100-FX mode support	19.65
10 Gigabit (XAUI) Ethernet							
TLK3104SA	Four-Ch. of 10/8:1 Xcvr	2.5-3.125 Gbps	4X 3.125 Gbps LVPECL (XAUI)	4X 10/8-Bit SSTL/HSTL	700 mW/Ch.	JTAG; Programmable Pre-Emphasis and XAUI I/F	69.30
TLK3104SC	Four-Ch. of 4.1: Xcvr	3.0-3.125 Gbps	4X LVPECL	20X622 LVDS Lines	700 mW/Ch.	JTAG, 8b/10b On/Off	126.00
TLK3114SC	Four-Ch. of 10/8:1: Xcvr	2.5-3.125 Gbps	4X 3.125 Gbps LVPECL (XAUI)	4X 10/8-Bit SSTL/HSTL (XGMII)	600 mW/Ch.	IEEE 802.3ae Backplane Transceiver Compliant	57.75
TLK3118	Four-Ch. 10/8:1 Xcvr w/ (XAUI) Full Redundancy	2.5-3.125 Gbps/Ch.	4X 3.125 LVPECL (XAUI)	8/10 HSTLx4 (XGMII)	<2 W	Full Redundancy for Four Channels (XAUI)	80.00
TLK10021	Four XAUI to XFI	10 Gbps	1 XFI	4 XAUI	800 mW	Built-In Testability	Web
LVDS Serdes							
SN65LVDS93/94	Four-Ch. 28:4 TX/RX Chipset	140-455 Mbps/Ch.	5 LVDS	28 LVTTL	250 mW/Chip	Supports Up to 1.82 Gbps Throughout	3.45
SN65LVDS95/96	Three-Ch. 21:3 TX/RX Chipset	140-455 Mbps/Ch.	4 LVDS	28 LVTTL	250 mW/Chip	Supports Up to 1.82 Gbps Throughout	3.45
SN65LV1023A/1224B	Single-Ch. 10:1 TX/RX Chipset	100-660 Mbps	1 LVDS	10 LVTTL	<400 mW	Low Power Solution	4.60
SN75LVDT1422	14:1 Xcvr SerDes	140 Mbps-1.4 Gbps	1 LVDS	14-Bit LVTTL	<300 mW	Supports Spread Spectrum Clocking	3.70
SN75LVDS82/83	Four-Ch. 28:4 TX/RX Chipset	0.651-1.428 Gbps	4 LVDS	28 LVTTL	250 mW/Chip	Commercial Temp	2.25
SN75LVDS84A/86	Three-Ch. 21:3 TX/RX Chipset	0.42-1.428 Gbps	3 LVDS	21 LVTTL	250 mW/Chip	Commercial Temp	2.10

[1]*CML = Current Mode Logic; VML = Voltage Mode Logic.*

*New products are listed in **bold red**.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

M-LVDS Transceivers, Drivers, Receivers and Clock Buffers

Device[1]	No. of Tx	No. of Rx	Rx Type	Half/ Full Duplex	Input Signal	Output Signal	Signaling Rate (Mbps)	Part-to-Part Skew (ps) (max)	Tx t_{pd} (ns) (typ)	Rx t_{pd} (ns) (typ)	I_{CC} (mA) (max)	ESD HBM (kV)	Package(s)	TIA/EIA-899 Standard Compliance	Price*
SN65MLVD2	—	1	1	—	M-LVDS	LVTTL	200	—	—	—	—	—	—	✔	Web
SN65MLVD200A	1	1	1	Half	LVTTL, M-LVDS	LVTTL, M-LVDS	100	1000	2.5	3.6	24	8	8SOIC	✔	1.55
SN65MLVD207	1	1	2	Full	LVTTL, M-LVDS	LVTTL, M-LVDS	200	1000	1.5	4	24	8	14SOIC	✔	1.85
SN65MLVD047	4	0	—	Half	LVTTL	M-LVDS	200	1000	1.5	—	60	12	16SOIC, 16TSSOP	✔	1.45
SN65MLVD128	8	1	—	—	LVTTL	M-LVDS	200	800	1.5	1.5	140	8	48TSSOP	✔	3.80
SN65MLVD080	8	8	1	Half	LVTTL, LVDS	LVTTL, M-LVDS	250	1000	2.4	6	180	8	64TSSOP	✔	4.75

[1]*Supply voltage for all devices listed above is 3.3 V and temperature range is –40 to 85°C.*

*New products are listed in **bold red**.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

LVDS Line Drivers and Receivers

Device	Max Drvr/Rcvr t_{pd} (ns)	Max Speed (Mbps)	Max Supply Current (mA)	HBM ESD Protection (kV)	# Inputs	# Outputs	Output Skew (ps)[1]	Pulse Skew (ps)[1]	Packages	Comments	Price*
SN65LVDS31	1.7	400	35	8	4 LVTTL	4 LVDS	—	200 typ	16-pin SOIC, 16-pin TSSOP	Quad driver	1.50
SN65LVDS33[2]	6	400	23	15	4 LVDS	4 LVTTL	150 typ	200 typ	16-pin SOIC, 16-pin TSSOP	Quad receiver	2.22

[1]*R_L = 100 Ω, C_L = 10 pF with max. spec.*

[2]*Integrated termination option.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

LVDS/LVPECL/CML Repeaters/Translators and Crosspoints

Device[1]	Description	No. of Tx	No. of Rx	Input Signal	Output Signal	Signaling Rate (Mbps)	Jitter Max (ps)	Part-to-Part Skew (ps) (max)	Tx t_{pd} (ns) (typ)	Rx t_{pd} (ns) (typ)	I_{CC} (mA) (max)	ESD HBM (kV)	Package(s)	Price*
Crosspoint Switch Family														
SN65LVCP23	2X2 Crosspoint Switch: LVPECL Outputs	2	2	LVPECL, LVDS, CML	LVPECL	1300	100	100	0.65	0.65	65	5	16SOIC, 16TSSOP	5.20
SN65LVCP40	Dual 1:2 Mux with Equalizer and Pre-Emphasis	6	6	LVPECL, LVDS, CML	CML	4000	30	500	1	1	254	4	48QFN	17.40
SN65LVDS122[2]	2X2 Crosspoint Switch: LVDS Output	2	2	LVPECL, LVDS, CML	LVDS	1500	65	150	0.9	0.9	100	4	16SOIC, 16TSSOP	4.75
SN65LVDS250[2]	4X4 Crosspoint Switch: LVDS Output	4	4	LVPECL, LVDS, CML	LVDS	2000	50	150	0.9	0.9	145	3	TSSOP	7.75
SN65LVCP404	4X4 Crosspoint Switch: LVDS Output	4	4	LVPECL, LVDS, CML	LVDS	4000	30	500	1	1	—	4	48QFN	Web
Repeaters/Translators														
SN65CML100	LVDS/LVPECL/CML-to-CML Repeater/Translator	1	1	LVPECL, LVDS, CML	CML	1500	70	100	0.8	—	12	5	8SOIC, 8VSSOP	2.55
SN65LVDS20	2.5/3.3-V LVDS repeater with enable	1	1	LVPECL LVDS, CML	LVDS	4000	45	130	0.63	—	45	3	8QFN	3.30
SN65LVP20	2.5/3.3-V LVPECL	1	1	LVPECL LVDS, CML	LVPECL	4000	10	130	0.63	—	45	3	8QFN	4.40

[1]*Supply voltage for all devices listed above is 3.3 V.*

*New products are listed in **bold red**.*

[2]*Integrated termination available (100 Ω)-SN65LVDTxxx.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Selection Guides

Clock Distribution Circuits

Device	Description	Input Level	Output Level	Frequency (MHz)	V_{CC} (V)	Package(s)	Price*
Ethernet							
CDCL6010	Clock multiplier and jitter cleaner with internal VCO	LVDS	CML	15 to 1250	1.8	48/QFN	7.50
CDCV304	1:4 fanout for PCI-X and general apps	LVTTL	LVCMOS	0 to 140	3.3	8/TSSOP	1.10
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3.5 GHz	2.5/3.3	32/LQFP	5.50
CDCLVD110A	1:10 programmable LVDS clock	LVDS	LVDS	0 to 900	2.5	32/TQFP	5.90
CDC7005	Clock synchronizer and jitter cleaner	LVCMOS	LVPECL	10 to 800	3.3	64/BGA, 48/QFN	10.00
CDCM7005	Clock synchronizer and jitter cleaner	LVCMOS/LVPECL	LVCMOS/LVPECL	0 to 1500	3.3	64/BGA, 48/QFN	10.75
CDC421125	Low-jitter clock generator for 125-MHz Ethernet	Crystal/Single-Ended	LVPECL	125	3.3	24/QFN	TBD
1G Ethernet							
CDCL6010	Clock multiplier and Jitter cleaner with internal VCO	LVDS	CML	15 to 1250	1.8	48/QFN	TBD
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3.5 GHz	2.5/3.3	32/LQFP	5.55
CDCV304	1:4 fanout for PCI-X and general apps	LVTTL	LVCMOS	0 to 140	3.3	8/TSSOP	1.10
CDC421125	Low-jitter clock generator for 125-MHz Ethernet	Crystal/Single-Ended	LVPECL	125	3.3	24/QFN	TBD
10G Ethernet							
CDCL6010	Clock multiplier and jitter cleaner with internal VCO	LVDS	CML	15 to 1250	1.8	48/QFN	TBD
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3.5 GHz	2.5/3.3	32/LQFP	5.55
CDC421156	Low-jitter clock generator for 156.25-MHz 10G Ethernet	Crystal/Single-Ended	LVPECL	156.25	3.3	24/QFN	TBD
CDC421312	Low-jitter clock generator for 312.50-MHz 10G Ethernet	Crystal/Single-Ended	LVPECL	312.5	3.3	24/QFN	TBD
Fibre Channel							
CDC421106	Low-jitter clock generator for 106.25-MHz Fibre Chan	Crystal/Single-Ended	LVPECL	106.25	3.3	24/QFN	TBD
CDC421212	Low-jitter clock generator for 212.25-MHz Fibre Chan	Crystal/Single-Ended	LVPECL	212.5	3.3	24/QFN	TBD
PCI Express							
CDC421100	Low-jitter clock generator for 100-MHz PCI Express	Crystal/Single-Ended	LVPECL	100	3.3	24/QFN	TBD
CDC421250	Low-jitter clock generator for 250-MHz PCI Express	Crystal/Single-Ended	LVPECL	250	3.3	24/QFN	TBD
Communications							
CDCM7005	Clock synchronizer and jitter cleaner	LVCMOS/LVPECL	LVCMOS/LVPECL	0 to 1500	3.3	64/BGA, 48/QFN	10.75
CDC7005	Clock synchronizer and jitter cleaner	LVCMOS	LVPECL	10 to 800	3.3	64/BGA, 48/QFN	10.00
CDCE706	Programmable 3-PLL clock generator with EEPROM	Crystal/Single-Ended/ Differential	LVTTL	<300	3.3	20/TSSOP	3.60
CDC706	Programmable 3-PLL clock generator	Crystal/Single-Ended/ Differential	LVTTL	<300	3.3	20/TSSOP	3.60
CDCE421	Flexible low-jitter clock generator, 10 MHz to 1.1 GHz	Crystal/Single-Ended	LVPECL	11 MHz to 1.1 GHz	3.3	24/QFN	TBD
TRX ADC/DAC Frequency Synthesizers/Jitter Cleaners							
CDC7005	Clock synchronizer and jitter cleaner	LVCMOS	LVPECL	10 to 800	3.3	64/BGA, 48/QFN	10.00
CDCM7005	Clock synchronizer and jitter cleaner	LVCMOS/LVPECL	LVCMOS/LVPECL	0 to 1500	3.3	64/BGA, 48/QFN	10.75
CDCLVP110	1:10 LVPECL/HSTL with selectable input clock	LVPECL/HSTL	LVPECL	0 to 3.5 GHz	2.5/3.3	32/LQFP	5.55
Baseband Card							
CDCL6010	Clock multiplier and jitter cleaner with internal VCO	LVDS	CML	15 to 1250	1.8	48/QFN	7.50
CDCVF25084	1:8 low-power 4x multiplier with two banks, SSC	LVTTL	LVTTL	10 to 180	3.3	16/TSSOP	2.45
CDCVF25081	1:8 low-power PLL clock with two banks, SSC	LVTTL	LVTTL	8 to 200	3.3	16/TSSOP/SOIC	1.25
CDC351I	1:10 with fast tpd fanout, 3-state outputs	LVTTL	LVTTL/LVCMOS	0 to 100	3.3	24/SOIC/SSOP	5.65
CDCLVD110A	1:10 programmable LVDS clock	LVDS	LVDS	0 to 900	2.5	32/TQFP	5.90
CDCP1803	1:3 buffer with dividers	LVPECL/LVDS	LVPECL	0 to 800	3.3	24/QFN	3.15
CDCE706	Programmable 3-PLL clock generator with EEPROM	Crystal/Single-Ended/ Differential	LVTTL	<300	3.3	20/TSSOP	3.60
CDCV304	1:4 fanout for PCI-X and general apps	LVTTL	LVCMOS	0 to 140	3.3	8/TSSOP	1.10

**Suggested resale price in U.S. dollars in quantities of 1,000.*

*New products are listed in **bold red**.*

Overview

To Know More

For detailed information about power management ICs for communications infrastructure:

Plug-In Power Modules

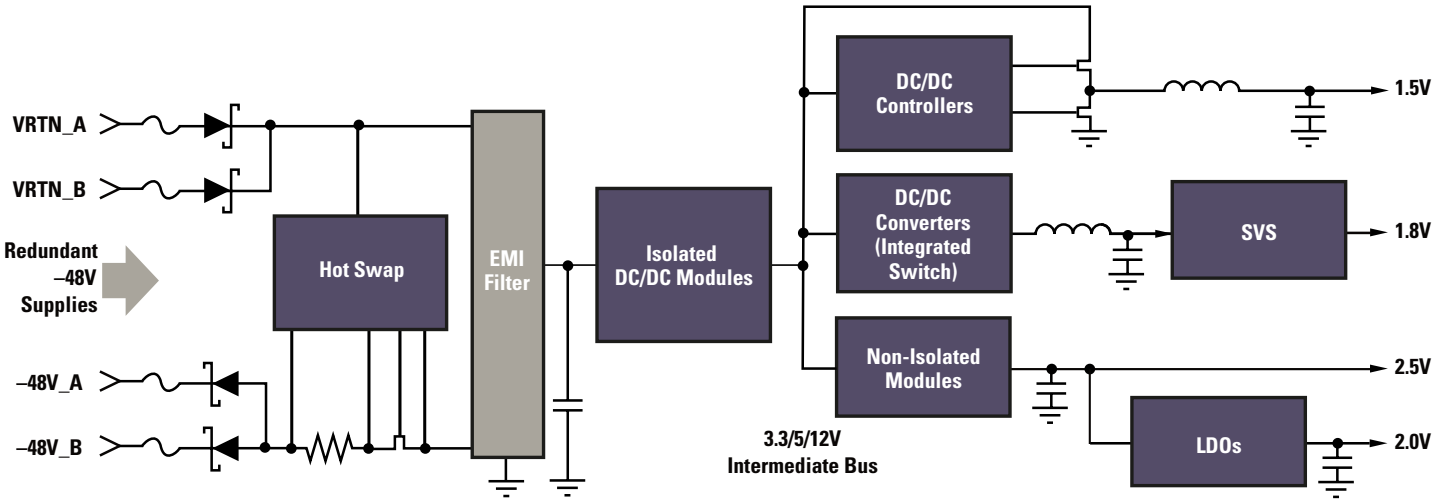
System Power

Communications infrastructure (CI) systems require that designers consider a wide range of power management technology. From discrete devices to modular approaches, designers must select technology that addresses the technical challenge of the system and offers ancillary benefits in terms of ease-of-use and supply chain reliability and efficiency.

Much of TI's broad range of high-performance power management products has been targeted at communications infrastructure applications. Additionally, TI provides customers with the design tools and support they need to make their designs easier and speed time-to-market. A wide range of discrete devices as well as isolated and non-isolated modular power technology is available.

Products specific to communications infrastructure applications include the following:

- **DC/DC Controllers and Converters:** These devices generate regulated supply rails. The TPS54xxx (SWIFT™) family of converters integrates the output FETs to simplify design, and the family provides output currents up to 14 A. Controllers such as the TPS40K™ series are ideal for a broader range of input voltages and output currents.
- **Isolated Plug-In Modules:** A number of products are specifically designed for 48-V bus applications. Many devices feature multiple channels for improved integration and lower system cost.
- **Non-Isolated Plug-In Modules:** Modules specifically designed for point-of-load applications come in high-performance packaging. A broad range of voltage and current options make these devices ideal for wireless infrastructure systems.
- **Hot Swap Power Managers:** Hot swap devices for the +48-V or the –48-V bus feature power limiting to ensure the MOSFET operates in its safe operating area.
- **Linear Regulators:** TPS79xxx low-noise LDOs are specifically designed for noise-sensitive RF applications and are stable with small ceramic capacitors.
- **Supply Voltage Supervisors:** Single- and dual-channel supply voltage supervisors provide fault protection while consuming very little board area.



Board power point-of-load power solution.

For more information about power management, visit: power.ti.com

Plug-In Power Modules

Point-of-Load Power Modules Offer *TurboTrans*™ Technology

T2 Series of Point-of-Load Modules

Get samples and datasheets at: **www.ti.com/T2**

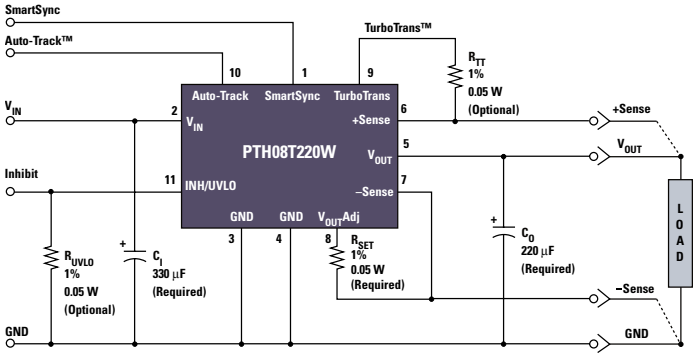
The PTH T2 series of plug-in power modules will support step-down DC/DC conversion from a wide-range input with adjustable output voltages from 0.7 to 5.5 V at output currents of up to 50 A. The power modules incorporate an innovative new *TurboTrans*™ technology that allows up to an 8x reduction in the amount of output capacitance.

Key Features

- *TurboTrans*™ technology
- SmartSync synchronization
- Auto-Track™ sequencing
- Prebias start-up capability
- Output current of up to 50 A
- Efficiencies up to 96%
- POLA™-compatible
- Packaging: Low-profile DIP module

Applications

- Wireless infrastructure
- Telecom
- Networking
- Servers



PTH08T220W block diagram.

Plug-In Power Selection Guide

Plug-In Power Modules

Device[1]	Input Bus Voltage (V)	Description	P_{OUT} or I_{OUT}	V_O Range (V)	V_O Adjustable	Auto-Track™ Sequencing	POLA™	Price*
Non-Isolated Single Positive Output								
PTH03010W	3.3	3.3-V Input, 15-A ISR with Auto-Track™ Sequencing	15 A	0.8 to 2.5	✔	✔	✔	11.60
PTH03020W	3.3	3.3-V Input, 22-A ISR with Auto-Track Sequencing	22 A	0.8 to 2.5	✔	✔	✔	18.15
PTH03030W	3.3	3.3-V Input, 30-A ISR with Auto-Track Sequencing	30 A	0.8 to 2.5	✔	✔	✔	25.00
PTH03050W	3.3	3.3-V Input, 6-A ISR with Auto-Track Sequencing	6 A	0.8 to 2.5	✔	✔	✔	6.90
PTH03060W	3.3	3.3-V Input, 10-A ISR with Auto-Track Sequencing	10 A	0.7 to 2.5	✔	✔	✔	9.80
PTH04000W	3.3/5	3-V to 5.5-V Input, 3-A POL with Auto-Track Sequencing	3 A	0.9 to 3.6	✔	✔	✔	4.50
PTH04040W	3.3/5	3-V to 5.5-V Input, 60-A ISR with Auto-Track Sequencing	60 A	0.8 to 3.6	✔	✔	✔	35.00
PTH04T220/221W	3.3/5	2.2-V to 5.5-V Input, 16-A T2 2nd Gen PTH POL with TurboTrans™	16 A	0.7 to 3.6	✔	✔	✔	12.60
PTH04T230/231W	3.3/5	2.2-V to 5.5-V Input, 6-A T2 2nd Gen PTH POL with TurboTrans	6 A	0.7 to 3.6	✔	✔	✔	7.90
PTH04T240/241W	3.3/5	2.2-V to 5.5-V Input, 10-A T2 2nd Gen PTH POL with TurboTrans	10 A	0.7 to 3.6	✔	✔	✔	10.80
PTH04T260/261W	3.3/5	2.2-V to 5.5-V Input, 6-A T2 2nd Gen PTH POL with TurboTrans	3 A	0.7 to 3.6	✔	✔		6.25
PTH05010W	5	5-V Input, 15-A ISR with Auto-Track Sequencing	15 A	0.8 to 3.6	✔	✔	✔	11.60
PTH05020W	5	5-V Input, 22-A ISR with Auto-Track Sequencing	22 A	0.8 to 3.6	✔	✔	✔	18.15
PTH05030W	5	5-V Input, 30-A ISR with Auto-Track Sequencing	30 A	0.8 to 3.6	✔	✔	✔	25.00
PTH05050W	5	5-V Input, 6-A ISR with Auto-Track Sequencing	6 A	0.8 to 3.6	✔	✔	✔	6.90
PTH05060W	5	5-V Input, 10-A ISR with Auto-Track Sequencing	10 A	0.8 to 3.6	✔	✔	✔	9.80
PTH05T210W	5	5-V Input, 30-A T2 2nd Gen PTH POL with TurboTrans	30 A	0.7 to 3.6	✔	✔	✔	18.00
PTH08T210W	12	5.5-V to 14-V Input, 30-A T2 2nd Gen PTH POL with TurboTrans	30 A	0.7 to 3.6	✔	✔	✔	18.00
PTH08T220/221W	5/12	4.5-V to 14-V Input, 16-A T2 2nd Gen PTH POL with TurboTrans	16 A	0.7 to 5.5	✔	✔	✔	12.60
PTH08T230/231W	5/12	4.5-V to 14-V Input, 6-A T2 2nd Gen PTH POL with TurboTrans	6 A	0.7 to 5.5	✔	✔	✔	7.90
PTH08T240/241W	5/12	4.5-V to 14-V Input, 10-A T2 2nd Gen PTH POL with TurboTrans	10 A	0.7 to 5.5	✔	✔	✔	10.80
PTH08T260/261W	5/12	4.5-V to 14-V Input, 3-A T2 2nd Gen PTH POL with TurboTrans	3 A	0.7 to 5.5	✔	✔		6.25
PTH12010L/W	12	12-V Input, 12-A ISR with Auto-Track Sequencing	12 A	0.8 to 1.8/1.2 to 5.5	✔	✔	✔	11.60
PTH12020L/W	12	12-V Input, 18-A ISR with Auto-Track Sequencing	18 A	0.8 to 1.8/1.2 to 5.5	✔	✔	✔	18.15
PTH12030L/W	12	12-V Input, 26-A ISR with Auto-Track Sequencing	26 A	0.8 to 1.8/1.2 to 5.5	✔	✔	✔	25.00
PTH12040W	12	12-V Input, 50-A ISR with Auto-Track Sequencing	50 A	0.8 to 5.5	✔	✔	✔	30.00
PTH12050L/W	12	12-V Input, 6-A ISR with Auto-Track Sequencing	6 A	0.8 to 1.8/1.2 to 5.5	✔	✔	✔	6.90
PTH12060L/W	12	12-V Input, 10-A ISR with Auto-Track Sequencing	10 A	0.8 to 1.8/1.2 to 5.5	✔	✔	✔	9.80
Isolated Single Output								
PT4210	48	3- to 7-W, 48-V Input, Isolated DC/DC Converter	3 to 7 W	3.3 to 12				18.75
PT4520	48	20-W, 48-V Input, Isolated DC/DC Converter	20 W	1.5 to 15	✔			32.45
PTB48520W	48	25-A, 48-V Input, Isolated POL Converter with Auto-Track I/O	75 W	1.8 to 3.6	✔	✔		62.00
PTB48560A/B/C	48	30-W, 48-V Input, Isolated POL Converter with Auto-Track I/O	30 W	3.3, 5, 12	✔	✔		25.00
PTEA4	48	50-W, 48-V Input, Isolated DC/DC Converter - Industry Std Footprint	50W	12	✔			26.50
PTMA4	48	10-W, 48-V Input, Isolated DC/DC Converter - Industry Std Footprint	10 W	3.3, 5, 12	✔			14.00
PTQA4	48	100-W, 48-V Input, Isolated DC/DC Converter - Industry Std Footprint	100 W	2.5, 3.3, 5	✔			35.00
PTQB4	48	200-W, 36-V to 75-V Input, Isolated Bus Converter with Auto-Track Control	200 W	8		✔		45.00
Isolated Multiple Outputs								
PTB48500	48	30-W, 48-V Input, Isolated Dual DC/DC Converter	30 W	3.3/1.2	✔			43.00
PTB48501A	48	35-W, 48-V Input, Isolated Dual DC/DC Converter	35 W	3.3/1.2 or 1.5	✔			45.00
PTB48502A	48	40-W, 48-V Input, Isolated Dual DC/DC Converter	40 W	3.3/1.2 or 1.5	✔			49.00

[1]See power.ti.com for a complete product offering.

*New products are listed in **bold red**.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

System Power Selection Guides

Hot Swap Controllers (External FET)

Device	Channels	V_{IN} Range (V)	Enable/ Shutdown	UV	OV	Fault	PG	Auto Retry	Ramp	Power Limiting	Package	Price*
TPS2393	1	–20 to –80	1H	✔	✔	✔	✔	✔	Current	No	14-pin TSSOP	1.80
TPS2399	1	–36 to –80	1H				✔	✔	Current	No	8-pin MSOP	1.25
TPS2491	1	9 to 80	1H	✔			✔	✔	Current	Yes	10-pin MSOP	1.70

**Suggested resale price in U.S. dollars in quantities of 1,000.*

DC/DC Controllers

Device	V_{IN} (V)	V_O (V) (max)	V_O (V) (min)	V_{REF} Tol (%)	Driver Current (A)	Output Current Capability (A)	Multiple Outputs	Frequency (kHz)	Protection[1]			Sync Pin	Price*
									OCP	UVLO	PG		
TPS40021	2.25 to 5.5	4	0.7	1	2	25	No	Program up to 1 MHz	✔	✔	✔	✔	1.15
TPS40057	8 to 40	35	0.7	1	1	20	No	Program up to 1 MHz	✔	✔			1.35
TPS40075	4.5 to 28	23	0.7	1	1	20	No	Program up to 1 MHz	✔	✔	✔		1.35
TPS40140	4.5 to 15	5.8	0.7	0.5	2	25 each channel	2 stack up to 16	Program up to 1 MHz	✔	✔	✔	✔	3.05

[1]*OCP = over-current protection, UVLO = under-voltage lockout, PG = Power Good.*

*New products are listed in **bold red**.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

DC/DC Converters (Integrated Switch)

Device[1]	I_{OUT} (mA)	V_{IN} (V)	V_{OUT} (V)	Max Frequency (kHz)	Power Good	Enable	Current Limit	Thermal Shutdown	UVLO	Sync Pin	Soft Start	EVM	Package	Comments	Price*
TPS54110	1500	3.0 to 6.0	Adj. to 0.9	700	✔	✔	✔	✔	✔	✔	✔	✔	20 HTSSOP	Synchronous Buck	2.00
TPS62110	1500	3.1 to 17	Adj. to 1.2	1000	✔	✔	✔	✔	✔	✔	✔	✔	16 QFN	Synchronous Buck	2.50
TPS54350	3000	4.5 to 20	Adj. to 0.9	700	✔	✔	✔	✔	✔	✔	✔	✔	16 HTSSOP	Sync. or Non-sync. Buck	2.05
TPS54317	3000	3.0 to 6.0	Adj. to 0.9	1600	✔	✔	✔	✔	✔	✔	✔	✔	24 QFN	Synchronous Buck	2.50
TPS54550	6000	4.5 to 20	Adj. to 0.9	700	✔	✔	✔	✔	✔	✔	✔	✔	16 HTSSOP	Sync. or Non-sync. Buck	2.95
TPS54610	6000	3.0 to 6.0	Adj. to 0.9	700	✔	✔	✔	✔	✔	✔	✔	✔	28 HTSSOP	Synchronous Buck	3.35
TPS54910	9000	3.0 to 4.0	Adj. to 0.9	700	✔	✔	✔	✔	✔	✔	✔	✔	28 HTSSOP	Synchronous Buck	4.20
TPS54010	14000	2.25 to 4.0	Adj. to 0.9	700	✔	✔	✔	✔	✔	✔	✔	✔	28 HTSSOP	Dual Input Bus (2.5, 3.3 V)	5.30

[1]*Software tool for all devices available at **www.ti.com/swift***

*New products are listed in **bold red**.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Low Dropout Regulators (LDOs)

Device[1]	I_O (mA)	V_{DO} at I_O (mV)	I_q (µA)	Output Options		V_{IN}		Accuracy (%)	Package(s)						C_O[2]	Comments	Price*
				Fixed Voltage (V)	Adj. (V)	(V) (min)	(V) (max)		QFN	DDPAK-7	SOIC-8	MSOP	SOT223	TO263			
TPS794xx	250	145	172	1.8, 2.5, 2.8, 3.0, 3.3	1.2 to 5.5	2.7	5.5	3			✔	✔			2.2-µF C	RF Low Noise, High PSRR	0.65
TPS795xx	500	105	265	1.6, 1.8, 2.5, 3.0, 3.3	1.2 to 5.5	2.7	5.5	2				✔			1-µF C	RF Low Noise, High PSRR	1.05
TPS796xx	1000	200	310	1.8, 2.5, 2.8, 3.0, 3.3	1.2 to 5.5	2.7	5.5	2				✔	✔		1-µF C	RF Low Noise, High PSRR	1.10
TPS786xx	1500	390	310	1.8, 2.5, 2.8, 3.0, 3.3	1.2 to 5.5	2.7	5.5	2				✔	✔		1-µF C	RF Low Noise, High PSRR	1.35
TPS74201	1500	55	300	Adjustable only	0.8 to 3.3	0.9	5.5	1	✔	✔					Any/None	Tracking/Adj. Soft Start	2.25
TL1963A	1500	341	1000	1.5, 1.8, 2.5, 3.3	1.21 to 21	2.22	20	1			✔		✔	✔	10-µF C	Fast Transient Response	2.05

[1]*xx represents the voltage option. For example, 33 represents the 3.3-V option. The adjustable output voltage option is represented by 01.*

[2]*C = ceramic.*

*New products are listed in **bold red**.*

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Supply Voltage Supervisors

Device	Number of Supervisors	Supervised Voltages	Package	I_{DD} (µA) (typ)	Time Delay (ms)	Reset Threshold Accuracy (%)	Manual Reset Input/MR	Active-Low Reset Output	Reset Output Topology[1]	Price*
TPS3801	1	Adj./1.8/2.5/3.0/3.3/5.0	SC-70	9	200	2	✔	✔	PP	0.49
TPS3106	2	Adj./0.9/1.6/3.3	SOT-23	1.2	130	0.75	✔	✔	OD	0.90
UCD9080	8	Prog. by software GUI	32 QFN	300	Prog.	Power Supply Sequencer and Monitor				2.95

[1]*PP = push-pull, OD = open drain.*

*New products are listed in **bold red**.*

Note: Custom voltages can be provided. Minimum order quantities may apply. Contact TI for details and availability.

**Suggested resale price in U.S. dollars in quantities of 1,000.*

Overview

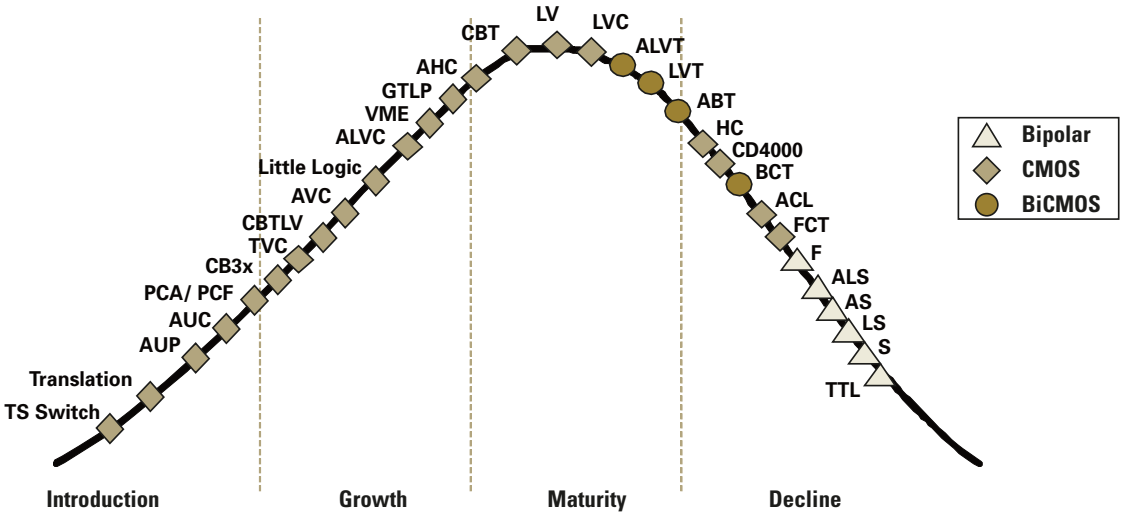
To Know More

For detailed information about logic for communications infrastructure:

As communications infrastructure designers look to increase data throughput, reduce power consumption and shrink form factors, TI's logic portfolio is constantly advancing while at the same time the company is dedicated to providing legacy logic devices.

As the leading provider of logic, TI's latest technologies are targeted for the fast-moving market of communications infrastructure systems. Advanced CMOS families and functions like the LVC and ALVC are optimized at 3.3-V V_{CC}. And the CBT and CBTLV families of bus switches offer designers a broad portfolio to meet diverse switching needs.

For more information about logic, visit: logic.ti.com

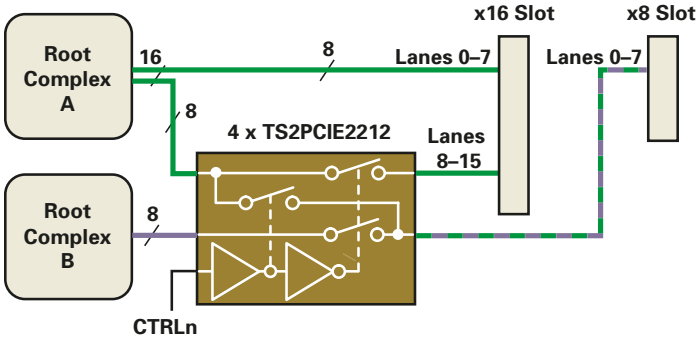


Two-Lane 1:2 PCI Express MUX/DeMUX
TS2PCIE2212

Get samples and datasheets at: **www.ti.com/sc/device/TS2PCIE2212**

The TS2PCIE2212 can be used to multiplex/demultiplex two PCI Express lanes. The switch operates at the PCI Express 2.5-Gbps signal-processing speed and is composed of two banks. Each bank accommodates two sources (A and B) and two destinations (A and B).

When a logic-level low is applied to the control pin (CTRL), source A is connected to destination A, and source B is connected to destination B. When a logic-level high is applied to CTRL, source A is connected to destination B, while source B and destination A are open.

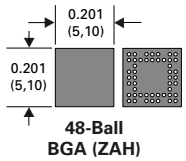


TS2PCIE2212 solution.

Applications

- Servers and workstations
- Laptop docking stations
- PCs and laptops

Advanced Package Option



Device Characteristics

Device	V_{DD} (V) (min/max)	No. of Lanes	r_{on} (Ω) (typ)	Data Rate (Gbps)	Description	I_{CC} (µA)	$C_{IO(ON)}$ (pF)	Crosstalk (dB)	Off Isolation (dB)
TS2PCIE2212	1.7/1.9	2:4	10	2.5	2-lane 1:2 PCI Express MUX/DeMUX	160	3.5	–39	–38
TS3L500AE	3.0/3.6	8:16	4	1.1	SPDT Gigabit LAN Switch	250	2.5	–37	–37

Maintenance and Control: I²C I/O Expansion

Get more information at: **www.ti.com/i2c**

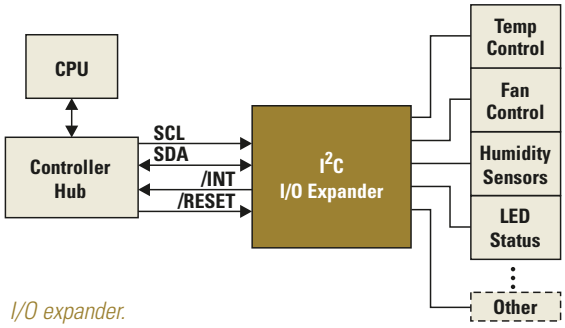
Designers can make better use of their scarce GPIOs by using TI's I²C I/O expanders and multiplexers to time-share multiple peripherals to a single I²C port. For example, the I/O expanders and multiplexers can be used to monitor and control a total system by taking advantage of the already available I²C bus.

Advantages

- Resolves I²C address conflicts
- Processor pin savings
- Improved board routing
- Reduced board space

Applications

- I²C bus isolation
- LED control
- Temperature sensing
- Fan control



I/O expander.

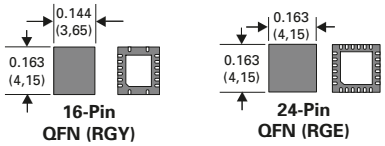
Suggested Devices

Device Type	Device	Frequency (kHz) (max)	I²C Address	V_{CC} Range (V)	Bit or Channel Width
I²C I/O Expanders	PCA9536	400	1000 001	2.3 to 5.5	4 bits
	TCA6408	400	0100 xxx	1.65 to 5.5	8 bits
	PCA6107	400	0011 xxx	2.3 to 5.5	8 bits
	PCF8574	100	0100 xxx	2.5 to 6.0	8 bits
	PCA9554	400	0011 xxx	2.3 to 5.5	8 bits
	PCA9557	400	0011 xxx	2.3 to 5.5	8 bits
	PCF8575	400	0100 xxx	2.5 to 5.5	16 bits
	PCA9535	400	0100 xxx	2.3 to 5.5	16 bits
	PCA9538	400	1110 xxx	2.3 to 5.5	8 bits
	PCA9539	400	1110 1xx	2.3 to 5.5	16 bits
	PCA9555	400	0100 xxx	2.3 to 5.5	16 bits
I²C MUXes and Switches	PCA8550	400	1001 110	3.0 to 3.6	5 bits
	PCA9544A	400	1110 xxx	2.3 to 5.5	4 channels
	PCA9545A	400	1110 0xx	2.3 to 5.5	4 channels
	PCA9546A	400	1110 xxx	2.3 to 5.5	4 channels
	PCA9548	400	1110 xxx	2.3 to 5.5	8 channels
I²C Bus Buffer/Hub	P82B96	400	—	8.0 to 15	—
	PCA9518*	400	—	3.0 to 3.6	5 channels

**Preview*

Advanced Package Options

(Additional packages may be available)



Serial Communications Interface
RS-232, USB, RS-485/422

Get more information at: **www.ti.com/interface**

RS-232: The TIA/EIA-232 devices provide a single-ended interface between data terminal equipment (DTE) and data communication equipment (DCE).

USB: The TUSB1105/6 and **TUSB2551*** provide an analog USB interface along with flexible voltage-level translation and system-level ESD protection.

RS-485/422: TI's robust TIA/EIA-485/422-compliant devices are specially designed for harsh industrial environments that can require differential signal transmission at up to 50 Mbps or as far as 1.2 km.

Key Features

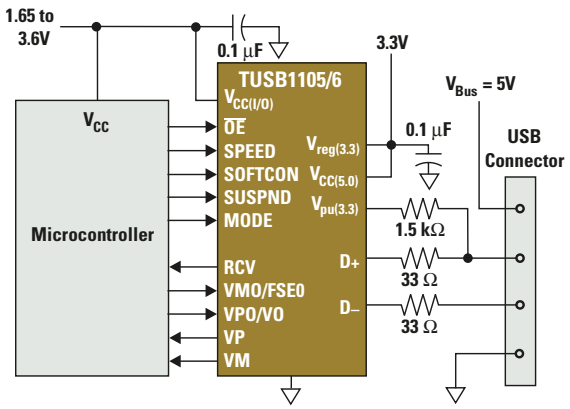
- System-level ESD protection
- NiPdAu Pb-Free solution for whisker-free, reliable packages
- Space-saving QFN package options

**Preview*

Suggested Devices

Type	Tx/Rx	Device (Speed)	
RS-232	1/1	SNx5C3221E (1 Mbps)	
	2/2	SNx5C3222E (1 Mbps)	SNx5C3223E (1 Mbps)
		SNx5C3232E (1 Mbps)	
	3/2	TRS3386E (250 kbps)	
	3/5	TRS3243E (500 kbps)	
RS-485	1/1	SN65ALS176/A/B (35 Mbps)	
	2/2	SNx5C1167 (10 Mbps)	SNx5C1168 (10 Mbps)
	0/4	AM26LS32A (10 Mbps)	AM26LV32 (10 Mbps)
	4/0	AM26LV31 (10 Mbps)	SN75ALS192 (20 Mbps)
USB 2.0	1/1	TUSB1105/6 and **TUSB2551*** (Full and low speed)	

**Preview*



Typical USB interface application.

Gunning Transceiver Logic Plus
GTLP Family

Get samples, datasheets and application reports at: **logic.ti.com**

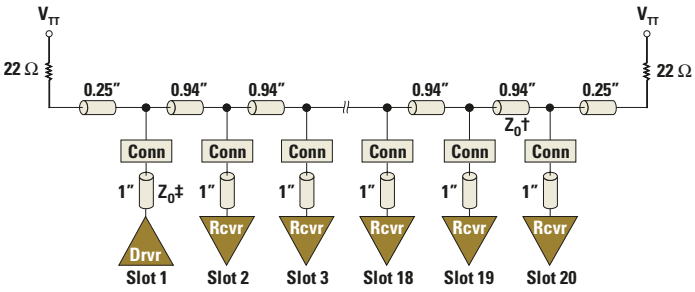
TI provides backplane interface solutions for telecom/datacom end equipment with the open-drain GTLP technology. This provides better signal integrity and overall system improvement over traditional logic, driving heavily loaded backplanes.

Key Features

- GTLP low-output-voltage swing reduces EMI
- Reduced-input GTLP threshold provides adequate noise margin
- TI-OPC™ and OEC circuitry provide improved signal integrity
- I_{off}, power-up 3-state and BIAS V_{CC} support live insertion
- Bi-directional interface between GTLP and LVTTL signal levels
- 5-V-tolerant LVTTL I/Os allow mixed-voltage systems
- Up to 100-mA drive capability to drive heavily loaded backplanes
- Packaging: Space-saving TSSOP (DGG), TVSOP (DGV) and LFBGA (GKE/GKF)

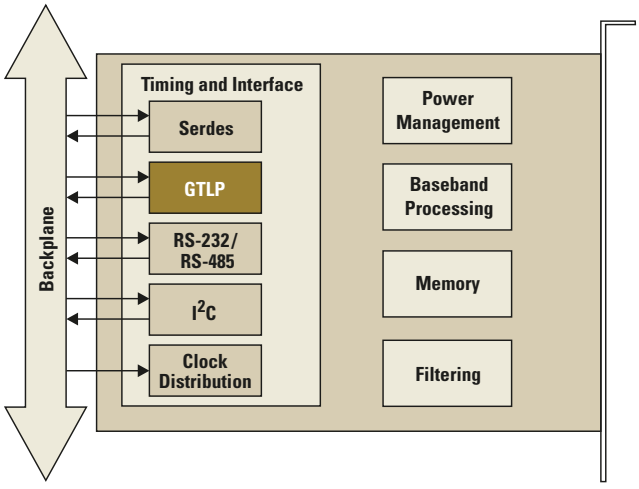
Applications

- Base stations
- Networking



† Unloaded backplane trace natural impedance (Z_0) is 45 Ω. 45 to 60 Ω is allowed with 50 Ω being ideal.
‡ Card stub natural impedance (Z_0) is 60 Ω.

Single-bit representation of a multipoint parallel backplane.



Radio card diagram.

Universal Bus Transceiver for the VMEbus Backplane
SN74VMEH22501A

Get samples, datasheets and application reports at:
www.ti.com/sc/device/SN74VMEH22501A

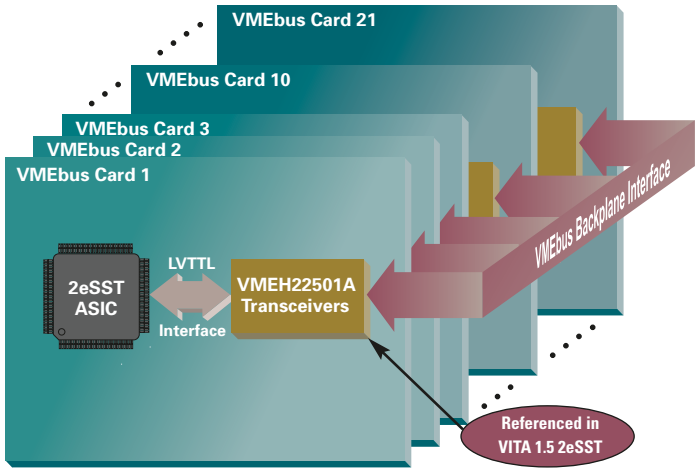
The VMEbus has served the market well for more than 20 years. Each process improvement has been compatible with previous versions, allowing for longevity of the technology. The latest transfer protocol, two edge source synchronous transfer (2eSST), has an achievable performance of 320 Mbps. The SN74VMEH22501A is the only logic transceiver in the industry today that can transmit clean signals at 2eSST speeds down a standard VMEbus.

Key Features

- Backward-compatible existing logic can be used where older backplane technologies such as ABT, ABTE and LVT are still present. New cards can use VME technology while the rest of the backplane remains unchanged.
- V_{CC} = 3.3 V, most popular supply voltage in the industry
- Output edge control reduces electromagnetic interference (EMI)
- Pseudo-ETL input thresholds improve noise margins over traditional logic such as ABTE
- 5-V-tolerant I/Os
- Bus hold eliminates the need for pull-up/down resistors when bus is idle
- Series-damping resistors improve ground bounce on the 3A port and Y outputs
- Flow-through architecture facilitates printed circuit board layout
- Multiple ground and supply pins minimize high-speed switching noise
- 64-mA I_{OL} specification permits backward compatibility to older VMEbus pull-up termination for open-drain outputs

Applications

- Industrial controls
- High-performance network systems
- Telecommunications
- Simulation
- Office automation
- Instrumentation systems



Typical VMEbus interface application.

16-Bit Buffer/Driver with 3-State Outputs
SN74ALVC16244A, SN74LVC16244A

Get samples and datasheets at: **www.ti.com/sc/device/SN74ALVC16244A** and **www.ti.com/sc/device/SN74LVC16244A**

Ideal for base station and networking applications, both the LVC and ALVC families of logic technologies offer solutions for speed-critical 3.3-V system designs. The LVC family is a high-performance version with 0.8-µ CMOS process technology. With typical propagation delays of less than 2 ns, ALVC provides 24 mA of current drive and static power consumption.

Key Features

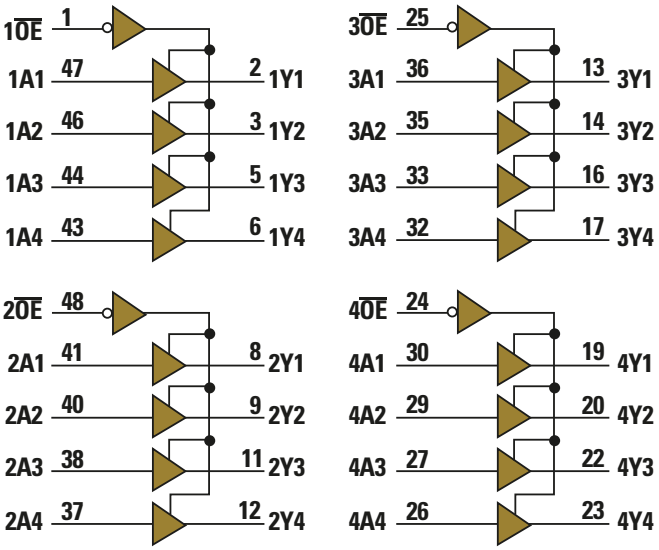
- 3.6 ns max t_{pd} at 3.3 V (ALVC)
- 5.2 ns max t_{pd} at 3.3 V (LVC)
- I_{off} circuitry (LVC)
- Packaging: BGA

Applications

- Base stations
- Networking

ALVC Parameters

Parameter	SN74ALVC16244A
Voltage nodes (V)	3.3, 2.7, 2.5, 1.8
V_{CC} range (V)	2.3 to 3.6
Input level	LVTTL
Output level	LVTTL
Output drive (mA)	–24/24
t_{pd} (ns) (max)	3.6
Static current	0.04



Pin numbers shown are for the DGG and DL packages.

SN75ALVC16244A logic diagram (positive logic).

Low-Voltage Quadruple-FET Bus Switch
SN74CBTLV3125

Get samples and datatsheets at: **www.ti.com/sc/device/SN74CBTLV3125**

The CBTLV family of bus switches operates at the low-voltage 3.3-V operating node. These high-speed, bus-connect devices benefit designs with greater system speed and reduced power consumption. The SN74CBTLV3125 quadruple-FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE\) input is high.

Key Features

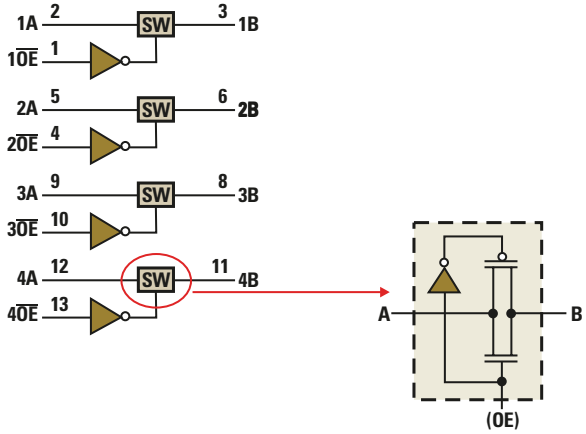
- Standard SN74CBTLV3125-type pinout
- 5-Ω switch connection between two ports
- Isolation under power-off conditions
- Latch-up performance exceeds 100 mA per JESD 78, Class II

Applications

- Base stations
- Networking

CBTLV3125 Parameters

Parameter	SN74CBTLV3125
Voltage nodes (V)	3.3, 2.5
V_{CC} range (V)	2.3 to 3.6
No. of bits	4
r_{on} (Ω) (max)	7
t_{pd} (ns) (max)	0.25



SN74CBTLV3125 block diagram.

SN74CBTLV3125 Bus Switches

Device	Package	Pins	Temp (°C)	Pack Quantity	Price*
SN74CBTLV3125D	D	14	–40 to 85	50	0.81
SN74CBTLV3125DBQR	DBQ	16	–40 to 85	2500	0.81
SN74CBTLV3125DGVR	DGV	14	–40 to 85	2000	0.81
SN74CBTLV3125DR	D	14	–40 to 85	2500	0.81
SN74CBTLV3125NSR	NS	14	–40 to 85	2000	0.88
SN74CBTLV3125PWR	PW	14	–40 to 85	2000	0.81

**Suggested resale price in U.S. dollars in quantities of 1,000.*

ALVC Buffer/Drivers

Device	Package	Pins	Temp (°C)	Pack Quantity	Price*
SN74ALVC16244ADGGR	DGG	48	–40 to 85	2000	1.12
SN74ALVC16244ADL	DL	48	–40 to 85	25	1.12
SN74ALVC16244ADLR	DL	48	–40 to 85	1000	1.12
SN74ALVC16244AGQLR	GQL	56	–40 to 85	1000	1.23

**Suggested resale price in U.S. dollars in quantities of 1,000.*

LVC Products

Device	Package	Pins	Temp (°C)	Pack Quantity	Price*
SN74LVC16244ADGGR	DGG	48	–40 to 85	2000	1.01
SN74LVC16244ADGVR	DGV	48	–40 to 85	2000	1.01
SN74LVC16244ADL	DL	48	–40 to 85	25	1.01
SN74LVC16244ADLR	DL	48	–40 to 85	1000	1.01
SN74LVC16244AGQLR	GQL	56	–40 to 85	1000	1.12

**Suggested resale price in U.S. dollars in quantities of 1,000.*

GTLP Transceivers

Device	Description	Price*
SN74GTLP1394	2-bit LVTTL-to-GTLP adjustable-edge-rate bus Xcvr with split LVTTL port, feedback path and selectable polarity	2.53
SN74GTLP1395	Two 1-bit LVTTL/GTLP adjustable-edge-rate bus Xcvrs with split LVTTL port, feedback path and selectable polarity	2.75
SN74GTLP2033	8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path	6.05
SN74GTLP2034	8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path	6.05
SN74GTLP21395	Two 1-bit LVTTL/GTLP adjustable-edge-rate bus Xcvrs with split LVTTL port, feedback path and selectable polarity	2.75
SN74GTLP22033	8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path	6.05
SN74GTLP22034	8-bit LVTTL-GTLP adjustable-edge-rate registered transceiver with split LVTTL port and feedback path	6.05
SN74GTLP817	GTLP-to-LVTTL 1-to-6 fanout driver	2.63
SN74GTLPH1612	18-bit LVTTL-to-GTLP adjustable-edge-rate universal bus transceiver	6.38
SN74GTLPH1616	17-bit LVTTL-to-GTLP adjustable-edge-rate universal bus transceiver with buffered clock outputs	6.38
SN74GTLPH1627	18-bit LVTTL-to-GTLP bus Xcvr with source synchronous clock outputs	5.63
SN74GTLPH1645	16-bit LVTTL-to-GTLP adjustable-edge-rate bus transceiver	3.85
SN74GTLPH1655	16-bit LVTTL-to-GTLP adjustable-edge-rate universal bus transceiver	6.38
SN74GTLPH16612	18-bit LVTTL-to-GTLP universal bus transceiver	4.95
SN74GTLPH16912	18-bit LVTTL-to-GTLP universal bus transceiver	4.90
SN74GTLPH16916	17-bit LVTTL-to-GTLP universal bus transceiver with buffered clock outputs	5.25
SN74GTLPH16945	16-bit LVTTL-to-GTLP bus transceiver	3.96
SN74GTLPH306	8-bit LVTTL-to-GTLP bus transceiver	3.96
SN74GTLPH3245	32-bit LVTTL-to-GTLP adjustable-edge-rate bus transceiver	5.83
SN74GTLPH32912	36-bit LVTTL-to-GTLP universal bus transceiver	7.50
SN74GTLPH32916	34-bit LVTTL-to-GTLP universal bus transceiver with buffered clock outputs	7.50
SN74GTLPH32945	32-bit LVTTL-to-GTLP bus transceiver	4.95

**Suggested resale price in U.S. dollars in quantities of 1,000.*

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