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Semiconductor Wafer Test Workshop

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New Directions In Parametric and Defect Structure Testing

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V93k pA Project

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IBM Inline Test Parallel Test Team

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Outline

- **Motivation: Challenges of monitoring variability moving to 22 nm.**
- **Improving the test process:**
  - Parallel test of parametric macros.
  - Use of array based diagnostics.
  - Improving tester utilization.
  - **Developing the tools required to meet these challenges.**
- **pA Metrology.**
- **Summary.**

Variability Challenges at 22 nm and Beyond

- Spreads in basic parameters (like V_t) are becoming worse. Larger statistics are required.
- Test time for process monitoring can't grow.
- The manufacturing process must be economically viable.

- Need to improve test efficiency *(what is tested; how we test) :*

IBM 300 mm Manufacturing Facility, East Fishkill N.Y.

Improving Process Metrology and Test Efficiency

- **Standard Parametric Structures: (Simple macros wired directly to a 1x25 pad cage).**
  - Business as usual, but test lots of them.
  - Test many in parallel instead of serially.

- **Array Based Parametric Diagnostics.**
  - Take advantage of an addressable multiplexer structure to access large numbers of test cells.
  - Requires components of both digital and analog test systems.

- **Array Based Digital (Defect)**
  - Use on chip electronics and memory like structure to test large numbers of cells quickly.
  - Pass / Fail test which uses digital read out circuitry on chip and is fast.

Traditional In Line Test

- **Standard Parametric**
  - Individual transistors.
  - Serps/Combs.
  - CV, CBCM.
  - PSRO.

- **Array Based Parametric Diagnostics (APDs)**
  - Deep statistics on basic process parameters like CA contact resistance, V_t variability.

- **Array Based Digital**
  - Defect monitors.
  - SRAM.

Agilent 4073: ~ 6 SMUs

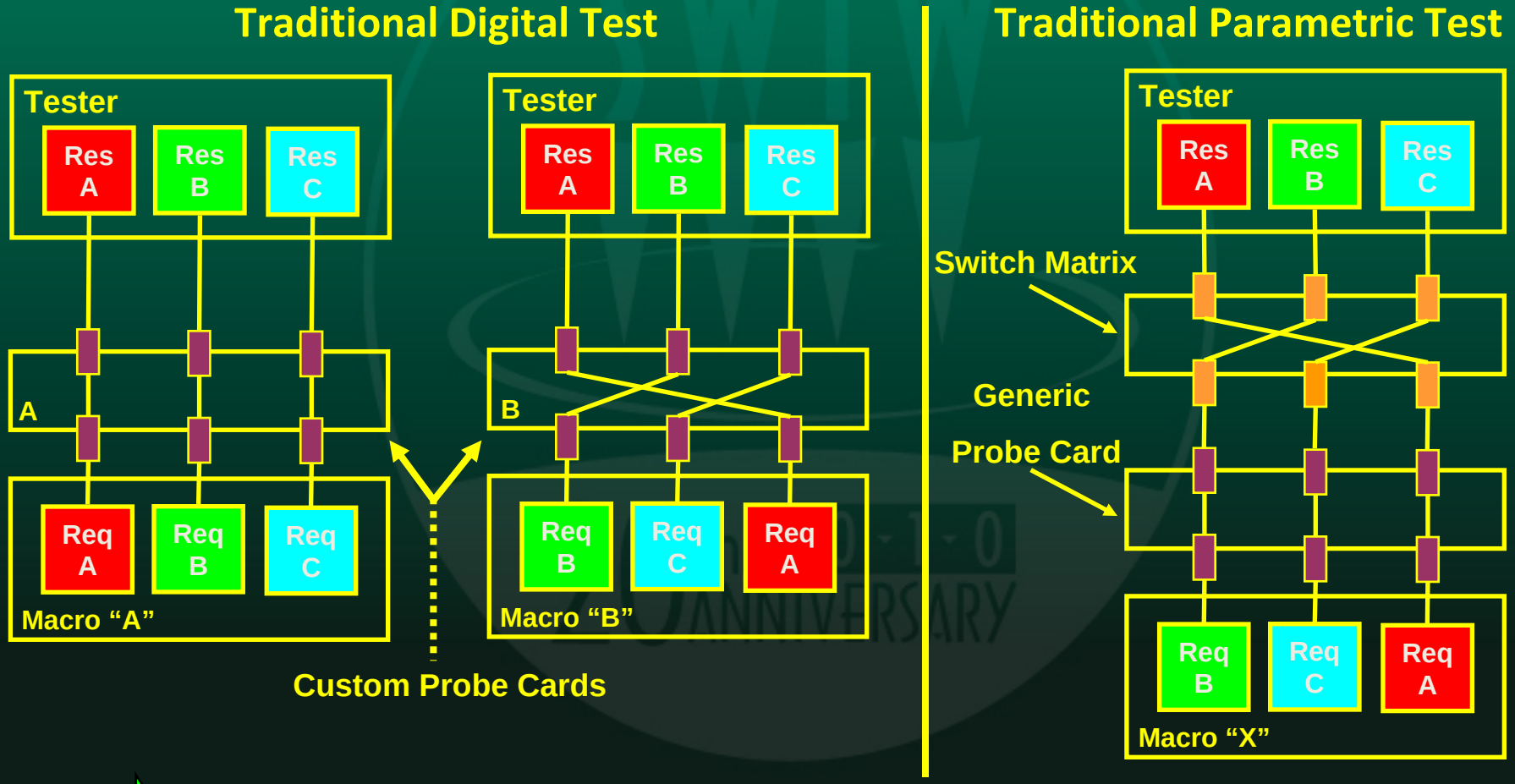
Verigy 93k: ~1024 Pins

Lessons From Memory Test: Parallelism

Multi-DUT Test Systems

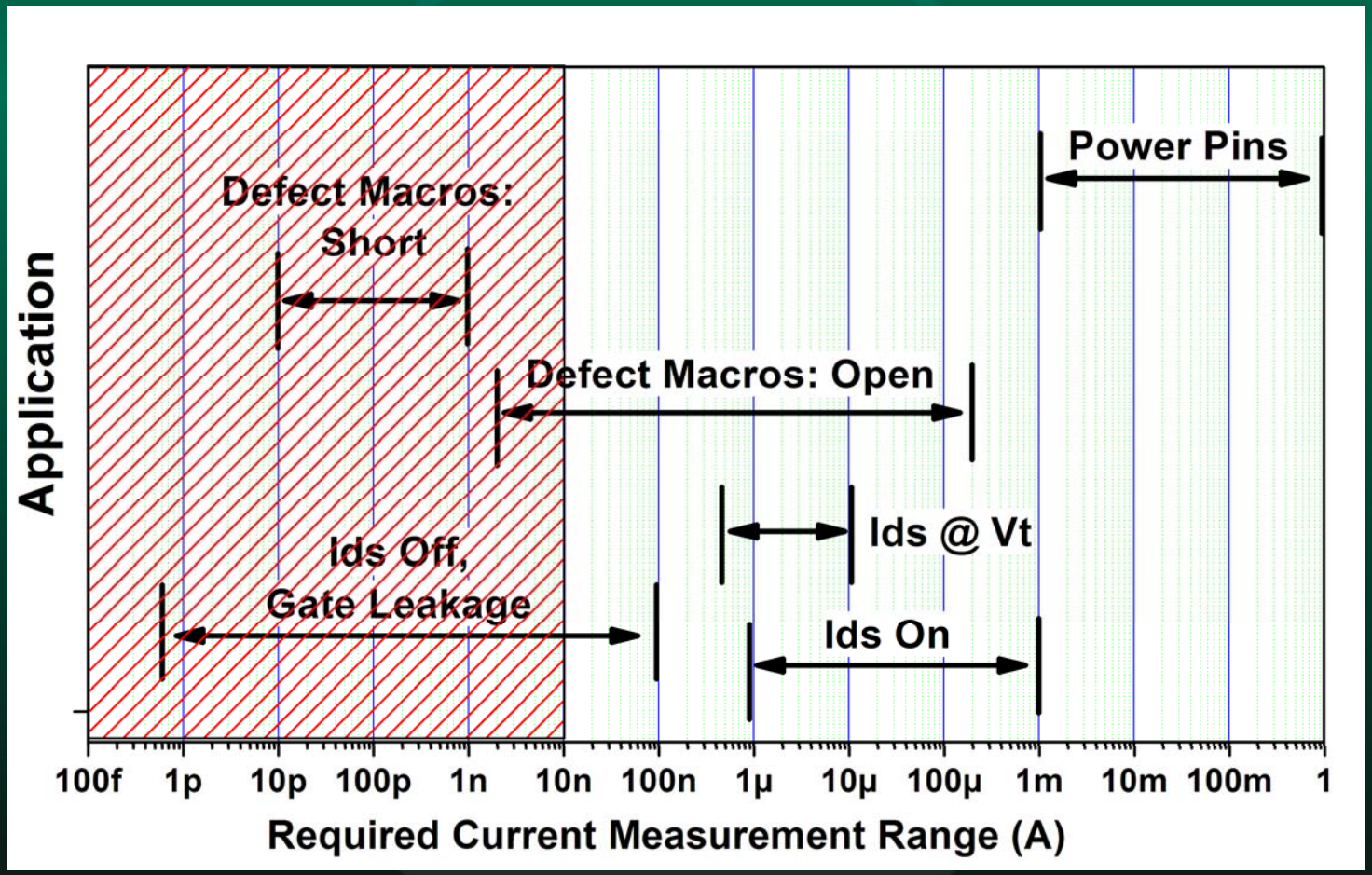
Massive test parallelism improves efficiency, drives down cost.

Lessons From Parametric Test: Software Configurable Interface



Any pin / any function greatly simplifies interfacing to DUT.

Current Measurement Range vs. Test Application



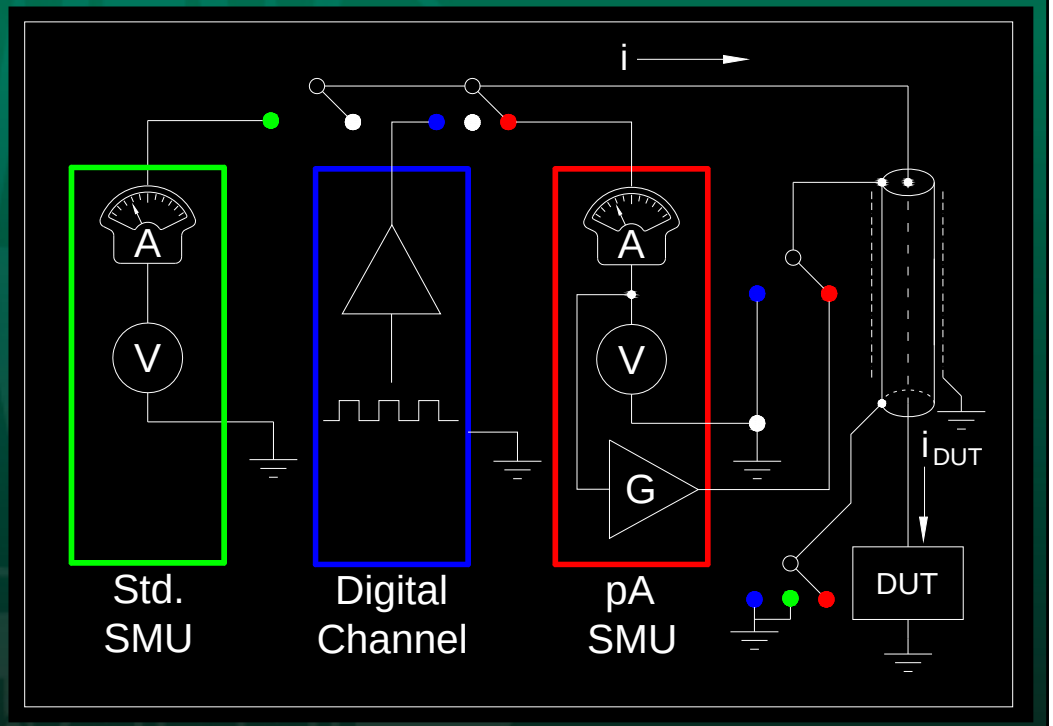
- Active and passive device characterization spans many orders of magnitude in current measurement.
- Current levels below **10nA** require specialized SMUs.

Hybrid Tester

- **Typical digital ATE pin channels possess many of the requirements for parallel test of standard parametric macros, as well as array based and all digital.**
  - Per pin Source Measurement Unit (SMU).
  - Digital I/O capable.

— BUT —

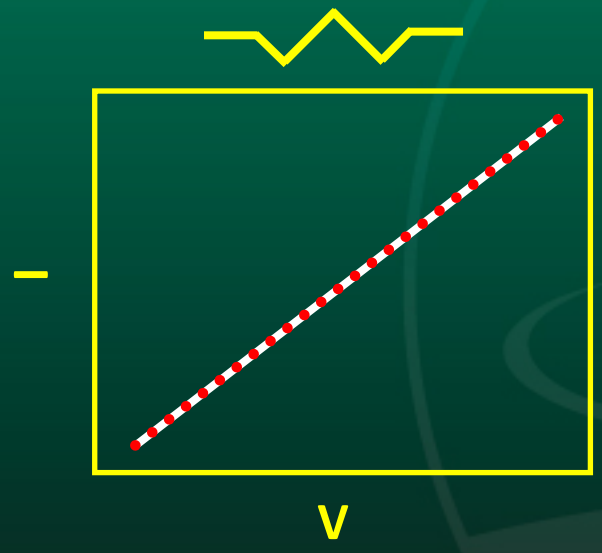
- **Low end current measurement range (~10 nA) insufficient for some active and passive parametric tests.**
- **Enabling full spectrum of active and passive device characterization requires adding an SMU resource with measurement resolution ~1pA**
- **System Noise level must also be low enough for level of metrology required.**



One Channel of Pin Electronics

Devices: Effects of Noise

Resistor, Linear

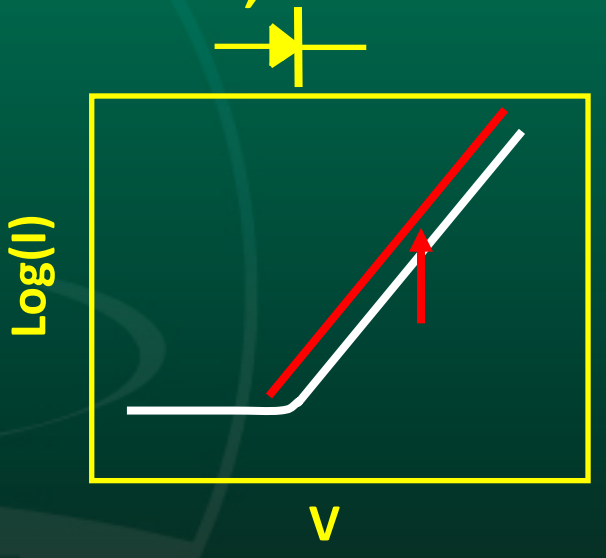


- **Linear IV curve.**
- **Noise from SMU will average to zero effect on IV over enough acquisition cycles.**

Transistor

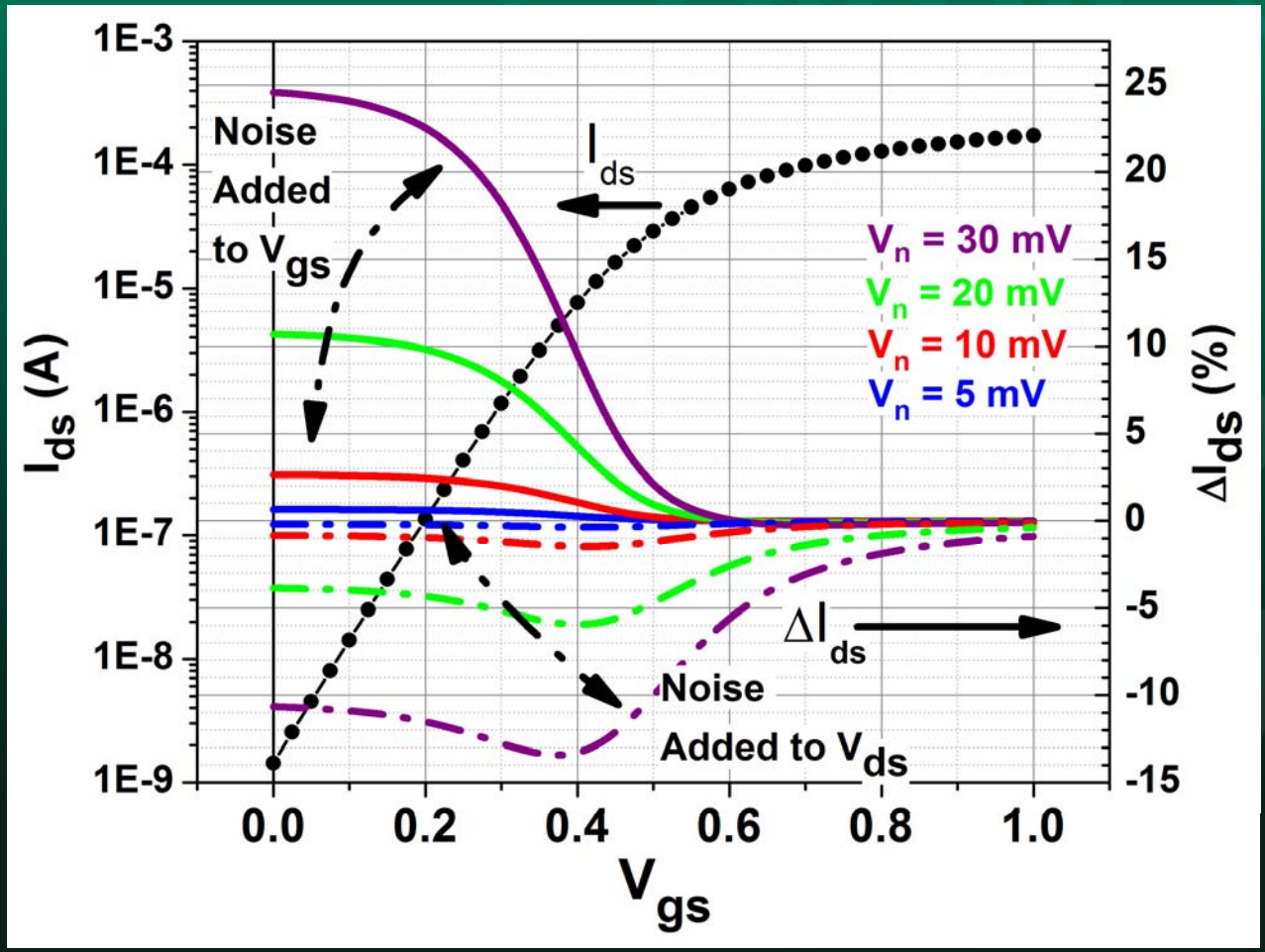
Transistor IV will be affected differently at different bias points, depending on whether the IV looks linear, or nonlinear.

Diode, Nonlinear



- **IV curve is nonlinear, except in constant current reverse saturation region.**
- **Noise from SMU will be rectified, shift IV to higher currents.**

NFET IV In Presence of Noise



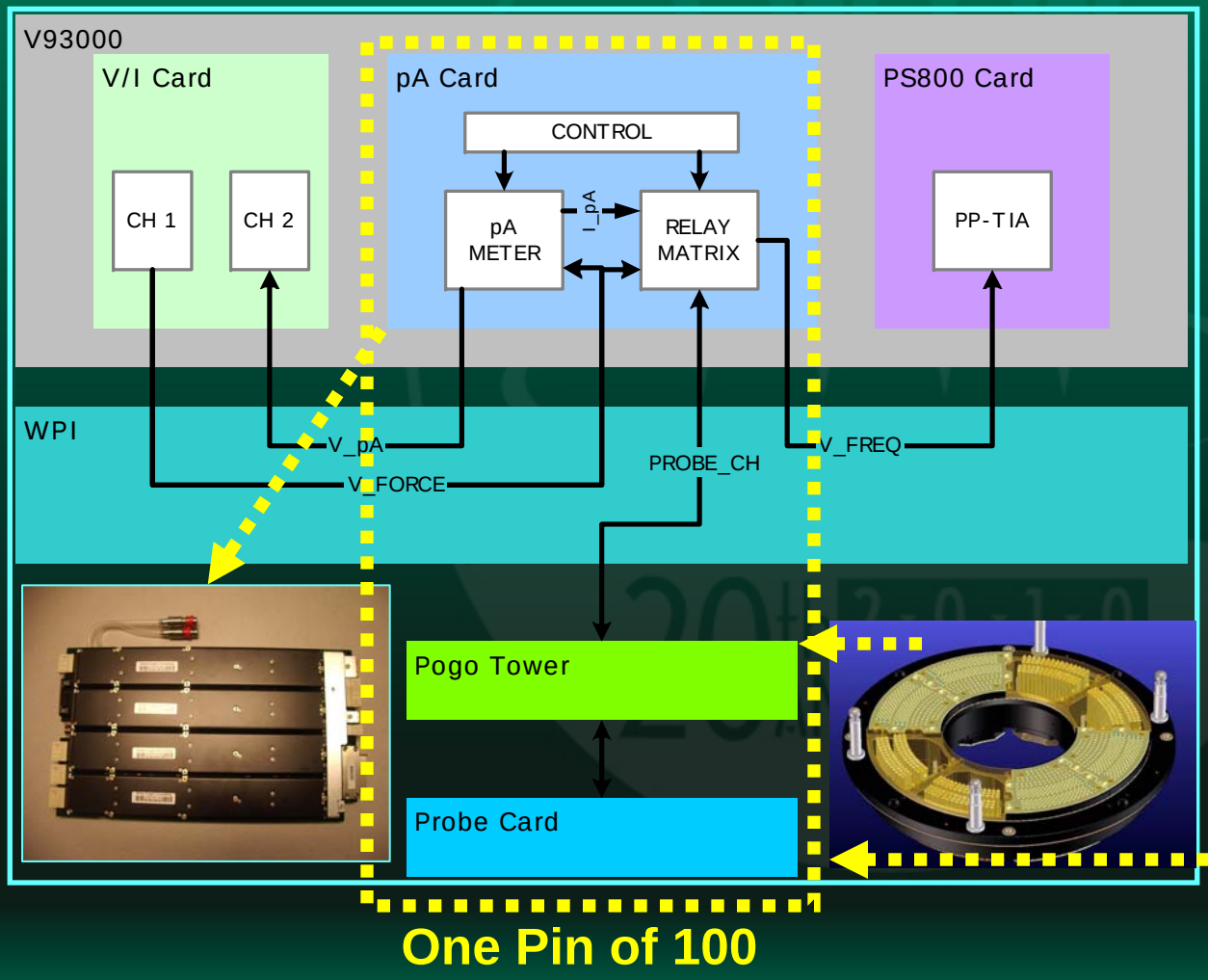
- Noise on SMUs which establish GND, VGS, or VGS will effect the IV curve.
- Magnitude of the noise term depends strongly on the bias point on the IV.
- Noise effects are minimal where the device looks linear; most pronounced in regions of nonlinear response (sub-threshold).

Implementation

- **Verigy 93k SOC base tester platform.**
  - PS800 digital pin electronics.
  - VI/32 SMU for current range I_m > 200 nA.
- **Newly developed** pA SMU **for current range I_m > 5 pA.**
- **Low leakage switch matrix enabling steering any tester resource to any of 100 pins.**
- **Low leakage interface enabling current measurements down to pA levels.**
- **Complete integration of all system resources with standard tester software.**

Verigy 93k

93k DC-Parallel Test Cell



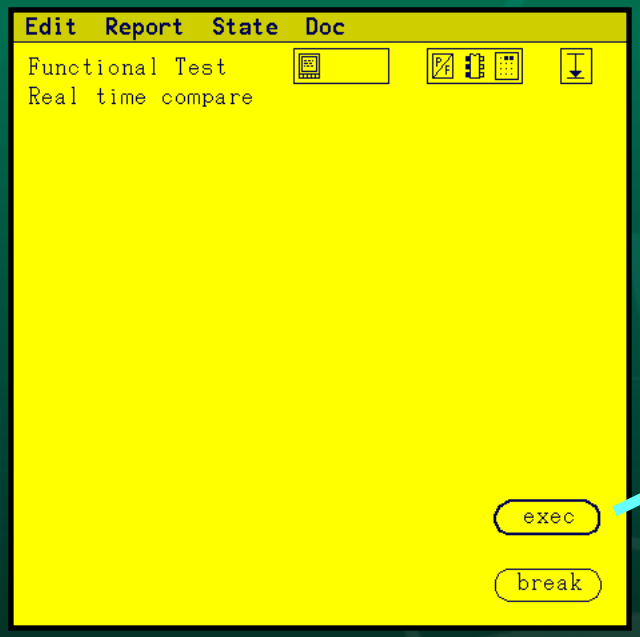
- **pA electronics architecture.**
  - V/I used to set voltage and read I/V converter output.
  - High degree of parallelism in data acquisition, and switch matrix control.
- **Typical data acquisition time 100 ms.**
- **Signal path tightly guarded and air wired inside module.**
- **Pogo tower and cable critical to low noise in a high vibration environment.**

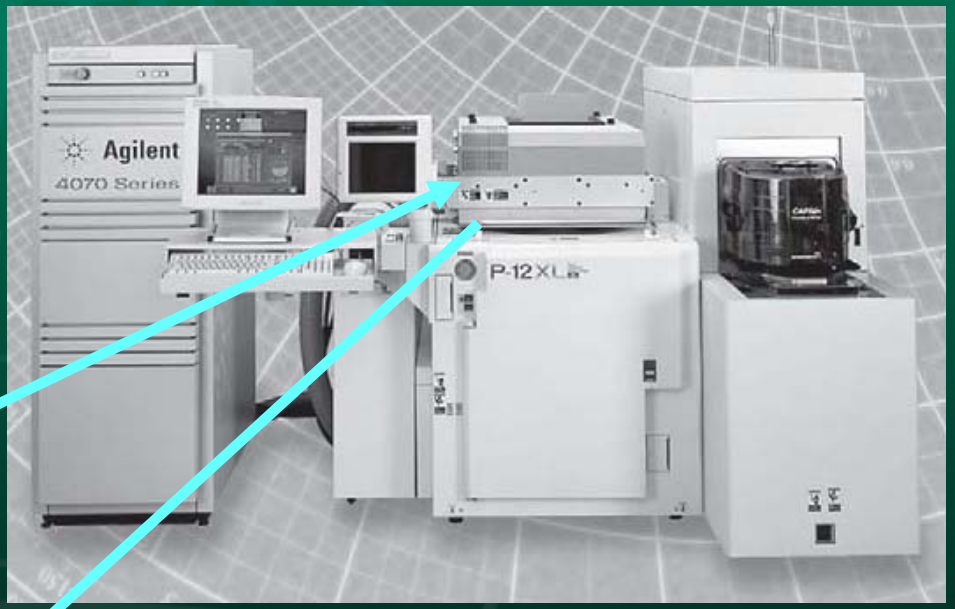
Newly Developed

Validation

- **In the hardware business, test equipment is our compass.**

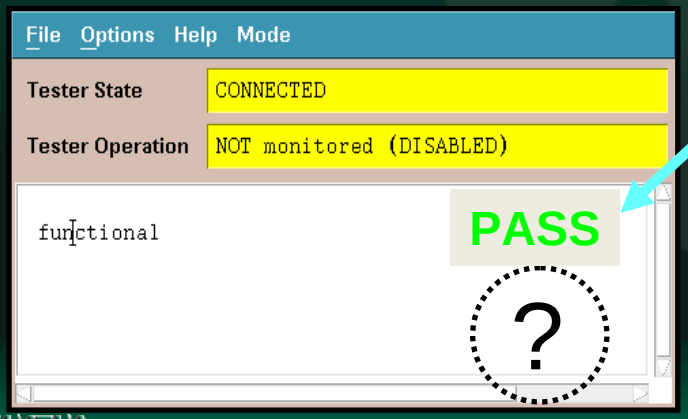
A Question of Faith





Test

Result

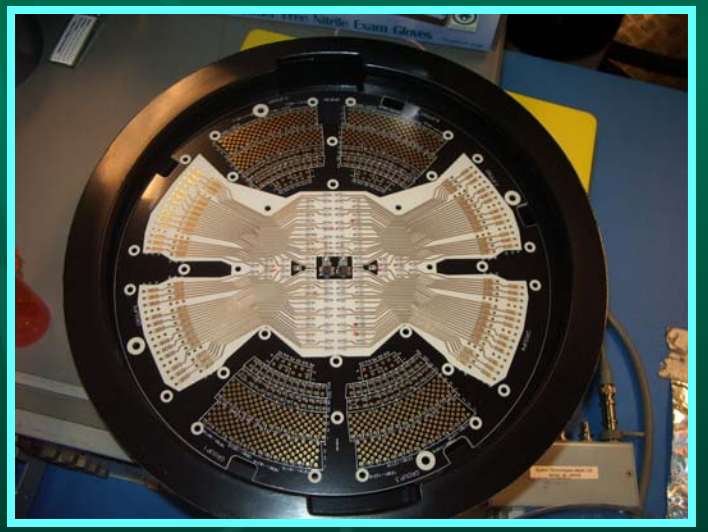


- Large ATE systems provide the means to execute complex tests with great efficiency.
- However, the details of the test process are inherently difficult to observe.

Validation Methodology

1. **Validation load board (VLB).**
   - 40MΩ and 4GΩ load boards, 1 load / channel (100 resistors / board).
   - Resistors are calibrated at Verigy's Cupertino facility.
   - IV curves of the VLB are then compared to measured values on a point by point (typically 18 voltages from -1 to +7.5V).

   No Observability.

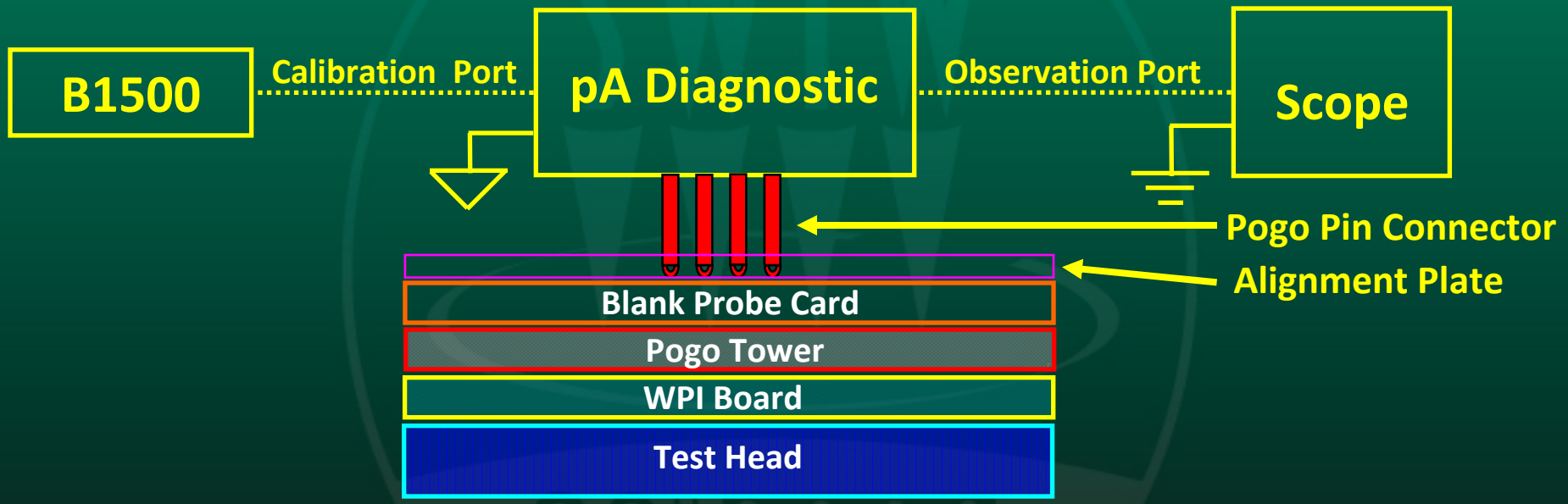


2. **pA Diagnostic instrument.**

   Adds observation points.

3. **Verigy NIST traceable calibration instrument.**
4. **Correlation of wafer data from 4073 parametric tester.**
   - e.g., V_t correlation.

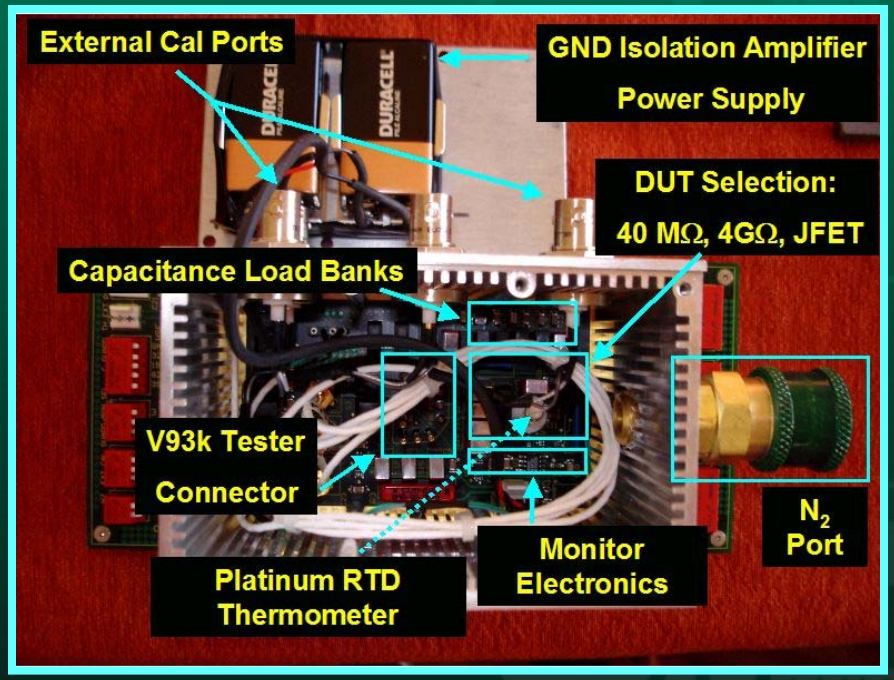
pA Diagnostic Instrument



- **pA diagnostic**
  - One selectable precision load used to measure each channel (40 MΩ, 4 GΩ, PN junction or N channel JFET).
  - Voltage monitors for DUT, and guard **(Observability).**
  - Ability to stress measurement and guard channels with large capacitive loads.
  - Direct, simple calibration with B1500 or Agilent 4073 provides absolute NIST traceability.

pA Metrology

Instrument Details

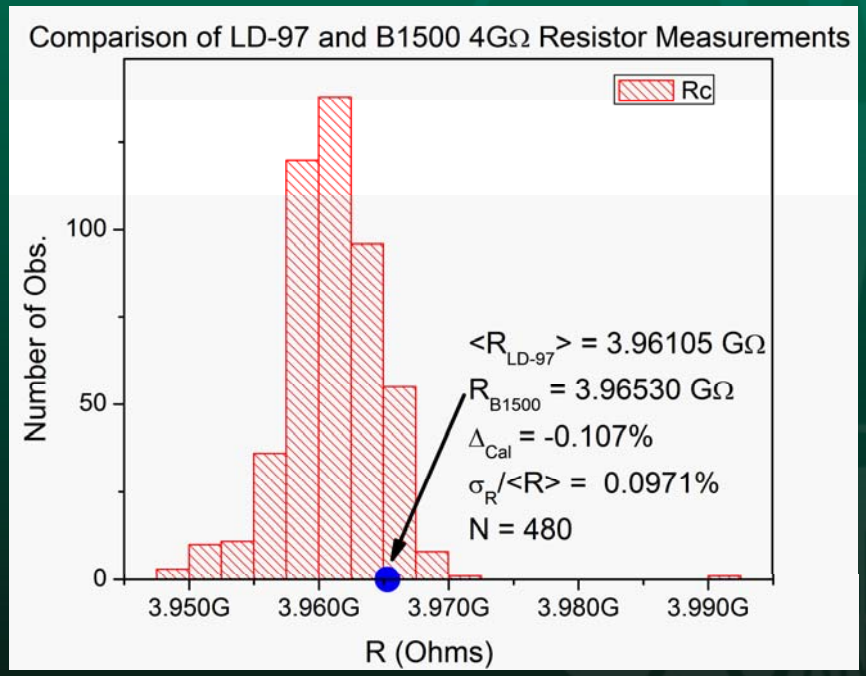


Parallel Tester Characterization

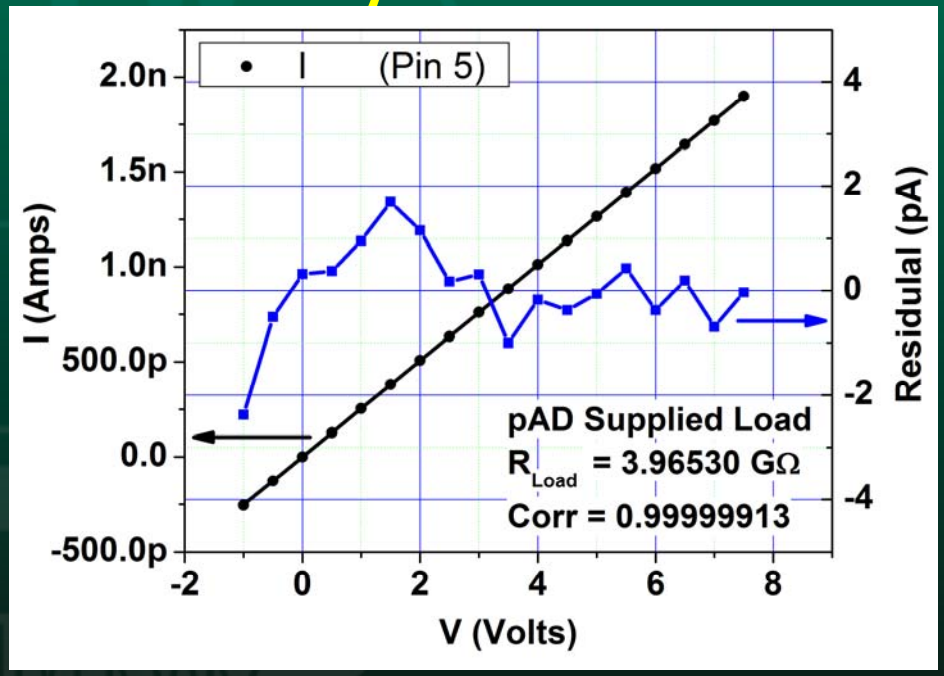
• pA diagnostic enables trouble shooting channels and direct channel to channel comparison with NIST traceable loads.

Linear Validation

4GΩ Resistor Measurement



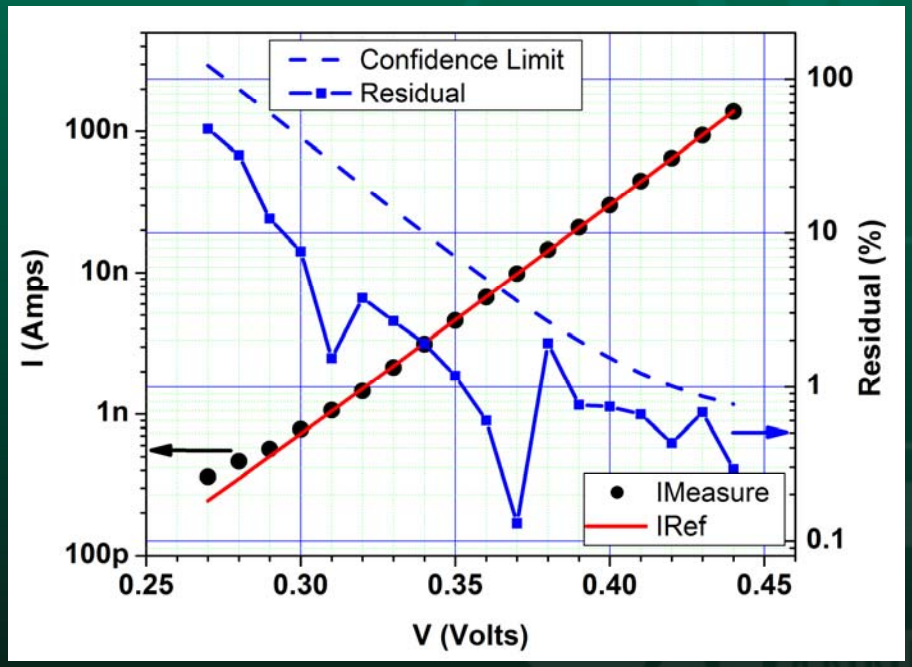
Linearity Measurement



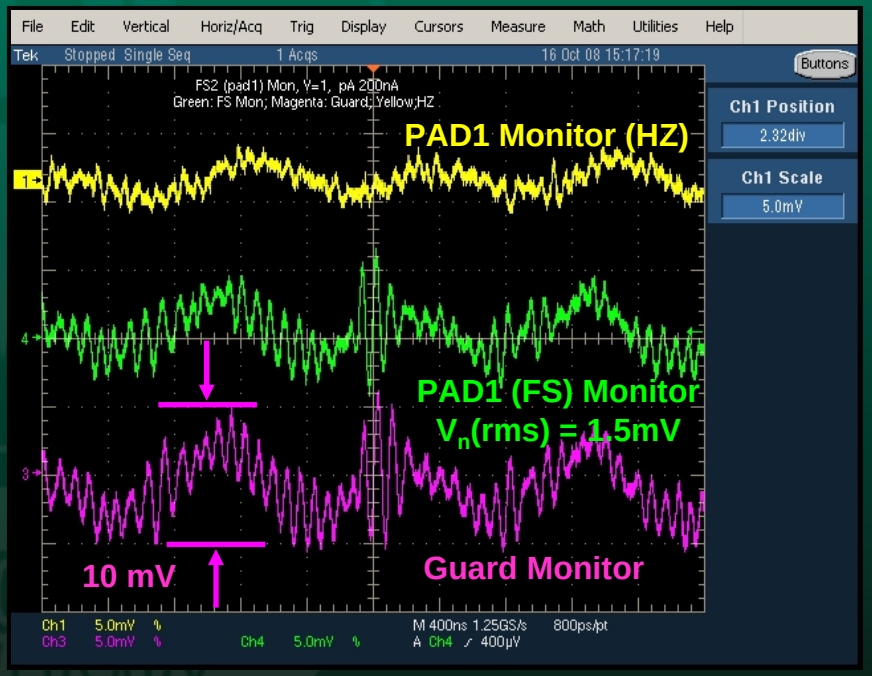
- pA SMU, 2 nA range, 100 ms settling time.
- 48 channel median calibration resistor measurement deviates from B1500 measurement by less than 0.11 %.

Nonlinear Validation

PN Junction IV

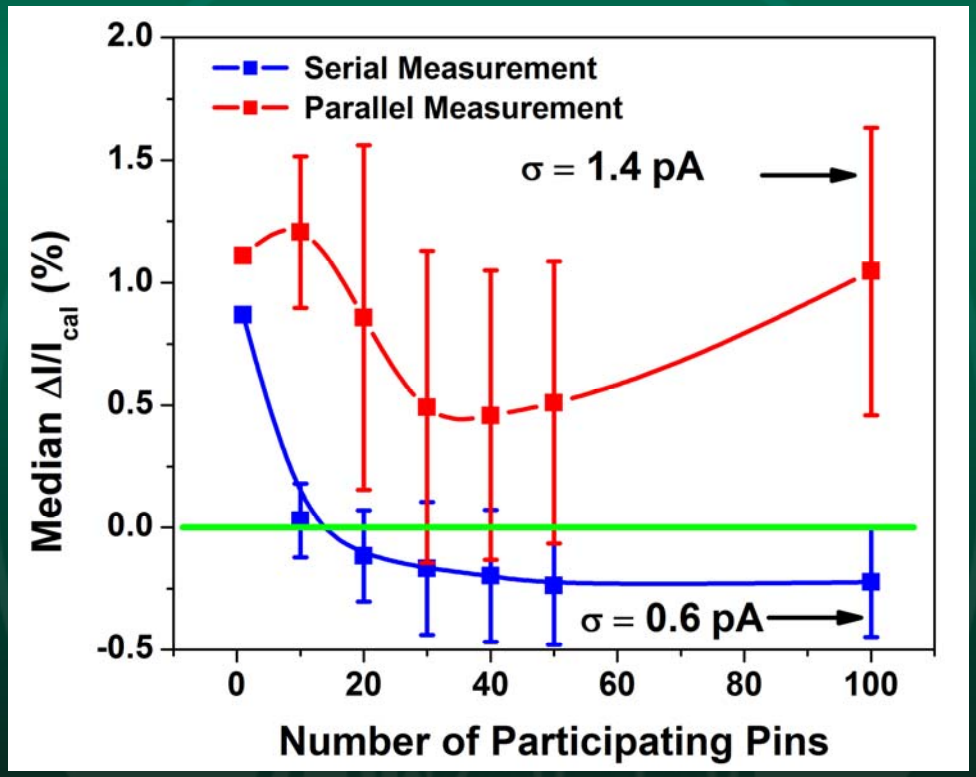


SMU Noise Characterization



- pA SMU, 200 nA range, 100 ms settling time.
- PN junction IV matches B1500 value within SMU spec. accuracy.
- High impedance monitors allow SMU noise characterization without loading SMU or DUT.

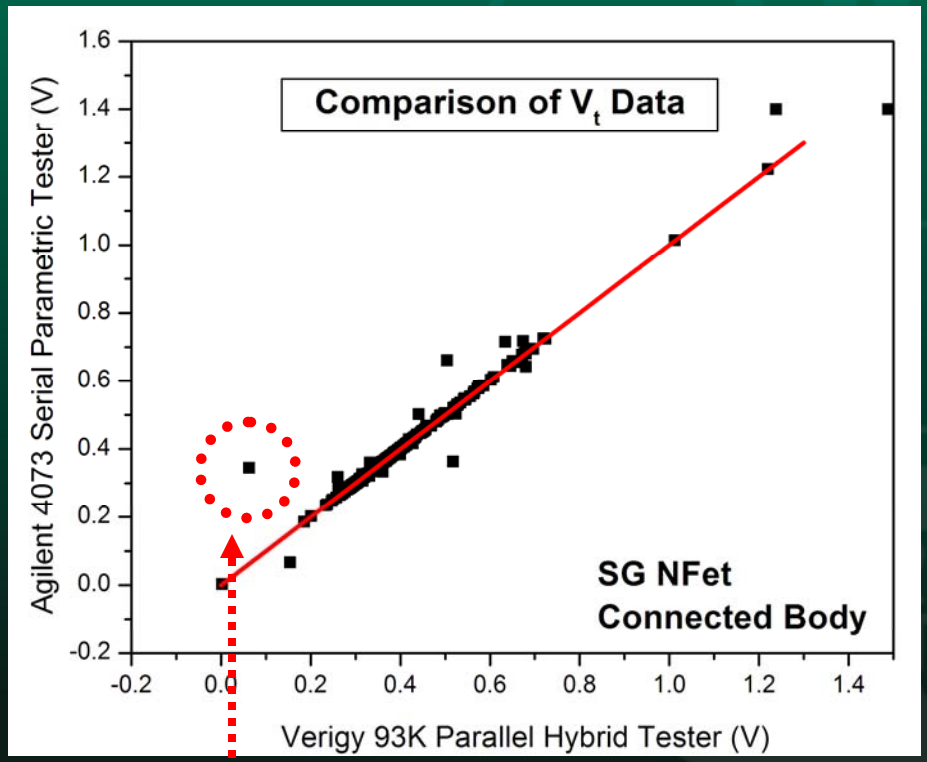
Serial and Parallel Performance



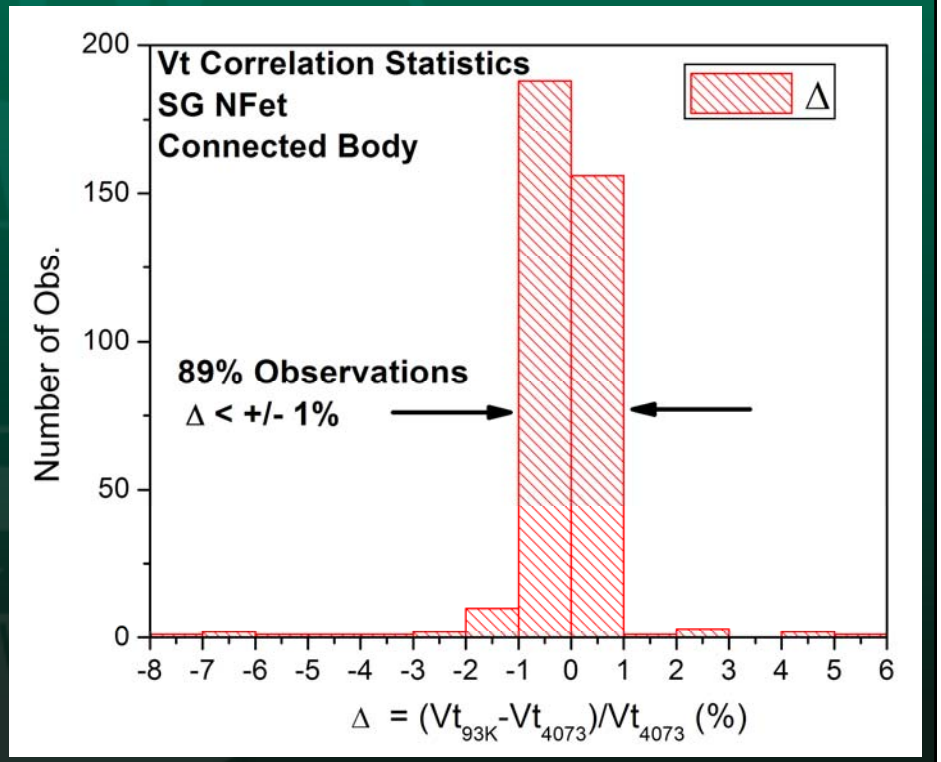
- 1-100 channel VLB measurement, 4GW load, 1V, 250 pA.
- Graph shows median and std. deviation of measurements performed serially and in parallel.
- Full parallel acquisition data demonstrates minimal channel to channel cross coupling (small additional error term ~ 1%, <3 pA) over measurements made serially.

Wafer Vt Correlation Data

Correlation



Statistics



- Wafer correlation work in progress.
- Major focus is elimination of fliers.

Summary

- **Demonstrated hybrid test system capable of parallel parametric measurements down to pA levels.**
  - 100 channel “any pin any function” for test of standard pad cage parametric macros, digital yield macros, and array based parametric macros.
  - All parametric instrumentation (including pA SMU) integrated with standard test system software.
  - NIST traceable calibration and validation infrastructure.
- **Qualified for manufacturing test of defect structures.**
  - 5X throughput improvement demonstrated.
- **Active device qualification experiments in progress.**