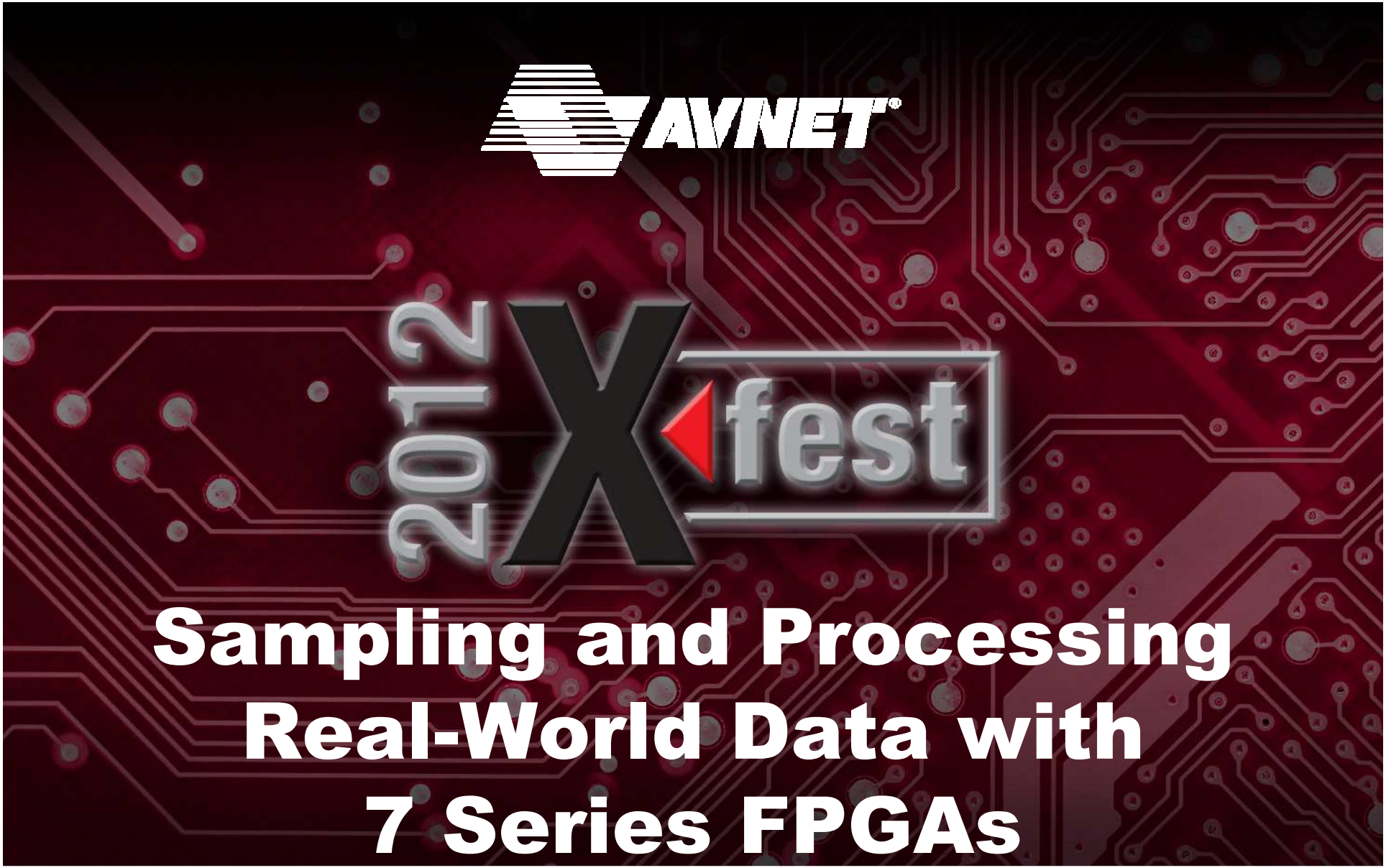

Sampling and Processing Real-World Data with 7 Series FPGAs

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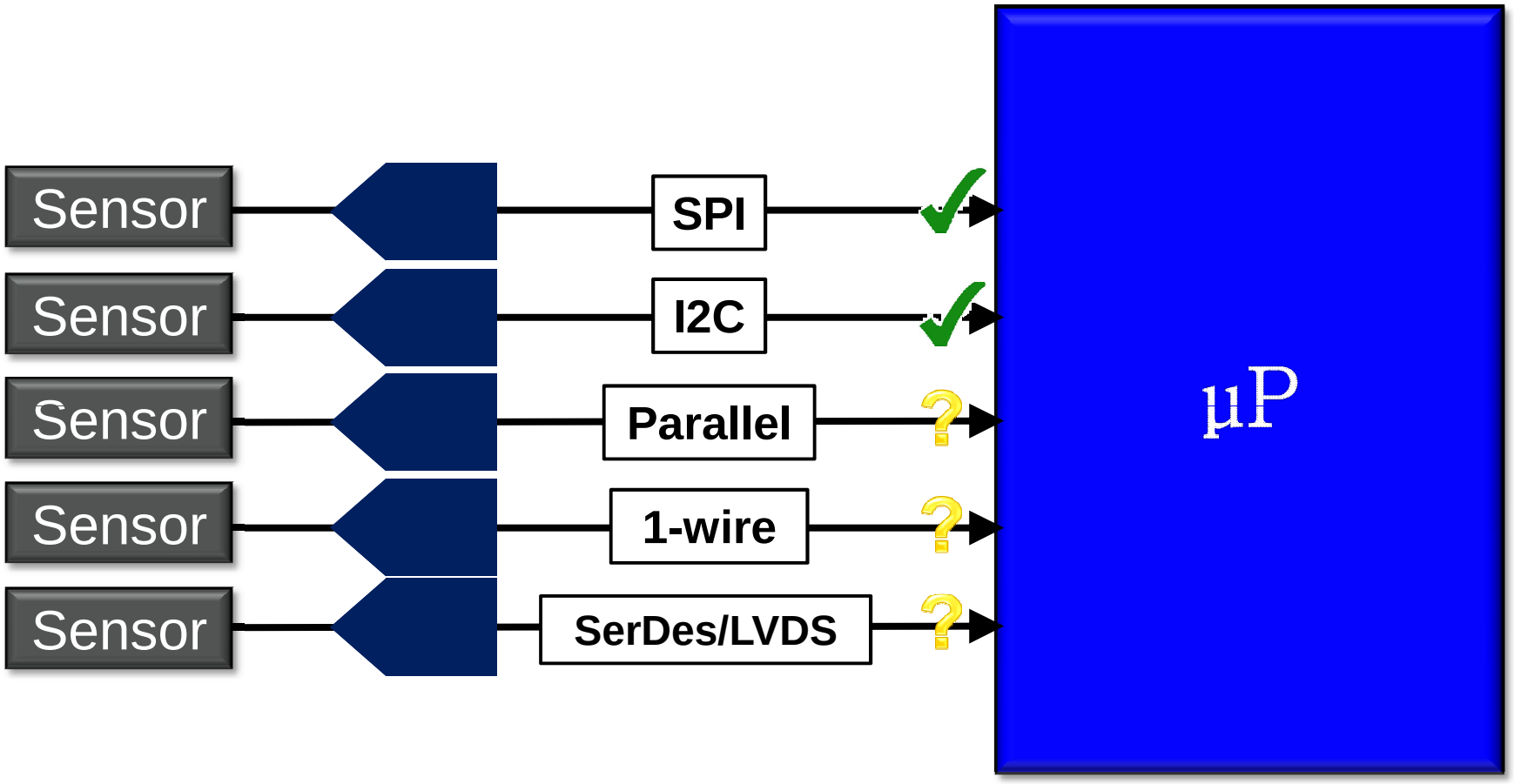
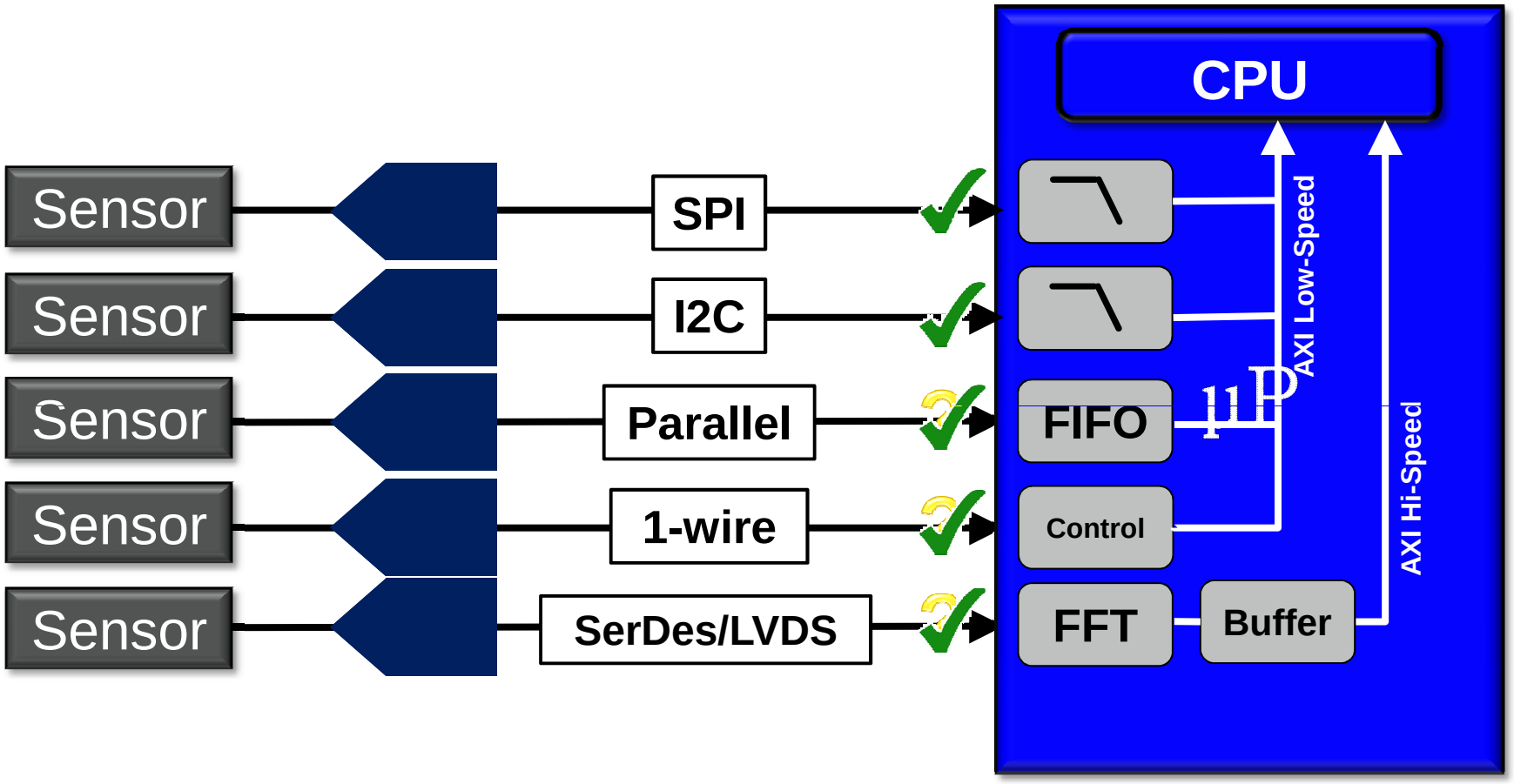
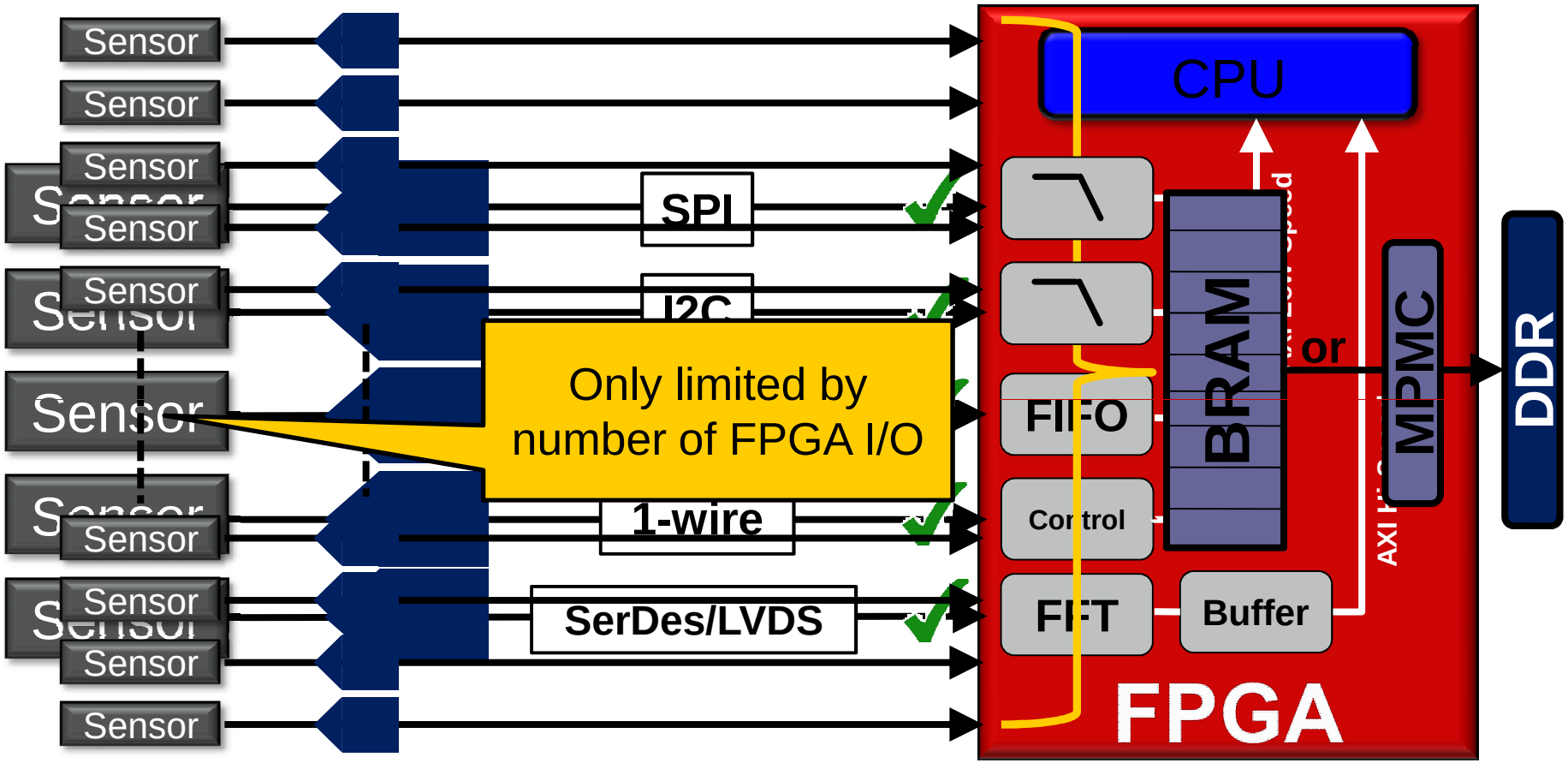
Why an Analog Course at Xfest?



Why an Analog Course at Xfest?



Why an Analog Course at Xfest?



FPGAs offer unmatched system performance and flexibility

Course Objectives

- **Explore complexities in analog signal chain components and learn how digitally controlled Analog Front Ends (AFE) increase design flexibility**
- **Learn how to maximize low and medium performance standalone data converters**
- **Understand capabilities and benefits of XADC component**
- **Accelerate your prototype with Pmods™ and FMC evaluation boards**

Agenda

- **Analog signal chain**
- **Standalone data converter solutions**
- **XADC solution and the customizable analog interface**
- **Prototyping with expansion boards**

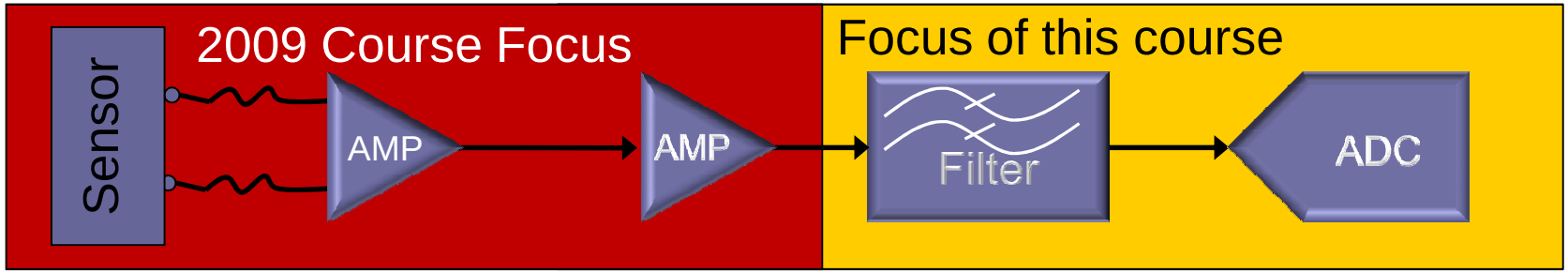
Agenda

- **Analog signal chain**
- Standalone data converter solutions
- XADC solution and the customizable analog interface
- Prototyping with expansion boards

Sampling Real World Data

- **Demand for sensor critical applications is increasing**
  - Often measuring such things as temperature, weight, shock/vibration, air quality and more

- **System designers must design optimal signal path solution for varying sensor types**
  - Sensor types require optimal analog signal chains
  - Covered in 2009 X-fest Analog Course

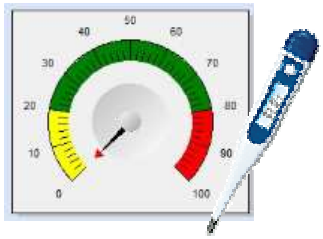


So Many Things to Sample!

- **Sensors require optimal analog interfaces**

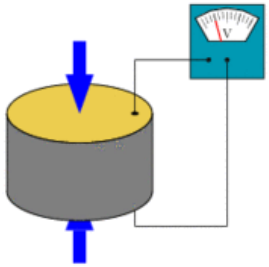
System Monitoring / Temperature Sensing

- Changes in voltage



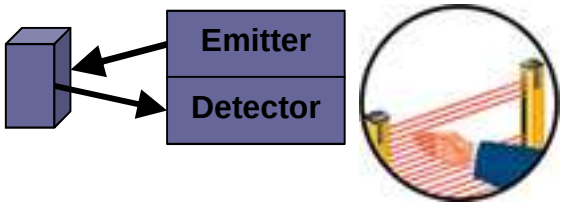
Pressure/Load Force Sensing

- Small changes in resistance or capacitance



Optical Sensing

- Changes in current



Motion Sensing

- Changes in voltage based on magnetic field

Chemical Analysis

- Small changes in current or voltage
- High impedance

Maximizing ADC Performance

- **To achieve maximum ADC performance you must carefully build the analog signal chain!**
  - For example, inputs to SAR ADC's look like dynamic loads, thus amplifier selection is critical
- **It's important to select the right**
  - Input amplifier or buffer
  - Voltage (or current) reference
    - Voltage reference buffer (for multiple ADC systems)

ADC Amplifiers

- **Consult reference material from supplier**
  - ADC's datasheet
  - ADC's website
  - Evaluation board docs
- **Look at the published AC specs for alternatives**
  - Slew rate
  - Forward settling time
  - Reverse settling time
    - Look at output resistance

Choosing the Right Amplifier

- **Pick an op amp that does not degrade the ADC performance**
  - DC performance
    - Offset and offset drift
    - Input bias current
    - Open loop gain
    - Linearity
    - 1/f noise
  - AC performance
    - Noise
    - Distortion
    - Slew rate and settling time
    - Reverse settling time (recovery to ADC transient)

Matching DC performance is straight forward

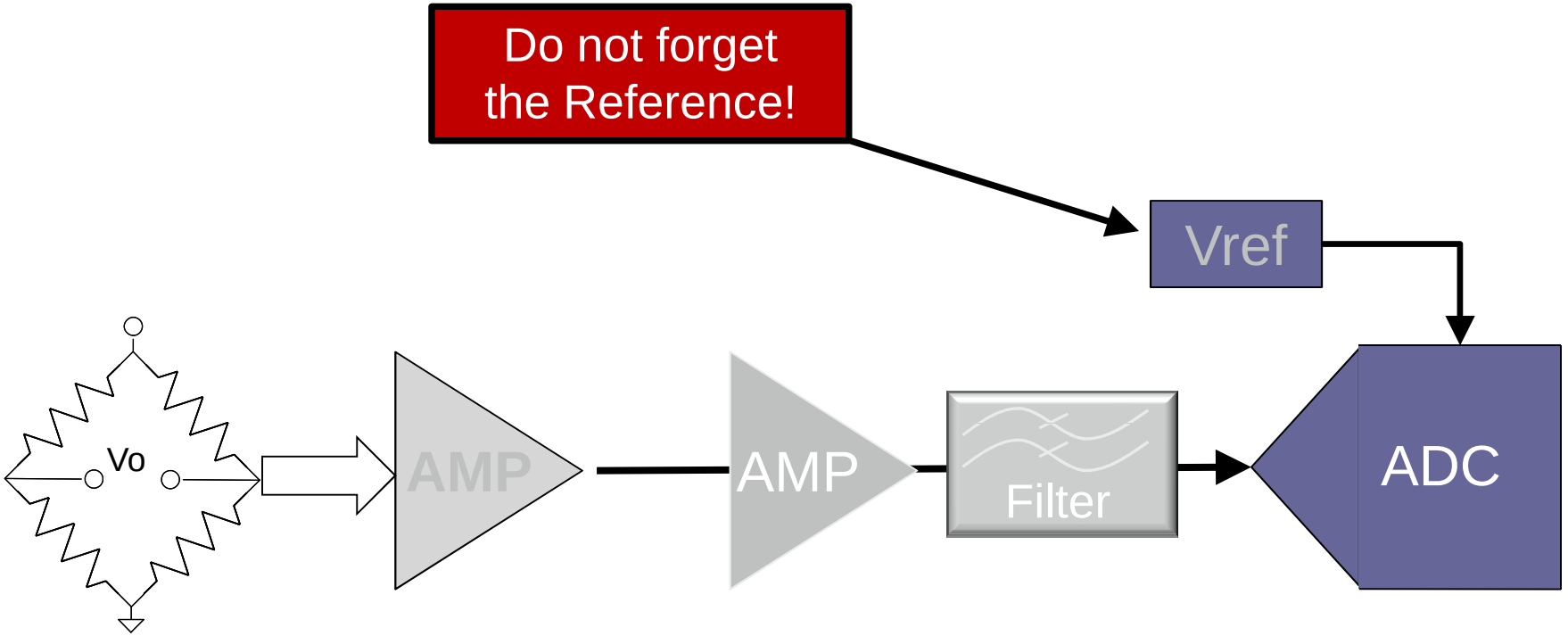
Matching AC performance is challenging

Maximizing AC performance

- **AC performance must be known for the exact circuit configuration used in the ADC driver circuit**
  - Too many possibilities to include in a datasheet
- **Datasheets provide a very good start for selecting candidates**
- **Ultimately the op-amp circuit must be prototyped to measure AC performance**

Evaluation boards provide an easy way to do this

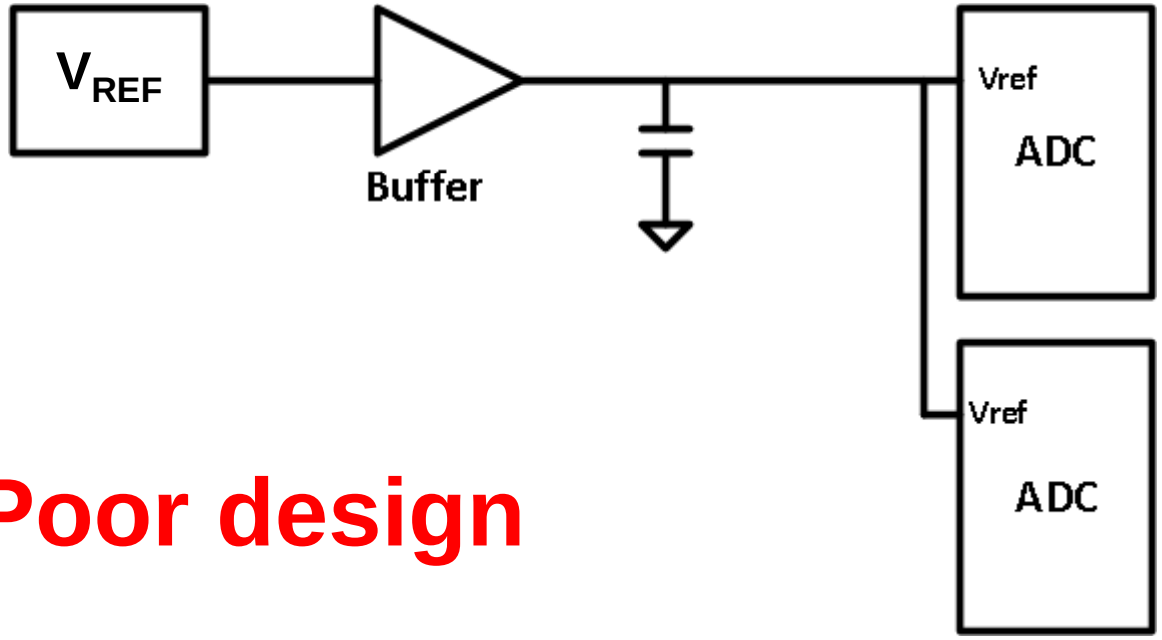
Analog Signal Chain Review



A clean voltage reference is critical as well

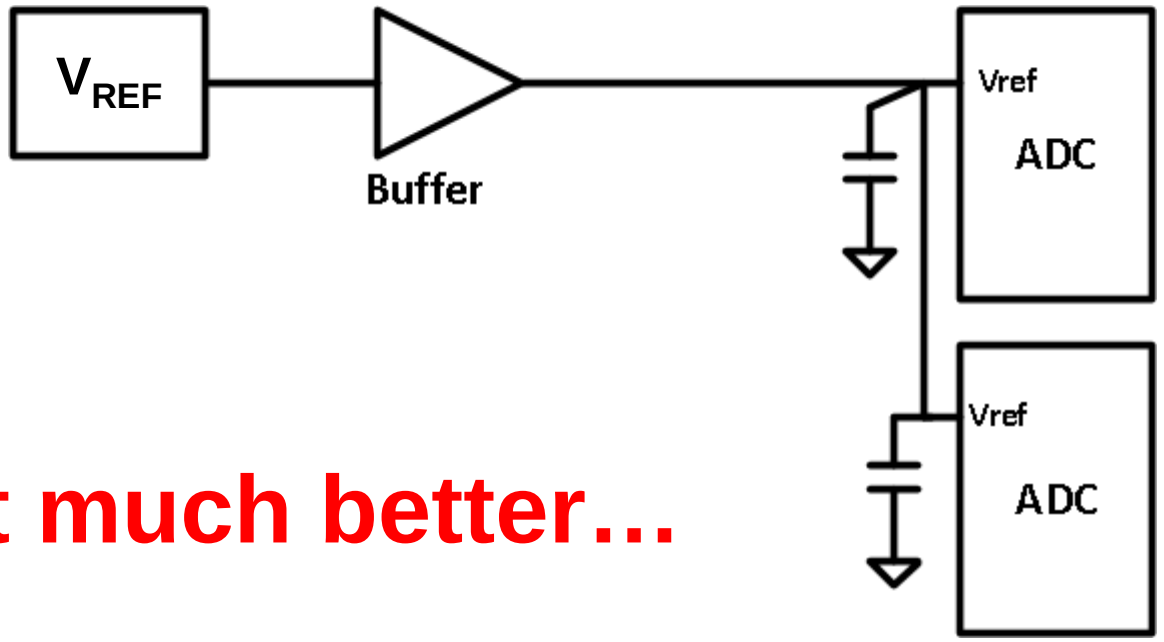
Referencing Multiple ADCs

- **When referencing multiple ADC's, what's the best method?**



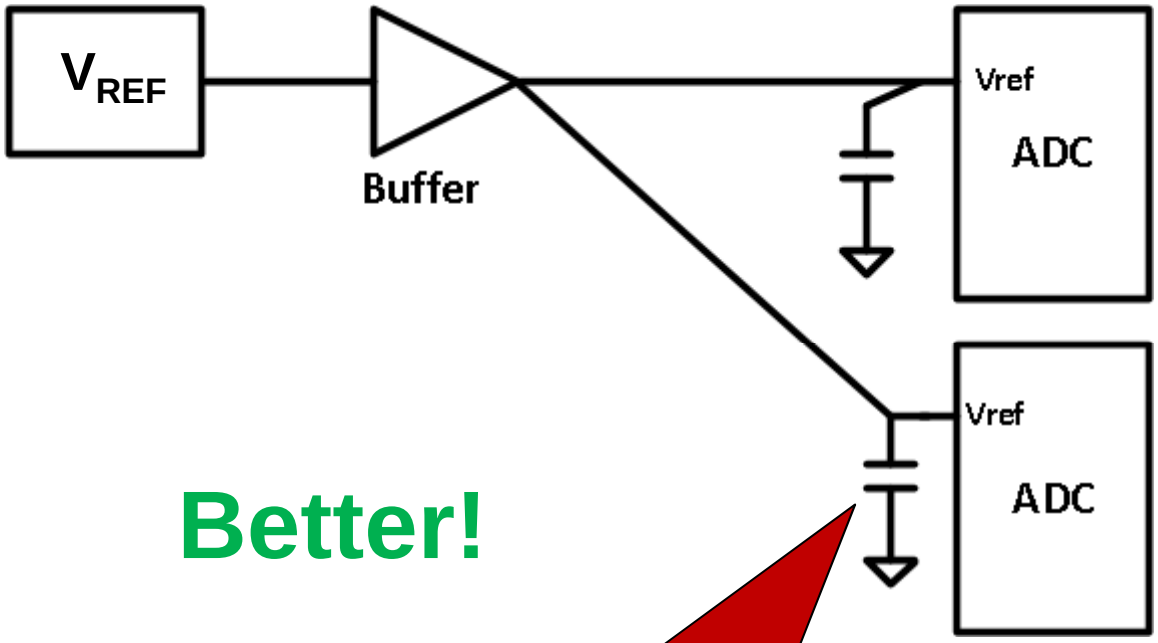
Poor design

Referencing Multiple ADCs



Not much better…

Referencing Multiple ADCs



Better!

Look in datasheet for capacitor value recommendations to avoid phase margin corruption

- **One reference capacitor is required at each ADC**
- **Use a star configuration to prevent crosstalk between ADCs**

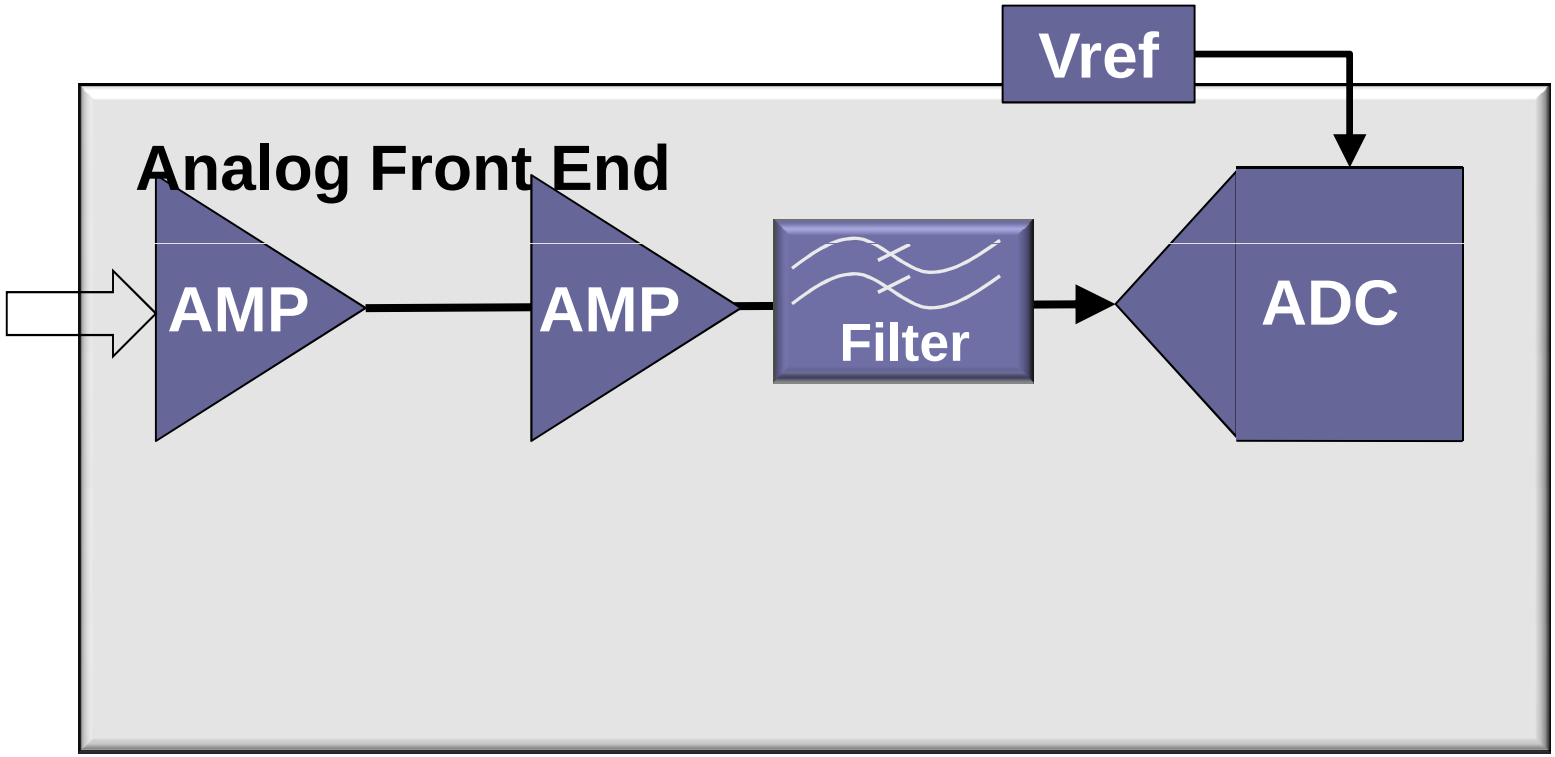
Analyzing the Analog Signal Chain

- **Most suppliers provide analog simulation tools that evaluate the circuitry**
  - Simulations are only as good as the models and input stimulus
- **There's no substitute for testing under the exact operating conditions**

Why not integrate all of this into a single IC?

What is an Analog Front End?

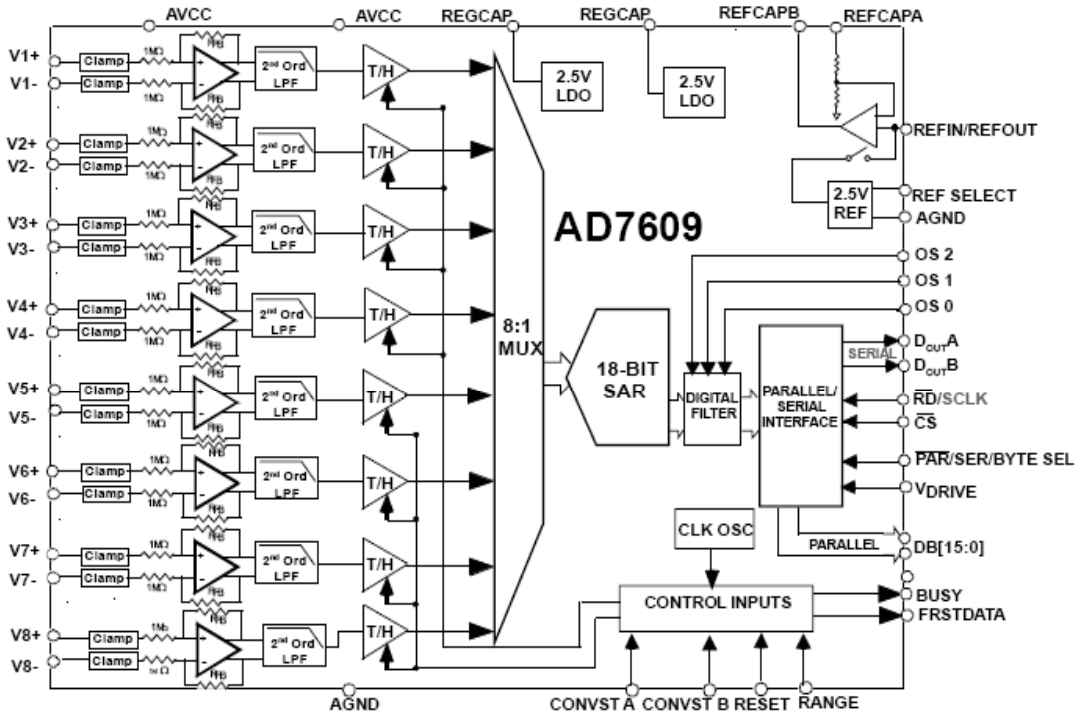
- What's next?
- How about combining it all into a single IC?



ADI AD7609 : 18 Bit, 8-Channel ADC

Building Block for High Dynamic Range Applications

- **Features**
  - **8 channels simultaneous sampling @ 200KSPS**
  - Single 5V supply operation
  - Differential Analog Inputs **+/-20V** & +/-10V
  - Analog Inputs can withstand **7KV HBM ESD**
  - +/-16.5V Analog input clamp protection
  - 1Meg Resistor input impedance
  - 2nd Order Analog **Anti-Alias Filter**
  - Backend Digital filter
  - 2.5V reference and reference buffer
  - SPI and Parallel interface
- **Performance**
  - 18 Bits No Missing Codes
  - INL +/- 2.5LSB (Typ)
  - 91 dB SNR @ 200k
  - **105 dB DR @3.125ksps (digital filter on, OSR = 64)**
  - 105mW Power (Typ)
  - NFS/PFS Code 0.1% FSR over Temperature



Energy

Process Control

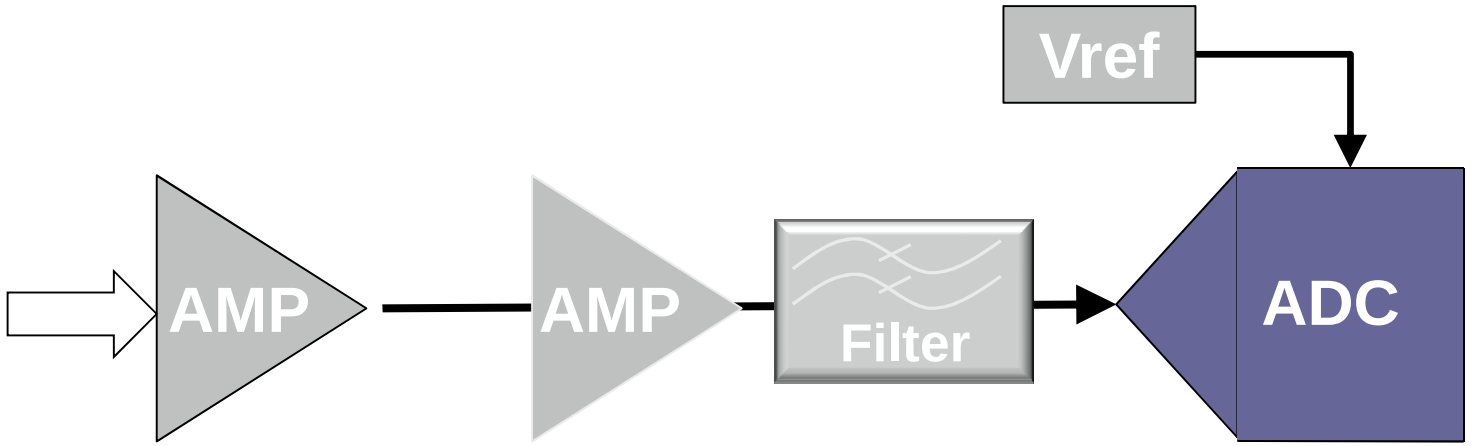
Instrumentation

Agenda

- Analog signal chain
- **Standalone data converter solutions**
- XADC solution and the customizable analog interface
- Prototyping with expansion boards

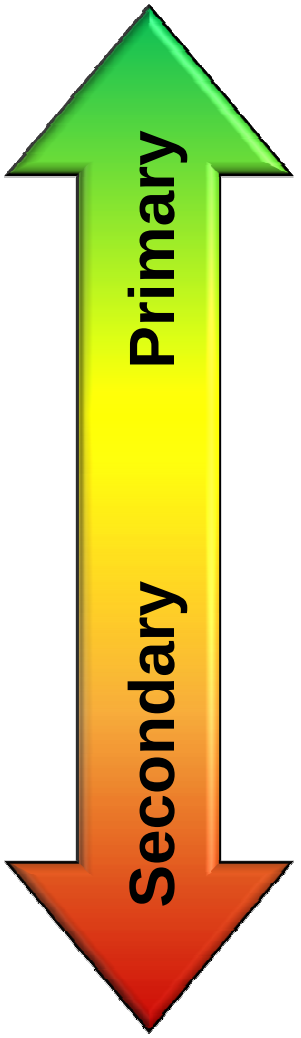
What about ADC's?

- **We've talked about the signal chain…**
- **How do we choose the ADC?**



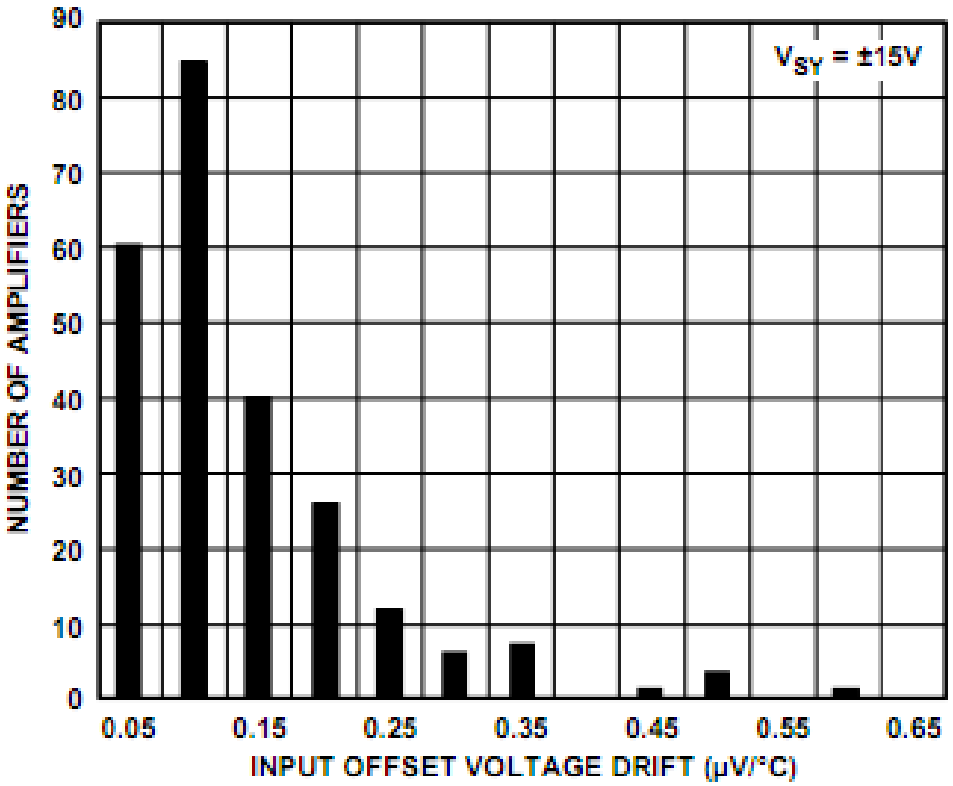
Choosing the Right ADC

- **Resolution**
- **Bandwidth of interest**
- **Input**
  - Input types (Unipolar, Bipolar, +/-10V)
  - Channel count
  - Mux'ed vs. simultaneous sampling
- **Interface**
- **Size**
- **Power consumption**
- **ADC architecture**
- **Error & dynamic specifications**
- **Other system considerations**
  - Internal/External Reference, FIFO, PGA, GPIO



Understanding ADC Errors

- **When evaluating ADC performance it's important to understand errors**
  - Linearity errors
  - Gain errors
  - DC offset errors
  - Input offset and offset drift
    - Input offset can be calibrated out
    - Drift cannot



ADC Architectures

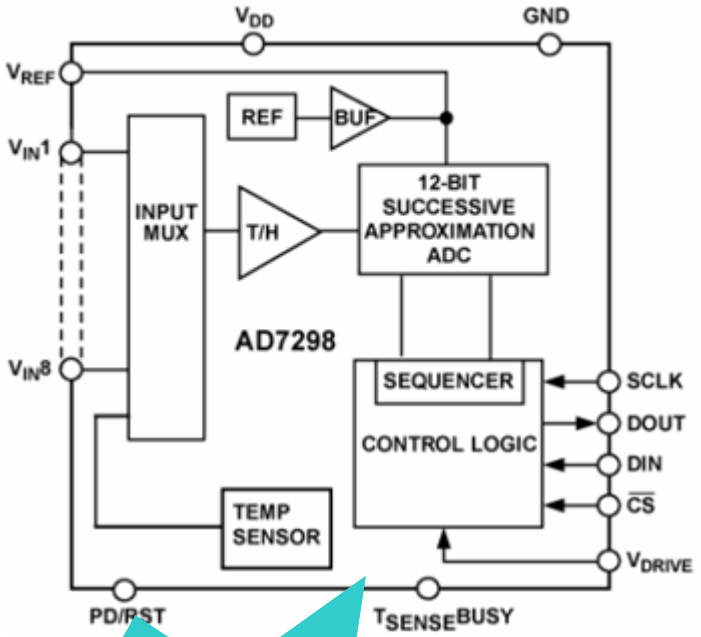
- **Sampling Rate vs. Resolution**

Analog to Digital Converter Topologies			
Topology	Typical Resolution	Typical Sample Rate	Details
Flash	< 16 bits	100M – 3G	Fastest Sample Rate Costly, Big, > Power
Pipeline	8-16 bits	1M – 500M	High Speed Low Latency
SAR	8-18 bits	20K – 10M	Low Latency Low Power (= SPS)
Delta Sigma	12-31 bits	15 – 4M	Excellent Line Rejection Built-in Filtering (OverS)

Analog Devices AD7298

KEY FEATURES:

- **Sequencer allows multi-channel programmability**
  - 8-channel multiplexer with configurable sequence
- **ADC with 1 MSPS Throughput Rate**
- **Internal temperature sensor**
  - ±3ºC max (-40ºC to 125ºC)
- **Accurate AC and DC performance:**
  - INL: ±0.5LSB
  - DNL: ±0.5LSB
  - SNR: 72dB
- **0-2.5V analog input range**
- **Internal Reference**
  - 2.5V, 12ppm/ºC typ



Smallest multi-ch ADC + Tsense + Vref on market

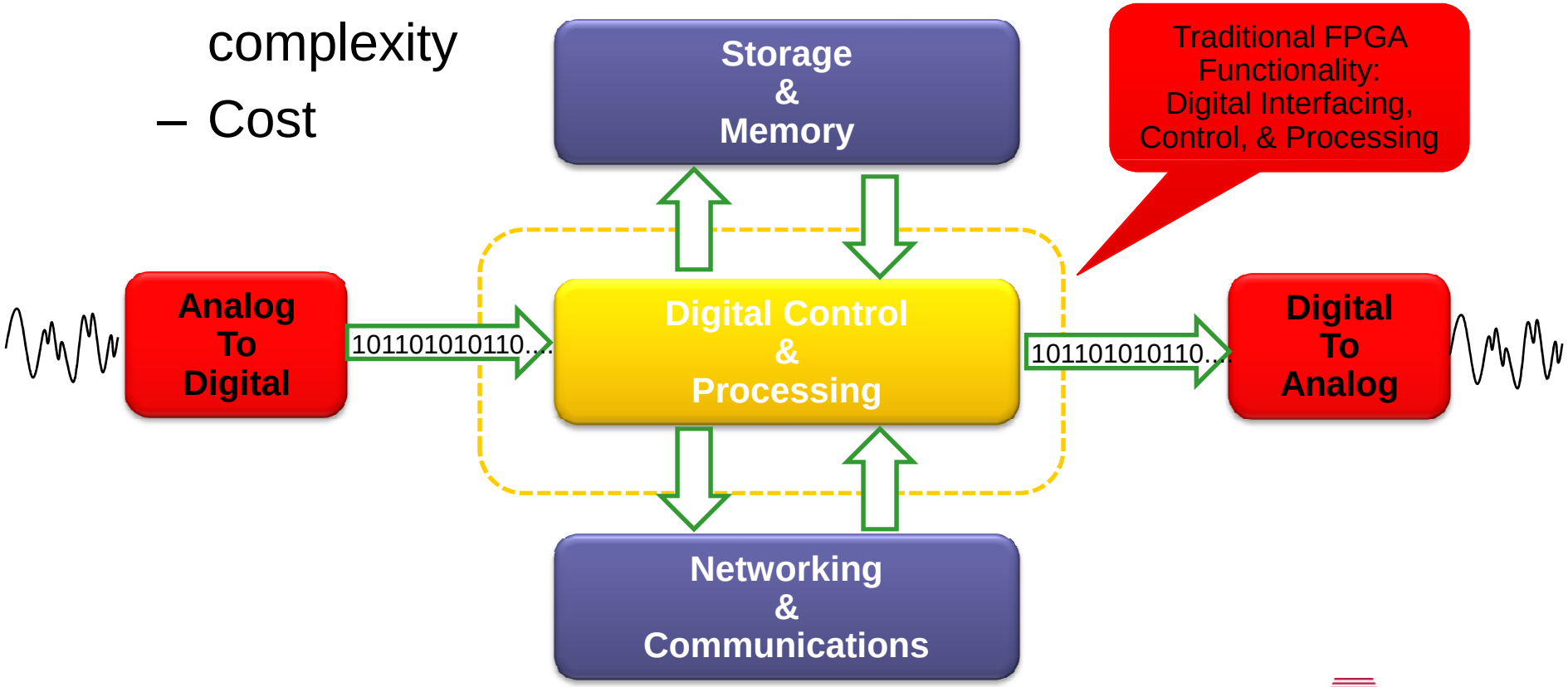
Resolution	Throughput	Channel No.	Interface	Power Supply	Package
12-Bit	1 MSPS	8	Serial SPI	2.8V – 3.6V VDD, 1.65V – 3.6V VIO	20-lead LFCSP

Agenda

- Analog signal chain
- Standalone data converter solutions
- **XADC solution and the customizable analog interface**
- Prototyping with expansion boards

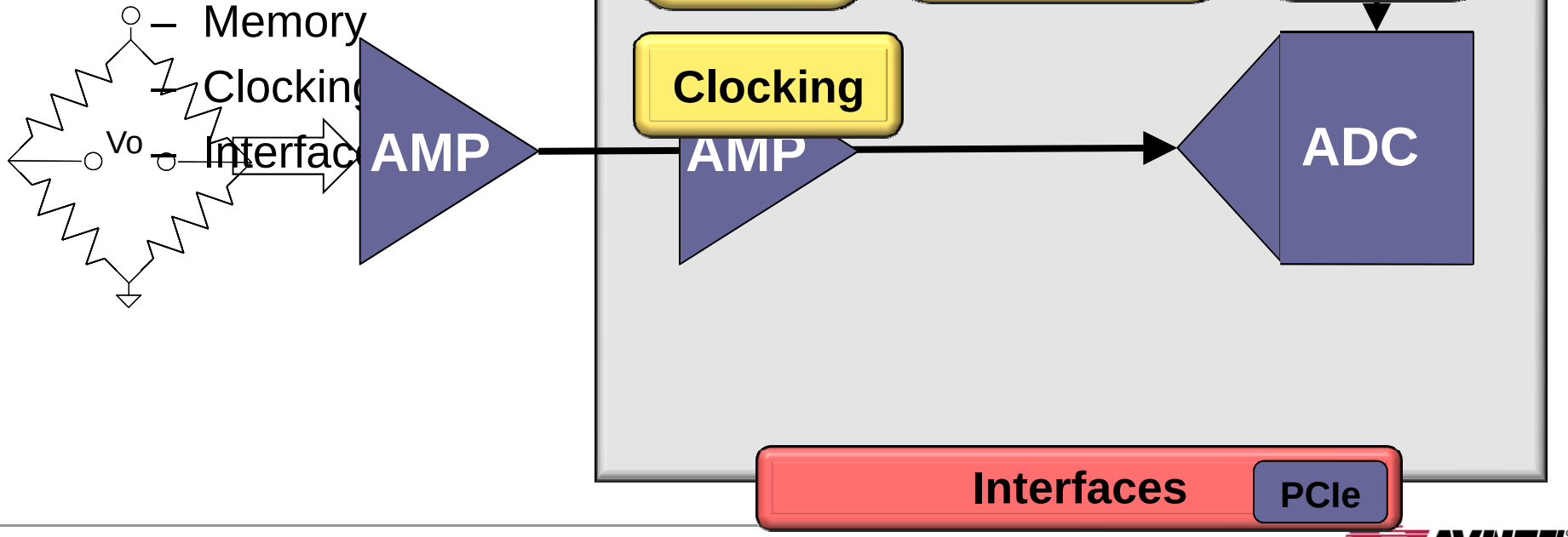
Integrating an ADC into the FPGA

- **Adding analog to an FPGA reduces**
  - IC count
  - Board complexity
  - Cost



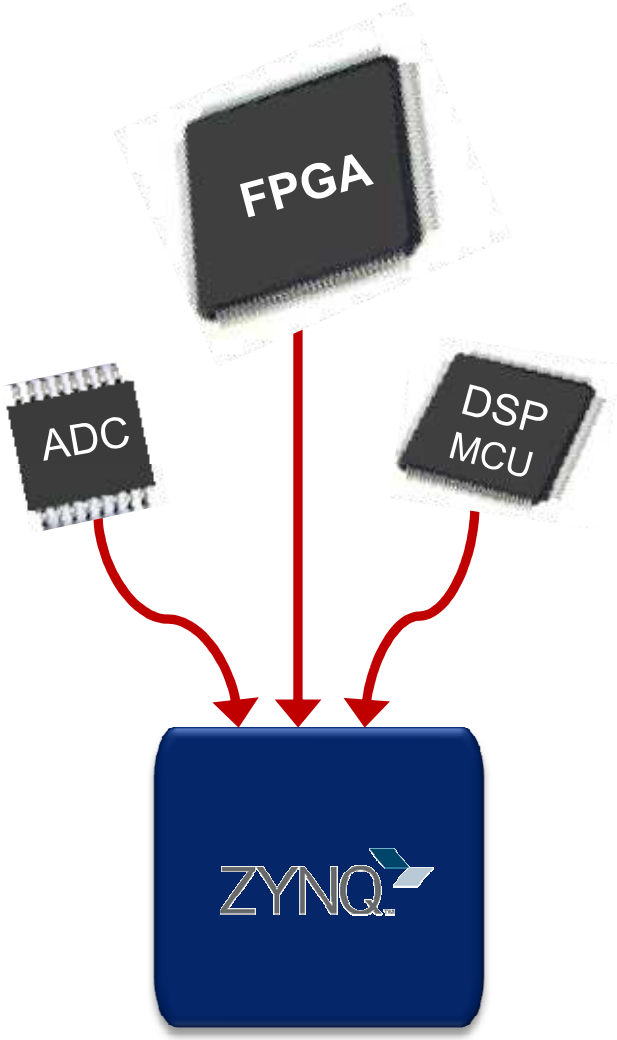
Introducing the XADC

- **Not just an FPGA anymore!**
  - Programmable logic
  - DSP
  - Processing
  - Memory
  - Clocking
  - Interfac

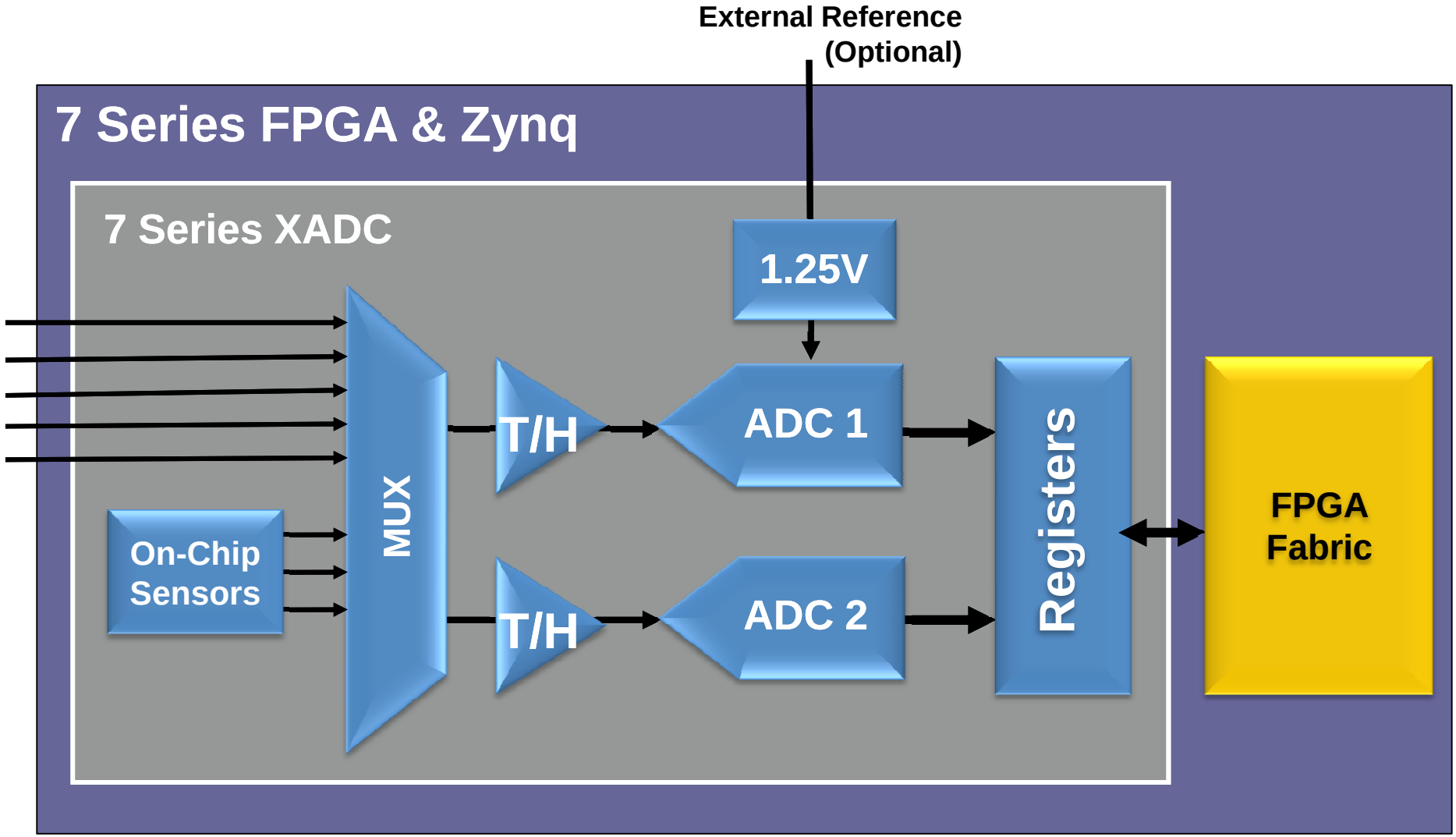


Benefits of Integration

- **Reduced Cost**
- **Elimination of discrete analog components and associated board area**
  - Reduce obsolescence
- **Customization of Analog Interface**
  - Flexible analog interface
    - Configure up to 17 analog inputs
    - Change ADC timing
  - Logic can be used for:
    - Calibration
    - Signal processing, etc.



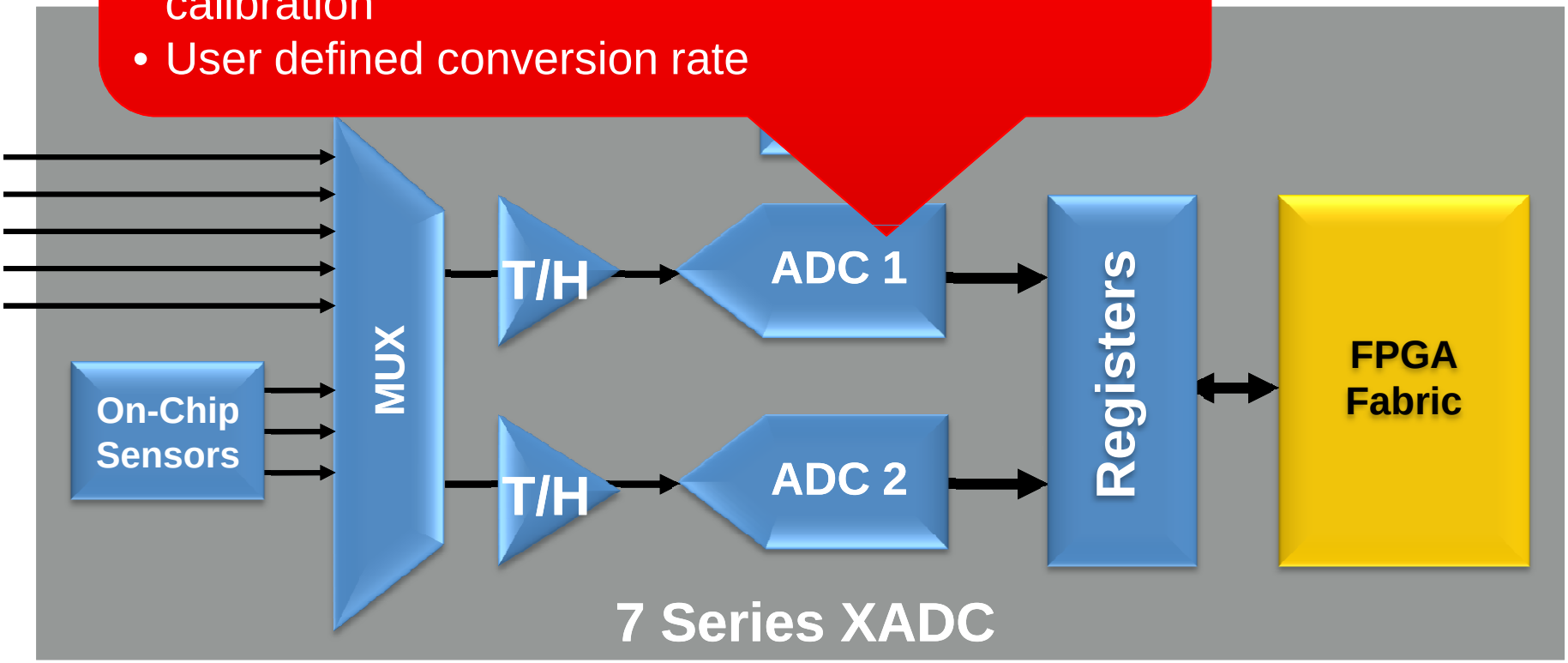
XADC Block Diagram



Dual ADCs

Dual 12-bit 1Msps Analog-to-Digital Converters

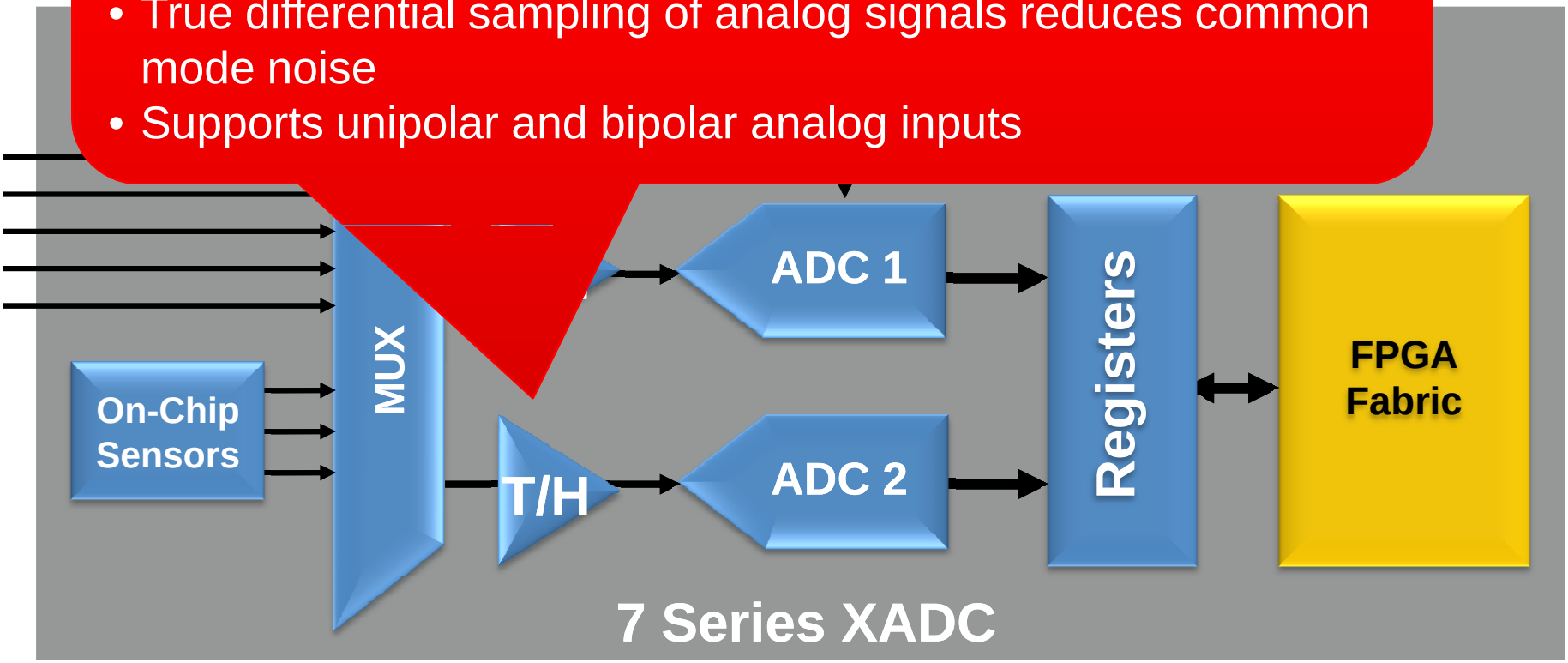
- Independent operation possible
- ADCs carry out 16-bit conversion with digital calibration
- User defined conversion rate



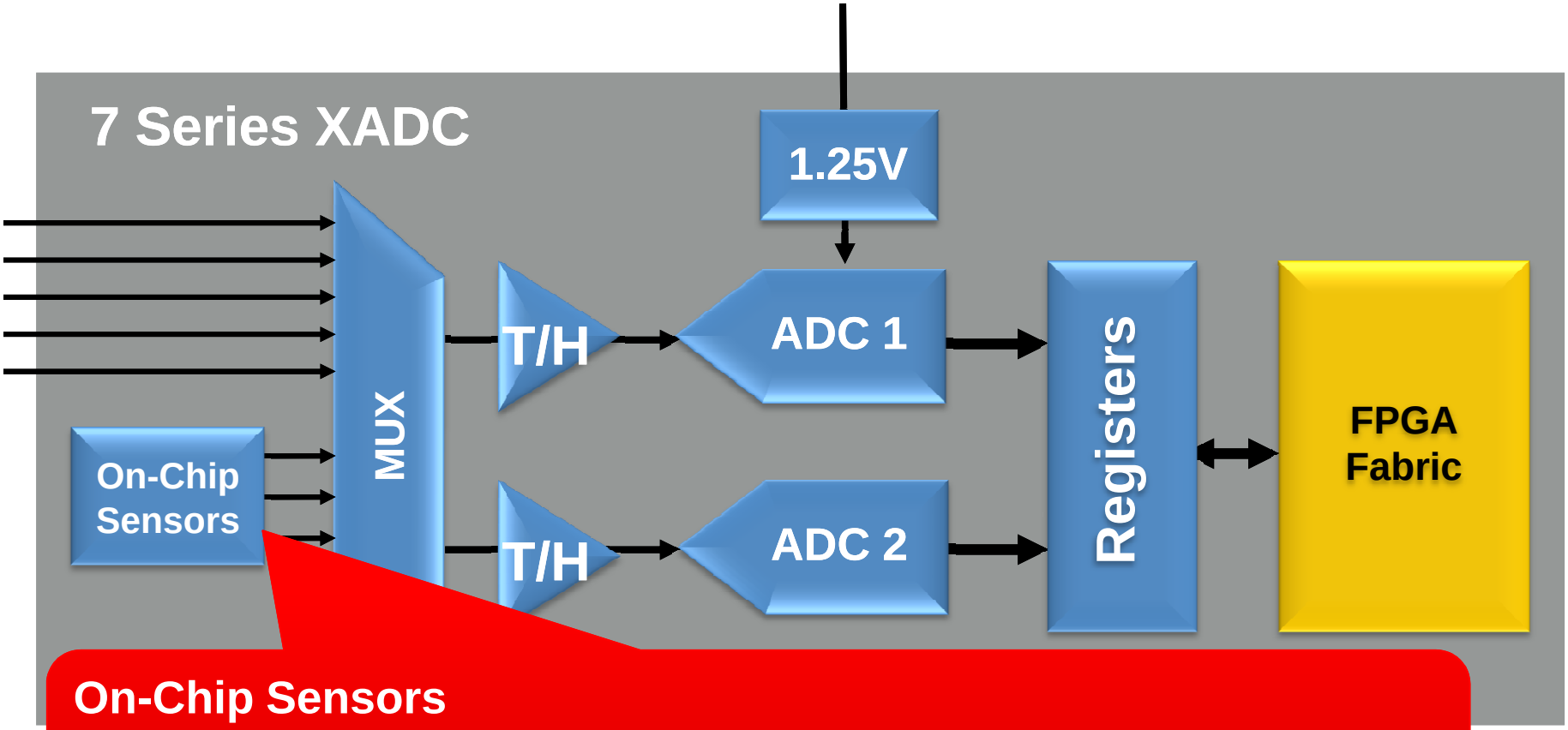
Separate Track & Hold Amplifiers

Two Flexible Track & Hold (T/H) Amplifiers

- Precise control of sampling timing & simultaneous sampling capability
- True differential sampling of analog signals reduces common mode noise
- Supports unipolar and bipolar analog inputs



On-Chip Sensors



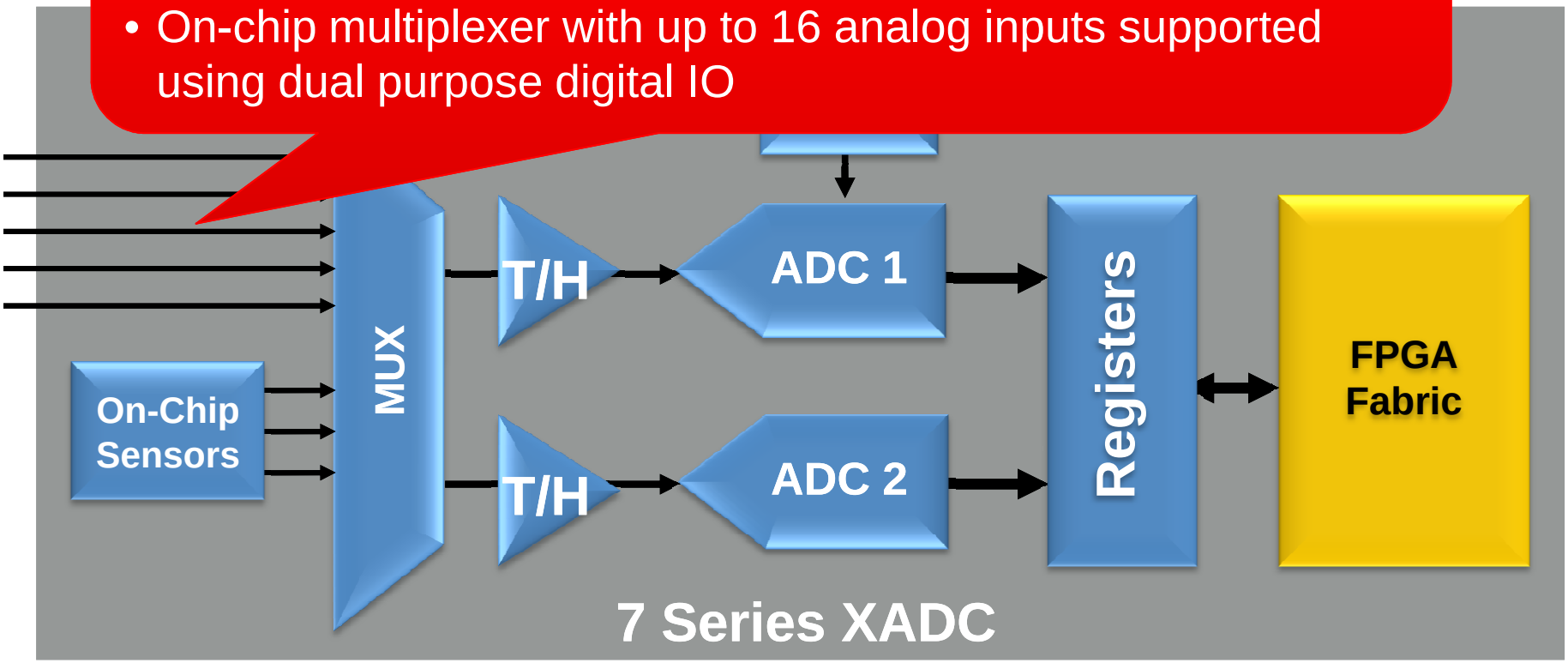
On-Chip Sensors

- Temperature sensors with ±4ºC error from -40ºC to +100ºC
- Power supply monitoring with ±1% error from -40ºC to +100ºC

Flexible External Analog Inputs

External Analog Input Channels

- One dedicated input channel for use with external analog multiplexer
- On-chip multiplexer with up to 16 analog inputs supported using dual purpose digital IO

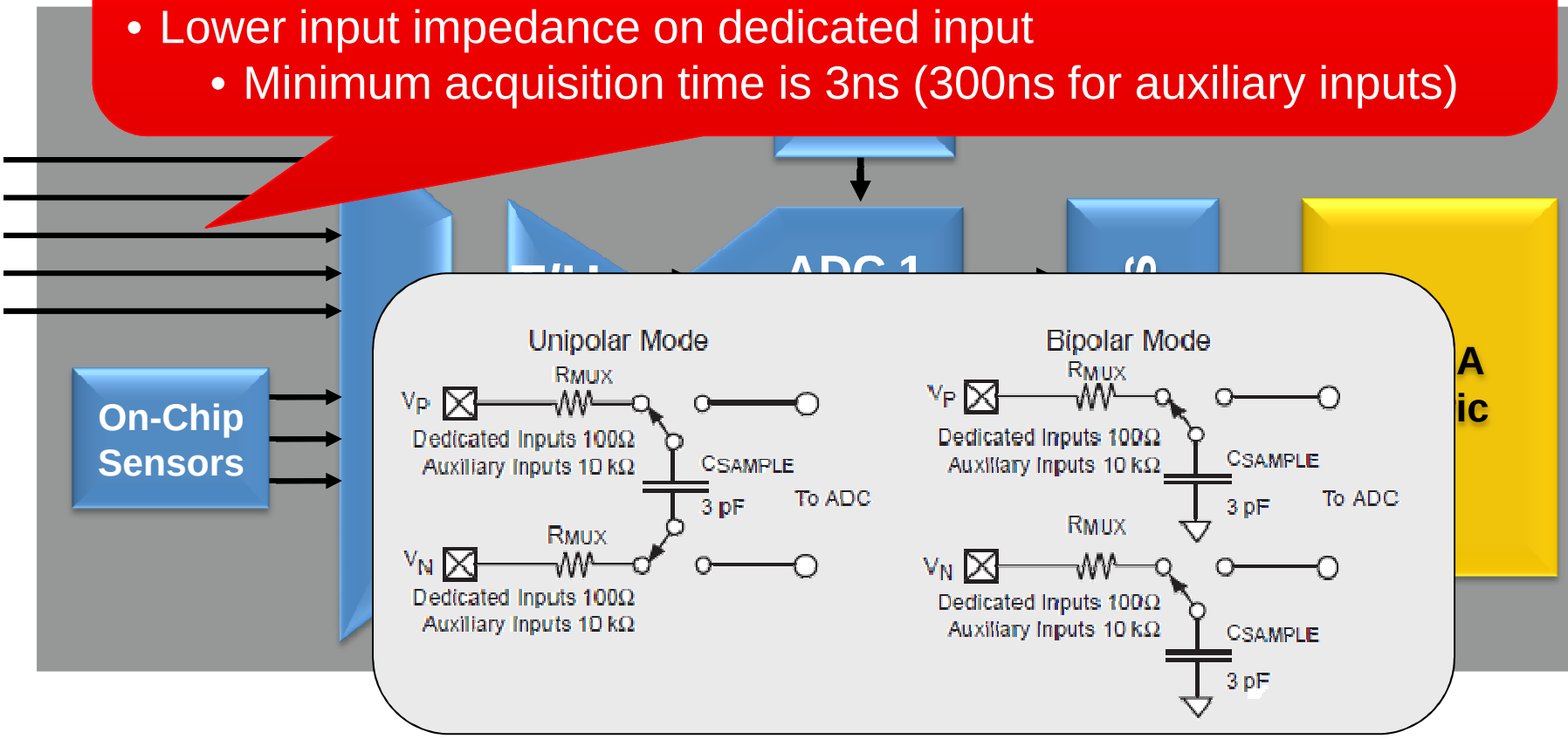


Note: Auxiliary channels 6, 7, 13, 14, and 15 are not supported on Kintex-7 devices

Flexible External Analog Inputs

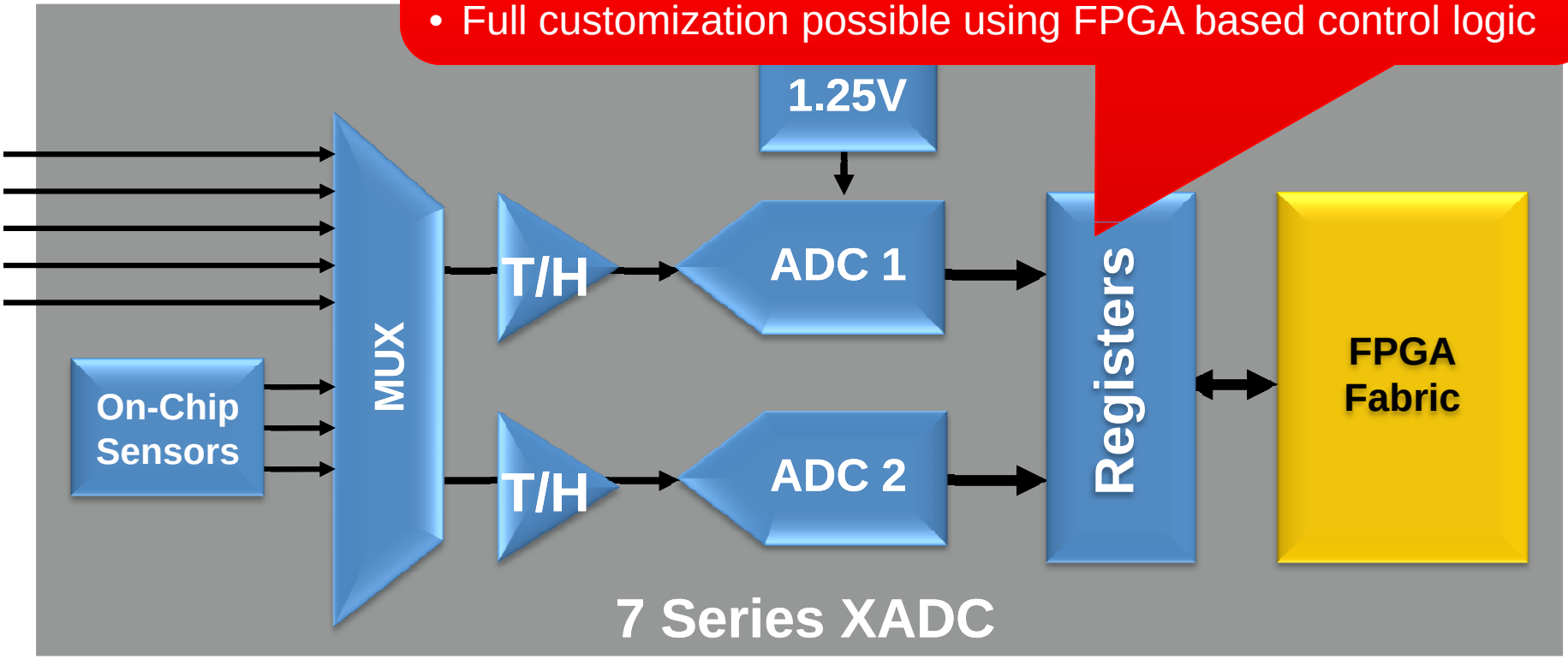
External Analog Input Channels

- Full scale input range is 1V p-p
- Use differential configuration for common mode noise rejection
- Lower input impedance on dedicated input
  - Minimum acquisition time is 3ns (300ns for auxiliary inputs)



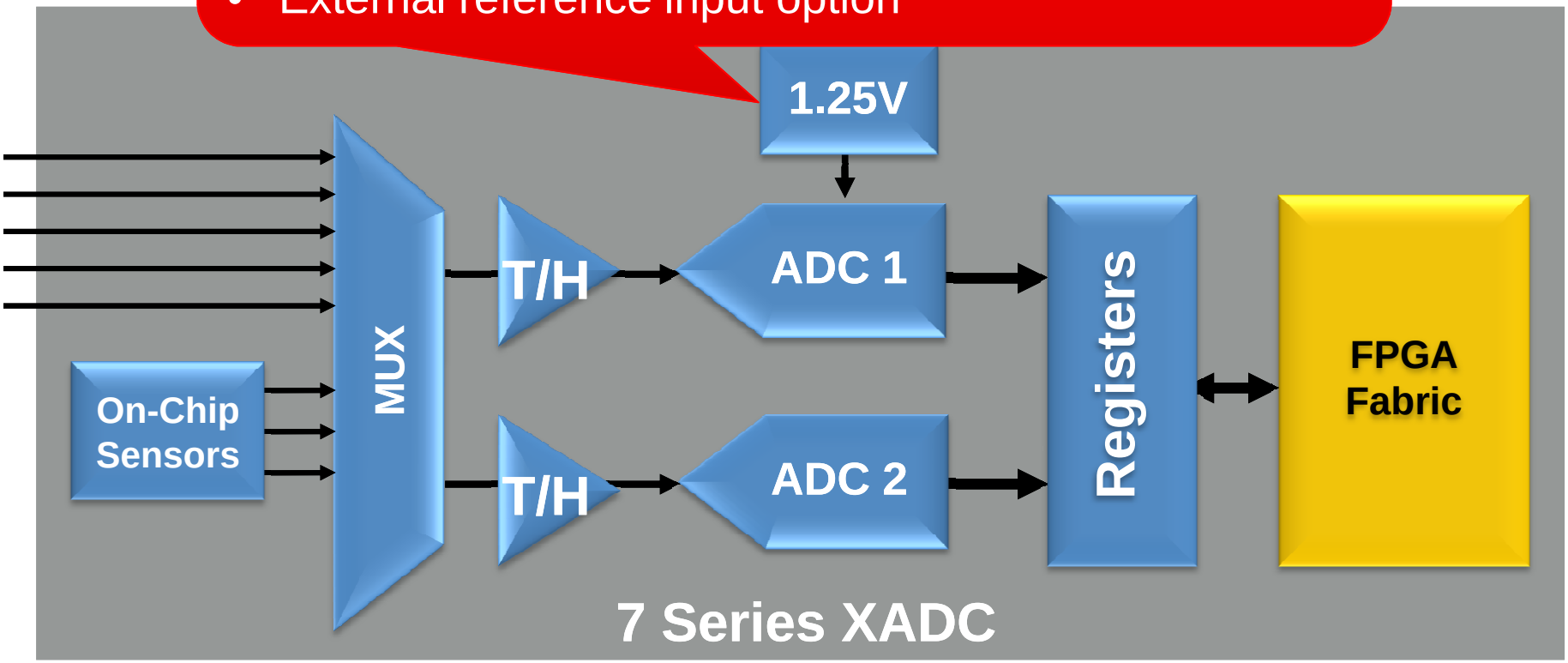
High Speed Digital Interface

Programmable XADC Operation
- 250MHz Read / Write Register access
- Operation can be altered at any time via FPGA Interface
- Full customization possible using FPGA based control logic

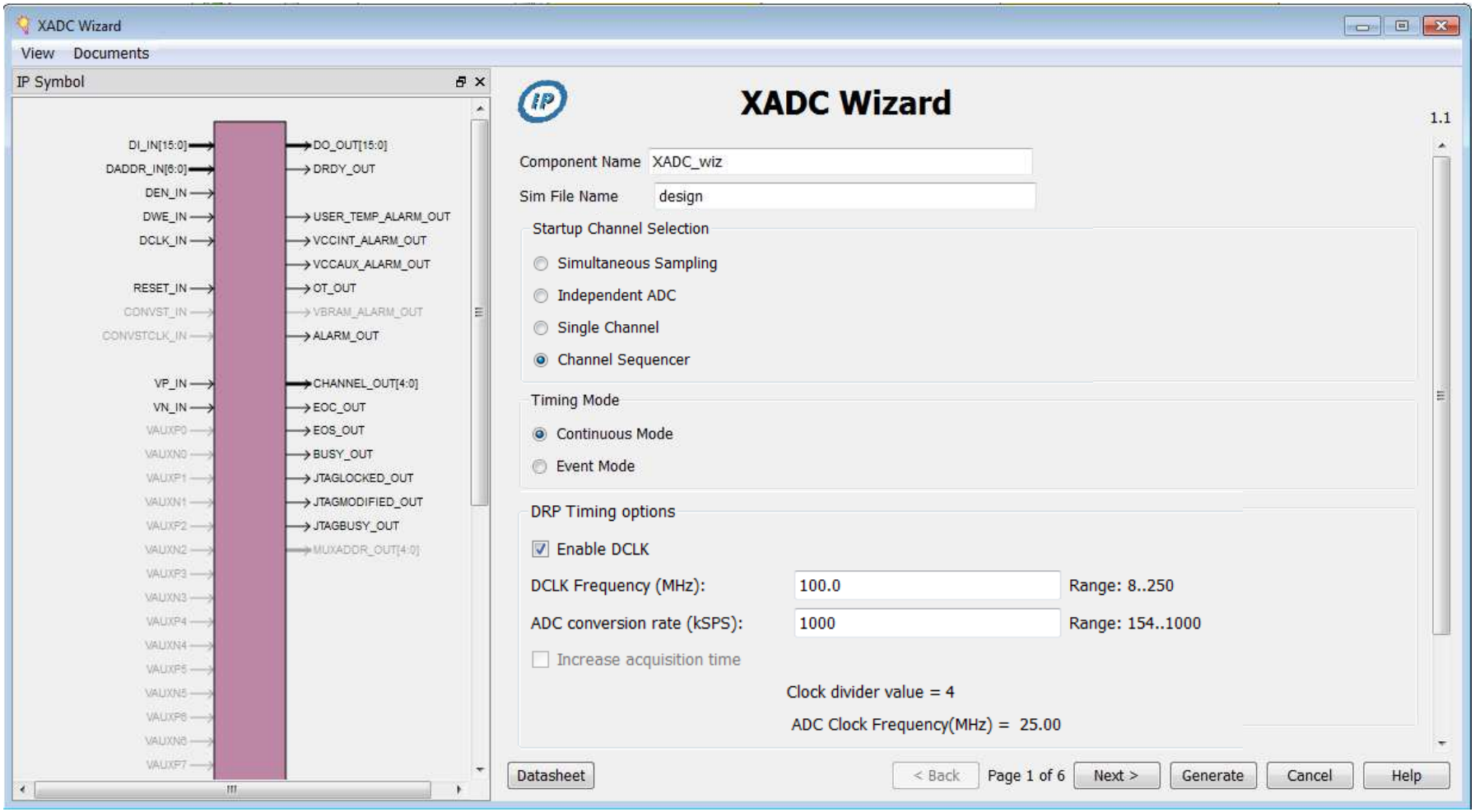


Internal Voltage Reference

Internal Reference
- **1.25V**
- **±1% error from -40°C to +100°C**
- External reference input option



XADC Wizard Simplifies HDL Instantiation



Wizard simplifies XADC Instantiation

No HDL experience required – even analog guys can get started

XADC Safety Alarms

- **Trigger and reset thresholds for temp alarms**
- **Upper and lower voltage thresholds for on-chip power supplies**

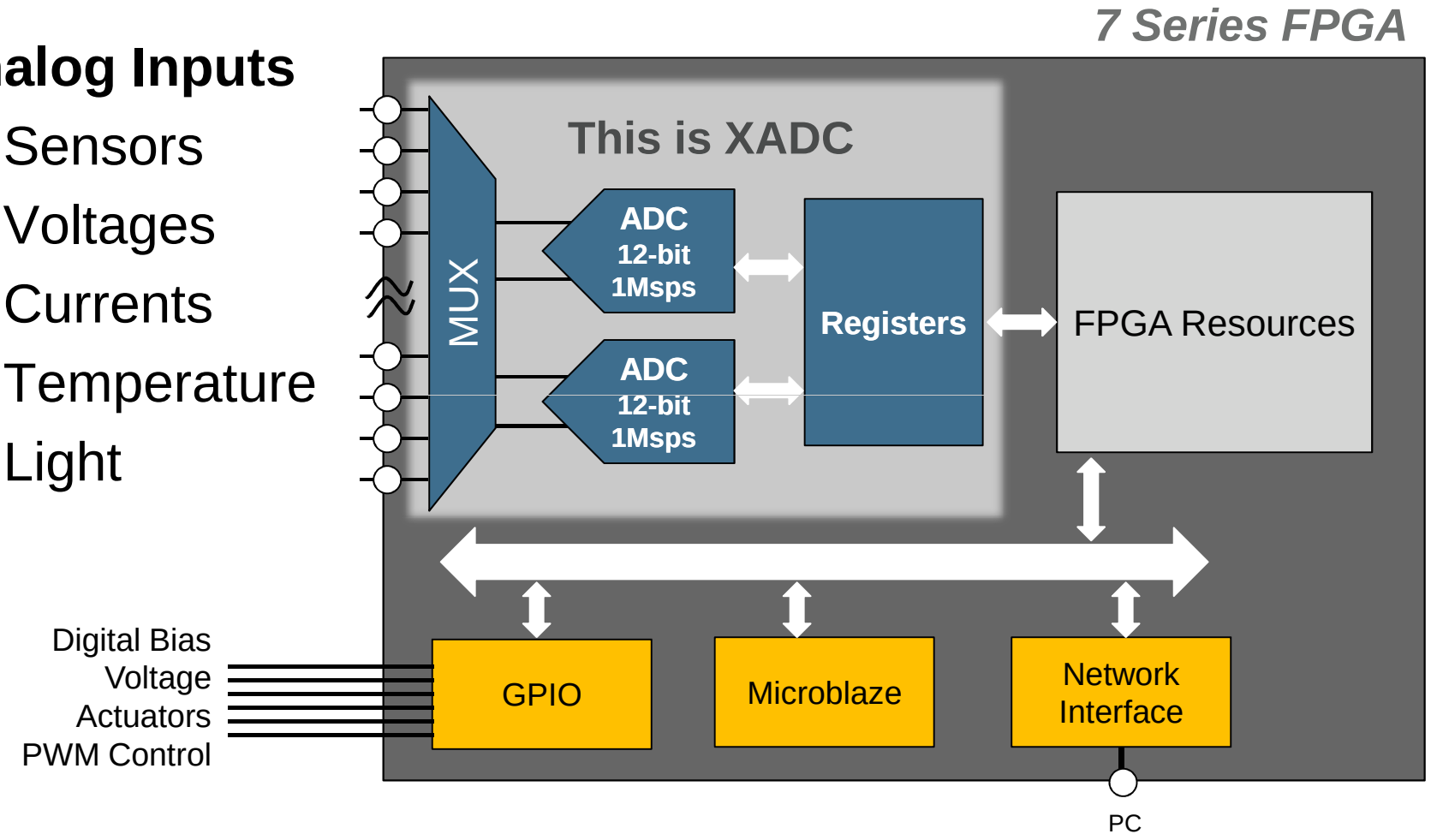
XADC & Agile Mixed Signal

- **XADC is a high quality & flexible analog interface new to 7 series**
  - Dual 12-bit 1Msps ADCs, On-Chip Sensors, 17 flexible analog inputs, Track & Holds with programmable signal conditioning
    - Integration of up to $2-3 of external ADC functionality

- **Agile Mixed Signal (AMS)**
  - Using the FPGA programmable logic to customize the XADC & replace other external analog functions e.g., linearization, calibration, filtering, and DC balancing to improve data conversion resolution.

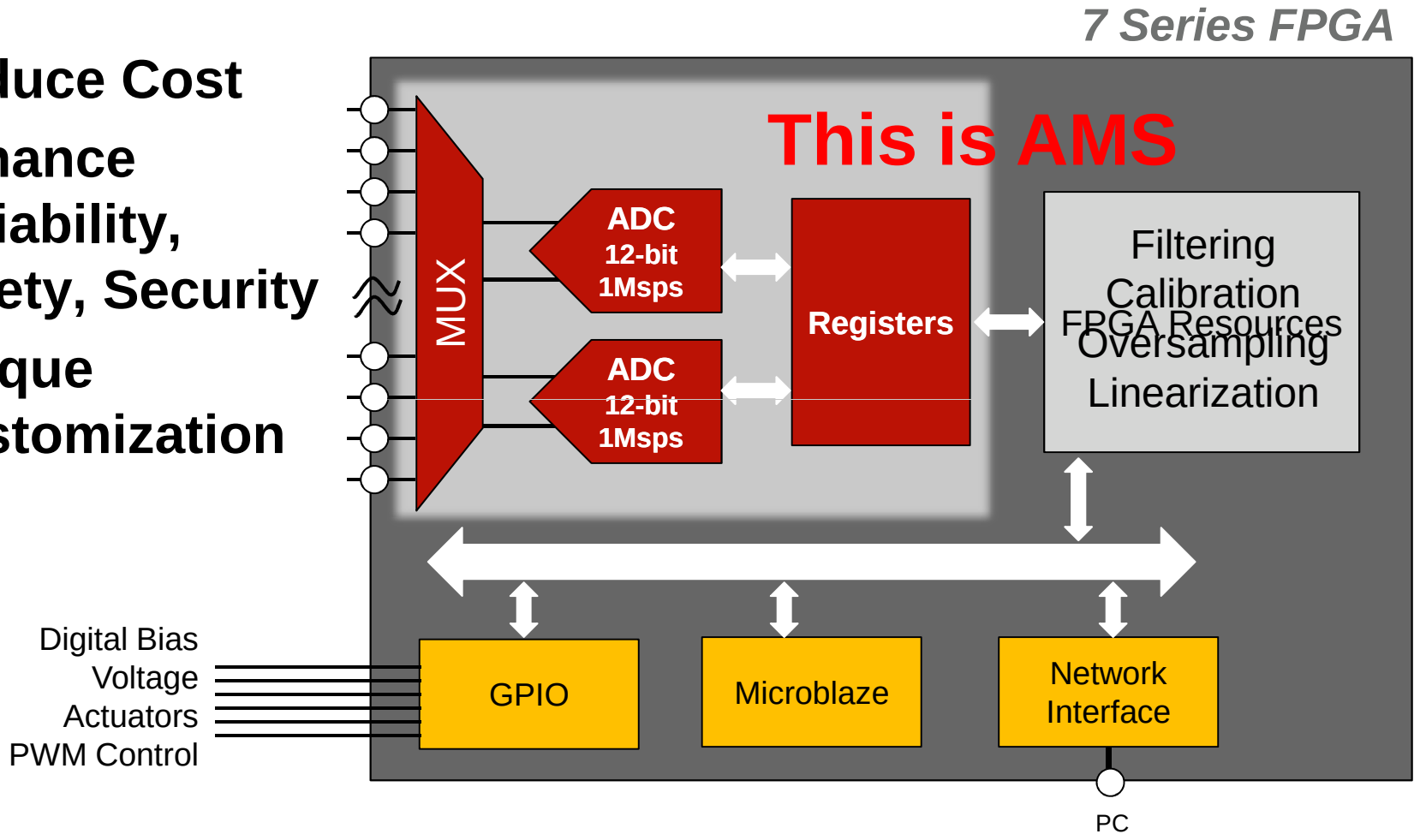
AMS = More Than Just an Integrated ADC

- **Analog Inputs**
  - Sensors
  - Voltages
  - Currents
  - Temperature
  - Light



AMS = More Than Just an Integrated ADC

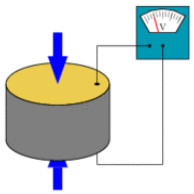
- **Reduce Cost**
- **Enhance Reliability, Safety, Security**
- **Unique Customization**



AMS = combination of analog & programmable logic

Benefits of Integration

- **Remember, there are many sensor types**
  - Each having it's own output range



- Weigh-scale systems typically use load-cell bridge sensors with maximum full-scale outputs of 1 mV to 2 mV

- **In ADC applications, dynamic range is the ratio of the RMS value of the full scale to the RMS noise**

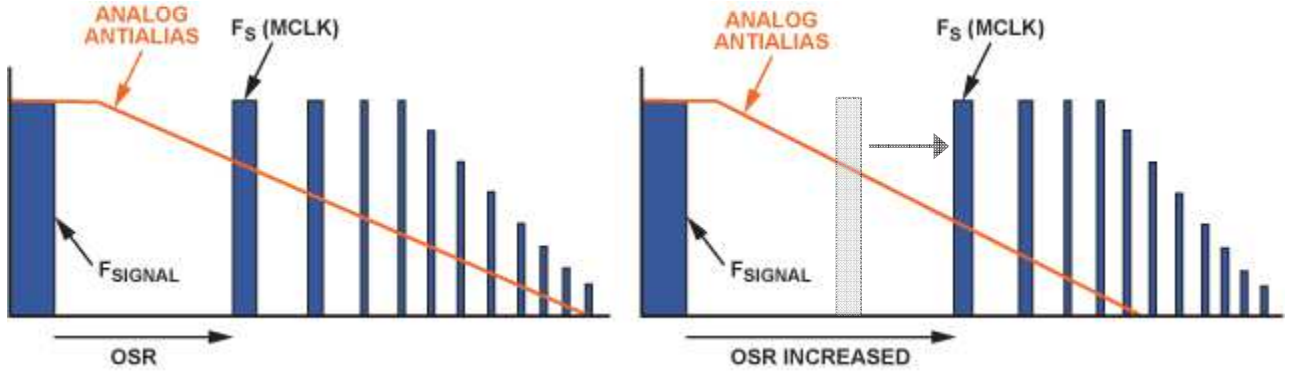
For an ***N*-bit** ADC, the dynamic range (DR) can be calculated as:

$DR = 6.021N + 1.763$ dB

So for a 12-bit ADC:
Dynamic Range = 74dB

Increasing Dynamic Range

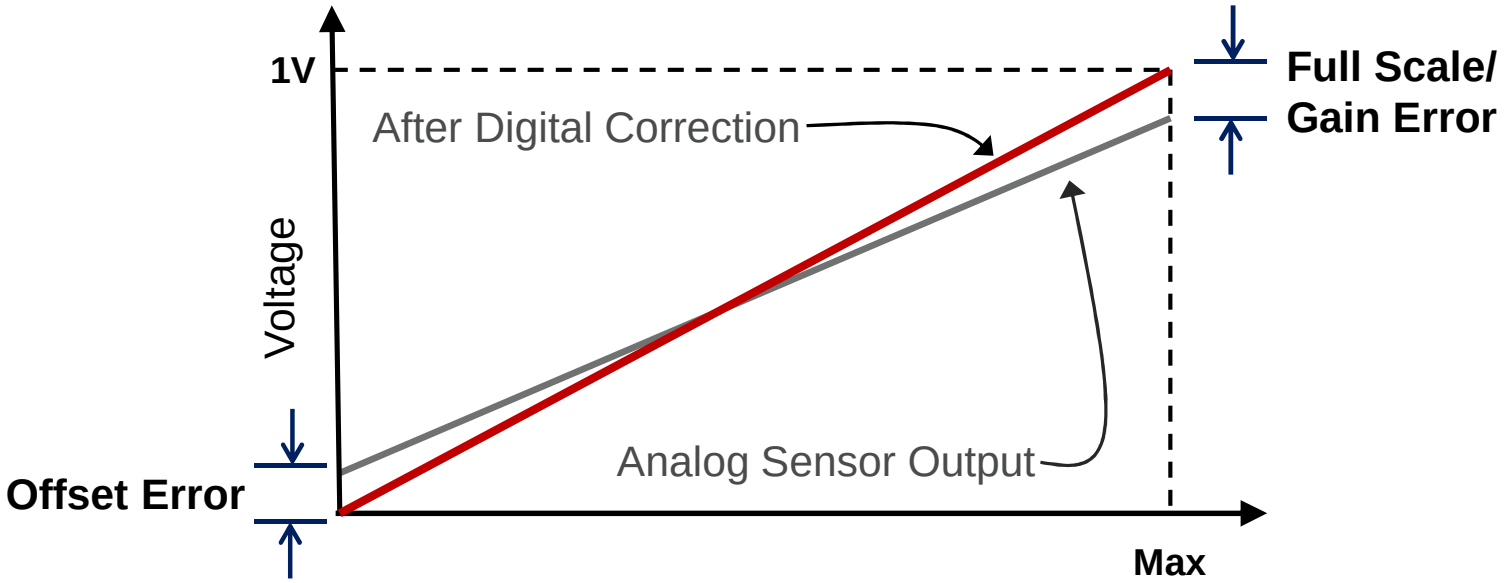
- **One method for increasing the dynamic range of a successive-approximation ADC is to implement *oversampling***
- **As a general rule, every doubling of the sampling frequency yields approximately a 3-dB improvement in noise performance**



- **Decimation in FPGA can average samples and increase dynamic range**
  - Even more with calibration values

AMS Digital Correction - Offset & Gain

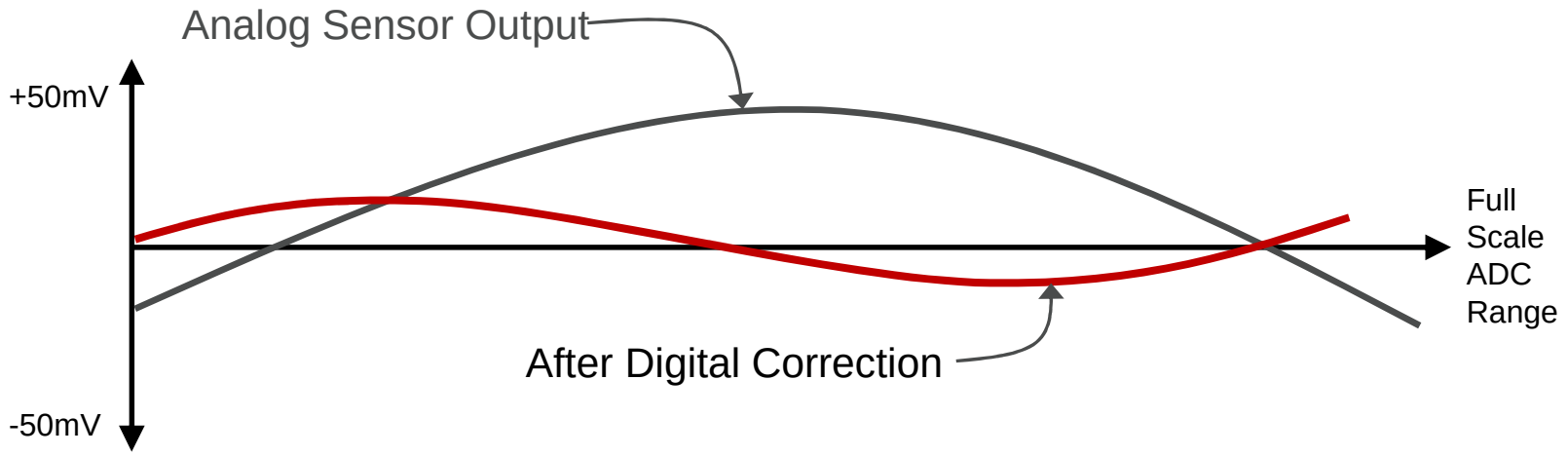
- **FPGA resources, including DSP, BRAM and logic, can be applied to correct or calibrate the transfer function of the sensor**



See Xilinx white paper WP398

AMS Digital Correction - Linearization

- **Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line**



- **Linearization of a large number of channels is very efficient**
  - Same resource can be shared across all channels due to the high FPGA fabric clock rates

AMS – Oversampling and Decimation

- **As noted before, every doubling of the sampling frequency increases dynamic range by 3dB**

From before, 12-bit ADC:
Dynamic Range = 74dB

Experiment: Oversample by 64
$2^{Oversample\_rate} = 64$; OSR = 6

Every doubling increases 3dB

3dB x 6 (OSR) = 18dB increase!

92dB

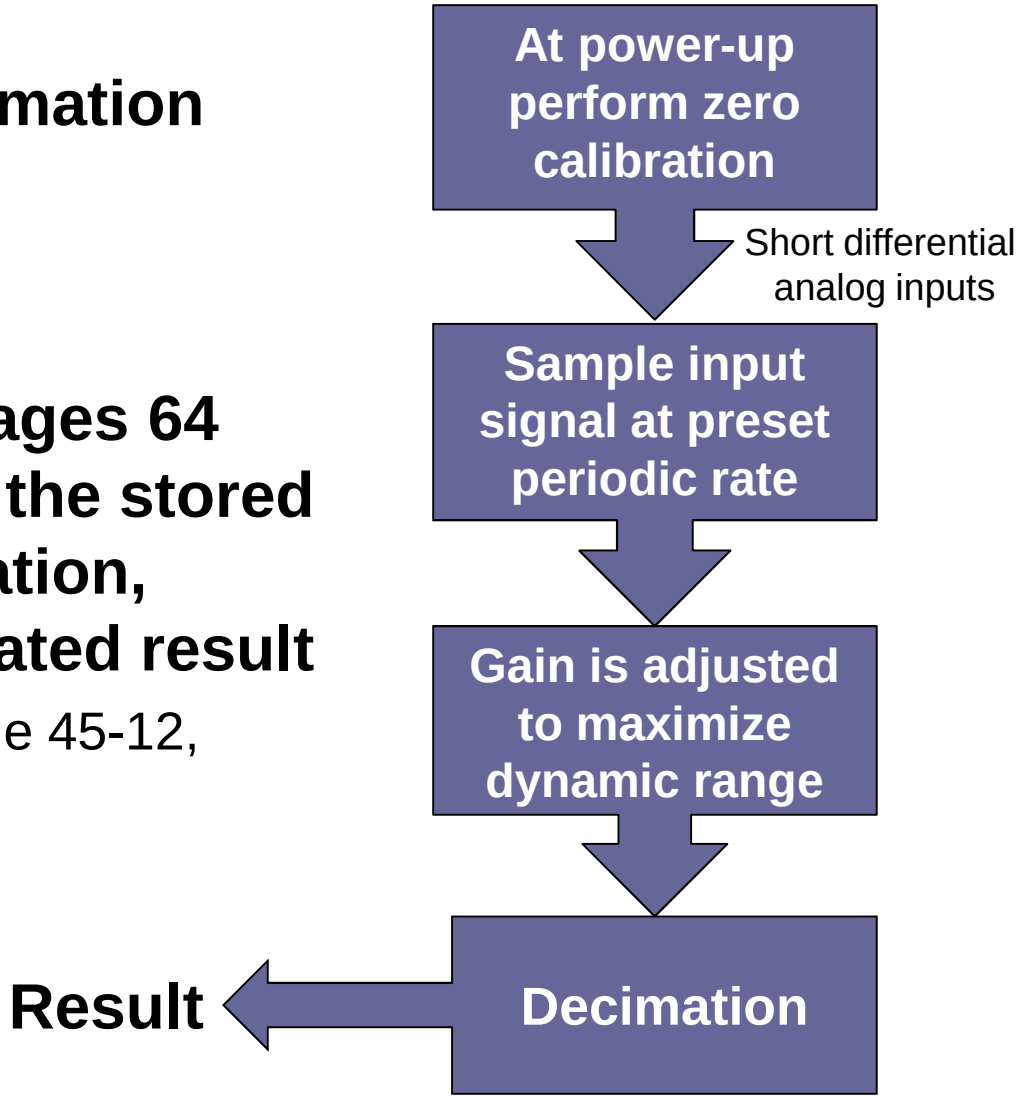
- **What to do with Oversampled data?**
- **Decimation and Gain Control in FPGA!**

AMS – Oversampling and Decimation

- **Here is a look at a decimation algorithm in an FPGA**

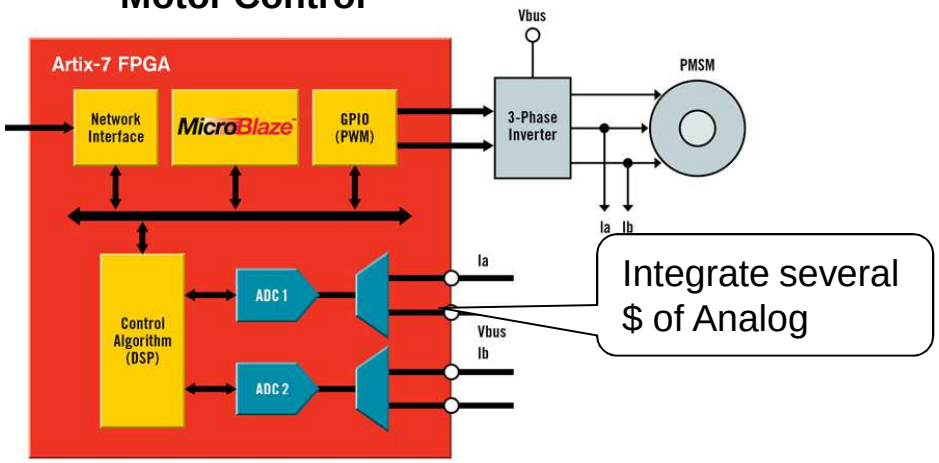
- **Decimation block averages 64 stored samples. Using the stored gain and offset information, produces a new decimated result**
  - See ADI's Analog Dialogue 45-12, December'11

Increasing DR by 18dB using resources already available!

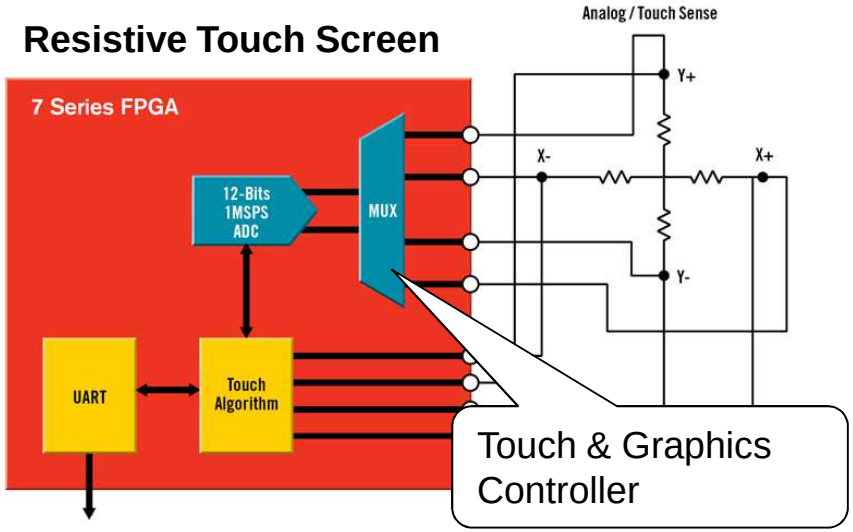


AMS Examples

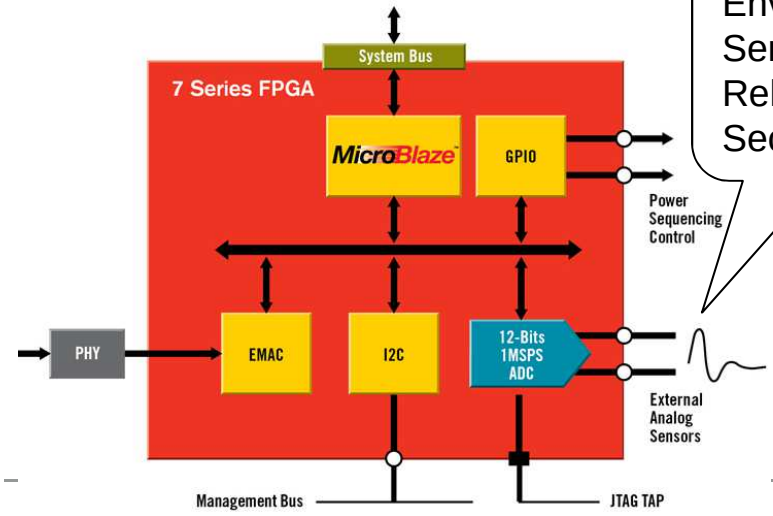
Motor Control



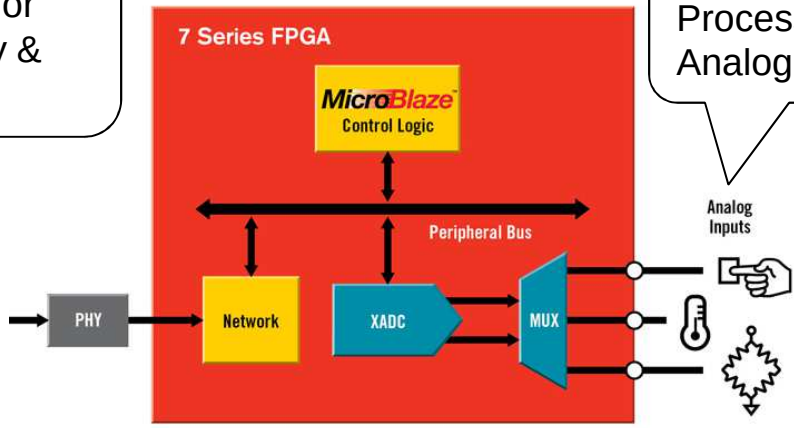
Resistive Touch Screen



System Management IC

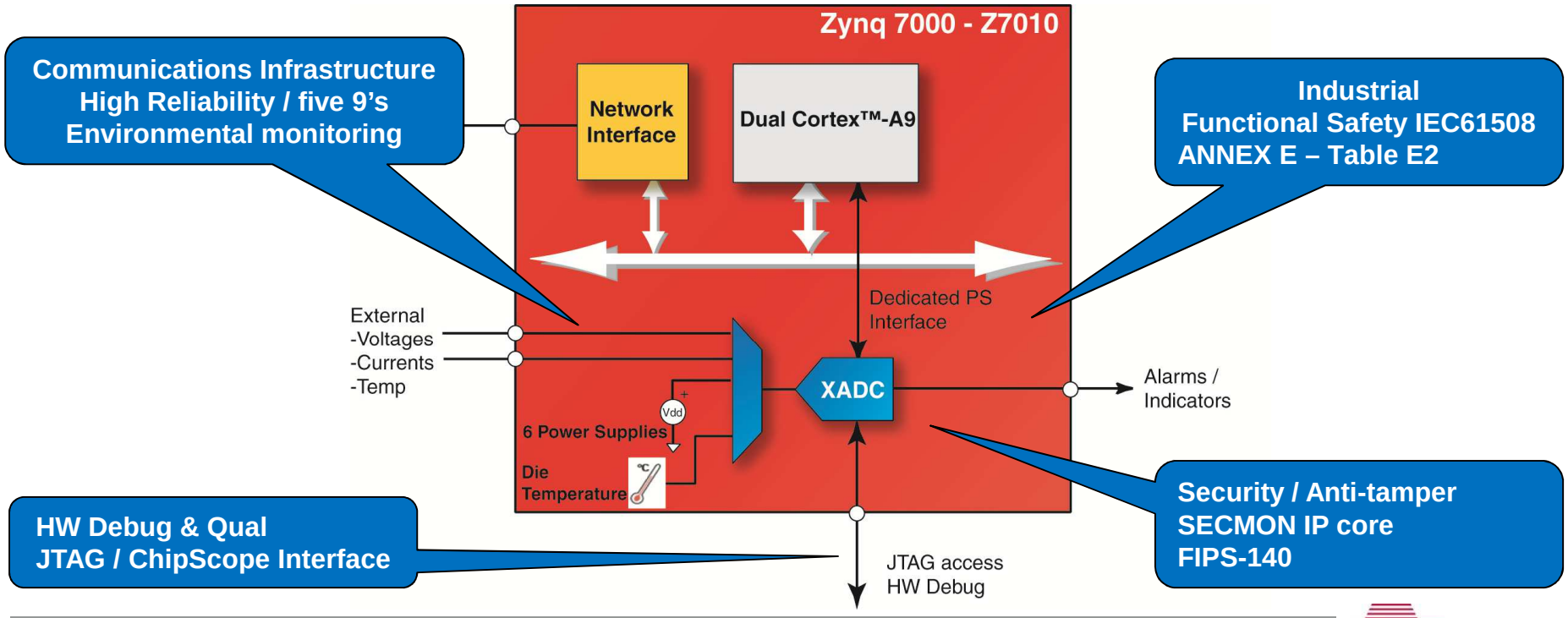


Analog Sensor Interface



On-Chip Monitoring

- **All Applications & Devices**
  - Generic requirement for Virtex, Kintex, Artix, & Zynq devices
- **Enhance Reliability, Safety, and Security of FPGA designs**
  - Mandated in many applications & covered by industry standards

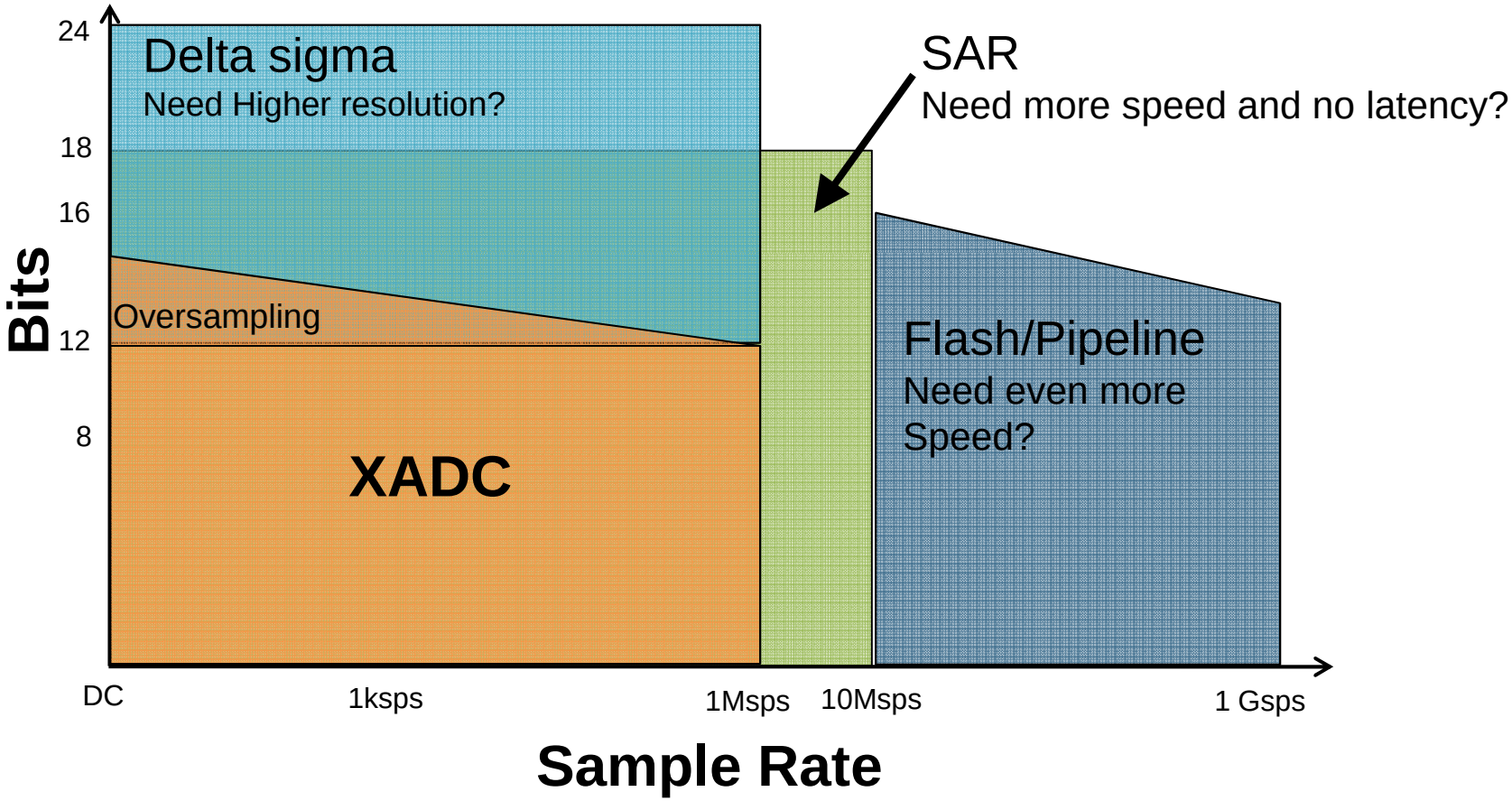


Agile Mixed Signal Benefits

- **Reduce Cost**
  - Integration of discrete analog components and reduced board area
    - Also eliminate risk of obsolesce & reduce long lead times for proprietary analog components
- **Enhanced Reliability, Safety & Security**
  - On chip sensors for improved reliability, safety & security
    - Monitoring of the physical environment required in a wide range of applications
- **Unique Customization**
  - Programmable logic customizes the XADC to address diverse needs
    - Simplify external analog signal conditioning / Enhance ADC performance
      - Oversampling & decimation , calibration, linearization, and signal processing etc.

XADC vs. Discrete ADC's

- **When is XADC a good fit?**



Agenda

- Analog signal chain
- Standalone data converter solutions
- XADC solution and the customizable analog interface
- **Prototyping with expansion boards**

Prototyping with Evaluation Boards

- **Pmods and FMC cards allow rapid prototyping**
  - Pmods = Peripheral Modules
    - Data Converters, Wireless/Bluetooth, SD Card, LCD
    - Over 50 available, many more coming soon
    - Many low-cost add-on peripheral modules as low as $10
  - FMC = FPGA Mezzanine Card
    - Feature high performance circuitry, typically > $100
    - Over 30 available, many more coming soon
- **Available reference designs allow you to quickly and easily:**
  - Evaluate the capability of the circuitry
  - Use the code examples as starting points to integrate this type of functionality into your design

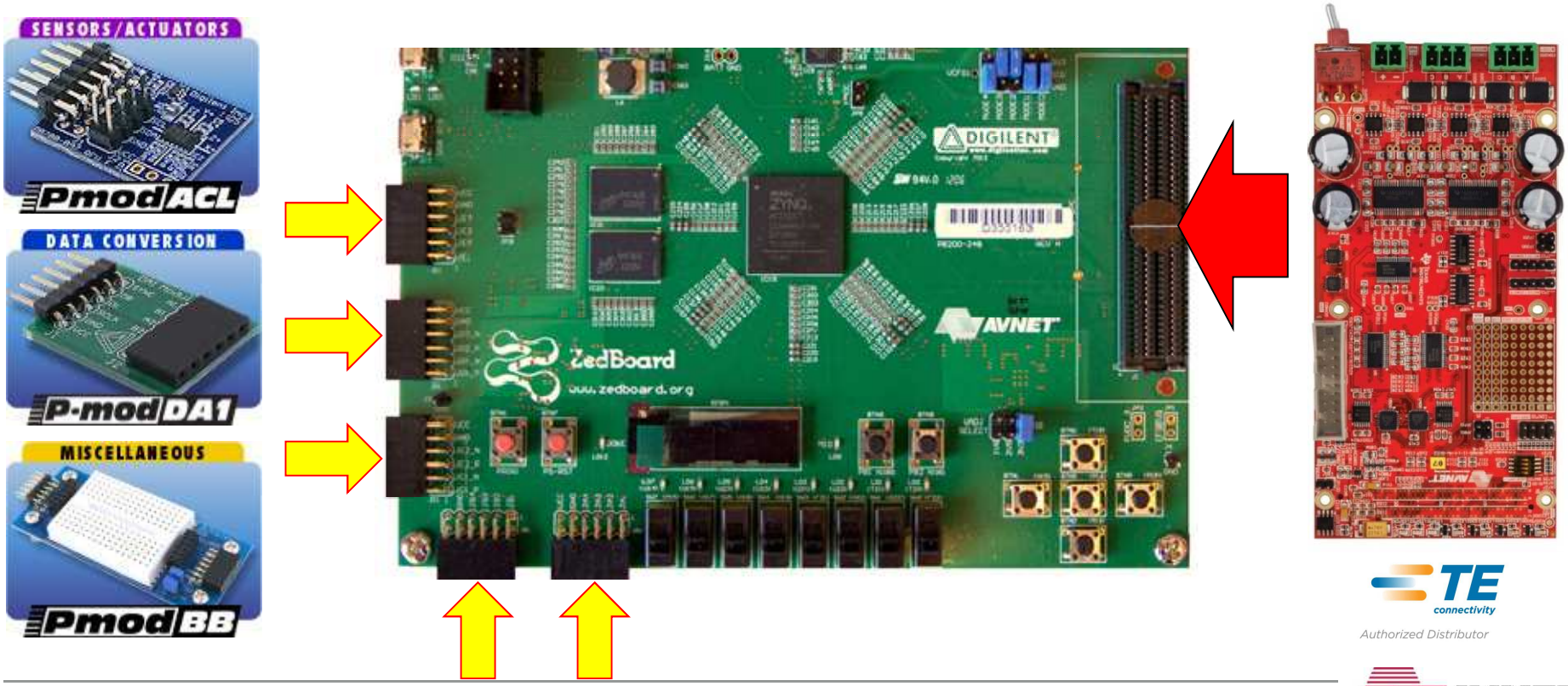
Prototyping designs has never been easier

Prototyping with Evaluation Boards

ANALOG DEVICES

Pmods

FMC

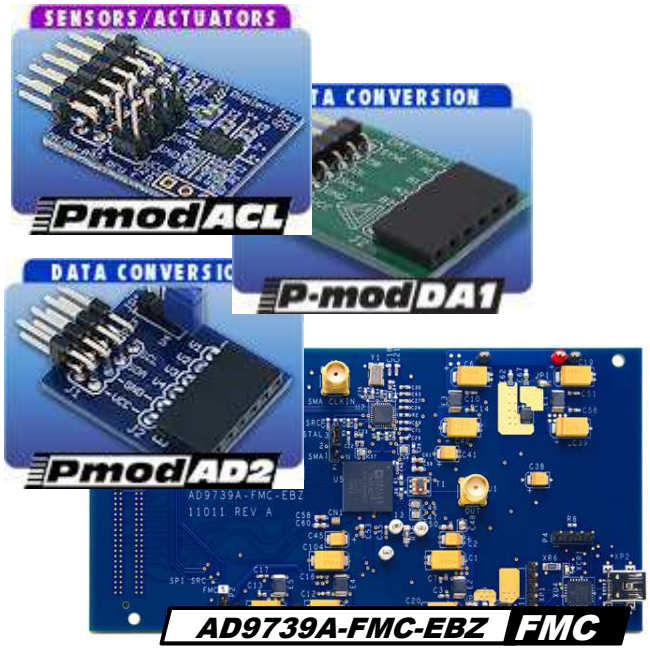


TE connectivity

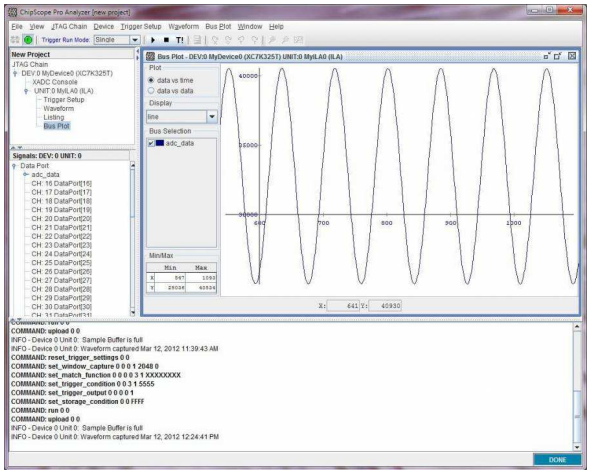
Authorized Distributor

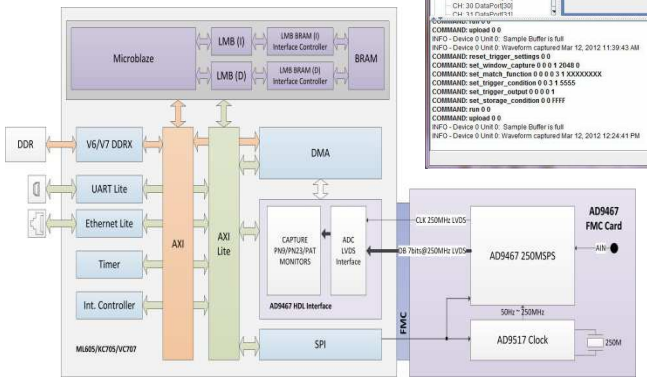
AVNET

Analog Devices Evaluation Boards



Reference Designs with Immediate Results





ANALOG DEVICES

Pmods

- 12-, 16-, and 24-bit ADCs
- 8-, 12-, and 16-bit DAC's
- 3-axis Accelerometer
- Gyroscope
- Digital Potentiometer
- I2C Temp Sensor

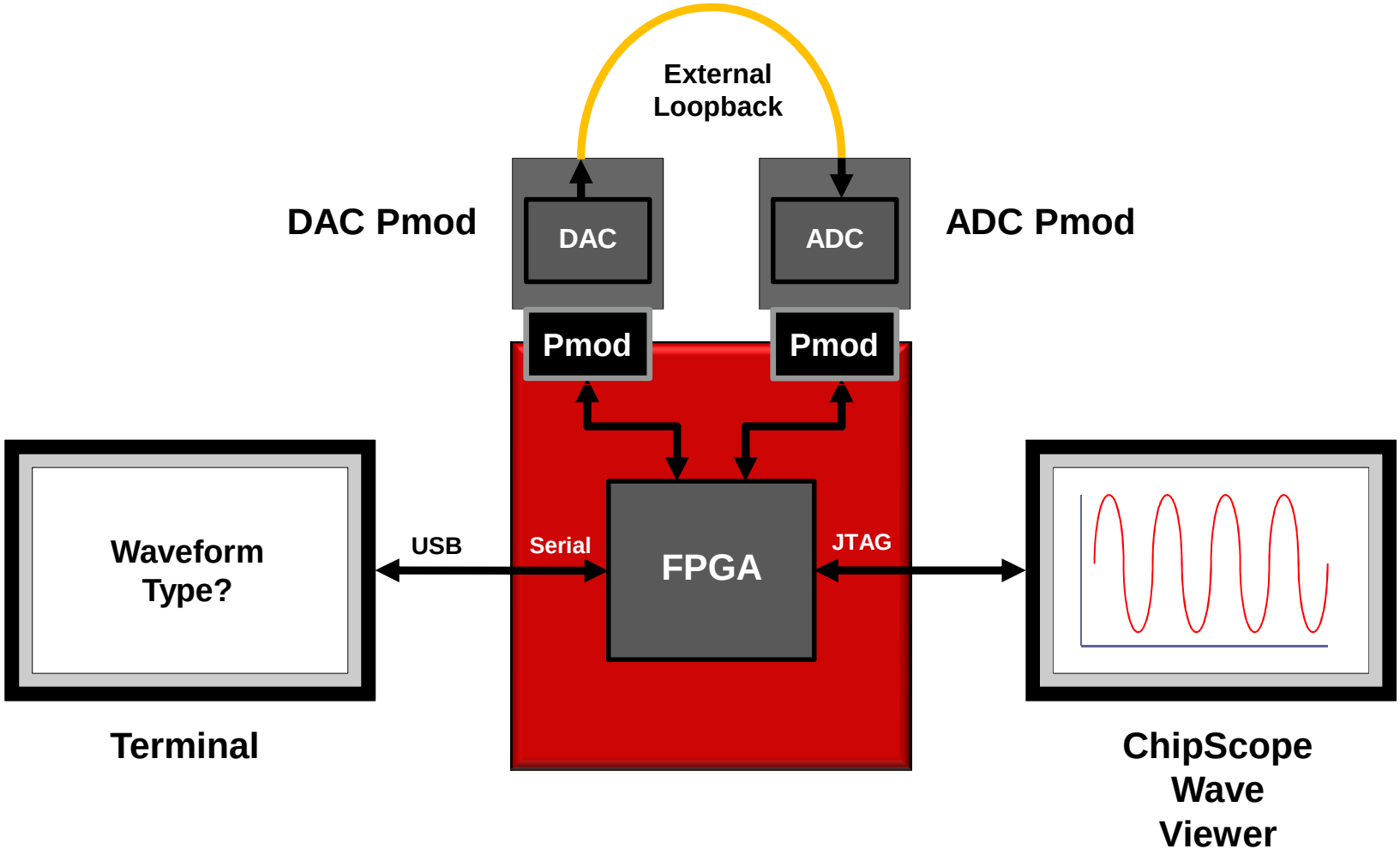
FMCs

- Hi-speed 14-bit DAC @ 2.5GSPS
- High-speed 16-bit ADC @ 250MSPS
- RF Transmit and Receive channels
- Interposer for SDP-B

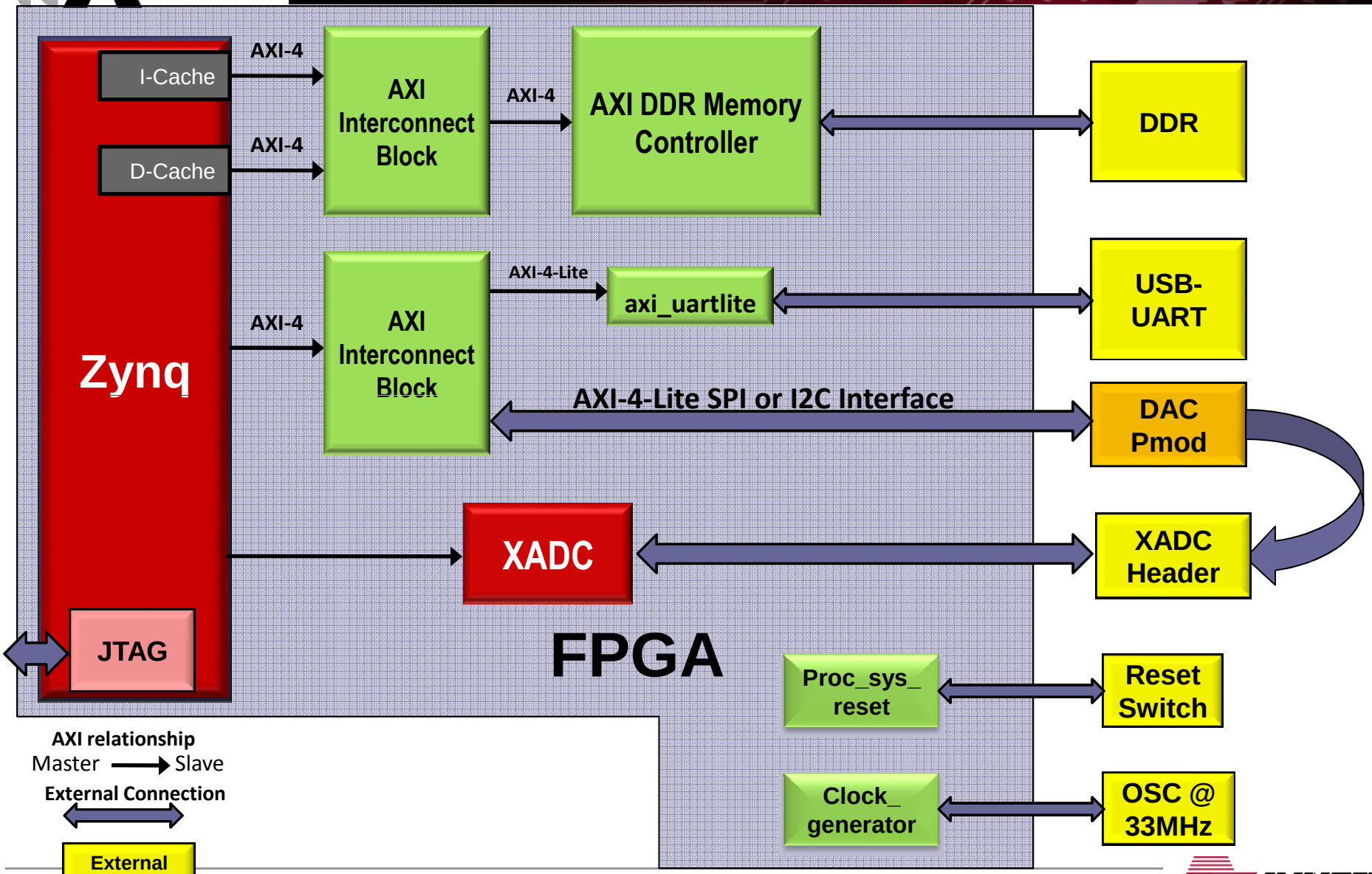
AMS

- Instrumentation Amplifier Board
- RF RMS Detector
- RF LogAmp Detector

Sample Pmod Reference Design



Embedded Platform



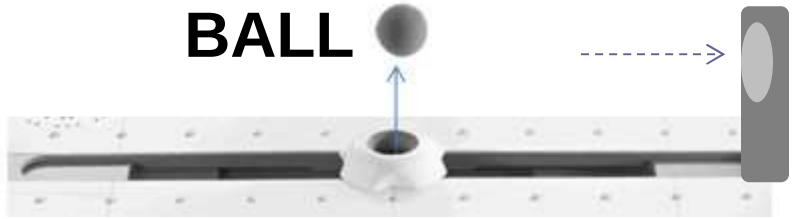
Why Analog at Xfest

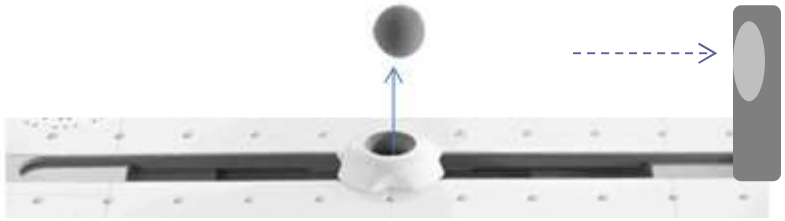
DEMO - Head To Head Race

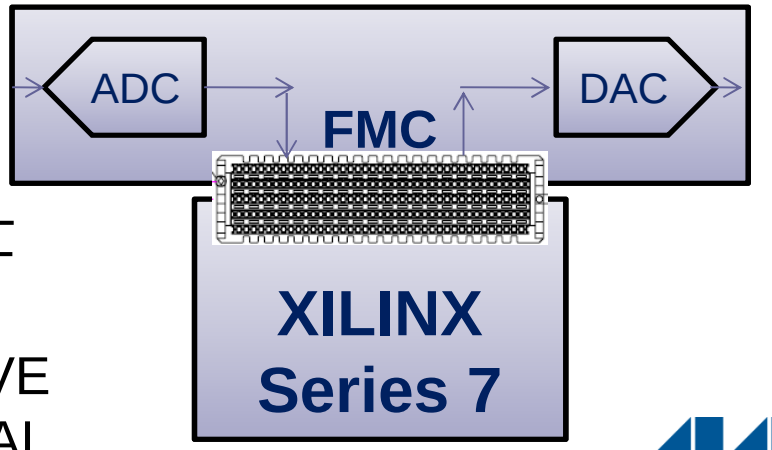
FLOATING BALL

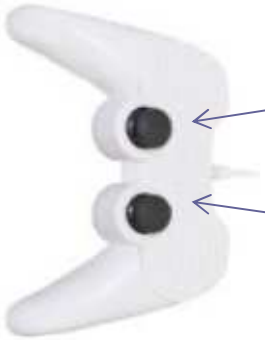
Player 1

Player 2









BALL HEIGHT

DRIVE TO GOAL

JOYSTICK

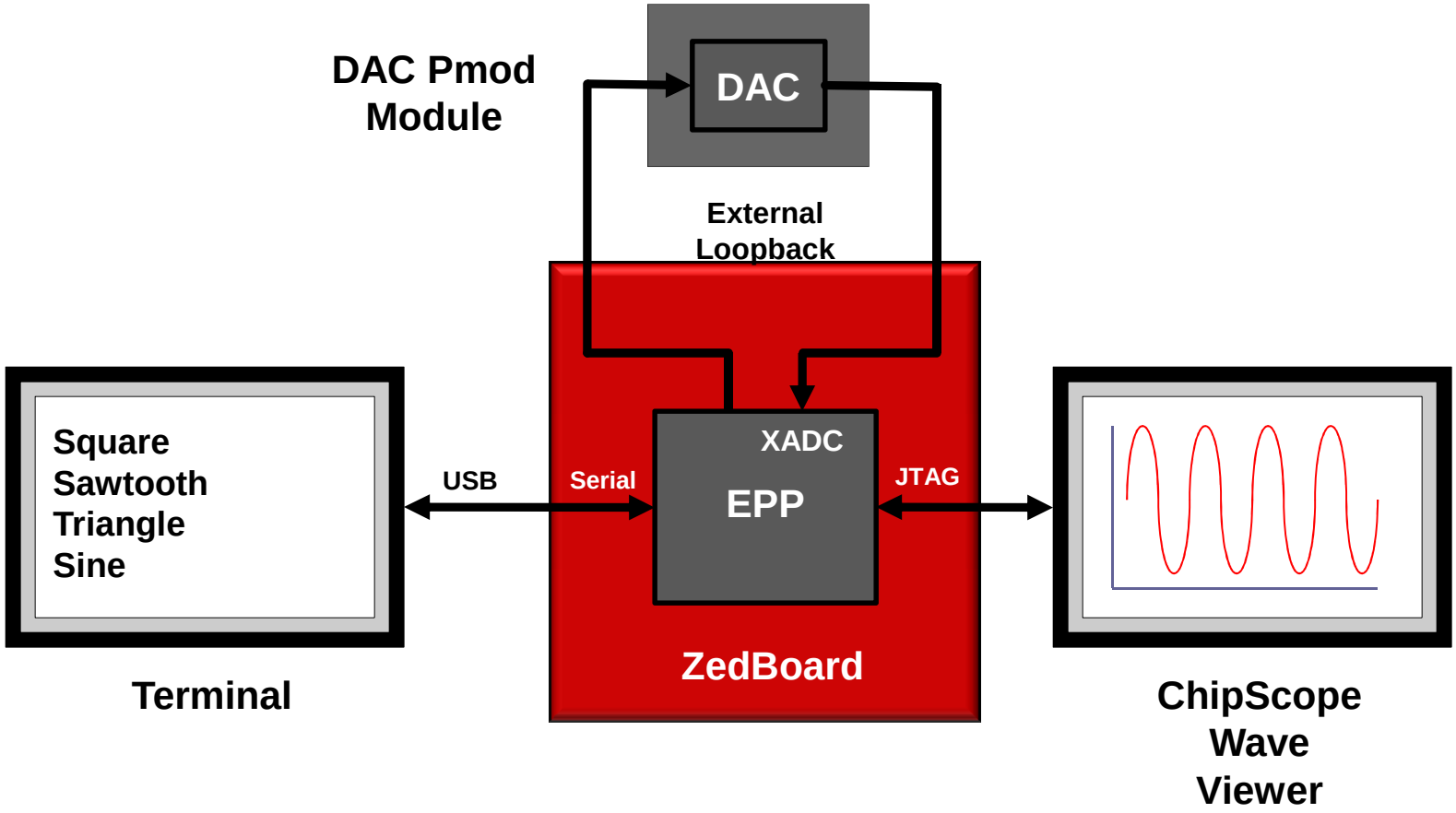
FIRST TO GOAL WINS

MAXIM INNOVATION DELIVERED®

AVNET®

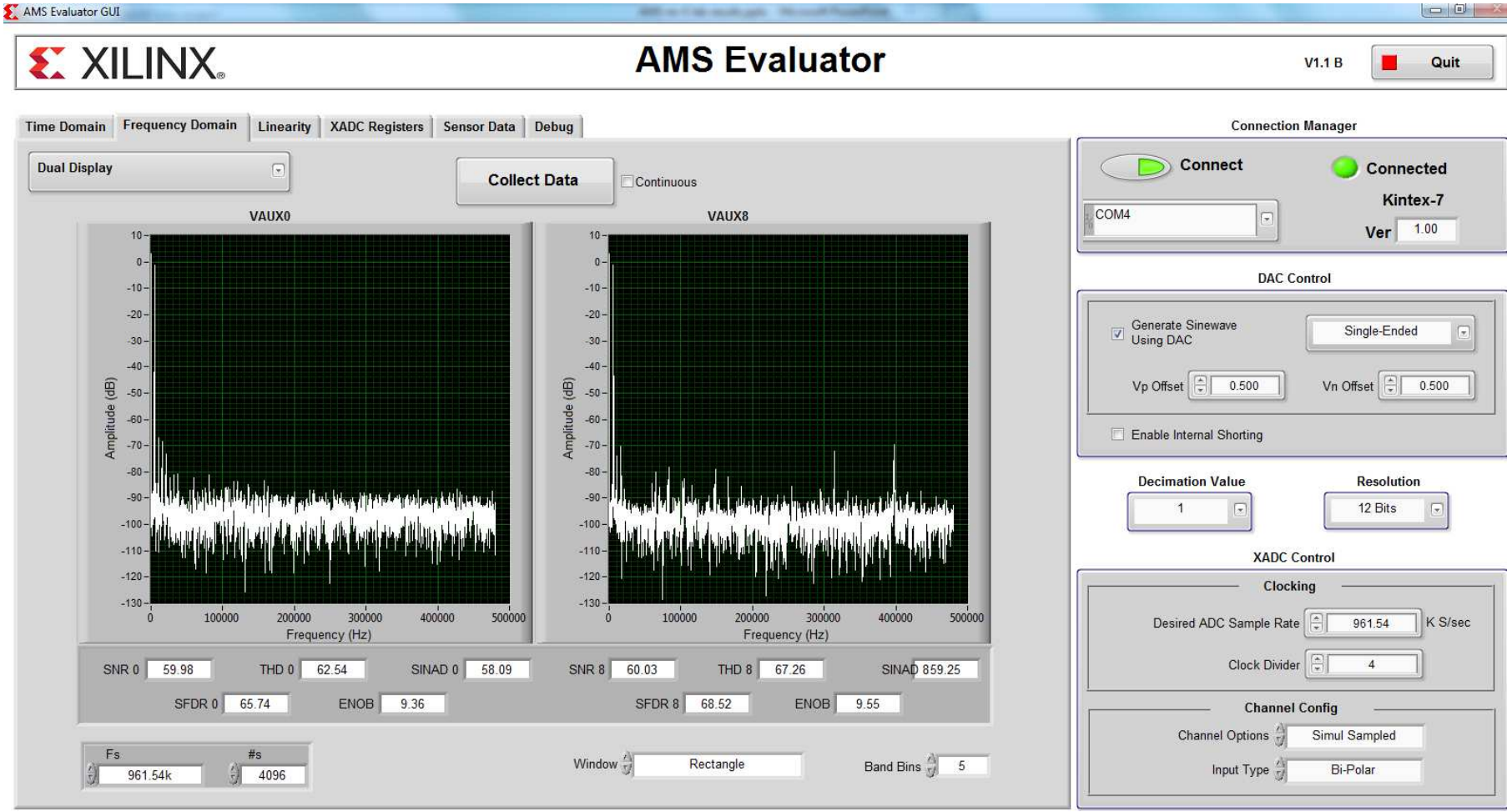
DEMO – ADC in Action

- **See XADC sampling real-time waveforms**



DEMO – AMS Evaluator

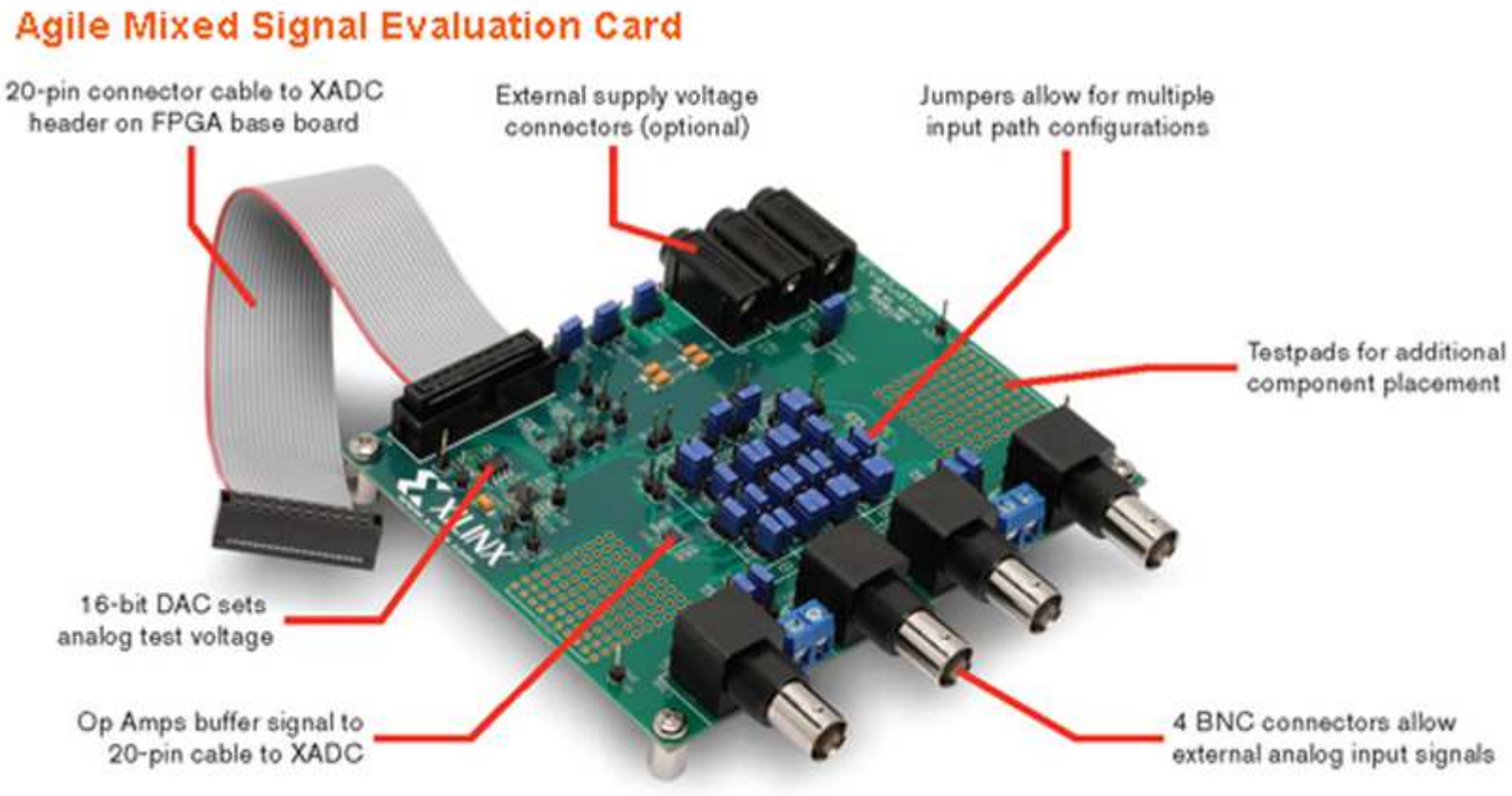
Evaluator, Frequency Domain Simultaneous Sampling



See it at the Xilinx Booth

AVNET

AMS Evaluation Card



Next Steps

- **Visit supplier tables to see running demos with evaluation boards**
- **Purchase an evaluation board with a Pmod or FMC**
- **Download our reference designs and experiment!**
- **Attend other Xfest courses**
  - Wireless Communication Systems Course
  - FPGA-Based Motor Control Course
- **Additional Training**
  - Avnet Speedway or On-Ramp Training
  - Xilinx Training
    - Agile Mixed Signaling
    - Any DSP/System Generator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