UG522: Mandatory Crystal Adjustment for EFR32ZG14/EFR32ZG23 Based Products User's Guide

This document describes the mandatory adjustment of the system crystal which must be performed on a product based on the EFR32ZG14 and EFR32ZG23 devices.

The purpose of this document is to describe the required method to match the system crystal of an EFR32ZG14- or EFR32ZG23-based products to the parasitic of that product. The procedure is required to ensure that the crystal tolerances of the product are within the specifications of the Z-Wave protocol.

KEY POINTS

- About Crystal Tolerances
- How to Adjust the System Crystal
- Effects of the System Crystal's Production Calibration
- Second Source Crystal Components

Audience:

The intended readers of this document are:

- Product design engineers
- Production test engineers
- Z-Wave application programmers

Prerequisites:

The readers of this document are assumed to have knowledge of:

- The Z-Wave protocol
- Basic RF knowledge
- Basic RF measurement skills

Access to the bring-up software tool RailTest is required.

Knowledge and access to the following documents are essential:

- [1] UG523: Bring-Up/Test HW Development User's Guide
- [2] AN961: Bringing Up Custom Devices for the Mighty Gecko and Flex Gecko Families

Table of Contents

1. Abbreviations

Abbreviation	Explanation
PCB	Printed Circuit Board
ppm	Parts Per Million
SoC	System on Chip

2. About Crystal Tolerances

The precision of the system crystal in a radio system, such as the Z-Wave radio system, is vital. If the transmitters and receivers in the Radio system are not operating with the correct clock frequency, and if the frequency difference between the parts is large, it will affect the obtainable range between the parts. This leads to customers experiencing a bad performance of the radio system. It is therefore mandatory to make sure that the system frequency of a radio product is as accurate as possible and adheres to the specifications of the radio protocol used, in this case, the Z-Wave protocol.

The total tolerance of a crystal is a sum of three contributions:

1. Initial tolerances
2. Temperature tolerances
3. Aging tolerances

For the Z-Wave protocol, the required tolerances for the crystal after five years of operation is ±27 ppm.

To avoid frequency harmonics in any Z-Wave frequency band, only a 39 MHz crystal is supported. The crystal requirements for EFR32ZG14 and EFR32ZG23 can be found in the table below.

Table 2.1. Crystal Requirements for EFR32ZG14 and EFR32ZG23

Chipset	Frequency	Total Tolerance	Load Capacitance (CL)	Shunt Capacitance (C0)	ESR
EFR32ZG14	39 MHz	±27 ppm	6-12 pF	Typically 2-3 pF	Max. 60 Ω
EFR32ZG23	39 MHz	±27 ppm	10 pF	Typically 2-3 pF	Max. 60 Ω

The recommended crystal parts for EFR32ZG14 and EFR32ZG23 can be found in the table below.

Table 2.2. Recommended Crystal Parts

Chipset	Crystal Manufacturer	Crystal Part Number	ESR (Ω)	C0 (max) (pF)	Temp (°C)	Temp Toler-ance (ppm)	Mfg Tolerance (ppm)	Aging (ppm)	CL (pF)	Footprint (mm)
EFR32ZG14	TXC	8Y39072002	35	1	-40 to +95	±13	±7	±2	10	2.0 x 1.6
EFR32ZG23	Tai-Saw	TZ3541C	35	2	0 to +50	±16	±8	±3	10	2.0 x 1.6

Note: The crystal parts in this table are the ones used for validation and characterization of the specific Z-Wave devices. However, both parts meet the crystal requirements for EFR32ZG14 and EFR32ZG23 (see Table 2.1 Crystal Requirements for EFR32ZG14 and EFR32ZG23 on page 4); therefore, both can be used with any of these Z-Wave devices. List of alternative crystal parts can be found in Table 5.1 Second Source Crystal Components on page 10 in section 5. Second Source Crystal Components.

The Initial tolerances are affected by:

- Parasitic load capacitance at the crystal component connections
- Parasitic load of the Z-Wave SoC
- Pressure exerted on the component package

The Temperature tolerances are affected by:

- The temperature of the environment

The Aging tolerances are affected by:

- Overdrive of the crystal
- Overheat of the component

- Mechanical stress due to normal usage

If it is assumed that the crystal is not stressed in any way, not mechanically nor electrically, there are two parameters left, which can give a tolerance change for the crystal, i.e., change the frequency of the crystal. These parameters are: the parasitic load capacitance added by the PCB of the product and the differences of the load capacitance of the crystal oscillators for the individual Z-Wave SoCs.

Depending on the implementation of the crystal oscillator circuit of an SoC, external load-caps may be required. However, this is not the case for the EFR32ZG14 or the EFR32ZG23 devices, where the load-caps are integrated on the die of the chipsets, as illustrated in the figure below:

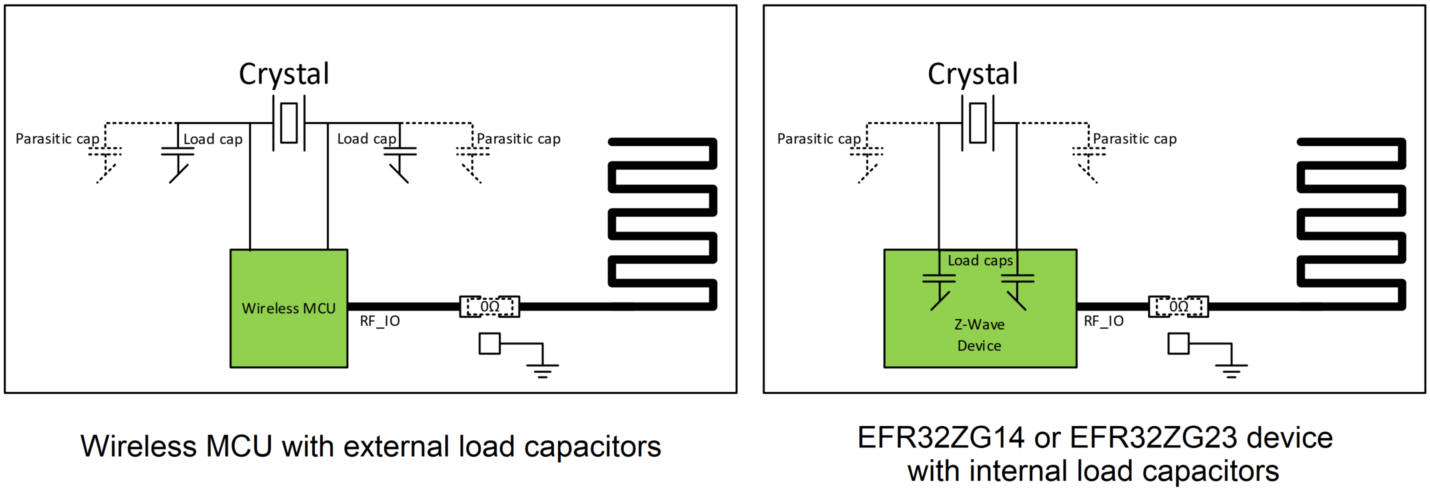

Figure 2.1. External vs. Internal Load Capacitance

The amount of parasitic capacitance seen by the crystal depends on:

- Trace length
- PCB material properties
- Differences in the internal size of the SoC load caps

These parameters vary from product-design to product-design and from Z-Wave SoC to Z-Wave SoC.

To counteract the parasitic load capacitance of the PCB, device implementation, and Z-Wave SoCs, the Z-Wave protocol offers the possibility to adjust the internal load capacitances in such a way that the total capacitance seen by the crystal fulfills the crystal specifications.

3. How to Adjust the System Crystal

As described in Section 2. About Crystal Tolerances, implementing the 39MHz system crystal on a PCB and connect it to the Z-Wave SoC will affect the crystal frequency. This is due to the parasitic load capacitance added to the crystal terminals by the traces from the Z-Wave device to the crystal component and due to the variance in the internal load capacitance of the Z-Wave SoCs.

To counteract the added parasitic load capacitance, the Z-Wave protocol offers the possibility to change the value of the internal load capacitance in such a way that the sum of the internal load capacitance and the parasitic load capacitance is equal to the nominal load capacitance of the crystal. When the crystal operates with the nominal load capacitance, the frequency of the crystal will also be the nominal frequency:

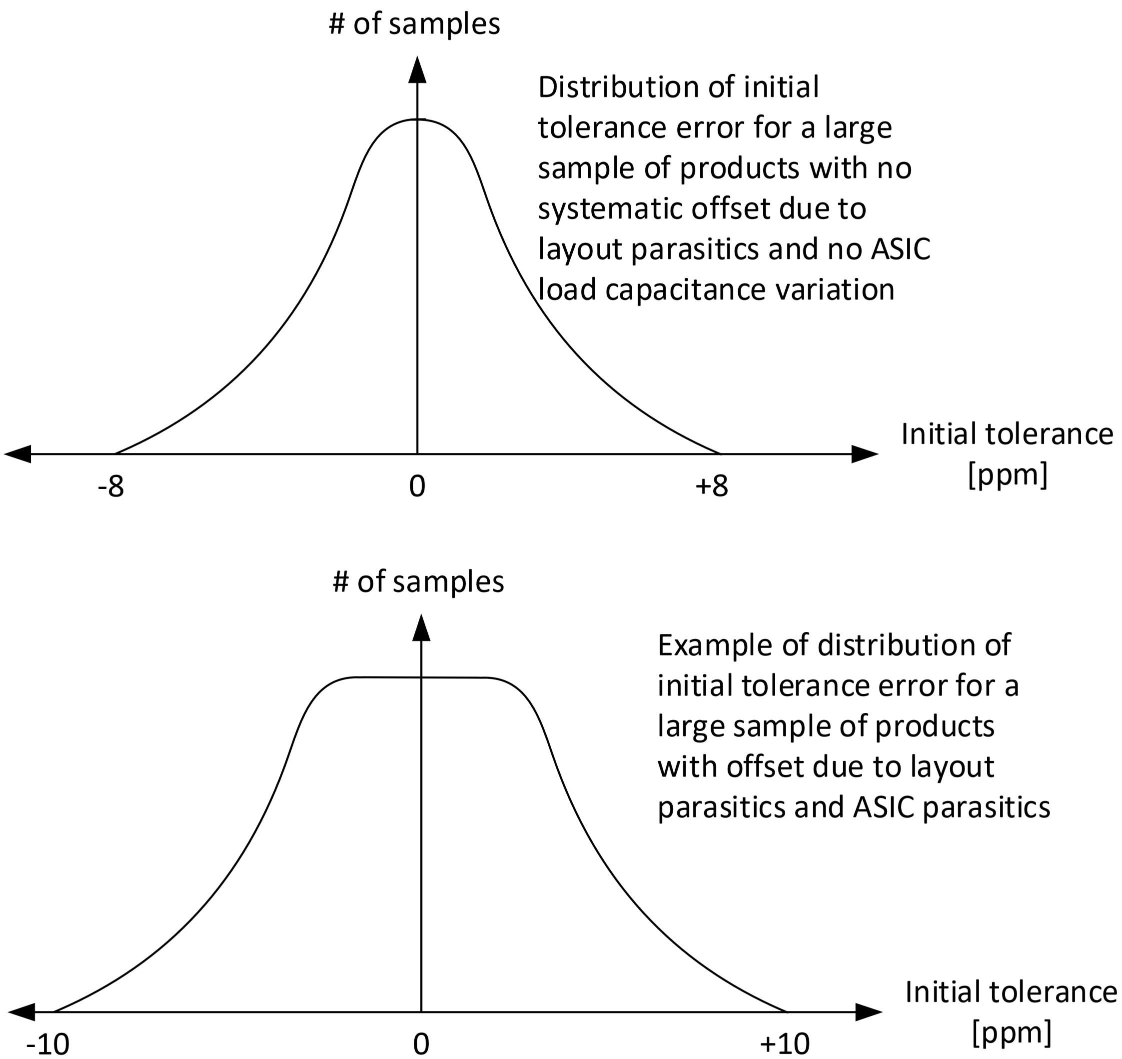

Figure 3.1. Offset Error Due to Parasitic Load Capacitance

The figure above shows how the distribution of the initial frequency errors will be for two various products: one ideal product (not realistic to realize) with no parasitic capacitances at all and one product with a parasitic capacitance from both the PCB and the Z-Wave SoC.

The frequency error of an RF-enabled product can be measured by measuring the RF frequency of a Carrier Wave (CW) transmitted by the product. If the product is designed for the EU region, and a CW is enabled for, as an example, channel 2, then any measured average frequency offset from 868420000 Hz is an RF frequency error that must be corrected.

Refer to [1] to see how a CW is set up in connection with the usage of the test software RailTest.

Since the parasitic capacitances seen by the crystal consists of two parts: A “stationary part” origin from the PCB traces and a “variable part” origin from the variation of the internal load capacitances of the Z-Wave SoC, each individual product of the product range must be calibrated during the production flow.

The frequency of a product is changed by adjusting a value called the CTune value. The determination of the CTune value for each part is an iterative process and can be described as shown below:

Table 3.1. CTune Measurement Method

1	Program RailTest to the item to calibrate. Refer to [1] for more information.
2	For each item, follow the procedure described in [1] and measure and adjust the CW frequency.
3	Using the method described in [1], adjust the CTune value for this item until $f_{measured} = f_{target}$.
4	Program the found CTune value for the item into the flash memory of the Z-Wave SoC [2] and [3]

The found CTune value is incorporated into the Z-Wave protocol by setting the token TOKEN_MFG_CTUNE equal to the CTune value found. For handling of manufacturing tokens, refer to [2].

Once adjusted, the average frequency error should be within ±1 ppm for each product item at 25°C.

The CTune found is valid for the specific product item. If the firmware is updated, the new firmware must use the initially found CTune value. In other words, the CTune value must follow the product item during its entire life.

4. Effect of the Production Calibration the System Crystal

Section 3. How to Adjust the System Crystal describes how to remove the frequency offset of a product. This will ensure that the system frequency error is reduced to ±1ppm.

When each product is production calibrated, the net result will be as shown below:

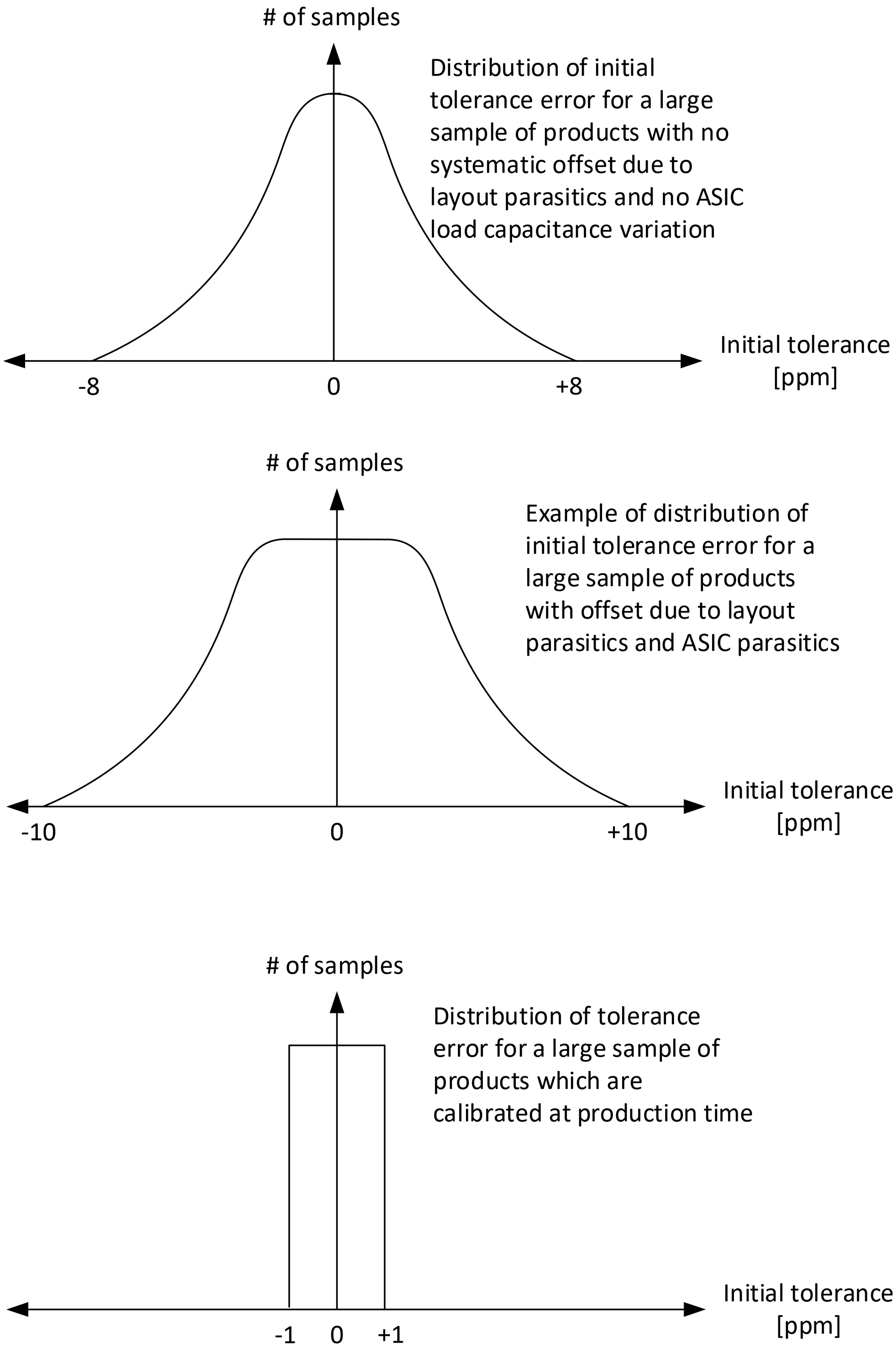

Figure 4.1. Effect of Production Calibration

As seen from the figure above, the initial crystal tolerance is at ±8 ppm, and the offset due to layout parasitic and Z-Wave SoC variance is reduced to e.g., ±1 ppm since each product is individually measured and calibrated.

To sum up: to individually calibrate each product item, one must:

1. Be able to download RailTest during the manufacturing of the product
2. Be able to control RailTest during the manufacturing of the product
3. Be able to precisely measure a CW from the product with a precision of ±1 ppm
    a. With the aid of a spectrum analyzer or an RF frequency counter
4. Be able to derive a CTune value from the frequency measured
5. Be able to incorporate the CTune value found into the Z-Wave protocol code to download

As seen in the procedure description above, the CTune value found must be incorporated into the Z-Wave protocol. This is done in the form of a TOKEN_MFG_CTUNE value, with value = CTune, which is programmed into memory according to the description given in [2].

5. Second Source Crystal Components

In case a second source HFXO is needed, the below components are suggested:

Table 5.1. Second Source Crystal Components

Crystal Manufacturer	Crystal Part Number	ESR (Ω)	C0 (max) (pF)	Temp (°C)	Temp Tolerance (ppm)	Mfg Tolerance (ppm)	Aging (ppm)	CL (pF)	Footprint (mm)
Tai-Saw	TZ3541B	35	1	-40 to +105	±16	±7	±2	10	2.0 x 1.6
Siward	XTL501170-S315-031	35	3	-40 to +105	±17	±6	±2	10	2.0 x 1.6
Siward	XTL501350-S315-027	40	3	-40 to +85	±15	±8	±3	10	2.0 x 1.6
Siward	XTL501140-S315-020	50	3	-40 to +90	±14	±8	±3	10	2.0 x 1.6
TXC	8Y39072004	35	2	-40 to +105	±16	±7	±2	10	2.0 x 1.6

Other crystal vendors that meet these requirements can be used.

Note: The “CTune” value must be measured and applied to each unit manufactured.

Note: Selecting a crystal is an important step in the design of an end-product. Once an end-product has obtained RF regulatory certifications, the RF regulatory authorities do not allow the change of the crystal without re-certification.

6. References

1. UG523: Mandatory Crystal Adjustment for EFR32ZG14/EFR32ZG23 Based Products User's Guide
2. AN961, Bringing Up Custom Devices for the Mighty Gecko and Flex Gecko Families.
3. INS14285, Z-Wave product in volume

7. Revision History

Revision 8

December, 2021

- Extend document to include EFR32ZG23
- Updated document format and replacing INS14498 "Mandatory Crystal Adjustment for EFR32ZG14 Based Products"

Revision 7

June, 2020

- Standard Technical Publications review

Revision 6

June, 2020

- Removed description of batch calibration since this has proven not to be correct. Each individual product item must be calibrated.

Revision 5

September, 2019

- Reviewed Sections 3, 4, and 6

Revision 4

August, 2019

- Added Second Source description

Revision 3

March, 2019

- Emphasized that only a 39 MHz crystal is supported.
- Corrected crystal type number.
- Updated drawing, showing internal cap in EFR32ZG14.
- Rephrased wording at the start of the section.
- Added a table-structure for CTune measurement method

Revision 2

January, 2019

- Section 2, 5, and 7: Type errors fixed and corrected sentences
- Grammar and structure (consistent format) modification

Revision 1

December, 2018

- Initial version
- Added how to populate the CTune value as a manufacturing token.

IoT Portfolio
www.silabs.com/products

Quality
www.silabs.com/quality

Support & Community
www.silabs.com/community

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701