UG453: RS9116X EVK HW User's Guide

Version 1.9

June 28, 2021

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About this Document

This document contains pertinent information on the RS9116 Module's Evaluation Board and its usage for evaluating Silicon Labs' RS9116 based ultra-low-power, single spatial stream, dual-band 802.11n + BT 5.0 Convergence modules.

Note:

Contents of this document apply to both WiseConnect and n-Link modules.

1 Overview

The RS9116 Evaluation Kit consists of RS9116 Module Evaluation Board (EVB), a platform for evaluating the RS9116 modules with multiple Host Processors/MCUs over interfaces like SPI, USB-CDC, SDIO, USB and UART. Silicon Labs' RS9116 wireless modules with single and dual-band provide a comprehensive multi-protocol wireless connectivity solution including 802.11 a/b/g/n (2.4/5 GHz), and dual-mode Bluetooth 5. The wireless modules offer high throughput, extended range with power-optimized performance. The wireless modules are FCC, IC, and ETSI/CE certified.

Note:

Refer to ***Getting Started with RS9116 EVK and WiSeConnect*** at https://docs.silabs.com/rs9116/latest/wiseconnect-getting-started, for a quick evaluation of RS9116W.

Refer to ***Getting Started with n-Link*** at https://docs.silabs.com/rs9116/latest/nlink-documentation, for a quick evaluation of the Evaluation Board.

All the latest user-level Documents, Firmware Release packages, certifications of the module, and other materials related to the RS9116-based modules are available in https://www.silabs.com/wireless/wi-fi/rs9116-wi-fi-ncp-modules click the ***View Documentation*** link.

For SDIO and USB Interface, contact Silicon Labs Sales Team at https://www.silabs.com/about-us/contact-sales for availability.

2 Evaluation Kit Details

2.1 Evaluation Kit Part Numbers

2.1.1 Ordering Information for Evaluation Kits

Single Band - RS9116X-SB-EVK1, RS9116X-SB-EVK2
Dual-Band - RS9116X-DB-EVK1

2.1.2 Related Links

- https://www.silabs.com/wireless/wi-fi - Check for RS9116 Wi-Fi NCP and Transceiver Modules

2.2 Evaluation Kit Contents

The RS9116 Module Evaluation Kit comes with the following components:

1. RS9116 Module Evaluation Board (EVB)
2. Micro A/B-type USB cable
3. SDIO Adaptor Cable
4. SPI Adaptor Cable
5. EFX32-CON-BRD - Interconnect Board for connecting to Silicon Labs WSTK[1]
6. SPI cable for EFX32-CON-BRD
7. Jumper wires

It is highly recommended to use the Micro A/B type USB cable that comes with the kit. If a longer cable is needed ensure that you use a USB-IF certified cable which can supply peak current of at least 500mA.

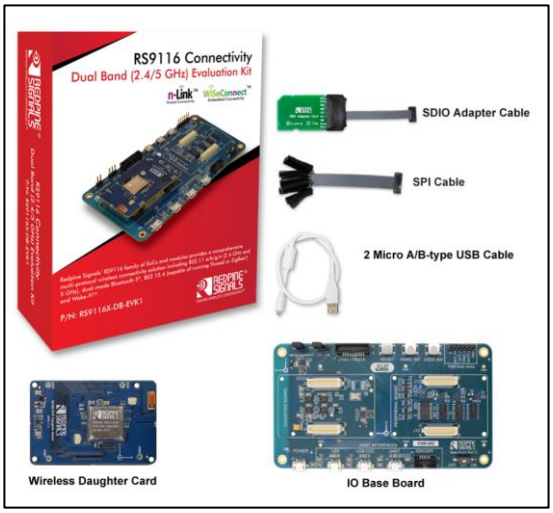


Figure 1: Evaluation Kit Contents

[1] Contact Silabs sales if user has an earlier kit and would like to get the interconnect board EFX32-CON-BRD.

3 Evaluation Board Hardware Details

This section describes RS9116 EVB's various components and headers.

As shown in the image below, the RS9116 EVB has four USB connectors for the Power, USB, USB-CDC, and UART connections. The UART signals of the module are converted to USB using on-board circuit. The board also has an SDIO/SPI header.

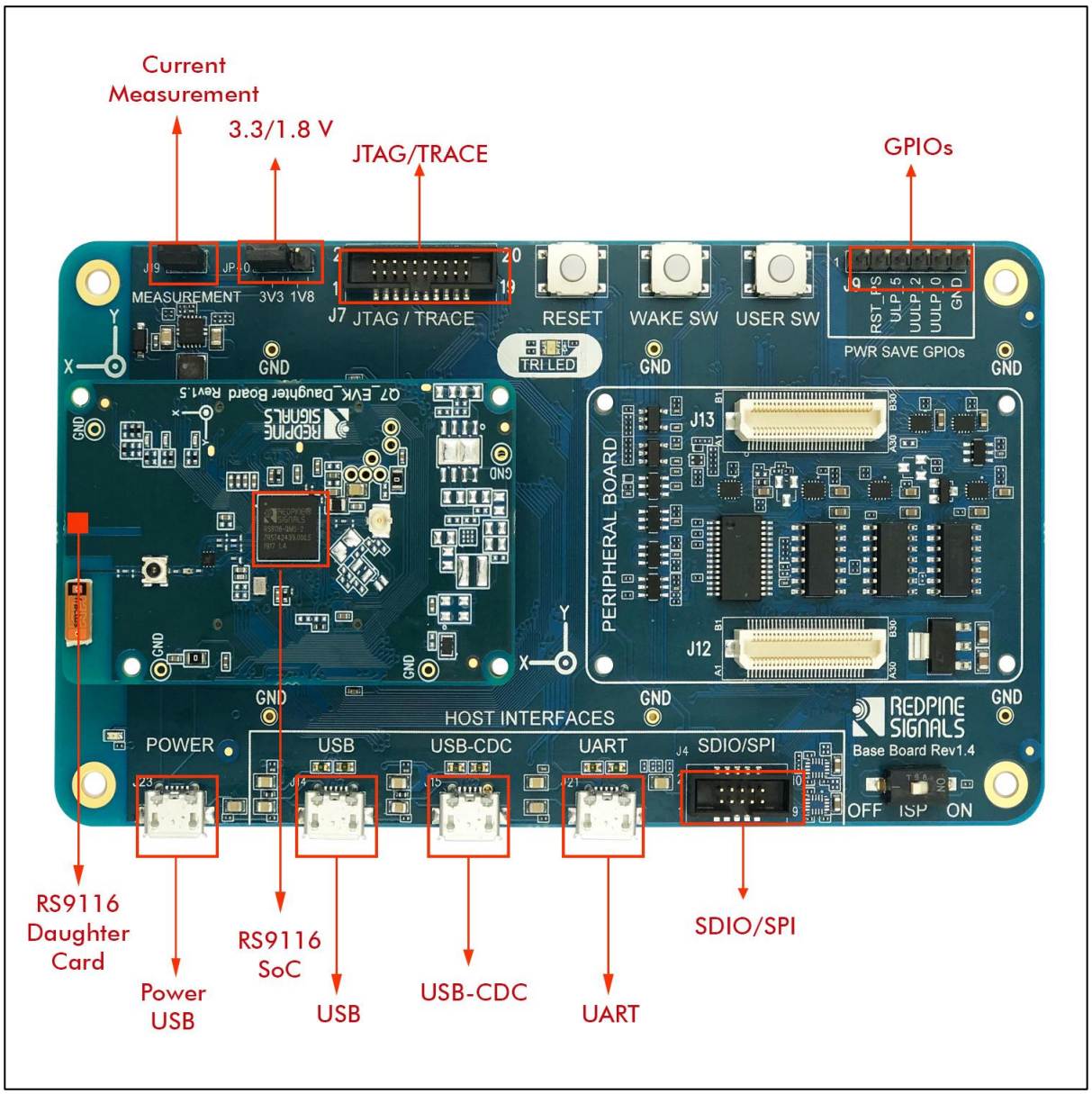


Figure 2: RS9116 EVB

The board is designed to configure the module to use the interface on which power supply is detected. The SDIO and SPI interfaces require the power supply to be provided over the POWER port using a USB cable. Hence, for these interfaces, it is required that the USB Power connection be provided first followed by the SDIO or SPI connection. Follow the steps below to use the EVB with different interfaces:

1. USB, UART, USB-CDC Modes
   a. Connect the Micro A/B-type USB cable between a USB port of a PC/Laptop and the micro-USB port labeled USB, UART, or USB-CDC on the EVB. The USB, USB-CDC, and UART connections also provide power, so only one USB cable needs to be connected.

2. SPI Mode
    a. Connect the Micro A/B-type USB cable between a USB port of a PC/Laptop and the micro-USB port labeled POWER on the EVB.
    b. Connect the 10-pin header of the SPI Adaptor Cable to the EVB. Connect the other wires of this connector to the SPI signals of a Host MCU platform. The details of the Header are given in section Headers on the EVB.
3. SDIO Mode
    a. Connect the Micro A/B-type USB cable between a USB port of a PC/Laptop and the micro-USB port labeled POWER on the EVB.
    b. Connect the 10-pin header of the SDIO Adaptor Cable to the EVB. Connect the other wires of this connector to the SDIO signals of a Host MCU platform. The details of the Header are given in section Headers on the EVB.

There is a 2-pin inline jumper available for measuring the current being sourced by the module during different stages of operation. This is labeled as "MEASUREMENT" on the baseboard. The user may connect a power meter or an ammeter to this jumper to measure the current.

Note:

Assembly drawings of this EVB (Base Board and Daughter Board (CC1 and QMS)) can be found in Section 6: EVB Assembly Drawings.

Some of the critical parts' Reference Designators of this EVB are shown below:

- J19 - Power Measurement (Connect power meter's negative terminal on pin #1 and positive on pin #2)
- JP40 - Select between 3.3 V or 1.8 V supply voltage
- J7 - JTAG/TRACE header
- J9 - Power Save GPIOs
- J23 - Power to the EVK
- J14 - USB connection/power
- J15 - USB-CDC connection/power
- J21 - UART connection/power
- J4 - SDIO/SPI header

Make sure the ISP switch is in the OFF state. If it is ON state, boot loader messages will be displayed.

Important Note:

If the baseboard Rev is 1.1 or below, follow this procedure:

1. For SDIO/SPI, insert the USB into the Power port first before the SDIO/SPI connector is connected to the Host platform.
2. For USB and USB-CDC, please connect the USB port to the Host platform first before connecting the USB for the Power port.

4 Headers on the EVB

4.1 Headers' Pin Orientations

The figure below shows the pin orientations for the SDIO/SPI header.

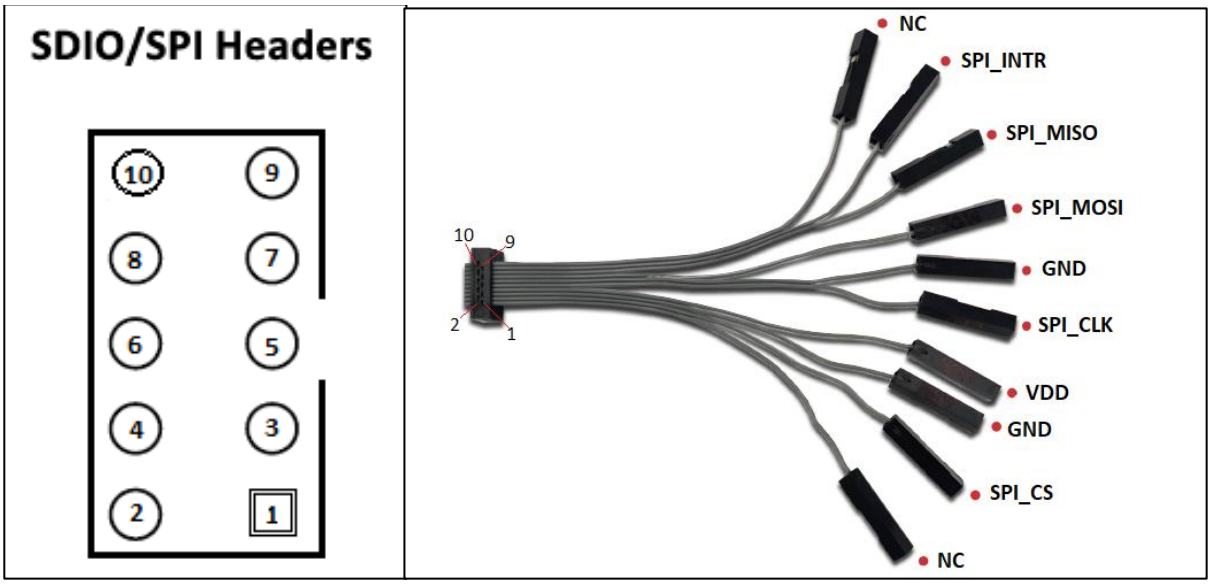


Figure 5: Headers' Pin Orientations

4.2 SPI Header Pin Description

The following table describes the pins of the SPI header.

Table 1: SPI Header Pins

Pin Number	Pin Name	Direction	Description
1	NC	-	This pin must be left open
2	SPI_CS	Input	SPI slave, select from the host (active low)
3	GND	-	Ground
4	VDD	-	Supply voltage
5	SPI_CLK	Input	Serial clock in from the host. The clock can be up to80 MHz
6	GND	-	Ground
7	SPI_MOSI	Input	SPI data input
8	SPI_MISO	Output	SPI data output
9	SPI_INTR	Output	Active high, level triggered interrupt, used in SPI mode. The interrupt is raised by the Evaluation Board to indicate there is data to be read by the Host.
10	NC	-	No Connect

4.3 SDIO Header Pin Description

The following table describes the pins of the SDIO header.

Table 2: SDIO Header Pins

Pin Number	Pin Name	Direction	Description
1	SDIO_DATA3	Input/Output	Data3 of the SDIO interface.
2	SDIO_CMD	Input/Output	SDIO Mode: SDIO interface command signal.
3	GND	-	Ground
4	VDD	-	Supply voltage.
5	SDIO_CLK	Input	This signal is the SDIO clock.
6	GND	-	Ground
7	SDIO_DATA0	Input/Output	Data0 of the SDIO interface.
8	SDIO_DATA1	Input/Output	Data1 of the SDIO interface.
9	SDIO_DATA2	Input/Output	Data2 of the SDIO interface.
10	NC	-	No Connect

Reset - When the EVB is powered through the USB on "Power" port or through the power on any interface (UART, USB, USB-CDC, SDIO/SPI) then it gets the Power-on Reset.

To control the reset there are two methods:

1. Reset Button on the baseboard.
2. The host can control the Reset by controlling the pin #2 (RST_PS) on header J9 via GPIO.

Note:

Signal Integrity Guidelines for SPI/SDIO interface: Glitches in the SPI/SDIO clock can potentially take the SPI/SDIO interface out of synchronization. The quality and integrity of the clock line need to be maintained. In case a cable is used for the board to board connection, the following steps are recommended (please note that this is not an exhaustive list of guidelines and depending on individual cases additional steps may be needed):

1. Minimize the length of the SPI/SDIO bus cable to as small as possible, preferably to within an inch or two.
2. Increase the number of ground connections between the EVB and the Host processor PCB.

4.4 PWR Save GPIOs Header Pin Description

J9 is a 6 pin header has Reset and power save mode related GPIOs. Following table provides the details:

Table 3: GPIO Header Pins

Pin Number	Pin Name	Direction	Description
1	-	-	Reserved
2	RST_PS	Input	**Pin Name on SoC/Module:** RESET_N (Active Low) The host can control the Reset by controlling this pin via MCU GPIO.
3	ULP_5	Input	**Pin Name on SoC/Module:** ULP_GPIO_5 LP_WAKEUP_IN : This is LP mode Power save Wakeup indication to Device from HOST
4	UULP_2	Input	**Pin Name on SoC/Module:** HOST_BYP_ULP_WAKEUP This signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from its Ultra Low Power (ULP) sleep mode.
5	UULP_0	Output	**Pin Name on SoC/Module:** UULP_VBAT_GPIO_0 SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.
6	GND	-	Ground

5 EFX32-CON-BRD

EFX32-CON-BRD is designed to enable easier SPI and GPIOs (Reset and power save) connections with Silicon Labs WSTK boards and RS9116W evaluation boards.

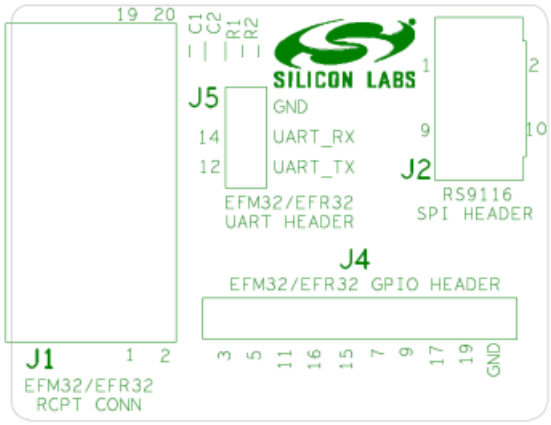


Figure 4: EFX32-CON-BRD

J1 Connector on the EFX32-CON-BRD can be directly plugged into EXP header of different STK boards.

Please refer WSTK getting started guide with RS9116W for more details on the SPI and other GPIO connections for respective WSTK on EXP header.

Below is the setup diagram where Simplicity Studio IDE is used on PC to program and debug examples for RS9116W with Silicon Labs WSTK board.

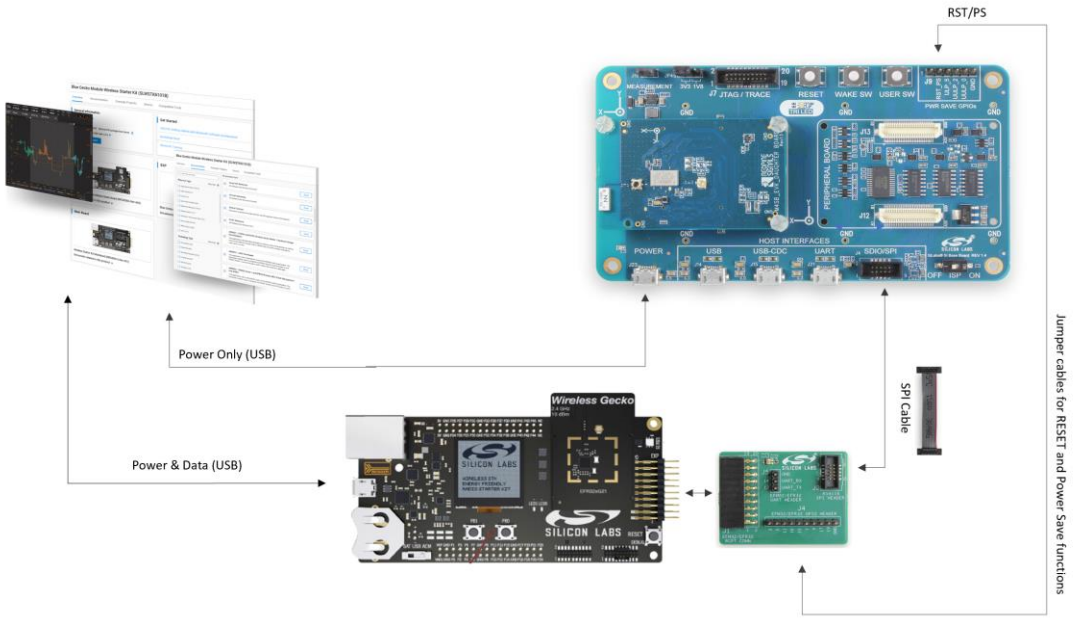
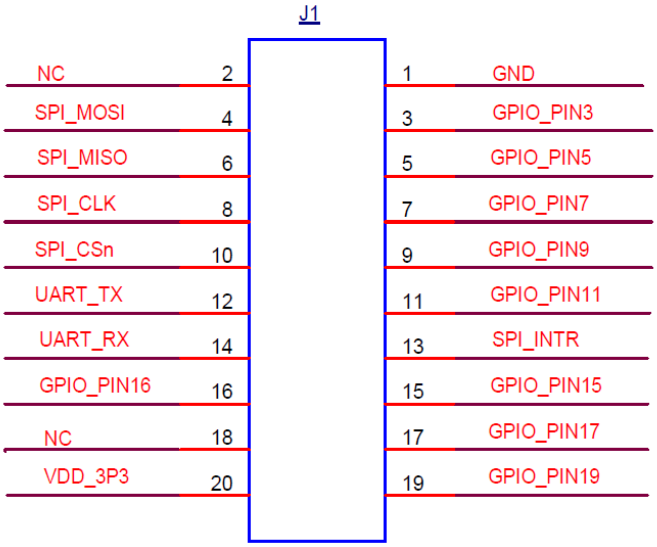


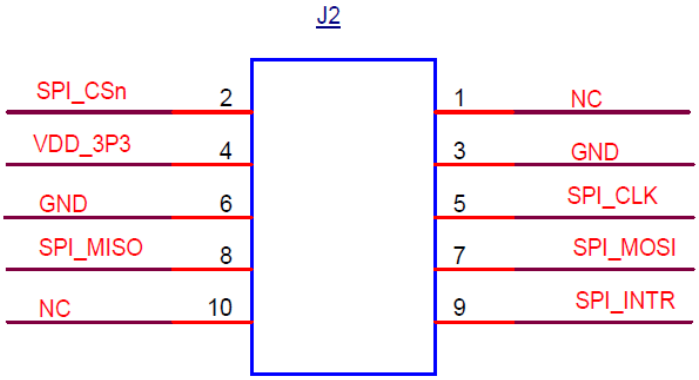
Figure 5: RS9116W + WSTK with EFX32-CON-BRD Setup Diagram

5.1 J1 Header Pin Details

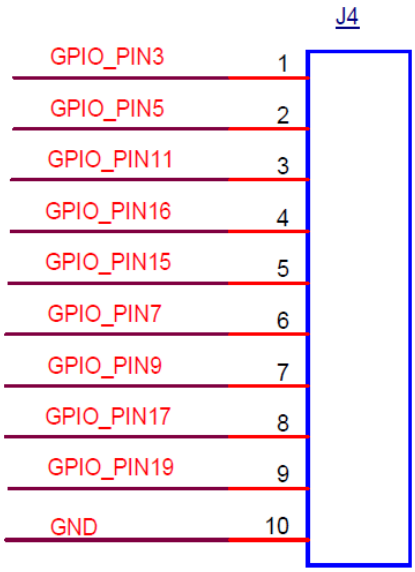


5.2 J2 Header Pin Details

This is having same connections as J4 header (SPI/SDIO) on RS9116 EVB.



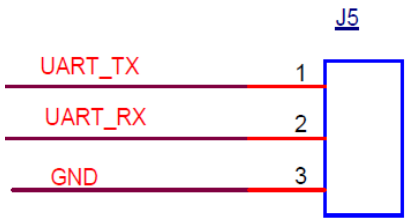
5.3 J4 Header Pin Details



Note:

These GPIO pins are used to connect the low power handshake and reset signals between the WSTK and the RS9116X EVK board via a connector board. Specific GPIO pin selection depends on the EFx Radio Board or EFM board. Please refer to the respective Getting Started with EFx steps for more connection details.

5.4 J5 Header Pin Details



6 EVB Assembly Drawings

6.1 Base Board Assembly Drawings:

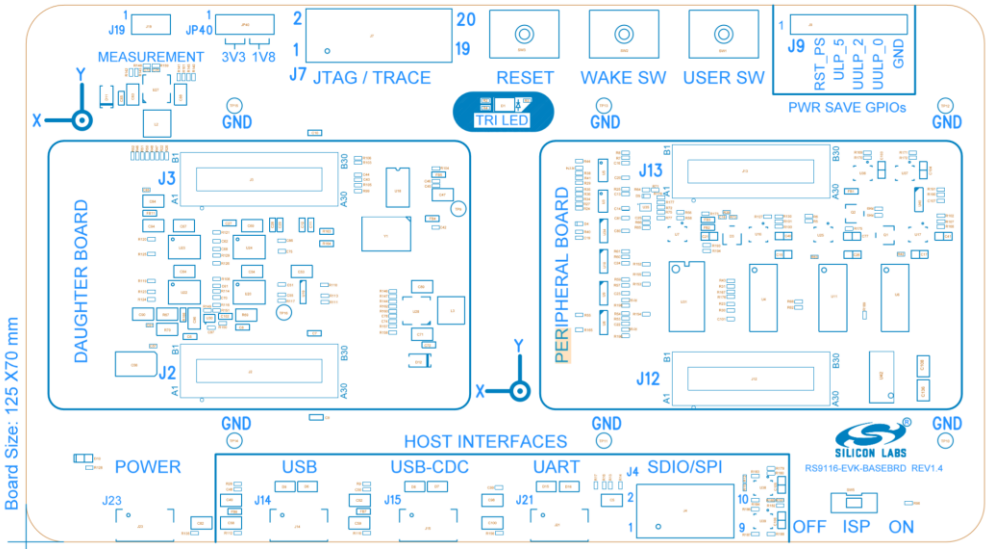


Figure 6: Base Board Assembly Drawings

6.2 QMS Daughter Board Assembly Drawings:

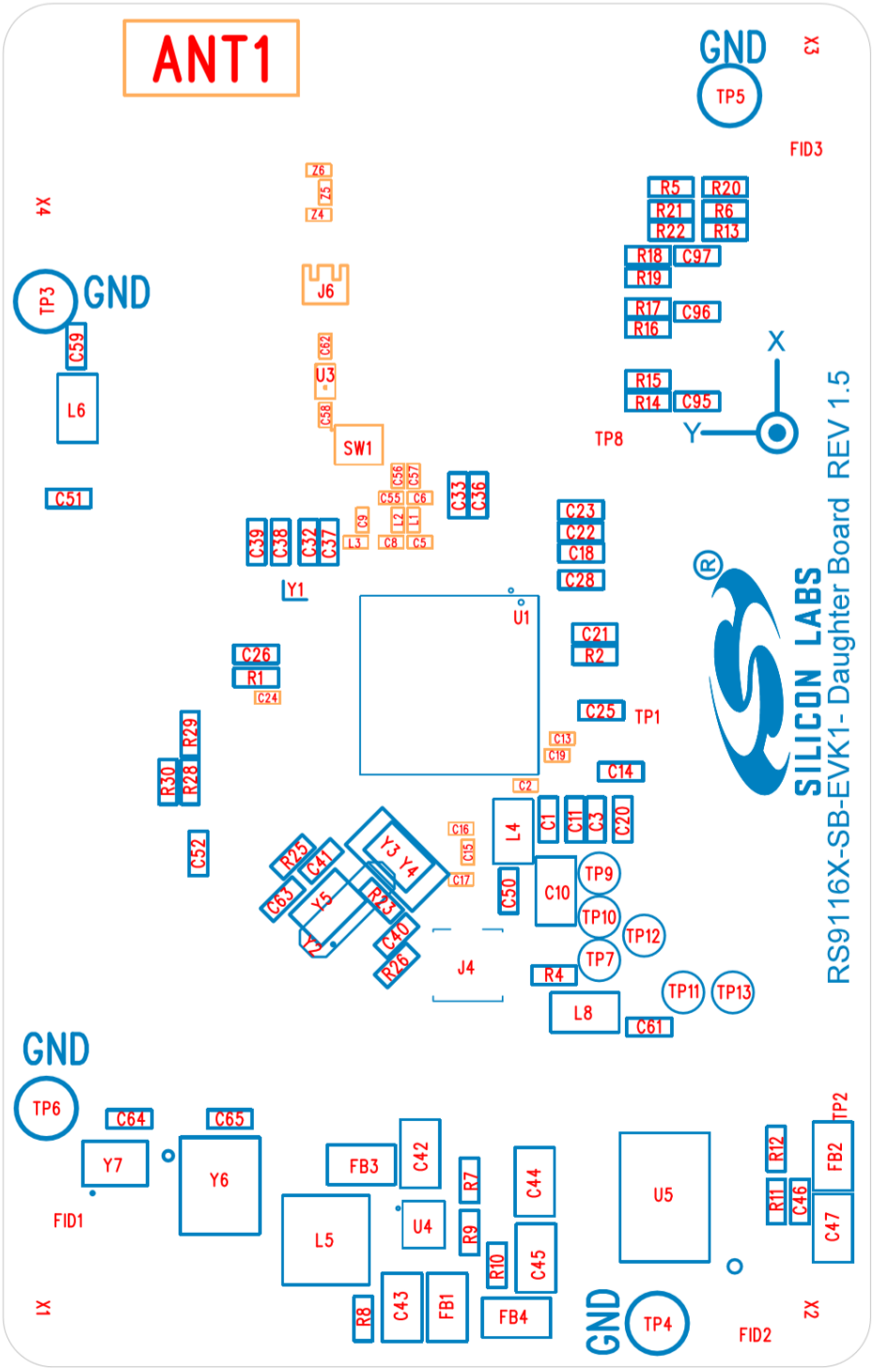


Figure 7: Daughter Board Assembly Drawing

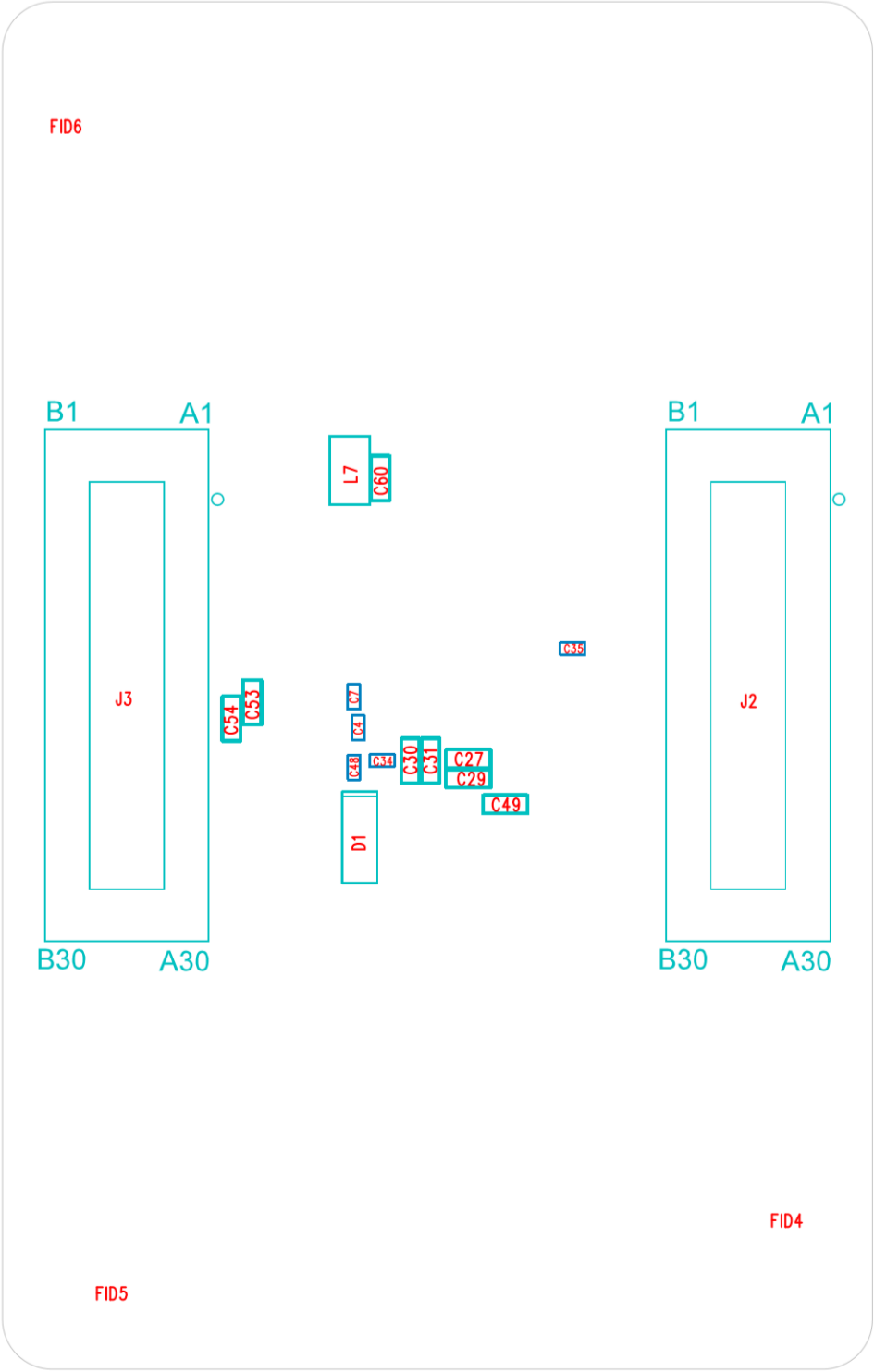


Figure 8: Daughter Board Assembly Drawing

6.3 CC1 Daughter Board Assembly Drawings:

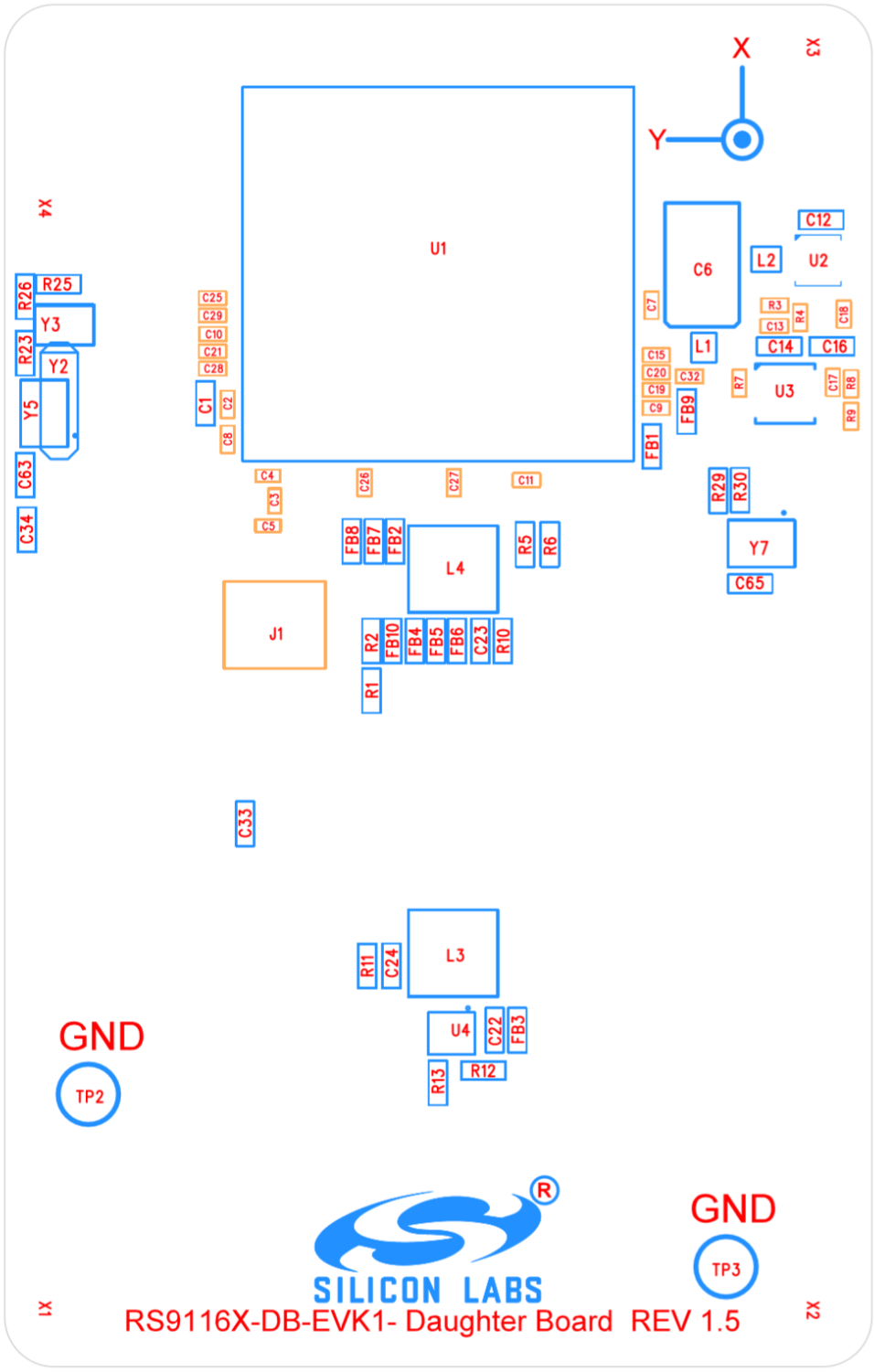


Figure 9: Daughter Board Assembly Drawing

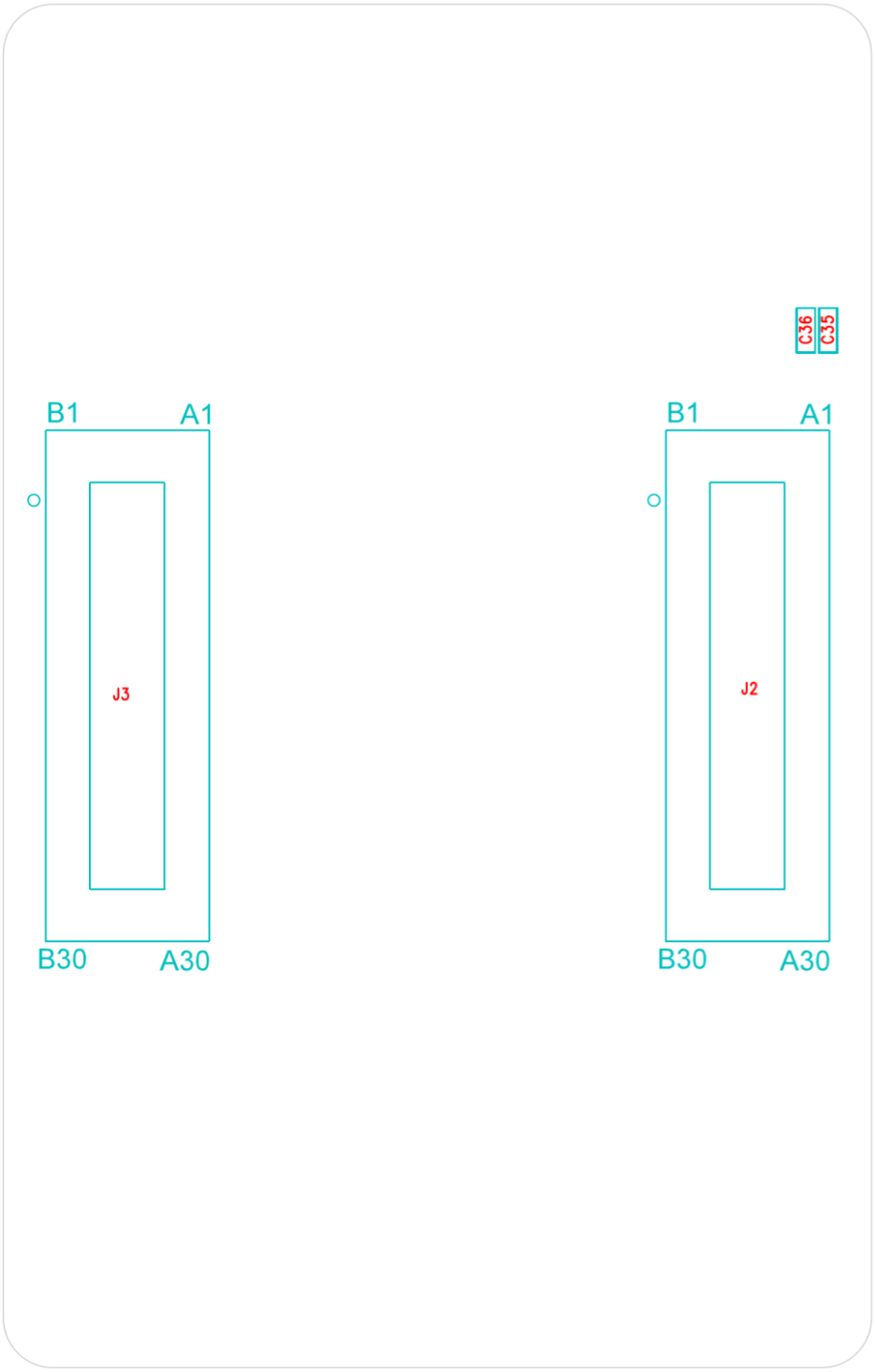


Figure 10: Daughter Board Assembly Drawing

6.4 B00 Daughter Board Assembly Drawings:

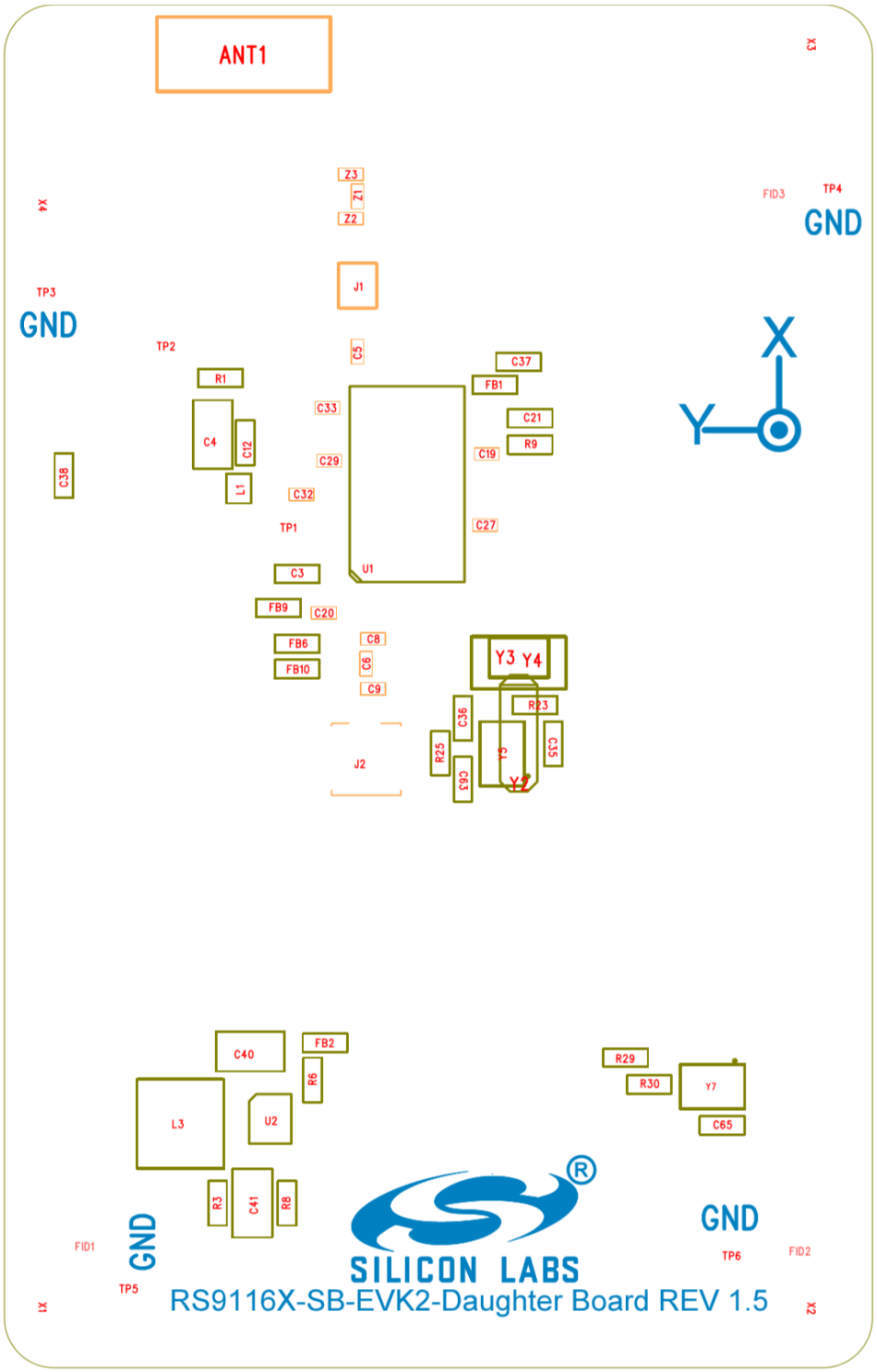


Figure 11: Daughter Board Assembly Drawing

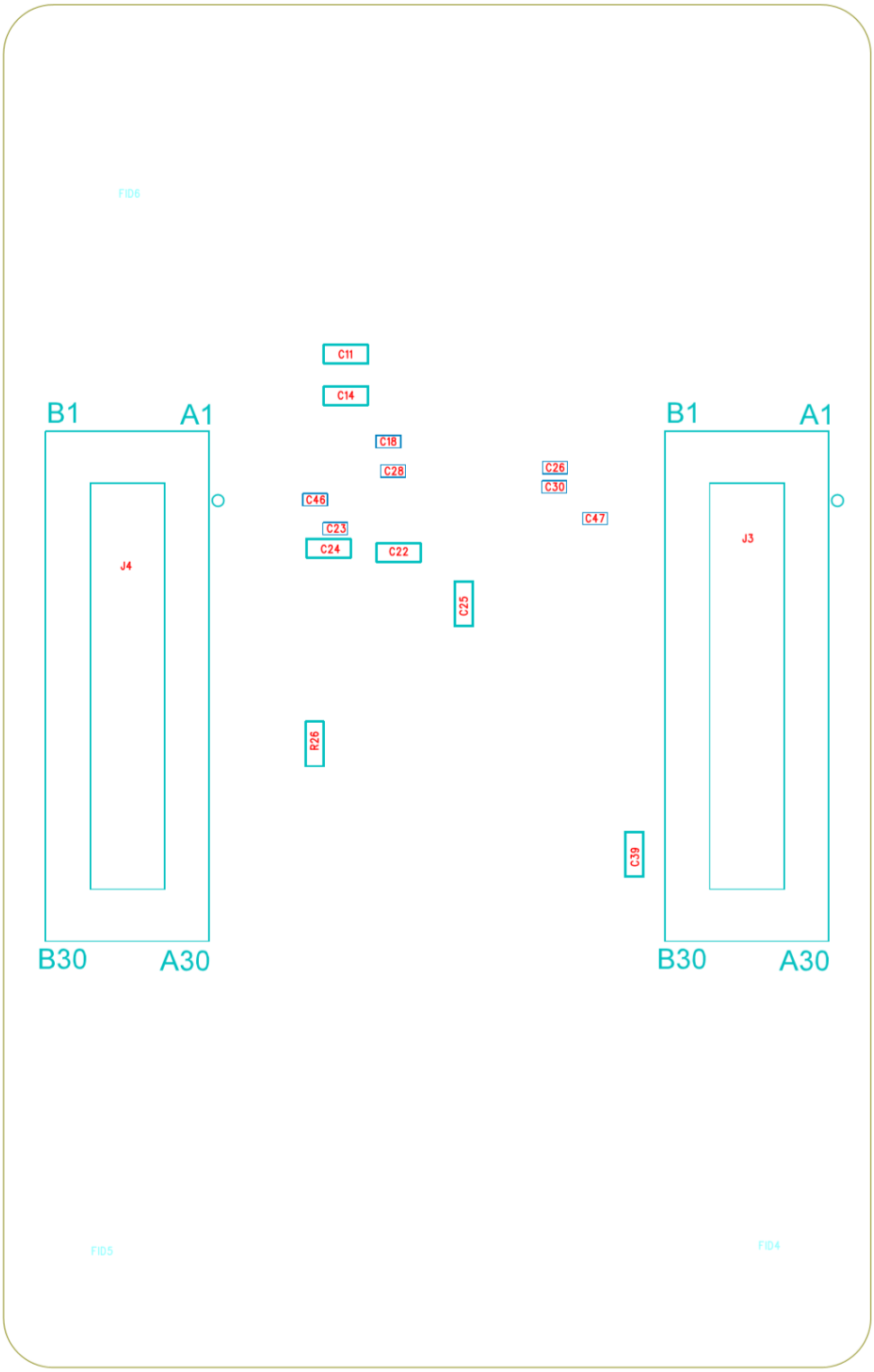


Figure 12: Daughter Board Assembly Drawing

7 Revision Report

Revision Number	Version Number	Date	Changes
1	1.0	May 2018	Include changes
2	1.1	Jun 2018	Include changes
3	1.2	Oct 2018	1. Corrected OpenKM path 2. Corrected Radius server path 3. DevCPP example update 4. Added details to run UART examples with TeraTerm Script
4	1.3	Jan 2019	1. Corrected figure 21. 2. Added the ABRD requirement for UART.
5	1.4	Mar 2019	1. Deleted the Zigbee section 2. SDIO related updates.
6	1.5	Jun 2019	Corrected wifiuser.pem path
7	1.6	May 2020	1. Folder paths updated as per new release package 2. Updated spell mistakes
8	1.7	Oct 2020	1. Added Note in the Hardware details section for Assembly drawings info for EVB 2. Added Appendix E_EVB Assembly Drawings page for the same. 3. Corrected some block diagrams. 4. Dev C++ related information removed. 5. Added FW TTL Scripts steps for execution. 6. Default ABRD is provided in the ttl scripts as default. 7. Updated the Website URL's with latest .
9	1.8	Jan 2021	1. Updated "ext_custom_feature_bit_map" in at+rsi_opermode command to 384k Memory configuration in Section 4.5, 4.6, and 4.7. 2. Updated "Config_bit_map" in at+rsibt_addattribute command to Zero(0) in Section 4.5.1.1.1 and 4.5.1.2.1. 3. Added a note and a link to Getting Started documents for quick evaluation. **Note:** This document should be used with WiSeConnect version 2.3.0.
10	1.9	Jun 2021	1. Added EFX32-CON-BRD details 2. Removed section Evaluation of WiSeConnect 3. Removed Appendix - Running Tera Term Scripts

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