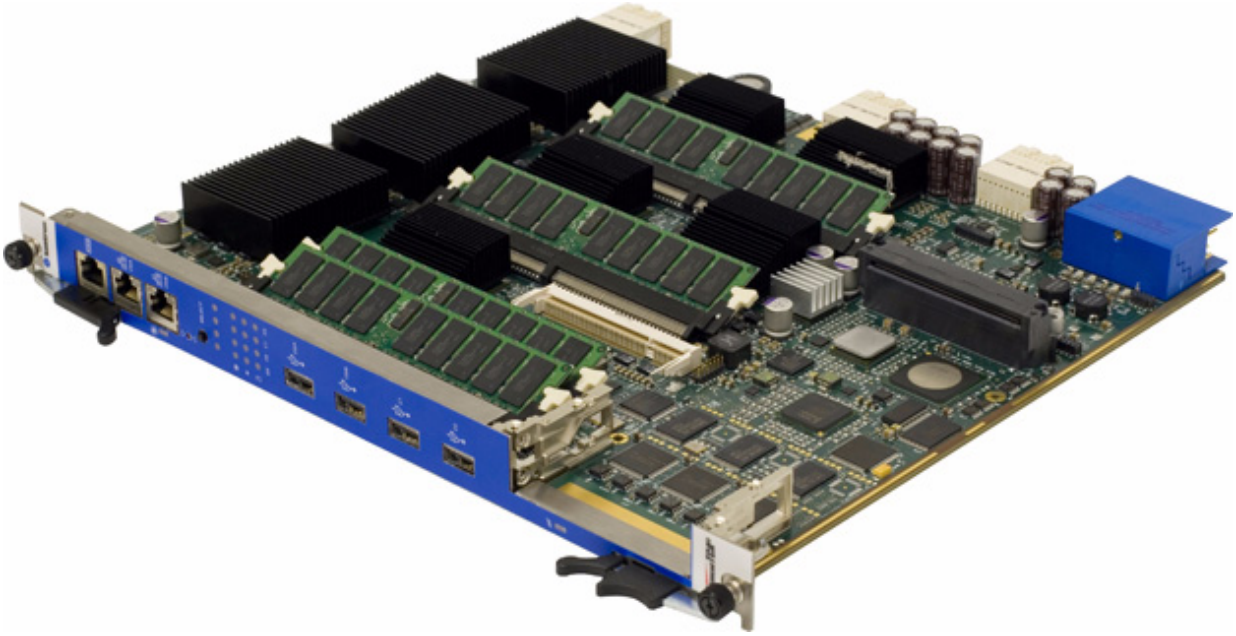
AT8030 User's Guide

AdvancedTCA®



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kontron

Revision History

Rev. Index	Brief Description of Changes	Date of Issue
1.0	first release	December 2007
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Safety Instructions

Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisories" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.
- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support

WARNING

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedure, which can include wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.
- When you want to remove the protective foil (if present), make sure you are properly grounded and that you touch a metalic part of the board.

CAUTION

Removing the protective foil from the top and bottom cover might create static.
When you remove those protections, make sure you follow the proper ESD procedure.

Preface

How to Use This Guide

This user's guide is designed to be used as step-by-step instructions for installation, and as a reference for operation, troubleshooting, and upgrades.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following is a summary of chapter contents:

- Chapter 1, Product Description
- Chapter 2, Board Features
- Chapter 3, Installing the board
- Chapter 4, Hardware Management
- Chapter 5, Software Setup
- Appendix A, Memory & I/O Maps
- Appendix B, Extension Registers
- Appendix C, Connector Pinout
- Appendix D, BIOS Setup Error Codes
- Appendix E, Software Update
- Appendix F, Supported RFC and MIB
- Appendix G, Bootloader
- Appendix H, Getting Help

Customer Comments

If you have any difficulties using this user's guide, discover an error, or just want to provide some feedback, please send a message to: Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide on our Web site. Thank you.

Advisory Conventions

Seven types of advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are Note, Signal Paths, Jumpers Settings, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.

Note:
Indicate information that is important for you to know.

Signal Path:
Indicate the places where you can fin the signal on the board.

Jumper Settings:
Indicate the jumpers that are related to this sections.

BIOS Settings:
Indicate where you can set this option in the BIOS.

Software Usage:
Indicates how you can access this feature through software.

CAUTION
Indicate potential damage to hardware and tells you how to avoid the problem.

WARNING
Indicates potential for bodily harm and tells you how to avoid the problem.

ESD Sensitive Device:
This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.
Please read also the section "Special Handling and Unpacking Instructions".

CE Conformity:
This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section "Regulatory Compliance Statements" in this manual.

Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible future shipment.

Powering Up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting without any other I/O peripherals attached, including AMC adapters.

Make sure your system provides the minimum DC voltages required at the board's slot, especially if DC power is carried by cables.

If you are still not able to get your board running, contact our Technical Support for assistance.

Adapter Cables

Because adapter cables come from various manufacturers, pinouts can differ. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

Storing Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Regulatory Compliance Statements

FCC Compliance Statement for Class A Devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING

This is a Class A product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.

Safety Certification

All Kontron equipment meets or exceeds safety requirements based on the IEC/EN/UL/CSA 60950-1 family of standards entitled, "Safety of information technology equipment." All components are chosen to reduce fire hazards and provide insulation and protection where necessary. Testing and reports when required are performed under the international IECEE CB Scheme. Please consult the "Kontron Safety Conformity Policy Guide" for more information. For Canada and USA input voltage must not exceed -60Vdc for safety compliance.

CE Certification

The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

Limited Warranty

Kontron grants the original purchaser of Kontron's products a TWO YEAR LIMITED HARDWARE WARRANTY as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long- term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

Kontron will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refunding. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of Kontron liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

Kontron issues no warranty or representation, either explicit or implicit, with respect to its products reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will Kontron be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if Kontron were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no Kontron employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's consent.

Chapter 1

Product Description

1. Product Description

1.1 Product Overview

An ideal processor node for IP Multimedia System (IMS) clustering applications, the AT8030 AdvancedTCA processor board is designed with three Intel® Core 2 Duo ® processors each with dedicated memory, plus 10 GbEthernet (GbE) links on the fabric interface and one AdvancedMC slot. The AT8030 provides equipment manufacturers the flexibility to customize the design of their network system solutions, especially for various 10 GbE-based systems that drive IMS-based broadband applications that require the seamless delivery of video and data content in IPTV or VoD networks.

1.2 What's Included

This board is shipped with the following items:

- One AT8030 board
- One RJ45-DB9 serial adaptor (1015-9404)
- One AMC gap filler
- Cables that have been ordered

If any item is missing or damaged, contact the supplier.

1.3 Board Specifications (Unit Computer Section)

Table 1-1:Board Specifications (Unit Computer Section)

Features	Description
Processors	• One PowerQUICC III, MPC8547 1GHz • Passive heatsink
Bus Interfaces	• Memory bus at 400 MHz, 72 bits wide • PCI 32bits/66MHz
Expansion Slot	• None
System Memory	• Up to 512 MB on 1x200-pin latching DDR-2 400MHz SDRAM (SO-CDIMM) • ECC support, support SEC/DED • 1 DDR-2 channel
Flash Memory	• 256MB NOR Flash
Connectors	• 1 selectable Serial Port (RJ-45)
IPMI Features	• Management Controller compliant to PICMG 3.0 R2.2, AMC.0 R2.0 and IPMI v1.5 rev 1.1. • Management Controller is run time field reprogrammable without payload impact. • Robust fail safe bootblock implementation • Remote upgrade capability from all IPMI interfaces (Host Interface/IPMB-0/LAN) compliant to HPM.1 • Fast interrupt driven SMS host interface compliant to IPMI-KCS v1.5 rev 1.1 • Standard Management Controller message bridging to AMC via IPMB-L • Management Controller support standard PCI Hot Plug for PCI-Express AMC. • IPMI Watchdog supporting FRB2, POST, OS Load and SMS/OS watchdog with interrupt on pretimeout • SEL (System Event Log) support with storage for up to 1023 events • FRU Inventory Area support • SENSOR device support • AMC.0 R2.0 Clock Ekeying support • PICMG 3.0 Bused Resource Control support
Supervisory	• Supports a system management interface via an IPMI V1.5 compliant controller • Watchdog for Boot Loader execution and OS loading (through IPMI and FPGA watchdogs) • Hardware system monitor (voltages, temperature), CPU temperature monitor / alarm; board temperature sensor, power failure through IPMC

1.4 Board Specifications (CPU0 Section)

Table 1-2:Board Specifications (CPU0 Section)

Features	Description
Processors	• One 1.5 GHz Intel LV L7400 dual core processor • Passive heatsink
Cache Memory	• 32KB L1 instruction and 32KB L1 data cache dedicated for each core. • 4MB L2 cache on each processor chip shared by both cores.
Chipset	• Embedded Northbridge(MCH) and Southbridge(ICH) Intel 3100
Bus Interfaces	• CPUs Front Side bus at 667 MHz, 64-bit data, 36-bit address • Single channel DDR2 Registered ECC at 400 MHz • One x8 configurable PCI-express port (2x4 mode) • Four x1 configurable PCI express port (4x1 mode)
Expansion Slot	• 1 Mid-size AdvancedMC bay • AMC.1 Type4 - x4 PCIExpress • AMC.2 - Common Options Type E2 - Dual GbEthernet - Fat pipes options Type 4 - Quad GbEthernet • AMC.3 Dual port SAS
System Memory	• Up to 8 GB on 2x240-pin latching DDR-2 400MHz SDRAM (PC2-3200) • ECC support, support SEC/DED • 512Mbit, 1Gbit or 2Gbit Technology
BIOS Storage	• Two redundant 1MB BIOS (Field software upgradeable) • Roll back functionality controlled by the management controller
Storage	• 2 ports SAS available through AdvancedMC modules or through Rear I/O • 2 GB USB FLASH drive

Features	Description
Connectors	• 1 selectable Serial Port (RJ-45) • 2 USB 2.0 • 2 GbE ports (RJ-45)
BIOS Features	• AMI BIOS • Save CMOS in NVRAM • Boot from all Ethernet interfaces • Boot from SAS • Boot from USB 2.0 (Floppy, CD-ROM, Hard Disk, Flash) • Auto configuration and extended setup • Diskless, Keyboard less, and battery less operation extensions • System and LAN BIOS shadowing • Advanced Configuration and Power Interface (ACPI 1.0 & 2.0) • Console redirection to serial port (VT100)with CMOS setup access • Field updateable BIOS • Event (SERR, PERR, correctable/uncorrectable ECC, POST errors, PCI-Express) log support to the management controller
IPMI Features	• Management Controller compliant to AMC.0 R2.0 and IPMI v1.5 rev 1.1. • Management Controller is run time field reprogrammable without payload impact. • Robust fail safe bootblock implementation • Remote upgrade capability from all IPMI interfaces (Host Interface/IPMB-0/LAN) compliant to HPM.1 • Fast interrupt driven SMS host interface compliant to IPMI-KCS v1.5 rev 1.1 • Gracefull shutdown support via ACPI • IPMI Watchdog supporting FRB2, POST, OS Load and SMS/OS watchdog with interrupt on pretimeout • IPMI v2.0 IOL and Serial Over Lan support on base interface • FRU Inventory Area support • SENSOR device support
Supervisory	• Supports a system management interface via an IPMI V1.5 compliant controller • Watchdog for BIOS execution and OS loading (through IPMI) • Hardware system monitor (voltages, temperature), CPU temperature monitor / alarm; board temperature sensor, power failure through the management controller

1.5 Board Specifications (CPU1 & 2 Section)

Table 1-3:Board Specifications (CPU1 & 2 Section)

Features	Description
Processors	• One 1.5 GHz Intel LV L7400 dual core processor • Passive heatsink(s)
Cache Memory	• 32KB L1 instruction and 32KB L1 data cache dedicated for each core. • 4MB L2 cache on each processor chip shared by both cores.
Chipset	• Embedded Northbridge(MCH) and Southbridge(ICH) Intel 3100
Bus Interface	• CPUs Front Side bus at 667 MHz, 64-bit data, 36-bit address • Single channel DDR2 Registered ECC at 400 MHz • One configurable PCI-express port (1x4 mode)
Expansion Slot	• None
System Memory	• Up to 4 GB on 1x240-pin latching DDR-2 400MHz SDRAM (PC2-3200) • ECC support, support SEC/DED • 512Mbit, 1Gbit or 2Gbit Technology only
BIOS Storage	• Two redundant 1MB BIOS (Field software upgradeable) • Roll back functionality controlled by the management controller
Connectors	• 1 selectable Serial Port (RJ-45) • 1 USB 2.0
BIOS Features	• AMI BIOS • Save CMOS in NVRAM • Boot from all Ethernet interfaces • Boot from USB 2.0 (Floppy, CD-ROM, Hard Disk, Flash) • Auto configuration and extended setup • Diskless, Keyboard less, and battery less operation extensions • System and LAN BIOS shadowing • Advanced Configuration and Power Interface (ACPI 1.0 & 2.0) • Console redirection to serial port (VT100)with CMOS setup access • Field updateable BIOS • Event (SERR, PERR, correctable/uncorrectable ECC, POST errors, PCI-Express) log support to the management controller
Storage	• 2 GB USB FLASH drive
IPMI Features	• Management Controller compliant to AMC.0 R2.0 and IPMI v1.5 rev 1.1. • Management Controller is run time field reprogrammable without payload impact. • Robust fail safe bootblock implementation • Remote upgrade capability from all IPMI interfaces (Host Interface/IPMB-0/LAN) compliant to HPM.1 • Fast interrupt driven SMS host interface compliant to IPMI-KCS v1.5 rev 1.1 • Gracefull shutdown support via ACPI • IPMI Watchdog supporting FRB2, POST, OS Load and SMS/OS watchdog with interrupt on pretimeout • IPMI v2.0 IOL and Serial Over Lan support on base interface • FRU Inventory Area support • SENSOR device support
Supervisory	• Supports a system management interface via an IPMI V1.5 compliant controller • Watchdog for BIOS execution and OS loading (through IPMI) • Hardware system monitor (voltages, temperature), CPU temperature monitor / alarm; board temperature sensor, power failure through the management controller

1.6 Board Specifications (all)

Table 1-4:Board Specifications (all)

Features	Description
Board Specifications	• PICMG 3.0 (Advanced TCA core specification) • PICMG 3.1 (Ethernet/Fiber Channel over Advanced TCA) • PICMG AMC.0 (Advanced mezzaninne card base specification) • PICMG AMC.1 (Advance mezzaninne card PCI-Express) • PICMG AMC.2 (Advance mezzaninne card Ethernet) • PICMG AMC.3 (Advance mezzaninne card Storage)
OS Compatibility (CPU Engine 0, 1 & 2)	• Red Hat Enterprise Linux 5 • Wind River PNE Linux 1.5
Power Requirements	• -38Vdc to -72 Vdc (for Canada and USA input voltage must not exceed -60Vdc for safety compliance) • 200W maximum including 25W budget for an AMC module. Additional 25W maximum for RTM.
Environmental Temperature	Operating: 0-55°C/32-131°F with 30 CFM airflow Storage and Transit: -40 to +70°C/-40 to 158°F
Environmental Humidity	Operating: 5% to 93% @40°C/104°F non-condensing Storage and Transit: 5% to 95% @ 40°C/104°F non-condensing
Environmental Altitude*	Operating: 4,000 m / 13,123 ft Storage and Transit: 15,000 m / 49,212 ft
Environmental Shock	Operating: 3G each axis Storage and Transit: 18G each axis
Environmental Vibration	Operating: 5-200Hz. 0.2G, each axis Storage and Transit: 5 Hz to 20 Hz @ 1 m2/s3 (0.01 g2 /Hz) (flat) 20 Hz to 200 Hz @ -3 dB/ oct (slop down)
Reliability	• MTBF: > 105 000 hours @ 40 C / 104 F (Telcordia SR-332, Issue 1) • AMC supply protected by active breaker • USB voltage protected by active breakers
Safety / EMC*	• Safety: CB report to IEC60950-1, CE Mark to EN 60950-1:2001. Meets or exceeds UL 60950-1/CSA C22.2 No 60950-1-07. • Designed to meet GR-1089-CORE • EMI/EMC: FCC 47 CFR Part 15, Class A; CE Mark to EN55022/EN55024/EN300386

* Designed to meet or exceed

1.7 Compliance

This product conforms to the following specifications:

- PICMG3.0R2.0 ECN001 & ECN 002 (Advanced TCA core specification)
- PICMG3.1R1.0 (Ethernet/Fiber Channel over Advanced TCA)
- AMC.0 R2.0 (Advanced mezzaninne card base specification)
- AMC.1 R1.0 (Advance mezzaninne card PCI-Express)
- AMC.2 R1.0 (Advance mezzaninne card Ethernet)
- AMC.3 R1.0 (Advance mezzaninne cardStorage)
- ACPI rev 2.0

1.8 Hot-Plug Capability

The AT8030 supports Full Hot Plug capability as per PICMG3.0R2.0 ECN001 & ECN 002. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG3.0R2.0 specification for additional details.

The AT8030 supports PCI-Express Hotplug on AMC B1. The IPMC uses the standard PCI Express Hotplug Controller on the CPU0 Engine allowing hot insertion and removal of an AMC.1 module.

1.9 Interfacing with the Environment

1.9.1 RTM (rear transition module)

The RTM8030 is a single slot (6HP) AdvancedTCA Rear Transition Module. This module provides additional connectivity for AT8030 CPU front blade.

1.9.1.1 Standard Compliance

- PICMG3.0 R2.0 ECN001 & ECN002 - Advanced Telecommunication Computing Architecture
- SAS1R10 - Serial Attached SCSI - 1.1 Revision 10. (SAS-1.1)
- SFF-8470 (T10 Technical Committee and SCSI Trade Association)

1.9.1.2 SAS Feature

One 3Gbit/s SAS port available either:

- On the faceplate through a SFF-8470 connector for cabling (signal integrity garanted over 6 meters).
- Through an onboard SFF-8482 hard drive receptacle.

1.9.1.3 Serial Port Feature

- Two serial ports available on the RTM face plate through two RJ-45 connectors.
- RS-232 signal levels at RTM face plate connector.
- Serial port speed capability is: 9.6kbits/s to 115.2kbits/s.

1.9.1.4 Hot Swap

The RTM8030 supports hot swapping by using the switch connected to the face plate lower ejector. This switch indicates the coming hot swap action. The insertion of the RTM to a slot is always done over a non powered connector. During the extraction procedure, the management power is disabled only when the RTM8030 is removed. This procedure meets the AdvancedTCA AMC behavior.

1.9.1.4.1 Inserting the RTM8030 into the slot

The presence of the RTM is indicated by one signal. The front blade IPMC recognizes the RTM insertion when the signal is low. After recognizing the RTM, the IPMC turns the blue LED ON and enables the management power to the RTM. Once the IPMB-L link is working, the IPMC accesses the MMC to retrieve FRU data. After knowing the type of RTM inserted, the IPMC negotiates with the shelf manager in order to activate the +12V payload power. After RTM local voltages have been ramped up, the RTM's MMC enables the RTM Link.

After this the front board IPMC informs the shelf manager there is a functional RTM blade present.

1.9.1.4.2 Removing the RTM8030 from the slot

The RTM_EJECT signal goes HIGH by opening the RTM lower ejector handle. This indicates to the front blade IPMC that a hot swap action is going to take place. The IPMC then negotiates the removal with the System manager and if it is granted, it proceeds with the removal process.

The IPMC proceeds to the deactivation by disabling ekey governed links, the IPMC then disables the RTM Link and turns OFF the payload +12V power. When it is safe to remove the RTM blade from the slot, the IPMC turns the Blue / Hot Swap LED ON. Front Blade IPMC turns OFF the management power only when there is no RTM detected. (RTM8030 removed from the slot)

1.9.2 Mezzanine

The AT8030 has one AMC bay. Using a mezzanine allows to add storage or I/O not provided on board.

1.9.2.1 AMC Expansion

The AMC slot provides an AMC.1 type 4, AMC.2 Type E2 and 4, AMC.3 Dual Port SAS. This means that the following signaling are supported:

- PCI-Express X4 on AMC ports 4-7
- PCI-Express clock on FCLKA
- Gigabit Ethernet on AMC port 0 and 1, 8-11
- Telco clocks on TCLKA, B, C, D
- SAS on AMC port 2 and 3

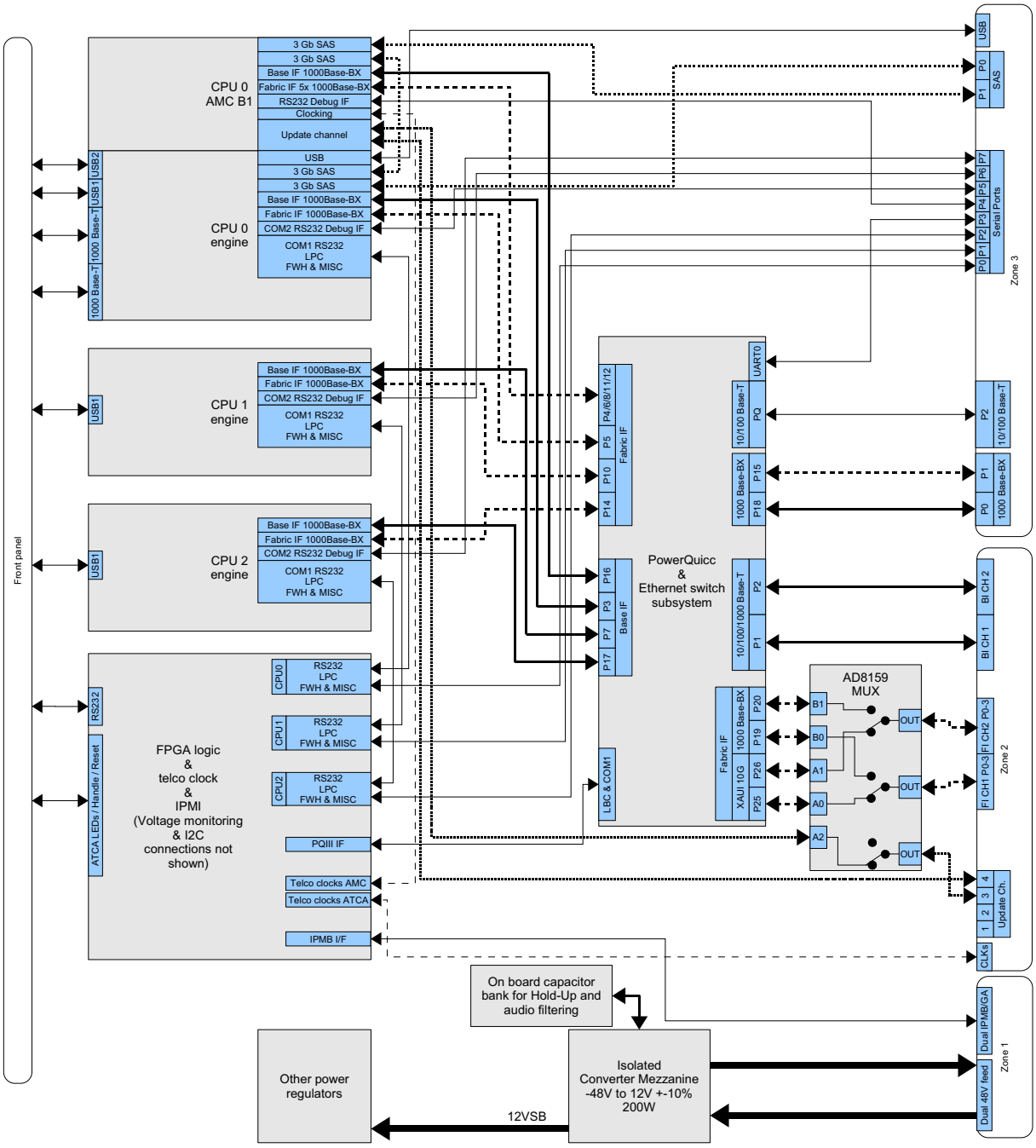
Chapter 2

Board Features

2. Board Features

2.1 Block Diagram

Figure 2-1:Block Diagram



2.2 Unit Computer

The Unit Computer manages the Ethernet switch of the AT8030. It is a Freescale MPC8547 which integrates a PowerPC processor core with system logic required for networking, telecommunications, and wireless infrastructure applications. The MPC8547operates with a core frequency of 1000MHz and 400MHz Core Complex Bus (CCB) frequency respective DDR2 SDRAM data rate.

512MB external onboard DDR2-400MHz SDRAM with ECC support are available to the Unit Computer. Memory used is standard SO-CDIMM module using a DDR-II SODIMM socket.

The boot code is fetched from two external NOR FLASH memory chips. Two 1024Mb NOR FLASH memory chips are assembled resulting in a total of 256 Mbytes of Flash Memory. The FLASH memory is connected to the LBC bus of the MPC8547 in 32bit port size.

The Unit Computer manages the Ethernet Switch via the 32bit, 66MHz PCI local bus and acts as the PCI host processor with internal PCI arbiter. The PCI interface operates synchronously to the system clock.

The Unit Computer is connected to the FPGA via the LBC bus in 8bit port size. The LBC controller operates at a frequency of 50 MHz or 66 MHz, depending on the MPC8547 speed.

The Unit computer has 3 Ethernet connections.

- One 1000Base-BX to the Base Interface
- One 1000Base-BX to the Fabric Interface
- One 10/100Base-TX to the RTM

2.3 CPU Engines (Virtual prAMCs)

2.3.1 CPU0 Engine

2.3.1.1 Serial Attached SCSI(SAS)

The CPU engine 0 includes a SAS controller (LSISAS1064E). This controller embeds four 3 Gb/s SAS link, but only two are used. One port goes to the AMC storage port 2 and the other port is routed to the Zone 3 RTM connector. The AMC storage port 3 is a direct connection to the Zone 3 RTM connector. The controller is connected to a x1 PCI-Express port on the Intel 3100 IMCH.

Here's a list of the main features of the controller:

SAS and SSP Features:

- Each PHY supports 3.0 Gbit/s and 1.5 Gbit/s SAS data transfers.
- Support SSP to enable communication with other SAS device.
- Support SMP to communicate topology management information.
- Provide a serial, point-to-point, enterprise-level storage interface.
- Transfer data using SCSI information units.

SATA and STP features:

- Supports SATA data transfers of 3.0 Gb/s and 1.5 Gb/s.
- Support STP data transfers of 3.0Gb/s and 1.5 Gb/s.
- Provide a serial, point-to-point storage interface.

2.3.2 Common Features to CPU0, CPU1 & CPU2 Engines

2.3.2.1 Processors

Intel® Core™2 Duo L7400 processors are members of Intel's growing product line of multi-core processors based on Intel® Core™ microarchitecture, delivering breakthrough energy-efficient performance for embedded platforms. This processor provides an excellent performance per watt choice. It integrates two complete execution cores in one physical package, providing advancements in simultaneous computing for multi-threaded applications and multi-tasking environments. While incorporating advanced processor technology, this processor remains softwarecompatible with previous IA-32 processors.

2.3.2.1.1 Processors Highlights

• Intel® Wide Dynamic Execution: Executes four instructions per clock cycle to improve execution speed and efficiency. Each core can complete up to four full instructions simultaneously using an efficient 14-stage pipeline.

• Intel® Advanced Smart Cache: Improves system performance by significantly reducing memory latency to frequently used data through dynamic allocation of shared L2 cache to each of the processor cores.

• Intel® Smart Memory Access: Optimizes use of available data bandwidth from the memory subsystem to accelerate out-of-order execution. A newly designed prediction mechanism reduces the time in-flight instructions have to wait for data. New pre-fetch algorithms move data from system memory into fast L2 cache in advance of execution. These functions keep the pipeline full, improving instruction throughput and performance.

• Intel® Advanced Digital Media Boost: Accelerates execution of SSE/2/3 instructions to significantly improve multimedia performance. 128-bit SSE instructions are issued at a throughput rate of one per-clock cycle, effectively doubling the speed of execution on a per-clock basis over previous-generation processors.

• Intel® Intelligent Power Capability: Manages runtime power consumption of execution cores by turning on computing functions only when needed. Reduces overall power consumption, enabling quieter, more power-efficient system designs.

• Intel® Virtualization Technology: Allows one hardware platform to function as multiple "virtual" platforms, improving manageability, limiting downtime and maintaining worker productivity by isolating computing activities into separate partitions. It also provides greater isolation and security between different applications and operating systems for added protection against corruption.

• Intel® 64 Architecture: Supports 64-bit instructions, providing flexibility for 64-bit and 32-bit applications and operating systems. Access to larger physical memory space reduces load on the system and allows faster access to data from RAM instead of drive.

• Digital Thermal Sensor (DTS): Measures maximum temperature on the die at any given time.

2.3.2.2 Intel 3100 Chipset

The Intel® 3100 chipset combines server-class memory and I/O controller functions into a single component, creating the first integrated Intel® chipset specifically optimized for embedded, communications, and storage applications. This single-chip system controller replaces a separate memory controller hub and I/O controller hub, significantly conserving board real estate and power consumption.

2.3.2.2.1 Product Highlights

2.3.2.2.1.1Memory

Intel 3100 chipset-based platforms are ECC-enabled and support single-channel DDR2-400 memory (up to 8/ 4 GB), which is ideal for storage and memory-intensive applications. The memory subsystem interface supports up to four ranks for a total system bandwidth of 3.2 GB/s.

2.3.2.2.1.2PCI Express

For demanding I/O and networking applications, PCI Express interfaces attach a variety of Intel and third-party I/O solution components and adapters directly to the Intel 3100 chipset (one x8 PCI Express interface and one x4 PCI Express interface). Each interface may be bifurcated to provide additional configuration flexibility. The interfaces provide throughput speeds of up to 4 GB/s on the x8 interface, and up to 2 GB/s on the x4 interface, allowing I/O to keep pace with the rest of the platform.

2.3.2.2.1.3Data Protection

The Intel 3100 chipset is designed to bring enterprise-level reliability, availability, serviceability, usability and manageability (RASUM) to the embedded platform. The chipset supports two bits of parity on 64 bits of data on internal buses. The PCI Express interface supports 32-bit cyclic redundancy check (CRC) for detection and automatic recovery of transient signaling errors. Memory interface supports Single Error Correct/ Double Error Detect (SEC/DED) ECC, auto retry on uncorrectable errors, and integrates a hardware memory scrubber to scan the populated memory space, proactively seeking out soft errors in the memory subsystem.

2.3.2.2.1.4Enhanced Direct Memory Access (EDMA)

A four-channel EDMA controller efficiently moves data within local system memory or from the local system memory to the I/O subsystem. Each EDMA channel provides low-latency, highthroughput data transfer capability with no CPU intervention for higher overall system performance. These transfers may be individually designated to be coherent (snooped on the FSB) or non-coherent (not snooped on the FSB), providing improvements in system performance and utilization when cache coherence is managed by software rather than hardware. EDMA also enables quality of service by prioritization of data.

2.3.2.3 *USB 2.0 Interfaces*

Each CPU engine embeds a USB storage controller. This controller is compliant to USB 2.0. CPU engine 0 provides two USB ports on the face plate and one on the RTM. CPU engine 1 & 2 provide one USB port on the front-plate. Those ports can be used for external storage and for booting.

USB features include:

- Capability to daisy chain as many as 127 devices per interface
- Fast bi-directional
- Isochronous/asynchronous interface
- 480 Mbs transfer rate
- Standardization of peripheral interfaces into a single format
- Retro compatible with USB 1.1 devices

USB supports Plug and Play and hot-swapping operations (OS level). These features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

Table 2-1:USB Connector Pinout

Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

Signal Path:
- 2 USB 2.0 on front panel for CPU engine 0 (J10 & J16)
- 1 USB 2.0 on front panel for CPU engine 1 (J17)
- 1 USB 2.0 on front panel for CPU engine 2 (J15)

BIOS Settings:
Advanced --> USB Configuration

2.3.2.4 *Onboard Storage*

Each CPU engine includes a USB mass storage controller (ST72681) attached to 16 Gb of NAND Flash memory. The BIOS supports this as a boot device. This device is available for any OS that supports the standard USB mass storage interface.

Note:
These Flash memories should be used in read only to preserve their memory life.

2.3.2.5 Real Time Clock & NVRAM

The AT8030 is a battery less board. The real time clock and non-volatile RAM integrated in the 3100MCH are powered by the suspend power when available. A double layer SuperCap powers CPU0s RTC and NVRAM when the suspend power is absent. The SuperCap will keep the real time clock running for a typical duration of 2 hours after 10 years. The real time clock precision is 27ppm or better.

Although it is possible to save the CMOS setup in NVRAM (or CMOS RAM), the default configuration saves the setup in flash. So, when the AT8030 are unpowered for too long, only the time and date will be lost.

2.3.2.6 Redundant BIOS Flash

Two BIOS flash (firmware hub or FWH) per CPU engine are present on the AT8030. If a BIOS update corrupts a flash and prevents the CPU from completing the boot sequence, the MMC will force a reboot from the other BIOS flash.

Note:
Since the CMOS setup is saved in flash, this will also restore the previous BIOS setup.

BIOS Settings:
Management --> System Information --> FWH In Use
Exit --> Exit and Execute BIOS Swap

2.4 Ethernet Interfaces

2.4.1 i82571EB Ethernet Controller

The four Ethernet controllers on the AT8030 are Intel's 82571EB. The front panel connections of CPU engine 0 are two copper 10/100/1000Base-T interfaces. The backplane Base and Fabric Interface connections for all three CPU engines are 1000Base-BX interface through the onboard Ethernet switch.

The i82571EB features high performance with TCP/IP and UDP/IP checksum offloading for IPv4 and IPv6, packet filtering, and jumbo frame up to 16K. See www.intel.com for additional details on the i82571.

The AT8030 has boot from LAN capability (PXE) on these ports. Enable the option from the BIOS Setup Program. Please refer to Section 5.1, AMI BIOS Set-up Program.

Signal Path:
The Ethernet Management RJ45 connector is on the faceplate.

BIOS Settings:
Advanced --> Expansion ROM Configuration

Software Usage:
You might need to configure the VLANs on the onboard switch. For proper commands, please refer to the CLI manual.

2.4.2 Onboard Ethernet Switch (Broadcom BCM56502)

The Onboard Ethernet Switch is a Broadcom BCM56502 24-Port GbE Multilayer Switch with two 10-GbE Uplink ports. The board use 20 GbE and two 10GbE ports. The four (4) unused ports are disabled by SW for power saving.

The BCM56502 provides a 32bit/66MHz PCI Management Interface which is connected to the Unit Computer.

Onboard Ethernet Switch RESET is separated from the Unit Computer RESET in order to provide a hitless restart function in case the Unit Computer software crashes.

See www.broadcom.com for additional details on the BCM56502.

2.4.3 Base & Fabric Interface Ethernet

Base & Fabric Interface Ethernet are implemented using a single chip Onboard Ethernet Switch (BCM56502). Fabric Interface (FI) traffic is separated from Base Interface (BI) traffic by switch fabric configuration. All GbE FI interfaces operate in SERDES mode. The Zone 2 FI connection from the switch operate in 10 GbE (XAUI) or 1 GbE based on e-keying.

The GbE BI interfaces operate in SERDES mode except the two ports connected to Zone 2 of the PIGMG® 3.0 backplane. Those ports operate in SGMII mode. An additional Dual-Port 10/100/1000Base-T Gigabit Ethernet Transceiver (BCM5482) is required to connect the switch to Zone 2 of the PIGMG® backplane.

The Base Interface Ethernet has the following connections to/from the Onboard Ethernet Switch.

- Two 10/100/1000Base-T connections to the Base Interface in Zone 2 of the PIGMG® 3.0 backplane
- One 1000Base-BX connection to the RTM through Zone 3
- One 1000Base-BX connection to the Unit Computer
- One 1000Base-BX connection to CPU 0
- One 1000Base-BX connection to CPU 1
- One 1000Base-BX connection to CPU 2
- One 1000Base-BX connection to AMC B1

The Fabric Interface Ethernet has the following connections from the Onboard Ethernet Switch.

- Two 10G XAUI connections to the Fabric Interface in Zone 2 of the PIGMG® 3.0 backplane*
- Two 1000Base-BX connection to the Zone 2*
- One 1000Base-BX connection to the RTM in Zone 3
- One 1000Base-BX connection to the Unit Computer
- One 1000Base-BX connection to CPU 0

- One 1000Base-BX connection to CPU 1
- One 1000Base-BX connection to CPU 2
- Five 1000Base-BX connection to AMC B1 (one to common option port 1, four to fat pipe port 8 to 11)

* Only one of those connections is enabled, at the same time, by e-keying

2.5 Serial Interfaces

The AT8030 uses serial interfaces to manage the CPUs. Since no video interface is provided on board, the only way to get visual information on the CPU engines is the serial console. Serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 9.6Kbps to 115Kbps.

There is a single serial port connector on the front-plate. This connector can be routed to any of the primary serial ports of the CPU engines and the Unit Computer. The user selects the routing with a pushbutton on the front-plate. The selected console will be displayed using a bank of 4 green LEDs.

The primary serial port of each CPU engine and UART0 of the Unit Computer can also be redirected to the RTM.

The secondary port of the CPU engines is routed directly to the RTM and there is a direct connection between the AMC connector and the RTM.

The front-plate serial port selection user interface is composed of four green LEDs and one pushbutton. On a blade insertion, the default selected port is the Ethernet Switch(ES) and the corresponding LED is turned on, the other LEDs remain off. Each time the user presses the button, the selected port changes to the next one in the following sequence: ES then CPU0 then CPU1 then CPU2 then ES... and so on.

Table 2-2:Serial Interface Pinout

Pin	Signal
1	RTS*
2	DTR*
3	TX#
4	GND
5	GND
6	RX#
7	DSR**
8	CTS**

* Driven Active but Not Used

** Not Used

Note:
Standard product uses a RJ-45 8 pins connector. RI (ring indicator) and DCD (data carrier detect) signals are not available.
The pinout is a custom one, not the same as RS-232D TIA/EIA-561.

Signal Path:
COM1 of each X86 CPU can be routed to the RTM or to their companion MMC/IPMC for SOL. They can also be routed to a RJ45 on the front-plate or to the RTM.
COM2 of the X86 CPUs are routed to the RTM.
UART0 of the ES can be routed to a RJ45 on the front-plate or to the RTM.

BIOS Settings:
System Management --> Remote Access Configuration

2.6 AMC Mezzanine

One AMC site is available. Characteristics of the AMC are as follow:

- Type B+
- Support mid-size single width mechanical format
- PCI-Express X4 with reference clock on AMC FCLKA
- Fully compliant PCI-Express hot-swap support
- Port 0 and 1, 8-11 connected to onboard Ethernet Switch
- Provision for telecom clocks on TCLKA, B, C, D
- SAS link to the CPU Engine 0 SAS controller and an other SAS link to the RTM connector.
- Compliant to AMC.0, AMC.1, AMC.2 and AMC.3

As per AMC.1 R2.0, the carrier board is required to provide PCI-E 100MHz reference clock to the AMC on FCLKA. However, modules are not required to use it. Kontron recommends using AMC-Express modules that use the reference clock on FCLKA. If the module makes its own reference clock, then the spread spectrum of CPU Engine 0's PCI-Express clock synthetizer will be disabled by e-keying; otherwise the behavior of the PCI-Express link will be erratic.

Note:
All electromagnetic compatibility testing has been done with spread spectrum. Disabling the spread spectrum can complicate EMC.

The SAS interface on port 2 allow to use SAS AMC storage mezzanine with AT8030, however, it can also accommodates SATA drives. It is correct electrically to hot swap a SATA/SAS AMC but it may cause driver problem in different operating system.

The telco clock signals allow the AT8030 to provide clocks to the AMC on TCLKA and TCLKC. It also allows an AMC to retrieve a clock and to provide it to the system through TCLKB and TCLKD. For possible clock frequency and connection with the backplane, refer to section Telecom Clock Option.

BIOS Settings:
Advanced --> PCI Express Configuration
SAS/SATA --> Expansion ROM

Software Usage:
To access the SAS BIOS press “CTRL-C” when the board boots.
You can also access the SAS controller by using the LSI Util (Linux Tool)

Software Usage:
AMC serial port available on port 15.
AMC serial port E-Keying OEM link type port GUID : 471C5D14-2AE7-42B9-A9B0-0628546B42CC

2.7 FPGA

The FPGA has many functions. One of them is to act as a companion chip to the IPMC. The states of all the critical signals controlled by the IPMC are memorized in the FPGA and are preserved while the IPMC firmware is being updated.

The FPGA is a RAM-based chip that is preloaded from a separate flash memory at power-up. Two such flash memory devices are provided; one that can only be programmed in factory and the other one that can be updated in the field. The factory flash is selected by inserting jumper JP2 pins 3-4. Field updates require to cycle the power of the board. The selected LED will blink if the factory flash is being used.

The appropriate procedure to upgrade the FPGA will be provided with the update code when needed.

2.8 Telecom Clock Option

The telecom clock option is not shown on the main block diagram. The circuit is made of MLVDS buffers, a PLD and a multi-service line card PLL. The PLD is hooked to the main FPGA with a fast serial link and from there, to the IPMC via a proprietary bus.

The PLD receives 19.44MHz clocks from the backplane (CLK2A and CLK2B) and use it as a reference to the DPLL. Anyone of the PLL clock outputs can be used to feed the AMC’s TCLKA using the FPGA interface. Please refer to section B.5. If a backplane clock is lost, the circuit will automatically switch to the redundant clock. If all backplane clocks are lost, the PLL will switch to holdover mode until a clock reappears. If both copies of the 19.44MHz from CLK2A and CLK2B are lost, the clock control circuitry activates an alarm to the IPMC as long as the telecom sync option is enabled in the shelf.

The PLD is field upgradeable. If upgrade is necessary for this device, an appropriate procedure will be provided with the code update.

Refer to the register description in appendix B.5 and to the ZL30108 datasheet available on Zarlink's web site (www.zarlink.com)for further details on possible clock speed and configuration.

2.9 Redundant IPMC/MMC Firmware & BootBlock

The IPMC/MMC run firmware from their internal 512KB flash. The BootBlock manager keeps the two copies of the IPMC/MMC firmware in dedicated flash memories. It acts as a watchdog to the IPMC/MMC and can rollback a firmware update in the IPMC/MMC in case of problems.

Note:
The IPMC/MMC has an internal hardware watchdog.

Chapter 3

Installing the Board

3. Installing the Board

3.1 Setting Jumpers

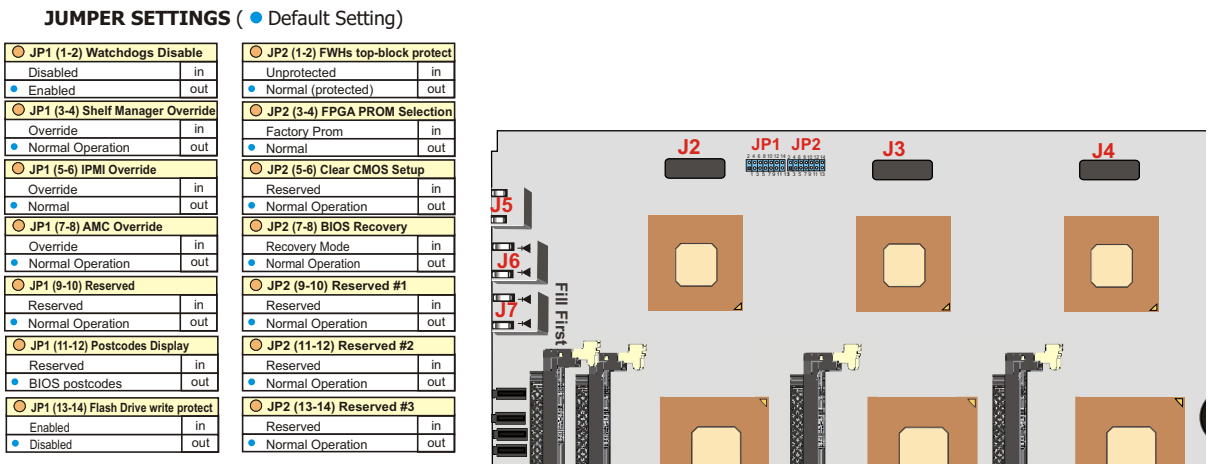
3.1.1 Jumper Description

Table 3-1:Jumper Description

Name	Description	Jumper
Watchdogs Disable		JP1 (1-2)
Shelf Manager Override		JP1 (3-4)
IPMI Override		JP1 (5-6)
AMC Override		JP1 (7-8)
AMC PCIe Override		JP1 (9-10)
Postcodes Display		JP1 (11-12)
Flash Drive Write Protect		JP1 (13-14)
FWHs top-block Protect		JP2 (1-2)
FPGA PROM Selection		JP2 (3-4)
Clear CMOS Setup		JP2 (5-6)
BIOS Recovery		JP2 (7-8)
Reserved #1		JP2(9-10)
Reserved #2		JP2 (11-12)
Reserved #3		JP2 (13-14)

3.1.2 Setting Jumper & Locations

Figure 3-1:Setting Jumpers & Locations



Note:
More details about the jumper settings can be found on the Quick Reference Sheet.

3.2 Processor

This product ships with the CPUs and a thermal solution installed. Because the thermal solution is custom and critical for passive cooling. Cooling performance can greatly be affected if manipulation is not handled within Kontron facility.

3.3 Memory

The CPU engines use 240 pins, 25 degree DIMM sockets. They are interfaced through a single memory channel that supports registered ECC x4 or x8 memory. CPU engines 1 & 2 provide only one DIMM while CPU engine 0 provides 2 DIMM. DDR2 400, 1.8 V, max. 1.2 inches high registered DIMMs must be used. The maximum DDR2 SDRAM size is 8 GB for CPU engine 0 and 4GB for CPU engine 1 and 2. The minimum size of SDRAM is 512 MB using a single 512 Mbit technology DIMM (9x8 DRAMs). The CPU engines support "single sided" and "dual sided" (single/dual rank) memory modules. This gives a possibility of 4 ranks for CPU 0 and 2 ranks for CPU1 & 2.

The PowerQuicc III has one SO-CDIMM (512MB DDR2-400 SDRAM).

All memory busses operate at 200 MHz clock speed with dual data rate. This means that data is transferred at 400 MHz.

The content of the SDRAM is not affected by a warm reset.

Only use validated memory with this product. Thermal issues or other problems may arise if you don't use recommended modules. At the time of publication of this user guide, the following memories were confirmed functional with the product. As the memory market is volatile, this list is subject to change, please consult your local technical support for an up to date list.

3.3.1 CPU engines 0, 1 & 2 memory list and characteristics:

Table 3-2: CPU engines 0, 1 & 2 memory list and characteristics

Manufacturer Part Number	Description	Company
M393T2863AZA-CE6	DIMM DDR2-533 1GB	Samsung
M393T5660AZA-CE6	DIMM DDR2-533 2GB	Samsung
M393T5166AZA-CE6	DIMM DDR2-533 4GB	Samsung

Memory should have the following characteristics:

- DDR2 400
- 1.8V only
- Single-sided or double-sided
- 1 layer of BGA on PCB side

- X4 or X8 configuration supported
- Serial Presence Detect (SPD) EEPROM
- 72-bit DIMMs only
- 1.2 inch maximum height

3.3.2 PowerQuicc III memory list and characteristics:

Table 3-3: PowerQuicc III memory list and characteristics

Manufacturer Part Number	Description	Company
VL491T6553T-D5	DIMM DDR2-400 512MB ECC	Virtium Technology Inc.

The Unit Computer DDR2 SDRAM memory is assembled on a SO-CDIMM. The SO-CDIMM is an upcoming JEDEC standard that uses the DDR2 SODIMM envelope but modifies the pinout in order to add ECC support. This means that the bus width supported is 64 bits plus 8 bits for ECC. The DDR2 SDRAM module is clocked at 200Mhz. The design supports modules of 512MB. This memory module consists of 9 CMOS DDR2 SDRAM chips. Standard DDR2-SODIMM are not supported.

Memory should have the following characteristics:

- DDR2 400
- 1.8V only
- Single-sided or double-sided
- 1 layer of BGA on PCB side
- X8 configuration supported
- Serial Presence Detect (SPD) EEPROM
- 72-bit DIMMs only
- 1.2 inch maximum height

WARNING

Because static electricity can cause damage to electronic devices, take the following precautions:

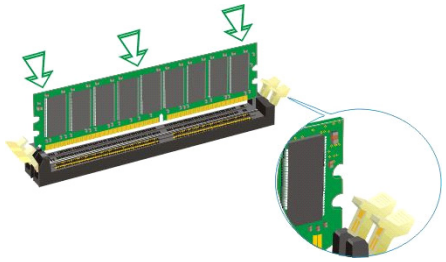
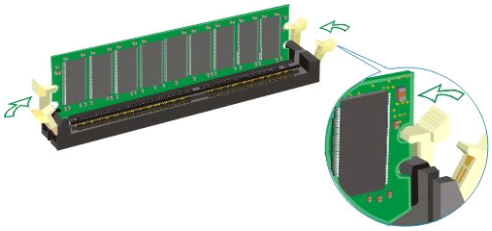
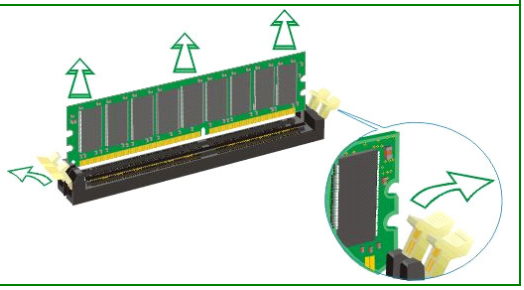
Keep the board in its anti-static package, until you are ready to install memory.

Wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.

Handle the board by the faceplate or its edges.

3.3.3 Installing Memory

Figure 3-2:Installing Memory

On an anti-static plane, place the board so that you are facing the memory sockets	
Insert the memory module into any available socket, aligning the notches on the module with the socket's key inserts.	
Push down the memory module until the retaining clips clip on each side.	
Repeat these steps to populate the other socket.	
To remove a memory module from a socket, push sideway the retaining clips on each side of the socket, to release the module. Pull out the memory from the socket.	

3.4 Onboard Interconnectivity

3.4.1 Onboard Connectors and Headers

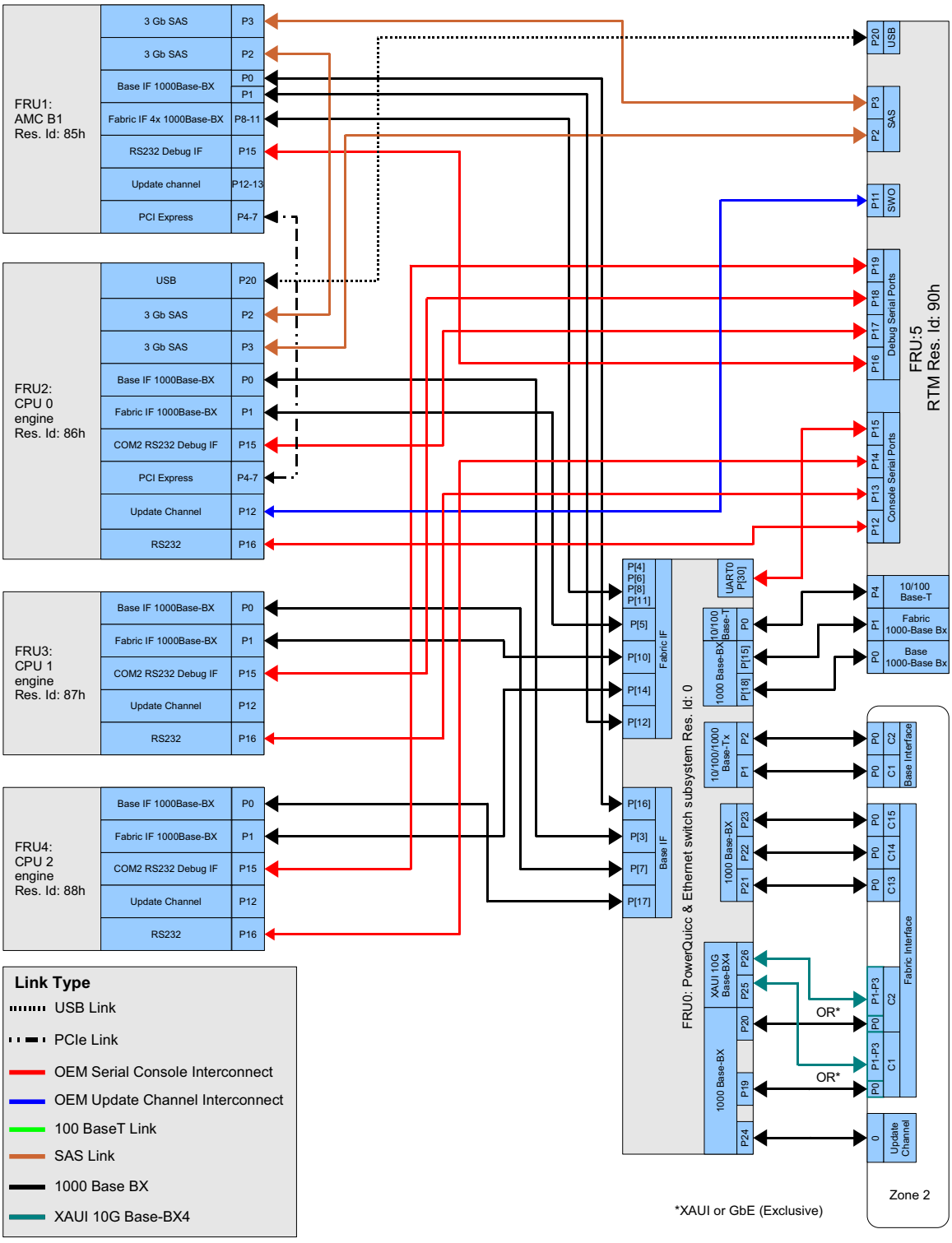
Table 3-4:Onboard Connectors and Headers

Description	Connector	Comments
CPU 0 XDP ITP	J2	CPU 0
CPU 1 XDP ITP	J3	CPU 1
CPU 2 XDP ITP	J4	CPU 2
Serial Port	J5	Shared RJ-45 Serial port connector
Ethernet	J6	Ethernet, CPU Engine 0
Ethernet	J7	Ethernet, CPU Engine 0
USB CPU0/A	J10	USB 2.0 Connector on faceplate, CPU Engine 0
CPU 0 Memory	J11 - J12	CPU 0 Memory sockets
CPU 1 Memory	J13	CPU 1 Memory socket
CPU 2 Memory	J14	CPU 2 Memory socket
USB CPU2	J15	USB 2.0 Connector on faceplate, CPU Engine 2
USB CPU0/B	J16	USB 2.0 Connector on faceplate, CPU Engine 0
USB CPU1	J17	USB 2.0 Connector on faceplate, CPU Engine 1
ES Memory	J18	ES Memory soket
Update Ch. / Telco Clock	J20	Update Channel and Telco Clock connector (Zone 2)
Base Interfac & Fabric Interface	J23	Base & Frabric Interfcae Connector (Zone 2)
RTM Connector	J30	RTM connector to connect to the ARTM3(Zone 3)
AMC B1	B1	Mid-Size AMC connector
Power Connector	P10	Power Connector (Zone 1)

3.4.2 Board and Carrier Point-to-Point Interconnect Overview

The Front Blade Unit is divided in multiple sections. In this way, each CPU engine represents a virtual AMC. The following figure represents all virtual devices present on the Front Blade Unit and the virtual links. This figure helps to clarify some sections for the E-Keying. It gives an overview of the logical/physical interconnections available between AMC and carrier components, including pseudo AMCs, virtual carrier resources and intelligent RTM.

Figure 3-3:Board and Carrier Point-to-Point Interconnect Overview



3.5 Board Hot Swap and Installation

Because of the high-density pinout of the hard-metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1 Rail guides must be installed on the enclosure to slide the board to the backplane.

2 Do not force the board if there is mechanical resistance while inserting the board.

3 Screw the frontplate to the enclosure to firmly attach the board to its enclosure.

4 Use extractor handles to disconnect and extract the board from its enclosure.

WARNING

Always use a grounding wrist wrap before installing or removing the board from a chassis.

3.5.1 Installing the Card in the Chassis

To install a card in a chassis:

1 Remove the filler panel of the slot or see "Removing the Board" below.

2 Ensure the board is configured properly.

3 Carefully align the PCB edges in the bottom and top card guide.

4 Insert the board in the system until it makes contact with the backplane connectors.

5 Using both ejector handles, engage the board in the backplane connectors until both ejectors are locked.

6 Fasten screws at the top and bottom of the faceplate.

3.5.2 Removing the Board

If you would like to remove a card from your chassis please follow carefully these steps:

1 Unscrew the top and the bottom screw of the front panel.

2 Unlock the lower handle latch, depending on the software step; this may initiate a clean shutdown of the operating system.

3 Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.

4 Use both ejectors to disengage the board from the backplane.

5 Pull the board out of the chassis.

3.5.3 Installing an AMC

To install an AMC:

1 Remove the AMC filler panel.

2 Carefully engage the AMC into the card guide. Push the AMC until it fully mate with its connector. Secure the AMC handle to the locking position.

3 In normal condition, the blue LED shall turn ON as soon as the AMC is fully inserted. It will turn OFF at the end of the hot swap sequence.

3.5.4 Removing an AMC

To remove an AMC:

1 Pull out the handle to unlock the AMC.

2 Wait for the blue LED to turn on continuously.

3 Pull out the AMC using the handle.

3.5.5 Installing the RTM8030

To install the RTM:

1 Remove the filler panel of the slot.

2 Ensure the board is configured properly.

3 Carefully align the PCB edges in the bottom and top card guide.

4 Insert the board in the system until it makes contact with the CPU board.

5 Using both ejector handles, engage the board in the CPU board connectors until both ejectors are locked.

6 Fasten screws at the top and bottom of the faceplate.

3.5.6 Removing the RTM8030

To remove the RTM:

1 Unscrew the top and the bottom screw of the faceplate.

2 Unlock the lower handle latch.

3 Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.

4 Use both ejectors to disengage the board from the CPU board.

5 Pull the board out of the chassis.

Chapter 4

Hardware Management

4. Hardware Management

4.1 Hardware Management Overview

The purpose of the hardware management system is to monitor, control, ensure proper operation and provides hot swap support of AdvancedTCA Boards. The hardware management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. It can retrieve inventory information and sensor readings as well as receive event reports and failure notifications from boards and other Intelligent FRUs. The hardware management system can also perform basic recovery operations such as power cycle or reset of managed entities.

4.2 Hardware Management Architecture on Front Blade Unit

Each CPU blade is logically independent and seen as built-in AMC.

The Zone 1 connector is the card power entry, the dual IPMB and the chassis slot address. The power entry is a dual -48Vdc. The IPMB is the I2C bus that connects the IPMC to the Shelf manager. The Hardware address is the 8 bit port that defines the address of the blade in the chassis.

The Zone 2 contains the base and the fabric interface. The Base interface is feed with two 1000 Base-T Ethernet link to an onboard Ethernet switch. Each CPU has an Ethernet link connected to the switch. This allows the IPMI Controller of each CPU to receive IPMI Over LAN command and send Serial Over LAN data to the two base interface channels. The Fabric Interface is two XAUI 10G Base-CX4 links.

The Zone 3 connector (RTM Interface) has three GbE link that come from the Base interface switch, the fabric interface switch and the PowerQuicc. Within PICMG wording, the RTM is an intelligent FRU of the blade which means it includes an IPMI Controller. The interface to that RTM IPMI Controller is IPMB-L and is accessible from the IPMC as a regular AMC. A serial port connector is also available on the RTM and is connected to the desired CPU using a rotary switch.

4.3 Hardware Management Functionality

The Front Blade Unit supports an “intelligent” hardware management system, based on the Intelligent Platform Management Interface Specification. The hardware management system of the Front Blade Unit provides the ability to manage the power and interconnect needs of intelligent devices, to monitor events, and to log events to a central repository.

4.3.1 IPMC specific features (FRU0)

4.3.1.1 IPMC - ShMC interface

The principal management-oriented link within a Shelf is a two-way redundant implementation of the Intelligent Platform Management Bus (IPMB). IPMB is based on the inter-integrated circuit (I2C) bus and is part of the IPMI architecture. In AdvancedTCA Shelves, the main IPMB is called IPMB-0. Each entity attached to IPMB-0 does so through an IPM Controller, the distributed management controller of the IPMI architecture. Shelf Managers attach to IPMB-0 through a variant IPM Controller called the Shelf Management Controller (ShMC). AdvancedTCA IPM Controllers, besides supporting dual redundant IPMBs, also have responsibility for detecting and recovering from IPMB faults.

The reliability of the AdvancedTCA IPMB-0 is improved by using two IPMBs, with the two IPMBs referenced as IPMB-A and IPMB-B. The aggregation of the two IPMBs is IPMB-0. The IPM Controllers aggregate the information received on both IPMBs. An IPM Controller that has a message ready for transmit uses the IPMBs in a round robin fashion. An IPM Controller tries to alternate the transmission of messages between IPMB-A and IPMB-B.

If an IPM Controller is unable to transmit on the desired IPMB then it tries to send the message on the alternate IPMB. By using this approach, an IPMB can become unavailable and then available without the IPM Controller needing to take specific action.

4.3.1.2 IPMC - System Manager Interface

The Section 25 of [IPMI 1.5] describes how IPMI messages can be sent to and from the IPMC encapsulated in RMCP (Remote Management Control Protocol) packets datagrams. This capability is also referred to as “IPMI over LAN” (IOL). IPMI also defines the associated LAN-specific configuration interfaces for setting things such as IP addresses other options, as well as commands for discovering IPMI-based systems. The Distributed Management Task Force (DMTF) specifies the RMCP format. This LAN communication path make the Front Blade Unit reachable to the System Manager for any management action (IPMC firmware upgrade, query of all FRU Data, CPU reset etc.) without the needs to goes through the ShMC.

On the Ethernet Switch, this communication path is supported from the OS layer. Since the Ethernet Switch is parts of the FRU 0 payload power, the IPMI over LAN is available only when payload is powered on FRU0 (M4 active) and the OS of Ethernet Switch is running. Kontron includes the open source "OpenIPMI" LAN software modules under the Linux OS of the Ethernet Switch to provide the IPMI over LAN feature. For more information see: http://openipmi.sourceforge.net/

The features of IPMI over LAN offers by Open IPMI is provided as is, Kontron will not support, enhance or provides maintenance for any of the Open IPMI software module.

4.3.1.3 IPMC - Payload interface

The IPMC payload interface of the Front Blade Unit uses the standard IPMI KCS interface. The IPMC KCS interface is visible from Ethernet Switch Linux OS. The standard Open IPMI Linux driver build for PowerPC is able to communicate with the IPMC through the standard KCS driver implementation.

The FPGA bridges the two bus type, since the H8S2166 used for IPMC has LPC host interface and the Ethernet Switch has LBC interface.

4.3.1.4 IPMC - System Event Log

The Kontron IPMC implementation includes a Local System Event Log device as specified in the Section 12 of [IPMI 1.5]. The local System Event Log is a nonvolatile repository for the front board and all managed FRU events (AMC/RTM/MMC built in). The local SEL uses 17.4K of non volatile storage and provides space for 1023 entries. However, even if blade events are log into the local SEL, the IPMI platform event messages are still generated by the IPMC's Event Generator and sent to the centralized SEL hosted by the Shelf Manager through the IPMB-0 communication path - [PICMG 3.0] chapter 3.5; [IPMI 1.5] Section 23. Local SEL is useful for maintenance purposes and provides access to the events when the FRU is extracted from the Shelf.

4.3.2 OEM Sensors

The IPMI v1.5 specification describes most of the sensors on the Front Blade Unit. However, in some situation, the IPMI specification does not have adequate sensor definition for the specific Unit or AdvancedTCA features. To fill this gap, the IPMI specification provides the ability to create OEM sensor definition that fulfills specific needs. Using OEM sensor for the System Management Software requires a-priori knowledge of the OEM "sensor type" and OEM-defined "Event/Reading Type Code" enumeration. The following table describes Kontron OEM sensor.

Table 4-1:Kontron OEM Power Good Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
77h OEM Kontron ATCA Power Good	08h Standard IPMI Power Supply	00h	VccGood 12V
		01h	VccGood 5V
		02h	VccGood 3.3V
		03h	VccGood 2.5V
		04h	VccGood 1.8V
		05h	VccGood 1.5V
		06h	VccGood 1.2V
		07h	VccGood Core
		08h	VccGood -5V
		09h	VccGood 1.1V
		10h	VccGood 1.05V
		11h	VccGood 1.25V

Table 4-2:Kontron OEM FRU Info Agent Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
0Ah Standard IPMI Discrete	C5h OEM Kontron FRU Info Agent	06h	Transition to degraded Event Data 2 is used a bit flag error Bit 7: unspecifiedError Bit 6: notPresentError Bit 5: multirecHeaderError Bit 4: multirecDataError Bit 3: timeout error Bit 2: ipmcError Bit 1: fruDataError Bit 0: commonHeaderError Event Data 3 is used a bit flag error Bit 7: reserved Bit 6: reserved Bit 5: SetPortState Not Supported Bit 4: SetPortState Error Bit 3: reserved Bit 2: reserved Bit 1: reserved Bit 0: Match Error, Not in single link matches
		08h	Install Error Event Data 2 is used a bit flag error Bit 7: unspecifiedError Bit 6: notPresentError Bit 5: multirecHeaderError Bit 4: multirecDataError Bit 3: timeout error Bit 2: ipmcError Bit 1: fruDataError Bit 0: commonHeaderError Event Data 3 is used a bit flag error Bit 7: SetClockState Not Supported Bit 6: SetClockState Error Bit 5: SetPortState Not Supported Bit 4: SetPortState Error Bit 3: Clock Internal Mismatch Bit 2: Clock Match Error, Not a single clock matches Bit 1: Internal mismatch Bit 0: Match Error, Not in single link matches

Table 4-3:Kontron OEM IPMB-L Link Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
6Fh Standard IPMI sensor specific	C3h OEM Kontron IPMB-L Link	02h	IPMB-L Disable Event Data 2: always 0 Event Data 3: bit[7:3]: always 0 bit [2:0]: 0h = no failure 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = clock low timeout 6h = Under test (the IPM Controller is attempting to determine who is causing a bus hang) 07h = Undiagnosed Communication Failure
		03h	IPMB-L Enable Event Data 2: always 0 Event Data 3: bit[7:3]: always 0 bit [2:0]: 0h = no failure 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = clock low timeout 6h = Under test (the IPM Controller is attempting to determine who is causing a bus hang) 07h = Undiagnosed Communication Failure

Table 4-4:Kontron OEM POST Code Value Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
6Fh Standard IPMI sensor specific	C6h OEM Kontron POST Code Value	00h to 07h	POST code LOW byte value, no event genarated on these offsets
		14h	POST Code Error Event Trigger Event Data 2: POST Low Nibble Event Data 3: POST High Nibble

Table 4-5:Kontron OEM Management Controller firmware ugrade Status Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
6Fh Standard IPMI sensor specific	C7h OEM Management Controller firmware upgrade Status	00h	First Boot asfet upgrade
		01h	First Boot after rollback

Table 4-6:Kontron OEM Switch Management Status Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
6Fh Standard IPMI sensor specific	C8h OEM Kontron Switch Management Status	00h	Switch Management Software Not Loaded (No event generated)
		01h	Switch Management Software Initializing (No event generated)
		02h	Switch Management Ready (No event generated)
		03h	Switch Management Software Fail Event Data 2: 00h :OS configuration file corrupted 01h: OS startup failure 02h: Switch Management Application Fail

Table 4-7:Kontron OEM Diagnostic Status Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
6Fh Standard IPMI sensor specific	C9h OEM Kontron Diagnostic Status	00h	Diagnostic Started
		01h	Diagnostic PASS
		02h	Diagnostic FAIL

Table 4-8:Kontron OEM External Component Firmware Upgrade Status Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
6Fh Standard IPMI sensor specific	CAh OEM Kontron External Component Firmware Upgrade Status	00h	Firmware upgrade in progress (no event).
		01h	Firmware upgrade succeeded.
		02h	Firmware upgrade failed.

Table 4-9:Kontron OEM FRU Over current Sensor definition

Event/Reading type code	"Sensor type	Sensor Specific offset	Event Trigger
03h Standard IPMI Discrete	CBh OEM Kontron FRU Over Current	00h 01h State Asserted / State Deasserted	Event Data 2: 00h: Over Current on Management power. 01h: Over Current on Payload power. Event Data 3:FRU ID

Table 4-10:Kontron OEM FRU Sensor error Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
03h Standard IPMI Discrete	CCh OEM Kontron FRU Sensor Error	00h 01h State Asserted / State Deasserted	Event Data 2: undefined Event Data 3:FRU ID

Table 4-11:Kontron OEM FRU Power denied Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
03h Standard IPMI Discrete	CDh OEM Kontron FRU Power denied	00h 01h State Asserted / State Deasserted	Event Data 2: Power denial cause 00h : Explicit by shelf manager or application 01h : Decided by carrier based on fru information 03h : Timeout (shelf manager didn't grant power in time) FFh : Undefined Event Data 3 :FRU ID

Table 4-12:Kontron OEM Reset Sensor definition

Event/Reading type code	Sensor type	Sensor Specific offset	Event Trigger
03h Standard IPMI Discrete	CFh OEM Kontron Reset	00h 01h State Asserted / State Deasserted	Event Data 2: Reset Type 00h: Warm reset 01h: Cold reset 02h: Forced Cold [Warm reset reverted to Cold] 03h: Soft reset [Software jump] Event Data 3: Reset Source 00h: IPMI Watchdog [cold, warm or forced cold] (IPMI Watchdog2 sensors gives additionnal details) 01h: IPMI commands [cold, warm or forced cold] (chassis control, fru control) 02h: Processor internal checkstop 03h: Processor internal reset request 04h: Reset button [warm or forced cold] 05h: Power up [cold] 06h: Legacy Initial Watchdog / Warm Reset Loop Detection * [cold reset] 07h: Legacy Programmable Watchdog [cold, warm or forced cold] 08h: Software Initiated [soft, cold, warm of forced cold] 09h: Setup Reset [Software Initiated Cold] FFh: Unknown

4.4 IPMC

4.4.1 Supported commands

The table below lists the IPMI commands supported by the IPMC (FRU0). This table is identical as the one provided by AMC.0 and PICMG 3.0. The last column states the Kontron support for the specific command.

Table 4-13:IPM Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
IPM Device "Global" Commands				M	M	
Get Device ID	17.1	App	01h	M	M	Yes
Cold Reset	17.2	App	02h	O	O	Yes
Warm Reset	17.3	App	03h	O	O	No
Get Self Test Results	17.4	App	04h	M	M	Yes
Manufacturing Test On	17.5	App	05h	O	O	Yes
Set ACPI Power State	17.6	App	06h	O	O	No
Get ACPI Power State	17.7	App	07h	O	O	No
Get Device GUID	17.8	App	08h	O	O	No
Broadcast "Get Device ID"	17.9	App	01h	O/M	M	Yes

Table 4-14:Watchdog Timer Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
BMC Watchdog Timer Commands				M	M	
Reset Watchdog Timer	21.5	App	22h	M	M	Yes
Set Watchdog Timer	21.6	App	24h	M	M	Yes
Get Watchdog Timer	21.7	App	25h	M	M	Yes

Table 4-15:Device Messaging Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
BMC Device and Messaging Commands[5]				M	O	
Set BMC Global Enables	18.1	App	2Eh	M	O/M	Yes
Get BMC Global Enables	18.2	App	2Fh	M	O/M	Yes
Clear Message Flags	18.3	App	30h	M	O/M	Yes

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Get Message Flags	18.4	App	31h	M	O/M	Yes
Enable Message Channel Receive	18.5	App	32h	O	O	Yes
Get Message	18.6	App	33h	M	O/M	Yes
Send Message	18.7	App	34h	M	M	Yes
Read Event Message Buffer	18.8	App	35h	O	O	Yes
Get BT Interface Capabilities	18.9	App	36h	M	O/M	Yes
Master Write-Read	18.10	App	52h	M	O/M	No
Get System GUID	18.13	App	37h	O	O	No
Get Channel Authentication Capabilities	18.12	App	38h	O	O	No
Get Session Challenge	18.14	App	39h	O	O	No
Activate Session	18.15	App	3Ah	O	O	No
Set Session Privilege Level	18.16	App	3Bh	O	O	No
Close Session	18.17	App	3Ch	O	O	No
Get Session Info	18.18	App	3Dh	O	O	No
Get AuthCode	18.19	App	3Fh	O	O	No
Set Channel Access	18.20	App	40h	O	O	No
Get Channel Access	18.21	App	41h	O	O	No
Get Channel Info	18.22	App	42h	O	O	No
Set User Access	18.23	App	43h	O	O	No
Get User Access	18.24	App	44h	O	O	No
Set User Name	18.25	App	45h	O	O	No
Get User Name	18.26	App	46h	O	O	No
Set User Password	18.27	App	47h	O	O	No

Table 4-16:Chassis Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Chassis Device Commands				O	O	
Get Chassis Capabilities	22.1	Chassis	00h	M	O	Yes
Get Chassis Status	22.2	Chassis	01h	O/M	O	Yes
Chassis Control	22.3	Chassis	02h	O/M	O	Yes
Chassis Reset	22.4	Chassis	03h	O	O	No
Chassis Identify	22.5	Chassis	04h	O	O	No
Set Chassis Capabilities	22.6	Chassis	05h	O	O	No
Set Power Restore Policy	22.7	Chassis	06h	O	O	No

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Get System Restart Cause	22.9	Chassis	07h	O	O	No
Get System Restart Cause	22.10	Chassis	08h	O	O	No
Get System Restart Cause	22.11	Chassis	09h	O	O	No
Get POH Counter	22.12	Chassis	0Fh	O	O	No

Table 4-17:Event Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Event Commands				M	M	
Set Event Receiver	23.1	S/E	01h	M	M	Yes
Get Event Receiver	23.2	S/E	02h	M	M	Yes
Platform Event (a.k.a. “Event Message”)	23.3	S/E	03h	M	M	Yes

Table 4-18:PEF and Alerting Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
PEF and Alerting Commands				O	O	
Get PEF Capabilities	24.1	S/E	10h	M	M	No
Arm PEF Postpone Timer	24.2	S/E	11h	M	M	No
Set PEF Configuration Parameters	24.3	S/E	12h	M	M	No
Get PEF Configuration Parameters	24.4	S/E	13h	M	M	No
Set Last Processed Event ID	24.5	S/E	14h	M	M	No
Get Last Processed Event ID	24.6	S/E	15h	M	M	No
Alert Immediate	24.7	S/E	16h	O	O	No
PET Acknowledge	24.8	S/E	17h	O	O	No

Table 4-19:Sensor Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Sensor Device Commands				O	M	
Get Device SDR Info	29.2	S/E	20h	O	M	Yes
Get Device SDR	29.3	S/E	21h	O	M	Yes
Reserve Device SDR Repository	29.4	S/E	22h	O	M	Yes
Get Sensor Reading Factors	29.5	S/E	23h	O	M	No
Set Sensor Hysteresis	29.6	S/E	24h	O	O	Yes
Get Sensor Hysteresis	29.7	S/E	25h	O	O	Yes
Set Sensor Threshold	29.8	S/E	26h	O	O	Yes
Get Sensor Threshold	29.9	S/E	27h	O	O	Yes
Set Sensor Event Enable	29.10	S/E	28h	O	O	Yes
Get Sensor Event Enable	29.11	S/E	29h	O	O	Yes
Re-arm Sensor Events	29.12	S/E	2Ah	O	O	No
Get Sensor Event Status	29.13	S/E	2Bh	O	O	No
Get Sensor Reading	29.14	S/E	2Dh	M	M	Yes
Set Sensor Type	29.15	S/E	2Eh	O	O	No
Get Sensor Type	29.16	S/E	2Fh	O	O	No

Table 4-20:FRU Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
FRU Device Commands				M	M	
Get FRU Inventory Area Info	28.1	Storage	10h	M	M	Yes
Read FRU Data	28.2	Storage	11h	M	M	Yes
Write FRU Data	28.3	Storage	12h	M	M	Yes

Table 4-21:SDR Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
SDR Device Commands				M	O	
Get SDR Repository Info	27.9	Storage	20h	M	M	No
Get SDR Repository Allocation Info	27.10	Storage	21h	O	O	No
Reserve SDR Repository	27.11	Storage	22h	M	M	No
Get SDR	27.12	Storage	23h	M	M	No

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Add SDR	27.13	Storage	24h	M	O/M	No
Partial Add SDR	27.14	Storage	25h	M	O/M	No
Delete SDR	27.15	Storage	26h	O	O	No
Clear SDR Repository	27.16	Storage	27h	M	O/M	No
Get SDR Repository Time	27.17	Storage	28h	O/M	O/M	No
Set SDR Repository Time	27.18	Storage	29h	O/M	O/M	No
Enter SDR Repository Update Mode	27.19	Storage	2Ah	O	O	No
Exit SDR Repository Update Mode	27.20	Storage	2Bh	M	M	No
Run Initialization Agent	27.21	Storage	2Ch	O	O	No

Table 4-22:SEL Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
SEL Device Commands				M	O	
Get SEL Info	25.2	Storage	40h	M	M	Yes
Get SEL Allocation Info	25.3	Storage	41h	O	O	Yes
Reserve SEL	25.4	Storage	42h	O	O	Yes
Get SEL Entry	25.5	Storage	43h	M	M	Yes
Add SEL Entry	25.6	Storage	44h	M	M	Yes
Partial Add SEL Entry	25.7	Storage	45h	M	M	No
Delete SEL Entry	25.8	Storage	46h	O	O	Yes
Clear SEL	25.9	Storage	47h	M	M	Yes
Get SEL Time	25.10	Storage	48h	M	M	Yes
Set SEL Time	25.11	Storage	49h	M	M	Yes
Get Auxiliary Log Status	25.12	Storage	5Ah	O	O	No
Set Auxiliary Log Status	25.13	Storage	5Bh	O	O	No

Table 4-23:LAN Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
LAN Device Commands				O	O	
Set LAN Configuration Parameters	19.1	Transport	01h	O/M	O/M	No
Get LAN Configuration Parameters	19.2	Transport	02h	O/M	O/M	No
Suspend BMC ARPs	19.3	Transport	03h	O/M	O/M	No
Get IP/UDP/RMCP Statistics	19.4	Transport	04h	O	O	No

Table 4-24:Serial/Modem Device Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Serial/Modem Device Commands				0	0	
Set Serial/Modem Configuration	20.1	Transport	10h	O/M	O/M	No
Get Serial/Modem Configuration	20.2	Transport	11h	O/M	O/M	No
Set Serial/Modem Mux	20.3	Transport	12h	O	O	No
Get TAP Response Codes	20.4	Transport	13h	O	O	No
Set PPP UDP Proxy Transmit Data	20.5	Transport	14h	O	O	No
Get PPP UDP Proxy Transmit Data	20.6	Transport	15h	O	O	No
Send PPP UDP Proxy Packet	20.7	Transport	16h	O	O	No
Get PPP UDP Proxy Receive Data	20.8	Transport	17h	O	O	No
Serial/Modem Connection Active	20.9	Transport	18h	O/M	O/M	No
Callback	20.10	Transport	19h	O	O	No
Set User Callback Options	20.11	Transport	1Ah	O	O	No
Get User Callback Options	20.12	Transport	1Bh	O	O	No

Table 4-25:Bridge (ICMB) Management Supported Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Bridge Management Commands (ICMB)[2]				0	0	
Get Bridge State	[ICMB]	Bridge	00h	O/M	O	No
Set Bridge State	[ICMB]	Bridge	01h	O/M	O	No
Get ICMB Address	[ICMB]	Bridge	02h	O/M	O	No
Set ICMB Address	[ICMB]	Bridge	03h	O/M	O	No
Set Bridge Proxy Address	[ICMB]	Bridge	04h	O/M	O	No
Get Bridge Statistics	[ICMB]	Bridge	05h	O/M	O	No
Get ICMB Capabilities	[ICMB]	Bridge	06h	O/M	O	No
Clear Bridge Statistics	[ICMB]	Bridge	08h	O/M	O	No

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Get Bridge Proxy Address	[ICMB]	Bridge	09h	O/M	O	No
Get ICMB Connector Info	[ICMB]	Bridge	0Ah	O/M	O	No
Get ICMB Connection ID	[ICMB]	Bridge	0Bh	O/M	O	No
Send ICMB Connection ID	[ICMB]	Bridge	0Ch	O/M	O	No

Table 4-26:Discovery (ICMB) Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Discovery Commands (ICMB)[2]				O	O	
Prepare For Discovery	[ICMB]	Bridge	10h	O/M	O	No
Get Addresses	[ICMB]	Bridge	11h	O/M	O	No
Set Discovered	[ICMB]	Bridge	12h	O/M	O	No
Get Chassis Device ID	[ICMB]	Bridge	13h	O/M	O	No
Set Chassis Device ID	[ICMB]	Bridge	14h	O/M	O	No

Table 4-27:Bridging (ICMB) Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Bridging Commands (ICMB)[2]				O	O	
Bridge Request	[ICMB]	Bridge	20h	O/M	O	No
Bridge Message	[ICMB]	Bridge	21h	O/M	O	No

Table 4-28:Event (ICMB) Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Event Commands (ICMB) [2]				O	O	
Get Event Count	[ICMB]	Bridge	30h	O/M	O	No
Set Event Destination	[ICMB]	Bridge	31h	O/M	O	No

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Set Event Reception State	[ICMB]	Bridge	32h	O/M	O	No
Send ICMB Event Message	[ICMB]	Bridge	33h	O/M	O	No
Get Event Destination	[ICMB]	Bridge	34h	O/M	O	No
Get Event Reception State	[ICMB]	Bridge	35h	O/M	O	No

Table 4-29:OEM for Bridge NetFn (ICMB) Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
OEM Commands for Bridge NetFn				O	O	
OEM Commands	[ICMB]	Bridge	C0h-FEh	O/M	O	No

Table 4-30:Other Bridge (ICMB) Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Other Bridge Commands				O	O	
Error Report	[ICMB]	Bridge	FFh	O/M	O	No

Table 4-31:PICMG 3.0 Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
AdvancedTCA®	PICMG® 3.0 Table				M	
Get PICMG Properties	3-9	PICMG	00h		M	Yes
Get Address Info	3-8	PICMG	01h		M	Yes
Get Shelf Address Info	3-13	PICMG	02h		O	N/A
Set Shelf Address Info	3-14	PICMG	03h		O	N/A
FRU Control	3-22	PICMG	04h		M	Yes
Get FRU LED Properties	3-24	PICMG	05h		M	Yes
Get LED Color Capabilities	3-25	PICMG	06h		M	Yes
Set FRU LED State	3-26	PICMG	07h		M	Yes
Get FRU LED State	3-27	PICMG	08h		M	Yes
Set IPMB State	3-51	PICMG	09h		M	Yes
Set FRU Activation Policy	3-17	PICMG	0Ah		M	Yes
Get FRU Activation Policy	3-18	PICMG	0Bh		M	Yes

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
Set FRU Activation	3-16	PICMG	0Ch		M	Yes
Get Device Locator Record ID	3-29	PICMG	0Dh		M	Yes
Set Port State	3-41	PICMG	0Eh		O/M	Yes
Get Port State	3-42	PICMG	0Fh		O/M	Yes
Compute Power Properties	3-60	PICMG	10h		M	Yes
Set Power Level	3-62	PICMG	11h		M	Yes
Get Power Level	3-61	PICMG	12h		M	Yes
Renegotiate Power	3-66	PICMG	13h		O	N/A
Get Fan Speed Properties	3-63	PICMG	14h		M if controls Shelf fans	N/A
Set Fan Level	3-65	PICMG	15h		O/M	N/A
Get Fan Level	3-64	PICMG	16h		O/M	N/A
Bused Resource	3-44	PICMG	17h		O/M	N/A
Get IPMB Link Info	3-49	PICMG	18h		O/M	Yes
FRU Control Capabilities	3-24	PICMG	1Eh		M	Yes

Table 4-32:AMC.0 Carrier Commands for IPMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on IPMC
AMC	AMC.0 Table					
Set AMC Port State	Table 3-27	PICMG	19h		O/M	Yes
Get AMC Port State	Table 3-28	PICMG	1Ah		O/M	Yes
Set Clock State	Table 3-44	PICMG	2Ch		O/M	Yes
Get Clock State	Table 3-45	PICMG	2Dh		O/M	Yes

4.4.2 Sensor Data Records

Information that describes the IPMC capabilities is provided through two mechanisms: capabilities commands and Sensor Data Records (SDRs). Capabilities commands are commands within the IPMI command set that return fields providing information on other commands and functions the controller can handle.

Sensor Data Records are data records containing information about the type and number of sensors in the platform, sensor threshold support, event generation capabilities, and information on what types of readings the sensor provides. The primary purpose of Sensor Data Records is to describe the sensor configuration of the hardware management subsystem to system software.

The IPMC are required to maintain Device Sensor Data Records for the sensors and objects they manage. Access methods for the Device SDR entries are described in the [IPMI 1.5] specification, Section 29, "Sensor Device Commands."

After a FRU is inserted, the System Manager, using the Shelf Manager, may gather the various SDRs from the FRU's IPM Controller to learn the various objects and how to use them. The System Manager uses the "Sensor Device Commands" to gather this information. Thus, commands, such as "Get Device SDR Info" and "Get Device SDR," which are optional in the IPMI specification, are mandatory in AdvancedTCA systems.

Most of the current Shelf Manager implementation gathers the individual Device Sensor Data Records of each FRU into a centralized SDR Repository. This SDR Repository may exist in either the Shelf Manager or System Manager. If the Shelf Manager implements the SDR Repository on-board, it shall also respond to "SDR Repository" commands.

This duplication of SDR repository commands creates sometime some confusion among AdvancedTCA users. This is mandatory for IPMC to support the Sensor Device Commands for IPMC built-in SDR as described in the [IPMI 1.5] specification, Section 29, "Sensor Device Commands." For the ShMC, the same set of commands for the centralized SDR Repository must be supported but they are described in the [IPMI 1.5] specification, Section 27, "SDR Repository Commands."

4.4.2.1 IPMC (FRU0) sensors

Table 4-33:FRU0 sensors

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
0	FRU0 Hot Swap	ATCA Board FRU Hot Swap Sensor, Sensor type = F0h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific -see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
1	FRU1 Hot Swap	External AMC Bay (B1) Hot Swap sensor, Sensor type = F0h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific -see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
2	FRU2 Hot Swap	Built in AMC CPU0 (B2) Hot Swap sensor, Sensor type = F0h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific -see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
3	FRU3 Hot Swap	Built in AMC CPU1 (B3) Hot Swap sensor, Sensor type = F0h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific -see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
4	FRU4 Hot Swap	Built in AMC CPU2 (B4) Hot Swap sensor, Sensor type = F0h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific -see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
5	FRU5 Hot Swap	RTM Hot Swap sensor, Sensor type = F0h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
6	FRU0 Reconfig	Sensor Population Change on Carrier caused by manage FRU insertion/ extraction, Sensor type = 12h System Event, Event Reading type code = 6Fh Sensor specific, only offset 0 is used, -see AMC.0 R2.0 for event trigger and, -see IPMI v1.5 table 36.3, Sensor type code 12h for sensor definition
7	Temp Switch	Switch Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 90°C: After Thermal Analysis. -Upper Critical event: 100°C: After Thermal Analysis. -Upper Non-Recoverable: 115°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
8	Temp Dual Phy Co	Dual PHY Copper Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 80°C: After Thermal Analysis. -Upper Critical event: 90°C: After Thermal Analysis. -Upper Non-Recoverable:105°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
9	Temp SOC-DIMM	SOC-DIMM Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 75°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 100°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
10	Temp Air Inlet	Air inlet Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 65°C: After Thermal Analysis. -Upper Critical event: 75°C: After Thermal Analysis. -Upper Non-Recoverable:90°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
11	Temp PQ3	PQ3 Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 75°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 100°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
12	Temp Dual Phy Se	Dual PHY SERDES Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 80°C: After Thermal Analysis. -Upper Critical event: 90°C: After Thermal Analysis. -Upper Non-Recoverable: 105°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
13	Temp LSI SAS Dis	Dual LSI SAS Disc Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 80°C: After Thermal Analysis. -Upper Critical event: 90°C: After Thermal Analysis. -Upper Non-Recoverable: 105°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
14	Temp Mez 12v Out	Power Mezzanine 12v Output Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 70°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 110°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
15	Temp -48 A Feed	Power Mezzanine Feed A Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 70°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 110°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
16	Temp -48 B Feed	Power Mezzanine Feed B Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 70°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 110°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
17	Power Good	Actual power status Sensor type = 08h Power Supply, Event Reading type code = 77h OEM see table sws-10-1137 for event trigger information
18	Power Good Event	Power status event that occur since the last power on or reset. Sensor type = 08h Power Supply, Event Reading type code = 77h OEM see table sws-10-1137 for event trigger information
19	Vcc -48 V A Feed	Voltage on -48v feed A board input power supply Sensor type = 02h voltage, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 37.5v Lower Critical event: -75v Hysteresis: 1.26v
20	Vcc -48 V B Feed	Voltage on -48v feed B board input power supply Sensor type = 02h voltage, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 37.5v Lower Critical event: -75v Hysteresis: 1.26v
21	Fuse-Pres A Feed	Fuse presence and fault detection -48 V on supply A Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : Presence detected, always present and do not generate event offset 1 event trigger: Power supply Failure detected = fuse blown -see IPMI v1.5 table x.xx, Sensor type code 08h for sensor definition
22	Fuse-Pres B Feed	Fuse presence and fault detection -48 V on supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : Presence detected, always present and do not generate event offset 1 event trigger: Power supply Failure detected = fuse blown -see IPMI v1.5 table x.xx, Sensor type code 08h for sensor definition
23	Fuse-RTN A Feed	Fuse presence and fault detection RTN (Return) on supply A Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0: Presence detected, always present and do not generate event offset 1: Power supply Failure detected, event trigger = fuse blown -see IPMI v1.5 table x.xx, Sensor type code 08h for sensor definition

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
24	Fuse-RTN B Feed	Fuse presence and fault detection RTN (Return) on supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : Presence detected, always present and do not generate event offset 1 event trigger: Power supply Failure detected = fuse blown -see IPMI v1.5 table x.xx, Sensor type code 08h for sensor definition
25	Fuse-Earl A Feed	Fuse presence and fault detection RTN (Return) on supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : Presence detected, always present and do not generate event offset 1 event trigger: Power supply Failure detected = fuse blown -see IPMI v1.5 table x.xx, Sensor type code 08h for sensor definition
26	Fuse-Earl B Feed	Fuse presence and fault detection RTN (Return) on supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : Presence detected, always present and do not generate event offset 1 event trigger: Power supply Failure detected = fuse blown -see IPMI v1.5 table x.xx, Sensor type code 08h for sensor definition
27	FRU input Power	FRU 0 Power consumption in watts, FRU 0 also includes FRU2/3/4 Sensor type = 0Bh Other Unit-Based Sensor (Watt) Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 180 Watts (TBC). -Upper Critical event: 200 Watts (TBC). -Hysteresis: 20 Watts
28	FRU1 Power	FRU 1 (AMC B2) Power consumption in watts Sensor type = 0Bh Other Unit-Based Sensor (Watt) Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 27 Watts (TBC). -Upper Critical event: 30 Watts (TBC). -Hysteresis: 3.75 Watts
29	FRU5 Power	FRU 5 (RTM) Power consumption in watts Sensor type = 0Bh Other Unit-Based Sensor (Watt) Event Reading type code = 01h threshold base event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 21.25 Watts (TBC). -Upper Critical event: 25Watts (TBC). -Hysteresis: 1.75 Watts
30	Board Reset	Board reset type and sources Sensor type = CFh OEM (Kontron Reset Sensor), Event Reading type code = 03h Digital Discrete offset 0,1 are used, see table sws-10-1177 for event trigger information

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
31	EventRcv ComLost	Specify if the communication with the event receiver (ShMc) has been lost. Sensor type = 1Bh Cable/Interconnect, Event Reading type code = 03h Digital Discrete, offset 0: event trigger, communication with ShMC lost offset 1: event trigger, communication with ShMC regain -see IPMI v1.5 table 36.2 and table 36.3 for sensor definition
32	IPMI Watchdog	IPMI Watchdog Sensor type = 23h Watchdog 2, Event Reading type code = 6Fh Sensor specific -see IPMI v1.5 table 36.2 and table 36.3 for sensor definition
33	IPMC Link State	IPMB-0 fault detection sensor Sensor type = F1h PICMG Physical IPMB-0 , Event Reading type code = 6Fh Sensor specific -see PICMG 3.0R2.0 section 3.8.4.2 for event trigger and sensor definition
34	FRU0 IPMBL State	IPMB-L branch from FRU0 fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
35	FRU1 IPMBL State	IPMB-L branch from FRU1 fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
36	FRU2 IPMBL State	IPMB-L branch from FRU2 fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
37	FRU3 IPMBL State	IPMB-L branch from FRU3 fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
38	FRU4 IPMBL State	IPMB-L branch from FRU4 fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
39	FRU5 IPMBL State	IPMB-L branch from FRU5 fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
40	Health Error	General health status, Aggregation of critical sensor This list is flexible and could be adjust based on customer requirements. Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, no critical sensors is asserted offset 1: event trigger, one or multiple critical sensors are asserted see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
41	FRU Over Icc	FRU OEM Over Current Sensor type = CBh OEM (Kontron FRU Over Current) Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, no Over Current offset 1: event trigger, Over Current detected see table sws-10-1174 for event trigger information
42	FRU Sensor Error	FRU Error during external FRU Sensor discovery Sensor type = CCh OEM (Kontron FRU sensor error) Event Reading type code = 03h Digital Discrete offset 0,1 are used, see table sws-10-1175 for event trigger information
43	FRU Pwr Denied	FRU is not allowed to power up because it power request is deny Sensor type = CDh OEM (Kontron FRU Power denied), Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU see table sws-10-1176 for event trigger information
44	FRU0 Agent	Module Data agent that verify FRU0 Data validity (checksum/E-key/etc) Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0AFh Generic Discrete, offset 6,8 are used, see table sws-10-1138 for event trigger information
45	FRU1 Agent	Module Data agent that verify FRU1 Data validity (checksum/E-key/etc) Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0AFh Generic Discrete, offset 6,8 are used, see table sws-10-1138 for event trigger information
46	FRU5 Agent	Module Data agent that verify FRU5 Data validity (checksum/E-key/etc) Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0AFh Generic Discrete, offset 6,8 are used, see table sws-10-1138 for event trigger information
47	IPMC Storage Err	Management sub-system health: non volatile memory error. Sensor type = 28h Management Subsystem Health Event Reading type code = 6Fh Sensor specific, only offset 1 is used, offset 1: event trigger, IPMC Non volatile memory error see IPMI v1.5 table 36.3, Sensor type code 28h for sensor definition
48	IPMC Reboot	IPMC reboot detection Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, Normal Condition (IPMC is running) offset 1: event trigger, IPMC has reboot see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition
49	Ver change	IPMC firmware upgrade detection Sensor type = 2Bh Version Change Event Reading type code = 6Fh Sensor specific, only offset 1 is used, offset 1/event data 2: 00h (unspecified): event trigger, A sensor configuration has changed offset 1/event data 2: 02h (Firm. Rev.): event trigger, A Firmware Upgrade has been done see IPMI v1.5 table 36.3, Sensor type code 2Bh (Version Change) for sensor definition

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
50	SEL State	Specify if the status of the SEL (Cleared/Almost Full/Full) Sensor type = 10h Event Logging Disable Event Reading type code = 6Fh Sensor specific, only offset 2,4,5 are used, offset 2: event trigger, The SEL has been cleared offset 4: event trigger, The SEL is Full offset 5: event trigger, The SEL has reached 75% of its capacity see IPMI v1.5 table 36.3, Sensor type code 10h (Event Log Disable) for sensor definition
51	Vcc +1.1	Voltage on 1.2v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.16v (10%) Lower Critical Event: 1.04v (10%) Hysteresis: 0.017v (1.5%)
52	Vcc +1.2	Voltage on 1.2v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.26v (5%) Lower Critical Event: 1.14v (5%) Hysteresis: 0.018v (1.5%)
53	Vcc +1.25	Voltage on 1.25v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1,312v (5%) Lower Critical event: 1,187v (5%) Hysteresis: 0,0187v (1.5%)
54	Vcc +1.5V	Voltage on 1.5v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.58v (5%) Lower Critical event: 1.42v (5%) Hysteresis: 0.025v (1.5%)
55	Vcc +1.8V	Voltage on 1.8v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.89v (5%) Lower Critical event: 1.71v (5%) Hysteresis: 0.027v (1.5%)
56	Vcc +2.5V	Voltage on 2.5v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 2.63v (5%) Lower Critical event: 2.37v (5%) Hysteresis: 0.038v (1.5%)

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
57	Vcc +3.3V	Voltage on 3.3v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 3.47v (5%) Lower Critical event: 3.13v (5%) Hysteresis: 0.050v (1.5%)
58	Vcc +5V	Voltage on 5v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 5.25v (5%) Lower Critical event: 4.75v (5%) Hysteresis: 0.075v (1.5%)
59	Vcc Mez Hold-UP	Voltage on power mezsanine Vcc HUV Hold-UP/Audio filter Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 59.2v (5%) Lower Critical event: 16v (5%) Hysteresis: 1.6v (1.5%)
60	Vcc +12V	Voltage on 12v board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 12.60v (5%) Lower Critical event: 11.40v (5%) Hysteresis: 0.180v (1.5%)
61	Vcc +1.2 SUS	Voltage on 1.2v suspend (management) board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.26v (10%) Lower Critical event: 1.14v (10%) Hysteresis: 0.018v (1.5%)
62	Vcc +3.3V SUS	Voltage on 3.3v suspend (management) board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 3.47v (5%) Lower Critical event: 3.13v (5%) Hysteresis: 0.050v (1.5%)
63	Vcc +5V SUS	Voltage on 5v suspend (management) board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 5.25v (5%) Lower Critical event: 4.75v (5%) Hysteresis: 0.075v (1.5%)

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
64	Vcc +12V SUS	Voltage on 12v suspend (management) board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 12.60v (5%) Lower Critical event: 11.40v (5%) Hysteresis: 0.180v (1.5%)
65	Vcc +2.5V REF	Voltage on 2.5v REF board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 2.63v (5%) Lower Critical event: 2.37v (5%) Hysteresis: 0.038v (1.5%)
66	Vcc +12V AMC	Voltage on 12v AMC power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 12.60v (5%) Lower Critical event: 11.40v (5%) Hysteresis: 0.180v (1.5%)
67	Vcc +12V RTM	Voltage on 12v RTM power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 12.60v (5%) Lower Critical event: 11.40v (5%) Hysteresis: 0.180v (1.5%)
72	TelcoClock Alarm	Sensor type = 24h Platform Alert Event Reading type code = 03h digital Discrete (deasserted/asserted), offset 0 and 1 are used, offset 0: event trigger - (deasserted) telecom clock synchronisation alarm deasserted offset 1: event trigger - (asserted) telecon clock synchronisation alarm asserted
73	Telecom Sync	Sensor type = 24h Platform Alert Event Reading type code = 03h digital Discrete (Disabled/Enabled), offset 0 and 1 are used, offset 0: event trigger - chassis telecom clock support Disable offset 1: event trigger - chassis telecom clock support Enable see IPMI v1.5 table 36.3, Sensor type code 24h (Platform Alert) for sensor definition
74	PQ3 Boot Error	U-BOOT Boot error sensor Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, offset 0 and 3 are used, offset 0: event trigger - OS load failed offset 3: event trigger - Boot monitor load failed see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
75	PQ3 POST Error	U-BOOT System Firmware Progress Sensor type = 0Fh System Firmware Progress Event Reading type code = 6Fh Sensor specific, only offset 0 is used, offset 0/event data 2: 00h (unspecified): event trigger, A Boot monitor POST failure offset 0/event data 2: 0Bh (Firm. corruption.): event trigger, Boot monitor backup image loaded/ Primary boot monitor corrupted see IPMI v1.5 table 36.3, Sensor type code 0Fh (System Firmware Progress) for sensor definition
76	PQ3 POST Value	Show current U-BOOT postcode value. No event generated by this sensor. Sensor type = C6h OEM (Kontron POST value sensor), Event Reading type code = 6Fh Sensor specific, offset 0 to 7 and 14 are used, see table sws-10-1140 for event trigger information
77	PQ3 OS stop	PQ3 OS critical Stop, Sensor type = 20h OS Critical Stop, Event Reading type code = 6Fhh Sensor specific, only offset 1 is used, offset 1: event trigger, Linux Kernel panic encontered see IPMI v1.5 table 36.3, Sensor type code 20h (OS Critical Stop) for sensor definition
78	PQ3 Critical Int	PQ3 Processor checkstop condition encontered Sensor type = 13h Critical Interrupt, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, normal condition, no checkstop offset 1: event trigger, processor is in checkstop condition see IPMI v1.5 table 36.3, Sensor type code 03h for sensor definition
79	PQ3 Diag Status	PQ3 Diagnostic Status Sensor type = C9h OEM (Kontron OEM Diagnostic Status), Event Reading type code = 6Fh Sensor specific, offset 0,1,2 are used, see table sws-10-1152 for event trigger information
80	PQ3 FwUp Status	Kontron OEM External Component firmware upgrade Status Sensor type = CAh OEM (OEM Kontron External Component Firmware Upgrade Status), Event Reading type code = 6Fh Sensor specific, offset 0,1,2 are used,
81	Switch Status	U-BOOT OEM Switch Management Status Sensor type = C8h OEM (Kontron Switch Management Status), Event Reading type code = 6Fh Sensor specific, offset 0,1,2,3 are used,
82	IPMC FwUp	Kontron OEM IPMC firmware upgrade Status Sensor type = C7h OEM (Management Controller firmware upgrade Status), Event Reading type code = 6Fh Sensor specific, offset 0,1are used
83	Temp Pres SPD0	Internal Temperature sensor presence on SOC-DIMM (sensor 9), if absent on board diode is used Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger: no event generated (Entity Present) offset 1 event trigger: no event generated (Entity Absent) see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition.

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event Trigger)
84	Fault SAS0	Fault status on SAS 0 link hook on CPU0, Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, no critical sensors is asserted offset 1: event trigger, one or multiple critical sensors are asserted see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition.
85	Fault SAS1	Fault on SAS 1 link hook on CPU0, Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, no critical sensors is asserted offset 1: event trigger, one or multiple critical sensors are asserted see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition.
86	IPMI Info-1	Internal IPMC firmware diagnostic event trigger: internal error condition
87	IPMI Info-2	Internal IPMC firmware diagnostic event trigger: internal error condition

4.4.2.2 IPMC (FRU0) sensors aggregation for health sensor

The following table shows the sensors involved in the health sensor aggregation.

Table 4-34:FRU0 Sensor Name

Sensor Name
Temp Switch
Temp Dual Phy Co
Temp SOC-DIMM
Temp Air Inlet
Temp PQ3
Temp Dual Phy Se
Temp LSI SAS Dis
Temp Mez 12v Out
Temp -48 A Feed
Temp -48 B Feed
Power Good Event
IPMI Watchdog
PQ3 Reset
PQ3 POST Value
PQ3 OS stop
PQ3 Critical Int
Vcc -48 V A
Vcc -48 V B
Vcc +1.1

Sensor Name
Vcc +1.2
Vcc +1.25
Vcc +1.5V
Vcc +1.8V
Vcc +2.5V
Vcc +3.3V
Vcc +5V
Vcc Mez Hold-UP
Vcc +12V
Vcc +1.2 SUS
Vcc +3.3V SUS
Vcc +5V SUS
Vcc +12V SUS
Vcc +2.5V REF
Vcc +12V AMC
Vcc +12V RTM

4.4.3 FRU Information

Table 4-35:ES - Board Information Area

ES – Board Information Area	
Field Description	Value (hex)
Format Version	0x01
Board Area Length	*Calculated
Language code	0x19
Manufacturing Date / Time	*Based on mfg. date
Board Manufacturer type/length	*Calculated
Board Manufacturer	"KONTRON "
Board Name type/length	*Calculated
Board Name	“AT8030”
Board Serial Number type/length	*Calculated
Board Serial Number	*10 digits serial number
Board Part Number type/length	*Calculated
Board Part Number	T5006###
FRU File ID type/length	0x00

ES – Board Information Area	
FRU File ID	null
No more fields	0xC1
Padding	0x00
Board Area Checksum	*Calculated

Table 4-36:ES - Product Information Area

ES – Product Information Area	
Field Description	Value (hex)
Format Version	0x01
Product Area Length	*Calculated
Language code	0x19
Product Manufacturer type/length	*Calculated
Product Manufacturer	"KONTRON "
Product Name type/ length	*Calculated
Product Name	“AT8030”
Product Part Number type/length	*Calculated
Product Part Number	T5006###
Product Version type/ length	*Calculated
Product Version	XX
Product Serial Number type/length	*Calculated
Product Serial Number	XXXXXXXXX
Product Part Number type/length	*Calculated
Asset Tag type/length	0xC0
Asset Tag	null
FRU File ID type/length	*Calculated
FRU File ID	“FRU5006-XX" *
No more fields	0xC1
Padding	0x00
Board Area Checksum	*Calculated

* Variable X, may change on revisions.

4.4.3.1 IPMC (FRU 0) Board E-Keying Information

One or more Board Point-to-Point Connectivity Records are included in the Board FRU Information and describe the connections to the Base, Fabric, and Update Channel Interfaces that are implemented on the

Board. These connections, each consisting of some subset of the Ports in one or more Channels, are generically referred to as a link. For more details about this record refer to PICMG 3.0 R2.0 section 3.7.2.3

In addition to mandatory base interface links and to the XAUI capability on the fabric, this record describes: alternative 1000Base-BX links on the fabric channel 1 and 2 and OEM connectivity on the update channel.

Table 4-37:Board Point-to-Point Connectivity Record

Type 14 – Atca Point-to-Point Connectivity Record	
Record Type ID	C0h
Record type ID	0xC0
Format Version	0x82 (last record)
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Type 14 – Atca Point-to-Point Connectivity Record (Data)	
Record Type ID	C0h
Record format version	02h
Manufacturer ID	00315Ah (PICMG Record ID)
PICMG Record ID	14h (Board Point-To-Point Connectivity Record)
Record Format Version	00h
OEM GUID Count	01h
OEM GUID List	
OEM GUID [F0]	OEM Redundancy Update Channel
Link Descriptor	00001101h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : None
Link Type (Bits 19-12)	01h : PICMG 3.0 Base Interface 10/100/ 1000 BASE-T
Link Designator (Bits 11-0)	101h : Base Interface, Channel 1, Port 0
Link Descriptor	00001102h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : None
Link Type (Bits 19-12)	01h : PICMG 3.0 Base Interface 10/100/ 1000 BASE-T
Link Designator (Bits 11-0)	102h : Base Interface, Channel 2, Port 0
Link Descriptor	00102F41h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	1h : Fixed 10GBASE-BX4 [XAUI]
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface
Link Designator (Bits 11-0)	F41h : Fabric Interface, Channel 1, Port 0, 1, 2, 3
Link Descriptor	00102141h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : Fixed 1000Base-BX
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface

Type 14 – Atca Point-to-Point Connectivity Record	
Link Designator (Bits 11-0)	141h : Fabric Interface, Channel 1, Port 0
Link Descriptor	00102F42h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	1h : Fixed 10GBASE-BX4 [XAUI]
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface
Link Designator (Bits 11-0)	F42h : Fabric Interface, Channel 2, Port 0, 1, 2, 3
Link Descriptor	00102142h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : Fixed 1000Base-BX
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface
Link Designator (Bits 11-0)	142h : Fabric Interface, Channel 2, Port 0
Link Descriptor	000F0F81h
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : None
Link Type (Bits 19-12)	F0h : OEM GUID Definition
Link Designator (Bits 11-0)	F81h : Update Channel Interface 1, Port 0 (all ten pairs)
Link Descriptor	0010214Dh
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : Fixed 1000Base-BX
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface
Link Designator (Bits 11-0)	14Dh : Fabric Interface, Channel 13, Port 0
Link Descriptor	0010214Eh
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : Fixed 1000Base-BX
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface
Link Designator (Bits 11-0)	14Eh : Fabric Interface, Channel 14, Port 0
Link Descriptor	0010214Fh
Link Grouping ID (Bits 31-24)	0h : Single-Channel link
Link Type Extension (Bits 23-20)	0h : Fixed 1000Base-BX
Link Type (Bits 19-12)	02h : PICMG 3.1 Ethernet Fabric Interface
Link Designator (Bits 11-0)	14Fh : Fabric Interface, Channel 15, Port 0

4.4.3.2 IPMC (FRU 0) Carrier Activation and Carrier Information Table

The following structure describes the maximum internal current, the current capacity of the AMC Bays, and their power on treatment.

TBC: Module Current and Maximum Internal Current needs to be confirmed after the Hardware qualification.

Table 4-38:AMC Carrier Activation and Current Management Record

Type 17 Carrier Activation And Current Management Record	
Record Type ID	C0h
Record format version	02h
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Manufacturer ID	00315Ah
PICMG Record ID	17h
Record Format Version	00h
Type 17 Carrier Activation And Current Management Record (Data)	
Maximum Internal Current	0069h (10.5 Amps at 12 V => 126 Watts)
Allowance for Module Activation Readiness	002h
Module Activation and Power Descriptor Count	05h
Carrier Activation and Power Descriptors.	7Ah, 19h, FFh
Local IPMB Address	7Ah
Maximum Module Current	15h (2.1 Amps at 12 V => 25.2 Watts)
Reserved	FFh
Carrier Activation and Power Descriptors.	7Ch, 32h, FFh
Local IPMB Address	7Ch (CPU0 Engine)
Maximum Module Current	22h (3.40 Amps at 12 V => 40.8 Watts)
Reserved	FFh
Carrier Activation and Power Descriptors.	7Eh, 19h, FFh
Local IPMB Address	7Eh (CPU1 Engine)
Maximum Module Current	19h (2.50 Amps at 12 V => 30 Watts)
Reserved	FFh
Carrier Activation and Power Descriptors.	80h, 19h, FFh
Local IPMB Address	80h (CPU2 Engine)
Maximum Module Current	19h (2.50 Amps at 12 V => 30 Watts)
Reserved	FFh
Carrier Activation and Power Descriptors.	90h, 19h, FFh
Local IPMB Address	90h
Maximum Module Current	09h (0.90 Amps at 12 V => 10.8 Watts)
Reserved	FFh

The Carrier Information Table shows the required FRU Information format that describes the specific AMC Bays implemented on a Carrier. For each AMC Bay on the Carrier, the Carrier Information Table includes a Site Number for that AMC Bay. The Carrier Information Table also includes a byte that contains the AMC.0 specification revision supported by the Carrier IPMC. Only the AMC.0 real physical site numbers are included, as AMC B1 is the only physical site available to the operator.

Table 4-39:Carrier Information Table Record

Type 1Ah Carrier Information Table Record	
Record Type ID	C0h
Record format version	02h
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Manufacturer ID	00315Ah (PICMG Record ID)
PICMG Record ID	0x1A (Carrier Information Table)
Record Format Version	00h
AMC.0 Extension Version	02h (AMC.0 R2.0)
Carrier Site Number Count	01h
Carrier Site Number	05h

4.4.3.3 IPMC (FRU 0) Carrier Point-To-Point Connectivity Information

The Carrier Point-to-Point Connectivity record is included in the Carrier FRU Information and describes the point-to-point connections implemented on the Carrier. The carrier FRU Information may include several Carrier Point-to-Point Connectivity records if a single record is not sufficient for describing all point-to-point connections implemented on the Carrier. The Carrier IPMC treats these multiple records as a single logical point-to-point AMC Bay Descriptors list. For more details about this record refer to AMC.0 R2.0 Section 3.9.1.

Table 4-40:Carrier Point-To-Point Connectivity Record

Type 18 - Carrier Point-To-Point Connectivity Record	
Record Type ID	C0h
Record format version	02h
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Manufacturer ID	00315Ah (PICMG Record ID)
PICMG Record ID	18h (Carrier Point-To-Point Connectivity Record)
Record Format Version	00h
Type 18 - Carrier Point-To-Point Connectivity Record (Data)	
Point-to-Point AMC Resource Descriptor	
Resource ID	85h -> AMC Bay (AMC B1)
Point-to-Point Count	0Eh
Point-to-Point Resource Descriptor	001000h
Reserved (Bits 23-18)	0

Type 18 - Carrier Point-To-Point Connectivity Record	
Local Port (Bits 13-17)	0
Remote Port (Bit 12-8)	16
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Count	0Eh
Point-to-Point Resource Descriptor	000C00h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	1
Remote Port (Bit 12-8)	12
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	004286h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	2
Remote Port (Bit 12-8)	2
Remote Ressource ID (Bits 7-0)	86h-> CPU0, B2 (SAS Controller))
Point-to-Point Resource Descriptor	006390h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	3
Remote Port (Bit 12-8)	3
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [SAS]
Point-to-Point Resource Descriptor	008486h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	4
Remote Port (Bit 12-8)	4
Remote Ressource ID (Bits 7-0)	86h-> CPU0, B2 (MCH PCI Express Port A)
Point-to-Point Resource Descriptor	00A586h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	5
Remote Port (Bit 12-8)	5
Remote Ressource ID (Bits 7-0)	86h-> CPU0, B2 (MCH PCI Express Port A)
Point-to-Point Resource Descriptor	00C686h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	6
Remote Port (Bit 12-8)	6
Remote Ressource ID (Bits 7-0)	86h-> CPU0, B2 (MCH PCI Express Port A)
Point-to-Point Resource Descriptor	00E786h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	7
Remote Port (Bit 12-8)	7
Remote Ressource ID (Bits 7-0)	86h-> CPU0, B2 (MCH PCI Express Port A)
Point-to-Point Resource Descriptor	010400H
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	8

Type 18 - Carrier Point-To-Point Connectivity Record	
Remote Port (Bit 12-8)	4
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	012600h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	9
Remote Port (Bit 12-8)	6
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	014800h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	10
Remote Port (Bit 12-8)	8
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	016B00h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	11
Remote Port (Bit 12-8)	11
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	018001h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	12
Remote Port (Bit 12-8)	0
Remote Ressource ID (Bits 7-0)	01h-> Update Channel Switch
Point-to-Point Resource Descriptor	01A101h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	13
Remote Port (Bit 12-8)	1
Remote Ressource ID (Bits 7-0)	01h-> Update Channel Switch
Point-to-Point Resource Descriptor	
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	15
Remote Port (Bit 12-8)	16
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [SERIAL]
Resource ID	86h -> CPU0 (Virtual AMC B2)
Point-to-Point Count	0Bh
Point-to-Point Resource Descriptor	000D00h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	0
Remote Port (Bit 12-8)	13
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	002800h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	1

Type 18 - Carrier Point-To-Point Connectivity Record	
Remote Port (Bit 12-8)	8
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	004285h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	2
Remote Port (Bit 12-8)	2
Remote Ressource ID (Bits 7-0)	85h-> AMC Bay (SAS)
Point-to-Point Resource Descriptor	006380h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	3
Remote Port (Bit 12-8)	3
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [SAS]
Point-to-Point Resource Descriptor	008485h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	4
Remote Port (Bit 12-8)	4
Remote Ressource ID (Bits 7-0)	85h-> AMC Bay(AMC B1 PCIe)
Point-to-Point Resource Descriptor	00A585h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	5
Remote Port (Bit 12-8)	5
Remote Ressource ID (Bits 7-0)	85h-> AMC Bay(AMC B1 PCIe)
Point-to-Point Resource Descriptor	00C685h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	6
Remote Port (Bit 12-8)	6
Remote Ressource ID (Bits 7-0)	85h-> AMC Bay(AMC B1 PCIe)
Point-to-Point Resource Descriptor	00E785h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	7
Remote Port (Bit 12-8)	7
Remote Ressource ID (Bits 7-0)	85h-> AMC Bay(AMC B1 PCIe)
Point-to-Point Resource Descriptor	0018B80h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	12
Remote Port (Bit 12-8)	11
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [SWO/Update Channel]
Point-to-Point Resource Descriptor	01F180h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	15
Remote Port (Bit 12-8)	17
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [Serial]

Type 18 - Carrier Point-To-Point Connectivity Record	
Point-to-Point Resource Descriptor	020C80h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	16
Remote Port (Bit 12-8)	12
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) (Serial FWH)
Point-to-Point Resource Descriptor	029480h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	20
Remote Port (Bit 12-8)	20
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [USB]
Resource ID	87h -> CPU1 (Virtual AMC B3)
Point-to-Point Count	5
Point-to-Point Resource Descriptor	000E00h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	0
Remote Port (Bit 12-8)	14
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	002900h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	1
Remote Port (Bit 12-8)	9
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	018201h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	12
Remote Port (Bit 12-8)	2
Remote Ressource ID (Bits 7-0)	01h-> Update Channel Switch
Point-to-Point Resource Descriptor	01F280h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	15
Remote Port (Bit 12-8)	18
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16) [Serial]
Point-to-Point Resource Descriptor	020D80h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	16
Remote Port (Bit 12-8)	13
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16)
Resource ID	88h -> CPU2 (Virtual AMC B4)
Point-to-Point Count	5
Point-to-Point Resource Descriptor	000F00h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	0

Type 18 - Carrier Point-To-Point Connectivity Record	
Remote Port (Bit 12-8)	15
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	002A00h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	1
Remote Port (Bit 12-8)	10
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	018301h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	12
Remote Port (Bit 12-8)	3
Remote Ressource ID (Bits 7-0)	01h-> Update Channel Switch
Point-to-Point Resource Descriptor	01F380h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	15
Remote Port (Bit 12-8)	19
Remote Ressource ID (Bits 7-0)	89h-> RTM (Serial)
Point-to-Point Resource Descriptor	020E80h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	16
Remote Port (Bit 12-8)	14
Remote Ressource ID (Bits 7-0)	90h-> RTM (Virtual Site Number 16)
Resource ID	90h-> RTM (Virtual Site Number 16)
Point-to-Point Count	4
Point-to-Point Resource Descriptor	000200h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	0
Remote Port (Bit 12-8)	2
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	002300h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	1
Remote Port (Bit 12-8)	3
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	004000h
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	5
Remote Port (Bit 12-8)	0
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Ethernet Switch)
Point-to-Point Resource Descriptor	01F100h

Type 18 - Carrier Point-To-Point Connectivity Record	
Reserved (Bits 23-18)	0
Local Port (Bits 13-17)	15
Remote Port (Bit 12-8)	30
Remote Ressource ID (Bits 7-0)	00h-> Carrier, Device 0 (Serial Port)

4.4.3.4 IPMC (FRU 0) AMC Point-To-Point Connectity Information

Each AMC point-to-point connectivity record contains AMC Link Descriptors, each of which identifies a Link and an associated protocol. Multiple AMC Link Descriptors can exist for a given point-to-point AMC Channel. This is used when a Channel can support multiple protocols such as SAS and SATA. For more details about this record refer to AMC.0 R2.0 Section 3.9.2.

Table 4-41:AMC Point-To-Point Connectivity Record (1 of 2) (Ethernet Switch)

"Type 19h - AMC Point-To-Point Connectivity Record (1 of 2 On-Carrier Ethernet Switch)	
Record Type ID	C0h
Record format version	02h
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Manufacturer ID	00315Ah (PICMG Iana Number)
PICMG Record ID	19h (AMC Point-To-Point Connectivity Record)
Record Format Version	00h
"Type 19h - AMC Point-To-Point Connectivity Record data (1 of 2 On-Carrier Ethernet Switch)	
OEM GUID Count	04h
OEM GUID [F0]	OEM Update Channel Interconnect
OEM GUID [F1]	OEM Serial Console Interconnect
OEM GUID [F2]	OEM 100-BaseT
OEM GUID [F3]	OEM USB Interconnect
Record Type/Connected-device ID	00h (On-Carrier Device 0, Ethernet Switch)
AMC Channel Descriptor Count	0Ch
AMC Channel Descriptor	0FFFFE4h (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	04h
AMC Channel Descriptor	0FFFFE5h (Ethernet Port)
Reserved (Bits 23-20)	0Fh

"Type 19h - AMC Point-To-Point Connectivity Record (1 of 2 On-Carrier Ethernet Switch)	
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	05h
AMC Channel Descriptor	0FFFFE6h (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	06h
AMC Channel Descriptor	0FFFFE7h (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	07h
AMC Channel Descriptor	0FFFFE8h (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	08h
AMC Channel Descriptor	0FFFFE9h (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	09h
AMC Channel Descriptor	0FFFFEAh (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	0Ah
AMC Channel Descriptor	0FFFFEBh (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	0Bh

"Type 19h - AMC Point-To-Point Connectivity Record (1 of 2 On-Carrier Ethernet Switch)	
AMC Channel Descriptor	0FFFFECh (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	0Ch
AMC Channel Descriptor	0FFFFEDh (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	0Dh
AMC Channel Descriptor	0FFFFEEh (Ethernet Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	0Eh
AMC Channel Descriptor	0FFFFF8h (Serial Port)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	18h
AMC Link Descriptor	FC00005100h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0100h : AMC Channel 0, lane 0
AMC Link Descriptor	FC00005101h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0101h : AMC Channel 1, lane 0
AMC Link Descriptor	FC00005102h
Reserved (Bits 39-34)	03Fh

"Type 19h - AMC Point-To-Point Connectivity Record (1 of 2 On-Carrier Ethernet Switch)	
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0102h : AMC Channel 2, lane 0
AMC Link Descriptor	FC00005103h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0103h : AMC Channel 3, lane 0
AMC Link Descriptor	FC00005104h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0104h : AMC Channel 4, lane 0
AMC Link Descriptor	FC00005105h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0105h : AMC Channel 5, lane 0
AMC Link Descriptor	FC00005106h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0106h : AMC Channel 6, lane 0
AMC Link Descriptor	FC00005107h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0107h : AMC Channel 7, lane 0

"Type 19h - AMC Point-To-Point Connectivity Record (1 of 2 On-Carrier Ethernet Switch)	
AMC Link Descriptor	FC00005108h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0108h : AMC Channel 8, lane 0
AMC Link Descriptor	FC00005109h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	0109h : AMC Channel 9, lane 0
AMC Link Descriptor	FC0000510Ah
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	010Ah : AMC Channel 10, lane 0
AMC Link Descriptor	FC0000510Bh
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : 1000 Base BX
AMC Link Type (Bits 19-12)	005h : AMC.2 Ethernet
AMC Link Designator (Bits 11-0)	010Bh : AMC Channel 11, lane 0
AMC Link Descriptor	FC000F010Ch
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : None
AMC Link Type (Bits 19-12)	F1h : OEM GUID Definition (Serial)
AMC Link Designator (Bits 11-0)	010Ch : AMC Channel 12, lane 0

Table 4-42:AMC Point-To-Point Connectivity Record (2 of 2) (Update Channel Switcher)

"Type 19h - AMC Point-To-Point Connectivity Record (2 of 2 On-Carrier Update Channel Switcher)	
Record Type ID	C0h
Record format version	02h
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Manufacturer ID	00315Ah (PICMG Iana Number)
PICMG Record ID	19h (AMC Point-To-Point Connectivity Record)
Record Format Version	00h
"Type 19h - AMC Point-To-Point Connectivity Record Data (2 of 2 On-Carrier Update Channel Switcher)	
OEM GUID Count	01h
OEM GUID [F0]	OEM Update Channel Interconnect
OEM GUID [F1]	OEM Serial Console Interconnect
OEM GUID [F2]	OEM 100-BaseT
OEM GUID [F3]	OEM USB Interconnect
Record Type/Connected-device ID	01h (On-Carrier Device 1,Update Channel Switch)
AMC Channel Descriptor Count	04h
AMC Channel Descriptor	0FFFFE0h (Update Channel)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	00h
AMC Channel Descriptor	0FFFFE1h (Update Channel)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	01h
AMC Channel Descriptor	0FFFFE2h (Update Channel)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	02h
AMC Channel Descriptor	0FFFFE3h (Update Channel)
Reserved (Bits 23-20)	0Fh
Lane 3 Port Number (Bits 19-15)	1Fh

"Type 19h - AMC Point-To-Point Connectivity Record (2 of 2 On-Carrier Update Channel Switcher)	
Lane 2 Port Number (Bits 14-10)	1Fh
Lane 1 Port Number (Bits 9-5)	1Fh
Lane 0 Port Number (Bits 4-0)	03h
AMC Link Descriptor	FC000F0100h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : None
AMC Link Type (Bits 19-12)	F1h : OEM GUID Definition (Update Channel)
AMC Link Designator (Bits 11-0)	0100h : AMC Channel 0, lane 0
AMC Link Descriptor	FC000F0101h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : None
AMC Link Type (Bits 19-12)	F0h : OEM GUID Definition (Update Channel)
AMC Link Designator (Bits 11-0)	0101h : AMC Channel 1, lane 0
AMC Link Descriptor	FC000F0102h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : None
AMC Link Type (Bits 19-12)	F0h : OEM GUID Definition (Update Channel)
AMC Link Designator (Bits 11-0)	0102h : AMC Channel 2, lane 0
AMC Link Descriptor	FC000F0103h
Reserved (Bits 39-34)	03Fh
AMC Asymmetric Match (Bits 33-32)	00b : Exact match
Link Grouping ID (Bits 31-24)	00h : Single Channel Link
AMC Link Type Extension (Bits 23-20)	00h : None
AMC Link Type (Bits 19-12)	F0h : OEM GUID Definition (Update Channel)
AMC Link Designator (Bits 11-0)	0103h : AMC Channel 3, lane 0

4.4.3.5 IPMC (FRU 0) Clock Ekeying Information

The clock ekeying is used to find and activate matching clock pairs to/from available clock sources and clock receivers. The Front Blade Unit hardware implementation specification provides an overview of the clock synchronization structure.

The carrier has a clock generator to be used as the (PCIe) FCLKA of AMC B1. Additionally, clocks from/to the AdvancedTCA backplane can be driven to/from the AMC B1 site using an on-carrier clock multiplexer.

Table 4-43:Carrier Clock Resource Ids assignment table

Carrier Clock Resource Ids	
0	PCIe Clock Generator
1	Clock Multiplexer

As the following tables indicate, match making and clock activation responsibility is split between the Carrier IPMC and the Application. As an exclusive local resource, PCIe clock generator clocks are matched and activated by the Carrier IPMC. However, shared clocks such as AdvancedTCA backplane clocks require control by the Application, as such, the "Clock Control" flag is set to "Activated by the Application" for these resources, and this means that the Application that needs these clocks shall issue a SetClockState (enable) command to the Carrier IPMC as well as to mating resources.

This is the clock ekeying information as it appears in the FRU multirecord area.

For more details about these records and the AMC.0 clock ekeying mechanism refer to AMC.0 R2.0 section 3.9.1.

It should be noted that for the AMC.1R1.0 , FCLKA usage is not yet fully defined by subsidiary specification and is subject to change. The current implementation on this unit is base on the information provided by AMC.0R2.0.

The "Carrier Clock Point-to-Point connectivity record" describes, as its name implies, the point-to-point clock links available between different resources.

Table 4-44:Carrier Clock Point-to-Point Connectivity Record

Type 2C - Carrier Clock Point-To-Point Connectivity Record (Header)		
Record Type ID	C0h	
Record format version	02h	
Record Length	*Calculated	
Record Checksum	*Calculated	
Header Checksum	*Calculated	
Manufacturer ID	00315Ah (PICMG Record ID)	
PICMG Record ID	2C (Carrier Clock Point-To-Point Connectivity Record)	
Record Format Version	00h	
Type 2C - Carrier Clock Point-To-Point Connectivity Record (Data)		
Clock Point-To-Point Resource Descriptor Count (m)		0x02
Clock Point-To-Point Resource Descriptor		
Clock Resource Id	0x00	7:6 00b = On-Carrier device
5:4 0h (reserved)		
3:0 On-Carrier Device 0 (PCIe clock generator)"		
Clock Point-to-Point Connection Count	0x01	
Point-to-Point Clock Connection descriptor		

Type 2C - Carrier Clock Point-To-Point Connectivity Record (Header)		
Local Clock Id	0x00	On-Carrier Clock Id 0
Remote Clock Id	0x05	AMC.0 R2.0 FCLKA clock
Remote Clock Resource Id	0x45	7:6 01b = AMC
5:4 0h (reserved)		
3:0 AMC Site Number (5 = AMC B1)"		
Clock Point-To-Point Resource Descriptor		
Clock Resource Id	0x00	7:6 00b = On-Carrier device
5:4 0h (reserved)		
3:0 On-Carrier Device 1(Clock Mux)"		
Clock Point-to-Point Connection Count	0x0A	
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x00	
Remote Clock Id	0x01	CLK1A
Remote Clock Resource Id	0x80	7:6 10b = Backplane clock
5:4 0h (reserved)		
3:0 0h "		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x01	
Remote Clock Id	0x02	CLK1B
Remote Clock Resource Id	0x80	7:6 10b = Backplane clock
5:4 0h (reserved)		
3:0 0h "		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x02	
Remote Clock Id	0x04	CLK2A
Remote Clock Resource Id	0x80	7:6 10b = Backplane clock
5:4 0h (reserved)		
3:0 0h "		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x03	
Remote Clock Id	0x05	CLK2B
Remote Clock Resource Id	0x80	7:6 10b = Backplane clock
5:4 0h (reserved)		
3:0 0h "		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x04	
Remote Clock Id	0x07	CLK3A
Remote Clock Resource Id	0x80	7:6 10b = Backplane clock
5:4 0h (reserved)		
3:0 0h "		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x05	

Type 2C - Carrier Clock Point-To-Point Connectivity Record (Header)		
Remote Clock Id	0x08	CLK3B
Remote Clock Resource Id	0x80	7:6 10b = Backplane clock
5:4 0h (reserved)		
3:0 0h "		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x06	
Remote Clock Id	0x01	TCLKA
Remote Clock Resource Id	0x45	7:6 01b = AMC
5:4 0h (reserved)		
3:0 AMC Site Number (5 = AMC B1)		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x07	
Remote Clock Id	0x02	TCLKB
Remote Clock Resource Id	0x45	7:6 01b = AMC
5:4 0h (reserved)		
3:0 AMC Site Number (5 = AMC B1)		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x08	
Remote Clock Id	0x03	TCLKC
Remote Clock Resource Id	0x45	7:6 01b = AMC
5:4 0h (reserved)		
3:0 AMC Site Number (5 = AMC B1)		
Point-to-Point Clock Connection descriptor		
Local Clock Id	0x09	
Remote Clock Id	0x04	TCLKD
Remote Clock Resource Id	0x45	7:6 01b = AMC
5:4 0h (reserved)		
3:0 AMC Site Number (5 = AMC B1)		

The "Clock Configuration record" describes, the characteristics of each of the clock identified the previous record . A separate record is present for each of the on-carrier resources.

Table 4-45:AMC.0 R2.0 Clock Configuration Record (1 of 2 PCIe Clock Generator)

Type 2D - Clock Configuration Record	
Record Type ID	C0h
Record format version	02h
Record Length	*Calculated
Record Checksum	*Calculated
Header Checksum	*Calculated
Manufacturer ID	00315Ah (PICMG Record ID)
PICMG Record ID	2D (Clock Configuration Record)

Type 2D - Clock Configuration Record		
Record Format Version	00h	
Type 2D - Clock Configuration Record (Data)		
Clock Resource Id	0x00	7:6 00b = On-Carrier device 5:4 0h (reserved) 3:0 00h = On-Carrier Device 0 (PCIe clock generator)
Clock Configuration Descriptor Count	0x02	
Clock Configuration Descriptors		
Clock Id	0x00	
Clock Control	0x00	7:1 0h (reserved) [0] 0b = Activated by Carrier IPMC
Indirect Clock Descriptors Count(m)	0x00	
Direct Clock Descriptors Count(n)	0x01	
Indirect clock Descriptor		
Direct clock Descriptor		
Features	0x01	7:2 0h (reserved) [1] 0b = Not connected through PLL [0] 1b = Clock source
Family	0x02	Reserved for PCI Express
Accuracy Level	0x00	N/A (TBC: unspecified)
Frequency	0x05F 5E100	100Mhz *tdb : waiting for AMC.1 workgroup on FCLKA usage for PCIe
Min Clock	0x05F 5E100	100Mhz *tdb : waiting for AMC.1 workgroup on FCLKA usage for PCIe
Max Clock	0x05F 5E100	100Mhz *tdb : waiting for AMC.1 workgroup on FCLKA usage for PCIe
Clock Id	0x01	
Clock Control	0x00	7:1 0h (reserved) [0] 0b = Activated by Carrier IPMC
Indirect Clock Descriptors Count(m)	0x00	
Direct Clock Descriptors Count(n)	0x01	
Indirect clock Descriptor		none
Direct clock Descriptor		
Features	0x01	7:2 0h (reserved) [1] 0b = Not connected through PLL [0] 1b = Clock source
Family	0x02	Reserved for PCI Express

Type 2D - Clock Configuration Record					
			Accuracy Level	0x00	N/A (TBC: unspecified)
			Frequency	0x05F 5E100	100Mhz *tdb : waiting for AMC.1 workgroup on FCLKA usage for PCIe
			Min Clock	0x05F 5E100	100Mhz *tdb : waiting for AMC.1 workgroupon FCLKA usage for PCIe
			Max Clock	0x05F 5E100	"100Mhz *tdb : waiting for AMC.1 workgroup on FCLKA usage for PCIe

Table 4-46:AMC.0 R2.0 Clock Configuration Record (2 of 2 Clock Multiplexer)

Type 2D - Clock Configuration Record					
Record Type ID				C0h	
Record format version				02h	
Record Length				*Calculated	
Record Checksum				*Calculated	
Header Checksum				*Calculated	
Manufacturer ID				00315Ah (PICMG Record ID)	
PICMG Record ID				2D (Clock Configuration Record)	
Record Format Version				00h	
Type 2D - Clock Configuration Record (Data)					
Clock Resource Id				0x00	7:6 00b = On-Carrier device 5:4 0h (reserved) 3:0 01h = On-Carrier Device 1 (Clock Multiplexer)
Clock Configuration Descriptor Count				0x0A	
Clock Configuration Descriptors					
	Clock Id			0x00	Receiver input from CLK1A
	Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
	Indirect Clock Descriptors Count(m)			0x02	
	Direct Clock Descriptors Count(n)			0x00	
		Indirect clock Descriptor			
		Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
			Dependent ClockId	6	
		Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
			Dependent ClockId	7	
		Direct clock Descriptor			none
	Clock Id			0x01	Receiver input from CLK2A

Type 2D - Clock Configuration Record				
Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
Indirect Clock Descriptors Count(m)			0x02	
Direct Clock Descriptors Count(n)			0x00	
Indirect clock Descriptor				
	Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
		Dependent ClockId	6	
	Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
		Dependent ClockId	7	
Direct clock Descriptor				none
Clock Id			0x02	Receiver input from CLK1B
Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
Indirect Clock Descriptors Count(m)			0x02	
Direct Clock Descriptors Count(n)			0x00	
Indirect clock Descriptor				
	Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
		Dependent ClockId	6	
	Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
		Dependent ClockId	7	
Direct clock Descriptor				none
Clock Id			0x03	Receiver input from CLK2B
Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
Indirect Clock Descriptors Count(m)			0x02	
Direct Clock Descriptors Count(n)			0x00	
Indirect clock Descriptor				
	Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
		Dependent ClockId	6	
	Clock Descriptor 1	Features		7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
		Dependent ClockId	7	
Direct clock Descriptor				none

Type 2D - Clock Configuration Record				
Clock Id			0x04	Source output to CLK3A
Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
Indirect Clock Descriptors Count(m)			0x02	
Direct Clock Descriptors Count(n)			0x00	
Indirect clock Descriptor				
	Clock Descriptor 0	Features	0x01	7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source
		Dependent ClockId	8	
	Clock Descriptor 1	Features	0x01	7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source
		Dependent ClockId	9	
	Direct clock Descriptor			none
Clock Id			0x05	Source output to CLK3B
Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
Indirect Clock Descriptors Count(m)			0x02	
Direct Clock Descriptors Count(n)			0x00	
Indirect clock Descriptor				
	Clock Descriptor 0	Features	0x01	7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source
		Dependent ClockId	8	
	Clock Descriptor 1	Features	0x01	7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source
		Dependent ClockId	9	
	Direct clock Descriptor			none
Clock Id			0x06	Source output to TCLKA
Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
Indirect Clock Descriptors Count(m)			0x04	
Direct Clock Descriptors Count(n)			0x00	
Indirect clock Descriptor				
	Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
		Dependent ClockId	0	

Type 2D - Clock Configuration Record					
		Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	1	
		Clock Descriptor 2	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	2	
		Clock Descriptor 3	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	3	
		Direct clock Descriptor			none
	Clock Id			0x07	Source output to TCLKC
	Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
	Indirect Clock Descriptors Count(m)			0x04	
	Direct Clock Descriptors Count(n)			0x00	
		Indirect clock Descriptor			
		Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	0	
		Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	1	
		Clock Descriptor 2	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	2	
		Clock Descriptor 3	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source
			Dependent ClockId	3	
		Direct clock Descriptor			none
	Clock Id			0x08	Receiver input from TCLKB
	Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
	Indirect Clock Descriptors Count(m)			0x02	
	Direct Clock Descriptors Count(n)			0x00	
		Indirect clock Descriptor			

Type 2D - Clock Configuration Record					
		Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
			Dependent ClockId	4	4
		Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
			Dependent ClockId	5	
		Direct clock Descriptor			none
	Clock Id			0x09	Receiver input from TCLKD
	Clock Control			0x01	7:1 0h (reserved) [0] 1b = Activated by Application
	Indirect Clock Descriptors Count(m)			0x02	
	Direct Clock Descriptors Count(n)			0x00	
	Indirect clock Descriptor				
		Clock Descriptor 0	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
			Dependent ClockId	4	
		Clock Descriptor 1	Features	0x02	7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver
			Dependent ClockId	5	
		Direct clock Descriptor			none

4.4.4 IPMI Over LAN

On the Ethernet Switch, the IPMI Over LAN functionality is provided via an OpenIPMI utility named IPMILAN. The IPMILAN daemon allows an IPMI system interface using the OpenIPMI device driver to be accessed using the IPMI 1.5 or 2.0 LAN protocol. The IPMILAN utility establishes the session and provides a bridge with the IPMC to execute the requested commands.

The OpenIPMI IPMI utility has the following known features/limitations:

- All the commands supported by the IPMC are working (since they are forwarded from the IPMILAN utility to the IPMC via the host interface KCS).
- All the minimum commands to establish a session are supported.
- Session commands with invalid parameters may be unsupported (depending on the error).
- All the commands related to Channels are not supported.

- All the commands related to Users are not supported.
- IOL and Users can be configured via a configuration file only.
- Some commands related to Session are not supported.
- SOL is not implemented.
- IOL 1.5 and 2.0 session establishment supported.
- RMCP supported algorithms are

  Authentication: None, Straight Password

  There is no concept of integrity and confidentiality in RMCP (IOL 1.5).
- RMCP+ supported algorithms are (all the mandatory one):

  Authentication: RAKP-none, RAKP-HMAC-SHA1

  Integrity: None, HMAC-SHA1-96

  Confidentiality: None, AES-CBC-128
- Upgrading a firmware using IOL 2.0 or 1.5 is working.
- 64 simultaneous sessions supported.

Since not all the IOL, Session, Channel, User commands are supported, this IMPLEMENTATION IS NOT IOL 1.5 NOR 2.0 COMPLIANT, but offer a nice path for other commands supported by the IPMC.

The features of IPMI over LAN offers by Open IPMI is provided as is, Kontron doesn't support, enhance or provide maintenance for any of the Open IPMI software module.

4.5 Built-In MMCs

4.5.1 Supported Commands

The table below lists the IPMI commands supported by the built in MMC (FRU2/3/4). This table is identical as the one provided by AMC.0 and PICMG 3.0. The last column states the Kontron support for the specific command.

Table 4-47:IPM Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
IPM Device "Global" Commands				M	M	
Get Device ID	17.1	App	01h	M	M	Yes
Cold Reset	17.2	App	02h	O	O	Yes
Warm Reset	17.3	App	03h	O	O	No
Get Self Test Results	17.4	App	04h	M	M	Yes
Manufacturing Test On	17.5	App	05h	O	O	Yes
Set ACPI Power State	17.6	App	06h	O	O	Yes
Get ACPI Power State	17.7	App	07h	O	O	Yes
Get Device GUID	17.8	App	08h	O	O	No
Broadcast "Get Device ID"[1]	17.9	App	01h	O/M	M	Yes

Table 4-48:Watchdog Timer Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
BMC Watchdog Timer Commands				M	M	
Reset Watchdog Timer	21.5	App	22h	M	M	Yes
Set Watchdog Timer	21.6	App	24h	M	M	Yes
Get Watchdog Timer	21.7	App	25h	M	M	Yes

Table 4-49:Device Messaging Supported Commands for built in MMC

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
BMC Device and Messaging Commands[5]				M	O	
Set BMC Global Enables	18.1	App	2Eh	M	O/M	Yes
Get BMC Global Enables	18.2	App	2Fh	M	O/M	Yes
Clear Message Flags	18.3	App	30h	M	O/M	Yes
Get Message Flags	18.4	App	31h	M	O/M	Yes
Enable Message Channel Receive	18.5	App	32h	O	O	Yes
Get Message	18.6	App	33h	M	O/M	Yes
Send Message	18.7	App	34h	M	M	Yes
Read Event Message Buffer	18.8	App	35h	O	O	Yes
Get BT Interface Capabilities	18.9	App	36h	M	O/M	Yes
Master Write-Read	18.10	App	52h	M	O/M	No
Get System GUID	18.13	App	37h	O	O	No
Get Channel Authentication Capabilities	18.12	App	38h	O	O	No
Get Session Challenge	18.14	App	39h	O	O	No
Activate Session	18.15	App	3Ah	O	O	No
Set Session Privilege Level	18.16	App	3Bh	O	O	No
Close Session	18.17	App	3Ch	O	O	No
Get Session Info	18.18	App	3Dh	O	O	No
Get AuthCode	18.19	App	3Fh	O	O	No
Set Channel Access	18.20	App	40h	O	O	No
Get Channel Access	18.21	App	41h	O	O	No
Get Channel Info	18.22	App	42h	O	O	No
Set User Access	18.23	App	43h	O	O	No
Get User Access	18.24	App	44h	O	O	No
Set User Name	18.25	App	45h	O	O	No
Get User Name	18.26	App	46h	O	O	No
Set User Password	18.27	App	47h	O	O	No
Activate Payload	24.1 (IPMI 2.0)	App	48h	O	O	Yes
Deactivate Payload	24.2 (IPMI 2.0)	App	49h	O	O	Yes
Get Payload Activation Status	24.4 (IPMI 2.0)	App	4Ah	O	O	Yes
Get Payload Instance Info	24.5 (IPMI 2.0)	App	4Bh	O	O	Yes
Set User Payload Access	24.6 (IPMI 2.0)	App	4Ch	O	O	Yes
Get User Payload Access	24.7 (IPMI 2.0)	App	4Dh	O	O	Yes

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Get Channel Payload Support	24.8 (IPMI 2.0)	App	4Eh	0	0	Yes
Get Channel Payload Version	24.9 (IPMI 2.0)	App	4Fh	0	0	Yes
Get Channel OEM Payload Info	24.10 (IPMI 2.0)	App	50h	0	0	No
Master Write-Read	18.10	App	52h	M	0/M	Yes
Get Channel Cipher Suites	22.15 (IPMI 2.0)	App	54h	0	0	Yes
Suspend / Resume Payload Encryption	24.3 (IPMI 2.0)	App	55h	0	0	Yes
Set Channel Security Keys	22.25 (IPMI 2.0)	App	56h	0	0	No
Get System Interface Capabilities	22.9 (IPMI 2.0)	App	57h	0	0	Yes

Table 4-50:Chassis Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Chassis Device Commands				0	0	
Get Chassis Capabilities	22.1	Chassis	00h	M	0	Yes
Get Chassis Status	22.2	Chassis	01h	0/M	0	Yes
Chassis Control	22.3	Chassis	02h	0/M	0	Yes
Chassis Reset	22.4	Chassis	03h	0	0	No
Chassis Identify	22.5	Chassis	04h	0	0	No
Set Chassis Capabilities	22.6	Chassis	05h	0	0	No
Set Power Restore Policy	22.7	Chassis	06h	0	0	No
Get System Restart Cause	22.9	Chassis	07h	0	0	No
Get System Restart Cause	22.10	Chassis	08h	0	0	No
Get System Restart Cause	22.11	Chassis	09h	0	0	No
Get POH Counter	22.12	Chassis	0Fh	0	0	No

Table 4-51:Event Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Event Commands				M	M	
Set Event Receiver	23.1	S/E	01h	M	M	Yes
Get Event Receiver	23.2	S/E	02h	M	M	Yes
Platform Event (a.k.a. “Event Message”)	23.3	S/E	03h	M	M	Yes

Table 4-52:PEF and Alerting Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
PEF and Alerting Commands				O	O	
Get PEF Capabilities	24.1	S/E	10h	M	M	No
Arm PEF Postpone Timer	24.2	S/E	11h	M	M	No
Set PEF Configuration Parameters	24.3	S/E	12h	M	M	No
Get PEF Configuration Parameters	24.4	S/E	13h	M	M	No
Set Last Processed Event ID	24.5	S/E	14h	M	M	No
Get Last Processed Event ID	24.6	S/E	15h	M	M	No
Alert Immediate	24.7	S/E	16h	O	O	No
PET Acknowledge	24.8	S/E	17h	O	O	No

Table 4-53:Sensor Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Sensor Device Commands				O	M	
Get Device SDR Info	29.2	S/E	20h	O	M	Yes
Get Device SDR	29.3	S/E	21h	O	M	Yes
Reserve Device SDR Repository	29.4	S/E	22h	O	M	Yes
Get Sensor Reading Factors	29.5	S/E	23h	O	M	No
Set Sensor Hysteresis	29.6	S/E	24h	O	O	Yes
Get Sensor Hysteresis	29.7	S/E	25h	O	O	Yes
Set Sensor Threshold	29.8	S/E	26h	O	O	Yes
Get Sensor Threshold	29.9	S/E	27h	O	O	Yes
Set Sensor Event Enable	29.10	S/E	28h	O	O	Yes

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Get Sensor Event Enable	29.11	S/E	29h	O	O	Yes
Re-arm Sensor Events	29.12	S/E	2Ah	O	O	No
Get Sensor Event Status	29.13	S/E	2Bh	O	O	No
Get Sensor Reading	29.14	S/E	2Dh	M	M	Yes
Set Sensor Type	29.15	S/E	2Eh	O	O	No
Get Sensor Type	29.16	S/E	2Fh	O	O	No

Table 4-54:FRU Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
FRU Device Commands				M	M	
Get FRU Inventory Area Info	28.1	Storage	10h	M	M	Yes
Read FRU Data	28.2	Storage	11h	M	M	Yes
Write FRU Data	28.3	Storage	12h	M	M	Yes

Table 4-55:SDR Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
SDR Device Commands				M	O	
Get SDR Repository Info	27.9	Storage	20h	M	M	No
Get SDR Repository Allocation Info	27.10	Storage	21h	O	O	No
Reserve SDR Repository	27.11	Storage	22h	M	M	No
Get SDR	27.12	Storage	23h	M	M	No
Add SDR	27.13	Storage	24h	M	O/M	No
Partial Add SDR	27.14	Storage	25h	M	O/M	No
Delete SDR	27.15	Storage	26h	O	O	No
Clear SDR Repository	27.16	Storage	27h	M	O/M	No
Get SDR Repository Time	27.17	Storage	28h	O/M	O/M	No
Set SDR Repository Time	27.18	Storage	29h	O/M	O/M	No
Enter SDR Repository Update Mode	27.19	Storage	2Ah	O	O	No
Exit SDR Repository Update Mode	27.20	Storage	2Bh	M	M	No
Run Initialization Agent	27.21	Storage	2Ch	O	O	No

Table 4-56:SEL Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
SEL Device Commands				M	O	
Get SEL Info	25.2	Storage	40h	M	M	No
Get SEL Allocation Info	25.3	Storage	41h	O	O	No
Reserve SEL	25.4	Storage	42h	O	O	No
Get SEL Entry	25.5	Storage	43h	M	M	No
Add SEL Entry	25.6	Storage	44h	M	M	No
Partial Add SEL Entry	25.7	Storage	45h	M	M	No
Delete SEL Entry	25.8	Storage	46h	O	O	No
Clear SEL	25.9	Storage	47h	M	M	No
Get SEL Time	25.10	Storage	48h	M	M	No
Set SEL Time	25.11	Storage	49h	M	M	No
Get Auxiliary Log Status	25.12	Storage	5Ah	O	O	No
Set Auxiliary Log Status	25.13	Storage	5Bh	O	O	No

Table 4-57:LAN Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
LAN Device Commands				O	O	
Set LAN Configuration Parameters	19.1	Transport	01h	O/M	O/M	Yes
Get LAN Configuration Parameters	19.2	Transport	02h	O/M	O/M	Yes
Suspend BMC ARPs	19.3	Transport	03h	O/M	O/M	Yes
Get IP/UDP/RMCP Statistics	19.4	Transport	04h	O	O	Yes

Table 4-58:Serial/Modem Device Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Serial/Modem Device Commands				O	O	
Set Serial/Modem Configuration	20.1	Transport	10h	O/M	O/M	No
Get Serial/Modem Configuration	20.2	Transport	11h	O/M	O/M	No
Set Serial/Modem Mux	20.3	Transport	12h	O	O	No
Get TAP Response Codes	20.4	Transport	13h	O	O	No

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Set PPP UDP Proxy Transmit Data	20.5	Transport	14h	O	O	No
Get PPP UDP Proxy Transmit Data	20.6	Transport	15h	O	O	No
Send PPP UDP Proxy Packet	20.7	Transport	16h	O	O	No
Get PPP UDP Proxy Receive Data	20.8	Transport	17h	O	O	No
Serial/Modem Connection Active	20.9	Transport	18h	O/M	O/M	No
Callback	20.10	Transport	19h	O	O	No
Set User Callback Options	20.11	Transport	1Ah	O	O	No
Get User Callback Options	20.12	Transport	1Bh	O	O	No

Table 4-59:Bridge (ICMB) Management Supported Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Bridge Management Commands (ICMB)[2]				O	O	
Get Bridge State	[ICMB]	Bridge	00h	O/M	O	No
Set Bridge State	[ICMB]	Bridge	01h	O/M	O	No
Get ICMB Address	[ICMB]	Bridge	02h	O/M	O	No
Set ICMB Address	[ICMB]	Bridge	03h	O/M	O	No
Set Bridge Proxy Address	[ICMB]	Bridge	04h	O/M	O	No
Get Bridge Statistics	[ICMB]	Bridge	05h	O/M	O	No
Get ICMB Capabilities	[ICMB]	Bridge	06h	O/M	O	No
Clear Bridge Statistics	[ICMB]	Bridge	08h	O/M	O	No
Get Bridge Proxy Address	[ICMB]	Bridge	09h	O/M	O	No
Get ICMB Connector Info	[ICMB]	Bridge	0Ah	O/M	O	No
Get ICMB Connection ID	[ICMB]	Bridge	0Bh	O/M	O	No
Send ICMB Connection ID	[ICMB]	Bridge	0Ch	O/M	O	No

Table 4-60:Discovery (ICMB) Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Discovery Commands (ICMB)[2]				0	0	
Prepare For Discovery	[ICMB]	Bridge	10h	O/M	0	No
Get Addresses	[ICMB]	Bridge	11h	O/M	0	No
Set Discovered	[ICMB]	Bridge	12h	O/M	0	No
Get Chassis Device ID	[ICMB]	Bridge	13h	O/M	0	No
Set Chassis Device ID	[ICMB]	Bridge	14h	O/M	0	No

Table 4-61:Bridging (ICMB) Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Bridging Commands (ICMB)[2]				0	0	
Bridge Request	[ICMB]	Bridge	20h	O/M	0	No
Bridge Message	[ICMB]	Bridge	21h	O/M	0	No

Table 4-62:Event (ICMB) Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Event Commands (ICMB) [2]				0	0	
Get Event Count	[ICMB]	Bridge	30h	O/M	0	No
Set Event Destination	[ICMB]	Bridge	31h	O/M	0	No
Set Event Reception State	[ICMB]	Bridge	32h	O/M	0	No
Send ICMB Event Message	[ICMB]	Bridge	33h	O/M	0	No
Get Event Destination	[ICMB]	Bridge	34h	O/M	0	No
Get Event Reception State	[ICMB]	Bridge	35h	O/M	0	No

Table 4-63:OEM for Bridge NetFn (ICMB) Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
OEM Commands for Bridge NetFn				0	0	
OEM Commands	[ICMB]	Bridge	C0h-FEh	O/M	0	No

Table 4-64:Other Bridge (ICMB) Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
Other Bridge Commands				O	O	
Error Report	[ICMB]	Bridge	FFh	O/M	O	No

Table 4-65:PICMG 3.0 Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
AdvancedTCA	PICMG® 3.0 Table				M	
Get PICMG Properties	3-9	PICMG	00h		M	Yes
Get Address Info	3-8	PICMG	01h		M	N/A
Get Shelf Address Info	3-13	PICMG	02h		O	N/A
Set Shelf Address Info	3-14	PICMG	03h		O	N/A
FRU Control	3-22	PICMG	04h		M	Yes
Get FRU LED Properties	3-24	PICMG	05h		M	Yes
Get LED Color Capabilities	3-25	PICMG	06h		M	Yes
Set FRU LED State	3-26	PICMG	07h		M	Yes
Get FRU LED State	3-27	PICMG	08h		M	Yes
Set IPMB State	3-51	PICMG	09h		M	N/A
Set FRU Activation Policy	3-17	PICMG	0Ah		M	N/A
Get FRU Activation Policy	3-18	PICMG	0Bh		M	N/A
Set FRU Activation	3-16	PICMG	0Ch		M	N/A
Get Device Locator Record ID	3-29	PICMG	0Dh		M	N/A
Set Port State	3-41	PICMG	0Eh		O/M	N/A
Get Port State	3-42	PICMG	0Fh		O/M	N/A
Compute Power Properties	3-60	PICMG	10h		M	N/A
Set Power Level	3-62	PICMG	11h		M	N/A
Get Power Level	3-61	PICMG	12h		M	N/A
Renegotiate Power	3-66	PICMG	13h		O	N/A
Get Fan Speed Properties	3-63	PICMG	14h		M	N/A
Set Fan Level	3-65	PICMG	15h		O/M	N/A
Get Fan Level	3-64	PICMG	16h		O/M	N/A
Bused Resource	3-44	PICMG	17h		O/M	N/A
Get IPMB Link Info	3-49	PICMG	18h		O/M	N/A
FRU Control Capabilities	3-24	PICMG	1Eh		M	Yes

Table 4-66:AMC.0 Commands for MMC built in

	IPMI Spec. section	NetFn	CMD	IPMI BMC req.	Carrier IPMC req.	Kontron support on MMC
AMC	AMC.0 Table					
Set AMC Port State	Table 3-27	PICMG	19h		O/M	Yes
Get AMC Port State	Table 3-28	PICMG	1Ah		O/M	Yes
Set Clock State	Table 3-44	PICMG	2Ch		O/M	Yes
Get Clock State	Table 3-45	PICMG	2Dh		O/M	Yes

4.5.2 Sensor Data Records

4.5.2.1 MMC Built in (FRU2/FRU3/FRU4) sensors

Built in MMCs have the capability of supporting any of the IPMI or OEM sensor types (similar to an IPM Controller on an AdvancedTCA Board). The MMC's sensors on IPMB-L are visible to the Shelf Manager through the Front Blade Unit Carrier IPMC over IPMB-0. Since the IPMC must present unique sensor numbers and sensor LUN over IPMB-0, it is necessary for the Front Blade Unit pseudo Carrier IPMC to translate the MMC's sensor number and sensor LUN to Carrier IPMC-wide unique numbers. The Unit Carrier IPMC device SDR repository holds a combination of its own SDRs and SDRs from the built in Module's MMC. The Unit Carrier IPMC adds the MMC's SDRs into its SDR Repository after Management Power (MP) has been enabled to the built in MMC.

Conversely, the MMC's SDRs are removed from the Unit Carrier IPMC's SDR repository after Management Power (MP) has been removed from a MMC. As mentioned previously, when the Carrier IPMC adds the MMC's SDRs into its SDR repository, it needs to ensure that the sensor number and sensor LUN assigned are unique to the Unit Carrier IPMC.

This is the list of FRU2/FRU3/FRU4 sensors.

Table 4-67:MMC Built in (FRU2/FRU3/FRU4) sensors

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event trigger)
0	BX:ModuleHotSwap	AMC.0 Module Hot Swap Sensor Sensor type = F2h PICMG Hot Swap, Event Reading type code = 6Fh Sensor specific -see AMC.0 R2.0 section 3.6.6 for event trigger and sensor definition
1	BX:FRU Agent	Module Data agent that verify FRU Data validity (checksum/E-key/etc) Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0AFh Generic Discrete, offset 6,8 are used, see table sws-10-1138 for event trigger information
2	BX:IPMBL State	IPMB-L fault detection sensor. Sensor type = C3h OEM (Kontron IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, see table sws-10-1139 for event trigger information
3	BX:MMC Stor Err	Management sub-system health: non volatile memory error. Sensor type = 28h Management Subsystem Health Event Reading type code = 6Fh Sensor specific, only offset 1 is used, offset 1: event trigger, IPMC Non volatile memory error see IPMI v1.5 table 36.3, Sensor type code 28h for sensor definition
4	BX:MMC Reboot	Management Controller reboot detection Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, Normal Condition (IPMC is running) offset 1: event trigger, Management Controller has reboot see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition
5	BX:Ver change	Management Controller firmware upgrade detection Sensor type = 2Bh Version Change Event Reading type code = 6Fh Sensor specific, only offset 1 is used, offset 1/event data 2: 00h (unspecified): event trigger, A sensor configuration has changed offset 1/event data 2: 02h (Firm. Rev.): event trigger, A Firmware Upgrade has been done see IPMI v1.5 table 36.3, Sensor type code 2Bh (Version Change) for sensor definition
6	BX:Temp CPU	Temperature of CPU Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Non-Critical event: 65 deg C. Upper Critical event: 75 deg C. Upper Non-Recoverable: 125 deg C. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event trigger)
7	BX:Temp FI/BI	Fabric/Base interfaces Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 95°C: After Thermal Analysis. -Upper Critical event: 105°C: After Thermal Analysis. -Upper Non-Recoverable: 120°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
8	BX:Temp Vcore	CPU Vcore Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 95°C: After Thermal Analysis. -Upper Critical event: 105°C: After Thermal Analysis. -Upper Non-Recoverable:120°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
9	BX:Temp MCH	MCH Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 85°C: After Thermal Analysis. -Upper Critical event: 95°C: After Thermal Analysis. -Upper Non-Recoverable: 110°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
10	BX:Temp DIMM0	Memory DIMM Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 75°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 100°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
11	B2:Temp DIMM1 (FRU2/CPU0 Engine Only)	Memory Second DIMM Temperature (only available on CPU0), Sensor Type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 75°C: After Thermal Analysis. -Upper Critical event: 85°C: After Thermal Analysis. -Upper Non-Recoverable: 100°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event trigger)
12	B2:Temp FrontEth (FRU2/CPU0 Engine Only)	Front Panel Ethernet Temperature, Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 95°C: After Thermal Analysis. -Upper Critical event: 105°C: After Thermal Analysis. -Upper Non-Recoverable: 115°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
13	B2:Temp LSI SAS (FRU2/CPU0 Engine Only)	LSI SAS Controller Temperature Sensor type = 01h temperature, Event Reading type code = 01h threshold base event base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event -Upper Non-Critical event: 85°C: After Thermal Analysis. -Upper Critical event: 95°C: After Thermal Analysis. -Upper Non-Recoverable: 110°C: After Thermal Analysis. -Hysteresis: 2 deg C ** All value can be adjusted after thermal analysis
14	BX:Vcc VTT DDR	Voltage on the memory (1.05) Sensor type = 02h Voltage, Event Reading type code = 01h threshold base event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.11v (10%) Lower Critical Event: 0.99v (10%) Hysteresis: 0.016v (1.5%)
15	BX:VCORE	CPU Core Voltage Sensor type = 02h Voltage, Event Reading type code = 01h threshold base event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical Event:1.03*Vmax(vid) Lower Critical Event: 0.97Vmin(vid) Hysteresis: 0.015v (1.5%)
16	BX:Vcc +1.5V SUS	Voltage on 1.5v suspend (management) board power supply Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.58v (5%) Lower Critical Event: 1.42v (5%) Hysteresis: 0.025v (1.5%)
17	BX:CPU VCCA	Voltage on CPU VCCA Sensor type = 02h Voltage, Event Reading type code = 01h threshold base Event trigger base on following thershold, see IPMI v1.5 section 29.13.3 for threshold base event Upper Critical event: 1.58v (5%) Lower Critical Event: 1.42v (5%) Hysteresis: 0.025v (1.5%)
18	BX:CPU Reset	Board reset type and sources Sensor type = CFh OEM (Kontron Reset Sensor), Event Reading type code = 03h Digital Discrete offset 0,1 are used, see table sws-10-1177 for event trigger information

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event trigger)
19	BX:Boot Error	CPU Boot Error Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, only offset 0 is used, offset 0: event trigger - No bootable Media see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition
20	BX:POST Value	Show current postcode value. No event generated by this sensor. Sensor type = C6h OEM (Kontron POST value sensor), Event Reading type code = 6Fh Sensor specific, offset 0 to 7 and 14 are used, see table sws-10-1140 for event trigger information
21	BX:POST Error	CPU Power On Self Test Error Sensor type = 0Fh System Firmware Progress Event Reading type code = 6Fh Sensor specific, only offset 0 is used, offset 0/event data 2: 00h (unspecified): event trigger, CMOS Setting Wrong, CMOS checksum bad CMOS Date/Time not set offset 0/event data 2: 01h : event trigger, No system memory is physically installed in the system offset 0/event data 2: 02h : event trigger, No usable system memory offset 0/event data 2: 03h : event trigger, Unrecoverable hard-disk/ATAPI/IDE device failure offset 0/event data 2: 04h : Unrecoverable system-board failure offset 0/event data 2: 0Dh :CPU speed matching failure see IPMI v1.5 table 36.3, Sensor type code 0Fh (System Firmware Progress) for sensor definition
22	BX:Critical Int	Critical Interrupt Sensor type = 13h Critical Interrupt, Event Reading type code = 6Fh Critical Interrupt offset 0,4,5 are used, offset 0: event trigger, Front Panel NMI / Diagnostic Interrupt offset 4: event trigger, PCI PERR offset 5: event trigger, PCI SERR see IPMI v1.5 table 36.3, Sensor type code 13h for sensor definition
23	BX:Memory	Memory Status Sensor type = 0Ch System Firmware Progress Event Reading type code = 6Fh Sensor specific, offset 0,1,3,4,5 are used, offset 0: event trigger, Memory Correctable ECC offset 1: event trigger, Memory Uncorrectable ECC offset 3: event trigger, Memory Scrub Failed (stuck bit) offset 4: event trigger, Memory Device Disabled offset 5: event trigger, Memory Correctable ECC / Memory logging limit Reach see IPMI v1.5 table 36.3, Sensor type code 0Ch for sensor definition
24	BX:Cmos Mem Size	POST Memory Resize, Indicates if CMOS memory size if wrong Sensor type = 0Eh Critical Interrupt, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, normal condition, no resize offset 1: event trigger, CMOS memory size if wrong see IPMI v1.5 table 36.3, Sensor type code 0Eh for sensor definition

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event trigger)
25	BX:PrebootPasswd	Platform Security Violation Attempt Sensor type = 06h Platform Security Violation Attempt, Event Reading type code = 6Fh Sensor Specific offset 1 and 4 are used, offset 1: event trigger, Pre-Boot Password Violation, User password (BIOS password check location is critical) offset 4: event trigger, Other Pre-Boot Password Violation (BIOS password check location is not critical) see IPMI v1.5 table 36.3, Sensor type code 06h for sensor definition
26	BX:CPU Status	CPU Status Sensor type = 07h Processor, Event Reading type code = 6Fh Sensor Specific offset 0,1,5 are used, offset 0: event trigger, CPU IERR offset 1: event trigger, CPU Thermal Trip offset 5: event trigger, Configuration Error see IPMI v1.5 table 36.3, Sensor type code 07h for sensor definition
27	BX:FWH 0 Error	Firmware Hub Boot Error. Specify if it was unable to boot from the BIOS on the Firmware Hub Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, only offset 3 is used, offset 3: event trigger - Invalid boot sector see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition
28	BX:FWH 1 Error	Firmware Hub Boot Error, Specify if it was unable to boot from the BIOS on the Firmware Hub Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, only offset 3 is used, offset 3: event trigger - Invalid boot sector see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition
29	BX:ACPI State	Advance Configuration and Power Interface State Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, offset 0 to15 are used, see IPMI v1.5 table 36.3, Sensor type code 22h (Boot Error) for sensor definition and event trigger
30	BX:IPMI Watchdog	IPMI watchdog Sensor type = 23h Watchdog 2, Event Reading type code = 6Fh Sensor specific, offset 0,1,2,3,8 are used, see IPMI v1.5 table 36.3, Sensor type code 23h (Watchdog 2) for sensor definition and event trigger
31	BX:Health Error	General health status, Aggregation of critical sensor This list is flexible and could be adjust based on customer requirements. Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, offset 0: event trigger, no critical sensors is asserted offset 1: event trigger, one or multiple critical sensors are asserted see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition
32	BX:MMC FwUp	Kontron OEM MMC firmware upgrade Status Sensor type = C7h OEM (Management Controller firmware upgrade Status) Event Reading type code = 6Fh Sensor specific, offset 0,1 are used,

IPMI sensor ID	Sensor Name	Description (Sensor Type, Event trigger)
33	BX:Temp Pre SPD0	Internal Temperature sensor presence on DIMM (sensor 10), if absent on board diode is used Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : no event generated (Entity Present), offset 1 event trigger: no event generated (Entity Absent), see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition
34	B2:Temp Pre SPD1 (FRU2/CPU0 Engine Only)	Internal Temperature sensor presence on DIMM1 (sensor 11), if absent on board diode is used Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, offset 0 event trigger : no event generated (Entity Present), offset 1 event trigger: no event generated (Entity Absent), see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition
35	BX:IPMI Info-1	Internal IPMC firmware diagnostic event trigger: internal error condition
36	BX:IPMI Info-2	Internal IPMC firmware diagnostic event trigger: internal error condition

4.5.2.2 MMC Built in sensors aggregation for health sensor

The following table shows the sensors involved in the health sensor aggregation. This sensor is part of table "MMC built in Sensor" SWS-10-1051 sensor name "BX:Health Error".

Table 4-68:MMC Sensor Names

Sensor Name
BX:Temp CPU
BX:Temp FBI
BX:Temp Vcore
BX:Temp MCH
BX:Temp FrontEth(Cpu0 Engine Only)
BX:Temp LSI SAS (Cpu0 Engine Only)
BX:Vcc VTT DDR
BX:VCORE
BX:Vcc VTT DDR
BX:Vcc +1.5V SUS
BX:CPU VCCA
BX:CPU Reset
BX:POST Value
BX:POST Error
BX:Cmos Mem Size

Sensor Name
BX:CPU Critical Int
BX:IPMI Watchdog
BX:FWH 0 Error
BX:FWH 1 Error

4.5.3 FRU Information

Table 4-69:CPU0 Engine - Board Information Area

CPU0 Engine – Board Information Area	
Field Description	Value (hex)
Format Version	0x01
Board Area Length	*Calculated
Language code	0x19
Manufacturing Date / Time	*Based on mfg. date
Board Manufacturer type/length	*Calculated
Board Manufacturer	"KONTRON "
Board Name type/length	*Calculated
Board Name	“AT8030 CPU0 Engine”
Board Serial Number type/length	C0
Board Serial Number	null
Board Part Number type/length	C0
Board Part Number	null
FRU File ID type/length	0x00
FRU File ID	null
No more fields	0xC1
Padding	0x00
Board Area Checksum	*Calculated

Table 4-70:CPU0 Engine - Product Information Area

CPU0 Engine – Product Information Area	
Field Description	Value (hex)
Format Version	0x01
Board Area Length	*Calculated
Language code	0x19
Board Manufacturer type/length	*Calculated

CPU0 Engine – Product Information Area	
Board Manufacturer	"KONTRON "
Board Name type/length	*Calculated
Board Name	“AT8030 CPU0 Engine”
Board Serial Number type/length	C0
Board Serial Number	null
Board Part Number type/length	C0
Board Part Number	null
FRU File ID type/length	*Calculated
FRU File ID	“FRU5006-CPU0-ZZ”
No more fields	0xC1
Padding	0x00
Board Area Checksum	*Calculated

4.5.4 MMC (FRU3/FRU4) FRU Data Information

Table 4-71:CPU1/CPU2 Engine - Board Information Area

CPU1/CPU2 Engine – Board Information Area	
Field Description	Value (hex)
Format Version	0x01
Board Area Length	*Calculated
Language code	0x19
Manufacturing Date / Time	*Based on mfg. date
Board Manufacturer type/length	*Calculated
Board Manufacturer	"KONTRON "
Board Name type/length	*Calculated
Board Name	“AT8030 CPUX Engine”
Board Serial Number type/length	C0
Board Serial Number	null
Board Part Number type/length	C0
Board Part Number	null
FRU File ID type/length	0x00
FRU File ID	null
No more fields	0xC1
Padding	0x00
Board Area Checksum	*Calculated

Table 4-72:CPU1/CPU2 Engine - Product Information Area

CPU1/CPU2 Engine – Product Information Area	
Field Description	Value (hex)
Format Version	0x01
Product Area Length	*Calculated
Language code	0x19
Product Manufacturer type/length	*Calculated
Product Manufacturer	"KONTRON "
Product Name type/ length	*Calculated
Product Name	“AT8030”
Product Part Number type/length	*Calculated
Product Part Number	“AT8030 CPUX Engine”
Product Version type/ length	*Calculated
Product Version	C0
Product Serial Number type/length	null
Product Serial Number	C0
Product Part Number type/length	null
Asset Tag type/length	C0
Asset Tag	null
FRU File ID type/length	*Calculated
FRU File ID	“FRU5006-ZZ"
No more fields	0xC1
Padding	0x00
Board Area Checksum	*Calculated

4.5.5 IPMI Over LAN

As mentioned earlier, the LAN interface specifications defines how IPMI messages can be sent to and from the MMCs encapsulated in RMCP (Remote Management Control Protocol) packets datagrams.

The LAN interface is a multisession interface compared to the KCS/IPMB interfaces that are session-less interface. Also, the LAN interface is considered as a not secure interface compared to the KCS/IPMB. Authentication and privileges level has been added for the commands that are critical to the system. With IOL 2.0, the concept of data integrity and confidentiality has been also added to offer full security.

4.5.5.1 IPMI Sessions, Authentications and Users

With the addition of LAN interface, the concept of sessions has been introduced in IPMI. Authenticated IPMI communication to the MC is accomplished by establishing a session. Once established, a session ID identifies a session. The Session ID may be thought as a handle that identifies a connection between a given remote user and the IPMC.

Session-less connections: IPMB, KCS, etc.

Multisession connections: LAN, etc...

Four different sessions is available at the same time for multisession connections.

For more information about session activation, see IPMI specification 2.0 Markup 2, May 2005 section 6.12.7.

Inactive sessions are closed after 1 minute as per IPMI specification Markup 2, May 2005 section 6.12.15. The session must be re-authenticated to be restored.

4.5.5.1.1 Authentication, Integrity and Confidentiality

For each session type (RMCP and RMCP+), some algorithms types are available.

RMCP supported algorithms are

Authentication: None, Straight Password

There is no concept of integrity and confidentiality in RMCP (IOL 1.5).

RMCP+ supported algorithms are (all the mandatory one):

- Authentication: RAKP-none, RAKP-HMAC-SHA1
- Integrity: None, HMAC-SHA1-96
- Confidentiality: None, AES-CBC-128

4.5.5.1.2 Users

USER 1: The IPMI specification 2.0 Markup 2, May 2005 mention that a "NULL" user must be present. This is in fact when no user (or NULL) is provided. The specification provide a way to access the "User 1" but don't define is initial privileges. The selected privileges are the USER one, forbidding to upgrade the IPMC. For example, in order to upgrade the IPMC over LAN, an external user needs to:

- Connect to the IPMC using the IPMB interface or the System Interface
- Creates an account and gives the Administrator privileges.
- Then, using the LAN, it is possible to upgrade the IPMC.

IPMI specification 2.0 Markup 2, May 2005 do not specify the number of users but writes the following (section 6.9):

- All authenticated channels are required to support at least one user (User ID 1).
- Usernames may be fixed or configurable, or a combination of both, at the choice of the implementation.
- If an implementation supports only one user with a fixed user name, then the fixed user name must be null (all zeros).
- Support for configuring user passwords for all User IDs is required.
- Support for setting per-user privilege limits is optional. If the Set User Access command is not supported, the privilege limits for the channel are used for all users.

Chosen implementation: 5 users including the USER 1.

Table 4-73:Front Blade Unit Default User for CPU session

User ID	Username	Password	Can be modified	Privileges
0	Reserved	Reserved	Reserved	Reserved
1	NULL	Empty	No	User
2	"admin"	"admin"	Yes	Administrator
3	Empty	Empty	Empty	Empty
4	Empty	Empty	Empty	Empty
5	Empty	Empty	Empty	Empty

4.5.5.2 IPMI "Send Message"

IOL is an interface like the KCS and the IPMB. The implementation supports the send message and the message bridging from one interface to the other.

See IPMI specification 2.0 section 6.13 named Message Bridging for all the details.

4.5.5.3 LAN Parameters

The IPMI specifies 2 commands to configure the LAN interface of a specific channel (Set and Get LAN Parameters). For more details about the bytes and bits defined here, refer to IPMI specification 2.0 Markup 2, May 2005 section 23.2.

To clarify the document, the undefined bits and bytes are not showed in the following table.

Table 4-74:LAN Parameters

Parameter	#	Byte/ Bit	Default Value	Default Description
Set In Progress (Volatile)	0	1 / 1:0	00b	Set complete
		Notes: Rollback is implemented as defined by the specification.		
Auth Type Support (read only)	1	1 / 5:0	010001h	None and Straight password / key supported

Parameter	#	Byte/ Bit	Default Value	Default Description
Auth Type Enable	2	1 / 5:0	000000h	Callback: No enable
		1 / 5:0	010000h	User level: Straight password / key supported
		2 / 5:0	010000h	Operator level: Straight password / key supported
		3 / 5:0	010001h	Admin level: None and Straight password / key supported
		4 / 5:0	Uns. level	Unsupported level
IP Address	3	01:04	0.0.0.0	0.0.0.0
IP Address source	4	1 / 3:0	01h	Fixed to static address. No other setting planned to be supported.
MAC Address	5	01:06	Chip MAC	Set to chip MAC in production
Subnet Mask	6	01:04	0.0.0.0	0.0.0.0
Ipv4 Header Parameters	7	1	40h	Time-to-live
		2 / 7:5	010b	Flags fixed to don't fragment
		3 / 7:5	000b	Precedence fixed to 000b
		3 / 4:1	1000b	Type of service fixed to minimize delay
Primary RMCP port number	8	1	26Fh	26Fh
Secondary RMCP port number	9	1	Unsupported pot 298h	
BMC-generated ARP control	10	01-janv	1	Enable BMC-generated ARP responses
		1/0	1	Enable BMC-generated Gratuitous ARPs
Gratuitous ARP interval	11	1	7	8 Seconds
VLAN ID	20	0/1	0	VLAN ID data
VLAN PRIORITY	21	1	0	VLAN Priority data

4.5.5.3.1 VLAN

Configuration options have been added to support IEEE 802.1q VLAN (virtual LAN) headers for IPMI over IP sessions on IEEE 802.3 Ethernet. VLAN works with VLAN-aware routers and switches to allow a physical network to be partitioned into 'virtual' networks. This can be used to isolate classes of network membership at the Ethernet Packet level rather than at the IP level, as might be done with a router. This can be used to set up a 'management VLAN' where only devices that are members of that VLAN receives packets related to management, and, conversely, is isolated from the need to process network traffic for other VLANs.

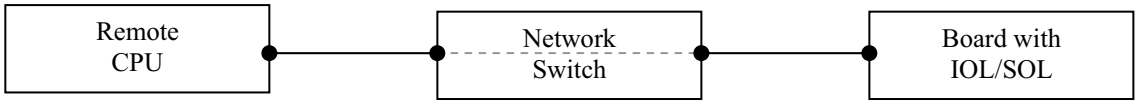
IPMI IOL end-node supports Ethernet II VLAN tagged frame format. This supports is provided by the 82571EB.

4.5.6 Serial Over Lan

This section provides the information required to establish an IPMI-Over-LAN sessions and activate the SOL payload in order to get an active SOL console sessions. In addition to the board payload supporting the IOL

(CPUx engine), a second CPU is required in order to remotely establish the IOL sessions. This second CPU is referred as the remote CPU and can be any computers (no IPMI support required).

Figure 4-1:Serial Over Lan



4.5.6.1 Configuring the IOL and SOL on the board payload

4.5.6.1.1 Configuring the IPMI-Over-LAN (IOL)

1 Enter the BIOS setup

2 Go to LAN configuration menu. LAN Configuration menu is located under 'System Management'. There is only 1 channel connected to the base interface.

3 Set LAN channel IP Address, Subnet Mask and if required the Gateway Address on the corresponding menu. The IOL IP address is static and does not support DHCP. Normally, the IOL IP address matches the corresponding base address LAN interface.

4 Set the channel to Active. Only 1 channel is available, so choose Disabled or Activate Channel 1.

5 Stay in CMOS setup to configure SOL.

4.5.6.1.2 Configuring the Serial-Over-LAN (SOL)

1 Go to the Remote Access Configuration menu. Remote Access Configuration menu is located under 'System Management'.

2 Set the Primary Serial Port Number to the serial port corresponding to the SOL architecture of the blade. The serial port is COM1. The serial port is the same as the front connector serial port. In order to leave the serial port to the SOL interface, just unconnected the serial cable from the front RJ45 jack, or select another CPU engine

3 Select port Baud Rate from the corresponding menu. Data Bits, Parity and Stop Bits shall be set to 8/ None/1.

4 Flow control shall be set to Hardware for proper operation.

5 Select Terminal option if required.

6 Save CMOS and exit.

4.5.6.2 Using SOL on remote CPU

IPMITool implements a Serial-Over-LAN console. It is recommended to have IPMITool version 1.8.9 (or higher). IPMITool can be downloaded from http://ipmitool.sourceforge.net/.

IOL information per board:

User / Password:

The default user "admin" and password "admin" give 'administrator' priviledges

IOL/SOL is unavailable when payload power is off or in reset.

1 Test the IOL connectivity. The following command shall return IPMC specific information:

```
ipmitool -H <ip address> -I lanplus -C 1 -U <user> -P <password> bmc info
```

2 Setup SOL console. The following command shall establish an IOL session and enable a SOL console:

```
ipmitool -H <ip address> -I lanplus -C 1 -U <user> -P <password>  sol
activate
```

If this command returns "Command not supported in present state"; disconnect the serial cable in the front serial RJ45 connector.

3 To access the CMOS BIOS menu, reset the board. Board BIOS splash screen will appear. Follow information to enter BIOS CMOS menu.

4 If you have a Linux console started on ttyS0 (getty or other), upon boot, you should get a login prompt (if you have the proper security configured - in file: `/etc/securetty`)

In order to have a console on ttySx, here is an example of the command to be added in the inittab file:

add `S1:2345:respawn:/sbin/agetty -hL ttyS0 115200 vt100` in inittab file:

`/etc/inittab` (the line should be add before 1:2345:respawn:/sbin/mingetty tty1).

See Linux documentation for complete details on how to get a Linux console started serial ttyS0.

Chapter 5

Software Setup

5. Software Setup

5.1 AMI BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory backed-up by a supercap (CPU Engine 0 only) or in the main BIOS flash and EEPROM. The latest is the default configuration.

5.1.1 Accessing the BIOS Setup Utility

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the AT8030 SBC. It uses the AMI Setup program, a setup utility in flash memory that is accessed by pressing the <F2> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

To run the AMI Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following messages, hit <F2> key to enter SETUP.

```
AMIBIOS(C)2006 American Megatrends, Inc.
KONTRON AT8030 BIOS Version 2.00

EVALUATION COPY, NOT FOR SALE
(C) American Megatrends, Inc.
64-0100-000001-00101111-102907-WHITLAKE-5006_040-Y2KC

CPU Engine: 0
Physical Processors: 1
Logical Processors: 2
Core Multi Processing: Enabled
FSB Speed: 666 MHz

Processor 0 Core 0 Type: Intel(R) Core(TM)2 CPU         L7400  @ 1.50GHz
Processor 0 Core 0 Speed: 1.50 GHz
Processor 0 Core 0 CPUID: 06F6
Processor 0 Core 0 Update Revision: 00C8

Processor 0 Core 1 Type: Intel(R) Core(TM)2 CPU         L7400  @ 1.50GHz
Processor 0 Core 1 Speed: 1.50 GHz
Processor 0 Core 1 CPUID: 06F6
Processor 0 Core 1 Update Revision: 00C8

Reset Type: Cold Reset
Currently Running on Primary FWH BIOS.

Press DEL to run Setup

 (F4 on Remote Keyboard)
Press F12 if you want to boot from the network
Press F11 for BBS POPUP

 (F3 on Remote Keyboard)
Initializing USB Controllers ..Done.
```

```
Memory Sockets          Size     Rank
DIMM 1 Memory Size      1024MB   Double
DIMM 2 Memory Size      1024MB   Double
DDR2 Speed: 400 MHz, Single Channel Mode
2048MB OK

USB Device(s):1 Storage Device
```

The main menu of the AMI BIOS CMOS Setup Utility appears on the screen. This example is based on CPU0 BIOS Setup Menu.

Figure 5-1:Example of BIOS Setup Menu

```
                              BIOS Setup Utility
 Main    Advanced    Security    Boot    System Management    Exit
 System Overview                                  Item Specific Help
 ----------------------------                     ------------------

 BIOS Version                    1.20.K
 Boot Block Version              1.00
 CPU Engine                      0

 DIMM 1 Memory Size              1 GB
 DIMM 2 Memory Size              1 GB

 System Memory Speed             400 MHz
 System Memory                   642 KB
 Extended Memory                 2048 MB                  <>    Select Screen
                                                          UD    Select Item
 System Time                     [15:00:03]               +-    Change Field
 System Date                     [09:08:2006]             Tab   Select Field
                                                          F1    General Help
                                                          F10   Save and Exit
                                                          ESC   Exit
```

Setup Default values provide optimum performance settings for all devices and system features.

Note:
The CMOS setup option described in this section is based on BIOS Version 2.00 The options and default settings may change in a new BIOS release.

CAUTION
These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

Note:
All options in Bold are the default settings.

5.1.2 Menu Bar

The Menu Bar at the top of the window lists these selections:

Table 5-1:BIOS Menu Bar

Menu Selection	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system.
Security	Use this menu to configure Security features.
Boot	Use this menu to determine the booting device order.
System Management	Use this menu to set and view the System Managment on your system.
Exit	Use this menu to choose Exits option.

Use the left and right arrows keys to make a selection.

5.1.2.1 Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates.

Table 5-2:BIOS Legend Bar

Key	Function
<F1>	General Help windows (see 4.1.2.2).
<Esc>	Exit this menu.
--> arrow keys	Select a different menu.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<->	Select the Previous Value for the field.
<+>	Select the Next Value for the field.
<F2> and <F3>	Change colors used in Setup.
<F7>	Disacard the changes for all menus.
<F9>	Load the Optimal Default Configuration values for all menus.
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the sub-menu.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. To save value commands in the Exit Menu, save the values displayed in all menus.

To display a submenu, use the arrow keys to move the cursor to the submenu you want. Then press <Enter>.

5.1.2.2 Field Help Window

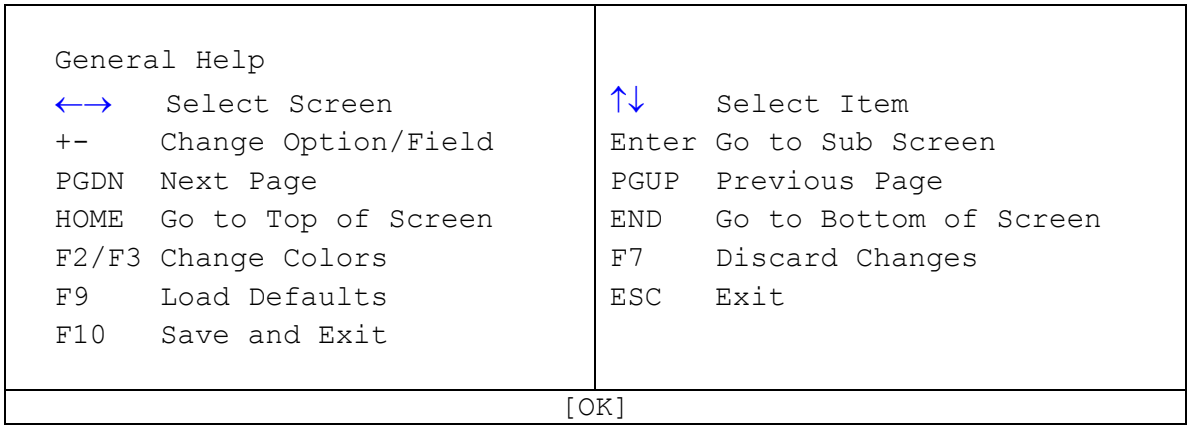
The help window on the right side of each menu displays the help text for the selected field.

It updates as you move the cursor to each field.

5.1.2.3 General Help Windows

Pressing <F1>on any menu brings up the General Help window that describes the legend keys and their alternates:

Figure 5-2:BIOS General Help Windows



5.1.3 Main Menu

Feature	Option	Description	Help text
BIOS Version	X.YY.KK	Displays the AMI BIOS version.	N/A, display only.
Build Date	MM/DD/YY	Display the BIOS build Date.	N/A, display only.
BIOS ID	5006_XYY	Displays the boot block version.	N/A, display only.
Boot Block Version	XYY	Diplay the FPGA Version.	N/A, display only.
CPU Engine	0/1/2	Displays the X86 CPU Engine currently executing this BIOS.	N/A, display only.
DIMM 1 Memory Size (CPU 0 only)	X KB/MB/GB	Displays DIMM 1 memory size. DIMM electrically closest to MICH (filled last). Kontron: DIMM slot physically furthest to the MICH.	N/A, display only.
DIMM 2 Memory Size (CPU 0 only)	X KB/MB/GB	Displays DIMM 2 memory size. DIMM electrically furthest to MICH (filled first). Kontron: DIMM slot physically closest to the MICH.	N/A, display only.
DIMM Memory Size (CPU 1 and 2)	X KB/MB/GB	Display DIMM memory size.	N/A, display only.
System Memory Speed	X MHz	Displays system memory speed.	N/A, display only.
System Memory	X KB	Displays amount system memory.	N/A, display only.
Extended Memory	X KB	Displays amount of extended memory.	N/A, display only.
System Time	HH:MM:SS	Set the system time.	Use [+] or [-] to configure system time.
System Date	MM/DD/YYYY	Set the system date.	Use [+] or [-] to configure system date.

5.1.4 Advanced Menu

Feature	Option	Description	Help text
Advanced Processor Configuration	N/A	Selects sub-menu.	N/A
ACPI Configuration	N/A	Selects sub-menu.	N/A
Event Log Configuration	N/A	Selects sub-menu.	N/A
Expansion ROM Configuration	N/A	Selects sub-menu.	N/A
PCI Express Configuration	N/A	Selects sub-menu.	N/A
USB Configuration	N/A	Selects sub-menu.	N/A
Advanced Chipset Control	N/A	Selects sub-menu.	N/A
MPS Revision	1.1 1.4	Configures the Multiprocessor Specification (MPS) revision level. Some operating systems might require revision 1.1 for compatibility reasons.	Multiprocessor specification revision level.

5.1.4.1 *Advanced Processor Configuration sub-menu*

Feature	Option	Description	Help text
Physical Processors	1	Displays the number of physical processors.	N/A, display only.
Logical Processors	1 or 2	Displays the number of logical processors.	N/A, display only.
Processor Type	Merom	Displays the type of the processor.	N/A, display only.
Processor 0 Speed	Varies	Displays the core speed of processor 0.	N/A, display only.
FSB Speed	Varies	Displays the Front Side Bus speed of processors (processor system bus speed).	N/A, display only.
Processor 0 Microcode	CPUID: XXX Update Revision: XXX	Displays the microcode version.	N/A, display only.
Processor 0 L2 Cache Size	2 MB	Displays processor 0 L2 Cache Size.	N/A, display only.
Processor Virtualization	Enabled **Disabled**	Allows a platform to run multiple operating systems and applications in independent partitions. With virtualization, one computer system can function as multiple “virtual” systems. BIOS locks this setting at the end of POST. Once locked, only a power cycle can unlock it for change.	Enabled: Processor virtualization in use. Disabled: Processor virtualization not in use."
SpeedStep	N/A	Selects sub-menu.	Configures SpeedStep technology.
Thermal Management	N/A	Selects sub-menu.	Configures thermal monitors.

5.1.4.2 SpeedStep Configuration sub-menu

Feature	Option	Description	Help text
Mode	Maximum Speed Minimum Speed **Variable Speed** Fixed Speed Disabled	Maximum: CPU speed is set to maximum. Minimum: CPU speed is set to minimum. Variable: CPU speed is controlled by operating system. Fixed: CPU speed is set to fixed value. Disabled: Default CPU speed is used.	Maximum: CPU speed is set to maximum. Minimum: CPU speed is set to minimum. Variable: CPU speed is controlled by operating system. Fixed: CPU speed is set to fixed value. Disabled: Default CPU speed is used.
Processor 0 Speed	1000 MHz (here all supported speeds between LFM and HFM as supported by Intel) 1500 MHz	All processor speed values are supported from LFM to HFM and in between as defined by Intel. Note: Help field will be shown only if option "Mode" is set to [Fixed Speed]. All other modes make this option display only.	Minimum speed: 1000 MHz Maximum speed: 1500 MHz
Processor 0 Core 0	Enabled (cannot be disabled)	Core 0 is the bootstrap core and it can't be disabled.	N/A, display only.
Processor 0 Core 1	**Enabled** Disabled	CMP can be disabled with this option i.e. only one execution core would be used.	Enabled: CMP is in use i.e. both CPU cores are available. Disabled: CMP is not used. Only Core 0 is available.

5.1.4.3 Thermal Management sub-menu

Feature	Option	Description	Help text
Thermal Monitor 1	**Enabled** Disabled	CPU thermal monitor mechanism.	Enabled: TM1 in use. Disabled: TM1 not in use. Use only for testing purposes.
Thermal Monitor 2	**Enabled** Disabled	CPU thermal monitor mechanism.	Enabled: TM2 in use. Disabled: TM2 not in use. Use only for testing purposes.
Digital Thermal Sensor	Enabled	Each execution core has a unique on die digital sensor (called Digital Thermal Sensor, DTS) whose temperature is accessible by BIOS via MSR (model specific register).	Enabled: DTS for each core is in use.

5.1.4.4 *ACPI Configuration sub-menu*

Feature	Option	Description	Help text
ACPI 2.0 Support	**Enabled** Disabled	Support for 64-bit addressing for ACPI System Description Tables can be enabled/disabled.	Enabled: 64-bit addressing supported for ACPI system description tables. Disabled: Only 32-bit addressing supported for ACPI system description tables.
ACPI APIC Support	**Enabled** Disabled	Support for ACPI APIC table pointer to Root System Description Table, RSDT pointer list can be enabled/disabled.	Enabled: ACPI APIC table support. Disabled: ACPI APIC table not supported.
Headless Mode	Enabled **Disabled**	Headless operation mode through ACPI can be enabled/disabled.	Enabled: Headless operation mode through ACPI supported. Disabled: Headless operation mode through ACPI not supported.

5.1.4.5 *Event Log Configuration sub-menu*

Feature	Option	Description	Help text
Event Log capacity	Space Available No Space	Displays whether there is room left to log events to the local system event log. The local event log needs to be cleared when this field shows “No Space”.	Shows if space is available in the Event Log for new log events.
Event Logging	**Enabled** Disabled	Configures if local system event log logging is enabled/disabled.	Enabled: Event Log is used. Disabled: Event Log is not used. If this option is disabled, no SEL events are available from this blade!
View Event Log	Enter	View all unread events in the Event Log.	View all unread events in the Event Log.
Mark Events as read	Enter	Mark all unread events as read in the Event Log.	Mark all unread events as read in the Event Log.
Clear all Event Logs	Enter	Discard all events in the Event Log.	Discard all events in the Event Log.
ECC Event Logging	**Enabled** Disabled	ECC Event Logging can be enabled/disabled.	Enabled: ECC event logging enabled. Disabled: ECC event logging disabled.
ECC Error Reporting	Correctable **Uncorrectable** Both Disabled	ECC error reporting mode.	Correctable: ECC for testing purposes. Uncorrectable: ECC errors reported. Both: ECC errors for testing purposes. Disabled: ECC errors not reported.
NSI Event Logging	**Enabled** Disabled	The IMCH and IICH are physically connected by an internal interface called NSI (North South Interface). NSI event logging can be enabled/disabled.	Enabled: NSI event logging enabled. Disabled: NSI event logging disabled.
FSB Event Logging	**Enabled** Disabled	The Front Side Bus is the connection between the chipset and the memory. FSB event logging can be enabled/disabled.	Enabled: FSB event logging enabled. Disabled: FSB event logging disabled.
Memory Buffer Event Logging	**Enabled** Disabled	Signals errors occurring in the chipset memory system coherent Posted Memory Write Buffer (PMWB). Memory buffer event logging can be enabled/ disabled.	Enabled: Memory buffer event logging enabled. Disabled: Memory buffer event logging disabled.
PCI Express Error Logging	**Enabled** Disabled	PCI Express error event logging can be enabled/disabled.	Enabled: PCI-E error event logging enabled. Disabled: PCI-E error event logging disabled.
PCI Express Error Masking	N/A	Selects sub-menu.	N/A

5.1.4.6 *PCI Express Error Masking sub-menu*

Feature	Option	Description	Help text
Mask duplicate Errors	**Yes** No	Duplicate errors can be masked if they are found in successive SMI interrupts when set to Yes. Note: Duplicate errors detected within a single SMI interrupt are always masked.	Yes: Mask duplicate errors found in successive SMI interrupts. No: Duplicate errors found in successive SMI interrupts are not masked. Note: Duplicate errors in single SMI interrupt are always masked.
Mask Unsupported Requests	**Yes** No	Unsupported request errors can be masked when set to Yes. If set to No, the default Mask is used based on Chipset recommendations.	Yes: Unsupported request errors can be masked. No: Default mask is used.

5.1.4.7 *Expansion ROM Configuration sub-menu*

Feature	Option	Description	Help text
Ethernet BI Expansion ROM	**Enabled** Disabled	The base interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via base interface is not available to boot the system.	Enabled: Initializes base interface PXE expansion ROM. Disabled: Base interface PXE expansion ROM not used. If disabled, remote LAN boot via BI is not available to boot the system!
Ethernet FI Expansion ROM	Enabled **Disabled**	The fabric interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via fabric interface is not available to boot the system.	Enabled: Initializes fabric interface PXE expansion ROM. Disabled: Fabric interface PXE expansion ROM not used. If disabled, remote LAN boot via FI is not available to boot the system!
Management Ports Expansion ROM (CPU 0 only)	Enabled **Disabled**	The Management Ports PXE Expansion ROM on the face plate can be enabled/disabled. If disabled, remote LAN boot via the management ports on the face plate is not available to boot the system.	Enabled: Initializes Management Ports PXE expansion ROM. Disabled: Management Ports PXE expansion ROM not used. If disabled, remote LAN boot via Management Ports is not available to boot the system!
SAS Expansion ROM (CPU 0 only)	**Enabled** Disabled	The SAS Expansion ROM can be enabled/ disabled. If disabled, any SAS devices attached to the system are not available to boot the system.	Enabled: Initializes SAS expansion ROM. Disabled: SAS expansion ROM not used. If disabled, any SAS devices attached to the system are not available to boot the system!
AMC Slot Expansion ROM (CPU 0 only)	Enabled **Disabled**	Enables or disables AMC Slot Expansion ROM(s), if any detected. If disabled, AMC Expansion ROM(s) code will not be executed during POST.	Enabled: Initializes AMC slot expansion ROM. Disabled: AMC slot expansion ROM not used.

5.1.4.8 *PCI Express Configuration sub-menu*

Feature	Option	Description	Help text
AMC Slot Hot Plug Support (CPU 0 only)	**Enabled** Disabled	AMC slot hot plug support can be enabled/ disabled.	Enabled: Hot plug for AMC slot available. Disabled: Hot plug for AMC slot not available.

5.1.4.9 USB Configuration sub-menu

Feature	Option	Description	Help text
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 Controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).	FullSpeed: 12 Mbps HiSpeed: 480 Mbps
BIOS EHCI Hand-Off	Enabled **Disabled**	A workaround for OSes without EHCI hand-off support can be enabled/disabled. The EHCI ownership change should be claimed by an EHCI driver.	Enabled: EHCI hand-off support enabled. Disabled: EHCI hand-off support disabled.
External USB Storage Booting	Enabled **Disabled**	External USB storage Devices booting can be disabled. This is used to prevent booting from external USB hard-drive, CD-ROM, floppy or memory stick. This option only affect USB booting, not OS support for USB storage devices.	Enabled: On-board or External USB storage devices can boot the system. Disabled: Only on-board USB storage device can boot the system.
USB Mass Storage Device Configuration (only present if USB Mass Storage detected)	N/A	Selects sub-menu.	Configure the USB Mass Storage Class Devices.

5.1.4.10 USB Mass Storage Device Configuration sub-menu

Feature	Option	Description	Help text
Device #1-6		Mass Storage Device identification	
Emulation Type (for each devices)	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD.

5.1.4.11 *Advanced Chipset Control sub-menu*

Feature	Option	Description	Help text
Memory Remapping Feature	**Enabled** Disabled	Remapping of overlapped PCI memory above the total physical memory can be allowed/ denied. If remapping of memory is done, it will be accessible above 4GB and thus will require PAE support in OS.	Enabled: Allows remapping of overlapped PCI memory above the total physical memory. Requires PAE support in OS. Disabled: Memory remapping not allowed.
DMA Controller	**Enabled** Disabled	DMA Controller can be enabled/disabled.	Enabled: DMA controller enabled. Disabled: DMA controller disabled.
DDR2 Refresh	3.9 µS 7.8 µS **Auto**	Allows override selection of the DDR2 refresh rate for normal operation. Higher Refresh Rate may be required when operating in high temperature environments.	Allows override selection of the DDR2 refresh rate for normal operation.
Spread Spectrum Clocking Mode	**Enabled** Disabled	Allows BIOS to set Clock Spread Spectrum for EMI (electromagnetic interference) control.	Enabled: Allows setting of Clock Spread Spectrum for EMI control. Disabled: Denies setting of Clock Spread Spectrum for EMI control.

5.1.5 Security Menu

Feature	Option	Description	Help text
Supervisor Password	Installed Not Installed	Indicates the status of the Supervisor Password.	Indicates the status of the supervisor password.
User Password	Installed Not Installed	Indicates the status of the User Password.	Indicates the status of the user password.
Set Supervisor Password	Enter	The supervisor password can be installed or changed.	Install or change the supervisor password.
Set User Password	Enter	The user password can be installed or changed.	Install or change the user password.
Clear User Password	Enter	Immediately clears the User password.	Clears user password.
User Access Level	No Access **View Only** Limited Full Access	Controls the user access level to the BIOS Setup utility. Supervisor has full access to the BIOS Setup utility. No Access: Prevents user access to the setup utility. View Only: Allows read only user access to the setup utility i.e. none of the fields can be changed. Limited: Allows limited fields such as date and time to be changed in user access to the setup utility. Full Access: Allows unlimited user access to the setup utility	Controls access to the setup utility. No Access: Prevents user access. View Only: Allows read only user access. Limited: Allows limited fields to be changed. Full Access: Allows unlimited user access.
Execute Disable Bit	Enabled **Disabled**	Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot preventing certain classes of malicious buffer overflow attacks when combined with a supporting operating system.	Enabled: Allows processor to prevent application code access to certain memory areas. Needs supporting OS. Disabled: No restrictions to application code memory area access by processor.

5.1.6 Boot Menu

Feature	Option	Description	Help text
Boot Settings Configuration	N/A	Selects sub-menu.	Selects boot settings configuration.
Boot Device Priority	N/A	Selects sub-menu.	Selects boot device priority.
Hard Disk Drives	N/A	Selects sub-menu.	Lists available hard disk drives in priority order.
Removable Drives	N/A	Selects sub-menu.	Lists available removable disk drives in priority order.
CD/DVD Drives	N/A	Selects sub-menu.	Lists available CD/DVD drives in priority order.
USB Drives	N/A	Selects sub-menu.	Lists available USB drives in priority order.
Network Drives	N/A	Selects sub-menu.	Lists available network drives in priority order.
Other Drives	N/A	Selects sub-menu.	Lists available other drives in priority order.

5.1.6.1 Boot Settings Configuration sub-menu

Feature	Option	Description	Help text
Quick Boot Mode	**Enabled** Disabled	Allows/denies skipping the memory tests during a cold boot. Quick Boot enabled has no impact on a warm reset boot since then memory is not initialized during a warm reset.	Enabled: Allows skipping the memory tests during a cold boot. Disabled: Allows the extended memory test to be executed during a cold boot.
Extended Memory Test	Enabled **Disabled**	If enabled, extended memory test is applicable when Quick Boot is disabled and a cold reset occurs. If disabled, extended memory test is not performed except if memory configuration has changed or in the very first boot of the blade. Warm reset should always be as fast as possible and extended memory test is never executed in warm reset.	Enabled: Extended memory test is applicable when Quick Boot is disabled and a cold reset occurs. Disabled: Extended memory test is not performed in a reset.

5.1.6.2 Boot Device Priority sub-menu

Feature	Option	Description	Help text
1st Boot Device	Type: Boot device	Specifies the priority of the available boot sources. The list includes USB CD ROM, USB Hard Drive, SAS Hard Drive and PXE. Other supported devices might be dynamically added to the list.	Specifies the priority of the available boot sources.
		...	
Nth Boot Device	Type: Boot device	Specifies the boot priority of the available boot sources. The list includes USB CD ROM, USB Hard Drive, SAS Hard Drive and PXE. Other supported devices might be dynamically added to the list.	Specifies the priority of the available boot sources.

5.1.6.3 Hard Disk Drives sub-menu

Feature	Option	Description	Help text
1st Drive	Varies	Specifies the boot priority of the available Hard Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.
		...	
Nth Drive	Varies	Specifies the boot priority of the available Hard Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.

5.1.6.4 Removable Drives sub-menu

Feature	Option	Description	Help text
1st Drive	Varies	Specifies the boot priority of the available Removable devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.
...			
Nth Drive	Varies	Specifies the boot priority of the available Removable devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.

5.1.6.5 CD/DVD Drives sub-menu

Feature	Option	Description	Help text
1st Drive	Varies	Specifies the boot priority of the available CD/DVDDisk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.
...			
Nth Drive	Varies	Specifies the boot priority of the available CD/DVD Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.

5.1.6.6 USB Disk Drives sub-menu

Feature	Option	Description	Help text
1st Drive	Varies	Specifies the boot priority of the available USB Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.
...			
Nth Drive	Varies	Specifies the boot priority of the available USB Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.

5.1.6.7 Network Disk Drives sub-menu

Feature	Option	Description	Help text
1st Drive	Varies	Specifies the boot priority of the available Network Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.
...			
Nth Drive	Varies	Specifies the boot priority of the available Network Disk devices.	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.

5.1.6.8 *All Other Disk Drives sub-menu*

Feature	Option	Description	Help text
1st Drive	Varies	Specifies the boot priority of any other available devices (other than Hard Disk, Removable, CD/DVD, USB disk or Network).	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.
...			
Nth Drive	Varies	Specifies the boot priority of any other available devices (other than Hard Disk, Removable, CD/DVD, USB disk or Network).	Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device.

5.1.7 System Management Menu

Feature	Option	Description	Help text
Remote Access Configuration	N/A	Selects sub-menu.	N/A
Set LAN Configuration	N/A	Selects sub-menu.	IPMI over LAN (and Serial Over LAN).
Watchdog Timers	N/A	Selects sub-menu.	N/A
System Information	N/A	Selects sub-menu.	N/A

5.1.7.1 *Remote Access Configuration sub-menu*

Feature	Option	Description	Help text
Serial Port Number	**COM1** COM2	Configures serial port for console redirection. Also used for Headless operation mode through ACPI.	Select serial port for console redirection.
Serial Port 1 I/O address	3F8/IRQ4	Displays the hardware address of the COM 1 port.	N/A, display only.
Serial Port 2 I/O address	2F8/IRQ3	Displays the hardware address of the COM 2 port i.e. RTM serial port.	N/A, display only.
Baud Rate	9.6 KB 19.2 KB 38.4 KB 57.6 KB **115.2 KB**	Configures serial port Baud rate for both serial ports.	Select serial port Baud rate.
Data Bits	7 **8**	Configures the number of data bits in each transmitted or received serial character for both serial ports. Note: Serial Over LAN operation uses fixed parameter (Data Bits = 8).	Select the number of data bits in each transmitted or received serial character.
Parity	Even Odd **None**	Configures if parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data for both serial ports. Note: Serial Over LAN operation uses fixed parameter (Parity = None).	Select if parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data.
Stop Bits	**1** 2	Configures the number of stop bits transmitted and received in each serial character for both serial ports. Note: Serial Over LAN operation uses fixed parameter (Stop Bits = 1).	Select the number of stop bits transmitted and received in each serial character.
Flow Control	**Hardware** Software None	Configures flow control for console redirection for both serial ports.	Select flow control for console redirection.
Terminal Type	**ANSI** VT100 VTUTF8	Configures the type of console emulation used for both serial ports.	Select the typeof console emulation used.
Terminal Size	80x24	Displays terminal size.	N/A, display only.
Terminal Display Mode	**Normal Mode** Recorder Mode	Configures terminal display mode. If Normal Mode, console redirection done by the BIOS after POST will send ANSI codes. If Recorder Mode, console redirection done by the BIOS after POST will not send ANSI codes. This will result in faster text outputs, similar to a Linux console, but any program that rely on ANSI code to position the text will be practically unreadable.	Select terminal display mode.
BIOS Printouts	**Enabled** Disabled	Configures if BIOS POST messages are duplicated in a separate reserved memory region for OS examination.	Select if BIOS POST messages are duplicated in a separate reserved memory region for OS examination.

5.1.7.2 Set LAN Configuration Sub-menu

Feature	Option	Description	Help text
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
IP Address	N/A	Selects sub-menu.	Enter for IP Address Configuration.
MAC Address	N/A	Selects sub-menu.	Enter for MAC Address Configuration.
Subnet Mask	N/A	Selects sub-menu.	Enter for Subnet Mask Configuration.
Gateway Address	N/A	Selects sub-menu.	Enter for Gateway IP Address Configuration.
VLAN ID	N/A	Selects sub-menu.	Enter for VLAN ID Configuration.
VLAN Priority	N/A	Selects sub-menu.	Enter for VLAN Priority Configuration.
Active LAN Channel Number	**None** 01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Active LAN Channel Number for Set LAN Configuration Command.

5.1.7.3 IP Configuration sub-menu

Feature	Option	Description	Help text
LAN Parameter Selector	03	The parameter selector assignments are described in IPMI Specification 1.5, table 19-4. Selector #03: IP Address.	N/A, display only.
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
IP Address	xxx.xxx.xxx.xxx	This allows setting an IP Address for LAN configuration.	Enter IP Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only).
Current IP Address	xxx.xxx.xxx.xxx	Display the current LAN configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.7.4 MAC Address Configuration sub-menu

Feature	Option	Description	Help text
LAN Parameter Selector	05	The parameter selector assignments are described in IPMI Specification 1.5, table 19-4. Selector #05: MAC Address.	N/A, display only.
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
Current MAC Address	xx.xx.xx.xx.xx.xx	Display the current MAC Address stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.7.5 Subnet Mask Configuration sub-menu

Feature	Option	Description	Help text
LAN Parameter Selector	06	The parameter selector assignments are described in IPMI Specification 1.5, table 19-4. Selector #06: Subnet Mask.	N/A, display only.
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
Subnet Mask	xxx.xxx.xxx.xxx	This allows setting of a Subnet Mask for LAN configuration.	Enter Subnet Mask in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only).
Current Subnet Mask	xxx.xxx.xxx.xxx	Display the current Subnet Mask configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.7.6 Gateway Address Configuration sub-menu

Feature	Option	Description	Help text
LAN Parameter Selector	12	The parameter selector assignments are described in IPMI Specification 1.5, table 19-4. Selector #12: Default Gateway Address.	N/A, display only.
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status:	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
Gateway Address	xxx.xxx.xxx.xxx	This allows setting an Gateway IP Address for LAN configuration.	Enter Gateway IP Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only).
Current Gateway Address:	xxx.xxx.xxx.xxx	Display the current Gateway configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.7.7 VLAN ID Configuration

Feature	Option	Description	Help text
LAN Parameter Selector	20	The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #20: 802.1q VLAN ID (12-bit).	N/A, display only.
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status:	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
802.1q VLAN ID Value	xxx	This allows setting an 802.1q VLAN ID for LAN configuration.	Enter VLAN ID value in hexadecimal in the form of XXX.
Current 802.1q VLAN ID Value:	xxx	Display the current 801.1q VLAN ID configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.
Support VLAN Tagged Packets	**Enabled** Disabled	Select if 802.1q VLAN tagged packets are added.	Select if VLAN Tagged Packets are to be added or not.
VLAN Tagged Packets Status:	Enabled or Disabled	Display the current status of the 801.1q VLAN tagged packets configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.7.8 VLAN Priority Configuration

Feature	Option	Description	Help text
LAN Parameter Selector	21	The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #21: 802.1q VLAN Priority.	N/A, display only.
Channel Number	01	Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Only one channel on Base interface is available. The channel number assignments are described in IPMI Specification 1.5, table 6-1.	Enter Channel Number for SET LAN Config Command. Proper value below 16.
Channel Status:	Valid or Invalid	Display Valid if IPMC support LAN Channel.	N/A, display only.
802.1q VLAN Priority Value	x	This allows setting an 802.1q VLAN priority for LAN configuration.	Enter VLAN Priority value in decimal. Proper value below 8.
Current VLAN Priority Value:	x	Display the current 801.1q VLAN Priority configuration stored in IPMI NVRAM for IPMI LAN.	N/A, display only.

5.1.7.9 Watchdog Timer sub-menu

Feature	Option	Description	Help text
BIOS POST Timeout	0 60 120 **150** 300 600	Configures the BIOS POST IPMI HW watchdog timeout value in seconds. The BIOS POST watchdog will be disabled if the timeout value is set 0.	Select the BIOS POST IPMI HW watchdog timeout value.
BIOS POST Action	No Action **Warm Reset** Power Down Power Cycle	Configures which action to take when the BIOS POST IPMI HW watchdog expires. Note: warm reset is done only if a complete cold boot POST sequence has been successfully completed. If the warm reset flag at address 40:72h is not set, BIOS will force a cold reset.	Select which action to take when the BIOS POST IPMI HW watchdog expires.
OS Load Timeout	0 15 30 45 60 90 120 **150** 300 600	Configures the OS Load IPMI HW watchdog timeout value in seconds. The OS Load watchdog will be disabled if the timeout value is set 0.	Select the OS Load IPMI HW watchdog timeout value.
OS Load Action	No Action **Warm Reset** Power Down Power Cycle	Configures which action to take when the OS Load IPMI HW watchdog expires.	Select which action to take when the OS Load IPMI HW watchdog expires.

5.1.7.10 System Information sub-menu

Feature	Option	Description	Help text
Board Product Name	AT8030	Displays the CPU blade product name.	N/A, display only.
Board Vendor	Kontron	Displays CPU blade vendor.	N/A, display only.
Board Serial Number	Varies	Displays the CPU blade serial number.	N/A, display only.
Board Part Number	Varies	Displays the CPU blade part number.	N/A, display only.
Chassis Slot	1..16	Displays the current chassis slot number for the CPU blade.	N/A, display only.
FWH In Use	Primary Secondary	Displays the current Firmware device in use (primary or secondary).	The current Firmware device in use (primary or secondary).
IPMI Device and FW Info	N/A	Selects sub-menu.	N/A, display only.

5.1.7.11 IPMI Device and FW Info sub-menu

Feature	Option	Description	Help text
IPMI Version	1.5	Displays IPMI Specification version.	N/A, display only.
IPMI Device ID	Varies	Displays IPMI device ID. OEM defined, IPMI Device ID has been assigned like this: Renesas H8S2148 = 1 Kontron PMM = 2 Renesas H8S2145 = 3 Renesas H8S2166 = 4 Renesas H8S2138 = 5 Renesas H8S2168 = 6	N/A, display only.
IPMI Device Revision	Varies	Displays IPMI device revision. OEM defined, specify the version of the IPMI Device controller.	N/A, display only.
IPMI Firmware Version	Varies	Displays IPMI firmware version.	N/A, display only.
SDR Revision	Varies	Displays SDR (Sensor Data Record) revision. This field correpond to the implementation specific auxiliary information from IPMI ""Get Device ID Command"", byte 13. The SDR revision is displayed in decimal notation.	N/A, display only.
Aux Revision Info byte 1	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 14. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.
Aux Revision Info byte 2	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 15. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.
Aux Revision Info byte 3	Varies	Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 16. The byte is displayed as a 2-digit hexadecimal number.	N/A, display only.

5.1.8 Exit Menu

Feature	Option	Description	Help text
Exit Saving Changes	N/A	Saves modified settings into non-volatile memory and reboots the system.	Exit system setup saving changes to non-volatile memory.
Exit Discarding Changes	N/A	Discards modifications to settings and reverts to the state when Setup was entered, then complete remaining POST.	Exit system setup without saving changes.
Load Setup Defaults	N/A	Loads the factory default settings.	Load default settings.
Discard Changes	N/A	Discards modifications to settings and reverts to the state when Setup was entered.	Discard changes without exiting setup.
Exit & Update BIOS	N/A	Discard changes and forces a BIOS recovery mode on the next system reset and performs the system reset. A recovery USB CD-ROM, Flash disk or floppy must be present or the system needs to be configured for serial recovery mode. This mode can be used when on-board recovery jumper is not installed.	Force BIOS recovery mode on next system reset.
Exit & Execute BIOS Swap	N/A	Exits the Setup utility without saving any changes and then performs a swap of the on-board BIOS FWH chips. If the currently executing BIOS was the primary BIOS, the system would change to the backup BIOS (and vice versa).	Swap BIOS FWH without saving any changes.

5.2 Boot Utilities

AMI Boot Utilities are: Boot Menu POP-UP

Boot Menu POP-UP is a boot screen that displays a selection of boot devices from which you can boot your operating system.

5.2.1 Pressing <F2>

Pressing < F2 > during POST enters Setup.

5.2.2 Pressing <F11> (or <F3> from a Console Redirection terminal)

Pressing <F11> (or <F3> from a Console Redirection terminal) displays the Boot Menu POP-UP with these options:

1 Load the operating system from a boot device of your choice.

2 Exit the Boot Menu POP-UP (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

5.2.3 BOOT Menu POP-UP

The BOOT Menu POP-UP expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CDROM, Flash Disk, SCSI or LAN. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in the Boot device <F11> (or <F3> from a Console Redirection terminal).

5.3 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setup of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

5.3.1 Requirements

The terminal should emulate a VT100 or an ANSI terminal. Terminal emulation programs such as Telix©, HyperTherminal(Windows), minicom(Linux) or ProComm©(Windows) can also be used.

5.3.2 ANSI and VT100 Keystroke Mapping

Table 5-3:ANSI and VT100 Keystroke Mapping

Up	<ESC>[A
Down	<ESC>[B
Right	<ESC>[C
Left	<ESC>[D
Home	<ESC>[H
End	<ESC>[K
F1	<ESC>OP
F2	<ESC>OQ
F3	<ESC>OR
F4	<ESC>OT

5.3.3 VT-UTF8 Keystroke Mapping

The following "escape sequences" are defined in the "Conventions for Keys Not in VT100 Terminal Definition and ASCII Character Set" section of "Standardizing Out-of-Band Management Console Output and Terminal Emulation (VT-UTF8 and VT100+)",available for download at microsoft.com.

Table 5-4:VT-UTF8 Keystroke Mapping

F1 Key	<ESC>1
F2 Key	<ESC>2
F3 Key	<ESC>3
F4 Key	<ESC>4
F5 Key	<ESC>5
F6 Key	<ESC>6
F7 Key	<ESC>7

F8 Key	<ESC>8
F9 Key	<ESC>9
F10 Key	<ESC>0
F11 Key	<ESC>!
F12 Key	<ESC>@
Alt Modifier	<ESC>^A
Control Modifier	<ESC>^C
Home Key	<ESC>h
End Key	<ESC>k
Insert Key	<ESC>+
Delete Key	<ESC>-
Page Up Key	<ESC>?
Page Down Key	<ESC>/

These "escape sequences" are supported by VT-UTF8 compliant terminal connections, such as Windows Server 2003 Emergency Management Services (EMS).

AMIBIOS8 Serial Redirection supports these key sequences under two configurations:

- "Terminal Type" setup question is set to "VT-UTF8"
- "Terminal Type" setup question is set to "VT100" or "ANSI" and "VTUTF8 Combo Key Support" setup question is set to "Enabled"

5.4 Installing Drivers

WindRiver PNE Linux 1.5 BSP and RedHat Enterprise Linux 5 include all required drivers to fully support all on-board sevices.

Chapter 6

Unit Computer Management

6. Unit Computer Management

6.1 Ethernet Switch Management

The BCM56502 Ethernet Switch is managed by the Unit Computer. The basic management interfaces are SNMP and a command line interface (CLI). The CLI is accessible by the Unit Computer's serial or Ethernet interface. The Unit Computer can not be operated with an arbitrary operating system but executes a custom OS and switch specific application software.

Before loading the OS and application software, the bootloader code (universal bootloader, u-boot) initializes the main components of the board like CPU, SDRAM, serial lines etc. for operation. After this, kernel and application are started from flash. The bootloader may also be used for adjusting some basic settings like the parameters of the serial interface. Bootloader commands are listed in appendix Bootloader.

All three Unit Computer SW components (bootloader, OS and application software) are kept in the flash memory and are field updateable. The update process is described in Software Update appendix.

For supported RFCs and SNMP MIBs, refer to appendices Supported RFCs and Supported MIBs. For a comprehensive listing and description of available CLI commands, refer to the CLI Reference Manual.

6.2 Unit Computer Diagnostics

Upon power on or system reset, the bootloader performs a set of Power On Self Tests (POST) to check the integrity of specific components. Components where a POST is available are:

- SDRAM
- Serial line
- Ethernet interfaces
- IPMC KCS interface

In the case that a POST fails, a POST error code is written into the postcode high byte register of the onboard FPGA. The boot process is not stopped as there are good chances the board can boot even in case of POST errors. The postcode high byte register is also accessible by the IPMC which can report error codes to a separate management instance. Thus more comprehensive diagnostic tests could be started.

The following table shows a list of available POST routines including POST error codes.

Table 6-1:POST routines and error codes

Device	Test	POST Error Code
SDRAM	Data bus - walking 1 test	PCW_DLINE
SDRAM	Address bus - walking 1 test	PCW_ALINE
SDRAM	Memory - read/write test	PCW_MEM
ES UART	Serial loopback teststring	PCW_SERIAL

Device	Test	POST Error Code
ES I2C	Bus scan for devices from I2C_ADDR_LIST	PCW_I2C
ES FE	Phy access	PCW_ETH1
ES FE	Phy loopback test using special Ethernet test frame	PCW_ETH2
KCS	KCS READY signal test	KCSCTL

In addition to the Power On Self Tests described above, the bootloader logs the board startup sequence in the postcode low byte register. A postcode value is written each time a step in the start sequence has been completed successfully. The postcode stored is also accessible by the IPMC. In the case that an error occurs during execution of a step, the boot sequence is stopped because a fatal error has occurred with great likelihood. In this case, a management instance can read the last postcode written via the IPMC and thus determine where the fatal error has occurred.

A list of defined postcodes is shown in the table below.

Table 6-2:POST Boot Steps

POST Step Code	Value	Boot Step
PC_INIT	0x00	Initial PC, EBC has been set up
PC_BINIT	0x01	Board early init (interrupt settings)
PC_CLOCKS	0x02	Get system clocks
PC_TIMEB	0x03	Init timebase
PC_ENVINIT	0x04	Init environment
PC_BAUD	0x05	Init baudrate
PC_SERIAL	0x06	Init UART
PC_CPU	0x07	Check CPU
PC_PHY	0x08	Setup PHY
PC_I2C	0x09	Init I2C
PC_INITRAM	0x0A	Init SDRAM controller and SDRAM
PC_TESTRAM	0x0B	Test SDRAM
PC_INITSEQ	0x0F	Board init sequence completed
PC_INITBOARD	0x10	Board init ok, stack set up ok, board info struct set up
PC_RELOC	0x11	Relocation completed
PC_TRAP	0x18	Setup trap handler
PC_FLASH	0x19	Flash OK
PC_CPU2	0x1A	Init higher level parts of CPU
PC_RELOCENV	0x1B	Relocation of environment Ok
PC_BDINFO	0x1C	Fill missing fields of bdinfo
PC_PCI	0x1D	PCI configuration done
PC_DEVICES	0x1E	Device init done
PC_JUMPTABLE	0x1F	Jumptable init done
PC_CONSOLE	0x20	Console init done
PC_MAIN	0x2F	Enter main loop
PC_START_OS	0x3F	Pass control to OS, leave bootloader

Chapter 7

Thermal Considerations

7. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when using the AT8030.

7.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AT8030, all on-board components must remain within the maximum temperature specifications. The most critical components on the AT8030 are the processors, the memory modules and the chipset. Operating the AT8030 above the maximum operating limits will result in application performance degradation (due to throttling of the processor) or may even damage the board. To ensure functionality at a maximum operating temperature, the blade supports several temperature monitoring and control features.

7.1.1 Heat Sinks

Multiple key components of the AT8030 are equipped with specifically designed heat sinks to ensure the best possible product for operational stability and long-term reliability. The physical size, shape, and construction of the heat sinks ensures the lowest possible thermal resistance. Moreover, the heat sinks were specifically designed to use forced airflow as found in ATCA systems. Because the thermal solution is custom and critical for passive cooling, Kontron does not guarantee thermal performance if the heatsinks are removed and then reinstalled by the end user.

7.1.2 Temperature Sensors

The AT8030 is equipped with 28 temperature sensors that are accessible via IPMI. Sensors are precisely positioned near critical components to accurately measure the on-board parts temperature. Temperature monitoring must be exercised to ensure highest possible level of system thermal management. An external system manager constitutes one of the best solutions for thermal management, being able to report sensor status to end-user or manage events filters for example.

All sensors available on the AT8030, its RTM and the AMC it can carry are listed into the Sensor Data Repository with their thresholds as defined by the PICMG 3.0 specification. The following extract (from the PICMG 3.0 Base Specification) details naming convention for thresholds as well as the meaning of each threshold level.

IPMI non-critical / PICMG 3.0 minor / telco minor:

A warning that things are somewhat out of normal range, but not really a "problem" yet

IPMI critical / PICMG 3.0 major / telco major:

Things are still in valid operating range, but are getting close to the edge; unit still operating within vendor-specified tolerances

IPMI non-recoverable / PICMG 3.0 critical/ telco critical:

Unit no longer operating within vendor-specified tolerances

Most ATCA chassis react to temperature events in the following manner: when a minor threshold is reached, the shelf manager will incrementally increase airflow (fan speed) to bring the temperature below the crossed threshold. When a major threshold is reached, the shelf manager will increase the fans to maximum speed. When a critical threshold is reached, the shelf manager will shutdown the blade to prevent damage. The shelf alarm panel, when available, can inform the operator with LEDs when an alarm (minor, major, critical) is raised. Refer to your chassis documentation to adapt and optimize your temperature monitoring application to chassis capabilities. See also System Airflow section for more information.

Below is the list of temperature sensors with their respective thresholds.

Sensor ID	Lower Thresholds			Upper Thresholds		
	Minor	**Major**	**Critical**	**Minor**	**Major**	**Critical**
Temp Switch	5°C	0°C	-10°C	90°C	100°C	115°C
Temp Dual Phy Co	5°C	0°C	-10°C	80°C	90°C	105°C
Temp SOC-DIMM	5°C	0°C	-10°C	75°C	85°C	100°C
Temp Air Inlet	5°C	0°C	-10°C	65°C	75°C	90°C
Temp PQ3	5°C	0°C	-10°C	75°C	85°C	100°C
Temp Dual Phy Se	5°C	0°C	-10°C	80°C	90°C	105°C
Temp LSI SAS Dis	5°C	0°C	-10°C	80°C	90°C	105°C
Temp Mez 12v Out	0°C	-5°C	N/A	70°C	85°C	110°C
Temp -48V A Feed	0°C	-5°C	N/A	70°C	85°C	110°C
Temp -48V B Feed	0°C	-5°C	N/A	70°C	85°C	110°C
CPU2:Temp DIMM0	5°C	0°C	-10°C	75°C	85°C	100°C
CPU2:Temp MCH	5°C	0°C	-10°C	85°C	95°C	110°C
CPU2:Temp Vcore	5°C	0°C	-10°C	95°C	105°C	120°C
CPU2:Temp FI/BI	5°C	0°C	-10°C	95°C	105°C	115°C
CPU2:Temp CPU	5°C	0°C	-10°C	90°C	100°C	115°C
CPU1:Temp DIMM0	5°C	0°C	-10°C	75°C	85°C	100°C
CPU1:Temp MCH	5°C	0°C	-10°C	85°C	95°C	110°C
CPU1:Temp Vcore	5°C	0°C	-10°C	95°C	105°C	120°C
CPU1:Temp FI/BI	5°C	0°C	-10°C	95°C	105°C	120°C
CPU1:Temp CPU	5°C	0°C	-10°C	90°C	100°C	115°C
CPU0:Temp LSI SAS	5°C	0°C	-10°C	85°C	95°C	110°C
CPU0:Temp FrontEth	5°C	0°C	-10°C	95°C	105°C	115°C
CPU0:Temp BIMM1	5°C	0°C	-10°C	75°C	85°C	100°C
CPU0:Temp DIMM0	5°C	0°C	-10°C	75°C	85°C	100°C
CPU0:Temp MCH	5°C	0°C	-10°C	85°C	95°C	110°C
CPU0:Temp Vcore	5°C	0°C	-10°C	95°C	105°C	120°C
CPU0:Temp FI/BI	5°C	0°C	-10°C	95°C	105°C	115°C
CPU0:Temp CPU	5°C	0°C	-10°C	90°C	100°C	115°C

Table 7-1:Temperature Sensors Thresholds

7.1.3 Airflow Blockers

It is highly recommended to use airflow blockers in any empty ATCA slot or AMC bay to keep the airflow within the ATCA chassis. Failure to do so would go against forced air principles used by ATCA components, reducing the system's cooling efficiency. Moreover, airflow blockers offer an equivalent impedance to forced air to a typical board, which balances airflow across the chassis.

7.1.4 System Airflow

The airflow impedance (pressure) curve gives information for the thermal operational range of the system carrying the AT8030. Once the volumetric airflow capability of your chassis is known, the pressure curve can help determine the ambient (room) temperature setpoint that should be used for optimal operation. If you are using various models of ATCA blades in the same chassis, it is possible to find the best thermal fit. Having the volumetric airflow value for each chassis slot, it is then possible to decide the layout using the pressure curves.

Airflow (CFM)	Pressure drop (inch of water)	Airflow (CFM)	Pressure Drop (inch of water)
12	0,0274	27	0,0862
13	0,0295	28	0,0928
14	0,0317	29	0,0997
15	0,0346	30	0,1069
16	0,0371	31	0,1147
17	0,0402	32	0,1231
18	0,0433	33	0,1316
19	0,0468	34	0,1407
20	0,0505	35	0,1501
21	0,0546	36	0,1594
22	0,0587	37	0,1688
23	0,0634	38	0,1792
24	0,068	39	0,1895
25	0,0734	40	0,2001
26	0,0799		

Table 7-2:Pressure curve T5006 with AMC Filler

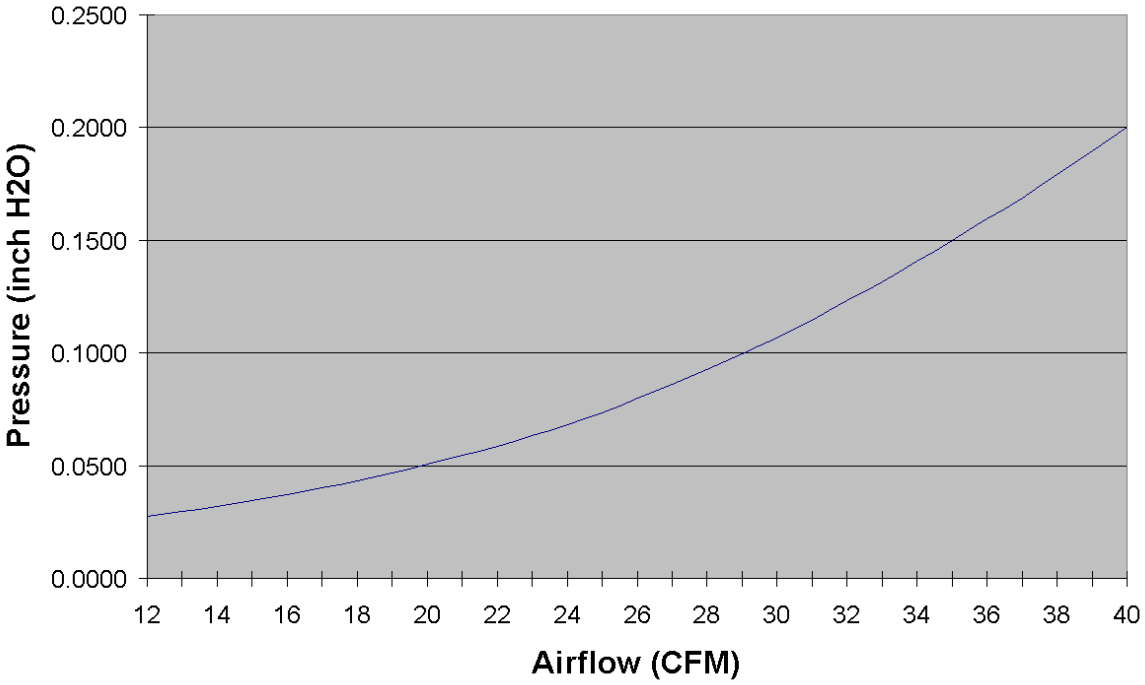
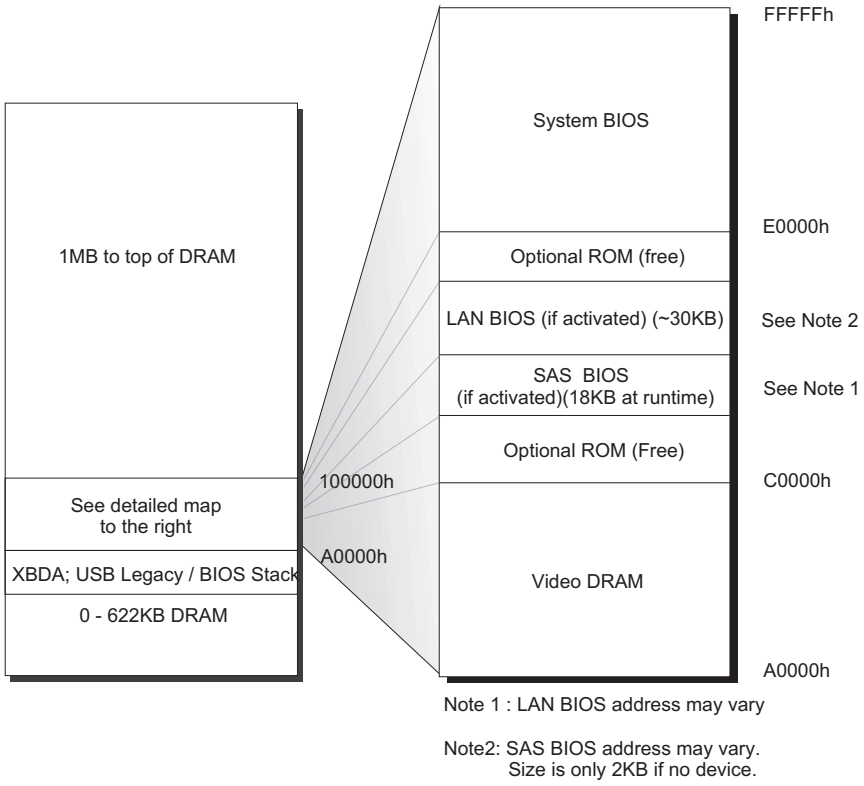


Figure 7-1:Pressure curve T5006 with AMC Filler

A. Memory & I/O Maps

A.1 Memory Mapping



Address	Function
00000-9B7FF	0-622 KB DRAM
9B800-9FFFF	622KB - 640 KB XBDA; USB Legacy / BIOS Stack
A0000-BFFFF	Video DRAM
C0000-DBFFF	Optional ROM (Free) LAN BIOS around 30KB if activated, address may vary External Fiber Channel BIOS 18KB-64KB , address may vary
E0000-FFFFF	System BIOS
100000-PCI Memory	DRAM available

A.2 Kontron I/O Mapping

Address	Optional Address	Function
000-01F		DMA Controller 1
020-03F		Interrupt Controller 1
040-05F		Timer
060-06F		Keyboard
070-07F		Real-time clock
080-09F		DMA Page Register
0A0-0BF		Interrupt Controller 2
0C0-0DF		DMA Controller 2
0F0-0F1, 0F8-0FF		Math Coprocessor
1F0-1F7, 3F6		Primary IDE
170-177, 376		Secondary IDE
200-20F		Kontron Registers (on-board)
378-37F		Parallel Port (Used as PLD POD)
3F8-3FF (COM1)	2F8-2FF (COM2)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	Serial Port 2 (COM2 by default)
400-7FF		Chipset Reserved
800-0FFF		Chipset Reserved

A.3 PCI IDSEL and Device Numbers

A.3.1 CPU Engine 0

BUS#	DEV#	V. ID	D. ID	Funct. #	Description	PCI Description
00	00	8086	35b0	0	Intel Corporation 3100 Chipset Memory I/O Controller Hub	Host Bridge
00	00	8086	35b1	1	Intel Corporation 3100 DRAM Controller Error Reporting Registers	Class ff00
00	01	8086	35b5	0	Intel Corporation 3100 Chipset Enhanced DMA Controller	System Peripheral
00	02	8086	35b6	0	Intel Corporation 3100 Chipset PCI Express Port A	PCI Bridge
00	03	8086	35b7	0	Intel Corporation 3100 Chipset PCI Express Port A1	PCI Bridge
00	1c	8086	2690	0	Intel Corporation 3100 Chipset PCI Express Root Port 1	PCI Bridge
00	1c	8086	2692	1	Intel Corporation 3100 Chipset PCI Express Root Port 2	PCI Bridge
00	1c	8086	2694	2	Intel Corporation 3100 Chipset PCI Express Root Port 3	PCI Bridge
00	1c	8086	2696	3	Intel Corporation 3100 Chipset PCI Express Root Port 4	PCI Bridge
00	1d	8086	2688	0	Intel Corporation 3100 Chipset UHCI USB Controller #1	USB Conteoller
00	1d	8086	2689	1	Intel Corporation 3100 Chipset UHCI USB Controller #2	USB Conteoller
00	1d	8086	268c	7	Intel Corporation 3100 Chipset EHCI USB2 Controller	USB Conteoller
00	1e	8086	244e	0	Intel Corporation 82801 PCI Bridge	PCI Bridge
00	1f	8086	2670	0	Intel Corporation 3100 Chipset LPC Interface Controller	ISA Bridge
00	1f	8086	269b	3	Intel Corporation 3100 Chipset SMBUS Controller	SMBus
02	00	8086	1060	0	Intel Corporation 82571EB Gigabit Ethernet Controller	Ethernet Controller
02	00	8086	1060	1	Intel Corporation 82571EB Gigabit Ethernet Controller	Ethernet Controller
03	00	1000	0056	0	LSI Logic / Symbios Logic SAS1064E PCI-Express Fusion-MPT SAS	SCSI Storage Controller
04	00	8086	105e	0	Intel Corporation 82571EB Gigabit Ethernet Controller	Ethernet Controller
04	00	8086	105e	1	Intel Corporation 82571EB Gigabit Ethernet Controller	Ethernet Controller

A.3.2 CPU Engine 1 & 2

BUS#	DEV#	V. ID	D. ID	Funct. #	Description	PCI Description
00	00	8086	35b0	0	Intel Corporation 3100 Chipset Memory I/O Controller Hub	Host Bridge
00	00	8086	35b1	1	Intel Corporation 3100 DRAM Controller Error Reporting Registers	Class ff00
00	01	8086	35b5	0	Intel Corporation 3100 Chipset Enhanced DMA Controller	System Peripheral
00	02	8086	35b6	0	Intel Corporation 3100 Chipset PCI Express Port A	PCI Bridge
00	03	8086	35b7	0	Intel Corporation 3100 Chipset PCI Express Port A1	PCI Bridge
00	1c	8086	2690	0	Intel Corporation 3100 Chipset PCI Express Root Port 1	PCI Bridge
00	1c	8086	2692	1	Intel Corporation 3100 Chipset PCI Express Root Port 2	PCI Bridge
00	1c	8086	2694	2	Intel Corporation 3100 Chipset PCI Express Root Port 3	PCI Bridge
00	1c	8086	2696	3	Intel Corporation 3100 Chipset PCI Express Root Port 4	PCI Bridge
00	1d	8086	2688	0	Intel Corporation 3100 Chipset UHCI USB Controller #1	USB Conteoller
00	1d	8086	2689	1	Intel Corporation 3100 Chipset UHCI USB Controller #2	USB Conteoller
00	1d	8086	268c	7	Intel Corporation 3100 Chipset EHCI USB2 Controller	USB Conteoller
00	1e	8086	244e	0	Intel Corporation 82801 PCI Bridge	PCI Bridge
00	1f	8086	2670	0	Intel Corporation 3100 Chipset LPC Interface Controller	ISA Bridge
00	1f	8086	269b	3	Intel Corporation 3100 Chipset SMBUS Controller	SMBus
02	00	8086	1060	0	Intel Corporation 82571EB Gigabit Ethernet Controller	Ethernet Controller
02	00	8086	1060	1	Intel Corporation 82571EB Gigabit Ethernet Controller	Ethernet Controller

B. Kontron Extension Registers

B.1 FPGA/CPLD Registers Definition

Unused bits are reserved. To insure compatibility with other product and upgrades to this product, do not modify unused bits. Bits marked NU are not used on this board. Writing to such bit does nothing and reading is undefined, either 0 or 1 may be returned.

Legend:

Symbol	Signification
U	Unchanged (stay unchanged after reset)
X	Not Defined (bit not used on this board)
NU	Not Used
NA	Not Applicable

B.2 L7400 Addressing Space

The following ranges will be used on Kontron Canada AdvancedTCA boards:

- I/O 0080-0081hfor 16-bit postcodes
- I/O 0200-020Fhto reserve permanently 32 locations in I/O space for on-board resources
- I/O 0378-037Ahhidden legacy LPT port for Xilinx JTAG programmer

Not all those I/O locations are used, but the LPC bridge will answer the cycle in zero wait-state.

B.2.1 Summary of On-board Registers

Those registers are physically implemented in the AT8030 FPGA.

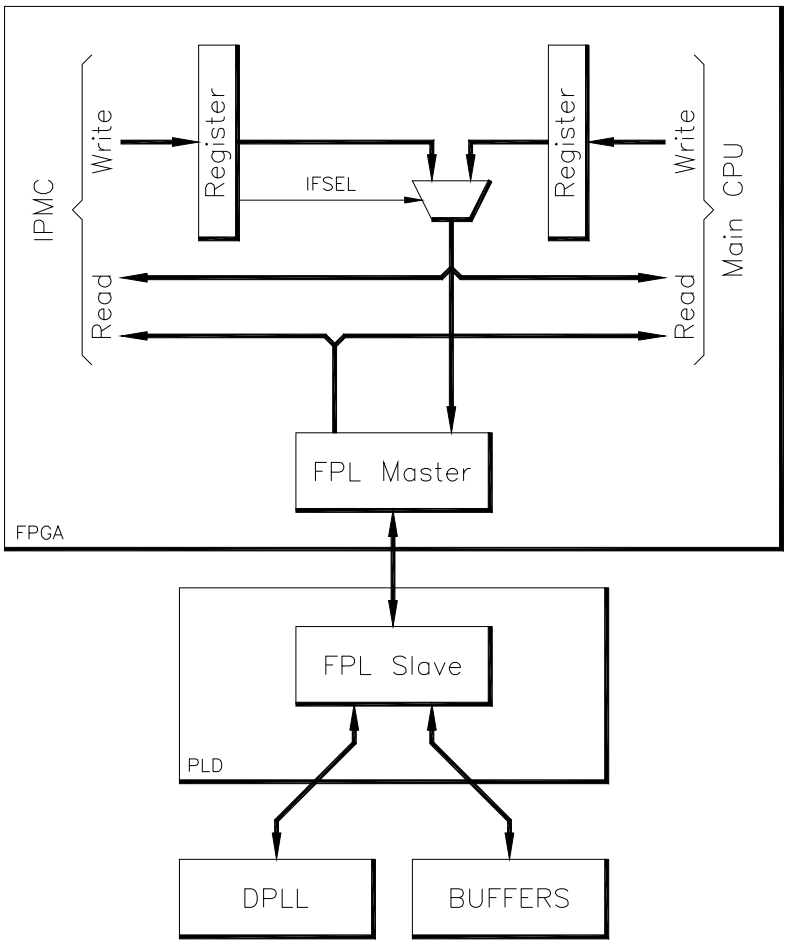
Address	Function
80-81h	
378-37Ah*	
600-7FFh	

* in case of hardware conflict, possible alternate addresses are:

- LPT1: 378-37Ah
- LPT2: 278-27Ah
- LPT3: 3BC-3BFh

B.3 IPMC/LPC Addressing Space

This function has a dual interface. At all time, all statuses are readable by the IPMC and by the main processor.



Only one side can write into the interface. Bit "IFSEL" is used to select which processor can write to the interface. Bit "IFSEL" is part of the interface, all processors can read its status but only the IPMC can write into it.

With the exception of bit "IFSEL" and the "Event & Alarm" register, both sides of the interface are identical.

B.3.1 Registers Summary

Offset	Function
00h	TelClock0: Backplane Clock Status & Interface select
01h	TelClock1: DPLL control & status
02h	TelClock2: AMCs Clock Enables & Frequency select
03h	TelClock3: PLD configuration & version
04h	TelClock4: Backplane CLK3 configuration
05h	TelClock5: Events and Alarms (IPMC side only)

B.3.2 Base+00h TelClock0: Backplane Clock Status, PLL Reference & Interface Selection

Offset	Action	D7	D6	D5	D4	D3	D2	D1	D0
00h	Read	IFSEL	MAN	SEL_REFA	BP_REF	CLK2B	CLK2A	CLK1B	CLK1A
	Write	IFSEL*	MAN	SEL_REFM	BP_REF	NU	NU	NU	NU
	PowerUp	0	0	0	0	NA	NA	NA	NA

CLK1A/B

CLK2A/B Coarse monitoring status. A 1 indicate that the corresponding backplane clock is present. A 0, that it is absent. Those statuses are valid only if CLK1A/B is 8kHz and CLK2A/B is 19.44MHz. If other frequencies are used, those bits should be ignored.

BP_REF Backplane set of clock to connect to the PLL.

0: Use backplane CLK1A and CLK1B (8kHz)

1: Use backplane CLK2A and CLK2B (19.44MHz)

SEL_REFA (read)

SEL_REFM (write) On a read, return the reference automatically selected by the PLD:

0: REF0 is the reference used by the PLL (i.e. CLKA).

1: REF1 is the reference used by the PLL (i.e. CLKB).

When bit MAN=1, the application software can select the reference by writting the desired value in this bit. This bit is not writtable when MAN=0. Note that on a read, this bit return the automatic selection even if MAN=1.

MAN 0: The PLD choose automatically the reference use by the DPLL (CLKA or B).

1: Selection of the DPLL reference is manual. Write the selection in bit SEL_REF.

IFSEL — Interface selection. This bit is always writable from the IPMC side but on the LPC side, the CPU can only read it.

1: IPMC has write control of the interface.

0: Main CPU (LPC) has write control of the interface

* bit IFSEL is writable only on the IPMC side of the interface.

B.3.3 Base+01h TelClock1: PLL Control & Status

Offset	Action	D7	D6	D5	D4	D3	D2	D1	D0
01h	Read	LOCK	FAIL1	FAIL0		TIE_CLR#	MODE	RESET	OOR
	Write					TIE_CLR#	MODE	RESET	OOR
	*					1	1	0	0

* power up and lpc reset

OOR — Out-Of-Range selection. Determine what is considered a precision fault by the PLL.

1: 64 - 83ppm.

0: 40 - 52ppm.

RESET — Hardware reset of the PLL. This bit is forced to '1' when the payload power (i.e. PLL power) is turned off.

1: reset

0: normal operation

MODE — PLL operating mode.

1: freerun mode (may be used for tests).

0: normal mode.

TIE_CLR# — Timing-Interval-Error adjustment.

1: normal mode.

0: adjust phase to match reference.

FAIL0 — REF0 (CLK2A) failed with current OOR setting.

1: failed clock.

0: passed clock.

FAIL1	REF1 (CLK2B) failed with current OOR setting. Same as FAIL0 but for REF1.
LOCK	PLL lock status. 1: PLL locked 0: PLL not locked (PLL in holdover or free running)

Note that this register needs to be reprogrammed every time the blade is reset. Those are direct pin control and status. See the ZL30108 datasheet for a detailed explanation of the functionality.

B.3.4 Base+02h TelClock2: AMCs Clock Enables & Frequency Selection

Offset	Action	D7	D6	D5	D4	D3	D2	D1	D0
02h	Read	B2TCF	B2TAF	B2TCEN	B2TAEN	B1TCF	B1TAF	B1TCEN	B1TAEN
	Write	B2TCF	B2TAF	B2TCEN	B2TAEN	B1TCF	B1TAF	B1TCEN	B1TAEN
	PowerUp	0	0	0*	0*	0	0	0*	0*

* also forced to 0 when the corresponding AMC is in fault or extracted

B1TAEN	AMC-B1 TCLKA Enable 1: drive AMC-B1 clock TCLKA 0: don't drive AMC-B1 TCLKA
B1TCEN	AMC-B1 TCLKC Enable 1: drive AMC-B1 clock TCLKC 0: don't drive AMC-B1 TCLKC
B1TAF	AMC-B1 TCLKA Frequency 1: use 8kHz frame pulse from PLL 0: use 19.44MHz from PLL
B1TCF	AMC-B1 TCLKC Frequency 1: use 8kHz frame pulse from PLL 0: use 19.44MHz from PLL
B2*	Reserved for AMC-B2 (for boards that have two AMCs).

Note about the 8kHz frequency. If the clock source of the PLL is 19.44MHz, the phase of this clock is unrelated to any other 8kHz clock in the system.

Also note that the AMC has to be present and fully powered for the enable bits to be settable. On a surprise extraction (user doesn't wait for the blue LED), the hardware automatically clears bits B1TCEN and B1TAEN in case a user would extract and re-insert immediatly the AMC.

B.3.5 Base+03h TelcoClock3: PLD Configuration & Version

Offset	Action	D7	D6	D5	D4	D3	D2	D1	D0
03h	Read	PLD_CONFIG				PLD_VERSION			
	Write								
	PowerUp								

PLD_CONFIG — Circuit configuration that the PLD expect. For the interface and circuit described in this document, this field is always 0000.

PLD_VERSION — Code version of the PLD for the above configuration. Currently 0000.

Note that if the PLD is absent or not programmed, this register will return FFh.

B.3.6 Base+04h TelcoClock4: Backplane CLK3A/B configuration (optional)

Offset	Action	D7	D6	D5	D4	D3	D2	D1	D0
04h	Read					CLK3AMC	CLK3FRQ	CLK3BE	CLK3AE
	Write					CLK3AMC	CLK3FRQ	CLK3BE	CLK3AE
	PowerUp					0	0	0	0

CLK3AE — Backplane CLK3A Enable.

0: don't drive this clock

1: drive this clock

CLK3BE — Same as CLK3AE but for CLK3B.

CLK3FRQ0 — Backplane CLK3A frequency.

0: copy AMC TCLKB to backplane CLK3A/B

1: copy AMC TCLKD to backplane CLK3A/B

CLK3AMC	Reserved for selection of the AMC that provides the clock for backplane CLK3A/B. Applicable to boards with two AMCs. 0: use AMC-B1 1: use AMC-B2

This register may be removed as well as the corresponding CLK3 buffer if the customer has no need to drive the backplane CLK3A/B.

Note that the FPGA will automatically clear bits CLK3BE and CLK3AE when the AMC is removed since the clock source is not valid anymore.

C. Connector Pinouts

C.1 Connectors and Headers Summary

Connector	Description
J5	Serial Port
J6 & J7	Ethernet
J10, J15, J16 & J17	USB Port
J20	Telco Clock I/O
J23	AdvancedTCA I/O
J30	RTM I/O
B1	AMC B1
P10	Power

C.2 Serial Port(J5)

Signal	Pin		Pin	Signal
RTS*	1		5	GND
DTR*	2		6	RX#
TX#	3		7	DSR**
GND	4		8	CTS**

* Driven Active but Not Used

** Not Used

C.3 Ethernet(J6 & J7)

Signal	Pin		Pin	Signal
TX+	1		5	N.C.
TX-	2		6	RX-
RX+	3		7	N.C.
N.C.	4		8	N.C.

C.4 USB Port (J10, J15, J16 & J17)

Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4

C.5 Telco Clock (J20)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	CLK1A+	CLK1A-	CLK1B+	CLK1B-	CLK2A+	CLK2A-
2	Tx4(UP)+	Tx4(UP)-	Rx4(UP)+	Rx4(UP)-	CLK3A+	CLK3A-
3	Tx2(UP)+(N.C.)	Tx2(UP)-(N.C.)	Rx2(UP)+(N.C.)	Rx2(UP)-(N.C.)	Tx3(UP)+	Tx3(UP)-
4	Tx0(UP)+	Tx0(UP)-	Rx0(UP)+	Rx0(UP)-	Tx1(UP)+(N.C.)	Tx1(UP)-(N.C.)
5	Tx2[15]+(N.C.)	Tx2[15]-(N.C.)	Rx2[15]+(N.C.)	Rx2[15]-(N.C.)	Tx3[15]+(N.C.)	Tx3[15]-(N.C.)
6	Tx0[15]+	Tx0[15]-	Rx0[15]+	Rx0[15]-	Tx1[15]+(N.C.)	Tx1[15]-(N.C.)
7	Tx2[14]+(N.C.)	Tx2[14]-(N.C.)	Rx2[14]+(N.C.)	Rx2[14]-(N.C.)	Tx3[14]+(N.C.)	Tx3[14]-(N.C.)
8	Tx0[14]+	Tx0[14]-	Rx0[14]+	Rx0[14]-	Tx1[14]+(N.C.)	Tx1[14]-(N.C.)
9	Tx2[13]+(N.C.)	Tx2[13]-(N.C.)	Rx2[13]+(N.C.)	Rx2[13]-(N.C.)	Tx3[13]+(N.C.)	Tx3[13]-(N.C.)
10	Tx0[13]+	Tx0[13]-	Rx0[13]+	Rx0[13]-	Tx1[13]+(N.C.)	Tx1[13]-(N.C.)

Pin	ROW G	ROW H	ROW AB	ROW CD	ROW EF	ROW GH
1	CLK2B+	CLK2B-	GND	GND	GND	GND
2	CLK3B+	CLK3B-	GND	GND	GND	GND
3	Rx3(UP)+	Rx3(UP)-	GND	GND	GND	GND
4	Rx1(UP)+(N.C.)	Rx1(UP)-(N.C.)	GND	GND	GND	GND
5	Rx3[15]+(N.C.)	Rx3[15]-(N.C.)	GND	GND	GND	GND
6	Rx1[15]+(N.C.)	Rx1[15]-(N.C.)	GND	GND	GND	GND
7	Rx3[14]+(N.C.)	Rx3[14]-(N.C.)	GND	GND	GND	GND
8	Rx1[14]+(N.C.)	Rx1[14]-(N.C.)	GND	GND	GND	GND
9	Rx3[13]+(N.C.)	Rx3[13]-(N.C.)	GND	GND	GND	GND
10	Rx1[13]+(N.C.)	Rx1[13]-(N.C.)	GND	GND	GND	GND

C.6 AdvancedTCA I/O AdvancedTCA 3.1 (J23)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	Tx2[2]+	Tx2[2]-	Rx2[2]+	Rx2[2]-	Tx3[2]+	Tx3[2]-
2	Tx0[2]+	Tx0[2]-	Rx0[2]+	Rx0[2]-	Tx1[2]+	Tx1[2]-
3	Tx2[1]+	Tx2[1]-	Rx2[1]+	Rx2[1]-	Tx3[1]+	Tx3[1]-
4	Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-
5	BI_DA1+	BI_DA1-	BI_DB1+	BI_DB1-	BI_DC1+	BI_DC1-
6	BI_DA2+	DI_DA2-	BI_DB2+	BI_DB2-	DI_DC2+	BI_DC2-
7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
8	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
9	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
10	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.

Pin	ROW G	ROW H	ROW AB	ROW CD	ROW EF	ROW GH
1	Rx3[2]+	Rx3[2]-	GND	GND	GND	GND
2	Rx1[2]+	Rx1[2]-	GND	GND	GND	GND
3	Rx3[1]+	Rx3[1]-	GND	GND	GND	GND
4	Rx1[1]+	Rx1[1]-	GND	GND	GND	GND
5	BI_DD1+	BI_DD1-	GND	GND	GND	GND
6	BI_DD2+	DI_DD2-	GND	GND	GND	GND
7	N.C.	N.C.	GND	GND	GND	GND
8	N.C.	N.C.	GND	GND	GND	GND
9	N.C.	N.C.	GND	GND	GND	GND
10	N.C.	N.C.	GND	GND	GND	GND

C.7 AdvancedTCA I/O RTM Connector (J30)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	V_12V_1	V_12V_5	V_12V_2	V_3V3_SUS	Reserved	RTM_PRSNT#
2	V_12V_3	V_12V_6	V_12V_4	N.C.	IPMC_SCL	IPMC_SDA
3	SP0_TX	SP0_RX	JTAG_TD1	JTAG_TDO	JTAG_TMS	JTAG_TCK
4	Reserved	Reserved	INT_0#	INT_1#	RTML_TX	RTML_RX
5	SP1_TX	SP1_RX	SP2_TX	SP2_RX	SP3_TX	SP3_RX
6	SP5_TX	SP5_RX	SP6_TX	SP6_RX	SP7_TX	SP7_RX
7	Reserved	Reserved	Reserved	N.C.	RESET_CPU0#	RESET_CPU1#
8	PQ3_FE_TX+	PQ3_FE_TX-	PQ3_FE_RX+	PQ3_FE_RX-	PQ3_FE_CTR	N.C.
9	SAS0_TX+	SAS0_TX-	SAS0_RX+	SAS0_RX-	SAS1_TX+	SAS_TX-
10	GE18_TXC+	GE18_TXC-	GE18_RXC+	GE18_RXC-	GE15_TXC+	GE15_TXC-

Pin	ROW G	ROW H	ROW AB	ROW CD	ROW EF	ROW GH
1	N.C.	RTM_ENABLE#	GND	GND	GND	GND
2	USB_D+	USB_D-	GND	GND	GND	GND
3	JTAG_TRST	N.C.	GND	GND	GND	GND
4	RTML_CLK	RESET/PROG	GND	GND	GND	GND
5	SP4_TX	SP4_RX	GND	GND	GND	GND
6	SFP_SCL	SFP_SDA	GND	GND	GND	GND
7	RESET_CPU2#	RESET_PQ3#	GND	GND	GND	GND
8	N.C.	N.C.	GND	GND	GND	GND
9	SAS1_RX+	SAS1_RX-	GND	GND	GND	GND
10	GE15_RXC+	GE15_RXC-	GND	GND	GND	GND

C.7.1 ATCA I/O RTM Intelligent Managed FRU Port Mapping

	A	B	C	D	E	F	G	H
Ch10	NU	NU	NU	NU	1000BX_TX2+(in)	1000BX_TX2-(in)	1000BX_RX2+(out)	1000BX_RX2-(out)
					Port 1*			
Ch9	SAS_0_TX+(in)	SAS_0_TX-(in)	SAS_0_RX+(out)	SAS_0_RX-(out)	SAS_1_TX+(in)	SAS_1_TX-(in)	SAS_1_RX+(out)	SAS_1_RX-(out)
	Port 2*				Port 2*			
Ch8	100BASE_TX+	100BASE_TX-	100BASE_RX+	100BASE_RX-	100BASE_CT	NC	NC	NC
	Port 5*							
Ch7	Reserved	Reserved	Reserved	Reserved	RESET_0#	RESET_1#	RESET_2#	RESET_3#
Ch6	RS232_5_TX	RS232_5_RX	RS232_6_TX	RS232_6_RX	RS232_7_TX	RS232_7_RX	UC_SCL	UC_SDA
	Port 17* / RTM:SP5***		Port 18* / RTM:SP6***		Port 19* / RTM:SP7***			
Ch5	RS232_1_TX	RS232_1_RX	RS232_2_TX	RS232_2_RX	RS232_3_TX	RS232_3_TX	RS232_4_TX	RS232_4_RX
	Port 13* / RTM:SP1***		Port 14* / RTM:SP2***		Port 15* / RTM:SP3***		Port 16* / RTM:SP4***	
Ch4	Reserved	Reserved	INT0	INT1	RTML_TX	RTML_RX	RTML_CLK	RESET/PROG
Ch3	RS232_0_TX	RS232_0_RX	JTAG_TDI(out)	JTAG_TDO(in)	RTM_TMS(out)	RTM_TCK(out)	RTM_TRST#(out)	NC
	Port 12* / RTM:SP0**							
Ch2	12V (in)	12V (in)	12V (in)	NC	MMC_SCL (in)	MMS_SDA (out)	USB_D+ (io)	USB_D- (io)
							Port 20*	
Ch1	12V (in)	12V (in)	12V (in)	3V3_SUS (in)	Reserved	RTM_PRNT# (out)	NC	RTM_EN# (in)

In - Input, driven by Carrier

Out- Output, driven by RTM

IO - Bidirectional

* port ID for carrier p2p connectivity information (see AMC.0 Rev2 section 3.9.1)

** connected to separate RJ45 connector on RTM

*** connection selected by rotary switch

In order to support 'ekey governed' interfaces on the RTM, AMC style port mapping is necessary.

For consistency with AMC.2 and AMC.3 , SAS and GbE port numbers have been assigned to 'standard' port numbers.

OEM links that require physical interconnects on the carrier (RS232 and SOC) have been assigned port numbers in the extended option region.

C.8 AMC B1 (B1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B1	GND	B43	GND	B86	GND	B129	TxD15-
B2	12V	B44	RxD4+	B87	TxD8-	B130	TxD15+
B3	PS1#	B45	RxD4-	B88	TxD8+	B131	GND
B4	MP_3V3	B46	GND	B89	GND	B132	RxD15-
B5	GA0	B47	TxD4+	B90	RxD8-	B133	RxD15+
B6	RSV	B48	TxD4-	B91	RxD8+	B134	GND
B7	GND	B49	GND	B92	GND	B135	TxD16-
B8	RSV	B50	RxD5+	B93	TxD9-	B136	TxD16+
B9	12V	B51	RxD5-	B94	TxD9+	B137	GND
B10	GND	B52	GND	B95	GND	B138	RxD16-
B11	RxD0+	B53	TxD5+	B96	RxD9-	B139	RxD16+
B12	RxD0-	B54	TxD5-	B97	RxD9+	B140	GND
B13	GND	B55	GND	B98	GND	B141	TxD17-
B14	TxD0+	B56	IPMB-L-SCL	B99	TxD10-	B142	TxD17+
B15	TxD0-	B57	12V	B100	TxD10+	B143	GND
B16	GND	B58	GND	B101	GND	B144	RxD17-
B17	GA1	B59	RxD6+	B102	RxD10-	B145	RxD17+
B18	12V	B60	RxD6-	B103	RxD10+	B146	GND
B19	GND	B61	GND	B104	GND	B147	TxD18-
B20	RxD1+	B62	TxD6+	B105	TxD11-	B148	TxD18+
B21	RxD1-	B63	TxD6-	B106	TxD11+	B149	GND
B22	GND	B64	GND	B107	GND	B150	RxD18-
B23	TxD1+	B65	RxD7+	B108	RxD11-	B151	RxD18+
B24	TxD1-	B66	RxD7-	B109	RxD11+	B152	GND
B25	GND	B67	GND	B110	GND	B153	TxD19-
B26	GA2	B68	TxD7+	B111	TxD12-	B154	TxD19+
B27	12V	B69	TxD7-	B112	TxD12+	B155	GND
B28	GND	B70	GND	B113	GND	B156	RxD19-
B29	RxD2+	B71	IPMB_SDA	B114	RxD12-	B157	RxD19+
B30	RxD2-	B72	12V	B115	RxD12+	B158	GND
B31	GND	B73	GND	B116	GND	B159	TxD20-
B32	TxD2+	B74	CLK1+	B117	TxD13-	B160	TxD20+
B33	TxD2-	B75	CLK1-	B118	TxD13+	B161	GND
B34	GND	B76	GND	B119	GND	B162	RxD20-
B35	RxD3+	B77	CLK2+	B120	RxD13-	B163	RxD20+
B36	RxD3-	B78	CLK2-	B121	RxD13+	B164	GND
B37	GND	B79	GND	B122	GND	B165	TCLK
B38	TxD3+	B80	CLK3+	B123	TxD14-	B166	TMS
B39	TxD3-	B81	CLK3-	B124	TxD14+	B167	TRST#

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
B40	GND	B82	GND	B125	GND	B168	TDO
B41	ENABLE#	B83	PS0#(GND)	B126	RxD14-	B169	TDI
B42	12V	B84	12V	B127	RxD14+	B170	GND
		B85	GND	B128	GND		

C.9 Power (P10)

Signal	Pin		Pin	Signal
N.P.	1		2	N.P.
N.P.	3		4	N.P.
HA0	5		6	HA1
HA2	7		8	HA3
HA4	9		10	HA5
HA6	11		12	HA7/P
IPMBA_SCL	13		14	SDA_A
SCL_B	15		16	SDA_B
N.C.	17		18	N.C.
N.C.	19		20	N.C.
N.C.	21		22	N.C.
N.C.	23		24	N.C.
SHELF_GND	25		26	LOGIC_GND
ENABLE_B	27		28	VRTN_A
VRTN_B	29		30	EARLY_A
EARLY_B	31		32	ENABLE_A
-48V_A	33		34	-48V_B

D. BIOS Setup Error Codes

D.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waiking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information.
E1-E8	
EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next. Refer to memory initialization ERROR CODE D.5

D.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O (if present). Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from media.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

D.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."

Checkpoint	Description
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.

Checkpoint	Description
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).
61-70	OEM POST Error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.
DD-DE	OEM PCI init debug POST code during DIMM init, See DIM Code Checkpoints section of document for more information.

D.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 CONFIGURES all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.
DD-DE	OEM PCI init debug POST code during DIMM init. DEh during BUS number assignment and DDh during ressource allocation, Hight byte is the BUS number.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.

1 = func#1, static devices initialization on the BUS concerned.

2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.

4 = func#4, IPL device initialization on the BUS concerned.

5 = func#5, general device initialization on the BUS concerned.

6 = func#6, error reporting for the BUS concerned.

7 = func#7, add-on ROM initialization for all BUSes.

8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).

1 = On-board System devices.

2 = ISA devices.

3 = EISA devices.

4 = ISA PnP devices.

5 = PCI devices.

D.5 Memory Initialization ERROR Code

Checkpoint	Description
E1h	Memory Error - No memory installed.
E3h	Memory Error - Unsupported DIMM type.
EAh	Memory Error - Memory timing error
EEh	Memory Error - Memory unsupported size.
EFh	Memory Error - Memory population order.
F3h	Memory Error - Error code for unsuccessful Memory Test.
F4h	Memory Error - Error code for unsuccessful ECC and Memory Initialization
F5h	Memory Error - Receive enable is busted so halt here

E. Software Update

E.1 IPMC/MMC Firmware Update Procedure

It is important to use compatible BIOS, IPMC/MMC, FPGA and U-BOOT (switch) versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade.

The current version of the IPMC firmware can be retrieved from the BIOS Setup IPMI Menu or using IPMITOOL, through HPM.1 functionalities.

The upgrade of the firmware is also done using HPM.1 functionalities of IPMITOOL. The upgrade can be done through any IPMI interface and is designed to be without payload impact.

Kontron recommends to use it's update CD to upgrade the firmware. To obtain the update CD, contact Kontron technical support department.

E.2 Updating AT8030 BIOS

The AMI Linux upgrade utility is used to upgrade the BIOS.

Please note that you'll have to reboot in order to take advantage of the new BIOS.

It is important to use compatible BIOS, IPMC and FPGA versions. Since all these software and hardware solution are exchanging information, they must be in synch. Please always follow Kontron documentation for all your upgrade. Kontron recommand to use it's update CD to upgrade the BIOS. To obtain the update CD, contact Kontron technical support department.

The recommended upgrade sequence must be: FPGA, IPMC, BIOS.

To read the actual version of FPGA and IPMC use the IPMITOOL tool. The BIOS version is written at every boot during BIOS POST, you can also get it by entering BIOS Setup Menu. The BIOS Setup does also provide the IPMC firmware version, via the IPMI Menu.

Type the following:

afulnx2 /i<BIOS_BIN_File_Name> /pbnc <enter>

(no space between /i and the filename)

/pbnc is for

b - Program Boot Block

n - Program NVRAM

c - Destroy System CMOS

After the upgrade process is completed, reboot by typing

Ctrl-alt-del keys

During BIOS POST, enter BIOS Setup Menu by typing

Del key

In BIOS Setup Menu, make sure to select BIOS Optimal Default Settings by typing F9 key

E.3 Updating the switch

The following procedure describes the firmware update of the board

1 Prepare network access of the board (see previous chapters)

2 Log in to the privileged exec mode of the CLI of the board

3 Check availability of valid boot image in slot 1 using the command

```
(Ethernet Fabric) #show bootvar
```

4 Copy new correct image (for example initrd2.pkg) into slot 2 using the CLI command

```
(Ethernet Fabric) #copy tftp://<IP_address>/initrd2.pkg image2
```

5 Select the second boot image to be used for next boot with the command:

```
(Ethernet Fabric) #boot system image2
```

6 Reboot system

```
(Ethernet Fabric) #reload
```

7 System will start using image 2. Check with

```
(Ethernet Fabric) #show bootvar
```

8 In case of having updated with a corrupted image, the AT8030 should try to boot twice the corrupted image and for the third time boot it should recover to image 1 to boot the system. Check with

```
(Ethernet Fabric) #show bootvar
```

F. Supported RFCs and MIBs

F.1 Supported RFCs

The Software supports the following standards and RFCs.

F.1.1 Management

- RFC 826 - ARP
- RFC 854 - Telnet
- RFC 855 - Telnet Option
- RFC 1155 - SMI v1
- RFC 1157 - SNMP
- RFC 1212 - Concise MIB Definitions
- RFC 1867 - HTML/2.0 Forms w/ file upload extensions
- RFC 1901 - Community based SNMP v2
- RFC 2068 - HTTP/1.1 protocol as updated by draft-ietf-http-v11-spec-rev-03
- RFC 2246 - The TLS Protocol, Version 1.0
- RFC 2271 - SNMP Framework MIB
- RFC 2295 - Transparent Content Negotiation
- RFC 2296 - Remote Variant Selection; RSVA/1.0 State Management "cookies"
- RFC 2346 - AES Ciphersuites for Transport Layer Security
- RFC 2576 - Coexistence between SNMP v1,v2 & v3
- RFC 2578 - SMI v2
- RFC 2579 - Textual Conventions for SMI v2
- RFC 2580 - Conformance statements for SMI v2
- RFC 2818 - HTTP over TLS
- RFC 3410 - (Informational): Introduction and Applicability Statements for Internet Standard
- Management Framework (December 2002)
- RFC 3411 - An Architecture for Describing SNMP Management Frameworks (December 2002)

- RFC 3412 - Message Processing and Dispatching (December 2002)
- RFC 3413 - SNMP Applications (December 2002)
- RFC 3414 - User-based Security Model (December 2002)
- RFC 3415 - View-based Access Control Model (December 2002)
- RFC 3416 - Version 2 of SNMP Protocol Operations (December 2002)
- RFC 3417 - Transport Mappings (December 2002)
- RFC 3418 - Management Information Base (MIB) for the Simple Network Management Protocol (SNMP) (December 2002).
- RFC 3635 Definition of Managed Objects for Ethernet-like Interface Types
- HTML 4.0 Specification - December, 1997
- Java & Java Script 1.3
- SSL 3.0 & TLS 1.0
- SSH 1.5 & 2.0
- Draft-ietf-secsh-transport-16 - SSH Transport Layer Protocol
- Draft-ietf-secsh-userauth-17 - SSH Authentication Protocol
- Draft-ietf-secsh-connect-17 - SSH Connection Protocol
- Draft-ietf-secsh-architecture-14 - SSH Protocol Architecture
- Draft-ietf-secsh-publickeyfile-03 - SECSH Public Key File Format
- Draft-ietf-secsh-dh-group-exchange-04 - Diffie-Hellman Group exchange for the SSH Transport Layer Protocol
- Configurable Management VLAN ID
- Industry Standard CLI

F.1.2 Switching

- IEEE 802.3ac - VLAN Tagging
- IEEE 802.3ad - Link Aggregation with Static LAG and LACP support
- IEEE 802.1S - Multiple Spanning Tree
- IEEE 802.1W - Rapid Spanning Tree
- IEEE 802.1D - Spanning Tree
- GARP

- GVRP - Dynamic VLAN Registration
- GMRP - Dynamic L2 Multicast Registration
- IEEE 802.1Q - Virtual LANs with Port Based VLANs
- IEEE 802.1v - Protocol based VLANs
- IEEE 802.1p - Ethernet Priority with User Provisioning & Mapping
- IEEE 802.1X - Port Authentication
- IEEE 802.3x - Flow Control
- IGMP Snooping
- Port Mirroring
- Broadcast Storm Recovery
- Static MAC Filtering
- Double VLAN / vMAN Tagging
- Jumbo Frames
- IPv6 Classification APIs
- XMODEM
- RFC 768 - UDP
- RFC 783 - TFTP
- RFC 791 - IP
- RFC 792 - ICMP
- RFC 793 - TCP
- RFC 951 - BOOTP
- RFC 1321 - Message Digest Algorithm (MD5)
- RFC 1534 - Interoperation between BOOTP and DHCP
- RFC 2030 - Simple Network Time Protocol (SNTP) Version 4 for IPv4, IPv6 and OSI
- RFC 2131 - DHCP Client
- RFC 2131 - DHCP Server
- RFC 2132 - DHCP Options and BOOTP Vendor Extensions
- RFC 2865 - RADIUS Client

- RFC 2866 - RADIUS Accounting
- RFC 2868 - RADIUS Attributes for Tunnel Protocol Support
- RFC 2869 - RADIUS Extensions
- RFC2869bis - RADIUS support for EAP
- RFC 3176 - InMon Corporation's sFlow: A Method for Monitoring Traffic in Switched and Routed Networks
- RFC 3396 - Encoding Long Option in the Dynamic Host Configuration Protocol (DHCPv4)
- RFC 3580 - 802.1X RADIUS Usage Guidelines
- Draft-ietf-magma-snoop-11.txt - Considerations for IGMP and MLD Snooping Switches

F.1.3 QoS

- Bandwidth Policing (Min and Max; per port/per VLAN)
- Committed Information Rate (CIR)
- Maximum Burst Rate (MBR)
- Per Port (Interface)
- Per VLAN
- Filtering (L3/L4 Access Lists)
- IP Classification - 6 Tuple Classification
- RFC 2474 - DiffServ Definition
- RFC 2475 - DiffServ Architecture
- RFC 2597 - Assured Forwarding PHB
- RFC 3246 - An Expedited Forwarding PHB
- RFC 3260 - New Terminology and Clarifications for DiffServ

F.2 Supported MIBs

The Software supports the following MIBs.

F.2.1 Enterprise MIB

- Support for all managed objects not contained in standards based MIBs.

F.2.2 Switching Package MIBs

- RFC 1213 - MIB-II
- RFC 1493 - Bridge MIB
- RFC 1643 - Ethernet-like -MIB
- RFC 2233 - The Interfaces Group MIB using SMI v2
- RFC 2618 - RADIUS Authentication Client MIB
- RFC 2620 - RADIUS Accounting MIB
- RFC 2674 - VLAN & Ethernet Priority MIB
- RFC 2819 - RMON Groups 1,2,3 & 9
- RFC 2863 - Interfaces Group MIB
- RFC 3291 - Textual Conventions for Internet Network Addresses
- IANA-ifType-MIB
- IEEE 802.1X MIB (IEEE8021-PAE-MIB)
- IEEE 802.3AD MIB (IEEE8021-AD-MIB)

F.2.3 QoS Package MIB

- RFC 3289 - DIFFSERV-MIB & DIFFSERV-DCSP-TC MIBs

G. Bootloader

The bootloader initializes the Unit Computer and its associated components board like SDRAM, serial lines etc. for operation. After this, kernel and application are started from flash. In addition, the bootloader provides a user interface with commands to access the board's components. Networking functions are available to load and start alternative kernel and application files. A powerful, redundant environment gives the user the capabilities to tailor the bootloader's startup behaviour to his needs.

G.1 General Operation

Upon power on or system reset, the bootloader is started and the Ethernet Switch subsystem is initialized. In the case that the serial port is connected to a terminal and a predefined string is entered after the SDRAM test and within the bootdelay time - which is 5 seconds by default - the startup procedure is interrupted and the bootloader's command prompt is presented to the user. If the bootdelay time expires without user interaction, the start sequence proceeds with loading and starting the operating system from flash.

In case of having reset the bootstopkey the boot process can not be interrupted (see section "Setting the bootstopkey")

In the bootloader command prompt, enter 'boot' to continue the boot process.

G.2 Bootloader Commands

The user interface of the u-boot bootloader provides a set of powerful commands to the user. The following functional groups can be distinguished:

- Environment control
- Memory operations
- Flash operations
- PCI control
- Networking functions
- Application control
- Miscellaneous commands

All commands available are listed with a short description when entering the 'help' command:

```
=> help
?      - alias for 'help'
Base   - print or set address offset
Bdinfo - print Board Info structure
bootm  - boot application image from memory
bootp  - boot image via network using BootP/TFTP protocol
cmp    - memory compare
```

```
cp     - memory copy
crc32  - checksum calculation
echo   - echo args to console
erase  - erase FLASH memory
flinfo  - print FLASH memory information
go     - start application at address 'addr'
help   - print online help
iminfo  - print header information for application image
loop   - infinite loop on address range
md     - memory display
mii    - MII utility commands
mm     - memory modify (auto-incrementing)
mw     - memory write (fill)
nm     - memory modify (constant address)
pci    - list and access PCI Configuraton Space
ping   - send ICMP ECHO_REQUEST to network host
printenv- print environment variables
protect - enable or disable FLASH write protection
rarpboot- boot image via network using RARP/TFTP protocol
reset  - Perform RESET of the CPU
run    - run commands in an environment variable
saveenv - save environment variables to persistent storage
setenv - set environment variables
tftpboot- boot image via network using TFTP protocol
version - print monitor version
```

More detailed help is displayed when entering 'help [command]'

```
=> help mm
mm [.b, .w, .l] address- memory modify, auto increment address
```

Important commads are (ordered in functional groups):

CMD	Function	Remarks
printenv	Print current environment variables	
setenv	Set environment variable	
saveenv	Save environment variables to persistent storage	Normal and redundant environment are written alternately

Environment Control

CMD	Function	Remarks
md	Memory display	Command without parameters displays the next memory block
mm	Memory modify (auto-incrementing)	
nm	Memory modify (constant address)	
mw	Memory write (fill)	
cp	Memory cp	This command also works when copying from and to flash
cmp	Memory compare	
crc32	Checksum calculation	
loop	Infinite loop on address range	

Memory Operations

CMD	Function	Remarks
flinfo	Print FLASH memory information	
erase	Erase FLASH memory	
protect	Enable or disable FLASH write protection	

Flash operations

CMD	Function	Remarks
pci	Short or long list of PCI devices on specified bus	
pci header	Show header of PCI "bus.device.function	"
pci display	Display PCI configuration space (CFG)	
pci next	Modify, read and keep CFG address	
pci modify	Modify and auto increment CFG address	
pci write	Write to CFG address	

PCI

CMD	Function	Remarks
bootp	Boot image via network using BootP/TFTP protocol	
tftpboot	Boot image via network using TFTP protocol	
rarpboot	Boot image via network using RARP/TFTP protocol	
mii	MII utility commands	
ping	Send ICMP ECHO_REQUEST to network host	U-boot does not respond to ICMP echo requests

Networking functions

CMD	Function	Remarks
bootm	Boot application image from memory	This command is used to start the operating system
go	Start application at specified address	
iminfo	Print header information for application image	Kernel and ramdisk images for u-boot are preceded by a 64 byte header

Application Control

CMD	Function	Remarks
bdinfo	Print board info structure	A pointer to the board info structure is passed when starting the linux kernel
echo	Echo args to console	
reset	Perform RESET of the CPU	
run	run commands in an environment variable	
version	Print monitor version	

Miscellaneous Commands

G.3 Bootloader Environment

The u-boot environment is a set of variables that can be used to customize the bootloader's startup behaviour. The environment is stored in a sector of the flash memory and copied into RAM upon bootloader startup. It is possible to change environment variables using the 'setenv' command. Changes take place in the copy of the environment located in the RAM, they are stored permanently after using the 'saveenv' command.

To keep the integrity and availability of the bootloader's environment, two mechanisms are used:

"The set of environment variables in flash is protected by a CRC32 checksum. This prevents the bootloader from reading a corrupted environment in case a power failure occurs during the saveenv command.

"A redundant environment sector is used. When storing the environment using the saveenv command, the environment is written into the redundant sector. After this has been successfully completed, the redundant environment becomes the active one and will be used upon next system reset. In case of a power failure during the environment storage, only the new environment would be corrupted. It won't be set to be active and the old environment would be used. Only the latest environment changes would be lost.

Variable	Function
baudrate	Serial console baudrate
bootdelay	Delay before automatically booting the default image
bootargs	This can be used to pass arguments to the 'bootm' command and thus to the kernel started.
bootcmd	This defines a command string that is automatically executed when the boot stop string is not entered on the console interface within the 'bootdelay' time after reset.

Variable	Function
i2cfast	This configures the LINUX 12C driver for fast mode (400 kHz)
ethaddr	Ethernet MAC address. This variable is set once during manufacturing and cannot be changed afterwards
ipaddr	IP address of the board
loadaddr	Load address for network file downloads
serverip	IP address of a tftp/bootp server for network downloads
bootstopkey	This defines a boot stop string ('stop').
gatewayip	IP address of a gateway to a tftp/bootp server
netmask	Netmask of the subnet where the board lives
serial#	Contains hardware identification information such as type string and/or serial number. This variable cannot be changed.
pram	This variable gives the amount of RAM memory which is not used by u-boot. This is necessary because the linux kernel has to be started with reduced memory to leave some memory for DMA. If the bootloader would use the full memory, the ramdisk would be located at an address that linux could not access later.
stdin	This and and the following 2 variables are set to 'serial' automatically by the bootloader
stdout	
stderr	
bootcount	This variable holds the number of CPU resets without power loss
memtest	This variable controls the amount of the POST SDRAM testing. 0: No SDRAM testing is performed upon power up 1: Data and address bus testing is performed upon power up. In addition, a memory read/write test is performed for 64 kB blocks at each 1MB boundary (fast testing). 2: Data and address bus testing is performed upon power up. In addition, a complete memory read/write test is performed for the total amount of RAM (complete testing).
post_en	In the case this variable has been set - independent of its value - a Power On Self Test testing several onboard devices is performed upon reset. SDRAM POST is not affected by this variable.

Important environment variables

G.4 Setting the bootstopkey

The default setting for the bootstopkey is "stop".

To change the bootstopkey the CLI command:

```
>no set bootstopkey
```

must be used. This resets the bootstopkey and the boot process can not be interrupted.

The command:

```
>set bootstopkey
```

reinitiates the key "stop" as bootstopkey.

For additional information about the CLI, refer to the CLI Reference Manual.

H. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support-kom@kontron.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555, Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

H.1 Returning Defective Merchandise

Before returning any merchandise please do one of the following:

- Call

    1 Call our Technical Support department in North America at (450) 437-5682 and in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order #, and the Serial Number of the defective unit.

    2 Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.

    3 The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.

    4 Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- Fax

    1 Make a copy of the request form on the following page.

    2 Fill it out.

    3 Fax it to us at: North America (450) 437-0304, EMEA +49 (0) 8341 803 339

- E-mail

    1 Send us an e-mail at: RMA@ca.kontron.com in North America and at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

H.2 When Returning a Unit

- In the box, you must include the name and telephone number of a contact person, in case further explanations are required. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555, Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

Return to Manufacturer Authorization Request

Contact Name:	_____		
Company Name:	_____		
Street Address:	_____		
City:	_____	Province/State:	_____
Country:	_____	Postal/Zip Code:	_____
Phone Number:	_____	Extension:	_____
Fax Number:	_____	E-Mail:	_____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department
in North America at (450) 437-0304
in EMEA at +49 (0) 8341 803 339

I. Glossary

Acronyms	Descriptions
6HP	Horizontal Pitch (1 HP = .2 inches, an ATCA board is 6HP). Refers to width.
ACL	Access Control List. IP Access Control List.
ACPI	Advanced Configuration & Power Interface
ADC	Analog to Digital Converter
AdvancedMC	(Same as AMC). Advanced Mezzanine Card.
AER	Advanced Error Reporting. PCI Express device capability for more robust error reporting and is implemented with a specific PCI Express capability structure. See the PCI Express Base Specification.
AMC	(Same as AdvancedMC). Advanced Mezzanine Card.
AMC.0	Advanced Mezzanine Card Base Specification.
AMC.1	PCI Express and Advanced Switching on AdvancedMC. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.2	Ethernet Advanced Mezzanine Card Specification. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.3	Advanced Mezzanine Card Specification for Storage. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
ANSI	American National Standards Institute
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
APM	Advanced Power Management
ARMD	ATAPI Removable Media Device
ARP	Address Resolution Protocol
ASCII	American Standard Code for Information Interchange. ASCII codes represent text in computers, communications equipment, and other devices that work with text.
ASF	Alert Standard Format. A standard for how alerting and remote-control capabilities on network controllers work.
ATA	Advanced Technology Attachment
ATAPI	Advanced Technology Attachment Packet Interface
ATCA	Advanced Telecommunications Computing Architecture
ATX	Advanced Technology Extended. Form factor for computer case.
BBS	BIOS Boot Specification
BCD	Binary-Coded Decimal
BDA	BIOS Data Area
BER	Bit Error Ratio
BEV	Bootstrap Entry Vector
BI	Base Interface. Backplane connectivity defined by the ATCA.
BIOS	Basic Input/Output System
BIST	Built-in Self Test
BMC	Base Management Controller
BOM	Bill Of Material
BT	Block Transfer. An optional IPMI system management interface.
CAD	Computer-Aided Design

Acronyms	Descriptions
CB	Certification Body
CCB	Core Complex Bus (Inside PowerQuicc III CPU)
CD	Compact Disk
CDROM	(Same as CD-ROM). Compact Disk Read-Only Memory.
CD-ROM	(Same as CDROM). Compact Disk Read-Only Memory.
CFM	Cubic Foot per Minute
CISPR22	Comité International Spécial des Perturbations Radioélectriques publication 22. Special International Committee on Radio Interference publication 22.
CLI	Command-Line Interface
CLK1	AdvancedTCA bused resource Synch clock group 1
CLK1A	AdvancedTCA bused resource Synch clock group 1, bus A
CLK1B	AdvancedTCA bused resource Synch clock group 1, bus A
CLK2	AdvancedTCA bused resource Synch clock group 2
CLK2A	AdvancedTCA bused resource Synch clock group 2, bus A
CLK2B	AdvancedTCA bused resource Synch clock group 2, bus B
CLK3	AdvancedTCA bused resource Synch clock group 3
CLK3A	AdvancedTCA bused resource Synch clock group 3 , bus A
CLK3B	AdvancedTCA bused resource Synch clock group 3 , bus B
CMIC	CPU Management Interface Controller
CMOS	Complementary Metal Oxide Semiconductor. Also refers to the small amount of battery (or capacitor) powered CMOS memory to hold the date, time, and system setup parameters.
CMP	Core Multi-Processing
COP	Common On-chip Processor. Common on-chip processor function.
COTS	Commercial-Off-The-Shelf
CPCI	Compact PCI
CPLD	Complex Programmable Logic Device
CP-TA	Communications Platforms Trade Association
CPU	Central Processing Unit. This sometimes refers to a whole blade, not just a processor component.
CPUID	CPU IDentification. Code that uniquely identify a processor type.
CRC	Cyclic Redundancy Check
CS1	Components Side 1 as describes in PICMG3.0.
CS2	Components Side 1 as describes in PICMG3.0.
CTCA	Compact Telecom Computing Architecture
CTS	Clear To Send
DC	Direct Current
DCM	Daughter Card Mezzanine
DDR	DDR SDRAM or Double-Data-Rate
DDR2	(Same as DDR-II). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DDR-II	(Same as DDR2). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DED	Double-bit Error Detect or Double-symbol Error Detect.
DFTG	Design For Testability Guidelines

Acronyms	Descriptions
DHCP	Dynamic Host Configuration Protocol
DIMM	Dual In-line Memory Module
DIN	Deutsches Institut für Normung. German Institute for Standardization.
DMA	Direct Memory Access
DMI	Desktop Management Interface
DOS	Disk Operating System
DPLL	Digital Phase-Locked Loop
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processing
DTC	Data Transfer Controller
DTR	Data Terminal Ready
DTS	Digital Thermal Sensor in IA32 processors.
DUART	Dual Universal Asynchronous Receiver/Transmitter
DVD	Digital Video Disk
ECC	Error Checking and Correction
EDMA	Enhanced Direct Memory Access
EEPROM	Electrically Erasable Programmable Read-Only Memory
ECM	E500 Coherency Module.
EFI	Extensible Firmware Interface
EFT	Electric Fast Transient
EHCI	Enhanced Host Controller Interface. Specification for Universal Serial Bus specification, revision 2.0.
EIA	Electronic Industries Alliance
EISA	Extended Industry Standard Architecture. Superset of ISA, 32-bit bus architecture.
EIST	(Same as SpeedStep). Enhanced Intel SpeedStep Technology
EM64T	Extended Memory 64 Technology. Intel 64 is Intel's implementation of x86-64 used by 64-bit operating systems.
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMTTM	Turbo mode and enhanced Multi Threaded Thermal Management
EOL	End Of Life
EPS	Engineering Product Specification
ERM	Electromagnetic compatibility and Radio spectrum Matters
ES	Ethernet Switch
ESD	ElectroStatic Discharge
ESI	Enterprise South bridge Interface. Interface to the I/O legacy bridge component of the Intel ICHx.
ETH	Same as Ethernet.
ETSI	European Telecommunications Standards Institute
FADT	Fixed ACPI Description Table
FAT	File Allocation Table. Usually followed by a number, ex.: FAT32, which defines the number of bits used to address clusters on a disk.
FC	Fibre Channel
FCC	Federal Communications Commission

Acronyms	Descriptions
FCPGA	Flip-Chip Pin Grid Array
FCS	First Customer Shipment. Refers to Kontron scheduling for boards.
FC-AL	Fibre Channel-Arbitrated Loop
FDD	Floppy Disk Drive
FI	Fabric Interface. Backplane connectivity defined by the ATCA.
FIFO	First In First Out
FML	Fast Management Link
FPGA	Field-Programmable Gate Array
FPL	FPGA-to-PLD Link. FPL is a 20 MHz serial link that exchange 32-bit of data in each direction between the FPGA and a companion PLD.Kontron proprietary
FRBx	Fault-Resilient Booting level [1-3]. A term used to describe system features and algorithms that improve the likelihood of the detection of, and recovery from, processor failures in a multiprocessor system.
FRB2	Fault-Resilient Booting, Level 2.
FRT	Free-Running Timer
FRU	Field Replaceable Unit. Any entity that can be replaced by a user in the field. Not all FRUs are hot swappable.
FSB	Front Side Bus
FTP	File Transfer Protocol
FW	FirmWare
FWH	FirmWare Hub. Boot flash connected to the LPC bus containing BIOS FW.
GA	Geographic Address
GARP	Generic Attribute Registration Protocol
Gb	Gigabit
GB	(Same as GByte) GigaByte.
GByte	(Same as GB) GigaByte.
GbE	Gigabit Ethernet
GHz	GigaHertz
GMRP	GARP Multicast Registration Protocol
GND	GrouND
GPCM	General-Purpose Chip select Machine
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
GRUB	GRand Unified Bootloader
GUID	Globally Unique Identifier
GVRP	GARP VLAN Registration Protocol
HDD	Hard Disc Drive
HFM	High Frequency Mode. The highest operating speed for the processor.
HMS	Hardware Management System
HPM	PICMG Hardware Platform Management specification family
HPM.1	Hardware Platform Management IPM Controller Firmware Upgrade Specification
HW	HardWare

Acronyms	Descriptions
HWS	HardWare Specification
I2C	Inter Integrated Circuit bus
IA-32	(Same as IA32). Intel Architecture 32 bits
IA32	(Same as IA-32). Intel Architecture 32 bits
IBA	Intel Boot Agent
IC	Integrated Circuit
ICE	In-Circuit Emulator
ICH	I/O Controller Hub
ICT	In-Circuit Test
ID	IDentification
IDE	Integrated Drive Electronics
IEC	International Electrotechnical Commission
IICH	Integrated I/O Controller Hub. Sub-part of the MICH chipset.
IEEE	Institute of Electrical and Electronics Engineers
IERR	Internal ERRor. A signal from the Intel Architecture processors indicating an internal error condition.
INT	INTerrupt
IMCH	Integrated Memory Controller Hub. Sub-part of the MICH chipset.
iMPACT	Xilinx iMPACT, a tool featuring batch and GUI operations, allows you to perform two basic functions: Device Configuration and File Generation.
IMVP-6	Intel Mobile Voltage Positioning. The Intel Mobile Voltage Positioning specification for the Intel® Core™ Duo Processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor.
IO	(Same as I/O). Input Output
IOAPIC	(Same as IO-APIC). IO Advanced Programmable Interrupt Controller
IOH	I/O Hub
IO-APIC	(Same as IOAPIC). IO Advanced Programmable Interrupt Controller
IOL	IPMI-Over-LAN
IP	Internet Protocol
IPM	Intelligent Platform Management
IPMB	Intelligent Platform Management Bus
IPMB-0	Intelligent Platform Management Bus Channel 0, the logical aggregation of IPMB-A and IPMB-B.
IPMB-A	Intelligent Platform Management Bus A
IPMB-B	Intelligent Platform Management Bus B
IPMB-L	Intelligent Platform Management Bus Local
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
IPMIFWU	Intelligent Platform Management Interface FirmWare Update
IPv6	Internet Protocol version 6
IRQ	Interrupt ReQuest
ISA	Industry Standard Architecture. 16-bit (XT) bus architecture.
ISE	Xilinx electronic design automation (EDA) tools for use with its devices.
ISO	International Organization for Standardization
ITU	International Telecommunication Union

Acronyms	Descriptions
ITU-T	ITU Telecommunication standardization sector. ITU is International Telecommunication Union.
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
KB	KiloByte
KCS	Keyboard Controller Style. An IPMI system interface.
KCS-SMM	Keyboard Controller Style. BIOS private IPMI system interface.
KCS-SMS	Keyboard Controller Style. Application IPMI system interface.
KHz	KiloHertz
LAN	Local Area Network
LBA	Logical Block Addressing
LBC	Local Bus Controller (On PowerQuicc III CPU)
LED	Light-Emitting Diode
LFCS	Limited First Customer Shipment. Refers to Kontron scheduling for boards.
LFM	Low Frequency Mode. The lowest operating speed for the processor.
LIP	Loop Initialization Primitive. Related to FC arbitrated loop topology (an initial message needed for learning the loop addresses and acquiring one).
LPC	Low Pin Count port
LPT1	Line Print Terminal 1
LSB	Least Significant Byte
LUN	Logical Unit Number
LV	Low Voltage
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Controller address of a computer networking device.
MB	MegaByte
MBE	Multiple Bit Error
MBIST	(same as MemBIST). Memory Built-In Selft-Test. Chipset feature for out-of-band memory testing and intialization.
MBR	Master Boot Record
MC	Management Controller
MCH	Memory Controller Hub
MemBIST	(same as MBIST). Memory Built-In Selft-Test. Chipset feature for out-of-band memory testing and intialization.
MDn	Message Digest algorithm (n=2, 5)
MDI	Medium Dependent Interface. MDI port or uplink port.
MHz	MegaHertz
MICH	Memory controller Hub and I/O Controller Hub. Chipset that integrates IMCH and IICH in a single chip solution.
Microcode	Intel-supplied data block used to correct specific errata in the processor.
MII	Media Independent Interface
MIIM	Media Independent Interface Management
MLVDS	Multipoint Low-Voltage Differential Signaling
MMC	Module Management Controller. MMCs are linked to the IPMC.

Acronyms	Descriptions
MMIO	Memory-Mapped IO
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MP	MultiProcessor
MPS	MultiProcessor Specification
MRC	Memory Reference Code. Chipset specific code provided by the manufacturer and integrated into the BIOS to test and intialize the system memory.
MSB	Most Significant Byte
MSI	Message Signaled Interrupts
MSR	Model Specific Register inside IA32 processors.
MTBF	Mean Time Between Failures
MTRR	Memory Type Range Register. CPU cache control registers.
MUX	MUltipleXer
NAND	Type of Flash Memory, used for mass storage.
NC	Not Connected
NDA	Non-Disclosure Agreement
NEBS	Network Equipment-Building System
NEDS	Network Equipment Development Standard
NMI	Non-Maskable Interrupt
NSI	North South Interface. Internal physical interface between the IMCH and IICH.
NV	Non-Volative. Refers to persistent storage.
NVRAM	Non-Volatile Random Access Memory
NVS	Non-Volatile Storage
O&M	(Same as OAM/OA&M). Operations and Maintenance
OAM	(Same as OA&M/O&M). Operations, Administration and Maintenance
OA&M	(Same as OAM/O&M). Operations, Administration and Maintenance
OEM	Original Equipment Manufacturer
OMU	Operations and maintenance Unit
OOS	Out Of Service
OS	Operating System
OSI	Open Source Initiative
PAE	Physical Address Extension. Feature of x86 processors that allows for up to 64 gigabytes of physical memory to be used in 32-bit systems, given appropriate operating system support.
PAM	Programmable Attribute Map. Chipset registers that controls the steering of read and write cycles that address the BIOS area.
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCI-32	Peripheral Component Interconnect 32 bits
PCI®	Peripheral Component Interconnect
PCIe	(Same as PCI-E). PCI-Express. Next generation I/O standard
PCI-E	(Same as PCIe). PCI-Express. Next generation I/O standard.
PCI-X	PCI + minor changes to the protocol and faster data rate.
PDP	Project Development Process
PDU	Power Distribution Unit

Acronyms	Descriptions
PECI	Platform Environment Control Interface
PECL	Positive Emitter-Coupled Logic
PEF	Platform Event Filtering. An IPMI subfunction.
PET	Platform Event Trap. An IPMI message type.
PEM	Power Entry Module
PERR	Parity ERRor. A signal on the PCI bus that indicates a parity error on the bus.
PHY	PHYsical layer. Generic electronics term referring to a special electronic integrated circuit or functional block of a circuit that takes care of encoding and decoding between a pure digital domain (on-off) and a modulation in the analog domain.
PIC	Programmable Interrupt Controller
PICMG	PCI Industrial Computer Manufacturers Group
PICMG®	PCI Industrial Computer Manufacturers Group
PIR	Product Issue Report
PIU	Plug-In Unit
PLCC	Plastic Leaded Chip Carrier
PLD	Programmable Logic Device
PLL	Phase Lock Loop
PMC	PCI Mezzanine Card
PMM	POST Memory Manager
PNE	Platform for Network Equipment. A Carrier Grade Linux (4.0) platform.
POH	System Operating Power-On Hours.
POR	Power-On Reset
POST	Power-On Self-Test
PPP	Point-to-Point Protocol
prAMC	Processor AMC
PROM	Programmable Read-Only Memory
PTS	Prepare To Sleep. An ACPI method called before the OS makes a change to system power state level.
PWB	(Same as PCB). Printed Wiring Board
PWM	Pulse-Width Modulation
PXE	Preboot eXecution Environment
QPI	QuickPath Interconnect. Point-to-point interconnect between Intel processors and IOH.
RAID	Redundant Array of Independent Disks / Redundant Array of Inexpensive Disks.
RAKP	RMCP+ Authenticated Key-Exchange Protocol
RAM	Random Access Memory
RAS	Row Address Strobe, used in DRAM. May also refers to Reliability, Availability, Serviceability features of the chipset.
RASUM	Reliability, Availability, Serviceability, Usability and Manageability features of the chipset (AER and ECC are RASUM features).
RCRB	Root Complex Register Block registers. Chipset memory-mapped space for configuration registers.
RGMII	Reduced Gigabit Media Independent Interface
RHEL	Red Hat Enterprise Linux
RIMM	Rambus Inline Memory Module
RMCP	Remote Management Control Protocol

Acronyms	Descriptions
RMII	Reduced Media Independent Interface
RMON	Remote network MONitoring
RMS	Root Mean Square
RoHS	Restriction of the Use of Certain Hazardous Substances
ROM	Read Only Memory. Also refers to option ROM or expansion ROM code used during POST to provide services for specific controllers, such as boot capabilities.
RPP	Reliability Prediction Procedure
RS-232	(Same as RS232). Recommended Standard 232.
RS232	(Same as RS-232). Recommended Standard 232.
RSS	Receive Side Scaling
RTC	Real Time Clock
RTM	Rear Transition Module
RTM-Link	Rear Transition Module Link. Kontron 3-wire protocol.
RTS	Request To Send
S.M.A.R.T.	Self-Monitoring, Analysis, and Reporting Technology for IDE.
S0	ACPI OS System State 0. Indicates fully on operating state.
S5	ACPI OS System State 5. Indicates Soft Off operating state.
SAS	Serial Attached SCSI
SATA	Serial ATA
SBC	Single Board Computer
SBE	Single Bit Error
SCI	System Control Interrupt
SCL	Serial CLock
SCSI	Small Computer System Interface
SDH	Synchronous Digital Hierarchy
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SEC	Single-bit Error Correct
SEEPROM	Serial EEPROM
SEL	System Event Log
SERDES	SERializer/DESerializer. Pair of functional blocks commonly used in high speed communications. These blocks convert data between serial data and parallel interfaces in each direction.
SERIRQ	Serial IRQ
SERR	System ERRor. A signal on the PCI bus that indicates a ‘fatal’ error on the bus.
SFP	Small Form-factor Pluggable
SGMII	Serial Gigabit Media Independent Interface. Standard interface used to connect a Gigabit Ethernet MAC-block to a PHY.
ShMC	Shelf Management Controller
SIMD	Single Instruction, Multiple Data
SIMM	Single In-line Memory Module
SIRQ	Serial Interrupt ReQuest
SLC	Single-Level Cell

Acronyms	Descriptions
SMART	Self-Monitoring, Analysis, and Reporting Technology, or S.M.A.R.T. A monitoring system for computer hard disks to detect and report on various indicators of reliability, in the hope of anticipating failures.
SMB	(Same as SMBus/SMBUS). System Management Bus.
SMBIOS	System Management BIOS
SMBUS	(Same as SMB/SMBus). System Management Bus.
SMBus	(Same as SMB/SMBUS). System Management Bus.
SMI	System Management Interrupt
SMM	System Management Mode
SMP	Symmetric MultiProcessing. SMP systems allow any processor to work on any task no matter where the data for that task are located in memory; with proper operating system support, SMP systems can easily move tasks between processors to balance the workload efficiently.
SMR	Special Modification Request. Indicates a customer specific change.
SMS	System Management Software
SMT	Surface MounT.
SMTP	Simple Mail Transfer Protocol
SNMP	Simple Network Management Protocol
SNTP	Simple Network Time Protocol
SO-CDIMM	Small Outline Clocked 72-bit Dual In-line Memory Module
SO-DIMM	Small Outline Dual In-line Memory Module
SOL	Serial Over LAN
SONET	Synchronous Optical NETworking
SPD	Serial Presence Detect. A standardized way to automatically access information about a computer memory module.
SPI	Serial Peripheral Interface
SpeedStep	(Same as EIST). Enhanced Intel SpeedStep Technology.
SRAM	Static Random Access Memory
SSE2	Streaming SIMD Extension 2. SIMD is "Single Instruction, Multiple Data".
SSE3	Streaming SIMD Extension 3. SIMD is "Single Instruction, Multiple Data".
SSH	Secure SHell. A network protocol that allows data to be exchanged over a secure channel between two computers.
SSP	Serial SCSI Protocol
STM-1	Synchronous Transport Module 1
STP	Spanning Tree Protocol
SW	SoftWare
SWS	SoftWare Specification
TA	Ambient Temperature
TAP	Telocator Access Protocol. An IPMI Serial/Modem interface component.
TCC	Thermal Control Circuit
TCLKA	Telecom CLocK A. AMC Clock Interface.
TCLKB	Telecom CLocK B. AMC Clock Interface.
TCLKC	Telecom CLocK C. AMC Clock Interface.
TCLKD	Telecom CLocK D. AMC Clock Interface.

Acronyms	Descriptions
TCO	Total Cost of Ownership. Refers to a logic block in the Intel ICH products family. The watchdog timer (WDT) is one of the functions of that logic block.
TCP	Transmission Control Protocol
TDP	Thermal Design Power
TM	(Same as TM1). Thermal monitor. CPU Thermal based on clock throttling.
TM1	Thermal monitor 1. CPU Thermal based on clock throttling.
TM2	Thermal monitor 2. CPU Thermal based on Enhanced Intel SpeedStep Technology transitions.
TOLM	Top Of Low Memory. Highest DRAM available to system, below 4GB.
TPM	Trusted Platform Module
TX	Transmit
TXD	Transmit
UA	Upgrade Agent
UART	Universal Asynchronous Receiver Transmitter
UC	Unit Computer
UDP	User Datagram Protocol. An Internet Protocol.
UHCI	Universal Host Controller Interface. Specification for Universal Serial Bus specification, revision 1.0.
UL	Underwriters Laboratories inc
UPM	User Programmable Machine
USB	Universal Serial Bus
UUID	Universal Unique ID number.
VA	Volt-Amperes. Unit used for apparent power.
VAC	Volt Alternating Current. Volt unit used when alternating current.
VCC	Power supply
VCORE	Processor CORE power supply
VID	Voltage IDentification. The CPU uses VID pins to support automatic selection of power supply voltages.
VGA	Video Graphics Array
VLAN	Virtual Local Area Network
VLSI	Very-large-scale integration
VSUS	Power supply in suspend power
VT	Video Terminal
VTT	Power supply
WD	WatchDog
WDT	WatchDog Timer
WfM	Wired for Management
WWN	World Wide Name
WWPN	World Wide Port Name
XAUI	X (meaning ten) Attachement Unit Interface. A standard for connecting 10 Gigabit Ethernet (10GbE) ports.
XDP	eXtended Debug Port
XMC	Switched Mezzanine Card