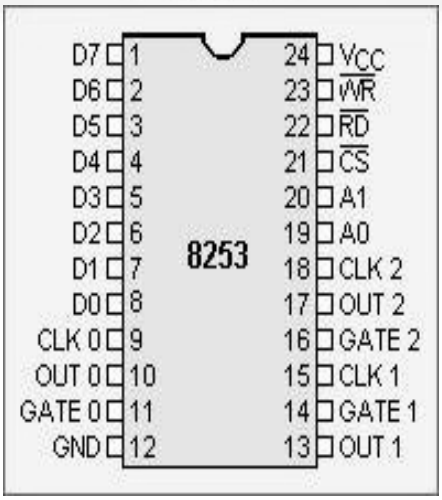
3.5 TIMER

PROGRAMMABLE INTERVAL TIMER (8253/8254)

The Intel 8253 and 8254 are Programmable Interval Timers (PTIs) designed for microprocessors to perform timing and counting functions using three 16-bit registers. Each counter has 2 input pins, i.e. Clock & Gate, and 1 pin for "OUT" output. To operate a counter, a 16-bit count is loaded in its register.On command, it begins to decrement the count until it reaches 0, then it generates a pulse that can be used to interrupt the CPU.

Difference between 8253 and 8254

8253	8254
Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
It uses N-MOS technology	It uses H-MOS technology
Read-Back command is not available	Read-Back command is available
Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.



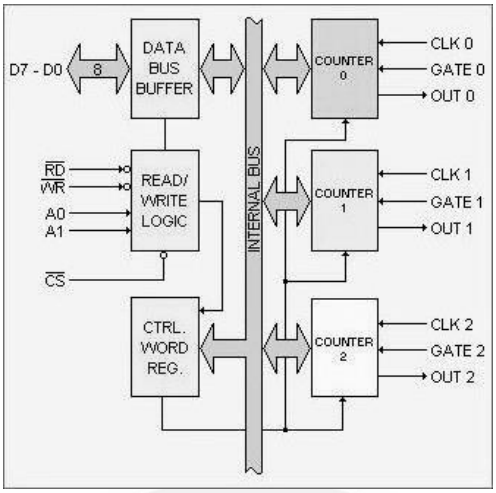


Figure 3.5.1 Internal blocks of 8253 and pin diagram

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

CS - Chip select . When it is low,enables the communication between CPU and 8253.

WR-When it is low,the CPU output data in the form of mode information are loading counters.

RD – When it is low,the CPU reads data.

A0-A1: These pins are connected to address bus. These are used to select one of the three counters.

D0-D7: These are tri-state bidirectional data bus used to interface 8253 to the system data bus.

CLK0, CLK1and CLK2-

These are clock signals for counter0, counter1 and counter2.

GATE0, GATE1 and GATE2-

These are gate terminals for counter0, counter1 and counter2.

OUT0, OUT1and OUT2-

These are output terminals for counter0, counter1 and counter2.

In the above Figure 3.5.1, there are three counters, a data bus buffer,

Read/Write control logic, and a control register. Each counter has two input signals - CLOCK & GATE and one output signal - OUT.

Data Bus Buffer

It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus.It has three basic functions

- Programming the modes of 8253/54.
- Loading the count registers.
- Reading the count values.

Read/Write Logic

It includes 5 signals, i.e. RD, WR, CS and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW.

Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to adecoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

A1	A0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register
X	X	No Selection

Table 3.5.1 Selection of Counters

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

COUNTERS

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

Control Word Register:

The bits D7 and D6 of the control word are to select one of the 3 counters.D5 and D4 are for loading /reading the count.D3,D2 and D1 are for the selection of operating mode of the selected counter.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 3.5.2 Control Word format of 8253

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

OPERATION OF 8253:

The functions of the 8253/54 can be described by Write and Read operation.

WRITE Operation:

- Write a control word into control register.
- Load the low-order byte of a count in the counter register.
- Load the high-order byte of count in the counter register.

READ OPERATION:

1. Simple Read: It involves reading a count after inhibiting the counter by controlling the gate input or the clock input of the selected counter, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high order byte.

2. Counter Latch Command: In the second method, an appropriate control word is written into the control register to latch a count in the output latch, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high order byte.

3. Read-Back Command (Available only for 8254): The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current status of the OUT pin and Null count flag of the selected counter(s).

8254 MODES OF OPERATION:

1. Mode 0 (Interrupt on terminal count)
2. Mode 1 (programmable Monoshot)
3. Mode 2 (Rate Generator)
4. Mode 3 (Square Wave Generator)
5. Mode4(Software Triggered Strobe)

6.Mode 5 (Hardware Triggered Strobe)

The Description and operation of various modes of timer are depicted in the figures below. **[Figure 3.5.3(a) to Figure 3.5.3(f)]**

MODE 0: INTERRUPT ON TERMINAL COUNT

- In this mode OUT is low.
- Once a count is loaded the counter is decremented after every cycle and when count reaches zero, the OUT goes high.
- This can be used as an interrupt. The OUT remains high until a new count or command word is loaded.

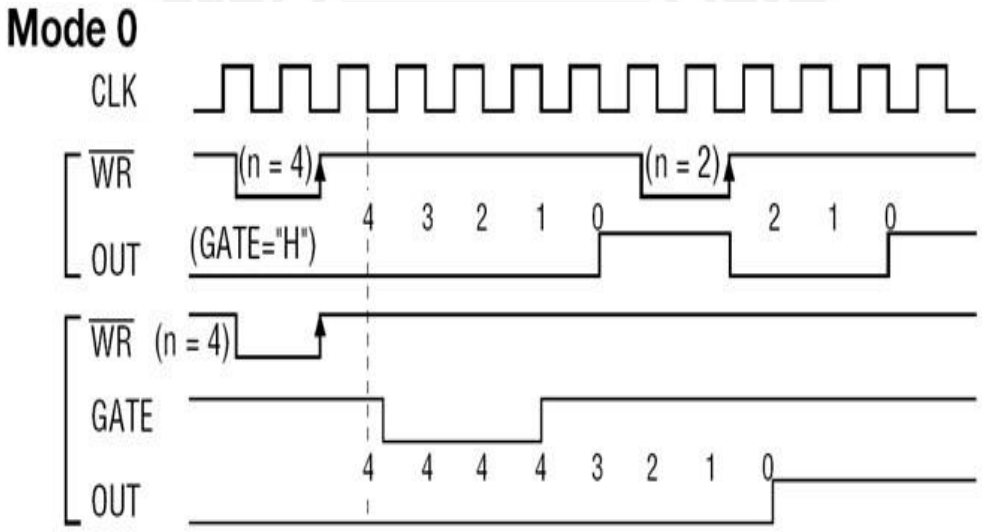


Figure 3.5.3(a) Interrupt On Terminal Count

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

MODE 1 (PROGRAMMABLE MONO SHOT)

- In this mode OUT is initially high.
- When gate is triggered, the OUT goes low and at the end of count it goes high again, thus generating a one shot pulse.

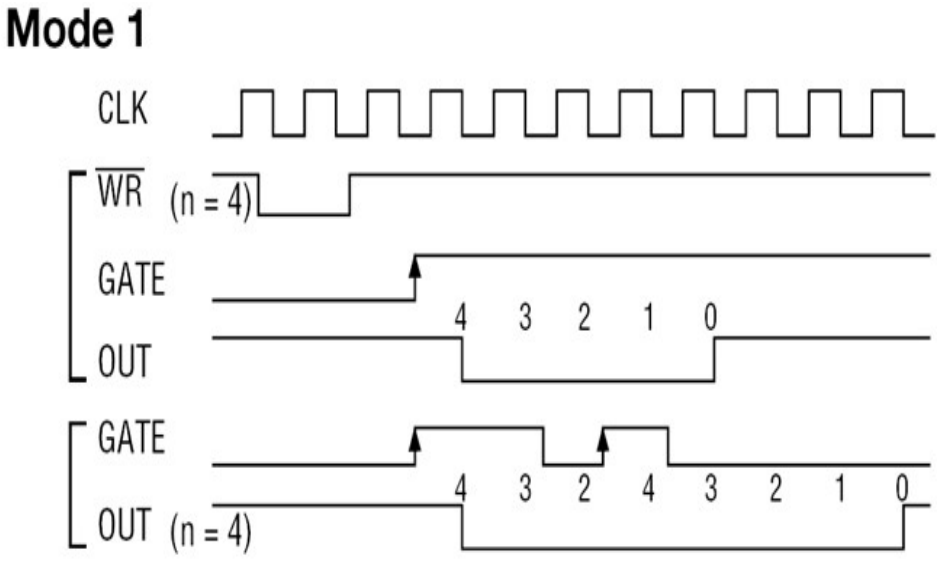


Figure 3.5.3(b) Programmable Mono Shot

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

MODE 2 (RATE GENERATOR)

The mode is used to generate a pulse equal to given clock period at a given interval.

When a count is loaded, the OUT stays high until count reaches 1 and then OUT goes low for 1 clock period then gets reloaded automatically and this is how pulse gets generated continuously.

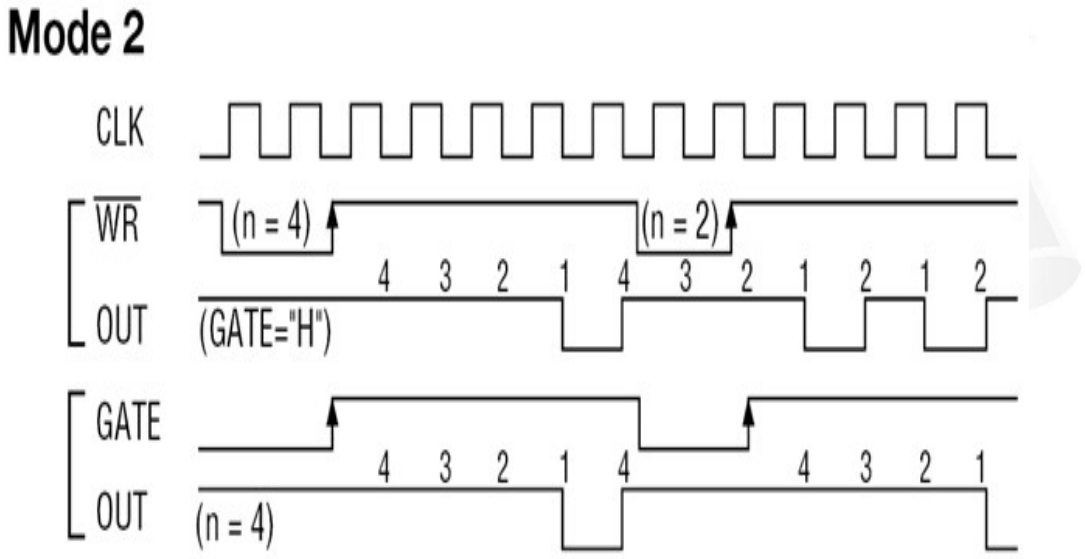


Figure 3.5.3(c) Rate Generator

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

MODE 3 (SQUARE WAVE GENERATOR)

- In this a continuous square wave with period equal to count is generated.
- The frequency of square wave = frequency of clock divide by count.
- if count (N) is odd pulse stay high for (N + 1)/2 and low for (N - 1)/2

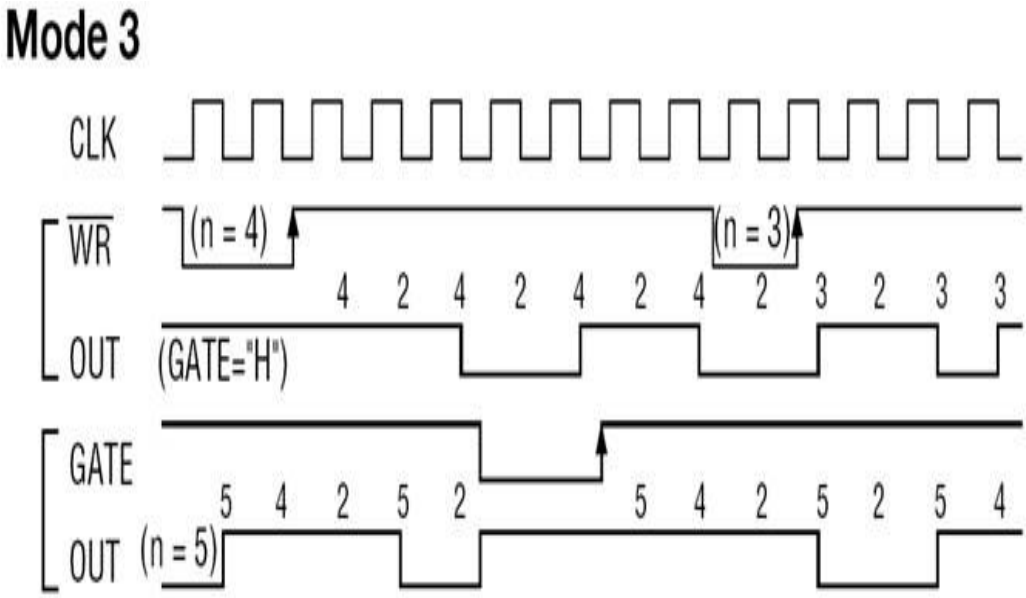


Figure 3.5.3(d) Square Wave Generator

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

Mode 4 (Software Triggered Strobe)

- In this mode OUT is initially high; it goes low for one clock period at the end of count.
- The count must be reloaded for subsequent outputs.

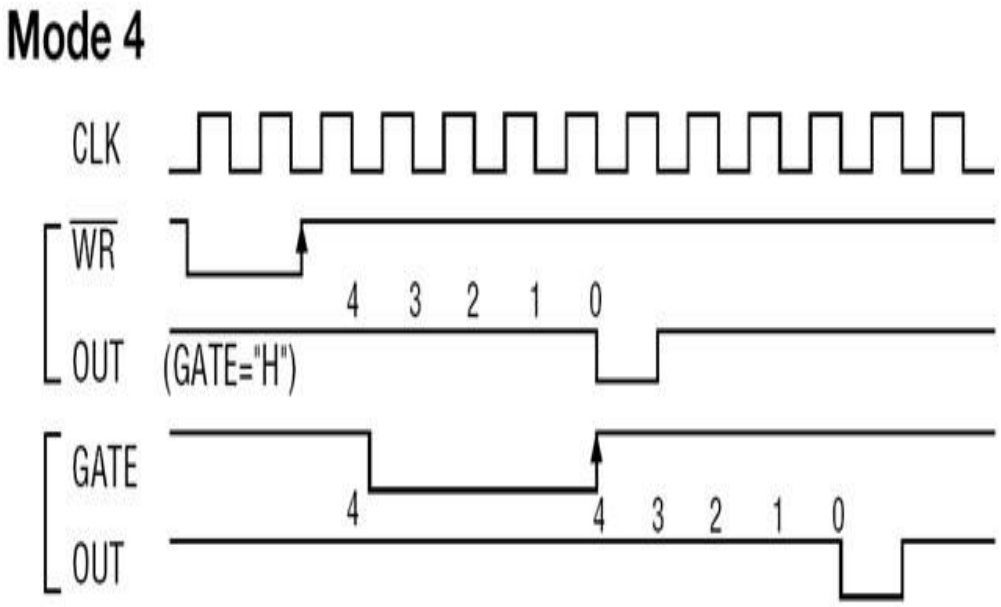


Figure 3.5.3(e) Software Triggered Strobe

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

Mode 5 (hardware triggered strobe)

- Same as MODE4 except that it is triggered by rising pulse at gate.

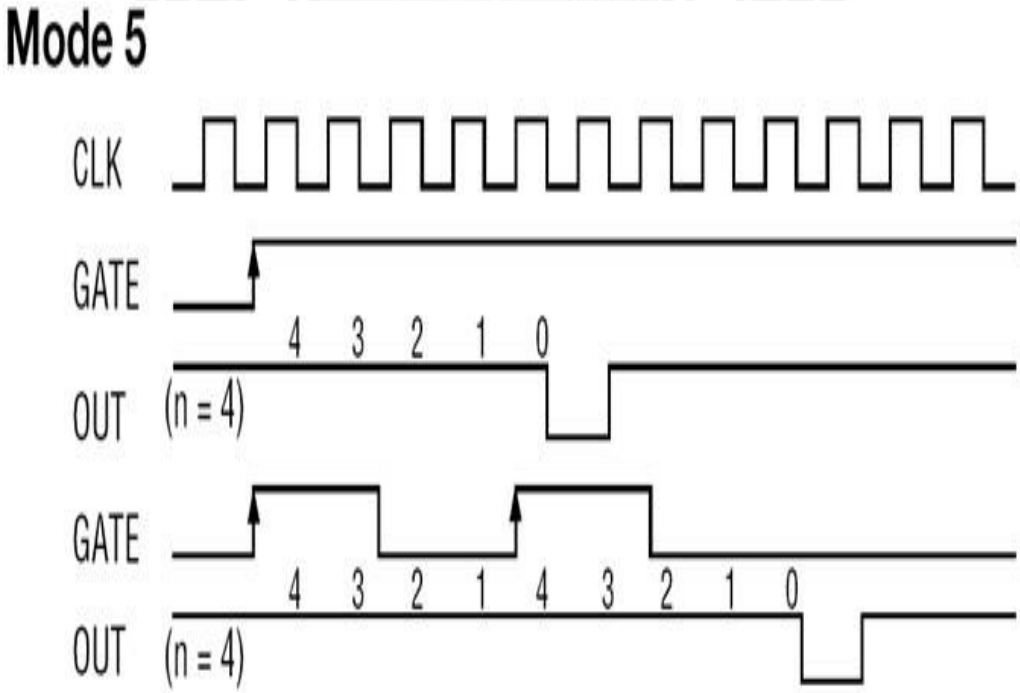


Figure 3.5.3(f) Hardware Triggered Strobe

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

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