phyBOARD®-Mira i.MX 6

Hardware Manual

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PB-01501-XXX Single Board Computer (SBC) in the following referred to as phyBOARD-Mira i.MX 6. The manual specifies the phyBOARD-Mira i.MX 6's design and function. Precise specifications for the NXP Semiconductors i.MX 6 microcontrollers can be found in the NXP Semiconductors i.MX 6 Data Sheet and Technical Reference Manual.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{RD}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device.
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- Text in ***bold italic*** indicates an interaction by the user, which is defined on the screen.
- Text in `Consolas` indicates an input by the user, without a premade text or button to click on.
- Text in *italic* indicates proper names of development tools and corresponding controls (windows, tabs, commands etc.) used within the development tool, no interaction takes place.
- White Text on black background shows the result of any user interaction (command, program execution, etc.)

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
A/V	Audio/Video
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or *Linux*) pre-installed on the module and Development Tools)
CB	Carrier Board, used in reference to the phyBOARD-Mira Development Kit Carrier Board
DFF	D flip-flop
DSC	Direct Solder Connect
EMB	External memory bus
EMI	Electromagnetic Interference
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
IRAM	Internal RAM, the internal static RAM on the NXP Semiconductors i.MX 6 microcontroller
J	Solder jumper, these types of jumpers require solder equipment to remove and place
JP	Solderless jumper, these types of jumpers can be removed and placed by hand with no special tools
NC	Not Connected
NM	Not Mounted
NS	Not Specified
PCB	Printed circuit board
PDI	Phytec Display Interface, defined to connect Phytec display adapter boards, or custom adapters
PEB	Phytec Expansion Board
PMIC	Power management IC
PoE	Power over Ethernet
PoP	Package on Package
POR	Power-on reset
RTC	Real-time clock
SBC	Single Board Computer, used in reference to the PBA-C(D)-06 /phyBOARD-Mira i.MX 6
SMT	Surface mount technology
SOM	System on Module, used in reference to the PCM-058 /phyCORE-i.MX 6 module
Sx	User button Sx (e.g. S1, S2) used in reference to the available user buttons, or DIP switches on the CB
Sx_y	Switch y of DIP switch Sx, used in reference to the DIP switch on the carrier board
VSTBY	SOM standby voltage input

Table 1: Abbreviations and Acronyms used in this Manual

	At this icon you might leave the path of this Application Guide.
	This is a warning. It helps you to avoid annoying problems.
	You can find information to solve problems.

Preface

As a member of Phytec's new phyBOARD® product family the phyBOARD-Mira i.MX 6 is one of a series of Phytec System on Modules (SBCs) that offer off-the-shelf solutions for a huge variety of industrial applications. The new phyBOARD® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes. All phyBOARDs are rated for industry, cost optimized and offer long-term availability. The phyBOARD-Mira i.MX 6 is one of currently six industrial-grade carrier boards which are suitable for series production and that have been realized in accordance with Phytec's new SBCplus concept. It is an excellent example of this concept.

SBCplus Concept
The SBCplus concept was developed to meet fine differences in customer requirements with little development effort and thus to greatly reduce the time-to-market.

Core of the SBCplus concept is the SBC design library (a kind of construction set) that consists of a great number of function blocks (so-called "building blocks") which are refined constantly. The recombination of these function blocks allows to develop a customer specific SBC within a short time. Thus, Phytec is able to deliver production-ready custom Single Board Computers within a few weeks at very low costs.

The already developed SBCs, such as the phyBOARD-Mira, each represent an intersection of different customer wishes. Because of that all necessary interfaces are already available on the standard versions, thus, allowing to integrate them in a large number of applications without modification. For any necessary detail adjustment extension connectors are available to enable adding of a wide variety of functions.

Cost-optimized with Direct Solder Connect (DSC) Technology
At the heart of the phyBOARD-Mira is the phyCORE-i.MX 6 System on Module (SOM). As with other SBCs of the phyBOARD® family the SOM can be directly soldered onto the carrier board PCB for routing of signals from the SOM to applicable I/O interfaces. This optional “Direct Solder Connect” (DSC) of the SOM eliminates costly PCB to PCB connectors, thereby further reducing overall system costs, and making the phyBOARDs ideally suited for deployment into a wide range of cost-optimized and robust industrial applications.

Customized Expandability from Phytec
Common interface signals route to standard connector interfaces on the carrier board such as Ethernet, CAN, RS-232, and audio. Due to the easily modifiable phyBOARD design approach (see "*SBCplus concept*"), these plug-and-play interfaces can be readily adapted in customer-specific variants according to end system requirements.

Some signals from the processor populating the SOM also extend to the expansion, and A/V connectors of the phyBOARD-Mira. This provides for customized expandability according to end user requirements. Thus expandability is made easy by available plug-and-play expansion modules from Phytec.

- HDMI and LVDS/Parallel Displays
- Power Supply, with broad voltage range
- Industrial I/O (including WLAN)
- Home-Control Board (WiFi, KNX/EIB, I/O)
- M2M Board (GPS, GSM, I/O's)
- Debug Adapter

The default orientation of the expansion bus connectors is parallel and on the top side of the carrier board PCB. However, in custom configurations the connectors can be mounted on the PCB's underside. Connectors in perpendicular orientation can also populate the top or underside of the PCB. This enables maximum flexibility for orientation of expansion modules on the phyBOARD-Mira, as well as integration of the system into a variety of end application physical envelopes and form factors.

Easy Integration of Display und Touch
The phyBOARD and its expansion modules enable easy connection of parallel or LVDS based displays, as well as resistive or capacitive touch screens.

OEM Implementation
Implementation of an OEM-able SBC subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyBOARD® SBC lies in its layout and test.

Software Support
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise.

Ordering Information

Ordering numbers:

phyBOARD-Mira i.MX 6 Development Kit:	**KPB-01501-xxx**
phyBOARD-Mira i.MX 6 SBC:	**PB-01501-xxx**

Product Specific Information and Technical Support

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/support/faq/faq-phyBOARD-Mira-i.MX6.html or
http://www.phytec.eu/support/faq/faq-phyBOARD-Mira-i.MX6.html

Other Products and Development Support

Aside of the new phyBOARD® familiy, Phytec supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional OEM modules, which can be embedded directly into the user's peripheral hardware design.

Take advantage of Phytec products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/support/ueberblick/ or
http://www.phytec.eu/support/ueberblick/

Declaration of Electro Magnetic Conformity of the Phytec phyBOARD-Mira i.MX 6

Phytec Single Board Computers (henceforth products) are designed for installation in electrical appliances, or as part of custom applications, or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
Phytec products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, Phytec products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

Phytec products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of Phytec products into target devices, as well as user modifications and extensions of Phytec products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM / SBC

When buying a Phytec SOM / SBC, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating long-livety of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in case of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the contact information given within this manual.

1 Introduction

1.1 Hardware Overview

The phyBOARD-Mira for phyCORE-i.MX 6 is a low-cost, feature-rich software development platform supporting the NXP Semiconductors i.MX 6 microcontroller. Moreover, due to the numerous standard interfaces the phyBOARD-Mira i.MX 6 can serve as bedrock for your application. At the core of the phyBOARD-Mira is the PCM-058/phyCORE-i.MX 6 System On Module (SOM), containing the processor, DRAM, NAND Flash, power regulation, supervision, transceivers, and other core functions required to support the i.MX 6 processor. Surrounding the SOM is the PBA-CD-06/phyBOARD-Mira carrier board, adding power input, buttons, connectors, signal breakout, and Ethernet connectivity amongst other peripherals.

The PCM-058 System On Module connects to the phyBOARD-Mira carrier board by use of two high density connectors. The phyBOARD-Mira is also available with the phyCORE-i.MX 6 in a direct solder form factor (PCL-058), a connector-less, BGA style variant of the PCM-058/phyCORE-i.MX 6 SOM. The PCL-058 SOM is directly soldered down to the phyBOARD-Mira using Phytec's Direct Solder Connect technology. This solution offers an ultra-low cost Single Board Computer for the i.MX 6 processor, while maintaining most of the advantages of the SOM concept.

Adding the phyCORE-i.MX 6 SOM into your own design is as simple as ordering the connectored version (PCM-058) and making use of our phyCORE Carrier Board reference schematics.

1.1.1 Features of the phyBOARD-Mira i.MX 6

The phyBOARD-Mira i.MX 6 supports the following features :

- Developed in accordance with Phytec's new SBCplus concept (*Preface*)
- Phytec’s phyCORE-i.MX 6 SOM (optionally with Direct Solder Connect (DSC))
- Pico ITX standard dimensions (100 mm × 72 mm)
- Boot from MMC or NAND Flash
- Max. 1.2 GHz core clock frequency and up to four cores
- Two different power supply options (5 V via 3.5 mm combicon or 12 V – 24 V through external power module)
- One RJ45 jacks for 10/100/1000 Mbps Ethernet
- One USB host interface brought out to an upright USB Standard-A connector, or at the Mini PCI express connector[1]
- One USB OTG interface available at an USB Micro-AB connector, or at the expansion connector[1]

1 : **Caution!** There is no protective circuit for the USB interfaces brought out at the Mini PCI Express connector and the expansion connector.

- One Secure Digital / Multi Media Memory Card interface brought out to a Micro-SD connector at the back side
- CAN interface at 2×5 pin header 2.54 mm
- One HDMI interface brought out to a standard type A connector
- One LVDS interface brought out to a 20 pin FFC connector at the backside, and separate connector for backlight supply and control
- One touch interface at 1x4 pin header 2.54 mm
- One LVDS camera interfaces compatible to Phytec phyCAM-S+ camera standard with I^2C for camera control
- One PCI interface brought out to a Mini PCI Express connector, SIM-card signals are also available at the expansion connector
- RS-232 or RS-485 transceiver supporting UART3 incl. handshake signals with data rates of up to 1 Mbps (2×5 pin header 2.54 mm)
- Reset-Button
- One multicolor LED
- Audio/Video (A/V) connectors
- Expansion connector with different interfaces
- RTC
- Backup supply for RTC via external 2-pole pin header or with Gold cap (lasts approx. 11 ½ days)

1.1.2 Block Diagram

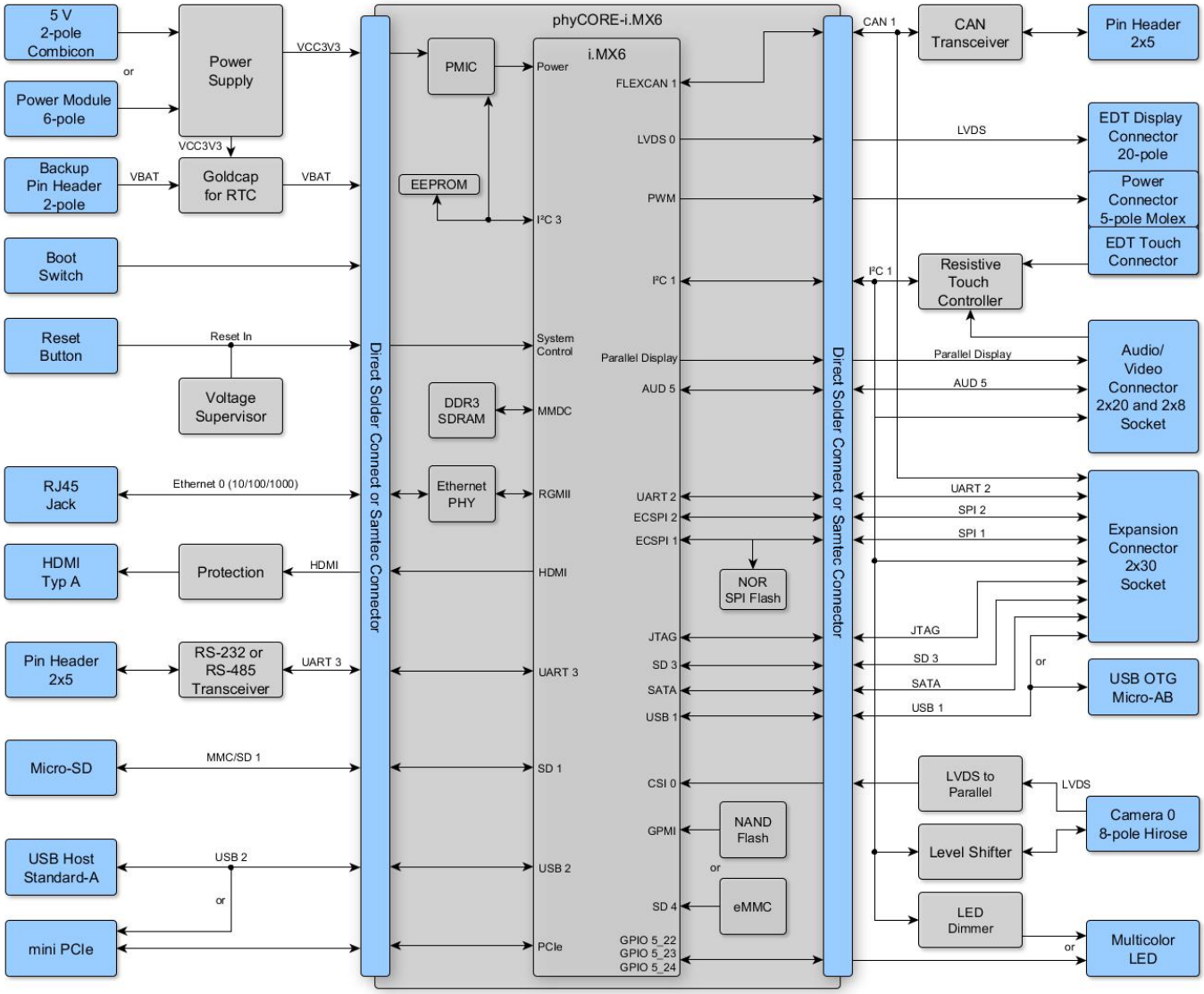


Figure 1: Block Diagram of the phyBOARD-Mira i.MX 6

1.1.3 View of the phyBOARD-Mira i.MX 6

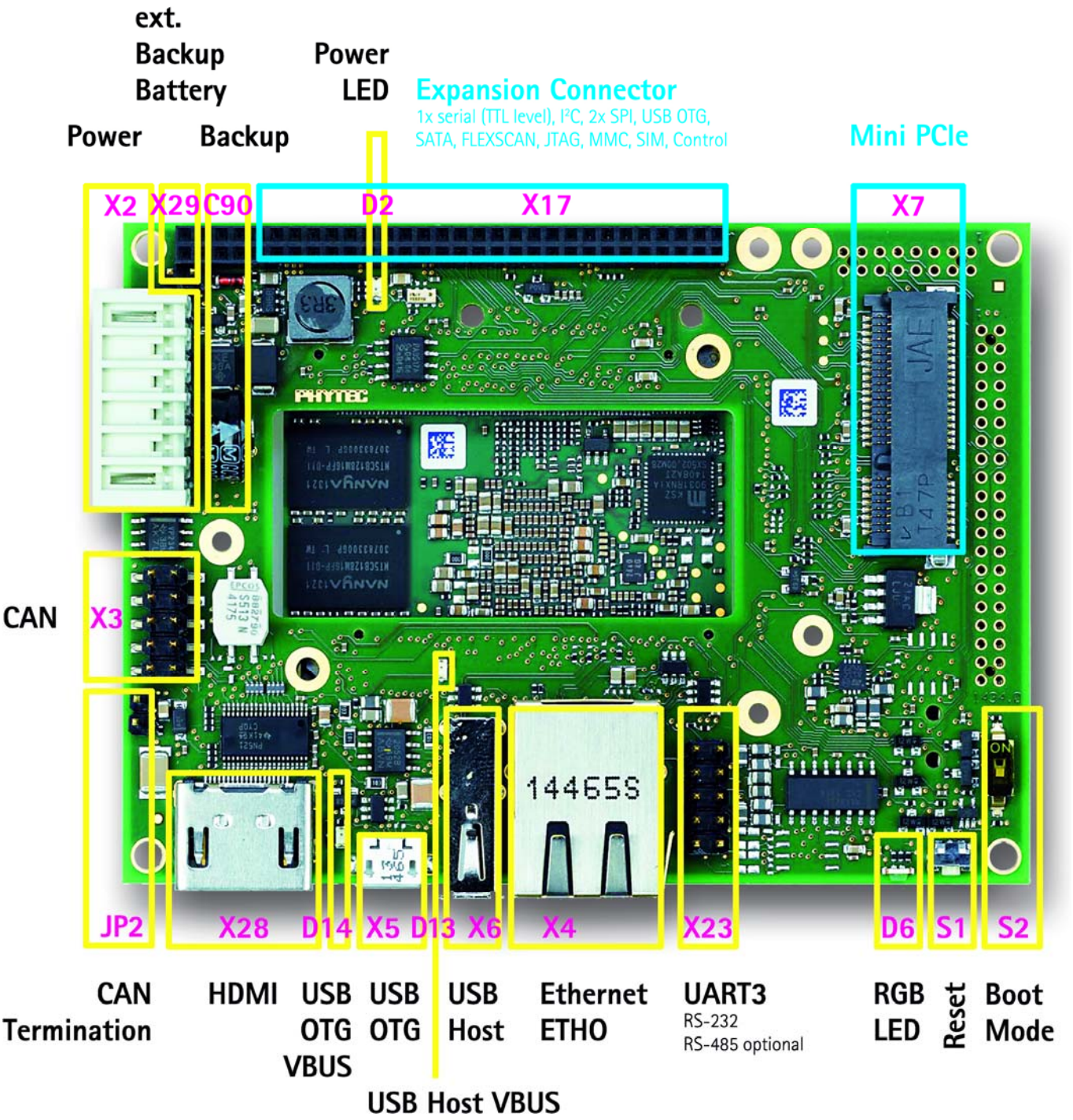


Figure 2: View of the phyBOARD-Mira i.MX 6 (top)

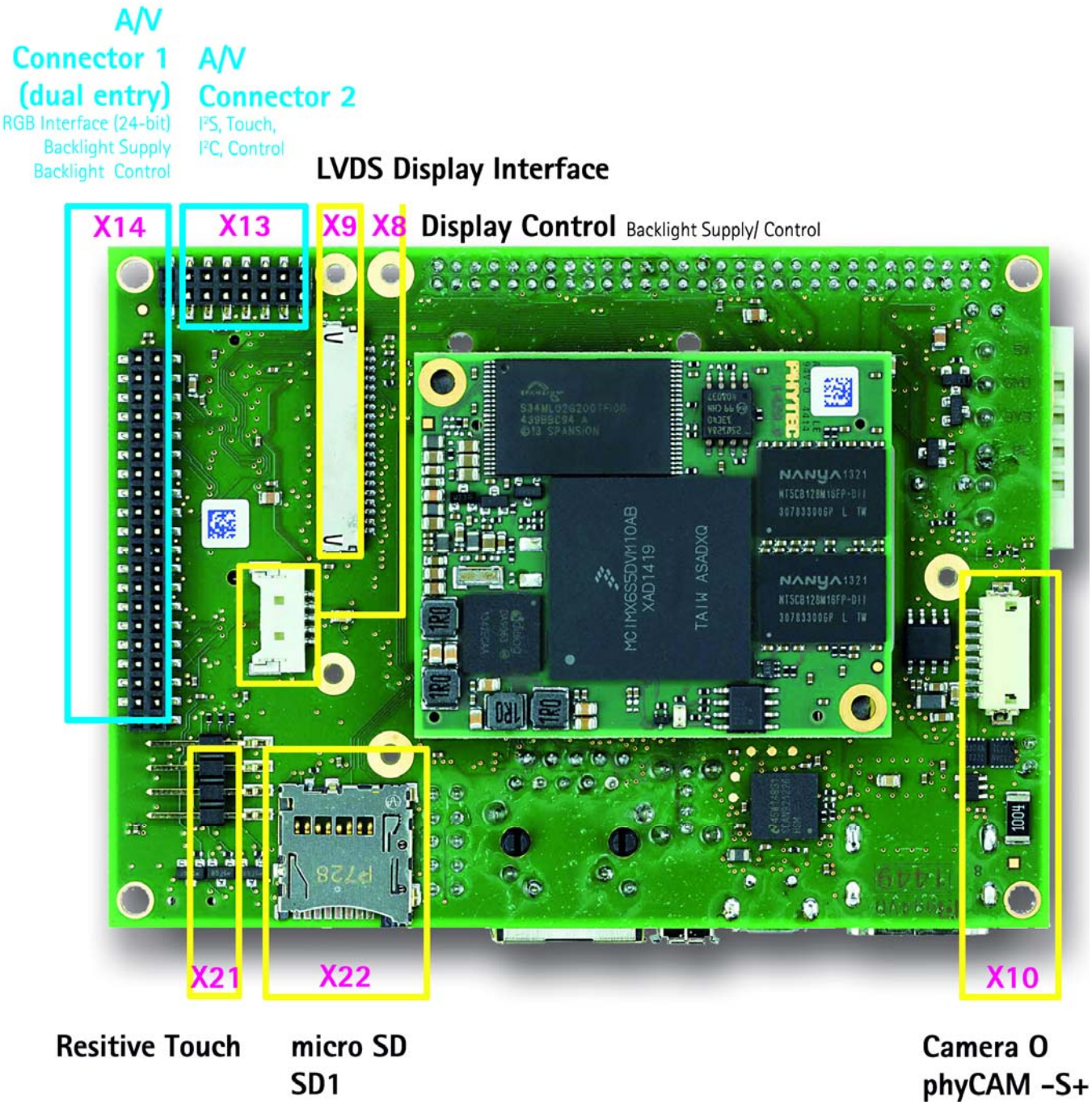


Figure 3: View of the phyBOARD-Mira i.MX 6 (bottom)

2 Accessing the phyBOARD-Mira Features

Phytec phyBOARD-Mira is fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up.

2.1 Overview of the phyBOARD-Mira Peripherals

The phyBOARD-Mira is depicted in *Figure 2*. It features many different interfaces and is equipped with the components as listed in *Table 2*, and *Table 3*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. *Figure 2* highlights the location of each peripheral for easy identification.

2.1.1 Connectors and Pin Header

Table 2 lists all available connectors on the phyBOARD-Mira. *Figure 2* highlights the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	phyCORE-Connector (2 x Samtec 2x70 pin)	
X2	Power supply 5 V only (via 6-pole WAGO male header, or 2-pole Phoenix Contact MINI COMBICON base strip)	*2.2.1.1*
X3	CAN connector (2×5 pin header 2.54 mm pitch)	*2.2.5*
X4	Ethernet 0 connector (RJ45 with speed and link LED)	*2.2.3*
X5	USB On-The-Go connector (USB Micro-AB)	*2.2.4*
X6	USB host connector (USB 2.0 Standard-A)	
X7	PCI Express connector (Mini PCI Express)	*2.2.7*
X8	Display backlight supply and control connector (5-pole Molex)	*2.2.11*
X9	Display LVDS connector(20 pin FCC connector 1 mm pitch)	*2.2.10*
X10	Camera phyCAM-S+ connector (8-pole Hirose Board-to-Wire Connector 1.25 mm pitch)	*2.2.8*
X13	A/V connector #1 (2×8 dual entry connector 2 mm pitch)	*2.2.16*
X14	A/V connector #2 (2×20 dual entry connector 2 mm pitch)	
X17	Expansion connector (2×30 socket connector 2 mm pitch)	*2.2.17*
X21	Touch connector (1x4 pin header 2.54 mm pitch)	*2.2.12*
X22	Secure Digital / Multi Media Card (Micro-slot)	*2.2.6*
X23	RS-232 with RTS and CTS, or RS-485 (UART3 2×5 pin header 2.54 mm pitch)	*2.2.2*
X28	HDMI connector (Typ-A)	*2.2.9*
X29	Backup voltage connector (1x2 pin header 2.54 mm pitch)	*2.2.1.3*

Table 2: phyBOARD-Mira Connectors and Pin Headers

	Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

2.1.2 LEDs

The phyBOARD-Mira is populated with three LEDs to indicate the status of the USB VBUS voltages, as well as of the power supply voltage. The fourth LED is a user programmable RGB-LED.

Figure 2 shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	See Section
D2	red	3.3 V voltage generation of the phyBOARD-Mira	*2.2.1.2*
D6	RGB	User programmable RGB-LED	*2.2.13*
D13	green	Indicates presence of VBUS at the USB host interface	*2.2.4*
D14	green	Indicates presence of VBUS at the USB OTG interface	

Table 3: phyBOARD-Mira LEDs Descriptions

2.1.3 Switches

The phyBOARD-Mira is populated with two switches, one to reset the phyBOARD-Mira and another to configure the boot sequence.

Figure 2 shows the location of the switches. Their function is listed in the table below:

Switch	Description	See Section
S1	Reset Button	*2.2.15*
S2	Boot Switch	*2.2.14*

Table 4: phyBOARD-Mira Switches Description

2.1.4 Jumpers

The phyBOARD-Mira comes pre-configured with one removable jumper (JP) and several solder jumpers (J). The jumpers allow flexible configuring of a limited number of features for development purposes to the user.

	Due to the small footprint of the solder jumpers (J) we do not recommend manual jumper modifications. This might also render the warranty invalid. Because of that only the removable jumper is described in this section. For information on the solder jumpers see *section3.2* and contact our sales team if you need jumper configurations different from the default configuration.

The function of the removable jumper on the phyBOARD-Mira is shown in *Table 5*. More detailed information can be found in the appropriate section.

Figure 2 shows the location of jumper JP2.

Jumper	Description	See Section
JP2	CAN Termination	*2.2.5*

Table 5: phyBOARD-Mira Jumper Description

	Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

2.2 Functional Components on the phyBOARD-Mira SBC

This section describes the functional components of the phyBOARD-Mira. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

2.2.1 Power Supply

	Do not change modules or jumper settings while the phyBOARD-Mira is supplied with power!

2.2.1.1 Power Connectors (X2)

The phyBOARD-Mira is available with two different power supply connectors. Depending on your order you will find one of the following connectors on your SBC:

1. a 2-pole Phoenix Contact MINI COMBICON base strip 3.5 mm connector (X2) suitable for a single 5 V supply voltage, or
2. a 6-pole WAGO male header (X2) to attach the Power Module for phyBOARDs (PEB-POW-01) which provides connectivity for 12 V – 24 V

The required current load capacity for all power supply solutions depends on the specific configuration of the phyCORE mounted on the phyBOARD-Mira, the particular interfaces enabled while executing software, as well as whether an optional expansion board is connected to the carrier board.

Phoenix Contact base strip WAGO male header 6-pole

Figure 4: Power Supply Connectors (X2), Backup Voltage Connector (X29)

2.2.1.1.1 Phoenix Contact 2-pole MINI COMBICON Base Strip (X2)

The permissible input voltage is +5 V DC if your SBC is equipped with a 2-pole Phoenix Contact MINI COMBICON base strip. A 5 V adapter with a minimum supply of 1.5 A is recommended to supply the board via the 2-pole base strip.

Figure 4 and the following table show the pin assignment.

Pin	Signal	Description
1	VCC5V_IN	+5 V power supply
2	GND	Ground

Table 6: Pin Assignment of the 2-pole Phoenix Contact MINI COMBICON Base Strip at X2

2.2.1.1.2 WAGO 6-pole Male Header (X2)

If a WAGO 6-pole male header is mounted on your board (*Figure 2* and *Figure 4*) your board is prepared to connect to a phyBOARD Power Module (PEB-POW-01), or a custom power supply circuitry. The ordering number of the mating connector from WAGO is:
EAN 4045454120610.

Use of the 6-pole connector has the following advantages:

- Higher and wider operate range of the input voltage
- External scaling potential to optimize the electrical output current, by use of customized power modules which match the requirements
- 5 V, 3.3 V and backlight power supply

Pin assignment of the 6–pole WAGO connector:

Pin	Signal	Description
1	VCC5V_IN	+5 V power supply
2	GND	Ground
3	VCC3V3_PMOD	+3.3 V power supply
4	VCC_BL	Backlight power supply (input voltage of power module)
5	PMOD_PWRGOOD	Power good signal (connected to reset nRESET_IN)
6	nPMOD_PWRFAIL	Power fail signal

Table 7: Pin Assignment of the 6-pole WAGO Connector at X2

A detailed description of the Power Module for phyBOARDs can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

2.2.1.2 Power LED D2

The red LED D2 next to expansion connector X17 (*Figure 2*) indicates the presence of the 3.3 V supply voltage generated from the 5 V input voltage.

2.2.1.3 VBAT, RTC and X29

The phyBOARD-Mira features an external RTC at U12 (*Figure 2*) in addition to the RTC of the Power Management IC mounted on the phyCORE-i.MX 6 module. It is used for real-time or time-driven applications. To backup the RTC a Gold cap (C90) (*Figure 2*) is placed on the phyBOARD-Mira. Alternatively the 2-pole pin header X29 can be used to connect an external battery (max. 3.6 V) to VBAT to feed in the backup voltage.

Figure 4 and the following table show the pin assignment of X29.

Pin	Signal	Description
1	VBAT	Backup Battery voltage
2	GND	Ground

Table 8: Pinout of the 2-pole pin header X29

The backup voltage source (either Gold cap at C90, or external battery via X29) supplies the external RTC at U12. It can also be connected to the backup voltage pin VBAT (A5) of the phyCORE-i.MX 6 via resistor R117[2] to supply some critical registers and the RTC of the Power Management IC on the SOM when the primary system power, VCC5V_IN, is removed. The backup supply for only the RTC (U12) lasts approximately 11½ days.

2: Resistor R117 is not mounted in the standard configuration of the phyBOARD-Mira.

2.2.2 UART Connectivity (X17 and X23)

The i.MX 6 SOM supports up to 5 so called UART units. On the phyBOARD-Mira TTL level signals of UART1 and UART2 (the standard console) are routed to expansion connector X17. UART3 is available at pin header connector X23 at RS-232 level, or optionally at RS-485 level[3].

	The Evaluation Board (PEB-EVAL-01) delivered with the kit plugs into the expansion connector and allows easy use of the standard console (UART2) which is required for debugging. Please find additional information on the Evaluation Board in Application Guide for phyBOARD Expansion Boards (L-793e).

Further information on the expansion connector can be found in *section 3.2.8.*

Pin header connector X23 is located next to the Ethernet connector (*Figure 5)* and provides the UART3 signals of the i.MX 6 at RS-232, or RS-485 level. The serial interface is intended to be used as data terminal equipment (DTE) and allows for a 5-wire connection including the signals RTS and CTS for hardware flow control. *Table 9* shows the signal mapping of the RS-232 and RS-485 level signals at connector X23.

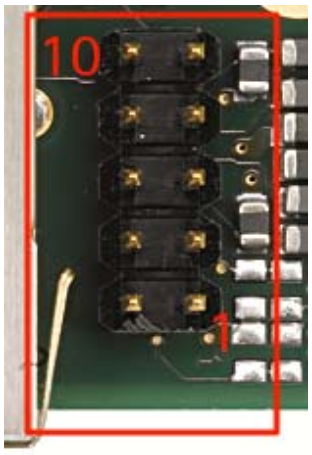


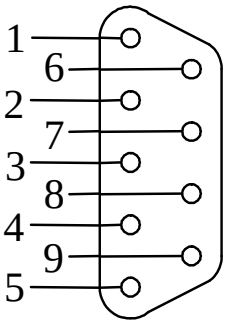
Figure 5: RS-232 or RS-485 Interface Connector X23

Pin	Signal	Pin	Signal
10	NC	9	GND
8	X_UART3_RS485_B[3]	7	X_UART3_RS485_A[3]
6	X_UART3_CTS_RS232	5	X_UART3_TXD_RS232
4	X_UART3_RTS_RS232	3	X_UART3_RXD_RS232
2	NC	1	NC

Table 9: Pin Assignment of RS-232 /RS-485 Interface Connector X23

3: The standard kit comes with an RS-232transceiver installed, if you need an RS-485 interface at X23 instead, please contact our sales team.

An adapter cable is included in the phyBOARD-Mira i.MX 6 Kit to facilitate the use of the UART3 interface. The following figure shows the signal mapping of the adapter.



Pin 2:	RxD-RS232
Pin 7:	RTS-RS232
Pin 3:	TxD-RS232
Pin 8:	CTS-RS232
Pin 4:	A-RS485[3]
Pin 9:	B-RS485[3]
Pin 5:	GND

Figure 6: RS-232 / RS-485 Connector Signal Mapping

2.2.3 Ethernet Connectivity (X4)

The Ethernet 0 interface of the phyBOARD-Mira is accessible at the RJ45 connector X4.

Figure 7: Ethernet Interface at Connectors X4

The standard phyBOARD-Mira is equipped with an RJ45 connector supporting a 10/100Base-T network connection. Optionally, it can be ordered with the phyCORE-i.MX 6 module configured for also 1000 Mbps Ethernet and a different RJ45 connector allowing to use the phyBOARD-Mira in a 10/100/1000Base-T network[4]. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connector. The Ethernet transceiver supports Auto MDI-X, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over path cable. They detect the TX and RX pins of the connected device and automatically configure the PHY TX and RX pins accordingly.

[4]: Please contact our sales team for more information.

2.2.4 USB Connectivity (X5 and X6)

The phyBOARD-Mira provides one USB host and one USB OTG interface.

USB1 is accessible at connector X5 (USB Micro-AB) and is configured as USB OTG. USB OTG devices are capable to initiate a session, control the connection and exchange host and peripheral roles between each other. This interface is compliant with USB revision 2.0.

USB2 is accessible at connector X6 (USB Standard-A) and is configured as USB host.

Both connectors are on the top side of the phyBOARD-Mira and located next to each other (*Figure*).

Figure 8: Components supporting the USB Interfaces

LED D14 displays the status of X_USB1_VBUS and LED D13 the status of X_USB2_VBUS.

Numerous jumpers allow to configure the USB interfaces according to your needs. Please refer to *section 1.1.1* for more information.

2.2.5 CAN Connectivity (X3, JP2)

The Controller Area Network (CAN) bus offers a low-bandwidth, prioritized message fieldbus for serial communication between microcontrollers. The Flexible Controller Area Network (FLEXCAN) module of the iMX 6 implements the CAN protocol according to the CAN 2.0B protocol specification. The first interface (FLEXCAN1) of the Flexible Controller Area Network is accessible at connector X3 (2×5 pin header, 2.54 mm pitch).

Jumper JP2 can be installed to add a 120 Ohm termination resistor across the CAN data lines if needed.

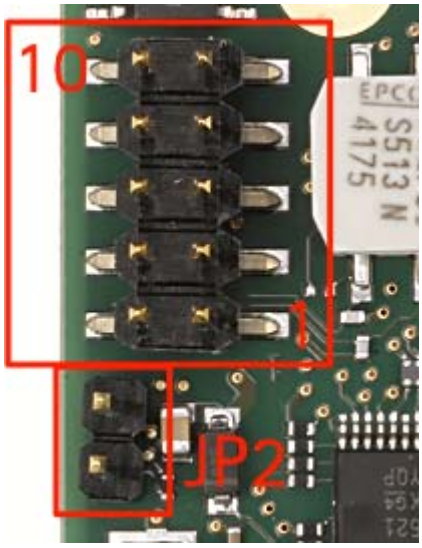


Figure 9: Components supporting the CAN Interface

Table 10 below shows the signal mapping of the CAN1 signals at connector X3.

Pin	Signal	Pin	Signal
10	NC	9	Shield
8	NC	7	NC
6	NC	5	GND
4	X_CANH	3	X_CANL
2	GND	1	NC

Table 10: Pin Assignment of CAN Connector X3

An adapter cable is included in the phyBOARD-Mira i.MX 6 Kit to facilitate the use of the CAN interface. The following figure shows the signal mapping of the adapter.

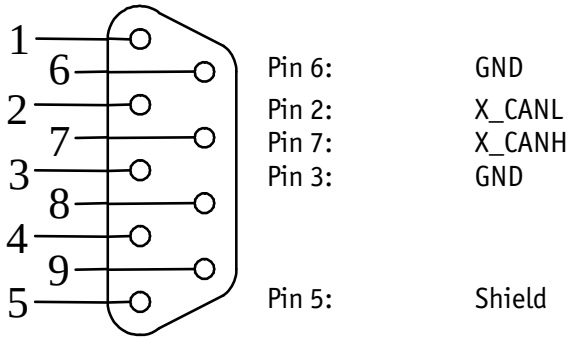


Figure 10: CAN Connector Signal Mapping

As an alternative option the TTL level signals of FLEXCAN1 can be also routed to expansion port X17 (*3.2.3*).

Depending on the muxing options a second CAN interface (FLEXCAN2) is available at expansion port X17 (*3.2.3*).

2.2.6 Secure Digital Memory Card/MultiMedia Card (X22)

Figure 11: SD/MM Card Interface at Connector X22 (back side)

The phyBOARD-Mira provides a standard microSDHC card slot at X22 for connection to MMC/SD interface cards. It allows easy and convenient connection to peripheral devices like SD- and MMC cards. Power to the SD interface is supplied by inserting the appropriate card into the MMC/SD connector, which features card detection, a lock mechanism and a smooth extraction function by Push-in/-out of card.

DIP switch S2 allows to toggle between NAND boot and boot from SD card. In order to boot from SD card S2 must be switched ON (refer to *section 2.2.14* for further information).

2.2.7 PCIe Connectivity (X7)

The 1-lane PCI express interface of the phyBOARD-Mira i.MX 6 provides PCIe Gen. 2.0 functionality which supports 5 Gbit/s operations. Furthermore the interface is fully backwards compatible to the 2.5 Gbit/s Gen. 1.1 specification. Various control signals are implemented with GPIOs[5]. The PCIe interface is brought out at the Mini PCIe connector X7 shown in the figure below.

Figure 12: PCIe Interface at Connector X7

The SIM/UIM[6] card signals of a connected PCIe module can be made available at expansion connector X17. Please refer to *Table 28* for more information about the jumper settings.

Soldering jumpers allow to connect the USB host interface to the Mini PCIe connector X7 (*Table 18*).

Please refer to *section 3.2.6* for in-depth information such as pin assignment and signals used to implement special features of the Mini PCIe interface.

2.2.8 Camera Connectivity (X10)

The SOM on the phyBOARD-Mira provides two types of camera interfaces (parallel and MIPI CSI-2).

Generally, the parallel port can be expanded on the carrier board in three ways:
1. according to the phyCAM-P camera interface standard
2. according to the as phyCAM-S+ camera interface standard
3. as interface for customer parallel cameras

On the phyBOARD-Mira the parallel Camera_0 interface is brought out as phyCAM-S+ camera interface (*Figure 13*) at connector X10 (*Figure 14*). Information on the phyCAM-S+ standard can be found in the phyCAM-manual (L-748).

5: For these pins there is no explicit multiplexing done in the BSP and they are configured with the i.MX6's default values. No further configuration is done and must be implemented by the developer.
6: User Identity Module (UIM) signals

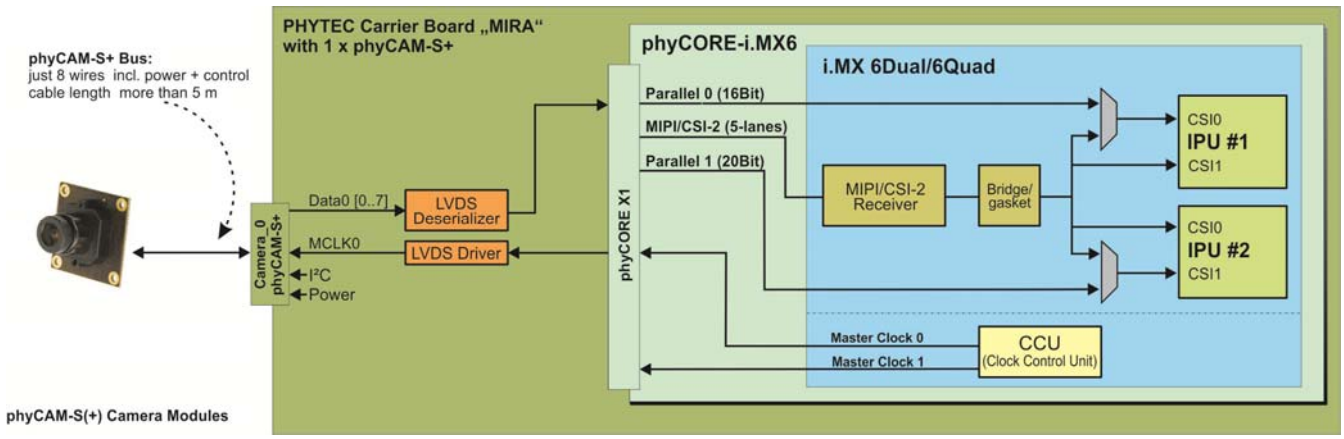


Figure 13: phyCAM-S+ Camera Interface on the phyBOARD-Mira

Figure 14: Camera Interface (phyCAM-S+) at Connector X10

The table below shows the pinout of connector X10.

Pin #	Signal Name	Description
1	Camera0_L0+	LVDS Input+
2	Camera0_L0-	LVDS Input-
3	Camera0_RXCLK-	LVDS Clock-
4	I2C_SDA_CAMERA	I^2C Data
5	I2C_SCL_CAMERA	I^2C Clock
6	Camera0_RXCLK +	LVDS Clock+
7	VCC_CAMERA0	Power supply camera (3.3 V)
8	GND	Ground

Table 11: Phytec Camera Connector X10

2.2.9 HDMI Connectivity (X28)

The phyBOARD-Mira i.MX 6 provides a High-Definition Multimedia Interface (HDMI) which is compliant to HDMI 1.4a, DVI 1.0, HDCP 1.4. It supports a maximum pixel clock of up to 340 MHz for up to 720p at 100 Hz and 720i at 200 Hz, or 1080p at 60 Hz and 1080i/720i at 120 Hz HDTV display resolutions, and a graphic display resolution of up to 2048x1536 (QXGA). Audio streams reach a sampling rate of up to 192 kHz. Please refer to the *i.MX 6 Applications Processor Reference Manual* for more information.

The HDMI interface is brought out at a standard HDMI type A connector (X28) on the phyBOARD-Mira i.MX 6 and comprises the following signal groups: three pairs of data signals, one pair of clock signals, an I²C bus which is exclusively for the HDMI interface, the Consumer Electronics Control (CEC) signal and the hot plug detect (HPD) signal. All signals are routed from the phyCORE-Connector to the HDMI receptacle through an HDMI Transmitter Port Protection and Interface Device. This device provides ESD protection and includes level shifting to shift the I²C interface signals and the hot plug detect signal from IO voltage (VCC3V3) to 5 V. The hot plug detect signal is pulled down to ground at the output of the protection device.

	Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Figure 15: HDMI Interface Connector X28

2.2.10 LVDS Display Connectivity (X9)

Meanwhile there are a few LVDS displays on the market with kind of standardized interfaces. The LVDS display connector X9 is intend to connect these displays with screen diagonals from 7" up to 12.1" at different resolutions.

The display connector X9 is a 20-pole receptacle with 1 mm pitch.

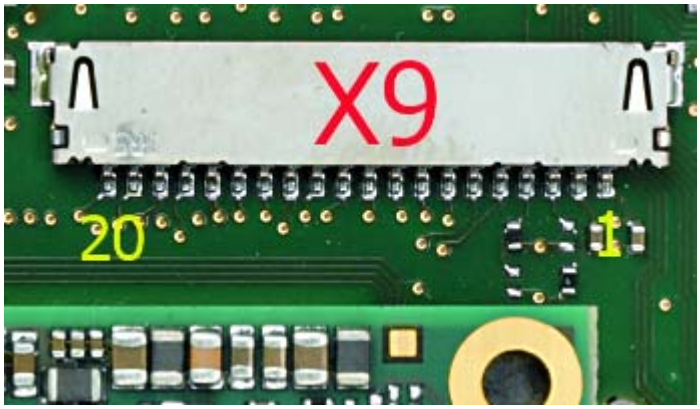


Figure 16: LVDS Display Connector X9

Various solder jumpers and resistors allow to adapt the pin assignment to different displays. If your kit includes a display all jumpers and resistors are preset corresponding to the display.

For more detail information about the pin assignment and how to set up the right configuration for a custom display refer to *section 3.2.5*.

2.2.11 Backlight and Display Control Connector (X8)

In order to support a backlight for the LVDS display X8 provides the supply voltages and control signals necessary.

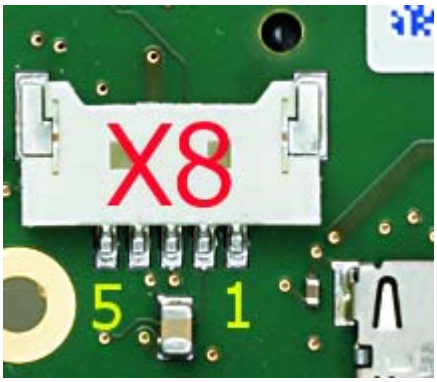


Figure 17: Backlight and Display Control Connector X8

The following table shows the pinout of the 1.25 mm pitch Molex PanelMate™ header.

Pin #	Signal name	ST	SL	Description
1	NC	-	-	Not connected
2	X_PWM1_OUT	O	3.3 V	PWM brightness output
3	X_LVDS_DISP_EN	O	3.3 V	Enable power supply display (Pull-Up R124 default nm)
			5.0 V	Enable power supply display (Pull-Up R109)
4	GND	-	-	Ground
5	VCC_BL	O	NS	Backlight power supply

Table 12: Display Power Connector X8 Signal Description

2.2.12 Touch Screen Connectivity (X13, X21)

As many smaller applications need a touch screen as user interface, different provisions are made to connect as well 4- wire resistive touch screens as various capacitive touch screens. A touch screen can be connected either to the dedicated touch connector X21, or to the touch signal inputs of A/V connector X13.

The following table summarizes the different possibilities available to connect a touch screen to one of these connectors.

Connector	Touch Screen
X21	4-wire resistive touch
X13 (pins 9 – 12)	4-wire resistive touch
X13 (pins 15 – 16)	Capacitive touch screen with I^2C interface

Table 13: Touch Screen Connectivity X13, X21

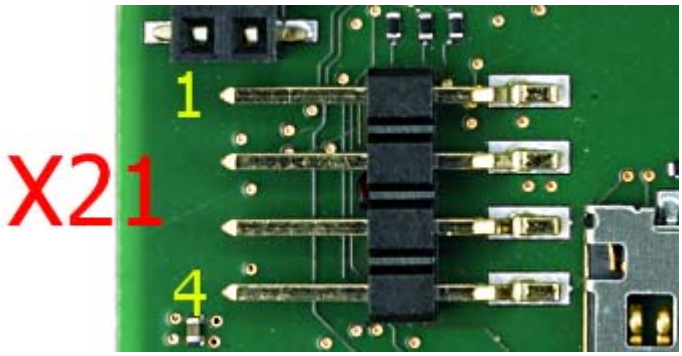


Figure 18: Touch Screen Connectors X21

2.2.13 Multicolor (RGB) LED (D6)

The phyBOARD-Mira provides one multicolor (RGB) LED (D6) (*Figure 2*) for user applications. The colors can be controlled with the following GPIOs

Color	Signal	Description
Red	X_CSI0_DAT4	GPIO5_IO22 of the i.MX 6
Green	X_CSI0_DAT5	GPIO5_IO23 of the i.MX 6
Blue	X_CSI0_DAT6	GPIO5_IO24 of the i.MX 6

Table 14: Multicolor LED Configuration

As an option the LED can be controlled with the LED dimmer IC at U6[7]. The LED dimmer can be accessed via I2C1 at address 0X62 and dynamically controls the LED with PWM signals.

7: The phyBOARD-Mira in the standard kit is not equipped with the LED dimmer. Please contact our sales team for more information.

2.2.14 Boot Mode (S2)

The phyBOARD-Mira has two defined boot sequence which can be selected with DIP switch S2.

Figure 19: Boot Switch (S2)

Boot Mode	Description
Boot mode 1 (S2 = OFF)	Boot from NAND
Boot mode 2 (S2 = ON)	Boot from SD/MMC 1

Table 15: Boot Switch Configuration (S2)

2.2.15 System Reset Button (S1)

The phyBOARD-Mira is equipped with a system reset button at S1. Pressing this button will toggle the X_nRESET pin (X1D32) of the phyCORE SOM low, causing the module to reset.

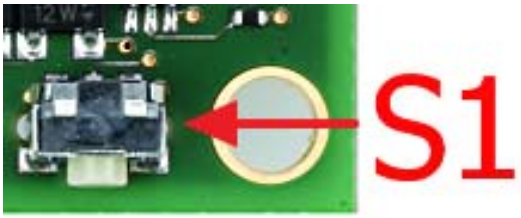


Figure 20: System Reset Button S1

2.2.16 Audio/Video connectors (X13 and X14)

The Audio/Video (A/V) connectors X13 and X14 provide an easy way to add typical A/V functions and features to the phyBOARD-Mira. Standard interfaces such as parallel display, I^2S and I^2C as well as different supply voltages are available at the two A/V female dual entry connectors. Special feature of these connectors are their connectivity from the bottom or the top.

For further information of the A/V connectors see *chapter 3.2.7*. Information on the expansion boards available for the A/V Connectors can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

2.2.17 Expansion connector (X17)

The expansion connector X17 provides an easy way to add other functions and features to the phyBOARD-Mira. Standard interfaces such as JTAG, UART, MMC, SPI and I^2C as well as different supply voltages and some GPIOs are available at the expansion female connector.

For further information of the expansion connector and the pinout see *chapter 3.2.8*. Information on the expansion boards available for the expansion connector can be found in the Application Guide for phyBOARD Expansion Boards (L-793e).

2.2.18 CPU Core Frequency Scaling

The i.MX 6 on the phyBOARD-Mira i.MX 6 is able to scale the clock frequency and the voltage. This is used to save power when the full performance of the CPU is not needed. Scaling the frequency and the voltage is referred to as 'Dynamic Voltage and Frequency Scaling' (DVFS).

The i.MX 6 BSP supports the DVFS feature. The *Linux* kernel provides a DVFS framework that allows each CPU core to have a min/max frequency and a governor that governs it. Depending on the i.MX 6 variant used several different frequencies are supported.

3 System Level Customizing

3.1 About this Section

This section addresses advanced developers who want to design custom expansion boards, or display adapters. It includes detailed information on the different interfaces and features of the phyBOARD-Mira at a system level.

3.2 System Level Hardware Information

3.2.1 Soldering Jumpers

Numerous jumpers and 0 Ohm resistors allow to configure the phyBOARD-Mira according to your needs.

	Due to the small footprint of the jumpers we do not recommend manual jumper modifications. This might also render the warranty invalid. Please contact our sales team if you need one of the configurations described below.

The following table lists all jumpers and resistors, and describes their function.

Jumper / Resistor	Description	See Section
J1	Selecting the reset signal at A/V connector X13	*3.2.7*
J5, J6	Rerouting of the USB OTG interface	*1.1.1*
J9, J10	Rerouting of the USB host interface	
J11	Changing the I^2C address of touchscreen controller U5	
J12	Selecting the reset signal at Mini PCIe connector X7	*3.2.6*
J14	Configuring rising, or falling edge strobe for the LVDS Deserializer of the phyCAM-S+ interface	
J17 – J20 R100 – R108	Adapting display connector X9 to different displays	*3.2.5*
J21 – J23, J25, J26J	Routing of the SIM card signals to expansion connector X17	*3.2.6, 3.2.8*
J28	Configuring the HDMI connector's shield signals	*3.2.4*
R110, R111	Rerouting of the FLEXCAN1 interface	*3.2.3.1*

Table 16: Soldering Jumpers on the phyBOARD-Mira

3.2.2 USB Connectivity

3.2.2.1 Rerouting the USB Interfaces to other Connectors (J5, J6, J9 and J10)

For later expansion boards the USB1 OTG interface can be routed to the expansion connector[8] (X17). Moreover the USB2 host interface can be routed to the Mini PCI Express connector[8] (X7). The following table shows all possible configurations.

Mode	J5	J6
USB1 at USB-OTG connector X5	**1+2**	**1+2**
USB1 at expansion connector X17	2+3	2+3

Table 17: USB1 (USB OTG) Routing Configuration

Mode	J9	J10
USB2 at USB-A connector X6	**1+2**	**1+2**
USB2 at Mini PCIe connector X7	2+3	2+3

Table 18: USB2 (USB host) Routing Configuration

3.2.2.2 Configuring the OTG Operating Mode (R10)

Resistor R10 configures the OTG operating mode. By default this resistor is not ,mounted, which leaves the USB_OTG_ID pin floating, and thus configuring the OTG interface as slave, or according to the configuration of the connected USB device. Mounting a 10 k resistor connects the X_USB_OTG_ID pin to GND, forcing the OTG interface into host mode.

8: **Caution!** There is no protective circuit for the USB interfaces brought out at the expansion connector (X17), or the Mini PCI Express connector (X7).

3.2.3 CAN Connectivity

3.2.3.1 Rerouting the CAN Interface (R110 and R111)

The first CAN interface (FLEXCAN1) can be routed to expansion connector X17. The signals are located at pin 47 (X_FLEXCAN1_TX) and pin 48 (X_FLEXCAN1_RX) of X17. The following table shows the possible configurations for FLEXCAN1.

Mode	J30	J31	U2
FLEXCAN1 at pin header X3	**n.m.**	**n.m.**	**m.**
FLEXCAN1 at expansion connector X17 (TTL level)[9]	2+3	1+2	n.m.

Table 19: Configurations for CAN interface

3.2.3.2 Second CAN Interface at X17

For later expansion boards the second CAN interface (FLEXCAN2) is also available at the expansion connector X17 (*Table 28*).

Usage of FLEXCAN2 at X17 requires changing of the pin muxing and additional software development.

3.2.4 I²C Connectivity

The I2C1 interface of the i.MX 6 is available at different connectors on the phyBOARD-Mira. The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Mini PCIe connector X7	pin 32 (I2C1_SDA), pin 30 (I2C1_SCL)
phyCAM-S connector X10	pin 4 (I2C1_SDA), pin 5 (I2C1_SCL)
Expansion connector X17	pin 11 (I2C1_SDA), pin 13 (I2C1_SCL)
A/V connector X13	pin 16 (I2C1_SDA), pin 15 (I2C1_SCL)

Table 20: I2C1 Connectivity

To avoid any conflicts when connecting external I²C devices to the phyBOARD-Mira the addresses of the on-board I²C devices must be considered. *Table 21* lists the addresses already in use. The table shows only the default address.

9: The standard kit comes with the CAN transceiver installed at U2. Please contact our sales team, if you need the FLEXCAN1 interface at expansion connector X17.

Board	Prod. No.	Device	Address used (7 MSB)
I2C3			
phyCORE-i.MX 6	PCM-058	EEPROM	0x50
		PMIC	0xB0, 0xB1
I2C1			
phyBOARD-Mira	PBA-C-06	Touch controller	0x44
		LED dimmer	0x62
		RTC	0x68
		Mini PCIe	- [10]
		phyCAM-S+	- [10]
AV-Adapter HDMI	PEB-AV-01	HDMI Core	0x70
		CEC Core	0x34
AV-Adapter Display	PEB-AV-02	GPIO Expander	0x41
Evaluation Board	PEB-EVAL-01	EEPROM	0x56
M2M Board	PEB-C-01	GPIO Expander	0x20
		GPIO Expander	0x21
		GPIO Expander	0x22

Table 21: I^2C Addresses in Use

3.2.5 LVDS connector (X9)

In the following table is a complete overview of the LVDS display connector pin assignment.

Pin #	Signal name	Type	SL	Description
1	VCC3V3	OUT	3.3 V	Power supply display[11]
2	VCC3V3	OUT	3.3 V	Power supply display[11]
3	X_LVDS_CONFIG1	OUT	3.3 V	Display configuration pin 1
4	X_LVDS_CONFIG2	OUT	3.3 V	Display configuration pin 2
5	X_LVDS0_TX0-	OUT	3.3 V	LVDS 0 data channel 0 negative output
6	X_LVDS0_TX0+	OUT	3.3 V	LVDS 0 data channel 0 positive output
7	GND	-	-	Ground
8	X_LVDS0_TX1-	OUT	3.3 V	LVDS 0 data channel 1 negative output
9	X_LVDS0_TX1+	OUT	3.3 V	LVDS 0 data channel 1 positive output
10	GND	-	-	Ground

10: Depends on the device connected
11: Provided to supply any logic on the display adapter. Max. draw 100 mA

11	X_LVDS0_TX2-	OUT	3.3 V	LVDS 0 data channel 2 negative output
12	X_LVDS0_TX2+	OUT	3.3 V	LVDS 0 data channel 2 positive output
13	GND	-	-	Ground
14	X_LVDS0_CLK-	OUT	3.3 V	LVDS 0 clock channel negative output
15	X_LVDS0_CLK+	OUT	3.3 V	LVDS 0 clock channel positive output
16	GND	-	-	Ground
17	X_LVDS_CONFIG3	OUT	3.3 V	Display configuration pin 3 or LVDS 0 data channel 3 negative output
18	X_LVDS_CONFIG4	OUT	3.3 V	Display configuration pin 4 or LVDS 0 data channel 3 positive output
19	X_LVDS_CONFIG5	OUT	3.3 V	Display configuration pin 5 or LVDS 0 data channel 3 negative output
20	X_LVDS_CONFIG6	OUT	3.3 V	Display configuration pin 6 or LVDS 0 data channel 3 positive output

Table 22: Pin Assignment LVDS Display Connector X9

Various solder jumpers and resistors allow to adapt the pin assignment to different displays. If your kit includes a display all jumpers and resistors are preset corresponding to the display. The following table gives an overview of possible configurations. Please consider the data sheet of the display used to find the right settings.

Pin #	Signal name	J or R	Setting	Description
3	X_LVDS_CONFIG1	R101[12]	if mounted	High level
		R103[12]	**if mounted**	**Low level**
4	X_LVDS_CONFIG2	**R100[12]**	**if mounted**	**High level**
		R102[12]	if mounted	Low level
17	X_LVDS_CONFIG3	J17	1+2	High level
			2+3	**X_LVDS0_TX3- connected**
18	X_LVDS_CONFIG4	J18	**closed**	**X_LVDS0_TX3+ connected**
			open	Not connected
19	X_LVDS_CONFIG5	J19	1+2	X_LVDS0_TX3- connected
			2+3	High level if R106[12] is mounted Low level if R108[12] is mounted
20	X_LVDS_CONFIG6	J20	1+2	X_LVDS0_TX3+ connected
			2+3	**High level if R105[12] is mounted** Low level if R107[12] is mounted

Table 23: Configuration for LVDS Display Connector X9

Due to the small footprint of the jumpers and resistors we do not recommend manual jumper modifications. This might also render the warranty invalid. Please contact our sales team if you need one of the configurations described.

12: All configuration resistors have a value of 10 k.

3.2.6 Mini PCI Express Connector (X7)

In the following table is a complete overview of the Mini PCI Express connector pin assignment.

Pin #	Signal name	Type	SL	Description
1	X_ECSPI2_MOSI/PCIe_nWAKE	IN	3.3 V	PCIe WAKE
2	VCC3V3	OUT	3.3 V	3.3 V power supply
3	X_ECSPI2_SS0/PCIe_COEX1	I/O	3.3 V	Coexistence pins for wireless solutions
4	GND	-	-	Ground
5	X_CSI1_DATA06/PCIe_COEX2	I/O	3.3 V	Coexistence pins for wireless solutions
6	VCC1V5	OUT	1.5 V	1.5 V power supply[13]
7	X_ECSPI2_SCLK/PCIe_nCLKREQ	IN	3.3 V	Clock request support
8	X_SIM_VCC	IN	-	UIM_PWR[14]
9	GND	-	-	Ground
10	X_SIM_IO	I/O	-	UIM_DATA[14]
11	X_PCIe0_CLK-	OUT	DIFF	PCIe0 reference clock -
12	X_SIM_CLK	IN	-	UIM_CLK[14]
13	X_PCIe0_CLK+	OUT	DIFF	PCIe0 reference clock +
14	X_SIM_RST	IN	-	UIM_RESET[14]
15	GND	-	-	Ground
16	X_SIM_VPP	IN	-	UIM_VPP[14]
17	RSVD3	-	-	Not connected
18	GND	-	-	Ground
19	RSVD4	-	-	Not connected
20	X_EIM_DA14/PCIe_nW_DISABLE	OUT	3.3 V	Wireless disable signal
21	GND	-	-	Ground
22	X_ECSPI2_MISO/PCIe_nPERST or X_nRESET (J12 1+2)	OUT	3.3 V	Functional card reset by GPIO or X_nRESET
23	X_PCIe_RXN	IN	DIFF	PCIe receive -
24	VCC3V3	OUT	3.3 V	3.3 V power supply
25	X_PCIe_RXP	IN	DIFF	PCIe receive +
26	GND	-	-	Ground

Table 24: Mini PCI Express Connector X7

13: The 1.5 V voltage can be switched OFF with signal X_CSI1_DATA09/EN_VCC1V5.
14: User Identity Module (UIM) signals

Pin #	Signal name	Type	SL	Description
27	GND	-	-	Ground
28	VCC1V5	OUT	1.5 V	1.5 V power supply
29	GND	-	-	Ground
30	X_I2C1_SCL	I/O	3.3 V	I2C1 clock
31	X_PCIe_TXN	OUT	DIFF	PCIe transmit -
32	X_I2C1_SDA	I/O	3.3 V	I2C1 data
33	X_PCIe_TXP	OUT	DIFF	PCIe transmit +
34	GND	-	-	Ground
35	GND	-	-	Ground
36	X_USB2_DM_PCIe	I/O	DIFF	USB host data -[15, 16]
37	GND	-	-	Ground
38	X_USB2_DP_PCIe	I/O	DIFF	USB host data +[15, 16]
39	VCC3V3	OUT	3.3 V	3.3 V power supply
40	GND	-	-	Ground
41	VCC3V3	OUT	3.3 V	3.3 V power supply
42	TP6	IN	NS	Test point for LED_WWAN
43	GND	-	-	Ground
44	TP7	IN	NS	Test point for LED_WLAN
45	RSVD9	-	-	Not connected
46	TP8	IN	NS	Test point for LED_WPAN
47	RSVD10	-	-	Not connected
48	VCC1V5	OUT	1.5 V	1.5 V power supply[17]
49	RSVD11	-	-	Not connected
50	GND	-	-	Ground
51	RSVD12	-	-	Not connected
52	VCC3V3	OUT	3.3 V	3.3 V power supply
S1	GNDM1	-	-	Ground
S2	GNDM2	-	-	Ground

Table 24: Mini PCI Express Connector X7 (continued)

15: J9 and J10 need to be set to 2+3 to route the USB2 host interface to the Mini PCI Express connector (*Table 18*).
16: **Caution!** There is no protective circuit for the USB interfaces brought out at the Mini PCI Express connector (X7).
17: The 1.5 V voltage can be switched OFF with signal X_CSI1_DATA09/EN_VCC1V5.

3.2.7 Audio/Video connectors (X13 and X14)

Audio/Video (A/V) connectors X13 and X14 provide an easy way to add typical A/V functions and features to the phyBOARD-Mira. Standard interfaces such as parallel display, I^2S and I^2C as well as different supply voltages are available at the two A/V female dual entry connectors. Special feature of these connectors are their connectivity from the bottom or the top. The pinout of the A/V connectors is shown in *Table 25* and *Table 26*.

The A/V connector is intended for use with phyBOARD Expansion Boards[18], and to add specific audio/video connectivity with custom expansion boards.

Figure 21: Audio/Video Connectors (X13and X14)

A/V connector X14makes all signals for display connectivity available, while X13 provides signals for audio and touch screen connectivity, as well as an I^2C bus and additional control signals.

18: Please find additional information on phyBOARD Expansion Boards in the corresponding application guide (L-793e).

Pin #	Signal Name	Type	SL	Description
1	GND	-	-	Ground
2	X_LCD_DATA16	OUT	3.3V	LCD Data 16 – red 0
3	X_LCD_DATA17	OUT	3.3 V	LCD Data 17 – red 1
4	X_LCD_DATA18	OUT	3.3 V	LCD Data 18 – red 2
5	X_LCD_DATA19	OUT	3.3 V	LCD Data 19 – red 3
6	GND	-	-	Ground
7	X_LCD_DATA20	OUT	3.3 V	LCD Data 20 – red 4
8	X_LCD_DATA21	OUT	3.3 V	LCD Data 21 – red 5
9	X_LCD_DATA22	OUT	3.3 V	LCD Data 22 – red 6
10	X_LCD_DATA23	OUT	3.3 V	LCD Data 23 – red 7
11	GND	-	-	Ground
12	X_LCD_DATA8	OUT	3.3 V	LCD Data 8 – green 0
13	X_LCD_DATA9	OUT	3.3 V	LCD Data 9 – green 1
14	X_LCD_DATA10	OUT	3.3 V	LCD Data 10 – green 2
15	X_LCD_DATA11	OUT	3.3 V	LCD Data 11 – green 3
16	GND	-	-	Ground
17	X_LCD_DATA12	OUT	3.3 V	LCD Data 12 – green 4
18	X_LCD_DATA13	OUT	3.3 V	LCD Data 13 – green 5
19	X_LCD_DATA14	OUT	3.3 V	LCD Data 14 – green 6
20	X_LCD_DATA15	OUT	3.3 V	LCD Data 15 – green 7
21	GND	-	-	Ground
22	X_LCD_DATA00	OUT	3.3 V	LCD Data 00 – blue 0
23	X_LCD_DATA01	OUT	3.3 V	LCD Data 01 – blue 1
24	X_LCD_DATA02	OUT	3.3 V	LCD Data 02 – blue 2
25	X_LCD_DATA03	OUT	3.3 V	LCD Data 03 – blue 3
26	GND	-	-	Ground
27	X_LCD_DATA04	OUT	3.3 V	LCD Data 04 – blue 4
28	X_LCD_DATA05	OUT	3.3 V	LCD Data05 – blue 5
29	X_LCD_DATA06	OUT	3.3 V	LCD Data 06 – blue 6
30	X_LCD_DATA07	OUT	3.3 V	LCD Data 07 – blue 7
31	GND	-	-	Ground
32	X_LCD_CLK	OUT	3.3 V	LCD Pixel Clock
33	X_LCD_ENABLE	OUT	3.3 V	LCD BIAS ENABLE

Table 25: Phytec A/V connector X14

Pin #	Signal Name	Type	SL	Description
34	X_LCD_HSYNC	OUT	3.3 V	LCD Horizontal Synchronization
35	X_LCD_VSYNC	OUT	3.3 V	LCD Vertical Synchronization
36	GND	-	-	Ground
37	GND	-	-	Ground
38	X_PWM1_OUT	OUT	3.3 V	Pulse Width Modulation
39	VCC_BL	OUT	NS	Backlight power supply[19]
40	VCC5V	OUT	5.0 V	5.0 V power supply

Table 25: Phytec A/V connector X14 (continued)

Pin #	Signal Name	Type	SL	Description	
1	X_AUD5_TXC	I/O	3.3 V	I²S Clock	
2	X_AUD5_TXFS	I/O	3.3 V	I²S Frame	
3	X_AUD5_RXD	I/O	3.3 V	I²S Analog-Digital converter (microphone)	
4	X_AUD5_TXD	I/O	3.3 V	I²S Digital-Analog converter (speaker)	
5	X_CSI1_DATA07/AV_INT	I/O	3.3 V	A/V interrupt, GPIO3_02[20]	
6	X_CSI1_DATA10/LCD_PWCTRL	OUT	3.3 V	LCD control, GPIO3_22	
7	GND	-	-	Ground	
8	X_nRESET	OUT	3.3 V	Reset[21]	(J1 1+2)
	X_LCD_RESET	OUT	3.3 V	Reset LCD	(**J1 2+3**)
9	TS_X+	IN	1.8 V	Touch X+	
10	TS_X-	IN	1.8 V	Touch X-	
11	TS_Y+	IN	1.8 V	Touch Y+	
12	TS_Y-	IN	1.8 V	Touch Y-	
13	VCC3V3	OUT	3.3 V	3.3 V power supply	
14	GND	-	-	Ground	
15	X_I2C1_SCL	I/O	3.3 V	I2C1 Clock	
16	X_I2C1_SDA	I/O	3.3 V	I2C1 Data	

Table 26: Phytec A/V connector X13

Jumper J1 connects either signal X_LCD_RESET or signal X_nRESET to pin 8 of X13. The following table shows the available configurations:

19: Voltage level is not specified and depends on the connected power module and the attached voltage.
20: **Note:** The A/V interrupt must be enabled with signal X_CSI1_DATA05_EN_SWITCH (GPIO3_04).
21: Reset signal depends on J1, please refer to *Table 27* for more information.

J1	Description
1+2	X_nRESET
2+3	**X_LCD_RESET**

Table 27: A/V Jumper Configuration J1

3.2.8 Expansion Connector (X17)

Expansion connector X17 provides an easy way to add other functions and features to the phyBOARD-Mira. Standard interfaces such as UART, SPI and I^2C as well as different supply voltages and some GPIOs are available at the expansion female connector.

The expansion connector is intended for use with phyBOARD Expansion Boards[22], and to add specific functions with custom expansion boards.

Figure 22: Expansion Connector (X17)

The pinout of the expansion connector is shown in the following table.

Pin #	Signal Name	Type	SL	Description
1	VCC3V3	OUT	3.3 V	3.3 V power supply
2	VCC5V	OUT	5.0 V	5.0 V power supply
3	VCC1V5	OUT	1.5 V	1.5 V power supply[23]
4	GND	-	-	Ground
5	X_ECSPI1_SS0	OUT	3.3 V	SPI 1 chip select 0
6	X_ECSPI1_MOSI	OUT	3.3 V	SPI 1 master output/slave input
7	X_ECSPI1_MISO	IN	3.3 V	SPI 1 master input/slave output
8	X_ECSPI1_SCLK	OUT	3.3 V	SPI 1 clock output
9	GND	-	-	Ground
10	X_UART2_RX_DATA	IN	3.3 V	UART 2 receive data (standard debug interface)
11	X_I2C1_SDA	I/O	3.3 V	I2C 1 Data
12	X_UART2_TX_DATA	OUT	3.3 V	UART 2 transmit data (standard

22: Please find additional information on phyBOARD-Mira i.MX 6 Expansion Boards in the corresponding application guide (L-793e).

23: The 1.5 V voltage can be switched OFF with signal X_CSI1_DATA09/EN_VCC1V5.

				debug interface)
13	X_I2C1_SCL	I/O	3.3 V	I2C 1 Clock
14	GND	-	-	Ground
15	X_JTAG_TMS	IN	3.3 V	JTAG Chain Test Mode Select signal

Table 28: Phytec Expansion Connector X17

16	X_JTAG_TRSTB	IN	3.3 V	JTAG Chain Test Reset	
17	X_JTAG_TDI	IN	3.3 V	JTAG Chain Test Data Input	
18	X_JTAG_TDO	OUT	3.3 V	JTAG Chain Test Data Output	
19	GND	-	-	Ground	
20	X_JTAG_TCK	IN	3.3 V	JTAG Chain Test Clock signal	
21	X_USB1_DP_EXP	I/O	DIFF	USB host data +[24, 25]	
22	X_USB1_DM_EXP	I/O	DIFF	USB host data -[24, 25]	
23	X_nRESET	OUT	3.3 V	Reset	
24	GND	-	-	Ground	
25	X_SD3_CMD	I/O	3.3 V	SD/MMC command	
26	X_SD3_DATA0	I/O	3.3 V	SD/MMC data 0	
27	X_SD3_CLK	I/O	3.3 V	SD/MMC clock	
28	X_SD3_DATA1	I/O	3.3 V	SD/MMC data 1	
29	GND	-	-	Ground	
30	X_SD3_DATA2	I/O	3.3 V	SD/MMC data 2	
31	X_CSI0_DAT11/ECSPI2_SS0	I/O	3.3 V	SPI2 chip select 0, UART1 RX, GPIO5_29	
32	X_SD3_DATA3	I/O	3.3 V	SD/MMC data 3	
33	X_CSI0_DAT10/ECSPI2_MISO	I/O	3.3 V	SPI2 MISO, UART1 TX, GPIO5_28	
34	GND	-	-	Ground	
35	X_SD3_DATA4	I/O	3.3 V	SD/MMC data 4, UART2 RX[26]	
36	X_SD3_DATA5	I/O	3.3 V	SD/MMC data 5, UART2 TX	
37	X_SATA_TXP	OUT	DIFF	SATA transmit positive	
38	X_SD3_DATA6	I/O	3.3 V	SD/MMC data 6	
39	X_SATA_TXN	OUT	DIFF	SATA transmit negative	
40	X_SD3_DATA7	I/O	3.3 V	SD/MMC data 7	
41	GND	-	-	Ground	
42	X_ECSPI2_RDY/nPMON_PWRFAIL	OUT	3.3 V	Power fail signal	(**J26 1+2**)
	X_SIM_VPP	-	-	UIM_VPP	(J26 2+3)
43	X_SATA_RXP	IN	DIFF	SATA receive positive	
44	X_CSI0_DAT8/ECSPI2_SCLK	OUT	3.3 V	SPI 2 clock output	(**J21 1+2**)
	X_SIM_VCC	OUT	-	UIM VCC	(J21 2+3)

Table 28: Phytec Expansion Connector X17 (continued)

24: J5 and J6 need to be set to 2+3 to route the USB1 OTG interface to the expansion connector (*Table 17*).
25: **Caution!** There is no protective circuit for the USB interfaces brought out at the expansion connector (X17).
26: **Caution!** If the UART2 signals are redirected to these pins the standard console is not available on the Evaluation Board (PEB-EVAL-01).

45	X_SATA_RXN	IN	DIFF	SATA receive negative	
46	GND	-	-	Ground	
47	X_FLEXCAN1_TX_EXP	OUT	3.3 V	CAN 1 transmit data[27]	(J30 2+3)
	X_PMIC_nONKEY	IN	3.3 V	PMIC nONKEY	(**J30 1+2**)
48	X_FLEXCAN1_RX_EXP	IN	3.3 V	CAN 1 receive data[27]	(J31 1+2)
49	X_USB_OTG_OC/FLEXCAN2_TX	OUT	3.3 V	CAN 2 transmit data	
50	X_USB_OTG_PWR/FLEXCAN2_RX	IN	3.3 V	CAN 2 receive data	
51	GND	-	-	Ground	
52	X_CSI0_DAT9/ECSPI2_MOSI	OUT	3.3 V	SPI 2 MOSI	(**J25 1+2**)
	X_SIM_RST	OUT	-	UIM Reset	(J25 2+3)
53	X_USB1_ID	IN	3.3 V	USB 1 identification	
54	X_USB1_VBUS	OUT	5.0 V	USB 1 bus voltage	
55	X_USB_OTG_CHD_B	OUT	3.3 V	USB 1 charger enable	(**J23 1+2**)
	X_SIM_IO	OUT	-	UIM Data	(J23 2+3)
56	GND	-	-	Ground	
57	VCC_BL	OUT	NS	Backlight power supply[28]	
58	X_ECSPI2_SS1	OUT	3.3 V	SPI 2 chip select 1	(**J22 1+2**)
	X_SIM_CLK	OUT	-	UIM Clock	(J22 2+3)
59	GND	-	-	Ground	
60	VCC5V_IN	IN	5.0 V	5 V input supply voltage	

Table 28: Phytec Expansion Connector X17 (continued)

27 : Please refer to section 3.2.3 to make CAN 1 available on expansion connector
28 : Voltage level is not specified and depends on the connected power module and the attached voltage.

4 Revision History

Date	Version #	Changes in this manual
16.10.2017	Manual L-843e_0	First edition based on the AppGuide (L-806e_2) Describes the phyCORE-i.MX 6 SOM (PCB 1429.5) with phyBOARD-Mira-Carrier Board (PCB 1434.3)

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