Front-end Firmware Transition and Documentation Status/Plans/Proposals

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v2 Firmware

- "Version 2" firmware is largely done:
  - New interface to the DAQ system.
    - Memory mapped registers for all current commands and auxiliary data readback.
    - New packet formats, inbound and outbound.
  - Selective digitization and readout.
    - Variable data size and new packet formats
  - Made for IRS2 Daughter Card Rev.B2.

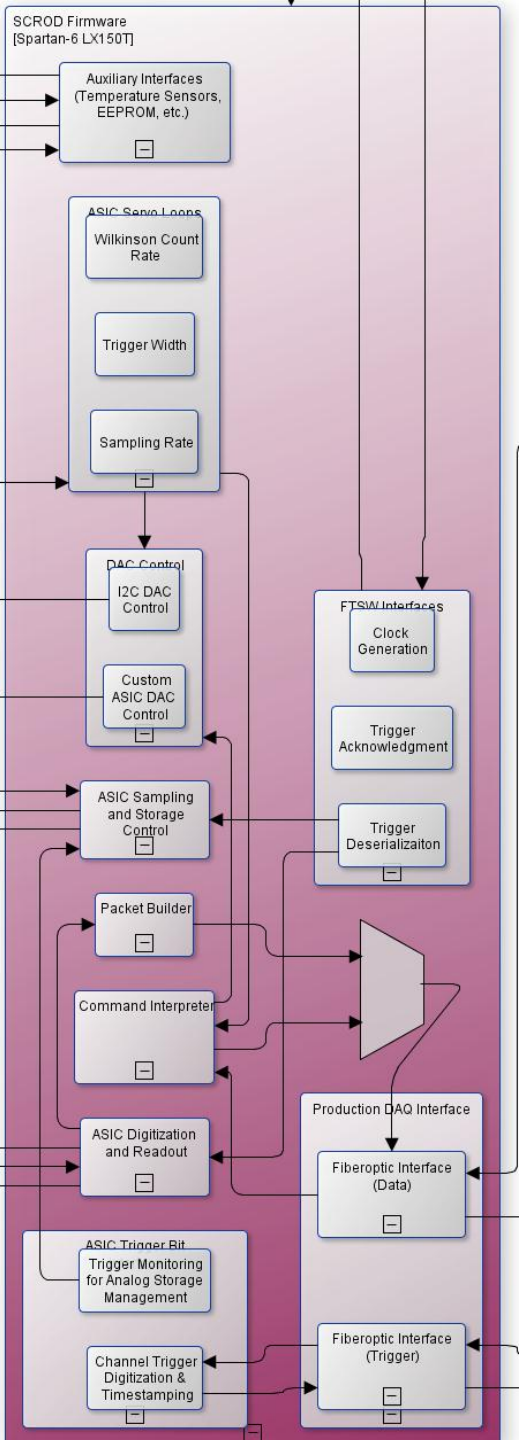
What's left to do for v2 firmware?

- Currently version:
  - http://idlab-scrod.googlecode.com
  - Path: SCROD-boardstack/new_daq_interface
    - (Should migrate to trunk at some point.)
- Since v2 will (hopefully) never be used for actual data acquisition, we do not need the following, still unimplemented features:
  - Distributed clocking (e.g., FTSW support).
  - Trigger interface (to GDL).
- Nevertheless, this firmware is useful as-is, or almost as-is for other projects:
  - I would like to add at least one more feature (probably on my own time): PLL dynamic reconfiguration.
    - Will allow for software-reconfiguration of sampling/storage clocks to support arbitrary sampling rates, etc.

Moving to v3 (i.e., IRS3B)

- I hope that I have made a flexible infrastructure that can relatively easily be maintained/expanded for v3 firmware.
- Three main pieces of documentation I am developing:
  1. Installation/compilation instructions for v2.
     - Already aware of a few extra installation instructions regarding command_interpreter.vhd
  2. Firmware documentation: description of blocks and overall integration.
  3. Interface document: for each system back-end can control, what does it do and how to use it.
- Will distribute links as they become available.

Firmware Statuses and Future Maintainers/Updaters(?)



Auxiliary interfaces (Matt A. + ??):

- Generic I2C interface (EEPROM, temp sensors, fiberoptic transceiver diagnostics)
  - Exists, working, recommend no/minimal changes for v3.

IRS3B control (Luca, Gary, Matt A.):

- Sampling and storage
  - Written for IRS2, must be changed for IRS3B.
- Trigger memory for region-of-interest mapping.
  - Exists, could use more testing.
- Region-of-interest
  - Exists, working, recommend minimal/no changes for v3.
- Digitizer + packet builder
  - Written for IRS3, must be changed for IRS3B.
  - Packet building can remain largely the same.
- ASIC feedback (+Leonid S., +Lynn W.)
  - Simple proportional feedback exists for Wilkinson rate, needs more testing.
  - Nothing yet on trigger width or sampling rate.

Command interpreter (Matt A. + ??)

- Picoblaze assembly code
  - Verified working, recommend only changing when absolutely necessary (e.g., change startup sequencing).
- Memory mapped register assignment
  - May need changes regularly for new functionality.

General fiberoptic (Matt A.+Ryan C.?)

- Verified working w/ Aurora.
- May require revamping for Belle II Link-like interface.

Trigger functionality (Eric C.? + ??)

- Trigger scalers exist, working. Recommend no/minimal changes.
- Trigger time stamping + data to back-end trigger system, not implemented (fiberoptic slot reserved).

FTSW interface (?? + M. Nakao)

- Mainly need to interface with Nakao-san on future FTSW updates.