Experimental characterization of the TOFPET2 ASIC

R. Bugalho^b, A. Di Francesco^a, L. Ferramacho^b, C. Leong^b, T. Niknejad^{a,b}, L. Oliveira^c, M. Rolo^d, J. C. Silva^{a,b}, R. Silva^{a,b}, M. Silveira^b, S. Tavernier^{b,e}, J. Varela^{a,b*}

 ^a LIP, Lisbon, Portugal
^b PETsys Electronics, Oeiras, Portugal
^c DEE, CTS-UNINOVA FCT-UNL, Caparica, Portugal
^d INFN – sez. Torino, Italia
^e Vrije Universiteit Brussel, Belgium

E-mail: joao.varela@cern.ch

ABSTRACT: We present the experimental characterization of the TOFPET2, a readout and digitization ASIC for radiation detectors using Silicon Photomultipliers. The circuit is designed in CMOS 110 nm technology, has 64 independent channels and is optimized for time-of-flight measurement in PET or other applications. The chip has quad-buffered TDCs and charge integration QDCs in each channel. The Coincidence Time Resolution (CTR) of 511 keV photon pairs from a ²²Na point source measured with 2x2x3 mm³ LSO:Ce crystals co-doped with 0.2% Ca is 118 and 119 ps FWHM when using respectively the SiPMs NUVHD 40um from Fondazione Bruno Kessler (FBK) and the S14160-3050HS MPPC from Hamamatsu Photonics (HPK). The energy resolution obtained for the 511keV photopeak is 10.5 and 12% FWHM when using respectively the SiPMs PM3325-WB from KETEK and the QFBR-S4N44P164S from Broadcom Inc.

KEYWORDS: TOFPET2, PET, Time-of-flight.

^{*} Corresponding author

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1. Introduction

The TOFPET2 ASIC is a low-power, low-noise, readout and digitization chip implemented in 110nm CMOS technology for fast radiation detectors used in Time-of-Flight (ToF) applications. The chip integrates signal amplification circuitry, discriminators, charge integration QDCs and high-performance TDCs for each of 64 independent channels. The circuit is an evolution of the TOFPET1 ASIC for Positron Emission Tomography (PET) applications using ToF information [1].

The TOFPET2 ASIC has 64 independent channels, each containing independent amplifiers, discriminators, time-to-digital converters and charge-to-digital converters (see **Figure 1**). The input pre-amplifier (*P*) provides a low impedance input (R_{IN}) to the sensor's output current signal. The input current I_{IN} is then replicated into 3 branches: *T*, *E* and *Q*.

The *T* and *E* branches have trans-impedance amplifiers (TIA) with configurable gains. The outputs of these modules are fed into discriminators for timing measurement (*T*) and hit selection (*E*). Each TIA is a PMOS current mirror replicating the AC part of the preamplifier current output on a resistor. The Q branch integrates a replica of the input current.

The output *Vout_T* connects to two identical discriminators (D_T1 and D_T2) whose threshold voltages (*Vth_T1* and *Vth_T2*) are set by 6-bit DACs. The offset *Vbaseline_T* is set by another 6-bit DAC and is used to trim the baseline of *Vout_T* relatively to the input of the discriminators. The LSB of the T1 and T2 thresholds are set globally in the ASIC settings. The discriminators output signals are used to control the ASIC internal triggering logic. Branch *E* is similar to branch *T*, with the following differences: the gain G_E of the trans-impedance amplifier is lower allowing a higher range of signals before saturation and its output feeds a single discriminator D_{-E} .



Figure 1. TOFPET2 channel architecture.

The output of the 3 discriminators connects to the Trigger Generator logic box which generates trigger signals *trigger_T*, *E*, *Q* and *B* (see **Figure 1**). The output of discriminator T1 (do_T1) passes through a configurable delay line (do_T1') . Due to this delay, the time of the rising edge of *trigger_T* is actually the time of the rising edge of $D_T1 + DELAY$. TOFPET2 implements a multi-level event trigger and rejection scheme. In nominal operation mode:

- Event time is measured at a low threshold (*Vth_T1*) than can be set as low as 0.25 p.e.
- Events that do not trigger threshold *Vth* T2 are rejected without any dead time.
- Events that trigger *Vth_T2* but not *Vth_E* are rejected with 5 clock period dead time.
- Only events that trigger all 3 thresholds are considered valid and digitized.

The ASIC can be configured in Time and Charge mode or in Dual Time mode. In both cases the *TDC T* measures the time of the rising edge of *trigger_T*. In Time and Charge mode, the *QDC* measures the charge integrated from the rising edge of do_T2 until the end of the (configurable) integration window. In Dual Time mode, the *TDC E* measures the time of the falling edge of do_E . In this mode, the time measurements can be used to estimate the width of the signal (Time over Threshold-ToT).

The TDCs are composed of a time-to-amplitude converter (TAC) followed by a 10-bit Wilkinson ADC 10-bit (see **Figure 1**). On the rising edge of *trigger_T*, switch SW_T closes, charging analog buffer C_T with current I_{TDC} . On the next rising edge of CLK, SW_T opens, stopping the charging process. The value of a global clock counter is latched providing the value *t coarse*. If the event is valid (E> *Vth_E*), the voltage stored in C_T is digitized as *t fine*. The *TDC E* operates identically using the *trigger_E* signal. The QDC is composed of a charge-to-amplitude converter (QAC) followed by a 10-bit Wilkinson ADC (shared with TDC E). On the rising edge of *trigger Q*, switch SW_Q closes, charging analog buffer C_Q with a replica of the

input current signal plus a DC current. SW_Q opens when the integration time has been reached. If the event is valid, the charge stored in C_Q is digitized.

Each channel has 4 sets of C_T , C_E and C_Q buffers where analog values are stored before being digitized. Every time the channel goes through the rearm state, a new buffer set is selected round-robin. This allows the channel to rearm without waiting for the previous event to be digitized. When an event is valid and digitized, the number of the analog buffer set used to process that event is transmitted along the event. Due to process variations, the analog buffers need to be calibrated for optimal results.

TOFPET2 includes event counters that allow events to be counted without being transmitted (and thus, not subject to event conversion and transmission limitations). In this context, events are programmable logical combinations of the discriminators outputs. The counting period is globally configurable up to 2^{24} clock cycles.

TOFPET2 has a circuit which injects an analog *Test Pulse* directly into channel's SiPM input node. This pulse has adjustable amplitude and is generated in response to a digital signal provided by the control logic. The circuit is shared by all the channels and each channel has a switch to select whether or not that channel's input node is connected to the global analog test pulse generator.

In the 2016, we have presented results obtained with the first version of TOFPET2 [2]. These measurements showed a time resolution larger than expected. The source of the timing degradation was identified to be the parasitic capacitance introduced by dummy fillings in the metal layers above the discriminator input lines.

A revised version of TOFPET2 was produced in 2017. First experimental results with TOFPET2 Rev-b have been reported in [3]. In this paper, we present the results of the characterization of TOFPET2 Rev-c obtained with internal test pulses, with laser pulses detected by different types of silicon-photomultipliers (SiPM), and with gamma rays from radioactive sources detected with LYSO crystals coupled to different SiPMs.

A more detailed description and simulation results of the TOFPET2 can be found in [4]. The TOFPET2 Rev-c datasheet is available in [5].

2. Test setup

The evaluation of the TOFPET2 ASIC was done using the PETsys TOFPET2 Evaluation Kit [6]. The evaluation kit (**Error! Reference source not found.**) is a complete readout system allowing to read two TOFPET2 ASICs. The evaluation kit has two TOFPET2 ASIC test boards and one FPGA board, hereafter called FEB/D board, with an Ethernet link. Each test board has one ASIC reading 64 channels. The test boards have connectors that directly accept the HPK S13361-350Ax-08 8x8 MPPC array or the KETEK PA3325-WB-0808 array. With some small adapters, these test boards could be used to read analog SiPMs from other vendors.

Flexible cables connect the TOFPET2 ASIC test boards to the FEB/D board. The FEB/D unit provide the ASIC test boards with all the necessary power, SiPM bias voltages, configuration and readout. The kit is provided with the firmware and software needed for acquiring and analysing the signals of the two ASICs, thus enabling the simultaneous operation of up to 128 channels. The test boards and the associated detectors based on LYSO crystals and SiPMs were operated inside a thermally stabilized dark chamber. Unless specified otherwise, all measurements were done at 20°C.



Figure 2. TOFPET2 Evaluation Kit.

3. ASIC intrinsic performance

The intrinsic performance of the ASIC was characterized by making use of the ASIC internal test features, without external stimulus other than the system clock and an external digital test pulse. In some cases, specified below, the characterization was done with SiPMs connected to the ASIC inputs. In the following sub-sections, we organize the presentation by ASIC block, discussing for each one the characterization parameters and the measurements performed.



Figure 3. Relative count rate with the SiPM bias voltage below breakdown as a function of the timing discriminator threshold, for KETEK-PM3325-WB SiPM (left) and HPK S13361-3050AE-04 MPPC (right). The DAC LSB is 3 mV.

3.1 Frontend amplifiers and discriminators

The characterization of the electronics noise was performed with a threshold scan above the baseline at the output of the timing post-amplifier. The threshold voltage is adjusted with a programmable Digital-to-Analog Converter (DAC) in the ASIC. The voltage corresponding to the DAC least significant bit (LSB) is also configurable. The ASIC inputs were connected to SiPMs. In the measurement of electronics noise, the SiPMs were biased slightly below the breakdown voltage such that the SiPM capacitance is close to nominal. These data were collected using the internal counters of the ASIC. The relative count rate was fitted with a s-curve yielding the standard deviation of the electronics noise. We measure $\sigma^{noise}=0.59$ DAC units with KETEK-PM3325-WB and $\sigma^{noise}=0.53$ DAC units with HPK S13361-3050AE-04 MPPC (Figure 3). From the simulation of the ASIC typical corner, one DAC count corresponds to 3 mV for the settings used in these tests.

The same technique was used to measure the average amplitude of single photon pulses. **Figure 4** shows the dark count rate as a function of the discriminator threshold measured with the HPK S13361-3050AE-04 MPPC biased at 3.5 V overvoltage and the KETEK-PM3325-WB SiPM biased at 4.0 V overvoltage. The plateaus relative to different numbers of photo-electrons are clearly visible. The amplitude of the single photo-electron (p.e.) signal measured with the HPK S13361-3050AE-04 MPPC is 9 DAC counts (27 mV) while with the KETEK-PM3325-WB SiPM it is 5 DAC counts (15 mV).



Figure 4. Dark count rate as a function of the discriminator threshold measured with the S13361-3050AE-04 MPPC biased at 3.5 V overvoltage and with the KETEK-PM3325-WB SiPM biased at 4.0 V overvoltage.

3.2 TDC performance

The linearity of the TDC is measured with random pulses that follow a uniform distribution in time. Photons from a ²²Na source measured with a LYSO crystal and a SiPM are used for this

purpose. **Figure 6** shows the Differential Non Linearity (DNL) and the Integral Non Linearity (INL) as a function of the ADC code obtained for a typical TAC. DNL is less than 0.2 LSB and the INL is less than 1 LSB. The small intrinsic non-linearity of the TDC could be corrected by the calibration procedure using test pulses or the code density method.

Although individual TACs exhibit a good linear behavior, due to process variations there are sizable differences between offsets and bin sizes across different TACs. The timing calibration is obtained either from the code density measured with random pulses or from external test pulses. In the latter case, the TDC calibration uses an external digital pulse synchronous to the system clock and distributed internally to the input of the TDCs in the chip. The firmware and software of the TOFPET2 evaluation kit allows to scan the time of the test pulse relative to the clock edge in programmable steps of a few tens of picosecond.



Figure 5. TDC differential non-linearity (left) and integrated non-linearity (right). The DNL and INL are plotted as a function of the ADC code after pedestal subtraction.

The output of the calibration includes a parametrization of the TDC non-linearity as well as the measurement of the TDC bin size. **Figure 6** shows the distribution of the TDC binning in two ASICs for an external clock of 200 MHz. The measured values correspond to 2 chips x 64 channels x 4 TAC x 2 branches. The TDC bin is 31 ± 3 ps.



Figure 6. Distribution of the TDC binning measured in 2 chips. For each chip, there are 64 channels and 8 measurements per channel (4 TACs x 2 branches).

The performance of the TDC when multiple ASIC channels are active was evaluated by comparing the time measured by one channel TDC as a function of the activity in the other ASIC channels. Figure 7 shows the difference of the time measurements in one channel when test pulses are distributed simultaneously to 1 or 64 channels. The test pulse is synchronous to clock and a phase scan was performed with steps of 236 ps over 8 clock periods. The average difference is smaller than ± 1 LSB.



Figure 7. Difference of the TDC time measurements when 1 or 64 ASIC channels are active.

3.3 Channel time resolution

The timing performance of the full ASIC channel was evaluated with test pulses. In TOFPET2, analog test pulses emulating detector signals can be induced in a test capacitance at the input of the pre-amplifier, using an external digital pulse as described in Section 1. The total capacitance of the test injection circuit is 112 pF. The rise time (10-90%) of the test pulse is 8 ns, similar to the pulses from a LYSO scintillating crystal. In this measurement, the amplitude of the test pulse is equivalent to about 100 photo-electrons. **Figure 8** shows the distribution of the time resolution measured at each phase of the test pulse relative to the clock (steps of 16 ps over 1 clock period). The average of the measured values is 23 ps (r.m.s.).



Figure 8. Full channel time resolution measured with internal test pulses.

The ASIC timing performance was also evaluated with laser pulses generated with the HPK PLP-10 Picosecond light pulser (see Section 4). The results were obtained in coincidence using different TOFPET2 ASICs in two Test Boards and a 50-50 laser beam splitter. Optical filters with absorption varying by a factor ten have been used to obtain pulses with amplitude of 100 and 1000 photo-electrons. The pulse amplitude calibration was obtained from the individual peaks in the ToT spectra of the first photoelectrons extrapolated to larger pulses. The measurements were done with two SIPM arrays: HPK S13361-3050AE-04 and KETEK PA3325-WB-0808. The resolution of the time difference of pulses with 1000 (100) p.e. is 25.9 (42.7) ps for the HPK S13361-3050AE-04 MPPC and 25.7 (37.3) ps for the KETEK PA3325-WB-0808 SiPM (Figure 9).



Figure 9. Resolution of the time difference of two channels in different ASICs illuminated with laser pulses with amplitude of 100 and 1000 photo-electrons for two different SiPM models.

3.4 Performance of the Charge Integration QDC

The QDC is composed of a charge integration analog buffer (QAC) followed by a 10-bit Wilkinson ADC. In normal operation, the QAC analog buffer is charged with a replica of the input current plus a DC current. An offset (pedestal) arises from the integration of the DC current. The nominal QDC binning is 3.6 pC per LSB and the nominal linear range is 160 QDC counts corresponding to 576 pC. This range is sufficient to measure pulses with 2500 p.e. detected with a SiPM of gain 1.25x10⁶. The QDC LSB corresponds to about 20 p.e. for the same SiPM gain. In order to use a higher SiPM gain, TOFPET2 has the option of reducing the QDC gain by a factor up to 2.5 extending the linear dynamic range up to 1440 pC. Above this charge, the preamplifier deviates from a linear behavior.

We have measured the linearity of the charge integration QDC by integrating the DC current in different time windows. In this measurement, the integrated charge extends roughly up to 1500 pC and the LSB corresponds to a pulse charge of 9.4 pC. As shown in **Figure 10**, we measure DNL below 0.8 LSB and the INL below 2.3 LSB.



Figure 10. (a) QDC differential non-linearity. (b) QDC integrated non-linearity.

The QDC noise is estimated from the distribution of measurements of the baseline DC current integrated in a fixed window of 240 ns (48 periods of the 200 MHz clock) typically used to measure pulses originated in the LYSO scintillating crystal. We obtain that the noise of the charge measurement is 0.65 LSB r.m.s. The full width half maximum (FWHM) of the electronic noise is 1.9 % of the amplitude of the 511keV photo-peak measured with the QCD nominal gain settings (see section 5).

The amplitude measured in one channel was evaluated as a function of activity in the other ASIC channels. Figure 11 shows the difference of the amplitude measurements in one channel when 1 or 64 channels are active. The integration window length was scanned between 100 ns and 400 ns. The average difference is smaller than ± 1.2 LSB.



Figure 11. Difference of the ADC amplitude measurements when 1 or 64 ASIC channels are active.

3.5 Rate performance

The TOFPET2 ASIC uses 1, 2 or 4 (configurable) output links each operating up to 800 Mbit/s. The output data is formatted in 64 bits event packages with 8B/10B encoding. The total

event output rate was measured as a function of the channel input rate using test pulses active in all 64 ASIC input channels showing that the TOFPET2 can sustain a total event rate of 38 Mcounts/s (**Figure 12**). We have measured the dependence of the time resolution on the channel input rate using laser pulses. In **Figure 13** we show that the time resolution is stable up to 600 kHz pulse rate.



Figure 12. Total output event rate as a function of the rate per channel with all channels active.



Figure 13. Time resolution of multi-photon laser pulses as a function of the channel input rate.

4. SPTR measurements with laser

Measurements of the Single Photon Time Resolution (SPTR) with TOFPET2 were performed using laser pulses generated by the HPK PLP-10 Picosecond Light Pulser. The pulses were triggered at a frequency of 156 kHz synchronously to the system clock. The light pulses were attenuated with optical filters to get on average one photo-electron per pulse. The data was acquired using the same threshold in the three TOFPET2 discriminators. The calibration of the threshold in number of photo-electrons was extracted from the threshold scan with dark counts (**Figure 4**). To reduce the dark count noise, the events were required to have a time stamp in a window of 100 ns around the expected time of the laser pulse. The amplitude of the events is extracted from the time-over-threshold (ToT) measurement. Events with amplitude compatible with one photo-electron were selected.



Figure 15. Single-Photon Time Resolution (SPTR) as a function of overvoltage obtained with the HPK-S14160-3050HS MPPC.

The SPTR obtained with the HPK S13361-3050AE-04 MPPC using the method described above was reported in [3]. For overvoltage 7.5 (4) V the result was 90 (130) ps r.m.s. With the same HPK S13361-3050AE-04 MPPC, we have measured the slew rate of the rising edge of the single photon pulse by scanning the time of arrival of the laser pulse as a function of the discriminator threshold. We obtain 32 mV/ns at overvoltage 7.5 V. Taking into account that the measured electronics noise is 1.6 mV (Section 3.1) we estimate that the contribution to the SPTR of the ASIC electronics noise is of the order of 50 ps r.m.s. for overvoltage 7.5 V.

In this work, we have measured the SPTR with the new HPK-S14160-3050HS MPPC. **Figure 14** shows the distribution of the Time of Arrival (ToA) of the laser pulses measured with the TOFPET2 ASIC when the SiPM is operated at 6.5 V overvoltage. We note that the distribution is not Gaussian presenting a tail on the right side. The origin of this tail is under investigation. Here we have fitted the data with a Gaussian distribution as illustrated in the figure. The resulting SPTR reflects the width of the core of the distribution. Using this method, **Figure 15** shows the SPTR measured as a function of the overvoltage. SPTR of 83 (126) ps r.m.s. was obtained at an overvoltage of 6.5 (4) V.

5. Energy and timing measurements with LYSO crystals

We have previously reported the measurement of the energy spectrum of ²²Na gamma rays obtained with a LYSO crystal of 3x3x5 mm³ mounted on a KETEK-PM3325-WB SiPM operated at 4 V overvoltage and readout with TOFPET2 [3]. The energy resolution of the 511 keV photo-peak was 10.5% (FWHM). In this work, we report the measurements done with the SiPM array Broadcom QFBR-S4N44P164S 4x4. **Figure 16** shows the pulse height spectrum obtained with a LYSO crystal of the same dimensions and with this SiPM operated at 3.8V overvoltage. The charge signal is integrated in a time window of 350 ns. The energy resolution at 511keV is 12.0% (FWHM). The energy spectrum is corrected for the non-linearity of the SiPM by recording pulse height spectra with ¹³³Ba (81, 356 keV), ²²Na (511, 1275 keV) and ¹³⁷Cs (662 keV) sources, and fitting the relation between ADC counts and gamma energy for the different gamma emissions lines.

The coincidence time resolution (CTR) of back-to-back 511 keV gamma rays from a ²²Na source was measured with LSO:Ce crystals co-doped with 0.2% Ca. Short crystals of 2x2x3 mm³ and long crystals of 3x3x20 mm³ typical of PET applications have been used. The crystals were glued to SiPMs of different producers (FBK/Broadcom, HPK, SensL and KETEK). The references of the SiPMs used and the results of the CTR measurements are summarized in **Table I**, together with the values of the SiPM bias voltage that optimize the time resolution. **Figure 17** shows the distribution of the coincidence time difference obtained with the HPK S14160-3050HS MPPC, for two dimensions of the crystals, namely 3x3x20 mm³ and 2x2x3 mm³. The measured CTR values are 183 ps and 119 ps (FWHM), respectively.



Figure 16. Pulse height spectrum obtained with a ²²Na radioactive source and with a LYSO crystal of 3x3x5 mm³ mounted on a Broadcom QFBR-S4N44P164S SiPM. The energy spectrum is corrected for the non-linearity of the SiPM.

SiPM	Bias voltage	Crystal dimensions (mm)	CTR with TOFPET2 (ps)
FBK-NUVHD 40um (4x4mm)	35.0	2x2x3	118
HPK S14160-3050HS	42.0	2x2x3	119
SENSL FJ-SMTPA -30035-E46 (3x3mm)	29.5	2x2x3	143
KETEK PM3325- WB (3x3mm)	32.5	2x2x3	144
FBK-NUVHD 40um (4x4mm)	35.0	3x3x20	183
HPK S14160-3050HS	42.0	3x3x20	183
SENSL FJ-SMTPA -30035-E46 (3x3mm)	29.5	3x3x20	228
KETEK PM3325- WB (3x3mm)	32.5	3x3x20	223

Table I. CTR measured with TOFPET2 associated to four different SiPMs and LSO:Ce crystals co-doped with 0.2% Ca with two different dimensions.

SENSL FJ-S0035-E46



Figure 17. CTR measured with LSO:Ce crystals co-doped with 0.2% Ca of 3x3x20 mm³ (left) and 2x2x3 mm³ (right) coupled to HPK S14160-3050HS MPPC.

6. Conclusions

A complete set of measurements with TOFPET2, a 64-channel ASIC for SiPM readout and digitization in TOF applications, were presented. In summary, the main TOFPET2 performance results are the following:

- Amplifier noise $\sigma \sim 0.1$ p.e. rms
- TDC DNL<0.2 LSB; INL<1 LSB
- Time resolution (test pulse): 23 ps r.m.s
- SPTR: 83 ps r.m.s (w/ HPK-S14160-3050HS MPPC @ 6.5 V overvoltage)
- CTR: 118 ps FWHM (w/ LSO:Ce 2x2x3 mm3; SiPM FBK-NUVHD 40um)
- ADC DNL <0.8 LSB; INL<2.3 LSB
- Charge integration noise: 1.9% FWHM of charge corresponding to 511 keV.
- Energy resolution at 511 keV: 10.5% FWHM (w/ LYSO; SiPM KETEK PM3325)

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