# *Inforce 68A1™*

## *Hardware Reference Manual*

***003835 Rev A***

***November 19, 2021***

**Submit technical questions at:**
**http://www.smartwirelesscomputing.com/techweb/**



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# Revision History

| Revision | Date | Description | Author |
|---|---|---|---|
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# Approval Record

| Function | Name | Date |
|---|---|---|
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# Preface

This Hardware Reference Manual explains hardware and mechanical specifications of the Inforce 68A1 board.

## Intended Audience

This Hardware Reference Manual is intended for technically qualified personnel. It is not intended for general audiences.

## Document Organization

The chapters in this document are arranged as follows:

1. Scope
2. Hardware Specifications
3. Mechanical Specifications
4. Appendix A
5. Contact Information

## Conventions

The following conventions are used in this document:

**CAUTION**

Cautions warn the user about how to prevent damage to hardware or loss of data.

**NOTE**

Notes call attention to important information.

## Note

- This document is subject to change without notice.
- Carrier parts are shown in some of the sections for better understanding.

## Support Information

Every effort has been made to ensure the accuracy of the Hardware Reference Manual. If you have any comments, questions, or ideas regarding this document, contact SMART Wireless's technical support at: **TechSupport-wc@smartwirelesscompute.com**

# Terminology

The table below gives descriptions to some common terms used in the Hardware Reference Manual.

| Term | Description |
|---|---|
| BLE | Bluetooth Low Energy |
| bps | Bits Per Second |
| CSI | Camera Serial Interface |
| DDR | Double Data Rate |
| DS | Default Speed |
| DSI | Display Serial Interface |
| DSP | Digital Signal Processing |
| GPIO | General-Purpose Input/Output |
| GPU | Graphical Processing Unit |
| HPH | Head Phone |
| HS | High Speed |
| HVX | Hexagon Vector Extensions |
| I2C | Inter-Integrated Circuit |
| JTAG | Joint Test Action Group |
| LDO | Low Drop Out |
| LED | Light-Emitting Diode |
| LPDDR | Low-power DDR |
| MIC | Microphone |
| MIPI | Mobile Industry Processor Interface |
| OTG | On The Go |
| PCIe | Peripheral Component Interconnect Express |
| PMIC | Power Management IC |
| PoP | Package On Package |
| PU | Pull Up |
| RF | Radio Frequency |
| SDC | Secure digital controller |
| SDIO | Secured Data Input/output |
| SDR | Single Data Rate |
| SLIM bus | Serial Low-power Inter-chip Media Bus |
| SOC | System On Chip |
| SOM | System on Module |
| SPI | Serial Peripheral Interface |
| SPMI | System power management interface |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |
| WLAN | Wireless local area network |

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# 1. SCOPE

This document describes the electrical, mechanical, and functional specifications of Qualcomm QCS8250-based Inforce 68A1 SOM.

## Overview

The table below presents a brief overview of Inforce 68A1 board.

**Table 1: Inforce 68A1 Board Overview**

| | | |
|---|---|---|
| ***Processor*** | | |
| Processor | Qualcomm® QCS8250 Processor (PoP package) | |
| ***Memory Devices*** | | |
| Main Memory and Storage | 8GB LPDDR5, 5500 MB/s<br>64GB UFS 2.1 | |
| ***SOM Interfaces*** | | |
| Interfaces | 1× USB v3.1 Gen 2 (Host)<br>1× USB v3.1 Gen 2Type C (Device mode, Host mode, DP, Debug)<br>2x 4 lane MIPI-DSI<br>1×UART(Debug)<br>5× 4 Lane MIPI-CSI+ 1× 2 Lane MIPI-CSI<br>3x Camera Control I2C,<br>1x PCIe Gen 3<br>2× MHF4-WiFi/BT, | 1× 4 bit SDC for SDcard<br>1× Line Out<br>1x Ear out<br>3× Mic In<br>1× Headphone Out,<br>1x LPI_MI2S2 / Soundwire and DMIC<br>2X DMIC / 1x LPI_MI2S1<br>1x MI2S2<br>1x MI2S0/GPIO<br>1x Sensor Core I2C<br>2x Regulator Out |
| ***Form Factor*** | | |
| Mechanical | 50mm×35mm<br>Tolerance +/- 0.2mm | |
| ***Power*** | | |
| Power Input | VBAT (+3.2 to +4.5V) | |
| ***Others*** | | |
| Temperature Specification | Commercial Grade | |

**NOTE**

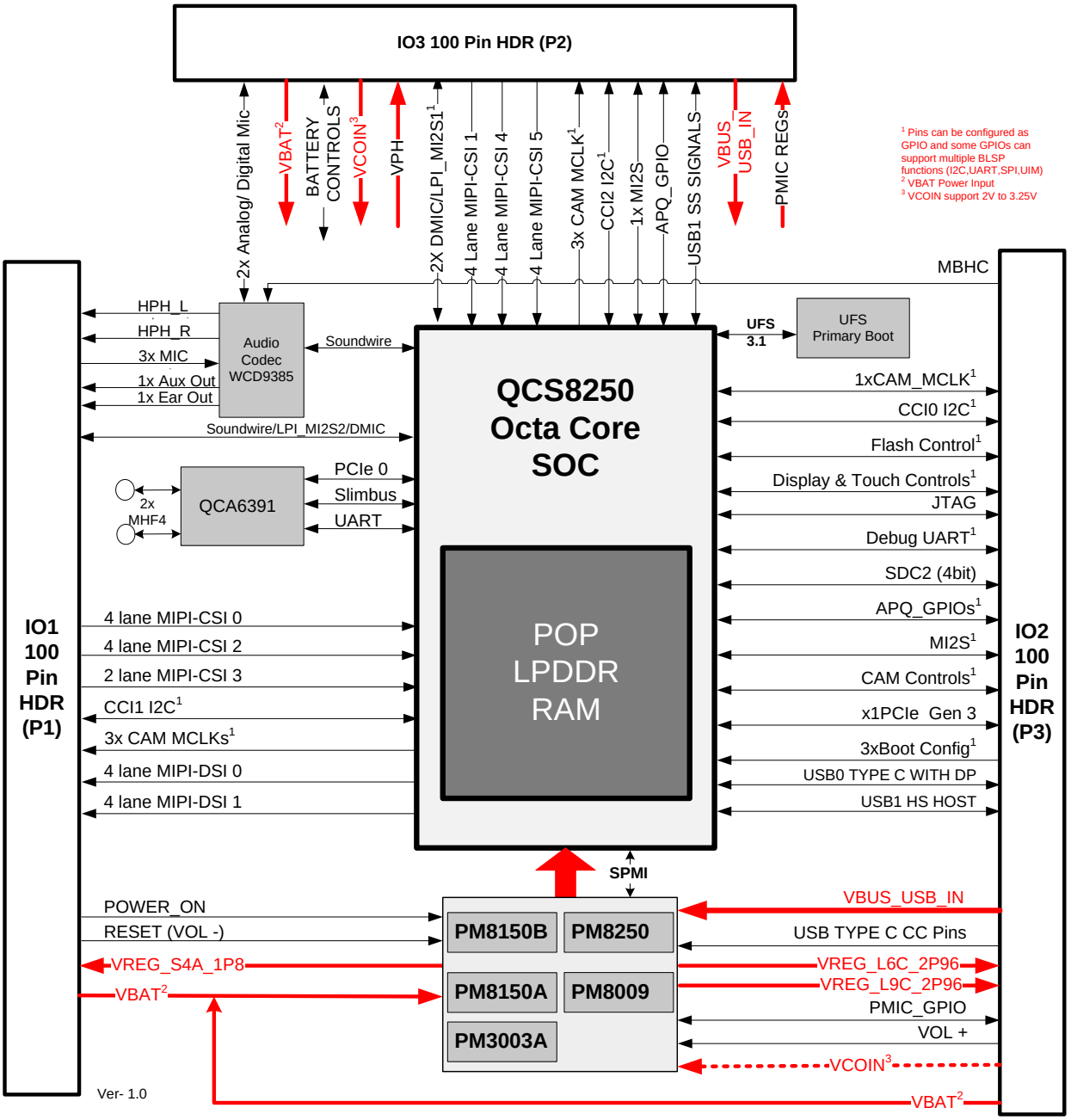
1. *MI2S0 muxed with QUP and selected GPIO_2 to high.*

# 2. HARDWARE SPECIFICATIONS

## 2.1 ARCHITECTURE

The functional diagram of the Inforce 68A1 SOM is shown below.

**Figure 1: Block Diagram**



## 2.1.1 SYSTEM OVERVIEW

The Inforce 68A1 SOM is based on the Qualcomm Octa-core QCS8250.

**Figure 2: Inforce 68A1 Board (Top Side)**

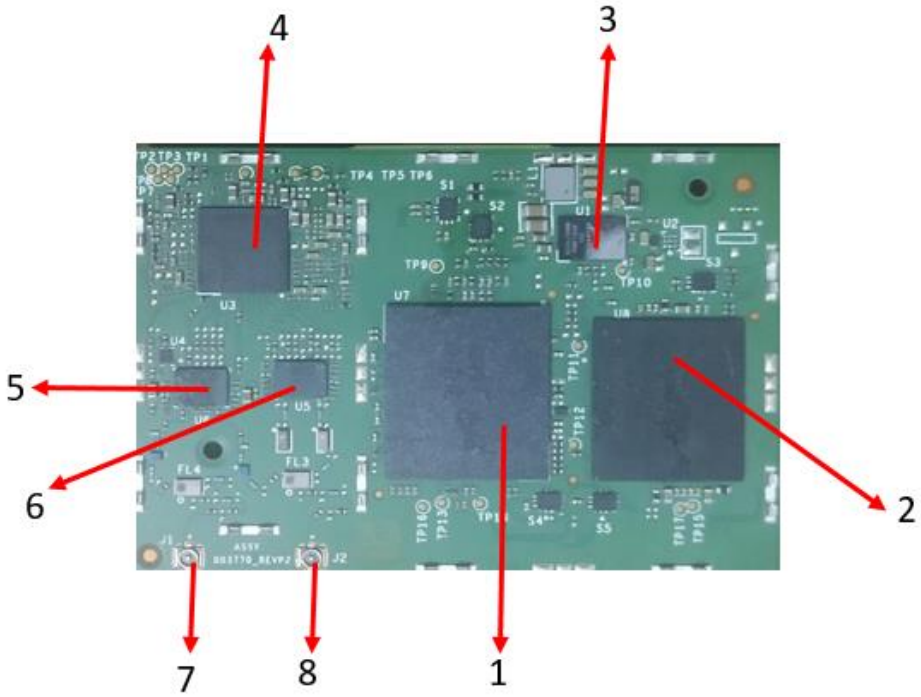
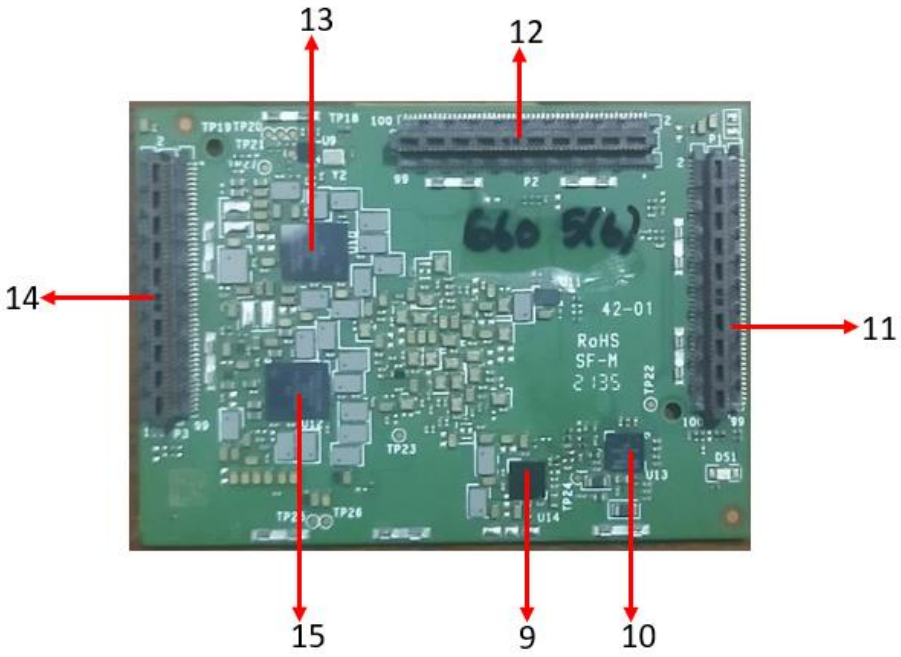



**Table 2: Inforce 68A1 Board Locations**

| No. | Description |
|---|---|
| 1 | QCS8250 + POP LPDDR5 |
| 2 | UFS |
| 3 | PMIC PM8150B |
| 4 | WIFI QCA6391 |
| 5 | FEM/2.4GHZ |
| 6 | FEM/5GHZ |
| 7 | Wi-Fi /BT Chain 1 MHF4 connector |
| 8 | Wi-Fi /BT Chain 0 MHF4 connector |
| 9 | PIMIC PM-8009 |
| 10 | Audio Codec WCD9385 |
| 11 | SOM Connector P1 (IO interface 1) |
| 12 | SOM Connector P2 (IO interface 3) |
| 13 | PIMIC PM8150A |
| 14 | SOM Connector P3 (IO interface 2) |
| 15 | PMIC PM8250 |

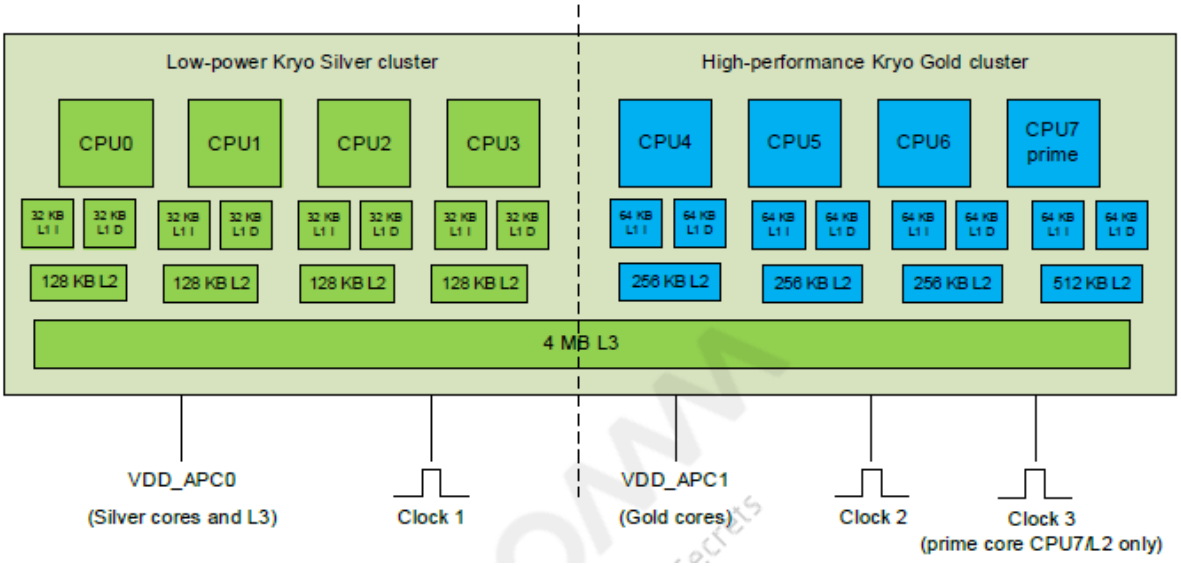
**Figure 3: Inforce 68A1 Board (Bottom Side)**




## 2.1.2 QCS8250 FEATURES

- Customized 64-bit Arm v8.2-compliant octa-core Kryo applications processor
- Qualcomm ® Adreno™ 650 graphics processing unit (GPU)
- Audio Qualcomm ® Hexagon™ DSP for LPASS
- Qualcomm® Hexagon™ DSP with quad Hexagon Vector eXtensions (HVX) processor for vision processing and machine learning
- Qualcomm Spectra™ 480 image processing engine for the ultimate photography and videography experiences
- Adreno 665 VPU for high-quality, ultra HD video encode and decode
- Adreno 995 DPU for on-device and external ultra HD display support
- Low-power audio subsystem combined with the Qualcomm Aqstic™ Audio Technologies WCD9385 audio codec for low power voice processing and audiophile quality audio playback
- Eight Kryo cores organized into two clusters:
    - Four high-performance Kryo cores – Gold cluster
        - Three Gold cores targeting 2.5 GHz
        - One Gold prime core targeting 2.8 GHz
    - Four low-power Kryo cores targeting 1.7 GHz for quad core – Silver cluster
- Dedicated L2 cache per Kryo Gold core and per Kryo Silver core

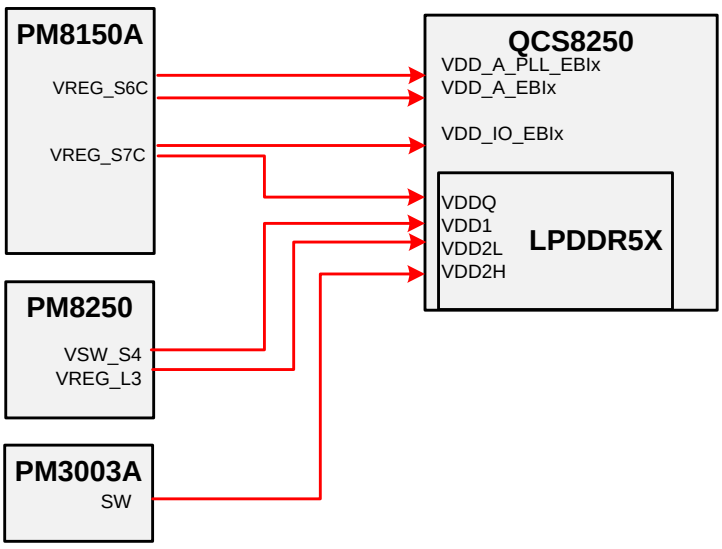
**Figure 4: Kryo Cores**




## 2.1.3 LPDDR5 INTERFACE

- Single x16 channel/die
- 1 Gig x 64 (4 channels x16 I/O)
- Supports clock up to 2.75GHz
- Memory mounted on top of QCS8250 (PoP package)
- LPDDRX power via QCS8250 from PMIC

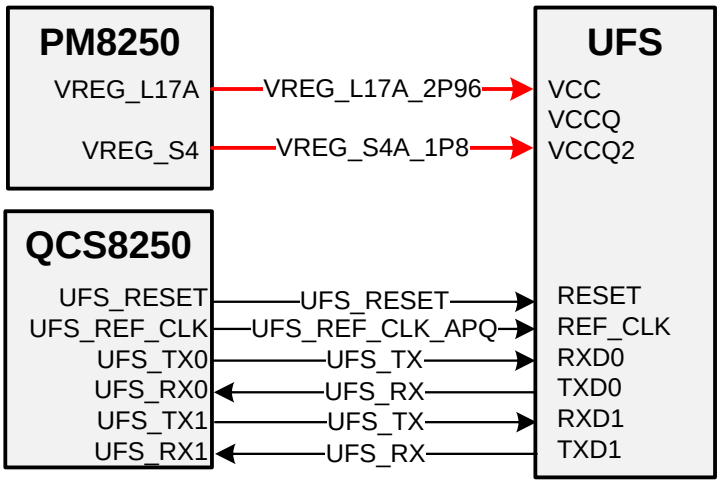
**Figure 5: LPDDR5 Power**



### 2.1.4 UFS INTERFACE

- UFS v2.1
- Gear 3 Two lane
- M-PHY v3.1

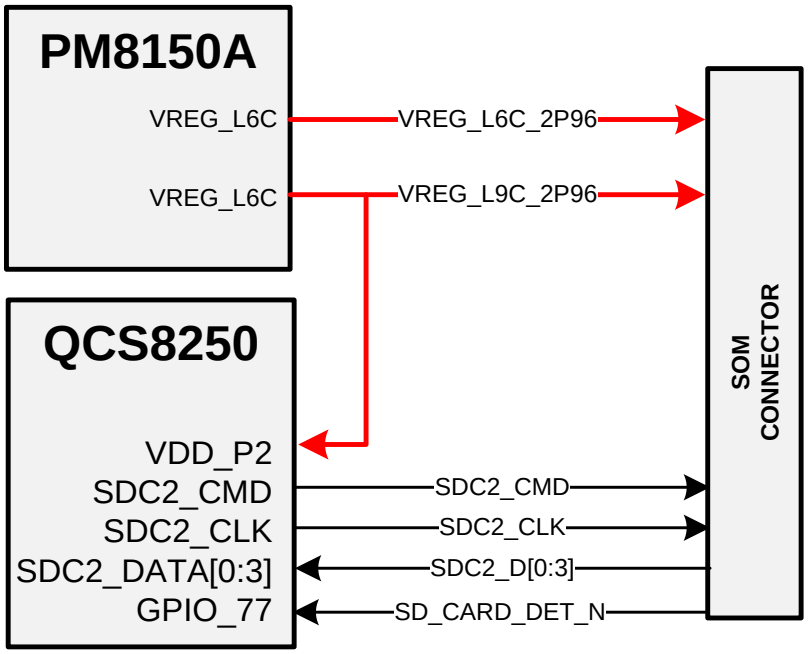
**Figure 6: UFS**



## 2.1.5 MICROSD CARD INTERFACE

- Supports SDIO (Ver. 3.0) interface for supporting standard micro SD cards.
- SDC2 Interface
- 4-bit Data Bus
- 208MHz Maximum Clock
- VREG_L6C_2P96 IO reference Dual voltage 1.8V or 2.95V interface
- VREG_L9C_2P96 SDcard power, Maximum current 800mA
- Supported modes:
    - 2.95 V – DS, HS
    - 1.8 V – SDR12, SDR25, SDR50, SDR104, DDR50

**Figure 7: SD Card Interface**



## 2.1.6 AUDIO INTERFACES

- Soundwire/LPI_MI2S2/DMIC
- 2X DMIC/LPI_MI2S1
- 1x MI2S2
- 1x MI2S0/GPIO

### WCD9385 CODEC

- **1× Line Out**
  - 1x Differential Mode optional for Aux-out 1
- **1x Ear Out**
  - 1x Differential
  - 32ohm Drive
- **1× Headphone Out**
  - High performance stereo single-ended Class-H headphone driver to drive 16 or 32 Ω loads
  - 1 Vrms ground referenced output capless output
  - Supports 32 bits data and up to 384 kHz sampling rate
- **3× Analog Mic In**
  - Single-ended Audio in
  - Capless input
  - MIC biased
- **2x Analog/ Digital_Mic In**
  - 48 kHz, DMIC CLK frequency = 2.4 MHz,

- **Soundwire communication to Processor**

**Figure 8: WCD9385 Implementation**

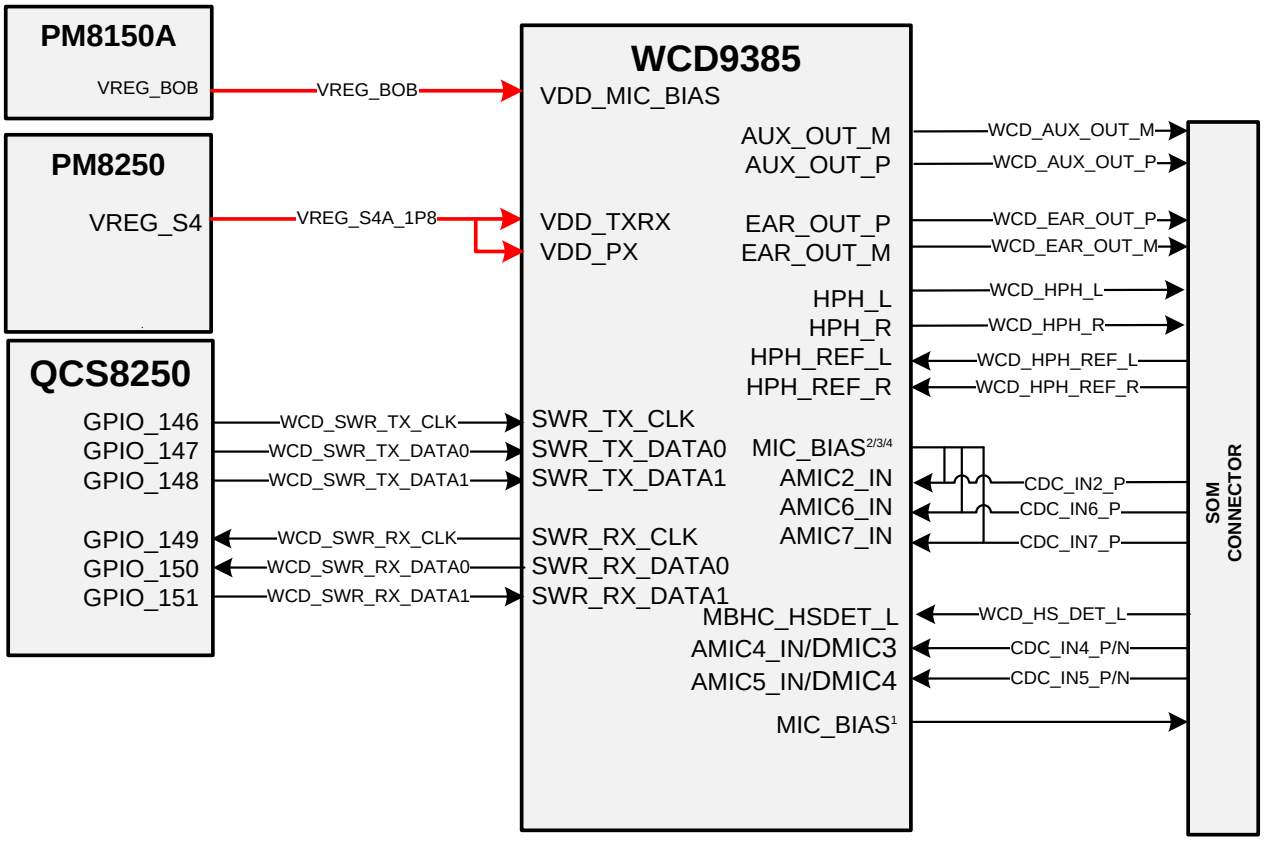
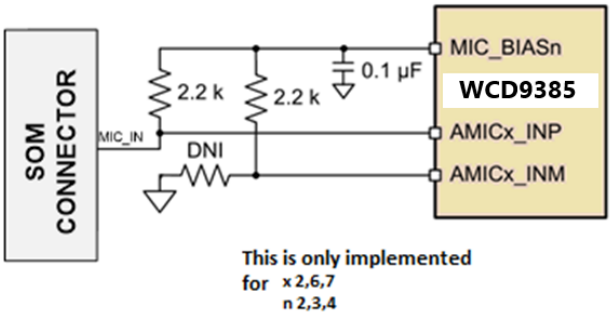



**Figure 9: MIC Input**

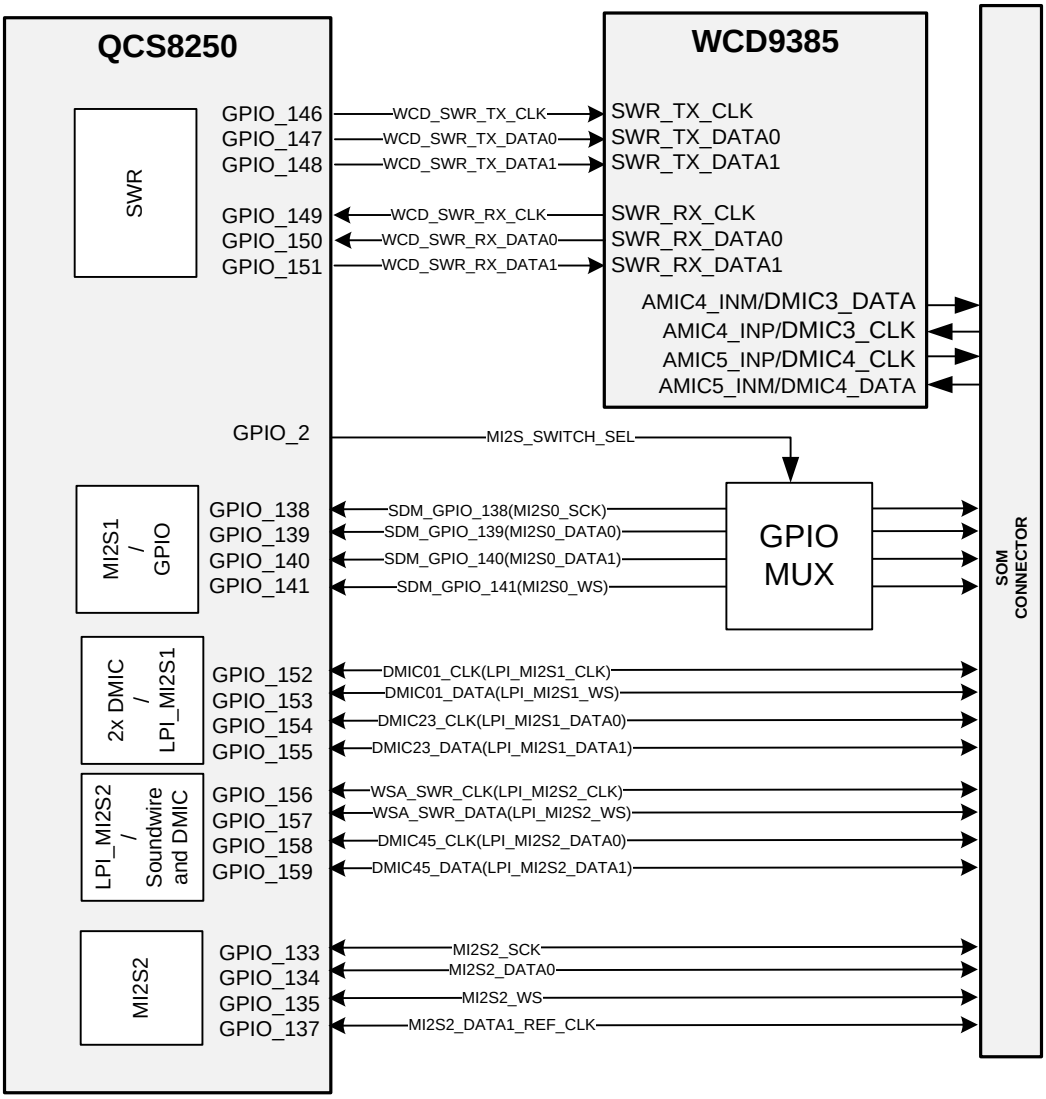


## DIGITAL AUDIO INTERFACES

QCS8250 supports various digital audio interfaces

- LPI_MI2S2 / Soundwire and DMIC
- 2X DMIC/LPI_MI2S1
- 1x MI2S2
- MI2S0/GPIO

**Figure 10: Digital Audio Interfaces**



### MI2S

- MI2S0 muxed with QUP and selected GPIO_2 to high

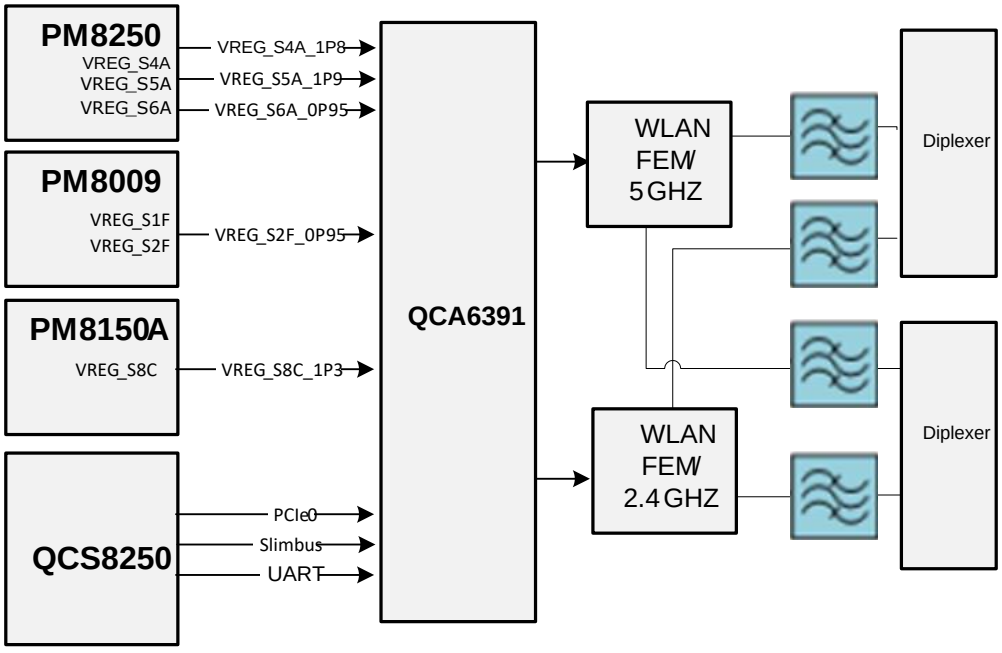
**Table 3: MI2S MUX**

| Pin | GPIO_2 = 0 (QUP) | GPIO_2 = 1 (MI2S) |
|---|---|---|
| SDM_GPIO_54_OR_138 | GPIO_54 | GPIO_138 MI2S0_SCK |
| SDM_GPIO_55_OR_141 | GPIO_55 | GPIO_141 MI2S0_WS |
| SDM_GPIO_52_OR_139 | GPIO_52 | GPIO_139 MI2S0_DATA0 |
| SDM_GPIO_53_OR_140 | GPIO_53 | GPIO_140 MI2S0_DATA1 |

## 2.1.7 WI-FI AND BLUETOOTH INTERFACE

- QCA6391 Dual-Band 2x2 MIMO DBS 802.11ax + Bluetooth
- WLAN: 802.11a/b/g/n/ac/ax, MU-MIMO
- Dual Band Simultaneous (DBS) with dual MAC, up to 1774.5 Mbps data rate (2x2+2x2 11ax DBS)
- Dual band 2.4G/5G chains
- Bluetooth v5.1 and ANT+, Bluetooth Milan ready
- Flexible interface Slimbus/PCM/I2S for BT audio
- 2× MHF4 Connector for external antenna

**Figure 11: Wi-Fi and Bluetooth Implementation**



## 2.1.8 DISPLAY INTERFACES

- The QCS8250 chipset can support 5040 × 216011 at 60 Hz (or 120 Hz in VR mode), up to 30 bpp.
- Two 4-lane DSI D-PHY 1.2 at 2.5 Gbps per lane
- Two 2560 × 2560 1 at 120 Hz for dual-panel VR displays, up to 30 bpp
- DisplayPort v1.4 at 8.1 Gbps/lane over Type-C with support for MST and VESA DSC v1.1 and FEC (USB3 and USB2 concurrency supported)
- Miracast – up to 4K60
- Adreno GPU 650, Fmax at 587 MHz – 4K 60 fps UI or 2X 2K 60 fps UI

### MIPI-DSI INTERFACE

- Two 4-lane; DSI D-PHY 1.2
- VESA DSC 1.1

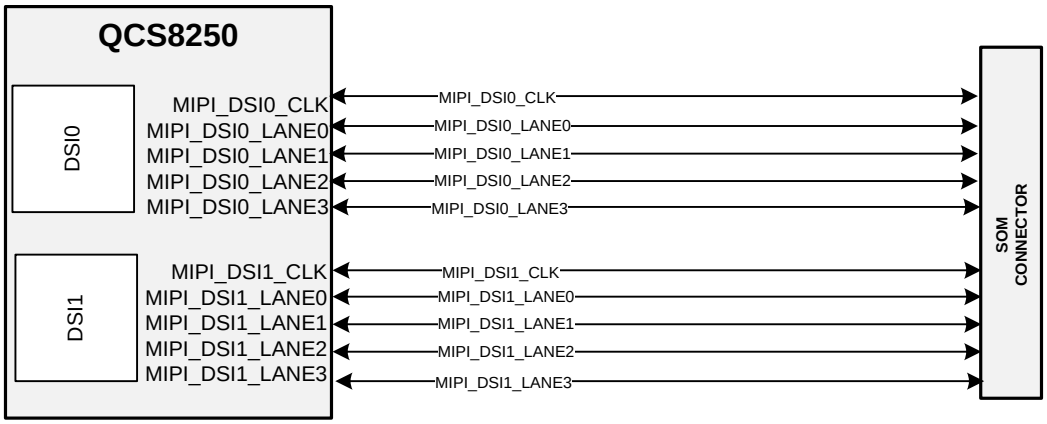
**Display Controls**

- Display Reset : GPIO_38
- Backlight Enable Output : GPIO_39
- PWM capable Output : PM8150A_GPIO_06

**Touch screen Support**

- Controls : QUP 13 I2C
- I2C Pull ups (2.2K to 1.8V) are present in the SOM
- Reset : GPIO_42
- Interrupt : GPIO_59

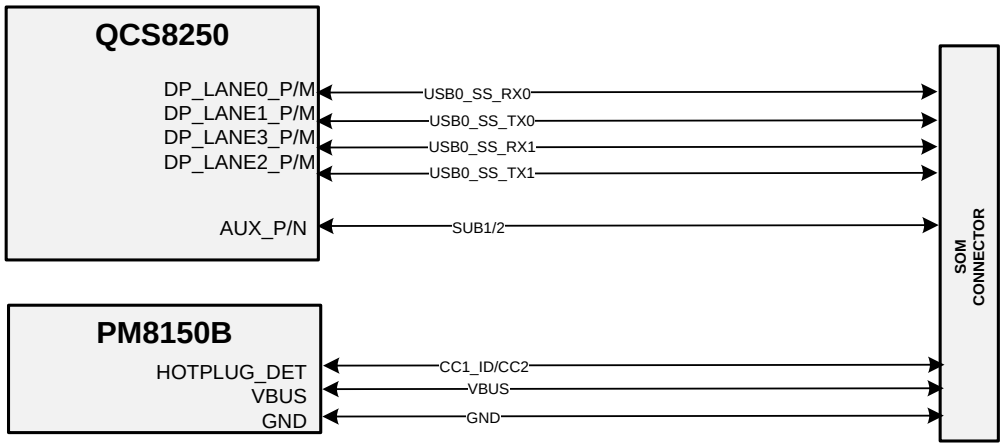
**Figure 12: MIPI-DSI Interface**



### DP INTERFACE

- DisplayPort v1.4 at 8.1 Gbps/lane over Type-C with support for MST and VESA DSC v1.1 and FEC (USB3 and USB2 concurrency supported)
- USB mode and DisplayPort mode can be simultaneously operating at USB 3 (10 Gbps) and DisplayPort (8.1 Gbps)
- In Display Port mode
  - The SM8250 can support up to 4-lane DisplayPort, 8.1 Gbps/lane
  - The USB 2.0 can be supported simultaneously.
  - USB 3.1 can be supported simultaneously.

**Figure 13: Type C Display port Interface**




## 2.1.9 CAMERA INTERFACES

- 5x 4-lane,+ 1× 2-lane camera interface
- Qualcomm Spectra 480 ISP to support up to 12 cameras by D-PHY and 18 cameras by C-PHY (seven concurrent)
- Real-time sensor input resolution: 25 + 25 + 2 + 2 + 2 + 2 + 2
- 64 MP 30 fps ZSL with a dual ISP
- Hardware 2PD support and improved face detection
- 4K120 camcorder and improved spatial noise reduction
- MIPI CSI configurable in 4 + 4 + 4 + 4 + 4 + 4 configuration
- D-PHY v1.2: 2.5 Gbps/lane on four lanes per port
- C-PHY v1.2: 10.26 Gbps/trio on three trios per port

## D-PHY, C-PHY SUPPORT

- Five 4-lane CSI D-PHY 1.2 at 2.5 Gbps per lane or Four 3-trio C-PHY 1.2 at 30.78 Gbps.
- One 2-lane CSI D-PHY
- C-PHY 1.2 is supported on the QCS8250 chipset, which uses single-ended signaling with an embedded clock (three wires per trio).

**Table 4: CPHY Pin out**

| DPHY PIN OUT | CPHY PIN OUT |
|---|---|
| MIPI_CSIx_CLK_P | Do not connect (DNC) |
| MIPI_CSIx_CLK_N | CSIx_A0_CLK_M |
| MIPI_CSIx_LANE0_P | CSIx_B0_LN0_P |
| MIPI_CSIx_LANE0_N | CSIx_C0_LN0_M |
| MIPI_CSIx_LANE1_P | CSIx_A1_LN1_P |
| MIPI_CSIx_LANE1_N | CSIx_B1_LN1_M |
| MIPI_CSIx_LANE2_P | CSIx_C1_LN2_P |
| MIPI_CSIx_LANE2_N | CSIx_A2_LN2_M |
| MIPI_CSIx_LANE3_P | CSIx_B2_LN3_P |
| MIPI_CSIx_LANE3_N | CSIx_C2_LN3_M |

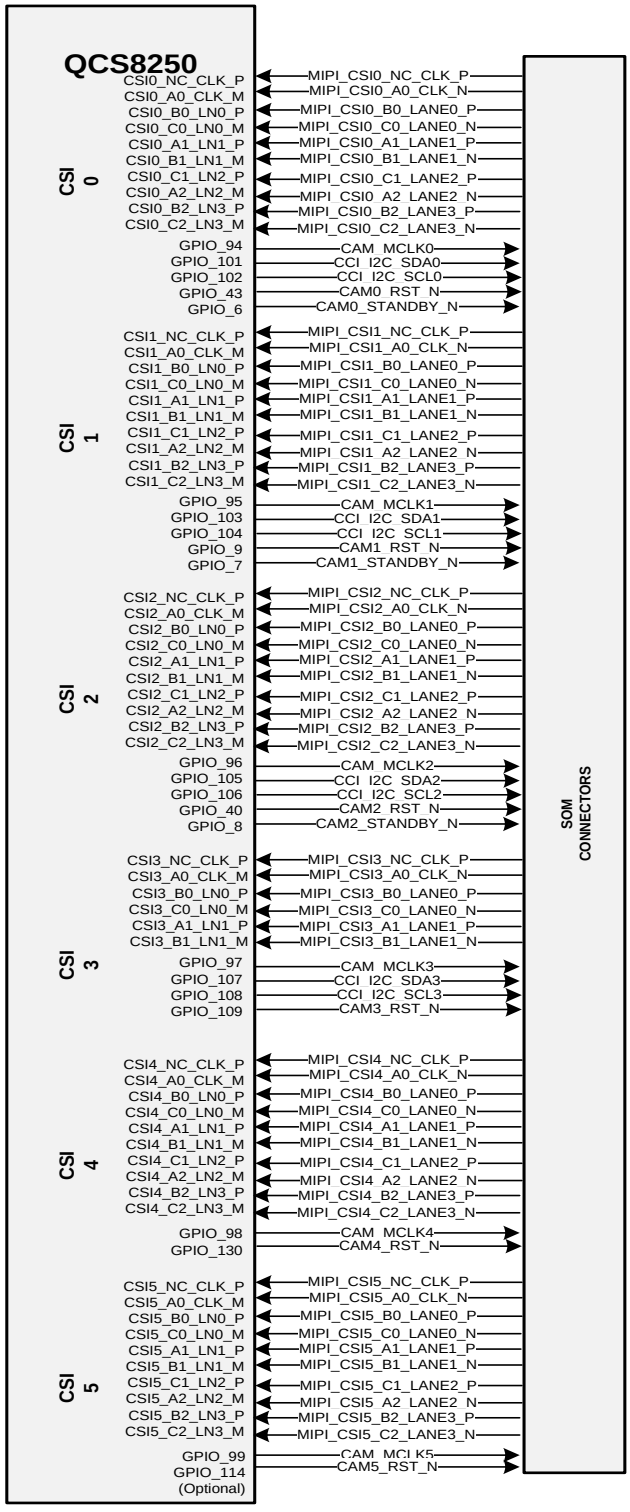
### Controls

- 2x Flash control GPIOs
- Reset & Mclock for each camera interface
- Depending on the use case cameras can either share the CCI_I2C
- Additional CAM_MLCK6 for multiple camera option

**Table 5: Camera PHY Interface**

| Camera | Lane | PHY |
|---|---|---|
| CSI0 | 4 | C/D PHY |
| CSI1 | 4 | C/D PHY |
| CSI2 | 4 | C/D PHY |
| CSI3 | 2 | D PHY Only |
| CSI4 | 4 | C/D PHY |
| CSI5 | 4 | D PHY Only |

## Figure 14: MIPI CSI Interface



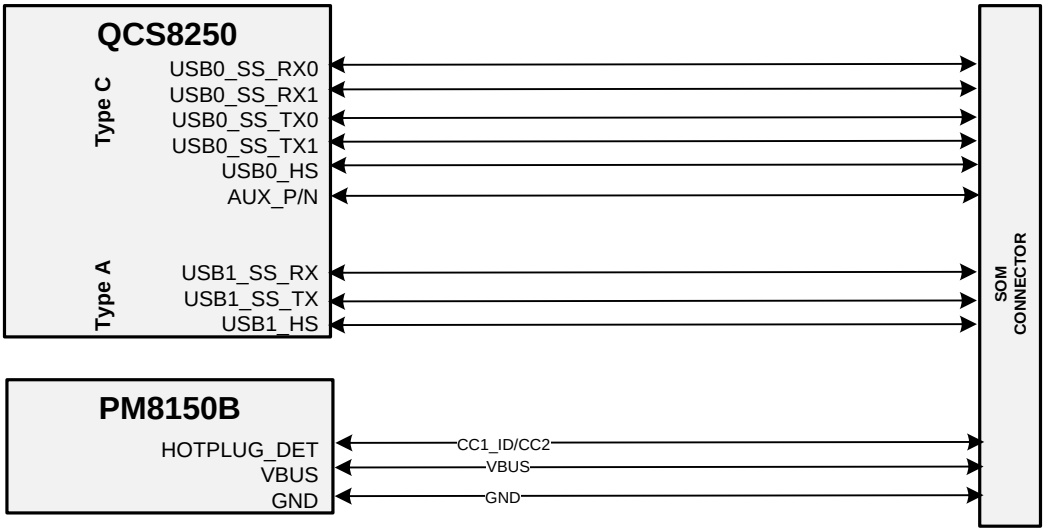
**NOTE**

- Do not use CCI I2Cs as general-purpose I2C ports
- I2C Pulls ups are present in the SOM

## 2.1.10 USB INTERFACE

- 2x USB 3.1 super-speed (USB0_SS & USB1_SS) and 2x USB 2.0 high-speed (USB1_HS & USB2_HS)
- Up to 480Mbps in USB2.0 mode
- Up to 10Gbps in USB3.1 mode
- USB Type C in default device mode and ADB is available on this port

**Figure 15: USB Interface**




**NOTE**

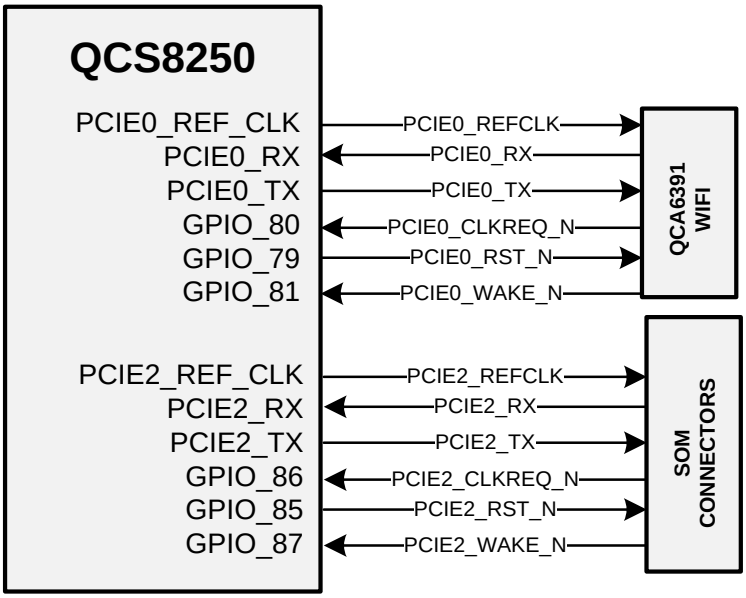
- Series capacitors are present on the TX lines

## 2.1.11 PCIE

### Specifications

- QCS8250 has three PCIe Interfaces
- PCIe0 is a Gen 3 1-lane interface
- PCIe1 is a Gen 3 2-lane interface (PCIe1 is not made available from the SoM)
- PCIe2 is a Gen 3 2-lane interface

**Figure 16: PCIE Interface**



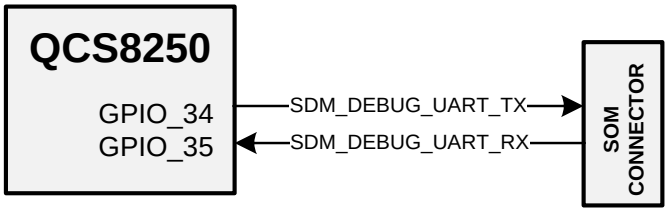

**NOTE**

Series capacitors are present on the TX lines

## 2.1.12 DEBUG UART

- Support for Debug UART interface (1.8V) via QUP12

**Figure 17: UART Interface**




## 2.1.13 RTC

- Supports 2V to 3.25V Cells
- No external resistor for current limit required
- 5 x 10uF Capacitors is placed inside the SOM for Sudden Momentary Power Loss (SMPL) not loose RTC contents.

## 2.1.14 BOOT CONTROL

### Boot Sequence Start

- Boot sequence starts when a low input trigger on keypad power on detect input (POWER_ON net P2.89 on SOM connector PHONE_ON_N pin of PM8250 & PM8150B).

**NOTE**

- Signal should stay low until JTAG_PS_HOLD(SDM_PS_HOLD) is asserted from low to high or a minimum duration of 200ms

### Boot Device Control

- Boot system from UFS, SD Card or USB.
- Boot signals are internally pulled down.
- During development or factory production, boot from the USB0 port can be forced by using GPIO_132 (FORCE_USB_BOOT).
- Logic state of Boot Configuration are latched during on processor resets out
- Each option holds a different boot sequence as described in the table below
- Each devices are tried on the order given on boot configuration option

**Table 6: Boot Configure Options**

| FASTBOOT | GPIO# | | | | Boot Sequence |
|---|---|---|---|---|---|
| | 90 | 76 | 47 | 27 | |
| 0b0000 | 0 | 0 | 0 | 0 | UFS HS G1 -> SD -> USB3.0 -> EDL(EDL path- USB only) |
| 0b0001 | 0 | 0 | 0 | 1 | SD -> UFS HS G1 -> EDL(EDL path- USB only) |
| 0b0010 | 0 | 0 | 1 | 0 | SD -> EDL(EDL path- USB only) |
| 0b0011 | 0 | 0 | 1 | 1 | USB -> EDL (EDL path - SD Then USB) |
| 0b0100 | 0 | 1 | 0 | 0 | QSPI -> EDL (EDL path - SD Then USB) |
| 0b0101 | 0 | 1 | 0 | 1 | SPI-> EDL (EDL path - SD Then USB) |

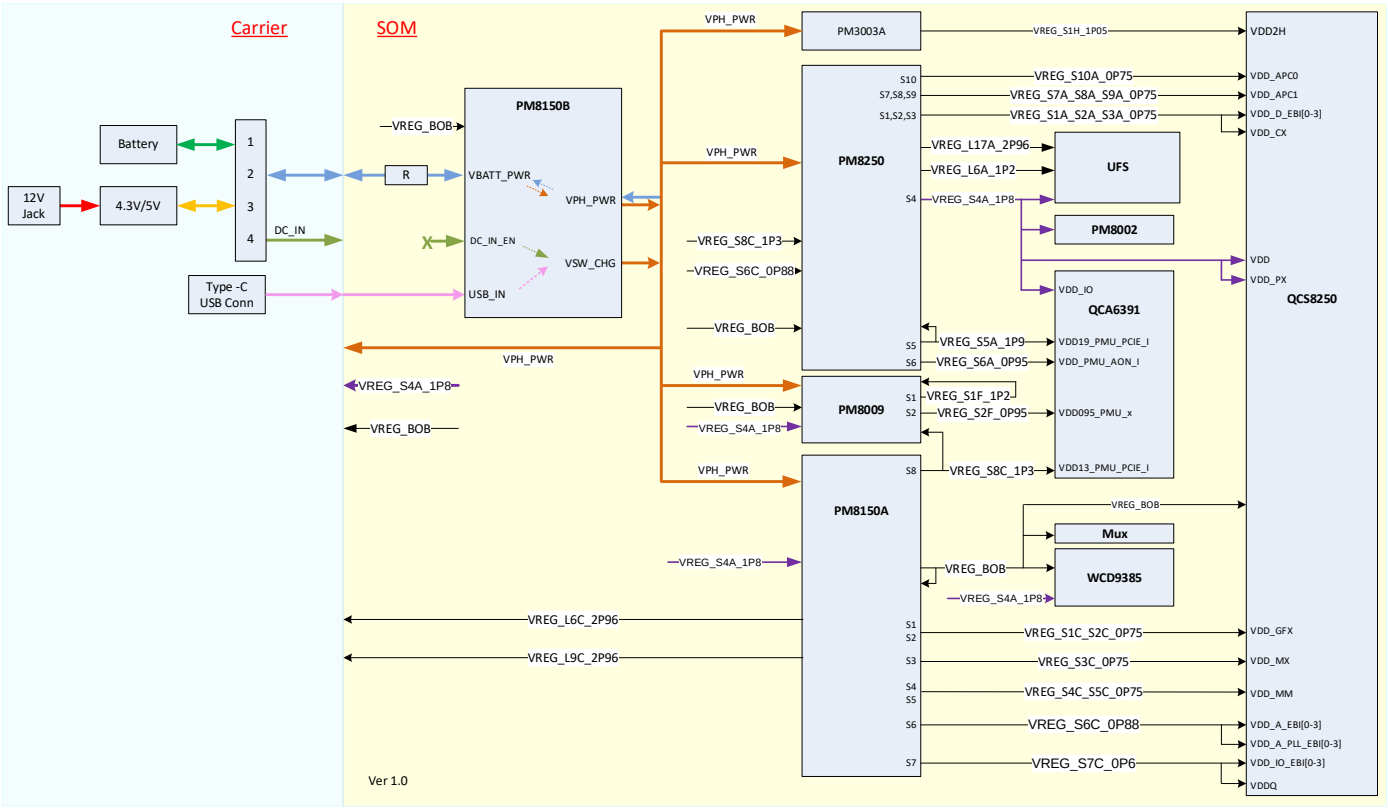
**NOTE**

- *Boot sequence will start only on a low input applied to keypad power on detect input.*
- *State of the Boot Config Pins are latched during APQ reset out*

## 2.1.15 POWER SUPPLY

- Power source from VBAT ranges from 3.2V to 4.5V (Single Cell Li-on Battery)
- Battery charging on the SOM through USB_VBUS as charger power input
- Power supply for QCS8250 power is from PMICs and to other devices (WIFI, UFS, etc).
- SOM supplies VREG_S4A_1P8 (1.8V IO power), VREG_L6C_2P96 (SDCard IO) and VREG_L9C_2P96 (SD card Power)

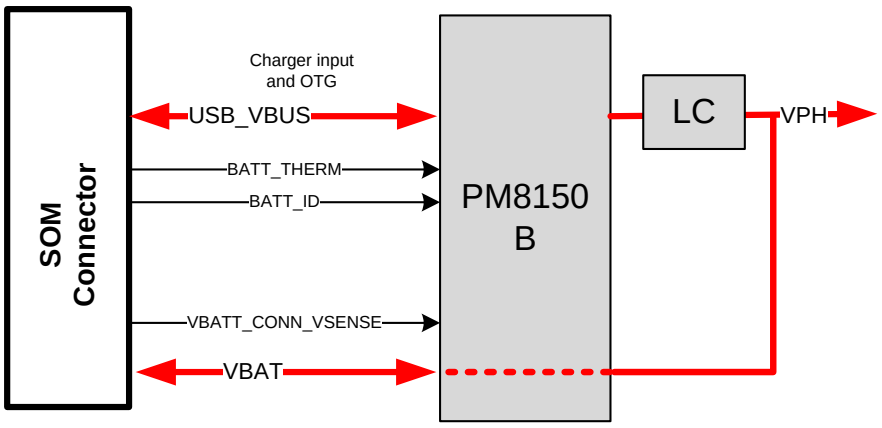
**Figure 18: Power Scheme**



## 2.1.16 CHARGER

- The SOM supports single cell lion charger
- Charge Current upto 6A
- Quick Charge 2.0, 3.0 and 4.0 hardware support
- USB Type-C and power delivery hardware support
- USB OTG and MHL/MyDP power support (1.5 A at +5-5.2 V)
- +3.6 V to +13.2 V operating input voltage range on USB_VBUS with +28 V OVP
- BATT_ID & BATT_THERM are terminated inside SOM with 7.5K and 100K respectively to work with battery-less operation

**Figure 19: Charger**




## 2.1.17 REGULATOR OUTPUTS

- Supports several regulator outputs including SD card power, IO reference power etc
- LDOs
    - VREG_L6C_2P96
    - VREG_L9C_2P96
- SMPS out
    - VREG_BOB
    - VREG_S4A_1P8
    - VPH_PWR

**Figure 20: Regulator Output**

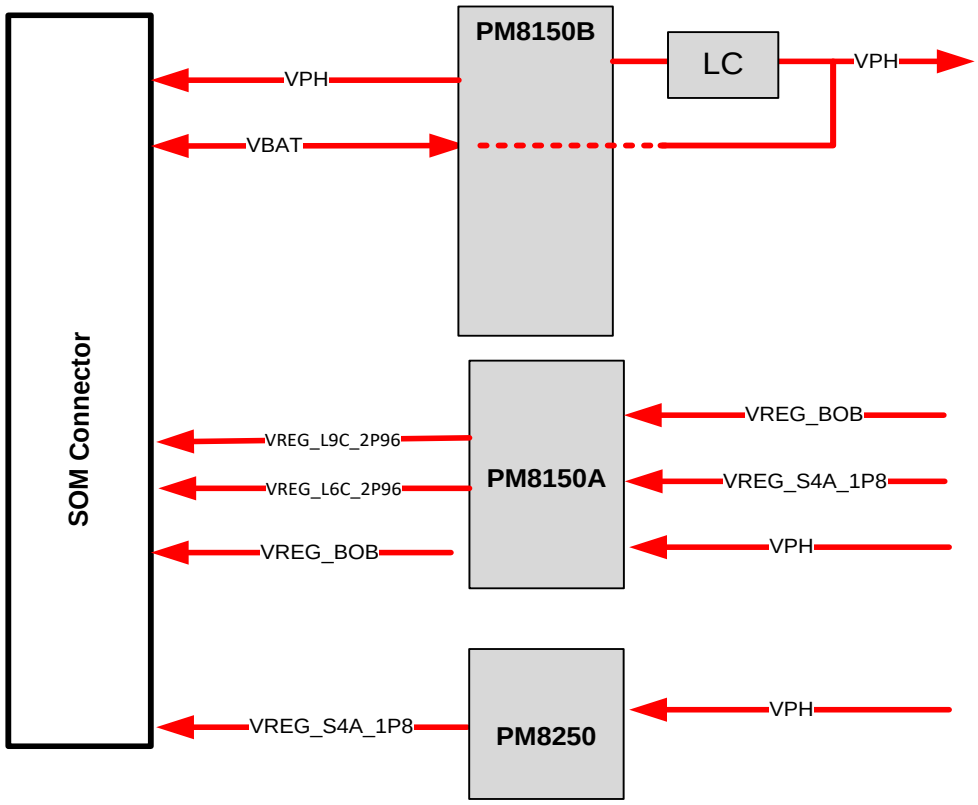


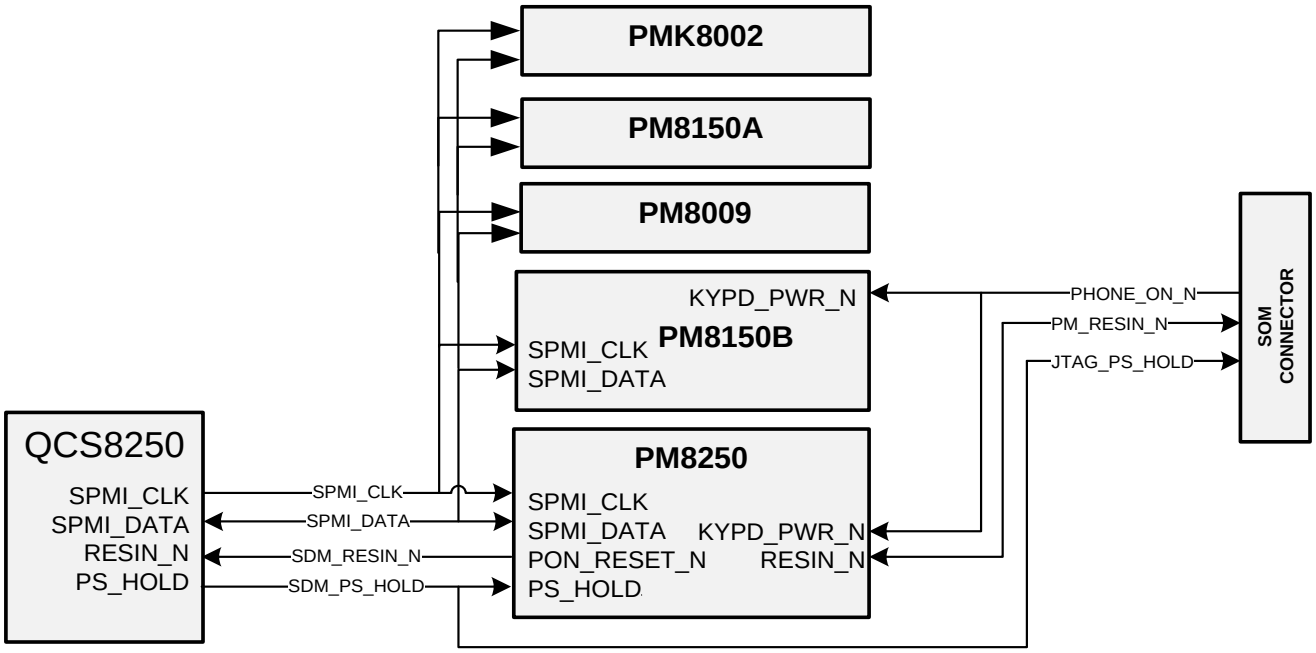

**Table 7: Regulator Specifications**

| Regulator | Regulator input | Input Voltage | Default V | I rated Max (mA) | Range | Present load inside SOM (mA) | Comments |
|---|---|---|---|---|---|---|---|
| VREG_BOB | VPH | VBAT | 3.3 | 3000 | 3.3-4 | 1700 | 3A capacity is when vph > 3.3V , if 3<VPH<3.3V only 2.5A available, Used for WIFI, SDCARD, UFS regulators |
| L6C | VREG_BOB | 3.3 | 2.96 | 150 | 1.8-2.96 | 0 | |
| L9C | VREG_BOB | 3.3 | 2.96 | 600 | 2.704-2.96 | 0 | |
| VREG_S4A_1P8 | VPH | VBAT | 1.8 | 3000 | 1.8V | 2300 | 700mA Output |

## 2.1.18 PMIC CONTROL

- PM8250, PM8150B, PM8150A, PMK8002 and PM8009 communicate to QCS8250 via SPMI interface
- PM_RESIN_N signal serves as reset input
- PHONE_ON_N serves power on trigger

**Figure 21: PMIC Control**




**NOTE**

- *Internal Pull ups are present in the PMICs for PHONE_ON_N and PM_RESIN_N*

## 2.1.19 GPIOS

- GPIOs can have multiple functions and QUP function
- QUP functions include UART, I2C and SPI
- 1 sensor core I3C
- All GPIOs are 1.8V level
- Only one protocol can be selected in one QUP engine at a time. For example, simultaneous UART and I2C functionality is no longer supported.
- Boot Configuration GPIOs must be taken care logic before processor resets out, Refer Boot Config section for Boot configurations
- Refer Appendix for GPIO list
- QUP I/Os use the following naming convention: qup_lm[n]
- m indicates the lane number, and n is the instance number

**Table 8: QUP configurations**

| QUP Lane | UART | I2C | SPI |
|---|---|---|---|
| QUP_L0 | CTS | SDA | MISO |
| QUP_L1 | RFR | SCL | MOSI |
| QUP_L2 | Tx | – | SCLK |
| QUP_L3 | Rx | – | CS_0 |
| QUP_L4 | – | – | CS_1 |
| QUP_L5 | – | – | CS_2 |
| QUP_L6 | – | – | CS_3 |

## 2.1.20 SENSOR CORE

- SOC has an integrated sensor subsystem called Snapdragon sensor core, which is dedicated to support low-power, always-on use cases
- The QCS8250 SoC's sensor core has a dedicated 1.0 MB L2/TCM cache.
- For sensor interrupts, any available MPM-capable GPIO can be routed as an interrupt to the Snapdragon sensor core subsystem.
- Sensor Core GPIOs are available on Pins SDM_GPIO_24_OR_160 & SDM_GPIO_25_OR_161 when GPIO_162 is high else QUP GPIOs will be Selected

**Table 9: Sensor Core GPIOs**

| **Sensor Core** | **Function 1** |
|---|---|
| SSC_0 | SSC_I3C_1_SDA |
| SSC_1 | SSC_I3C_1_SCL |

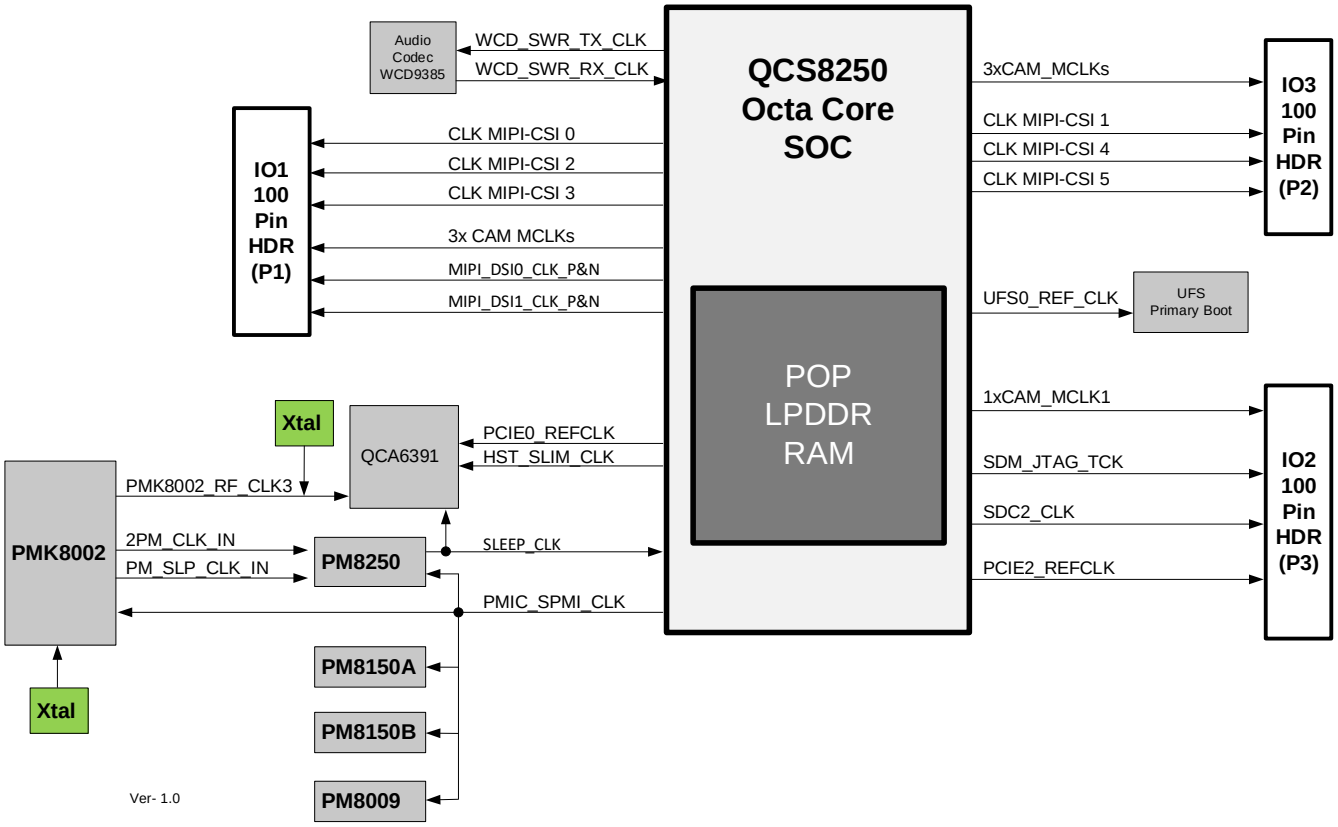
**Table 10: Sensor Core Mux**

| **Pin** | GPIO_162 **= 0** | GPIO_162 **= 1** |
|---|---|---|
| SDM_GPIO_24_OR_160 | GPIO_24 | SSC_0 |
| SDM_GPIO_25_OR_161 | GPIO_25 | SSC_1 |

## 2.1.21 CLOCK DISTRIBUTION NETWORK

- PMIC generates clock from 38.4MHz crystal and supplies clock to processor and other chips
- Processor supplies interface clocks

**Figure 22: Clock Distribution Network**

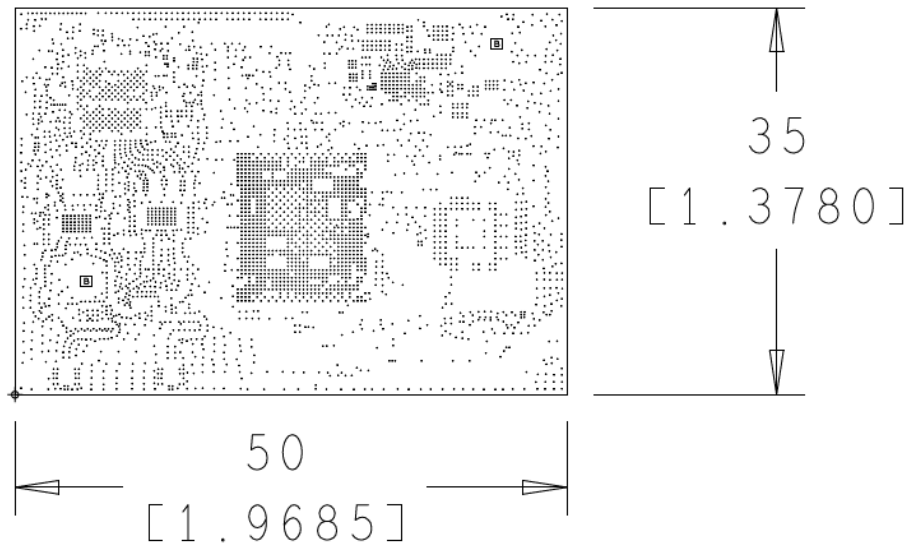


# 3. MECHANICAL SPECIFICATIONS

## 3.1 BOARD DIMENSIONS

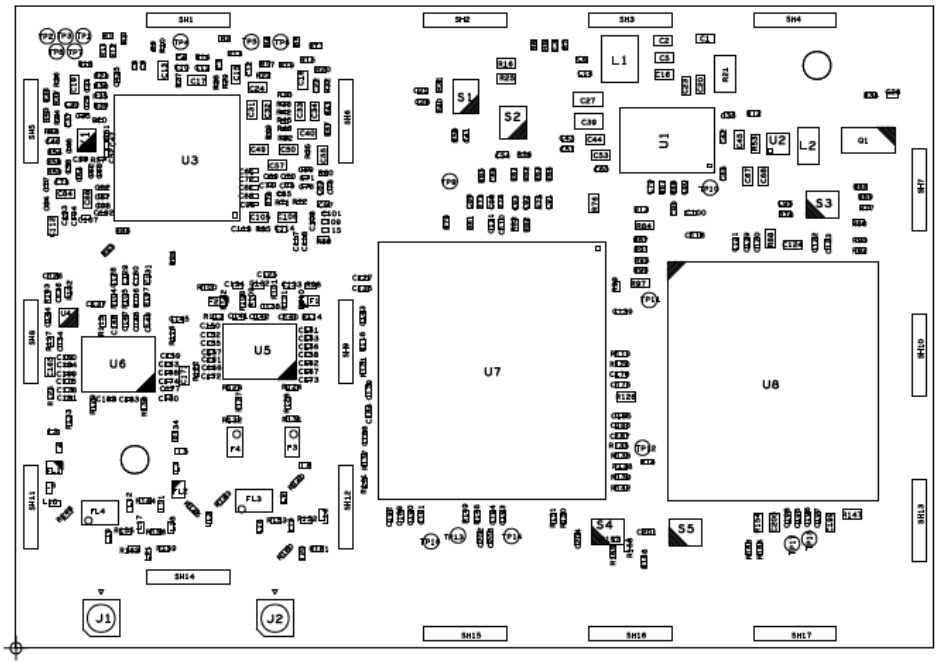
Dimensions : 50 × 35mm
Tolerance : +/-0.2mm
Layers : 14
PCB Thickness : 1mm

**Figure 23: Board Dimensions**



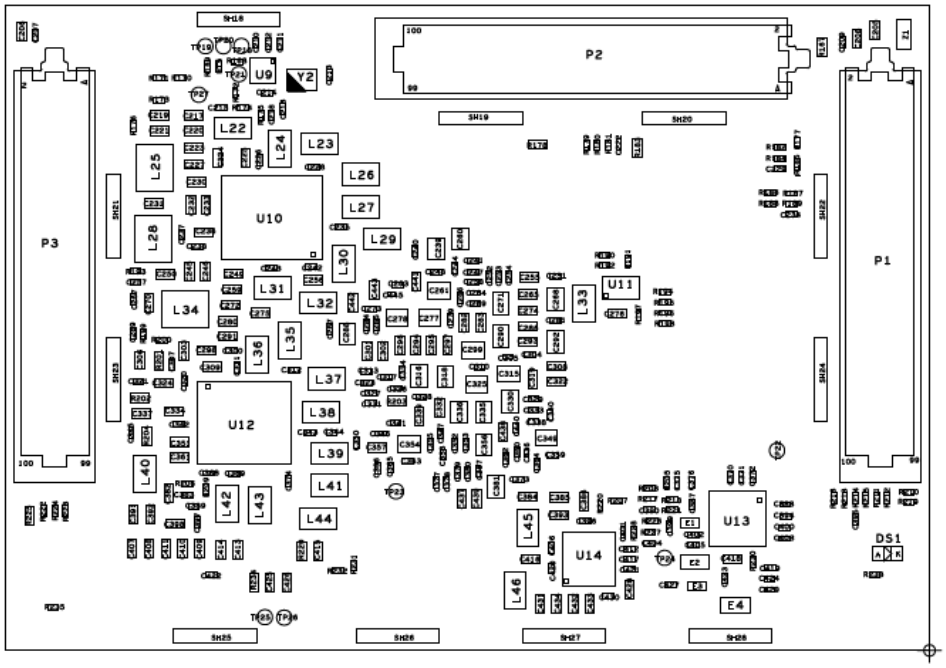
## 3.2 TOP FLOOR PLAN

**Figure 24: Top Floor Plan**




## 3.3 BOTTOM FLOOR PLAN

**Figure 25: Bottom Floor Plan**



# 4. APPENDIX A

## 4.1 SOM CONNECTORS

Manufacturer : Samtec
Manufacturer Part : ST4-50-1.50-L-D-P-TR

**Table 11: Connector IO interface 1 Pin out (Ref Des P1)**

| Pin | Net | Comments | QUP | Pin | Net | Comments | QUP |
|---|---|---|---|---|---|---|---|
| 1 | VBAT_CONN | Power input | | 2 | V3V3_CON | Power input | |
| 3 | VBAT_CONN | Power input | | 4 | VBAT_CONN | Power input | |
| 5 | WCD_EAR_OUT_P | Audio | | 6 | CAM_MCLK2 | | |
| 7 | WCD_EAR_OUT_M | Audio | | 8 | DMIC45_DATA | | |
| 9 | WCD_AUX_OUT_P | Audio | | 10 | CCI_I2C_SCL1 | | |
| 11 | WCD_AUX_OUT_M | Audio | | 12 | CAM_MCLK0 | | |
| 13 | CDC_IN6_P | Audio | | 14 | CCI_I2C_SDA1 | | |
| 15 | CDC_IN7_P | Audio | | 16 | GND | | |
| 17 | DMIC45_CLK | Audio | | 18 | MIPI_CSI0_C0_LANE0_N | Camera | |
| 19 | GND | | | 20 | MIPI_CSI0_B0_LANE0_P | Camera | |
| 21 | MIPI_CSI2_B2_LANE3_P | Camera | | 22 | GND | Camera | |
| 23 | MIPI_CSI2_C2_LANE3_N | Camera | | 24 | MIPI_CSI0_A0_CLK_N | Camera | |
| 25 | GND | Camera | | 26 | MIPI_CSI0_NC_CLK_P | Camera | |
| 27 | MIPI_CSI2_A2_LANE2_N | Camera | | 28 | GND | Camera | |
| 29 | MIPI_CSI2_C1_LANE2_P | Camera | | 30 | MIPI_CSI0_A1_LANE1_P | Camera | |
| 31 | GND | Camera | | 32 | MIPI_CSI0_B1_LANE1_N | Camera | |
| 33 | MIPI_CSI2_A1_LANE1_P | Camera | | 34 | GND | Camera | |
| 35 | MIPI_CSI2_B1_LANE1_N | Camera | | 36 | MIPI_CSI0_A2_LANE2_N | Camera | |
| 37 | GND | Camera | | 38 | MIPI_CSI0_C1_LANE2_P | Camera | |
| 39 | MIPI_CSI2_A0_CLK_N | Camera | | 40 | GND | Camera | |
| 41 | MIPI_CSI2_NC_CLK_P | Camera | | 42 | MIPI_CSI0_C2_LANE3_N | Camera | |
| 43 | GND | Camera | | 44 | MIPI_CSI0_B2_LANE3_P | Camera | |
| 45 | MIPI_CSI2_C0_LANE0_N | Camera | | 46 | GND | Camera | |
| 47 | MIPI_CSI2_B0_LANE0_P | Camera | | 48 | MIPI_CSI3_NC_CLK_P | Camera | |
| 49 | GND | | | 50 | MIPI_CSI3_A0_CLK_N | Camera | |
| 51 | MIPI_DSI1_LANE3_P | Display | | 52 | GND | Camera | |
| 53 | MIPI_DSI1_LANE3_N | Display | | 54 | MIPI_CSI3_B0_LANE0_P | Camera | |
| 55 | GND | Display | | 56 | MIPI_CSI3_C0_LANE0_N | Camera | |
| 57 | MIPI_DSI1_LANE2_P | Display | | 58 | GND | Camera | |
| 59 | MIPI_DSI1_LANE2_N | Display | | 60 | MIPI_CSI3_A1_LANE1_P | Camera | |
| 61 | GND | Display | | 62 | MIPI_CSI3_B1_LANE1_N | Camera | |
| 63 | MIPI_DSI1_LANE1_N | Display | | 64 | GND | | |
| 65 | MIPI_DSI1_LANE1_P | Display | | 66 | CAM3_RST_N | | |
| 67 | GND | Display | | 68 | CAM_MCLK3 | | |
| 69 | MIPI_DSI1_LANE0_P | Display | | 70 | GND | | |
| 71 | MIPI_DSI1_LANE0_N | Display | | 72 | MIPI_DSI0_LANE3_N | Display | |
| 73 | GND | Display | | 74 | MIPI_DSI0_LANE3_P | Display | |
| 75 | MIPI_DSI1_CLK_N | Display | | 76 | GND | Display | |
| 77 | MIPI_DSI1_CLK_P | Display | | 78 | MIPI_DSI0_LANE2_N | Display | |
| 79 | WCD_HPH_REF_R | | | 80 | MIPI_DSI0_LANE2_P | Display | |
| 81 | CDC_IN2_P | Mic In | | 82 | GND | Display | |
| 83 | WCD_HPH_R | Headphone Out | | 84 | MIPI_DSI0_LANE1_P | Display | |
| 85 | WCD_HPH_REF_L | Headphone Out | | 86 | MIPI_DSI0_LANE1_N | Display | |
| 87 | WCD_HPH_L | Headphone Out | | 88 | GND | Display | |
| 89 | PHONE_ON_N_CON | Power ON | | 90 | MIPI_DSI0_LANE0_P | Display | |
| 91 | PM_RESIN_N_CON | Vol-/ Reset | | 92 | MIPI_DSI0_LANE0_N | Display | |
| 93 | SDM_GPIO_28 | GPIO | QUP_L0(0) | 94 | GND | Display | |
| 95 | SDM_GPIO_29 | GPIO | QUP_L1(0) | 96 | MIPI_DSI0_CLK_P | Display | |
| 97 | VREG_S4A_1P8 | 1.8V Out | | 98 | MIPI_DSI0_CLK_N | Display | |
| 99 | VREG_S4A_1P8 | 1.8V Out | | 100 | GND | Display | |

## Table 12: Connector IO interface 2 Pin out (Ref Des P3)

| Pin | Net | Comments | QUP |
|---|---|---|---|
| 1 | VBAT_CONN | Power input | |
| 3 | VBAT_CONN | Power input | |
| 5 | CAM2_RST_N | | |
| 7 | CAM0_STANDBY_N | | |
| 9 | USB_CC2_R | USB | |
| 11 | FORCE_USB_BOOT_MCLK | | |
| 13 | SDM_FAST_BOOT_0 | | |
| 15 | CAM0_RST_N | | |
| 17 | FLASH_STROBE_EN | | |
| 19 | CCI_I2C_SDA0 | | |
| 21 | CCI_I2C_SCL0 | | |
| 23 | GND | | |
| 25 | USB0_SS_RX1_M | USB | |
| 27 | USB0_SS_RX1_P | USB | |
| 29 | GND | USB | |
| 31 | USB0_HS_DP | USB | |
| 33 | USB0_HS_DM | USB | |
| 35 | GND | USB | |
| 37 | USB2_HS_DP | USB | |
| 39 | USB2_HS_DM | USB | |
| 41 | GND | USB | |
| 43 | TS_I2C_SCL | Touch | |
| 45 | TS_I2C_SDA | Touch | |
| 47 | BACKLIGHT_EN | Backlight Enable Out | |
| 49 | SDM_GPIO_5 | | QUP_L1(1) |
| 51 | TS_INT_N | Touch | |
| 53 | PM8150A_GPIO_06_OR_10 | PMIC GPIO/PWM Out | |
| 55 | TS_RESET_N | Touch | |
| 57 | DISP0_RESET_N | Display Reset | |
| 59 | SDM_GPIO_4 | | QUP_L0(1) |
| 61 | SDM_DEBUG_UART_TX | Debug UART | |
| 63 | SDM_DEBUG_UART_RX | Debug UART | |
| 65 | GND | | |
| 67 | WSA_SWR_DATA | Soundwire | |
| 69 | WSA_SWR_CLK | Soundwire | |
| 71 | GND | | |
| 73 | PCIE2_REFCLK_P | pcie | |
| 75 | PCIE2_REFCLK_M | pcie | |
| 77 | GND | pcie | |
| 79 | PCIE2_TX0_P | pcie | |
| 81 | PCIE2_TX0_M | pcie | |
| 83 | GND | pcie | |
| 85 | PCIE2_RX0_P | pcie | |
| 87 | PCIE2_RX0_M | pcie | |
| 89 | GND | pcie | |
| 91 | PCIE2_CLK_REQ_N | pcie | |
| 93 | PCIE2_WAKE_N | pcie | |
| 95 | PCIE2_RST_N | pcie | |
| 97 | SDM_GPIO_30 | | QUP_L2(0) |
| 99 | SDM_GPIO_31 | | QUP_L3(0) |

| Pin | Net | Comments | QUP |
|---|---|---|---|
| 2 | VBAT_CONN | Power input | |
| 4 | VBAT_CONN | Power input | |
| 6 | FLASH_STROBE_TRIG | | |
| 8 | WDOG_DISABLE | | |
| 10 | KYPD_VOLP_N_CON | | |
| 12 | SDM_GPIO_52_OR_139 | | QUP_L0(17) |
| 14 | USB_VBUS | | |
| 16 | SDM_GPIO_55_OR_141 | | QUP_L3(17) |
| 18 | SDM_GPIO_53_OR_140 | | QUP_L1(17) |
| 20 | SDM_GPIO_54_OR_138 | | QUP_L2(17) |
| 22 | USB_CC1 | USB | |
| 24 | CAM_MCLK4 | | |
| 26 | USB_SBU1 | USB | |
| 28 | USB_SBU2 | USB | |
| 30 | GND | USB | |
| 32 | USB0_SS_TX1_M | USB | |
| 34 | USB0_SS_TX1_P | USB | |
| 36 | GND | USB | |
| 38 | USB0_SS_RX0_M | USB | |
| 40 | USB0_SS_RX0_P | USB | |
| 42 | GND | USB | |
| 44 | USB0_SS_TX0_M | USB | |
| 46 | USB0_SS_TX0_P | USB | |
| 48 | SDM_GPIO_24_OR_160 | | QUP_L0(8) |
| 50 | SDM_GPIO_25_OR_161 | | QUP_L1(8) |
| 52 | SDM_RESOUT_N | | |
| 54 | CAM4_RST_N | | |
| 56 | SDM_FAST_BOOT_1 | | |
| 58 | JTAG_PS_HOLD | | |
| 60 | SD_UFS_CARD_DET_N | Sdcard | |
| 62 | VREG_L6C_2P96 | Sdcard | |
| 64 | SDC2_DATA_2 | Sdcard | |
| 66 | SDC2_DATA_1 | Sdcard | |
| 68 | SDC2_CLK | Sdcard | |
| 70 | SDC2_DATA_3 | Sdcard | |
| 72 | SDC2_CMD | Sdcard | |
| 74 | SDC2_DATA_0 | Sdcard | |
| 76 | VREG_L9C_2P96 | Sdcard | |
| 78 | SDM_JTAG_TRST_N | jtag | |
| 80 | SDM_JTAG_SRST_N | jtag | |
| 82 | SDM_JTAG_TDO | jtag | |
| 84 | SDM_JTAG_TDI | jtag | |
| 86 | SDM_JTAG_TCK | jtag | |
| 88 | SDM_JTAG_TMS | jtag | |
| 90 | WCD_HS_DET_L | Headset Detect | |
| 92 | SDM_GPIO_41 | | QUP_L1(14) |
| 94 | CAM2_STANDBY_N | | |
| 96 | SOM_OPTION | Options (Auto Boot/ Charger Disable) | |
| 98 | VCOIN_R | Options | |
| 100 | USB_VBUS_R | Options | |

## Table 13: Connector IO interface 3 Pin out (Ref Des P2)

| Pin | Net | Comments | QUP |
|---|---|---|---|
| 1 | GND | Camera | |
| 3 | MIPI_CSI4_C1_LANE2_P | Camera | |
| 5 | MIPI_CSI4_A2_LANE2_N | Camera | |
| 7 | GND | Camera | |
| 9 | MIPI_CSI4_A1_LANE1_P | Camera | |
| 11 | MIPI_CSI4_B1_LANE1_N | Camera | |
| 13 | GND | Camera | |
| 15 | MIPI_CSI4_A0_CLK_N | Camera | |
| 17 | MIPI_CSI4_NC_CLK_P | Camera | |
| 19 | GND | Camera | |
| 21 | DMIC23_CLK | audio | |
| 23 | DMIC23_DATA | audio | |
| 25 | GND | | |
| 27 | VCOIN | RTC | |
| 29 | MIPI_CSI4_C2_LANE3_N | Camera | |
| 31 | MIPI_CSI4_B2_LANE3_P | Camera | |
| 33 | GND | Camera | |
| 35 | MIPI_CSI4_C0_LANE0_N | Camera | |
| 37 | MIPI_CSI4_B0_LANE0_P | Camera | |
| 39 | CABC_CON | | |
| 41 | GND | | |
| 43 | CAM_MCLK6 | | |
| 45 | CCI_I2C_SDA2 | | |
| 47 | CCI_I2C_SCL2 | | |
| 49 | VBAT_CONN | Power | |
| 51 | VBAT_CONN | Power | |
| 53 | VREG_BOB | LDO | |
| 55 | DMIC01_CLK | audio | |
| 57 | DMIC01_DATA | audio | |
| 59 | GND_P59 | | |
| 61 | MIPI_CSI5_A1_LANE1_P | Camera | |
| 63 | MIPI_CSI5_B1_LANE1_N | Camera | |
| 65 | GND | Camera | |
| 67 | MIPI_CSI5_NC_CLK_P | Camera | |
| 69 | MIPI_CSI5_A0_CLK_N | Camera | |
| 71 | GND | Audio | |
| 73 | CDC_IN4_M | Audio | |
| 75 | CDC_IN4_P | Audio | |
| 77 | CDC_IN5_P | Audio | |
| 79 | CDC_IN5_M | Audio | |
| 81 | MIC_BIAS1 | Audio | |
| 83 | GND | Audio | |
| 85 | MIPI_CSI5_B0_LANE0_P | Audio | |
| 87 | MIPI_CSI5_C0_LANE0_N | Audio | |
| 89 | GND | | |
| 91 | MIPI_CSI5_C1_LANE2_P | Camera | |
| 93 | MIPI_CSI5_A2_LANE2_N | Camera | |
| 95 | GND | Camera | |
| 97 | MIPI_CSI5_B2_LANE3_P | Camera | |
| 99 | MIPI_CSI5_C2_LANE3_N | Camera | |

| Pin | Net | Comments | QUP |
|---|---|---|---|
| 2 | GND | Camera | |
| 4 | MIPI_CSI1_A0_CLK_N | Camera | |
| 6 | MIPI_CSI1_NC_CLK_P | Camera | |
| 8 | GND | Camera | |
| 10 | MIPI_CSI1_C0_LANE0_N | Camera | |
| 12 | MIPI_CSI1_B0_LANE0_P | Camera | |
| 14 | GND | Camera | |
| 16 | MIPI_CSI1_A1_LANE1_P | Camera | |
| 18 | MIPI_CSI1_B1_LANE1_N | Camera | |
| 20 | GND | Camera | |
| 22 | MIPI_CSI1_A2_LANE2_N | Camera | |
| 24 | MIPI_CSI1_C1_LANE2_P | Camera | |
| 26 | GND | Camera | |
| 28 | MIPI_CSI1_C2_LANE3_N | Camera | |
| 30 | MIPI_CSI1_B2_LANE3_P | Camera | |
| 32 | GND | Camera | |
| 34 | USB2_SS_RX_M | USB | |
| 36 | USB2_SS_RX_P | USB | |
| 38 | GND | USB | |
| 40 | USB2_SS_TX_M | USB | |
| 42 | USB2_SS_TX_P | USB | |
| 44 | GND | USB | |
| 46 | CAM_MCLK5 | | |
| 48 | CAM_MCLK1 | | |
| 50 | CAM1_STANDBY_N | | |
| 52 | CAM1_RST_N | | |
| 54 | GND | | |
| 56 | MI2S2_WS | | |
| 58 | USB_VBUS | Power and battery | |
| 60 | USB_VBUS | Power and battery | |
| 62 | USB_VBUS | Power and battery | |
| 64 | VBAT_CONN | Power and battery | |
| 66 | VBAT_CONN | Power and battery | |
| 68 | GND | Power and battery | |
| 70 | VPH_PWR | Power and battery | |
| 72 | VPH_PWR | Power and battery | |
| 74 | VPH_PWR | Power and battery | |
| 76 | BATT_THERM | Power and battery | |
| 78 | BATT_ID | Power and battery | |
| 80 | VBATT_CONN_VSENSE_M | Power and battery | |
| 82 | VBATT_CONN_VSENSE_P | Power and battery | |
| 84 | MIC_BIAS3 | | |
| 86 | MIC_BIAS4 | | |
| 88 | GND | | |
| 90 | MI2S2_SCK | | |
| 92 | MI2S2_DATA0 | | |
| 94 | MI2S2_DATA1_REF_CLK | | |
| 96 | CCI_I2C_SDA3_CON | | |
| 98 | CCI_I2C_SCL3_CON | | |
| 100 | CAM5_RST_N_CON | | |

# 4.2 IO CONNECTOR GPIOS

- Refer processor datasheet for more details

**Table 14: IO CONNECTOR GPIOs**

| IO interface | pin | Net Name | Comments | QUP | QUP Number | GPIO | I2X/UART | Wake Capable |
|---|---|---|---|---|---|---|---|---|
| 1 | 6 | CAM_MCLK2 | | | | GPIO_96 | | |
| 1 | 10 | CCI_I2C_SCL1 | | | | GPIO_104 | I2C | Y |
| 1 | 12 | CAM_MCLK0 | | | | GPIO_94 | | |
| 1 | 14 | CCI_I2C_SDA1 | | | | GPIO_103 | I2C | Y |
| 1 | 66 | CAM3_RST_N | | | | GPIO_109 | | Y |
| 1 | 68 | CAM_MCLK3 | | | | GPIO_97 | | |
| 1 | 93 | SDM_GPIO_28 | GPIO | QUP_L0(0) | 0 | GPIO_28 | I3C | Y |
| 1 | 95 | SDM_GPIO_29 | GPIO | QUP_L1(0) | 0 | GPIO_29 | I3C | |
| 2 | 5 | CAM2_RST_N | | QUP_L0(14) | 14 | GPIO_40 | I3C | Y |
| 2 | 6 | FLASH_STROBE_TRIG | | | | GPIO_110 | | Y |
| 2 | 7 | CAM0_STANDBY_N | | QUP_L2(1) | 1 | GPIO_6 | | |
| 2 | 8 | WDOG_DISABLE | | QUP_L3(9) | 9 | GPIO_128 | | Y |
| 2 | 12 | SDM_GPIO_52_OR_139 | | QUP_L0(17) | 17 | GPIO_52 | UART | |
| 2 | 13 | SDM_FAST_BOOT_0 | | QUP_L3(8) | 8 | GPIO_27 | | Y |
| 2 | 15 | CAM0_RST_N | | QUP_L3(14) | 14 | GPIO_43 | | Y |
| 2 | 16 | SDM_GPIO_55_OR_141 | | QUP_L3(17) | 17 | GPIO_55 | UART | Y |
| 2 | 17 | FLASH_STROBE_EN | | | | GPIO_111 | | Y |
| 2 | 18 | SDM_GPIO_53_OR_140 | | QUP_L1(17) | 17 | GPIO_53 | UART | |
| 2 | 19 | CCI_I2C_SDA0 | | | | GPIO_101 | I2C | |
| 2 | 20 | SDM_GPIO_54_OR_138 | | QUP_L2(17) | 17 | GPIO_54 | UART | |
| 2 | 21 | CCI_I2C_SCL0 | | | | GPIO_102 | I2C | |
| 2 | 24 | CAM_MCLK4 | | | | GPIO_98 | | |
| 2 | 43 | TS_I2C_SCL | Touch | QUP_L1(13) | 13 | GPIO_37 | I2C | |
| 2 | 45 | TS_I2C_SDA | Touch | QUP_L0(13) | 13 | GPIO_36 | I2C | |
| 2 | 47 | BACKLIGHT_EN | Backlight Enable Out | QUP_L3(13) | 13 | GPIO_39 | | Y |
| 2 | 48 | SDM_GPIO_24_OR_160 | | QUP_L0(8) | 8 | GPIO_24 | I3C | Y |
| 2 | 49 | SDM_GPIO_5 | | QUP_L1(1) | 1 | GPIO_5 | I2C | |
| 2 | 50 | SDM_GPIO_25_OR_161 | | QUP_L1(8) | 8 | GPIO_25 | I3C | |
| 2 | 51 | TS_INT_N | Touch | QUP_L3(18) | 18 | GPIO_59 | UART | Y |
| 2 | 54 | CAM4_RST_N | | QUP_L1(10) | 10 | GPIO_130 | | |
| 2 | 56 | SDM_FAST_BOOT_1 | | QUP_L3(15) | 15 | GPIO_47 | | Y |
| 2 | 59 | SDM_GPIO_4 | | QUP_L0(1) | 1 | GPIO_4 | I2C | Y |
| 2 | 60 | SD_UFS_CARD_DET_N | Sdcard | | | GPIO_77 | | Y |
| 2 | 61 | SDM_DEBUG_UART_TX | Debug UART | QUP_L2(12) | 12 | GPIO_34 | UART | |
| 2 | 63 | SDM_DEBUG_UART_RX | Debug UART | QUP_L3(12) | 12 | GPIO_35 | UART | Y |

| IO interface | pin | Net Name | Comments | QUP | QUP Number | GPIO | I2X/UART | Wake Capable |
|---|---|---|---|---|---|---|---|---|
| 2 | 91 | PCIE2_CLK_REQ_N | pcie | | | GPIO_86 | | Y |
| 2 | 92 | SDM_GPIO_41 | | QUP_L1(14) | 14 | GPIO_41 | I3C | |
| 2 | 93 | PCIE2_WAKE_N | pcie | | | GPIO_87 | | Y |
| 2 | 94 | CAM2_STANDBY_N | | QUP_L0(4) | 4 | GPIO_8 | | |
| 2 | 95 | PCIE2_RST_N | pcie | | | GPIO_85 | | |
| 2 | 97 | SDM_GPIO_30 | | QUP_L2(0) | 0 | GPIO_30 | | |
| 2 | 99 | SDM_GPIO_31 | | QUP_L3(0) | 0 | GPIO_31 | | Y |
| 3 | 43 | CAM_MCLK6 | | | | GPIO_100 | | Y |
| 3 | 45 | CCI_I2C_SDA2 | | | | GPIO_105 | I2C | |
| 3 | 46 | CAM_MCLK5 | | | | GPIO_99 | | |
| 3 | 47 | CCI_I2C_SCL2 | | | | GPIO_106 | I2C | |
| 3 | 48 | CAM_MCLK1 | | | | GPIO_95 | | |
| 3 | 50 | CAM1_STANDBY_N | | QUP_L3(1) | 1 | GPIO_7 | | Y |
| 3 | 52 | CAM1_RST_N | | QUP_L1(4) | 4 | GPIO_9 | | |

# 4.3 ELECTRICAL SPECIFICATIONS OF PINS

**Table 15: IO CONNECTOR Power specifications**

| Voltage rail | Min V | Typical V | Max V |
|---|---|---|---|
| VBAT | 3.2 | 3.8V | 4.5 |
| 1.8V Out | 1.7 | 1.8 | 1.9 |
| SDCard Power | 2.7 | 2.95 | 3.6 |
| SDC2 IO | 1.7/2.7 | 1.8/2.95 | 1.9/3.04 |
| VCOIN | 2 | 3 | 3.25 |
| USB_VBUS | 3.6 | 5 | 13.2 |

**Table 16: IO specifications**

| 1.8V GPIO | Min V | Typical V | Max V |
|---|---|---|---|
| VIH | 1.26 | - | 2.1 |
| VIL | -0.3 | - | 0.54 |
| VOH | 1.35 | - | 1.8 |
| VOL | 0 | - | 0.45 |
| **SDCard IO 2.95V** | **Min V** | **Typical V** | **Max V** |
| VIH | 1.84 | - | 3.25 |
| VIL | -0.3 | - | 0.735 |
| VOH | 2.21 | - | 2.95 |
| VOL | 0 | - | 0.36 |
| **SDCard IO 1.8V** | **Min V** | **Typical V** | **Max V** |
| VIH | 1.27 | - | 2 |
| VIL | -0.3 | - | 0.58 |
| VOH | 1.4 | - | - |
| VOL | - | - | 0.45 |

# 4.4 RF CONNECTORS

Manufacturer : I-PEX

Manufacturer Part : 20449-001E-03

Description : MHF4 Coaxial RF connector

Functions :Wi-Fi, Bluetooth

**CAUTION**

Make sure that RF cable crimps are not touching any components nearby after assembled.

# 5. CONTACT INFORMATION

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| | |
|---|---|
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