DSPB56374SUG
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DSPB56374 Software Users Guide

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Chapter 1
Introduction

1.1 Feature and Architecture

The DSPB56374 digital audio decoder is designed to provide a high level of system integration for Digital Audio functionality with reduced complexity of operation over competitive market solutions. This solution is targeted as both a main processor for some applications, as well as an “add-on” device to upgrade functionality in high-end applications, such as low-tier AV receivers, mini-systems, televisions and car audio.

The architecture is based on the mini-SA adapted from the original Software Architecture (SA) implemented in Freescale Semiconductors (formerly Motorola) digital audio processors, including High-Level Executive (HLX), Low-Level Executive (LLX), Post-Processing Phases (PPP) and Input/Output components. The HLX runs a booting sequence, which takes charge of the initialization and configuration of the whole system. The LLX is the decoder for the different standard input bit-stream formats with multi-channel PCM being the only decoder (except NG) on the DSPB56374. Several PPPs are included in the ROM of the DSPB56374 to provide a variety of common audio functions. Four HLXs are provided by the DSPB56374 ROM for different application categories, as illustrated in Figure 1-1 through Figure 1-3. They are Automotive Application, AV/DVD Receiver Application, Television Application, and generic respectively. In each figure, some PPPs are provided in ROM (shown in gray boxes) and can be activated in user-defined slots. Other PPPs can be downloaded into RAM (shown in white boxes) and activated in user-defined slots. The figures also indicate that some PPPs are designed to operate mutually exclusive of each other (e.g., Level Meter and Spectrum Level Analyzer cannot operate at the same time).

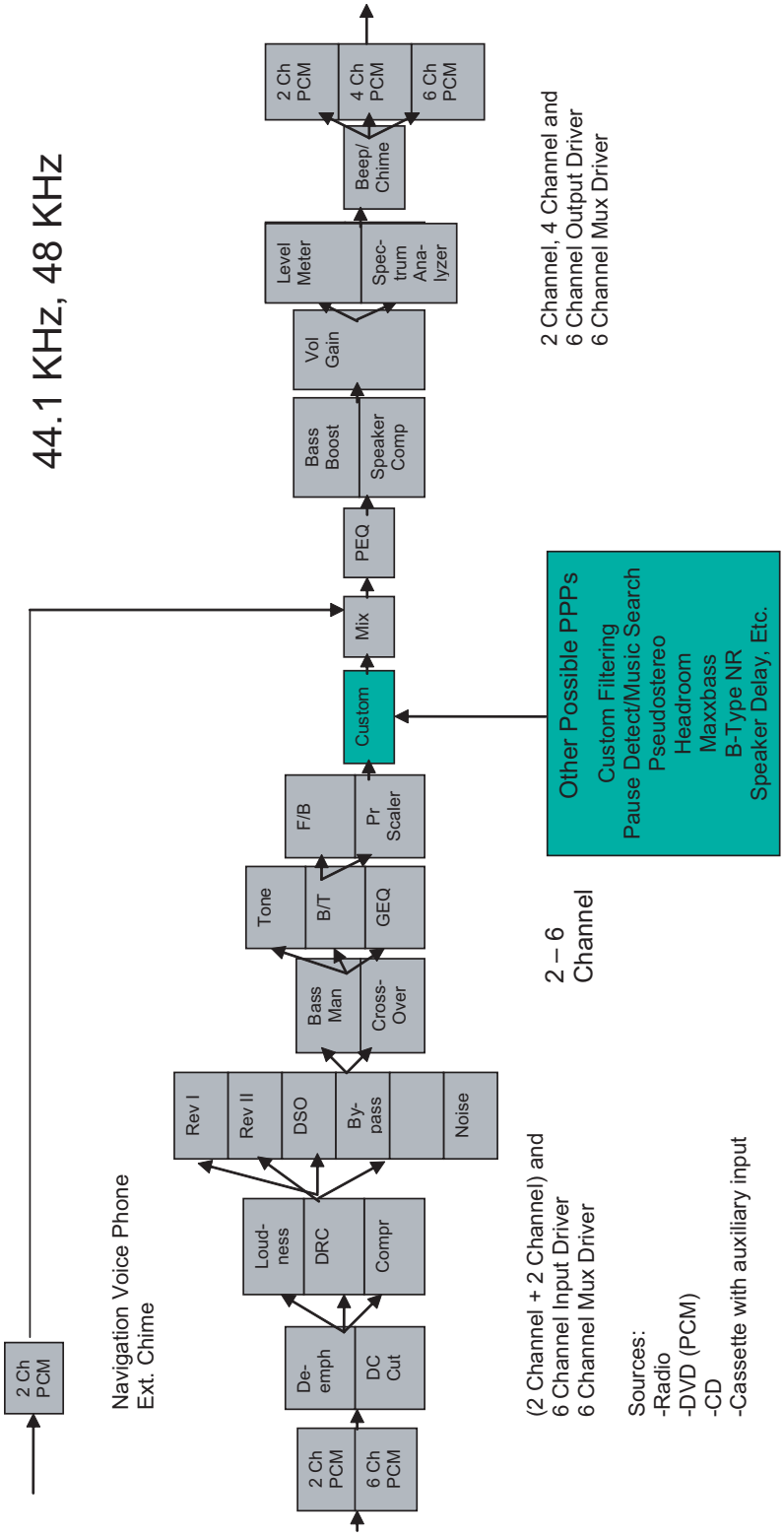


Figure 1-1. Automotive Application Example (Green HLX)

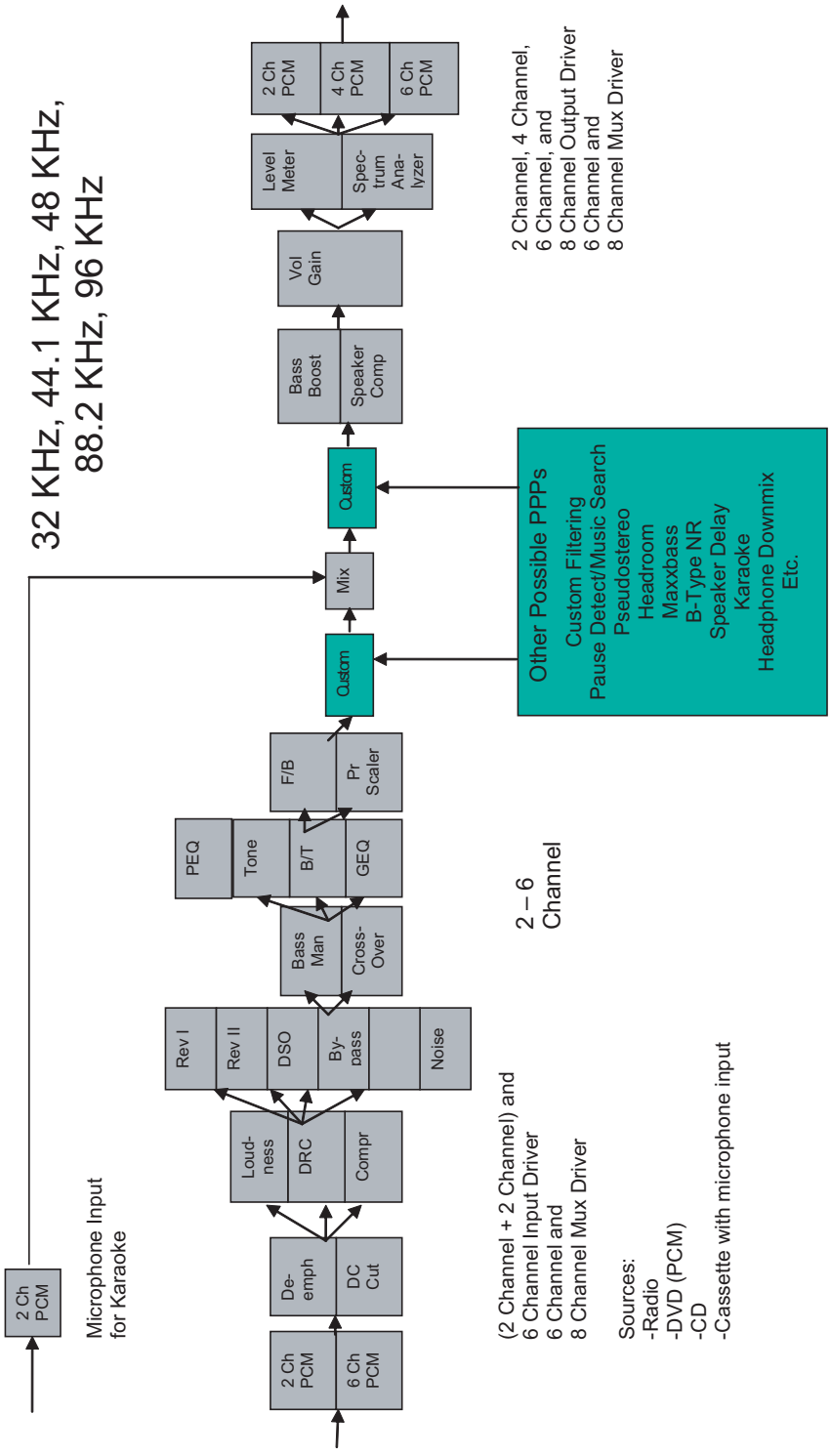


Figure 1-2. AV/DVD Receiver Application Example (Blue HLX)

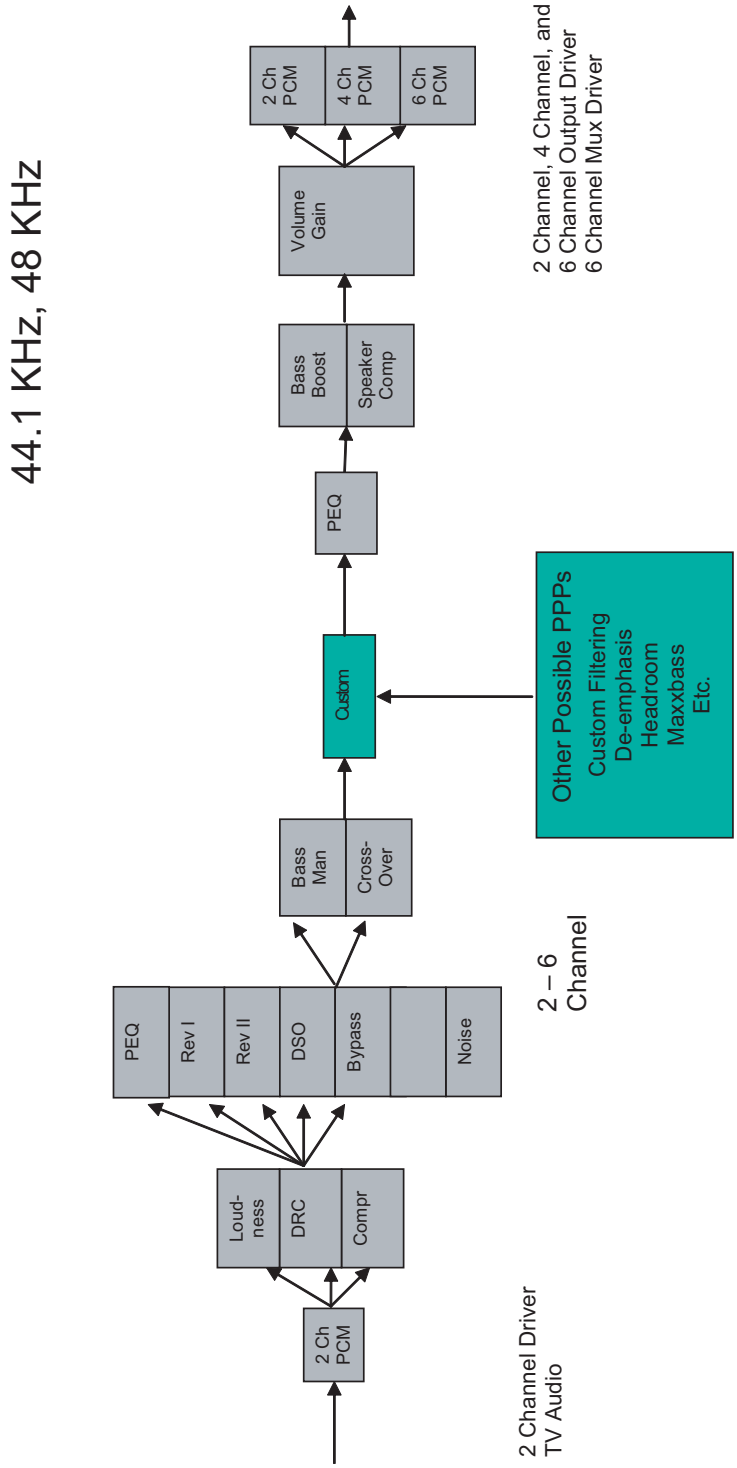


Figure 1-3. Television Application Example (Orange)

1.2 Users Guide Structure

The DSPB56374 Software Users Guide focuses on the description of system function and specifically lists the important Chirp commands to check the running status and adjust the configuration. Chapter 1 introduces the outline of the DSPB56374; Chapter 2 introduces the High Level Executive; Chapter 3 introduces the Low Level Executives, including their common behaviors and separate functions; Chapter 4 introduces the Dual Chip Solution for DSPB56374; Chapter 5 introduces the Bootstrap Modes provided on the DSPB56374; Chapter 6 introduces the standard Post Processing Phase; Chapter 7 introduces the Input/Output drivers; and Chapter 8 introduces the GPIO Manager.

1.3 Acronyms and Abbreviations

AAC	Advanced Audio Coding
AC-3	ATSC Digital Audio Compression Standard A/52
HLX	High Level Executive
LLX	Low Level Executive
MLX	Middle Level Executive
PDC	Post Decoder Control Block
PPP	Post Processing Phase
SA	Software Architecture
uC	Microcontroller
CHIRP	Communications Host Interface Remote Protocol
MPCM	Multi-channel PCM Decoder

Chapter 2
High-Level Executive

2.1 Overview

The DSPB56374 provides four HLXs, Green/Blue/Orange/Red, which are for Automotive, A/V, TV and Generic application, respectively. All HLXs provide multi-channel decoding and post processing of input bit streams, as well as noise generation. All HLX provide 8-channel decoding capabilities via the MPCM decoder. All HLXs provide 6-channel subwoofer management. All HLXs provide auto-detection capability, which can detect PCM/ DTS/AC3/AAC bit-stream, although the DSPB56374 only provides PCM decoding capability. Any DTS/AC3/AAC input bitstream will be muted at the output. In the case where a bit-stream format is not recognized, that bit stream will be processed as PCM. In order to reduce memory size, a tri-buffer mechanism is adopted by the DSPB56374. The DSPB56374 does not provide rate-doubling functionality.

All HLXs are classified as 48 kHz in their default setting.

The four HLXs differ in the PPPs, which are available to the user, as described in Table 2-1.

2.2 HLX Models

The DSPB56374 supports four HLXs, which are designed for Automotive, A/V, TV and Generic applications, respectively. The PPP slots are all empty except for the volume and gain PPPs, which are enabled upon reset. The DSPB56374 HLX arranges and gives the default PPP chain setup for each application, which is detailed in Chapter 6.

The HLX in the DSPB56374 has four models: Red, Blue, Orange and Green. The following table indicates their basic features and differences. All HLXs have the same features except for the PPPs available to the user.

Table 2-1. HLX in DSPB56374

HLX	Decoder	Output Channel	SWM	Maximum Delay	PPP
Red (Generic)	MPCM Noise Generator	8	5.1	C 5ms@48 kHz Ls 15ms@48 kHz Rs 15ms@48 kHz	Volume Manager Digital Gain
Blue (AV)	MPCM Noise Generator	8	5.1	C 5ms@48 kHz LS 15ms@48 kHz RS 15ms@48 kHz	De-emphasis & DC-Cut Loudness Compression Dynamic Range Control Tone Control Bass Treble Graphic EQ Parametric EQ Fade Balance Pre-Scaler Bass Boost Speaker Compensation Delay Manager Volume Gain Level Meter Spectrum Analyzer

Table 2-1. HLX in DSPB56374 (continued)

HLX	Decoder	Output Channel	SWM	Maximum Delay	PPP
Green (Automotive)	MPCM Noise Generator	8	5.1	C 5ms@48 kHz LS 15ms@48 kHz RS 15ms@48 kHz	Pause Decoder De-emphasis & DC-Cut Loudness Compression Dynamic Range Control Tone Control Bass Treble Graphic EQ Fade Balance Pre-Scaler Parametric EQ Bass Boost Speaker Compensation Delay Manager Volume Gain Level Meter Spectrum Analyzer Beep Chime
Orange (TV)	MPCM Noise Generator	8	5.1	C 15ms@48 kHz LS 25ms@48 kHz RS 25ms@48 kHz	Loudness Compression Dynamic Range Control Parametric EQ Bass Boost Speaker Compensation Delay Manager Volume Gain

Omega HLX

Omega/I²C The Omega/I²C HLX provides Chirp/I²C and Crimp processing. Crimp provides capabilities that allow Chirp opcodes to be processed from within user code executing on the DSPB56374. Two-word Chirp Type II and Type III Write opcodes can be processed using the RunCrimpA10 entry point as shown in Table 2-2. One-word Chirp Type IV and Type V Write opcodes and Type II–V Read opcodes can be processed using the RunCrimpA1 entry point as shown in Table 2-2, respectively. Chirp Type 0 Chirp Write and Read opcodes can be processed using the RunCrimpA10 and RunCrimpA1 entry points as for Chirp Type II Write and Read opcodes, respectively. Multi-word Type I Chirp opcodes cannot be processed using the Crimp facility.

Table 2-2. Crimp Processing Entry

Chirp Type	Number of Words	Read/Write	Run Crimp Entry
II III	2	Write	RunCrimp A10
IV V	1	Write	RunCrimp A1
II-V	1	Read	RunCrimp A1
0	Any	Read/Write	RunCrimp A10 RunCrimp A1
I	Any	Read/Write	N/A

Crimp Type II/III Write Example

```
move    #setHLXSpeakerFront, a1
move    #sotHLXSpeakerFrontDefault, a0
jsr     RunCrimpA10; process 2-word write opcode
```

Crimp Type IV/V Write Example

```
move    #setHLXSourceModePCM, a1
jsr     RunCrimpA1; process 1-word write opcode
```

Crimp Type II–V Read Example

```
move    #getHLXStatusSourceModePCM, a1
jsr     RunCrimpA1; process read opcode
move    a1, x: value; save result
```

Omega/I²C. The Omega/I²C HLX provides Chirp/I²C and Crimp processing capabilities.

2.3 HLX Control Function

2.3.1 System Error Number Status

The ERRNO Status Register is written and read by the opcodes shown below. The Error Number Register reflects the type of error occurring when the system is running; an error will cause the system to reboot. The Error PC Register records the PC when encountering an illegal instruction.

Table 2-3. System Symbolic Opcodes

Symbol	Description	Value
setERRNO	Set Error Number Register Value	0xc20100
getERRNO	Report Error Number Register Value	0x820100
ERRNO_ROMReset	System Boot	0x000000
ERRNO_RAMReset	Hardware RESET	0x000001
ERRNO_StackError	Stack Error	0x000002

Table 2-3. System Symbolic Opcodes (continued)

ERRNO_IllegalInstruction	Illegal Instruction	0x000003
ERRNO_DebugRequest	Debug Request	0x000004
ERRNO_Trap	Trap	0x000005
ERRNO_NMI	Non-Maskable Interrupt	0x000006
setERRPC	Set Error PC Register Value	0xc20101
getERRPC	Report Error PC Register Value	0x820101

2.3.2 Mute Processing

The HLX provides mute processing via commands, a control register, a status register, a logical GPIO input pin, and a logical GPIO output pin. The actual realization of this mute processing capability relies, however, on the mapping of the logical GPIO pins to physical signals for the DSPB56374.

If the LOCK* and MUTE* logical GPIO pins are not connected to physical pins as per the GPIO mapping provided in these GPIO models, mute processing capabilities are not provided. In this case, the mute processing operations have no effect on the rest of the system.

Table 2-4. Mute Processing Symbolic Opcodes

Symbol	Description	Value
setHLXConfigMuteOff	MUTE* is low (Un-mute)	0xe00406
setHLXConfigMuteOn	MUTE* is high (Mute)	0xe00407
setHLXUnmuteBlockLimit_0	Set Number of Blocks by which to Delay Un-mute	0xe02500
getHLXStatusMute	Get Mute Status -- Non-zero Indicates that Mute is Active	0xa02300
getHLXUnmuteBlockLimit	Get Number of Blocks by which to Delay Un-mute	0xa02500
getHLXUnmuteBlockCount	Get Delay Un-mute Count	0xa02600

2.3.3 Source Mode Support

The DSPB56374 supports three source modes: Auto, PCM and Noise Generator. Auto mode is the default setting and refers to the auto-detection mode. The following commands can be used to detect the current source mode.

Table 2-5. Source Mode Status Checking Symbolic Opcodes

Symbol	Description	Value
getHLXStatusSourceMode	Report Source Mode Status Register	0xa02100
gotHLXStatusSourceModeAuto	The Values Corresponding to Source Modes	0x000000
gotHLXStatusSourceModeNoise		0x000001
gotHLXStatusSourceModePCM		0x000002

2.3.4 Listening Mode Support

The DSPB56374 provides six listening modes: ProLogic (Lt/Rt), Mono, Stereo, Phantom, 3-Stereo and Surround. If a conflict occurs between the Listening Mode Control Register and the Speaker Control Register listed below, the speaker-control setting takes priority, i.e., speakers will only be active if they are present in the system.

Table 2-6. Listening Mode Control Symbolic Opcodes

Symbol	Description	Value
setHLXListeningModeProLogic	Set Control Register Value	0xe00a00
setHLXListeningModeMono		0xe00a01
setHLXListeningModeStereo		0xe00a02
setHLXListeningModePhantom		0xe00a03
setHLXListeningMode3Stereo		0xe00a04
setHLXListeningModeSurround		0xe00a05
getHLXListeningMode	Report Control Register Value	0xa00a00

2.3.5 Speaker Control Support

In the DSPB56374, if speaker control is enabled, the relevent downmix and output configuration will be applied according to the following commands. These commands should be used to configure the size and number of speakers in the system.

Table 2-7. Speaker Control Symbolic Opcodes

Symbol	Description	Value
setHLXSpeakerControlEnable	Enable or Disable Speaker Control.	0xe00d01
setHLXSpeakerControlDisable		0xe00d00
setHLXSpeakerSubwooferNone	Set the Attributes of Left, Right, Center, Surround, Back and Subwoofer Speakers, Respectively	0xe00e00
setHLXSpeakerSubwooferWide1		0xe00e11
setHLXSpeakerLeftRightNarrow2		0xe01102
setHLXSpeakerLeftRightWide2		0xe01112
setHLXSpeakerCenterNone		0xe01200
setHLXSpeakerCenterNarrow1		0xe01201
setHLXSpeakerCenterWide1		0xe01211
setHLXSpeakerSurroundNone		0xe01300
setHLXSpeakerSurroundNarrow1		0xe01301
setHLXSpeakerSurroundNarrow2		0xe01302
setHLXSpeakerSurroundWide1		0xe01311
setHLXSpeakerSurroundWide2		0xe01312
setHLXSpeakerBackNone		0xe00f00
setHLXSpeakerBackNarrow1		0xe00f01
setHLXSpeakerBackNarrow2		0xe00f02
setHLXSpeakerBackWide1		0xe00f11
setHLXSpeakerBackWide2		0xe00f12

Table 2-7. Speaker Control Symbolic Opcodes (continued)

Symbol	Description	Value
getHLXSpeakerControl	Get theAttributes of Left, Right, Center, Surround, Back and Subwoofer Speakers, Respectively	0xa00d00
getHLXSpeakerSubwoofer		0xa00e00
getHLXSpeakerBack		0xa00f00
getHLXSpeakerLeftRight		0xa01100
getHLXSpeakerCenter		0xa01200
getHLXSpeakerSurround		0xa01300

2.3.6 Listening Format and Program Format Support

The DSPB56374 extracts listening format information from the MLX audio-mode status to show currently working channels, which represent the audio mode at the DSP output. The program format is extracted from the LLX audio-mode status to represent which channels are active at the input, which determines the audio mode of incoming bit streams.

Table 2-8. Program Format Status Symbolic Opcodes

Symbol	Description	Value
getHLXStatusProgramFormat	Report Program Format	0x880006
gotBitLeft	Value Reflecting the Working Channel at Input	0x000001
gotBitRght		0x000002
gotBitLSur		0x000004
gotBitRSur		0x000008
gotBitCntr		0x000010
gotBitSubw		0x000020
gotBitLAux		0x000040
gotBitRAux		0x000080
gotBitLSec		0x000100
gotBitRSec		0x000200
gotBitSSur	Report Single Surround Channel (Ls) at Input	0x010000
gotBitStatusProgramFormatNotSurround	Report No Surround Channel Encoded at in Input Bitstream	0x020000
gotBitStatusProgramFormatYesSurround	Report Surround Channel Encoded at in Input Bitstream	0x040000
gotBitStatusProgramFormatDualMono	Report Mono on L/R Channels at Input Bitstream	0x080000
gotBitLFE	Report LFE Channel Exists at Input Bitstream	0x100000
gotBitValidAudioMode	Report Input Bitstream Audio Mode is Supported	0x800000

Table 2-9. Listening Format Status Symbolic Opcodes

Symbol	Description	Value
getHLXStatusListeningFormat	Report Listening Format.	0x880007
gotBitLeft	Value Reflecting the Working Channel at Output.	0x000001
gotBitRght		0x000002
gotBitLSur		0x000004
gotBitRSur		0x000008
gotBitCntr		0x000010
gotBitSubw		0x000020
gotBitLAux		0x000040
gotBitRAux		0x000080
gotBitLSec		0x000100
gotBitRSec		0x000200
gotBitSSur		0x010000

2.3.7 Free MIPS Report

The DSPB56374 can display the MIPS available over the interval between the following two chirp commands: setHLXConfigFreeMIPS (which resets the MIPS counter), and getHLXStatusFreeMIPS (which displays the MIPS available) as shown in Table 2-10.

Table 2-10. Free MIPS Symbolic Opcodes

Symbol	Description	Value
setHLXConfigFreeMIPS	Reset MIPS Counter.	0xe00408
getHLXStatusFreeMIPS	Report Free MIPS	0xa02200

2.3.8 Sample Rate Support

The DSPB56374 reports the output sample rate via the MLX sample rate register, with the following commands:

Table 2-11. Sample Rate Status Symbolic Opcodes

Symbol	Description	Value
getMLXSampleRate	Report the Sample Rate at the Output of the System.	0x880402
gotMLXSampleRate48000Hz		0x000000
gotMLXSampleRate44100Hz		0x000001
gotMLXSampleRate32000Hz		0x000002
gotMLXSampleRate96000Hz		0x000003
gotMLXSampleRate88200Hz		0x000004
getLLXStatusEncodedSampleRate	Report the Sample Rate of the Bitstream at the Input to the Decoder	0xa23300
getLLXStatusDecodedSampleRate	Report the Sample rate of the Data Stream at the Output of the Decoder	0xa23700

2.3.9 Audio Status Report

The MLX audio-status register of the DSPB56374 is accessed with the following commands.

Table 2-12. Audio Status Symbolic Opcodes

Symbol	Description	Value
getMLXAudioStatus	Report Audio Status at Output	0x880404
gotBitMLXAudioStatusLFEPresent	LFE is Generated by the LLX	0x000002
gotBitMLXAudioStatusEncodedKaraoke	Encoded Karaoke Status in Input	0x000010
gotBitMLXAudioStatusEncodedSurround	Indicate Surround Channels Encoded at Input Bitstream	0x000020
gotBitMLXAudioStatusDecodedSurround	Indicate Decoder has not Decoded the Surround Channels Encoded in the Input Bitstream; Output Channels are Still Surround Encoded	0x000040
gotBitMLXAudioStatusChangedSampleRate	Input and Output Sample Rates Dffer	0x000080

2.3.10 Volume Control Support

In the DSPB56374, the Volume Control Register (VCR) consists of three parts: VCR Track Volume, VCR Master Volume and VCR Channel Volume. The VCR Track Volume controls the maximum output power. The setting in the VCR Master Volume causes changes in all of the output channels. The VCR Channel Volume controls the respective channel. Increments and decrements in all three registers are in steps of 0.5 dB.

Table 2-13. Volume Control Symbolic Opcodes

Symbol	Description	Value
setVCRTrack	Set VCR Track Volume	0xc80200
setVCRMaster	Set VCR Master Volume	0xc80201
setVCRLeft	Set VCF Channel Volume	0xc80202
setVCRRght		0xc80203
setVCRLSur		0xc80204
setVCRRSur		0xc80205
setVCRCntr		0xc80206
setVCRSubw		0xc80207
setVCRLAux		0xc80208
setVCRRAux		0xc80209
getVCRTrack	Report VCR Track Volume	0x880200
getVCRMaster	Report VCR Master Volume	0x880201

Table 2-13. Volume Control Symbolic Opcodes (continued)

Symbol	Description	Value
getVCRLeft	Report VCR Channel Volume	0x880202
getVCRRght		0x880203
getVCRLSur		0x880204
getVCRRSur		0x880205
getVCRCntr		0x880206
getVCRSubw		0x880207
getVCRLAux		0x880208
getVCRRAux		0x880209

2.3.11 Audio-mode Support

When speaker control is disabled, customers can directly define the suitable audio mode in the LLX downmix control register and report the audio mode status by the MLX audio-mode register, as shown in Table 3-5. The audio mode control includes two methods: MLX control and LLX control. The MLX control is used to reflect the audio data status after post processing (PPP chain) in the SA system. The LLX control is the actual downmix control in the LLX layer, so it can determine the PPP's behavior effectively.

2.3.12 Audio Generator Report

In the DSPB56374, the MLX audio generator register reflects the type of the currently working decoder.

Table 2-14. Audio Generator Symbolic Opcodes

Symbol	Description	Value
getMLXAudioGen	Report audio generator	0x880405
Noise Generator	The value corresponding to the decoder type.	0x000001
MPCM		0x000002

Chapter 3
Low-Level Executive

3.1 Overview

The DSPB56374 provides two LLXs to customers, Noise Generator, and MPCM in different HLX. Refer to section 2, High-Level Executive for further details. The capabilities of these LLXs are described below.

3.2 General LLX

3.2.1 LLX Configuration

Table 3-1. LLX Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXConfig	Set LLX Configuration	0xc80801
sotLLXConfigDisable		0x000000
sotLLXConfigEnable		0x000001
setLLXConfigNone	Restart LLX	0xe20400
getLLXConfig	Report LLX configuration.	0x880801
gotLLXConfigEnable		0x000001
gotLLXConfigDisable		0x000000

3.2.2 LLX Status

The LLX updates the LLX Status Register according to the different states that exist and that can be seen in Table 3-2. Here, (x) means LLX output is muted (continuous zero output in some fashion) except in continuing normal or error operation.

Table 3-2. LLX Status Symbolic Opcodes

Symbol	Description	Value
getLLXStatus	Report LLX status	0x880800
gotLLXStatusInit	Loaded but not running. (x)	0x000000
gotLLXStatusSearch	Searching for sync. (x)	0x000001
gotLLXStatusDecode	Normal operation.	0x000002
gotLLXStatusPause	IEC 60958 pause. (x)	0x000003
gotLLXStatusError	Error but continuing.	0x000004
gotLLXStatusFail	Error and stopped (x), exit because of bit-stream error.	0x000005
gotLLXStatusDone	No error, and stopped. (x) Exit because of request or detect.	0x000006

3.2.3 LLX Scale Control

For DSPB56374, the scale range is from –2 to 2. In order to set the scale range in Hex, the user must use the factor, ½, before the setting. The scale range is from $800000 to $7fffff in Hex. The setting example refers to Table 3-4.

Table 3-3. LLX Scale Control Symbolic Opcodes

Symbol	Description	Value
setLLXScale	Configure the Scale of LLX.	0xc80802
getLLXScale	Report the configuration of LLXScale.	0x880802

Table 3-4. LLX Scale Control Setting Example

Required Scale Range Value	Setting Value in Hex
1.99999976	$c80802 $7fffff
1	$c80802 $400000
0.5	$c80802 $200000
-0.5	$c80802 $E00000
-1	$c80802 $C00000
-2	$c80802 $800000

3.2.4 LLX Downmix Control

LLX Downmix control register is able to directly decide the output data's audio mode in the system when speaker control is disabled; otherwise, it is immediately overwritten by speaker control register. Its content is listed in Table 3-5.

Table 3-5. Audio Mode Control and Status Symbolic Opcodes

Symbol	Description	Value
setLLXDownmix	Set downmix directly when speaker control is disabled. X/Y: X represents Lf/C/Rf, and Y represents Ls/Rs/La/Ra. X: 1→ C 2→ Lf/Rf 3→ Lf/C/Rf Y: 0→ None 1→ Ls 2→ Ls/Rs 3→ Ls/Cs/Rs 4→ Ls/Rs/Lb/Rb	0xc80803
setLLXDownmixProLogic(0/0)		0xe20c00
setLLXDownmixMono(1/0)		0xe20c01
setLLXDownmixStereo(2/0)		0xe20c02
setLLXDownmixStereo3(3/0)		0xe20c03
setLLXDownmixPhantom(2/2)		0xe20c06
setLLXDownmixSurround(3/2)		0xe20c07
setLLXDownmixPhantom1(2/1)		0xe20c04
setLLXDownmixSurround1(3/1)		0xe20c05
setLLXDownmixMono2(1/0)		0xe20c08
setLLXDownmixStereoUnknown(2/0)		0xe20c09
setLLXDownmixPhantom3(2/3)		0xe20c0c
setLLXDownmixSurround3(3/3)		0xe20c0d
setLLXDownmixPhantom4(2/4)		0xe20c0e
setLLXDownmixSurround4(3/4)		0xe20c0f
	Set corresponding audio mode with subwoofer.	0xe20c1X (0…f)
getLLXDownmix	Reports audio mode at LLX (The definition of the return value is the same as MLX audio mode register)	0x880803

Table 3-5. Audio Mode Control and Status Symbolic Opcodes (continued)

Symbol	Description	Value
getMLXAudioMode	Reports audio mode at output.	0x880403
gotMLXAudioModeProLogic	0/0: 2 front and 0 rear speakers	0x000000
gotMLXAudioModeMono	1/0: 1 front and 0 rear speakers	0x000001
gotMLXAudioModeStereo	2/0: 2 front and 0 rear speakers	0x000002
gotMLXAudioModeStereo3	3/0: 3 front and 0 rear speakers	0x000003
gotMLXAudioModePhantom1	2/1: 2 front and 1 rear speakers	0x000004
gotMLXAudioModeSurround1	3/1: 3 front and 1 rear speakers	0x000005
gotMLXAudioModePhantom	2/2: 2 front and 2 rear speakers	0x000006
gotMLXAudioModeSurround	3/2: 3 front and 2 rear speakers	0x000007
gotMLXAudioModeMonoOnLR	1/0: 1 front and 0 rear speakers	0x000008
gotMLXAudioModeStereoUnknown	2/0: 2 front and 0 rear speakers	0x000009
gotMLXAudioModeMonoMono	2/0: 2 front and 0 rear speakers	0x00000a
gotMLXAudioMode_b	0: without anything	0x00000b
gotMLXAudioModePhantom3	2/3: 2 front and 3 rear speakers	0x00000c
gotMLXAudioModeSurround3	3/3: 3 front and 3 rear speakers	0x00000d
gotMLXAudioModePhantom4	2/4: 2 front and 4 rear speakers	0x00000e
gotMLXAudioModeSurround4	3/4: 3 front and 4 rear speakers	0x00000f
gotBitMLXAudioModeBass	.1: 1 subwoofer	0x000010

3.2.5 LLX Sample Rate Detection Control

LLX Sample Rate Detection Register is used to directly set/get the input bit stream's sample rate by the commands shown in Table 3-6. These operations only work for the PCM LLX. Other LLX ignores it.

Table 3-6. LLX Sample Rate Detection Symbolic Opcodes

Symbol	Description	Value
setLLXSampleRate	The command takes effect when Sample Rate detection function is disabled. Refer to LLX Feature Control Table 3-13.	0xc80804
setLLXSampleRate48000Hz		0xe21000
setLLXSampleRate44100Hz		0xe21001
setLLXSampleRate32000Hz		0xe21002
setLLXSampleRate96000Hz		0xe21003
setLLXSampleRate88200Hz		0xe21004
getLLXSampleRate	Report the input bit stream's sample rate. The value of 'getLLXSampleRate' is written by the sample rate detection. When the sample rate detection is open, it will put the detected value into this place. If the sample rate detection is disabled, the value obtained by 0x880804 will never update even if the sample rate of the input bit-stream changes.	0x880804

Table 3-6. LLX Sample Rate Detection Symbolic Opcodes (continued)

Symbol	Description	Value
gotLLXSampleRate48000Hz		0x000000
gotLLXSampleRate44100Hz		0x000001
gotLLXSampleRate32000Hz		0x000002
gotLLXSampleRate96000Hz		0x000003
gotLLXSampleRate88200Hz		0x000004

DSPB56374 supports sample rate detection for non-sample rate encoded bitstreams with ESAI input driver and reports the detected sample rate via the LLX sample rate register.

Table 3-7. Sample Rate Detection for Non-encoded sample rate bitstream Symbolic Opcodes

Symbol	Description	Value
getMLXInputSampleRate	Report the compensated timer counter value during the sample rate detection	0x88080b
setMLXDSPFrequency	Set the reciprocal of exact DSP working frequency (MHz is the unit). Default value is $00b60b(1/180).	0xc8080c
getLLXSampleRate	Report the detected input sample rate.	0x880804
gotLLXSampleRate48000Hz		0x000000
gotLLXSampleRate44100Hz		0x000001
gotLLXSampleRate32000Hz		0x000002
gotLLXSampleRate96000Hz		0x000003
gotLLXSampleRate88200Hz		0x000004

3.2.6 LLX Status Audio Control

The control of LLX Audio Status is implemented by two registers, LLX Status Audio Mode Register and LLX Status Audio Status Register. The LLX Status Audio Mode Register is used to configure the input audio mode. In DSPB56374, for the input data is PCM, the standard audio mode of PCM is 2/0.0 (L/R), so use the commands shown at Table 3-8 to set the different audio mode. If the input PCM data has to be dealt as the Lt/Rt PCM data or PCM data carrying the LFE information without configuring the data's Audio Mode, the LLX Status Audio Status Register is the choice here, shown at Table 3-9.

Table 3-8. LLX Status Audio Mode Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXStatusAudioMode	Set LLX Status Audio Mode of input data.	0xc80806
sotLLXAudioModeBassEnable		0x000010
sotLLXAudioModeProLogic	2/0.0 (Lt, Rt)	0x000000
sotLLXAudioModeMono	C	0x000001
sotLLXAudioModeStereo	2/0.0 (Lo, Ro)	0x000002
sotLLXAudioModeStereo3	3/0.0 (L,C,R)	0x000003
sotLLXAudioModePhantom1	2/1.0 (L,R,Sub)	0x000004
sotLLXAudioModeSurround1	3/1.0 (L,C,R,Sub)	0x000005
sotLLXAudioModePhantom2	2/2.0 (L,R,LS,RS)	0x000006
sotLLXAudioModeSurround2	3/2.0 (L,C,R,LS,RS)	0x000007

Table 3-8. LLX Status Audio Mode Configuration Symbolic Opcodes (continued)

Symbol	Description	Value
sotLLXAudioModeMonoOnLR	1/0.0 (Lm,Lm)	0x000008
sotLLXAudioModeStereoUnknown	2/0.0 (Lu,Ru)	0x000009
sotLLXAudioModeDualMono	2/0.0 (M1,M2)	0x00000a
sotLLXAudioMode_b	2/0.0 (M1,M2)	0x00000b
sotLLXAudioModePhantom3	2/3.0 (L,R,LS,RS,B)	0x00000c
sotLLXAudioModeSurround3	3/3.0 (L,C,R,LS,RS,B)	0x00000d
sotLLXAudioModePhantom4	2/4.0 (L,R,LS,RS,LB,RB)	0x00000e
sotLLXAudioModeSurround4	3/4.0 (L,C,R,LS,RS,LB,RB)	0x00000f
getLLXStatusAudioMode	Report the LLX Status Audio Mode's configuration.	0x880806
gotLLXAudioModeBassEnable		0x000010
gotLLXAudioModeProLogic		0x000000
gotLLXAudioModeMono		0x000001
gotLLXAudioModeStereo		0x000002
gotLLXAudioModeStereo3		0x000003
gotLLXAudioModePhantom1		0x000004
gotLLXAudioModeSurround1		0x000005
gotLLXAudioModePhantom2		0x000006
gotLLXAudioModeSurround2		0x000007
gotLLXAudioModeMonoOnLR		0x000008
gotLLXAudioModeStereoUnknown		0x000009
gotLLXAudioModeDualMono		0x00000a
gotLLXAudioMode_b		0x00000b
gotLLXAudioModePhantom3		0x00000c
gotLLXAudioModeSurround3		0x00000d
gotLLXAudioModePhantom4		0x00000e
gotLLXAudioModeSurround4		0x00000f

3.2.7 LLX Status Audio Status Control

Table 3-9. LLX Status Audio Status Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXStatusAudioStatus	Configure the input data's audio status.	0xc80807
sotLLXAudioStatusMatrixDecoding	Matrix decoding active	0x000001
sotLLXAudioStatusLFE	LFE present at LLX output	0x000002
getLLXStatusAudioStatus	Report the input data's audio status.	0x880807

Table 3-9. LLX Status Audio Status Configuration Symbolic Opcodes

Symbol	Description	Value
gotLLXAudioStatusMatrixDecoding		0x000001
gotLLXAudioStatusLFE		0x000002

3.2.8 LLX Block Control

LLX Block Control is implemented by several registers, including LLX Block Length, LLX Block Stride, LLX Block Buffer and LLX Block Count registers. The available configuration commands are shown in Table 3-10. It is recommended that these commands are not used by the end customer.

Table 3-10. LLX Block Control Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXBlockLength	Set Block Length in LLX.	0xc80808
setLLXBlockStride	Set Block Stride in LLX.	0xc80809
setLLXBlockBuffer	Set Block Buffer in LLX.	0xc8080A
setLLXBlockCount	Set Channel Count of Buffer Block.	0xe22dnn
getLLXBlockLength	Get Block Length in LLX.	0x880808
getLLXBlockStride	Get Block Stride in LLX.	0x880809
getLLXBlockBuffer	Get Block Buffer in LLX.	0x88080A
getLLXBlockCount	Get Channel Count of Buffer Block.	0xa22d00

3.2.9 LLX Input & Output Mode Control

LLX Input & Output Mode is configured by LLX Input Mode and LLX Output Mode registers, respectively, shown in Table 3-11. An LLX reset command (e20400) must be used after configuring the input/output mode.

Table 3-11. LLX Input and Output Mode Control

Symbol	Description	DSP Pin No	Value
setLLXInputMode2Ch	Set Input L/R	SDI0	0xe22e00
setLLXInputMode4Ch	Set Input L/R, Ls/Rs	SDI0, SDI1	0xe22e01
setLLXInputMode6Ch	Set Input L/R, Ls/Rs, C/Sub	SDI0, SDI1, SDI2	0xe22e02
setLLXInputMode8Ch	Set Input L/R, Ls/Rs, C/Sub, La/Ra This mode is only supported on 50-pin DSP package.	SDI0, SDI1, SDI2, SDI0_1	0xe22e03
setLLXOutputMode2Ch	Set Output L/R	SDO0	0xe22f00
setLLXOutputMode4Ch	Set Output L/R, Ls/Rs	SDO0, SDO1	0xe22f01
setLLXOutputMode6Ch	Set Output L/R, Ls/Rs, C/Sub	SDO0, SDO1, SDO2	0xe22f02
setLLXOutputMode8Ch	Set Output L/R, Ls/Rs, C/Sub, La/Ra. This mode is only supported on 80-pin DSP package.	SDO0, SDO1, SDO2, SDO0_1	0xe22f03
getLLXInputMode	Report LLX Input Mode configuration.		0xa22e00

Table 3-11. LLX Input and Output Mode Control (continued)

Symbol	Description	DSP Pin No	Value
gotLLXInputMode2Ch			0x000000
gotLLXInputMode4Ch			0x000001
gotLLXInputMode6Ch			0x000002
gotLLXInputMode8Ch			0x000003
getLLXOutputMode	Report LLX Output Mode configuration.		0xa22f00
gotLLXOutputMode2Ch			0x000000
gotLLXOutputMode4Ch			0x000001
gotLLXOutputMode6Ch			0x000002
gotLLXOutputMode8Ch	The 8Ch mode is only supported on 80-pin DSP package.		0x000003

Table 3-12. LLX ERROR NO Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXERRNO	Set LLX Indication of Error.	0xc8080C
getLLXERRNO	Report LLX Indication of Error.	0x88080C

3.2.10 LLX Feature Control and LLX Aux Output Channel Control

These two registers are used to control LLX Feature and Aux Output Channel. LLX Feature Control is a bit-mapped register, in which every bit has its specific meaning, shown in Table 3-13. The Aux channel output can be configured to select from Lf/Rf, Ls/Rs, C/Sub, La/Ra, as shown in Table 3-14.

Table 3-13. LLX Feature Control Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXFeatureControl	Set LLX Feature Control.	0xe23500
sotLLXFeatureControlSRDetect	Bit0: Sample Rate Detection Feature Enable/Disable	0x000001
sotLLXFeatureControlAuxEnable	Bit1: Auxiliary Input Feature Enable/Disable	0x000002
sotLLXFeatureControlTDMInput	Bit2: TDM Input Driver Enable/Disable	0x000004
sotLLXFeatureControlTDMOutput	Bit3: TDM Output Driver Enable/Disable	0x000008
sotLLXFeatureControlPDCInfoTxGPIO	Bit4: PDC Info Transmit to GPIO Feature Enable/Disable	0x000010
sotLLXFeatureControlPDCInfoRxGPIO	Bit5: PDC Info Receive from GPIO Feature Enable/Disable	0x000020
sotLLXFeatureControlPDCInfoTxZone	Bit6: PDC Info Transmit to Zone Feature Enable/Disable	0x000040
sotLLXFeatureControlPDCInfoRxZone	Bit7: PDC Info Transmit to GPIO Feature Enable/Disable	0x000080
getLLXFeatureControl	Report LLX Feature Control configuration.	0xa23500
gotLLXSampleRateDetectionEnable	Bit0: Sample Rate Detection Feature Enable/Disable	0x000001
gotLLXAuxiliaryInputEnable	Bit1: Auxiliary Input Feature Enable/Disable	0x000002

When the LLX Feature Control Aux function is enabled by ‘sotLLXFeatureControlAuxEnable’, the Aux output can be configured, as shown in Table 3-15.

Table 3-14. LLX Aux Output Channel Control Configuration Symbolic Opcodes

Symbol	Description	Value
setLLXAuxOutputLeftRight	Set Aux output from Left, Right Channel	0xe23600
setLLXAuxOutputLsurRsur	Set Aux output from Ls, Rs Channel	0xe23601
setLLXAuxOutputCenSub	Set Aux output from Center, Subwoofer Channel	0xe23602
setLLXAuxOutputLbackRback	Set Aux output from Lb, Rb Channel	0xe23603
getLLXAuxOutputChannel	Report LLX Aux Output Channel configuration.	0xa23600
gotLLXAuxOutputLeftRight	Aux output from Left, Right Channel	0x000000
gotLLXAuxOutputLsurRsur	Aux output from Ls, Rs Channel	0x000001
gotLLXAuxOutputCenSub	Aux output from Center, Subwoofer Channel	0x000002
gotLLXAuxOutputLbackRback	Aux output from Lb, Rb Channel	0x000003

3.3 Multi-Channel PCM LLX

The multi-channel PCM decoder is equivalent to the natural decoders of the Audio SA to perform initialization, channel processing and data transferring. For audio, it executes scaling and masking; for information, it updates PDC with data in the info buffer (if information is fed from GPIO) or zone (if information is fed from SHI). Multi-Channel PCM is the only decoder (except NG) on DSPB56374; it also supports Auto-Detection, choosing input driver, as well as other functions.

The MPCM LLX provides decoding of PCM bit streams formatted in IEC 61937.

3.3.1 MPCM Audio Mode

MPCM Audio Mode Control Register determines oPDCAudioMode used in post processing when PCM is the source type.

Table 3-15. MPCM Audio Mode Control Symbolic Opcodes

Symbol	Description	Value
setMPCMAudioModeProLogic	LSB in offset word0 of Zone MPCM. Set MPCM audio mode. Select audio mode to use to interpret input.	0xe30c00
setMPCMAudioModeMono		0xe30c01
setMPCMAudioModeStereo		0xe30c02
setMPCMAudioModeStereo3		0xe30c03
setMPCMAudioModePhantom		0xe30c06
setMPCMAudioModeSurround		0xe30c07
setMPCMAudioModePhantom1		0xe30c04
setMPCMAudioModeSurround1		0xe30c05
setMPCMAudioModeMonoOnLR		0xe30c08
setMPCMAudioModeStereoUnknown		0xe30c09
setMPCMAudioModeDualMono		0xe30c0a
setMPCMAudioModePhantom3		0xe30c0c
setMPCMAudioModeSurround3		0xe30c0d
setMPCMAudioModePhantom4		0xe30c0e
setMPCMAudioModeSurround4		0xe30c0f
	Set corresponding audio mode with subwoofer.	0xe30c1X (0…f)

Table 3-15. MPCM Audio Mode Control Symbolic Opcodes (continued)

Symbol	Description	Value
getMPCMAudioMode	Report PCM audio mode	0xa30100
gotMPCMAudioModeProLogic	0/0: 2 front and 0 rear speakers	0x000000
gotMPCMAudioModeMono	1/0: 1 front and 0 rear speakers	0x000001
gotMPCMAudioModeStereo	2/0: 2 front and 0 rear speakers	0x000002
gotMPCMAudioModeStereo3	3/0: 3 front and 0 rear speakers	0x000003
gotMPCMAudioModePhantom1	2/1: 2 front and 1 rear speakers	0x000004
gotMPCMAudioModeSurround1	3/1: 3 front and 1 rear speakers	0x000005
gotMPCMAudioModePhantom	2/2: 2 front and 2 rear speakers	0x000006
gotMPCMAudioModeSurround	3/2: 3 front and 2 rear speakers	0x000007
gotMPCMAudioModeMonoOnLR	1/0: 1 front and 0 rear speakers	0x000008
gotMPCMAudioModeStereoUnknown	2/0: 2 front and 0 rear speakers	0x000009
gotMPCMAudioModeDualMono	2/0: 2 front and 0 rear speakers	0x00000a
gotMPCMAudioMode_b	0: without anything	0x00000b
gotMPCMAudioModePhantom3	2/3: 2 front and 3 rear speakers	0x00000c
gotMPCMAudioModeSurround3	3/3: 3 front and 3 rear speakers	0x00000d
gotMPCMAudioModePhantom4	2/4: 2 front and 4 rear speakers	0x00000e
gotMPCMAudioModeSurround4	3/4: 3 front and 4 rear speakers	0x00000f
gotBitMPCMAudioModeBass	.1: 1 subwoofer	0x000010

3.3.2 MPCM Auto Detection

Auto-detection provides detection for PCM, AC-3, DTS, and AAC. Unsupported bit streams are muted. In order to reduce MIPS, detection is performed only on designated channels, and all channels will be muted if unsupported bit streams are detected. Users are allowed to choose a specific channel upon which the auto-detection is performed, shown in Table 3-16.

Table 3-16. MPCM Auto Detection Control Symbolic Opcodes

Symbol	Description	Value
setMPCMAutoDetectOnLR	Set Auto Detection depend on L/R.	0xe30200
setMPCMAutoDetectOnLsRs	Set Auto Detection depend on Ls/Rs.	0xe30201
setMPCMAutoDetectOnCSubw	Set Auto Detection depend on C/Sub.	0xe30202
setMPCMAutoDetectOnLbRb	Set Auto Detection depend on La/Ra.	0xe30203
getMPCMAutoDetectMode	ISB. Report MPCM Auto Detection Mode.	0xa30200
gotMPCMAutoDetectOnLR		0x000000
gotMPCMAutoDetectOnLsRs		0x000001
gotMPCMAutoDetectOnCSubw		0x000002
gotMPCMAutoDetectOnLbRb		0x000003

3.3.3 MPCM Sample Rate

The DSPB56374 supports sample rate detection for non-sample rate encoded bitstream (PCM) using the ESAI input driver.The LLX sample rate register reports the result of the detected sample rate. The following sample rates at the input are fully supported: 48 kHz, 44.1 kHz, 32 kHz, 96kHz, and 88.2kHz.

PCM sample rate detection requires the information of the DSP working frequency since it utilizes the DSP internal Timer. It is the user's responsibility to input this value to the SA. The value written to the SA should be calculated as follows: Factor=1/DSP core clock.

Suppose the DSP core clock is 180 MHz, the factor=1/180=0.00555555, which is the default value.

Table 3-17. Sample Rate Detection for Non-Encoded Sample Rate Bitstream Symbolic Opcodes

Symbol	Description	Value
setMLXDSPFrequency	Set the reciprocal of exact DSP working frequency (MHz is the unit). Default value is $00b60b(1/180).	0xc8080c
getLLXSampleRate	Report the detected input sample rate	0x880804
gotLLXSampleRate48000Hz		0x000000
gotLLXSampleRate44100Hz		0x000001
gotLLXSampleRate32000Hz		0x000002
gotLLXSampleRate96000Hz		0x000003
gotLLXSampleRate88200Hz		0x000004

3.3.4 MPCM Silence Processing

The MPCM silence processing register determines the silence processing with auto detection in the MPCM decoder.

Table 3-18. MPCM Silence Processing Symbolic Opcodes

Symbol	Description	Value
setMPCMMuteStep	Positive fractional scaling value used for producing 'soft' mute and un-mute to cover noise conditions as determined by PCM LLX; step is implemented at sample rate. Internal limiting is provided to maintain a range of {from 0 to setLLXScale}. The most significant bit (bit23, sign bit) is ignored. The zero-value forces continuous un-mute (PCM LLX only).	0xc80c01
setMPCMAnalogSilenceCoef	Fractional value used as analog level averaging factor. For "analog silence," an average level is calculated and the result is returned. This calculation is maintained independent of block boundaries. Average level is determined by the formula: y(n) = A |x(n)| + (1-A) y(n-1) where averaging factor 'A' (scale value) is the value of AnalogSilenceCoef. Left and right input words are treated as consecutive samples.	0xc80c02
setMPCMSilenceControl	Configure ConfigSilence (LSB), AnalogSilenceLevel (ISB), and DigitalSilencePeriod (MSB) registers.	0xc80c03
setMPCMConfigSilence	This is a bit-mapped register, which uses set (register)+data, for example: setPCMConfigSilence+0x01 (where data = 0x01).	0xe30d00
setMPCMPostDecoderUnmute		0xe30d01
setMCMAutoDetectionReset	Disable the un-mute override (which keeps mute enabled), which is enabled at PCM LLX exit due to bitstream detect automatically reset and causes a "local restart"(PCM LLX does not exit), resetting all auto detection parameters to initial conditions. This flag is checked once per receive block prior to output processing.	0xe30d01

Table 3-18. MPCM Silence Processing Symbolic Opcodes (continued)

Symbol	Description	Value
setMCMMuteAllDecoderExits	Enables muting for suppression of potential noise as PCM LLX is reactivated after exit of any other (compressed bitstream) LLX. The default setting of (0) provides this mute feature only for the case where DTS LLX exits.	0xe30d03
setMPCMAnalogSilenceLevel	This value is translated to a 24-bit fractional analog level by left shifting 8 bits. As such, it is a positive level in the range {$000000... $00ff00}. A zero value disables analog silence detection. A non-zero value determines the analog silence threshold, with an average analog level less than or equal to the resulting value from the left shift generating an analog silence detect.	0xe30e00
setMPCMDigitalSilencePeriod	Use set (register)+data, for example: setPCMDigitalSilencePeriod+0x5e (where data = 0x5e). This value is translated to a 24-bit integer value by left shifting 10 bits. As such, it is a positive value in the range {$000000... $03fc00}. A zero value disables digital silence detection. A non-zero value determines the digital silence threshold, matched against a count of sequential zero value input words (left and right channels words are read alternately in sequence). This provides for a digital silence detect based on sample count. For example, ($01<<10) = $000400 samples' time = 1024 samples/(2 chans*48k samples/sec) ~ 10 ms, ($ff<<10) = $03fc00 samples' time = 261120 samples/(2 chans*48k samples/sec) ~ 2.7 sec. Digital silence detect is set for consecutive zero word count greater than or equal to the resulting value from the left shift.	0xe30f00
setMPCMPDCDoneAck	ISB in offset word4 of Zone MPCM.	0xe312nn
getMPCMMuteStep	Display soft mute/un-mute scaling step per sample.	0x880c01
getMPCMAnalogSilenceCoef	Display coefficient for analog silence calculation.	0x880c02
getMPCMSilenceControl	Display three byte registers for silence detection.	0x880c03
getMPCMConfigSilence	Report MPCM configuration of silence.	0xa30d00
gotMPCMConfigSilenceAutoDetectionReset		0x000001
gotMPCMConfigSilencePostDecoderUnmute		0x000001
gotMPCMConfigSilenceMuteAllDecoderExits		0x000002
getMPCMAnalogSilenceLevel	Report MPCM configuration of analog silence level.	0xa30e00
getMPCMDigitalSilencePeriod	Report MPCM configuration of digital silence period.	0xa30f00
getMPCMPDCDoneAck		0xa312nn

Table 3-19. MPCM Silence Processing Status Symbolic Opcodes

Symbol	Description	Value
getMPCMStatusSilence	This is a bit-mapped register. Silence detection is determined on a sample basis with 'Detected' flags updated every 128 samples.	0xa31100

Table 3-19. MPCM Silence Processing Status Symbolic Opcodes (continued)

gotMPCMStatusSilenceDetectedAnalog	This bit is set (1) by the PCM LLX when it detects analog silence. Otherwise, it is reset (0). This flag is nonfunctional for analog silence disabled (default configuration).	0x000001
gotMPCMStatusSilenceDetectedDigital	This bit is set (1) by the PCM LLX when it detects digital silence. Otherwise, it is reset (0). This flag is nonfunctional for digital silence disabled	0x000002
gotMPCMStatusSilenceNonSilenceOverrid e	NonSilenceOverride bit is set (1) by the PCM LLX when it exits to the MLX due to DTS (PCM) bitstream detection. It is reset (0) when digital silence is detected, AutoDetectionReset flag is set, or InitPCM entry is made. While this bit is set, audio output is muted, suppressing potential noise after exit by DTS (PCM) LLX. This flag is nonfunctional for digital silence disabled.	0x000004
gotMPCMStatusSilencePostSilence	PostSilence bit is set (1) by the PCM LLX when the trailing edge of digital silence is detected, i.e., after digital silence is detected and/or maintained, then non-silence is first detected. After InitAuto entry to PCM LLX, this flag is also set at any of the following: a) termination of digital silence (at SilenceDetectedDigital flag reset), b) end of IEC Pause detected, and c) setPCMAutoDetectionReset command issued./* This flag indicates current non-silence and that the count for un-mute to PCM decoding timeout is active. While this flag is set, audio output is muted. This flag is cleared (0) when continuous non- silence duration exceeds that determined by controlPCMNoDetectUnmutePeriod, digital silence is detected, or InitPCM entry is made. This flag is nonfunctional for digital silence disabled.	0x000008
gotMPCMStatusSilenceRxBufferClear	RxBufferClear bit is set (1) by the PCM LLX when the current receive buffer data contains all zero data values (1 block/channel). A single non-zero data value resets (0) this bit.	0x000010

3.3.5 MPCM Aux Control and MPCM Channel Mask Control

The MPCM Aux control and Channel Mask control are shown in Table 3-20 and Table 3-21, respectively.

Table 3-20. MPCM Aux Control Symbolic Opcodes

Symbol	Description	Value
setMPCMNoDetectUnmutePeriod	LSB. Use set (register)+data, for example: setPCMNoDetectUnmutePeriod+0xb (where data = 0xb).	0xe31500
setMPCMConfigDetect	ISB. This is a bit-mapped register.	0xe31600
setMPCMConfigDetectPreIECZeroDisable	When reset (0), IEC detection requires 'n' zero-value words preceding IEC Preamble; 'n' is determined by PreIECZeroMode flag. When set (1), IEC detection does not require any preceding zero-value words.	0xe31601
setMPCMConfigDetectPreIECZeroMode	When reset (0), IEC detection requires four zero-value words preceding IEC Preamble. When set (1), IEC detection requires two zero-value words preceding IEC Preamble. This bit is effective only for PreIECZeroDisable flag reset (0).	0xe31602
getMPCMAuxControl	Display three aux byte registers	0x880c05

Table 3-20. MPCM Aux Control Symbolic Opcodes (continued)

getMPCMNoDetectUnmutePeriod		0xa31500
getMPCMConfigDetect	This is a bit-mapped register	0xa31600
gotMPCMConfigDetectPreIECZeroDisable		0x000001
gotMPCMConfigDetectPreIECZeroMode		0x000002

Table 3-21. MPCM Channel Mask Control Symbolic Opcodes

Symbol	Description	Value
setMPCMMasking	Configure MPCM channel mask.	0xc80c07
sotMPCMMaskingLeftChannel	This is Mute Mask. Setting '1' means Mute, and '0' means Un-mute.	0x000001
sotMPCMMaskingRightChannel		0x000002
sotMPCMMaskingLsurChannel		0x000004
sotMPCMMaskingRsurChannel		0x000008
sotMPCMMaskingCenterChannel		0x000010
sotMPCMMaskingSubwooferChannel		0x000020
sotMPCMMaskingLbackChannel		0x000040
sotMPCMMaskingRbackChannel		0x000080
getMPCMMasking	Report MPCM channel mask configuration.	0x880c07
gotMPCMMaskingLeftChannel		0x000001
gotMPCMMaskingRightChannel		0x000002
gotMPCMMaskingLsurChannel		0x000004
gotMPCMMaskingRsurChannel		0x000008
gotMPCMMaskingCenterChannel		0x000010
gotMPCMMaskingSubwooferChannel		0x000020
gotMPCMMaskingLbackChannel		0x000040
gotMPCMMaskingRbackChannel		0x000080

3.4 Noise Generator LLX

The Noise Generator LLX provides three signal sources: white noise, pink noise and sine tone, composite operation modes-band pass filter (BPF) and soft mute & un-mute function, and output mode-sequence mode and pause mode.

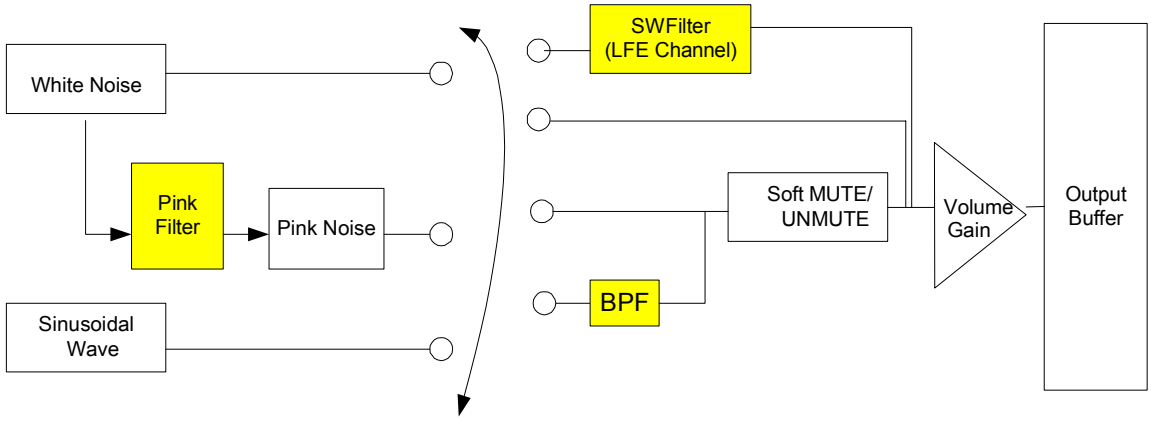


Figure 3-1. Noise Generator LLX Structure

3.4.1 NG Configuration

NG supports three output modes, scanning the channels in sequence, stopping at a channel indefinitely, and altering an output channel in the order chosen. The first is sequence mode selected by Configuration Sequence. Next is pause mode. In pause mode, users can point to the chosen channel via NG Status Register, described below. The final is advance mode whose command is Configuration Advance. Note that the output channels are limited by the current listening mode.

Table 3-22. NG Configuration Symbolic Opcodes

Symbol	Description	Value
setNGConfigNone	Disable NG	0xe28400
setNGConfigSequence	Sequence Mode	0xe28401
setNGConfigPause	Pause Mode	0xe28402
setNGConfigAdvance	Advance Mode	0xe28403
getNGConfig	Report configuration register value	0x880a01

3.4.2 NG Status

NG Status Register has two usages in DSPB56374 system. One is to report the current output channel, and the other is to point the output channel in pause mode.

Table 3-23. NG Status Symbolic Opcodes

Symbol	Description	Value
getNGStatus	Report status register value	0x880a00
setNGStatusLeft	Point the output channel in pause mode.	0xe28000
setNGStatusRght		0xe28001
setNGStatusLSur		0xe28002
setNGStatusRSur		0xe28003
setNGStatusCntr		0xe28004
setNGStatusSubw		0xe28005
setNGStatusLAux		0xe28006
setNGStatusRAux		0xe28007
setNGStatusNone		0xe28008

3.4.3 NG Flag

NG provides three generators: white noise, pink noise and sine tone; and two operation modes: BPF and soft mute & un-mute. Users can switch the different composite modes in NG Flag Register shown in Table 3-24.

Table 3-24. NG Flag Symbolic Opcodes

Symbol	Description	Value
setNGFlag	Set flag register value	0xe28800
sotBitNGFlagWhiteNoise	The corresponding generator or operation mode. The detailed setting refers to Table 3-26.	0x000040
sotBitNGFlagPinkNoise		0x000020
sotBitNGFlagSineTone		0x000010
sotBitNGFlagBPF		0x000004
sotBitNGFlagMuteUnMute		0x000002
sotBitNGFlagSameTime		0x000001
sotBitNGFlagSwfLPF		0x000008
getNGFlag	Report flag register value	0x880a02

Table 3-25. NG Composite Mode

Command for Generator	Command for Operation Mode	White Noise	Pink Noise	Sine Tone	BPF	Mute and Un-mute	Mute and Un-mute at the same time
1	1	OFF	OFF	ON	OFF	OFF	OFF
2	1	OFF	ON	OFF	OFF	OFF	OFF
4	1	ON	OFF	OFF	OFF	OFF	OFF
1	2	OFF	OFF	ON	OFF	ON	OFF
2	2	OFF	ON	OFF	OFF	ON	OFF
4	2	ON	OFF	OFF	OFF	ON	OFF
1	3	OFF	OFF	ON	OFF	ON	ON
2	3	OFF	ON	OFF	OFF	ON	ON
4	3	ON	OFF	OFF	OFF	ON	ON
1	4	OFF	OFF	ON	ON	ON	OFF
2	4	OFF	ON	OFF	ON	ON	OFF
4	4	ON	OFF	OFF	ON	ON	OFF
1	5	OFF	OFF	ON	ON	ON	ON
2	5	OFF	ON	OFF	ON	ON	ON
4	5	ON	OFF	OFF	ON	ON	ON
1	6	OFF	OFF	ON	ON	ON	OFF
2	6	OFF	ON	OFF	ON	ON	OFF
4	6	ON	OFF	OFF	ON	ON	OFF
1	7	OFF	OFF	ON	ON	ON	ON

Table 3-25. NG Composite Mode (continued)

2	7	OFF	ON	OFF	ON	ON	ON
4	7	ON	OFF	OFF	ON	ON	ON

Table 3-26. NG Flag Symbolic Opcodes

Symbol	Description	Value
setNGFlag	Set flag register value.	0xe28900
sotBitNGFlagWhiteNoise	The corresponding Generator or Operation Mode command. Refer to Table 3-25.	0x000040
sotBitNGFlagPinkNoise		0x000020
sotBitNGFlagSineTone		0x000010
sotBitNGFlagBPF		0x000004
sotBitNGFlagMuteUnMute		0x000002
sotBitNGFlagSameTime		0x000001
sotBitNGFlagSwfLPF		0x000008
getNGFlag	Report flag register value.	0x880a02

3.4.4 NG Pink Filter

NG Pink Filter Register is a pointer to call a coefficient table for the filter function entrance, which alters white noise to pink noise. By placing a new filter function entrance in the register, users can take advantage of their own algorithm.

Table 3-27. NG Configuration Symbolic Opcodes

Symbol	Description	Value
setNGFilter	Set pink filter register value	0xC80a03
getNGFilter	Report pink filter register value	0x880a03

3.4.5 NG Time Duration

NG Time Duration Register stipulates the time used in sequence mode, that is, it tells the system how long the output channel should be on before switching. The accounting unit is 0.116 µS per count.

Table 3-28. NG Time Duration Symbolic Opcodes

Symbol	Description	Value
setNGTimeDuration	Set time duration register value	0xC80a04
getNGTimeDuration	Report time duration register value	0x880a04

3.4.6 NG Sine Frequency

Choosing sine tone generator, users transform the signal frequency into the data needed by the DSPB56374 system according to the following equation.

$$NGSwgSinW = \sin\left(\frac{2\pi f}{f_s}\right)$$

$$NGSwgSinW = \sin\left(\frac{2\pi f}{f_s}\right)$$

In the equation, f is signal frequency and f_s is the sampling frequency. Note that the couple should be changed at the same time. Users are requested to give the preferable frequency before running the sine tone generator.

Table 3-29. NG Sine Frequency Symbolic Opcodes

Symbol	Description	Value
SetNGSwgSinW1	Set sine frequency register value	0xc80a05
SetNGSwgCosW1		0xc80a06
GetNGSwgSinW1	Report sine frequency register value	0x880a05
GetNGSwgCosW1		0x880a06

3.4.7 NG Mute & Un-mute Step

NG Mute & Un-mute Step Register is to manage the mute & un-mute time.

Table 3-30. NG Mute & Un-mute Symbolic Opcodes

Symbol	Description	Value
setNGMuteStep	Set mute & un-mute step register value	0xc80a07
setNGUnMuteStep		0xc80a08
getNGMuteStep	Report mute & un-mute step register value	0x880a07
getNGUnMuteStep		0x880a08

Chapter 4
Dual Chip

The DSPB56374 supports a dual chip mode.

4.1 Introduction

The Dual Chip Solution for the DSPB56374 will enable application software that runs on a single chip to be executed by two chips. One chip will focus on decoders and the other chip will focus on PPPs. The Dual Chip Solution provides the necessary MIPS as well as memory resources for a customer when a single chip solution doesn't meet their requirement.

4.2 Dual Chip Solution High Level Design

4.2.1 Overview

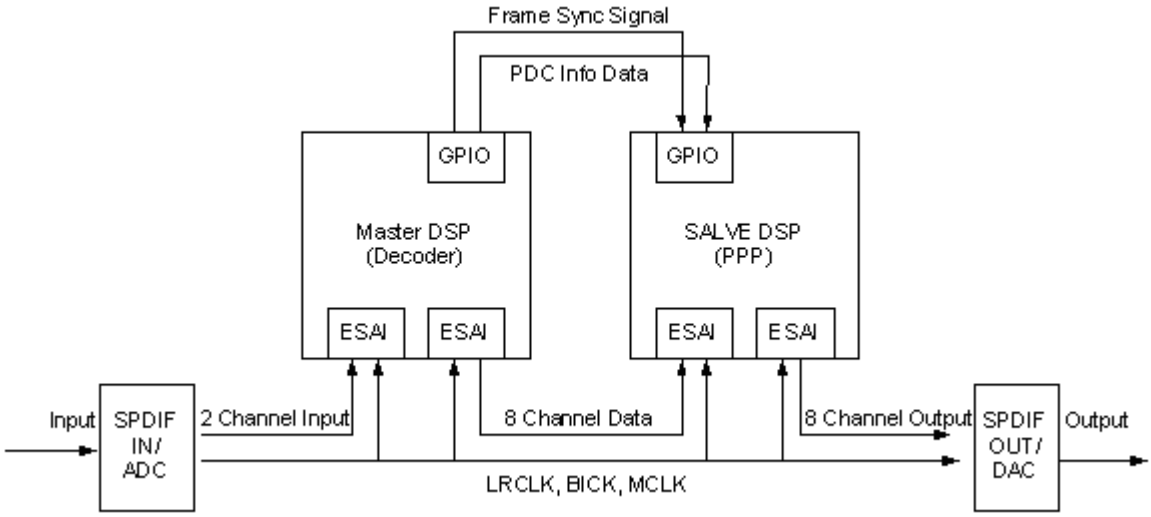


Figure 4-1. Dual Chip Solution

The dual chip solution allows the Audio SA system to be performed by two chips: one chip named the master DSP is focused on decoding as well as some small PPP; the other chip named slave DSP is for additional PPP processing. The DSPB56376 is most suitable as the slave DSP, as it has only one decoder, MPCM, and the various PPPs.

In total, 8 channels of data will be transferred from master DSP to the slave DSP via ESAI interface. In addition, some information (PDC info) generated by the master DSP will be needed by the slave DSP. It is transferred through the GPIO pins.

4.2.2 Dual Chip Configuration and Status Control

In a Dual Chip system, the information (Info) needs to be transferred from master chip to slave chip. The Info contents include VOR, oPDCAudioMode, oPDCAudioStatus, oPDCDecoderType and oPDCSampleRate. Through the Info transfer, the Post Processing Chain in the master chip is extended to the slave chip. With this structure, the PPP will work seamlessly in a dual chip system. In detail, the Info transfer has two methods, GPIO type or Zone type. If the Info is transferred by GPIO pin, it is called GPIO type. If the Info is transferred by uC, it is called Zone type, for that the uC will get the master chip Info in specified memory and transfer it to the slave chip.

The configuration opcodes of these two modes are shown in Table 4-1. When info transmit mode is set to send information to Zone instead of to the GPIO pin on master chip, the user can get information from InfoTxZone, such as InfoTxVOR0~7, TxAudioMode, TxAudioStatus, TxDecoderType and TxSampleRate. When info receive mode is set to get information from Zone instead of from GPIO pin on slave chip, the user can feed information to InfoRxZone, such as InfoRxVOR0~7, RxAudioMode, RxAudioStatus, RxDecoderType and RxSampleRate.

Table 4-1. Dual Chip Configuration Control Symbolic Opcodes

Symbol	Description	Value
setMasterChipSendInfoToGPIOPIN	Set Info Transmit by GPIO pin on Master Chip.	0xe23511 0xe20400
setSalveChipGetInfoFromGPIOPIN	Set Info Receive by GPIO pin on Slave Chip.	0xe23520 0xe20400
setMasterChipSendInfoToZone	Set Info Transmit by Zone on Master Chip.	0xe23541 0xe20400
getInfoTxVOR0	Get VOR0 ~ VOR 7 registers	0x880c14
getInfoTxVOR1		0x880c15
getInfoTxVOR2		0x880c16
getInfoTxVOR3		0x880c17
getInfoTxVOR4		0x880c18
getInfoTxVOR5		0x880c19
getInfoTxVOR6		0x880c1a
getInfoTxVOR7		0x880c1b
getInfoTxAudioMode	Get Audio Mode in InfoTxZone	0x880c1c
getInfoTxAudioStatus	Get Audio Status in InfoTxZone	0x880c1d
getInfoTxDecoderType	Get Decoder Type in InfoTxZone	0x880c1e
getInfoTxSampleRate	Get Sample Rate in InfoTxZone	0x880c1f
setSalveChipGetInfoFromZone	Set Info Receive by Zone on Slave Chip.	0xe23580 0xe20400
setInfoRxVOR0	Set VOR0 ~ VOR 7 registers	0xc80c08
setInfoRxVOR1		0xc80c09
setInfoRxVOR2		0xc80c0a
setInfoRxVOR3		0xc80c0b
setInfoRxVOR4		0xc80c0c
setInfoRxVOR5		0xc80c0d
setInfoRxVOR6		0xc80c0e
setInfoRxVOR7		0xc80c0f
setInfoRxAudioMode	Get Audio Mode in InfoTxZone	0xc80c10
setInfoRxAudioStatus	Get Audio Status in InfoTxZone	0xc80c11
setInfoRxDecoderType	Get Decoder Type in InfoTxZone	0xc80c12
setInfoRxSampleRate	Get Sample Rate in InfoTxZone	0xc80c13

Chapter 5
Bootstrap Modes

The DSPB56374 provides 16 bootstrap modes. All modes are reserved except the ones noted here. The following boot modes are supported:

- Mode 2 jump to ROM with initSPI
- Mode 5 boot via SPI (slave)
- Mode 6 boot via I2C with filter (slave)
- Mode 7 boot via I2C without filter (slave)
- Mode 9 boot via I2C serial EEPROM with filter (master)
- Mode B boot via SPI serial EEPROM (master)
- Mode C boot via GPIO serial SPI EEPROM
- Mode D jump to ROM with initDefaultHLX
- Mode E jump to ROM with initI2C (Chirp I2C mode)
- Mode F jump to ROM with initI2CP

Note that other memory sizes are available in the above families. (More information can be found in the DSP56374 Users Guide.)

Since each type of serial EEPROM has its own instructions, only the following devices are supported.

AT25256 256K bit SPI bus serial EEPROM from ATMEL

M95256 256K bit SPI bus serial EEPROM from ST

AT24C256 256K bit I2C bus serial EEPROM from ATMEL

M24256 256K bit I2C bus serial EEPROM from ST

Chapter 6
Post- Processing Phase

6.1 Overview

The Post Processing Chain is the part of the software architecture designed to process audio data, which has been decoded and placed in the output buffer. The Post Processing Chain handles multiple independently controlled audio processing blocks. Each block passes through program control so that it may process decoded audio data in the output buffer. The Post Processing Chain is a collection of serially executed Post Processing Phases. A PPP is implemented through a set of subroutines to enable a unique audio processing feature like bass management or volume control.

In the DSPB56374, many PPPs reside in the ROM, while providung the same flexibility as a custom PPP. These PPPs include some standard PPP of the DSPA56371, which keep the same control interfaces. Meanwhile, these PPP can be relocated and their host slots can be changed, as well.

The DSPB56374 provides a total of 35 slots for PPPs.

Post Processing Phases – Via the Slot. The PPC Block is the PPP described as Slot*X*, where X is a number. The Slot provides a shell from which RAM based software could be loaded and run, and it does not perform audio processing, but rather it is software to enable custom software to be added to the PPC. The Slot PPP is what enables an independent software developer to produce PPP described in this document. Several copies of the slot are implemented throughout the PPC to provide a scaleable configuration of PPP. The Slot is initialized to disable by default setting. Through initialization and activation technique, PPP software can be added.

Each Slot has been allocated its own zone from which standard commands can be issued. Standard Zone Table provides an indirect table to allow standard command mapping through CHIRP. This feature is particularly important for a PPP developer who wants to install the specific custom PPP in a slot.

Currently, available Freescale Semiconductor (formerly Motorola) PPPs for use in the Software Architecture DSPB56374 include the following:

- De-emphasis and DC-Cut
- Loudness
- Compression
- Compression Dynamic Range Control
- Parameter EQ
- Graphic EQ
- Speaker Compensation
- Bass-Boost
- Bass-Treble
- Pause-Detection
- Spectrum Analyzer
- Tone Control
- Fade Balance
- Pre-scaler
- Level Meter
- Beep
- Chime
- Volume Manager
- Digital Gain Manager
- General Delay Manager

Only the gain manager and volume manager PPP are enabled automatically. Each PPP can be loaded into any available slot and provides the option of supporting additional sample rates or filter coefficients loaded either in static mode via boot load process or dynamically via a micro-controller. In addition, the PPC Block and data structures are re-locatable**.**

It is shown in Table 6-1 through Table 6-4, the standard zone mappings to the Standard PPP and its Slot for Red/Blue/Green/Orange HLX.

Table 6-1. PPP slots for Red HLX

Slot	PPP	Index (Dec)	Zone	Notes
0	Empty Slot	N/A	N/A	$C81802+EPPC of Custom PPP To such free slot, the user can use chirp command, in 'PPP' column, to add the custom PPP. Refer to the following example 3.
1	Empty Slot	N/A	N/A	$C81805
2	Empty Slot	N/A	N/A	$C81808
3	Empty Slot	N/A	N/A	$C8180b
4	Empty Slot	N/A	N/A	$C8180e
5	Empty Slot	N/A	N/A	$C81811
6	Empty Slot	N/A	N/A	$C81814
7	Empty Slot	N/A	N/A	$C81817
8	Empty Slot	N/A	N/A	$C8181a
9	Empty Slot	N/A	N/A	$C8181d
10	Empty Slot	N/A	N/A	$C81820
11	Empty Slot	N/A	N/A	$C81823
12	Empty Slot	N/A	N/A	$C81826
13	Empty Slot	N/A	N/A	$C81829
14	Empty Slot	N/A	N/A	$C8182c
15	Empty Slot	N/A	N/A	$C8182f
16	Empty Slot	N/A	N/A	$C81832
17	Empty Slot	N/A	N/A	$C81835
18	Empty Slot	N/A	N/A	$C81838
19	Empty Slot	N/A	N/A	$C8183b
20	Empty Slot	N/A	N/A	$C8183e
21	Empty Slot	N/A	N/A	$C81841
22	Empty Slot	N/A	N/A	$C81844
23	Empty Slot	N/A	N/A	$C81847
24	Empty Slot	N/A	N/A	$C8184a
25	Empty Slot	N/A	N/A	$C8184d
26	Empty Slot	N/A	N/A	$C81850
27	Empty Slot	N/A	N/A	$C81853
28	Empty Slot	N/A	N/A	$C81856
29	Empty Slot	N/A	N/A	$C81859
30	Volume Manager	1	$2D	
31	Gain Manager	2	$2E	
32	Empty Slot	N/A	N/A	$C81862

Table 6-1. PPP slots for Red HLX (continued)

Slot	PPP	Index (Dec)	Zone	Notes
33	Empty Slot	N/A	N/A	$C81865
34	Empty Slot	N/A	N/A	$C81868
35	Empty Slot	N/A	N/A	$C8186b
36	Empty Slot	N/A	N/A	$C8186e
37	Empty Slot	N/A	N/A	$C81871
38	Empty Slot	N/A	N/A	$C81874
39	Empty Slot	N/A	N/A	$C81877

Table 6-2. PPP slots for Blue HLX

Slot	PPP	Index (Dec)	Zone	Notes
0	Empty Slot	N/A	N/A	$C81802+EPPC of Custom PPP To such free slot, the user can use chirp command, in 'PPP' column, to add the custom PPP. Refer to the following example 3.
1	Empty Slot	N/A	N/A	$C81805
2	De-emphasis & DC-Cut	7	$34	
3	Loudness	14	$24	
4	Compression DRC	16	$21	
5	Compression	15	$1F	
6	Empty Slot	N/A	N/A	$C81814
7	Empty Slot	N/A	N/A	$C81817
8	Empty Slot	N/A	N/A	$C8181a
9	Empty Slot	N/A	N/A	$C8181d
10	Empty Slot	N/A	N/A	$C81820
11	Empty Slot	N/A	N/A	$C81823
12	Empty Slot	N/A	N/A	$C81826
13	Empty Slot	N/A	N/A	$C81829
14	Tone Control	17	$1B	
15	Bass Treble	12	$25	
16	Graphic EQ	9	$29	
17	Parametric EQ	8	$2A	
18	Fade Balance	19	$3F	
19	Prescaler	20	$1C	
20	Empty Slot	N/A	N/A	$C8183e
21	Empty Slot	N/A	N/A	$C81841

Table 6-2. PPP slots for Blue HLX (continued)

Slot	PPP	Index (Dec)	Zone	Notes
22	Empty Slot	N/A	N/A	$C81844
23	Empty Slot	N/A	N/A	$C81847
24	Empty Slot	N/A	N/A	$C8184a
25	Empty Slot	N/A	N/A	$C8184d
26	Empty Slot	N/A	N/A	$C81850
27	Bass Boost	11	$26	
28	Speaker Compensation	10	$28	
29	DLM	4	$2C	
30	Volume	5	$2D	
31	Gain	6	$2E	
32	Level Meter	21	$40	
33	Spectrum Analyzer	18	$20	
34	Empty Slot	N/A	N/A	$C81868
35	Empty Slot	N/A	N/A	$C8186b
36	Empty Slot	N/A	N/A	$C8186e
37	Empty Slot	N/A	N/A	$C81871
38	Empty Slot	N/A	N/A	$C81874
39	Empty Slot	N/A	N/A	$C81877

Table 6-3. PPP slots for Green HLX

Slot	PPP	Index (Dec)	Zone	Notes
0	Empty Slot	N/A	N/A	$C81802+EPPC of Custom PPP To such free slot, the user can use chirp command, in 'PPP' column, to add the custom PPP. Refer to the following example 3.
1	Pause Detector	23	$41	
2	De-emphasis & DC-Cut	7	$34	
3	Loudness	16	$24	
4	Compression DRC	18	$21	
5	Compression	17	$1F	
6	Empty Slot	N/A	N/A	$C81814
7	Empty Slot	N/A	N/A	$C81817
8	Empty Slot	N/A	N/A	$C8181a
9	Empty Slot	N/A	N/A	$C8181d

Table 6-3. PPP slots for Green HLX (continued)

Slot	PPP	Index (Dec)	Zone	Notes
10	Empty Slot	N/A	N/A	$C81820
11	Empty Slot	N/A	N/A	$C81823
12	Empty Slot	N/A	N/A	$C81826
13	Empty Slot	N/A	N/A	$C81829
14	Tone Control	19	$1B	
15	Bass Treble	14	$25	
16	Graphic EQ	11	$29	
17	Fade Balance	21	$3F	
18	Prescaler	22	$1C	
19	Empty Slot	N/A	N/A	$C8183b
20	Empty Slot	N/A	N/A	$C8183e
21	Empty Slot	N/A	N/A	$C81841
22	Empty Slot	N/A	N/A	$C81844
23	Empty Slot	N/A	N/A	$C81847
24	Empty Slot	N/A	N/A	$C8184a
25	Parametric EQ	10	$2A	
26	Bass Boost	13	$26	
27	Speaker Compensation	12	$28	
28	DLM	4	$2C	
29	Volume	5	$2D	
30	Gain	6	$2E	
31	Level Meter	24	$40	
32	Spectrum Analyzer	20	$20	
33	Beep	8	$2F	
34	Chime	9	$2B	
35	Empty Slot	N/A	N/A	$C8186b
36	Empty Slot	N/A	N/A	$C8186e
37	Empty Slot	N/A	N/A	$C81871
38	Empty Slot	N/A	N/A	$C81874
39	Empty Slot	N/A	N/A	$C81877

Table 6-4. PPP slots for Orange HLX

Slot	PPP	Index (Dec)	Zone	Notes
0	Empty Slot	N/A	N/A	$C81802+EPPC of Custom PPP To such free slot, the user can use chirp command, in 'PPP' column, to add the custom PPP. Refer to the following example 3.
1	Empty Slot	N/A	N/A	$C81805
2	Empty Slot	N/A	N/A	$C81808
3	Loudness	11	$24	
4	Compression Dynamic Range Control	13	$21	
5	Compression	12	$1F	
6	Empty Slot	N/A	N/A	$C81814
7	Empty Slot	N/A	N/A	$C81817
8	Empty Slot	N/A	N/A	$C8181a
9	Empty Slot	N/A	N/A	$C8181d
10	Empty Slot	N/A	N/A	$C81820
11	Empty Slot	N/A	N/A	$C81823
12	Empty Slot	N/A	N/A	$C81826
13	Empty Slot	N/A	N/A	$C81829
14	Empty Slot	N/A	N/A	$C8182c
15	Empty Slot	N/A	N/A	$C8182f
16	Empty Slot	N/A	N/A	$C81832
17	Empty Slot	N/A	N/A	$C81835
18	Empty Slot	N/A	N/A	$C81838
19	Empty Slot	N/A	N/A	$C8183b
20	Empty Slot	N/A	N/A	$C8183e
21	Empty Slot	N/A	N/A	$C81841
22	Empty Slot	N/A	N/A	$C81844
23	Empty Slot	N/A	N/A	$C81847
24	Empty Slot	N/A	N/A	$C8184a
25	Parametric EQ	7	$2A	
26	Bass Boost	9	$26	
27	Speaker Compensation	8	$28	
28	DLM	4	$2C	
29	Volume	5	$2D	
30	Gain	6	$2E	

Table 6-4. PPP slots for Orange HLX (continued)

Slot	PPP	Index (Dec)	Zone	Notes
31	Empty Slot	N/A	N/A	$C8185f
32	Empty Slot	N/A	N/A	$C81862
33	Empty Slot	N/A	N/A	$C81865
34	Empty Slot	N/A	N/A	$C81868
35	Empty Slot	N/A	N/A	$C8186b
36	Empty Slot	N/A	N/A	$C8186e
37	Empty Slot	N/A	N/A	$C81871
38	Empty Slot	N/A	N/A	$C81874
39	Empty Slot	N/A	N/A	$C81877

The DSPB56374 provides a PPP Executive Chain, which is 3*N words table in RAM. Three words create a group, the first word represents the corresponding Slot Status, and the second is init index while the third word is filled with EPPC pointer.

With the PPP Executive Chain, the PPP's slot and EPPC can be relocated easily by Chirp Command in DSPB56374. In order to remove/add a PPP to a slot, the PPP Executive Chain is put to Zone 18. The following chirp commands are to control slot N.

cmd $c818XX ; XX = 3*N , this register means status.

cmd $c818YY; YY = 3*N+1, this is to set init index.

cmd $c818ZZ ; ZZ = 3*N+2, this is to control EPPC Pointer register.

6.1.1 Install New Custom PPP

IThe following teps can be used to install a custom PPP:

Step1: Download the custom PPP;

Step2: Fill the EPPC address into the specific slot in Executive Chain with command '$c818ZZ'. The detailed chirp command refer to Table 6-1through Table 6-4.

For example:

Load custom PPP in slot10 in Green HLX. Its EPPC is $xxxxxx. The procedure is:

1. Send command 'ldc PPP.cld' to load the cld file of PPP;
2. Send command '$c81820 $xxxxxx' to put the PPP into slot10;
3. Send command '$c81820 $0' to remove the PPP from slot10;

6.1.2 Remove the PPP

To remove a PPP from a slot, the EPPC word must be cleared in the Executive Chain.

For example:

Remove Loudness PPP in Green HLX. The procedure is:

1. Send command '$c8180b $0' to remove Loudness from slot3;

6.1.3 Change Slot and Memory

This operation is mostly used with the existing PPPs in DSPB56374. There are two types of slot changes; slot change with memory change and slot change without memory change.

1. Slot change with memory change. Follow steps:

   Step1: Fill the PPP index into the new slot in Executive Chain with command '$c818YY';

   Step2: Clear EPPC word in the old slot in Executive Chain;

   Step3: Fill the new PPP EPPC address into the new slot in Executive Chain with command '$c818ZZ',

Note: Note: the bit23 of new EPPC word must be set;

Step4: Call initPPL;

For example:

Change Level Meter PPP's slot31 (in Green HLX) to slot1, EPPC in Green HLX from old address '$B30' to new address '$c100', the changing procedure is:

a) Send command '$c81804 $1f' to configure the Init index as '1';
b) Send command '$c8185f $0' to clear the EPPC word in slot31;
c) Send command '$c81805 $80c100' to update the EPPC in slot1 as '$c100';
d) Send command '$c40002 $48 $FF1685 $400000' to call InitPPL.

2. Slot change without memory change. Follow steps:

Step1: Fill the PPP index into the new slot in Executive Chain with command '$c818YY';

Step2: Clear EPPC word in the old slot in Executive Chain;

Step3: Fill the old PPP EPPC address into the new slot in Executive Chain with command '$c818ZZ'.

For example:

Change Level Meter PPP slot31 (in Green HLX) to slot1, the old EPPC is $1000, the changing procedure is:

1. Send command '$c81804 $1f' to configure the Init index as '1';
2. Send command '$c8185f $0' to clear the EPPC word in slot31;
3. Send command '$c81805 $1000' to update the EPPC in slot1 as '$1000';

6.2 General Delay Manager

The Delay Post-Processing Phase or Delay Manager provides the capabilities required to implement delay control in a standard manner for multi-channel data within the Executive Programming Environment.

6.2.1 Delay Manager Status

The Delay Manager Status Register reports the active channel count through the delay manager.

Table 6-5. Delay Manager Status Symbolic Opcodes

Symbol	Description	Value
getDLMStatus	Report status register value.	0x882b00

6.2.2 Delay Manager Configuration

Delay Manager Configuration Register is set with six modes: Milliseconds and Half-milliseconds, belonging to time; Inches, Feet, Centimeters and Meters, in the field of distance. Users can choose the convenient mode then give the system the corresponding delay values for different channels in the Delay Value Register.

For example: Centimeter Mode.

In Figure 6-1, only the right channel value is set. The value represents the distance the speakers are from the listener. For this configuration, a 15ms Delay is added to all except the right channel.

Use the following Formula to figure out the delay:

Delay = Max delay value – Set delay value

L = 516 – 0 (15msec), R = 516 – 516 (0msec), C = 516 – 0 (15msec)

Ls = 516- 0 (15msec), Rs = 516 – 0 (15msec)

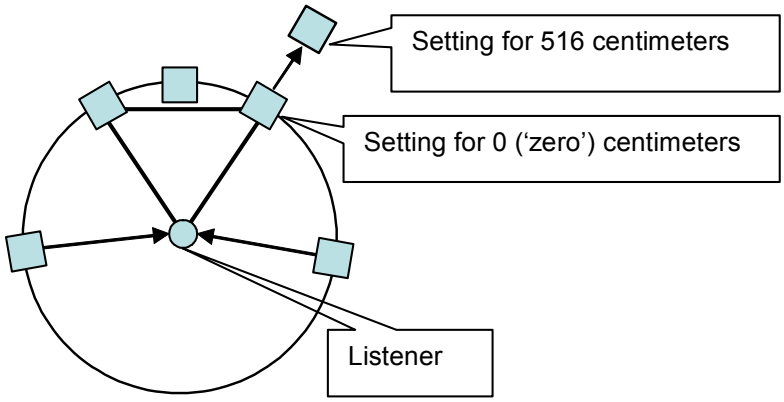


Figure 6-1. Centimeter Mode in Delay Manager

Table 6-6. Delay Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setDLMConfigDisable	Disable delay manager	0xeac400
setDLMConfigMilliseconds	Milliseconds mode	0xeac401
setDLMConfigMilliseconds2	Half-milliseconds mode	0xeac402
setDLMConfigInches	Inches mode	0xeac403
setDLMConfigFeet	Feet mode	0xeac404
setDLMConfigCentimeters	Centimeters mode	0xeac405
setDLMConfigMeters	Meters mode	0xeac406
setDLMConfigNoInitDisable	The following commands perform the same action as the above set, however, they do not initialize the delay buffers.	0xeac500
setDLMConfigNoInitMilliseconds		0xeac501
setDLMConfigNoInitMilliseconds2		0xeac502
setDLMConfigNoInitInches		0xeac503
setDLMConfigNoInitFeet		0xeac504
setDLMConfigNoInitCentimeters		0xeac505
setDLMConfigNoInitMeters		0xeac506
getDLMConfig	Report configuration register value.	0x882b01

6.2.3 Delay Value Register

Table 6-7. Delay Value Register Symbolic Opcodes

Symbol	Description	Value
setDLMDelayLeft	Set delay values of the corresponding channels according to ‘time’ modes.	0xc82b03
setDLMDelayRght		0xc82b04
setDLMDelayLSur		0xc82b05
setDLMDelayRSur		0xc82b06
setDLMDelayCntr		0xc82b07
setDLMDelaySubw		0xc82b08
setDLMDelayLAux		0xc82b09
setDLMDelayRAux		0xc82b0a
setDLMDelayLSec		0xc82b0b
setDLMDelayRSec		0xc82b0c
setDLMSpeakerLocationLeft	Set delay values of the corresponding channels according to ‘distance’ modes.	0xc82b03
setDLMSpeakerLocationRght		0xc82b04
setDLMSpeakerLocationLSur		0xc82b05
setDLMSpeakerLocationRSur		0xc82b06
setDLMSpeakerLocationCntr		0xc82b07
setDLMSpeakerLocationSubw		0xc82b08
setDLMSpeakerLocationLAux		0xc82b09
setDLMSpeakerLocationRAux		0xc82b0a
setDLMSpeakerLocationLSec		0xc82b0b
setDLMSpeakerLocationRSec		0xc82b0c
getDLMDelayLeft	Report the delay values of the corresponding channels.	0x882b03
getDLMDelayRght		0x882b04
getDLMDelayLSur		0x882b05
getDLMDelayRSur		0x882b06
getDLMDelayCntr		0x882b07
getDLMDelaySubw		0x882b08
getDLMDelayLAux		0x882b09
getDLMDelayRAux		0x882b0a
getDLMDelayLSec		0x882b0b
getDLMDelayRSec		0x882b0c

6.3 Gain Manager

The Gain Post-Processing Phase (Gain PPP) provides the capabilities required to implement digital gain in a standard manner for multi-channel data within the Executive Programming Environment. In conjunction with compatible operation of the Digital Volume Control Method Post-Processing Function, the Gain PPP provides an implementation of volume control as shown in Figure 6-2.

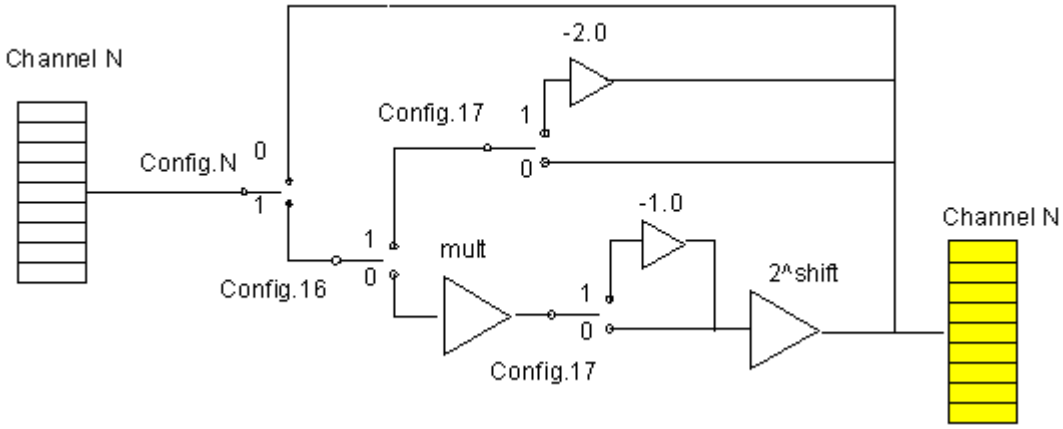


Figure 6-2. Gain Manager Structure

Config. N Corresponding with channel N

0 means channel N is masked

1 means channel N i s active

Config. 16 Bypass flag

0 means bypass flag is cleared

1 means bypass flag is set

Config. 17 Invert flag

0 means invert flag is cleared

1 means invert flag is set

6.3.1 Gain Manager Status

Table 6-8. Gain Manager Status Symbolic Opcodes

Symbol	Description	Value
getGMStatus	Report status register value.	0x882d00
gotGMStatusOkay	Result is okay	0x000000
gotGMStatusOverflow	Overflow in the computation	0x400000

6.3.2 Gain Manager Configuration

Table 6-9. Gain Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setGMConfig	Set all of bits 23-0. Bit 17: Inversion flag - invert output. Bit 16: Bypass flag - don't apply gains Bits 15-0: Channel mask	0xc82d01
setGMConfigFlagNone	Clear both bypass and invert flag	0xeb4700
setGMConfigFlagBypass	Set bypass flag	0xeb4701
setGMConfigFlagInvert	Set Invert flag	0xeb4702
setGMConfigFlagAll	Set both bypass and invert flag	0xeb4703
getGMConfig	Report configuration register value	0x882d01
getGMConfigMask	Report configuration channel mask	0xab4500
getGMConfigFlag	Report configuration control flag status	0xab4700

6.3.3 Gain Manager Coefficient Register

If Gain Manager is not bypassed and not automatically controlled by the Volume Manager, as is the case with the Digital Volume Control Method, the exponent and mantissa of each channel can be set separately to realize origin adjustment. The gain is represented by the exponent-mantissa pair E, M is M*2^(E+1). Note that the values of E and M have a scope of [-2, 2].

Table 6-10. Gain Manager Coefficient Register Symbolic Opcodes

Symbol	Description	Value
setGMGainLeftExponent	Set the exponent and mantissa for the corresponding channel	0xc82d02
setGMGainLeftMantissa		0xc82d03
setGMGainRghtExponent		0xc82d04
setGMGainRghtMantissa		0xc82d05
setGMGainLSurExponent		0xc82d06
setGMGainLSurMantissa		0xc82d07
setGMGainRSurExponent		0xc82d08
setGMGainRSurMantissa		0xc82d09
setGMGainCntrExponent		0xc82d0a
setGMGainCntrMantissa		0xc82d0b
setGMGainSubwExponent		0xc82d0c
setGMGainSubwMantissa		0xc82d0d
setGMGainLAuxExponent		0xc82d0e
setGMGainLAuxMantissa		0xc82d0f
setGMGainRAuxExponent		0xc82d10
setGMGainRAuxMantissa		0xc82d11
setGMGainLSecExponent		0xc82d12
setGMGainLSecMantissa		0xc82d13
setGMGainRSecExponent		0xc82d14
setGMGainRSecMantissa		0xc82d15
getGMGainLeftExponent	Report the exponent and mantissa for the corresponding channel	0x882d02
getGMGainLeftMantissa		0x882d03
getGMGainRghtExponent		0x882d04
getGMGainRghtMantissa		0x882d05
getGMGainLSurExponent		0x882d06
getGMGainLSurMantissa		0x882d07
getGMGainRSurExponent		0x882d08
getGMGainRSurMantissa		0x882d09
getGMGainCntrExponent		0x882d0a
getGMGainCntrMantissa		0x882d0b
getGMGainSubwExponent		0x882d0c
getGMGainSubwMantissa		0x882d0d
getGMGainLAuxExponent		0x882d0e
getGMGainLAuxMantissa		0x882d0f
getGMGainRAuxExponent		0x882d10
getGMGainRAuxMantissa		0x882d11

6.4 Volume Manager

The Volume Post-Processing Phase or Volume Manager provides the capabilities required to implement volume control in a standard manner for multi-channel data within the Executive Programming Environment. As shown in Figure 6-3, volume control components in High Level Executive, decoders in Low Level, PPP as well as Volume Control Method Post-Processing composite Volume Manager.

The Volume Manager provides a mechanism to attach a scale factor or size to the 24-bit fixed-point field of bits that are used to represent the audio data within the data buffers. The scale factor is not applied to the data field at the point in the processing chain at which it is generated, but rather it is stored to be applied at a later point in the processing chain. Throughout the decoding and post-processing chain, these scale factors are accumulated, and only at the very end of the audio processing chain are they combined with the data, in some cases, even after digital-to-analog conversion. This technique allows gross gain and attenuation factors to be applied to the data in the buffers, reducing neither the headroom that provides protection from overflow with large signals, nor the precision that provides protection from noise.

The Volume Manager must be run in conjunction with Digital Gain PPP to allow realization of the Digital Method of Volume Control.

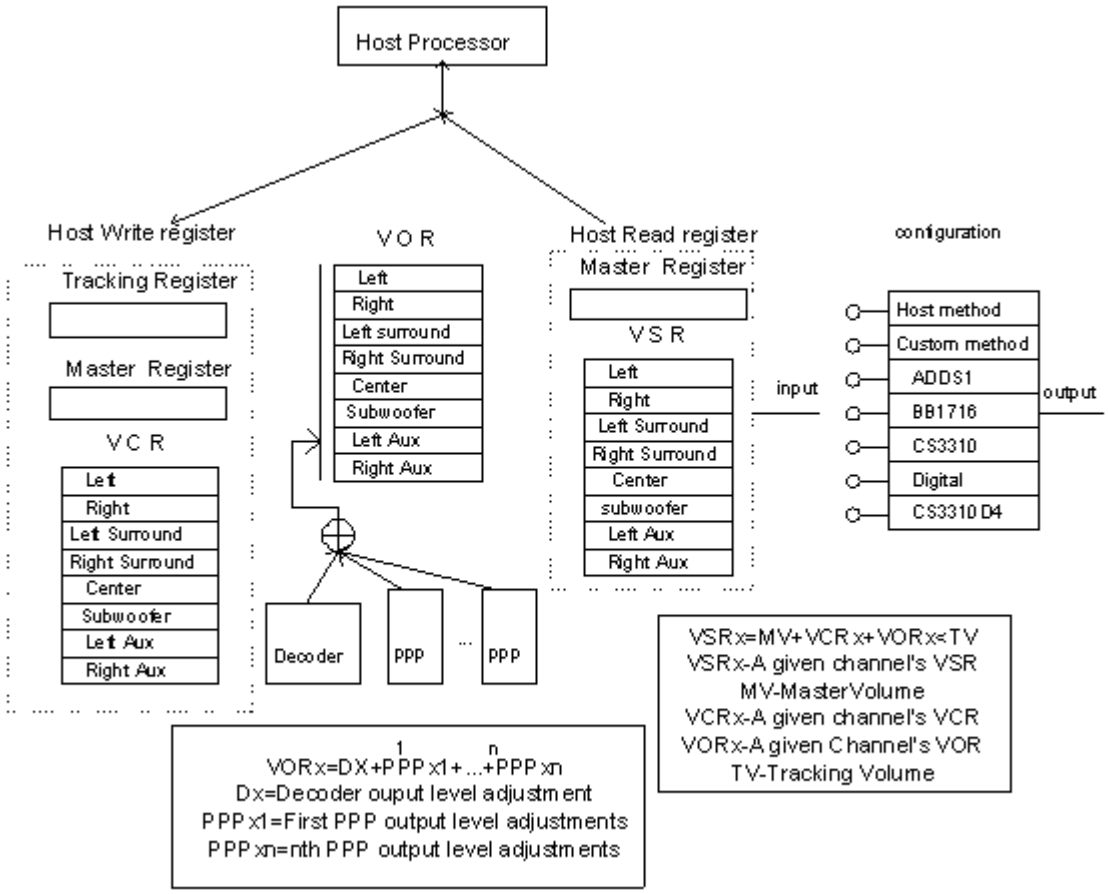


Figure 6-3. Volume Manager Structure

6.4.1 Volume Manager Status

Volume Manager Status Register should always be 0, indicating successful operation of the Volume Manager.

Table 6-11. Gain Manager Status Symbolic Opcodes

Symbol	Description	Value
getVMStatus	Report status register value.	0x882c00

6.4.2 Volume Manager Configuration

Table 6-12. Volume Manager Configuration Symbolic Opcodes

Symbol	Description	Value
setVMConfig	Set volume manager configuration	0xc82c01
sotVMConfigNone	The corresponding volume control method. Refer to the following table.	0x000000
sotVMConfigCustom		0x010000
sotVMConfigADDS1		0x020000
sotVMConfigADDS1_6		0x022906
sotVMConfigADDS1_8		0x022908
sotVMConfigADDS1_12		0x02290c
sotVMConfigBB1716		0x030000
sotVMConfigCS3310		0x040000
sotVMConfigCS3310_8		0x040008
sotVMConfigDigital		0x050000
sotVMConfigCS3310D		0x060000
sotVMConfigCS3310D_8		0x060008
getVMConfig	Report volume manager configuration	0x882c01

Table 6-13. Volume Control Method

Value		Volume Control Method
$000000		Host Method
$010000		Custom Method
$020000	$020000	DLC Method, Reserved for ADDS-1
	$022906	DLC Method, Reserved for ADDS-1/6 channel
	$02290c	DLC Method, Reserved for ADDS-1/12 channel
$0300nn	$030000	DLC Method, Reserved for PCM1716
	$030008	DLC Method, Reserved for PCM1716/8 channel
	$03000a	DLC Method, Reserved for PCM1716/10 channel
$0400nn	$040000	DLC Method, Reserved for CS3310
	$040008	DLC Method, Reserved for CS3310/ 8 channel
	$04000a	DLC Method, Reserved for CS3310/ 10 channel
$0500nn	$050000	Digital Gain Method
$0600nn	$060000	DLC Method, Reserved for CS3310D
	$060008	DLC Method, Reserved for CS3310D/8 channel
$0700nn		DLC Method, Reserved for CS3310D4

- Bits 23-18 of the configuration represent the Implementation method. The detailed information is as follows.

00: Host Method

If this option is selected, no method is provided for implementation of volume control. The correct values are computed into the Volume Status Registers, but these values are not useful in this case. It is assumed that host processor will provide an implementation of volume control.

01: Custom Method

If this option is selected, no implementation of volume control is provided directly by the Volume Manager, but an activation of an implementation is provided directly, and thus an implementation is provided indirectly, via custom code provided by the user. The correct values are computed into the Volume Status register, and these values are passed to the custom code which has been installed via the Code register in the post-processing control block.

02: Digital Level Control using the ADDS-1

03: Digital Level Control using the PCM1716

04: Digital Level Control using the CS3310

05: Digital Method

If this option is selected, volume control is provided via software within the Executive Programming Environment in the digital domain. The Digital Method of volume control requires that Volume Manager should be augmented by the Digital Gain PPP.

- Bits 15-8 represent the header of different implementation methods.
- Bits 7-0 represent the channel count.

6.5 De-emphasis & DC-Cut

De-emphasis is often used with pre-emphasis. Pre-emphasis is an intentional change made in the frequency response of a recording system to improve the signal-to-noise ratio or to reduce distortion. Typically, a high-frequency boost is used during recording, followed by complementary de-emphasis (a high-frequency cut) during playback.

De-emphasis supports 2-channel processing, which means to select one pair from Lf/Rf, Ls/Rs, C/Sub, or La/Ra. Each processed channel is subjected to the same filtering operation as outlined in the table and graphically depicted in the figure below. This is 50/15uS de-emphasis for compact disc as per IEC 60908 standard.

De-emphasis filter: The dotted line is the de-emphasis filter.

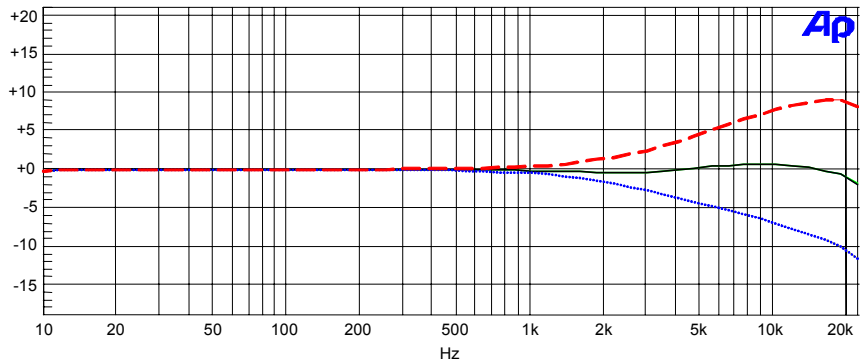


Figure 6-4. De-emphasis Characteristic

The DC-Cut PPP eliminates DC offset associated with some ADCs, and supports up to 8 channels of processing.

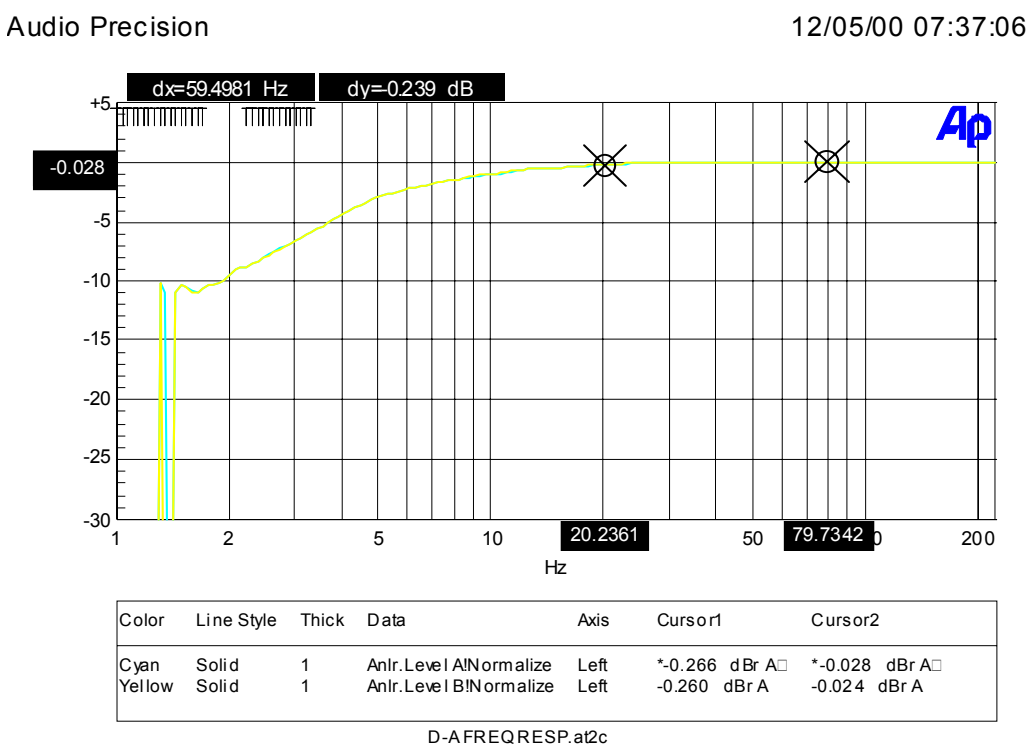


Figure 6-5. DC-Cut Characteristic

Table 6-14. De-emphasis & DC-Cut Configuration Register Symbolic Opcodes

Symbol	Description	Value
setDeemphDCCutConfig	Disable De-emphasis	0xc83301
sotBitDeemphConfigEnable	Enable De-emphasis	0x000001
sotBitDCCutConfigEnable	Enable DC-Cut	0x000002
sotBitDeemphDCCutConfigDisable	Disable De-emphasis & DC-Cut	0x000000
getDeemphDCCutConfig	Report configuration register value.	0x883301
gotBitDeemphDCCutConfigDisable		0x000000
gotBitDeemphConfigEnable		0x000001
gotBitDCCutConfigEnable		0x000002

Table 6-15. De-emphasis & DC-Cut Channel Mask Opcodes

Symbol	Description	Value
setDeemphDCCutChannelMask	Enable De-emphasis & DC-Cut Channel Mask.	0xc83302
sotBitDeemphChannelMaskLR	*Note1.	0x000080
sotBitDeemphChannelMaskLsRs		0x000040
sotBitDeemphChannelMaskCntrSub		0x000020
sotBitDeemphChannelMaskLaRa		0x000010
sotBitDCCutChannelMaskLR		0x000008
sotBitDCCutChannelMaskLsRs		0x000004
sotBitDCCutChannelMaskCntrSub		0x000002
sotBitDCCutChannelMaskLaRa		0x000001
getDeemphDCCutChannelMaskStatus	Report De-emphasis Channel Mask Status Register.	0x883302

Note:

1. In De-emphasis channel mask setting, only one pair of channels is effective, such as L/R, Ls/Rs, Cntr/Sub or La/Ra. If the user sets multi-channel mask, the effective channel must be the one with big value. For example: If the user sends command “$c83302 $50,” the effective channel will be Ls/Rs.

6.6 Loudness

The Loudness PPP provides low frequency boost and high frequency boost for up to 8 channels in either dynamic or static mode. It provides default setting for applications without a uC (i.e., static implementation, boost levels, cutoff frequencies, on/off).

The Loudness PPP provides 41 gain levels (from 0dB to 20dB in 0.5dB step). For dynamic step depends on the step and range of supported filter boost level, 41 steps dynamic loudness are supported at 44.1kHz and 48kHz. Coefficients can be loaded for filtering to accommodate custom filter implementations and sample rates.

The Loudness PPP provides two control types: dynamic and static. In static control, the user can control the boost level. In dynamic control, the PPP will first detect the input level, and according to this level, add the specified filter to boost each channel. When the input level is greater than or equal with No Effect Point, the boost level is 0dB. When input level range is from No Effect Point to Threshold, the boot level is from 0dB to Gain in linear. When input level is less than or equal with Threshold, the boost level is Gain. The dynamic loudness characteristic is depicted as Figure 6-6:

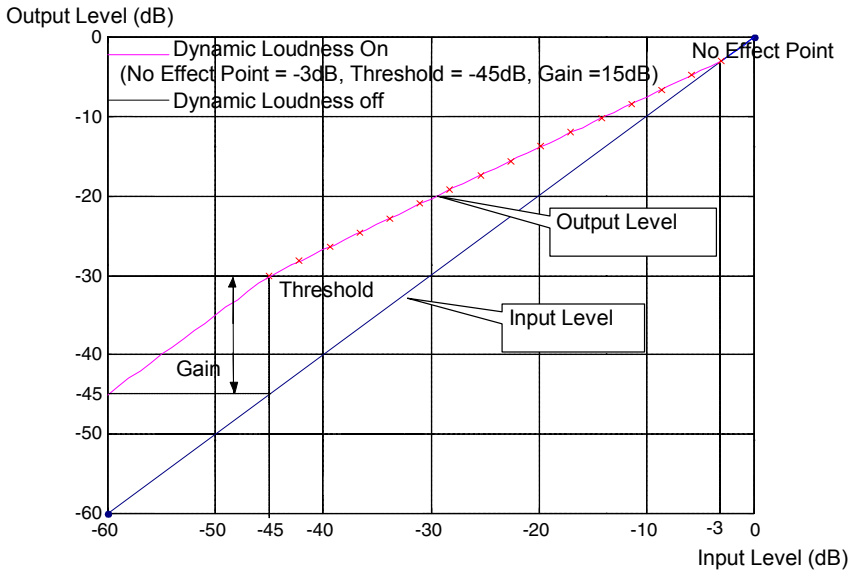


Figure 6-6. Dynamic Loudness Characteristic

When the Loudness PPP is invoked the first time, it has a default setting of static loudness control with 0 dB boost. The user can change the parameter on the fly in an active running system. In PPP processing, each channel is subjected to the same filtering process outlined in the table and graphically depicted in the figure below. The filter characteristics is as follows:

Loudness Control	Fc	Control Range	Default Boost
Low Frequency Boost	100 Hz	0-20 dB	0 dB
High Frequency Boost	5000 Hz	0-20 dB	0 dB

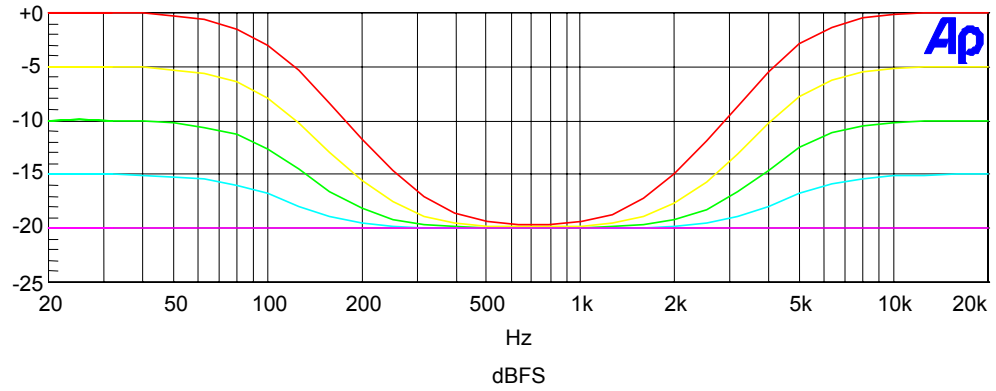


Figure 6-7. Static Mode, Bass Boost and Treble Boost

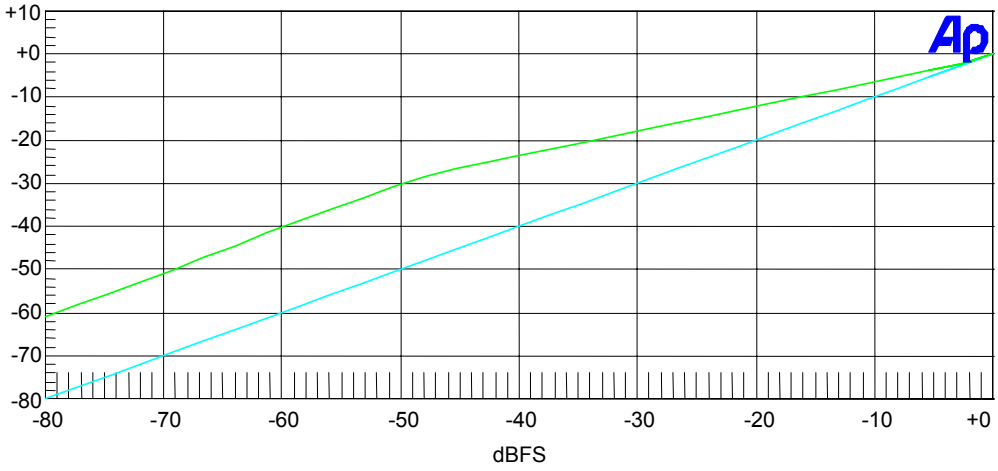


Figure 6-8. Dynamic Mode, 50 Hz

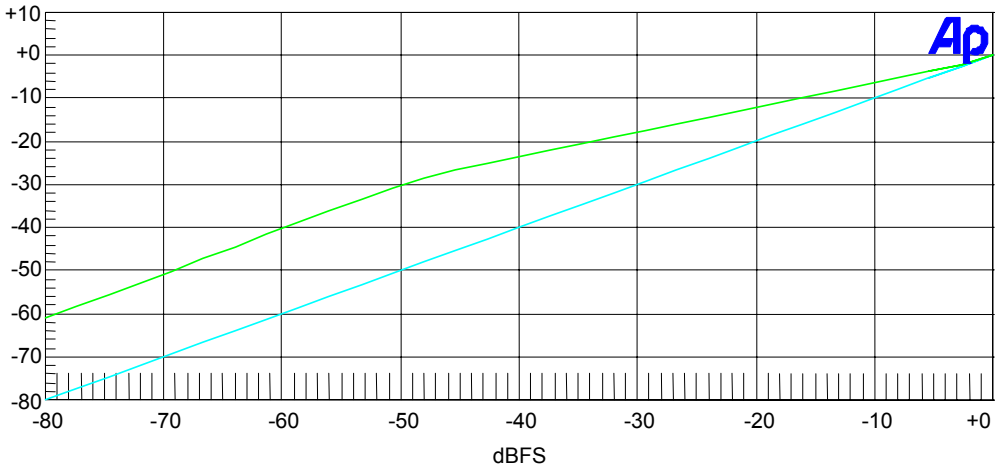


Figure 6-9. Dynamic Mode, 10000 Hz

Table 6-16. Loudness Configuration Register Symbolic Opcodes

Symbol	Description	Value
setLoudnessConfig		0xc82301
sotBitLoudnessConfigDisable	Disable Loudness	0x000000
sotBitLoudnessConfigEnable	Enable Loudness	0x000001
sotBitLoudnessAutoUpdate	Automatic Coefficients Calculation	0x000002
sotBitLoudnessDynamic	Dynamic Mode	0x000004
sotBitLoudnessChannelMaskLch	Channel Mask	0x000100
sotBitLoudnessChannelMaskRch		0x000200
sotBitLoudnessChannelMaskLsch		0x000400
sotBitLoudnessChannelMaskRsch		0x000800
sotBitLoudnessChannelMaskCch		0x001000
sotBitLoudnessChannelMaskSubch		0x002000
sotBitLoudnessChannelMaskLach		0x004000
sotBitLoudnessChannelMaskRach		0x008000
setLoudnessGainBass	In Static Mode	0xc82304
setLoudnessGainTreble	In Static Mode	0xc82305
getLoudnessConfig	Report configuration register value.	0x882301
gotBitLoudnessConfigDisable		0x000000
gotBitLoudnessChannelMaskLch	In Static Mode	0x000103
gotBitLoudnessChannelMaskRch		0x000203
gotBitLoudnessChannelMaskLsch		0x000403
gotBitLoudnessChannelMaskRsch		0x000803
gotBitLoudnessChannelMaskCch		0x001003
gotBitLoudnessChannelMaskSubch		0x002003
gotBitLoudnessChannelMaskLach		0x004003
gotBitLoudnessChannelMaskRach		0x008003
gotBitLoudnessChannelMaskLch	In Dynamic Mode	0x000107
gotBitLoudnessChannelMaskRch		0x000207
gotBitLoudnessChannelMaskLsch		0x000407
gotBitLoudnessChannelMaskRsch		0x000807
gotBitLoudnessChannelMaskCch		0x001007
gotBitLoudnessChannelMaskSubch		0x002007
gotBitLoudnessChannelMaskLach		0x004007
gotBitLoudnessChannelMaskRach		0x008007

For example:

1. Send command ‘$c82301 $303’ to enable Loudness PPP in Static Mode, and the selected channel are Lf/Rf;
2. Send command ‘$c82304 $0 ’ to set Bass Boost filter gain in Min (0 dB), ‘$c82304 $a’ to set the step of gain (5 dB), and ‘$c82304 $28 ’ to set the Max gain (20 dB);
3. Send command ‘$c82305 $0/$a/$28’ to set Treble gain in 0/5/20 dB;
4. Send command ‘$c82301 $307’ to enable Loudness PPP in Dynamic Mode, and the selected channel are Lf/Rf;
5. Send command ‘$c82301 $0’ to disable Loudness PPP;

6.7 Compression

The Compression PPP detects the input level and provides dynamic compression for up to 8 channels in a multiple channel system. It detects peak level first, and according to this level, adds a specified output level to boost each channel.

When the input level is greater than or equal to the Ref0dB point, the boost level is 0dB. When input level range is from Ref0dB to Threshold, the boost level is from 0dB to Gain in linear. When the input level is less than or equal to Threshold, the boost level is Gain. The user can define Threshold, Ref0dB and Gain. The Compression PPP characteristic is depicted in Figure 6-10.

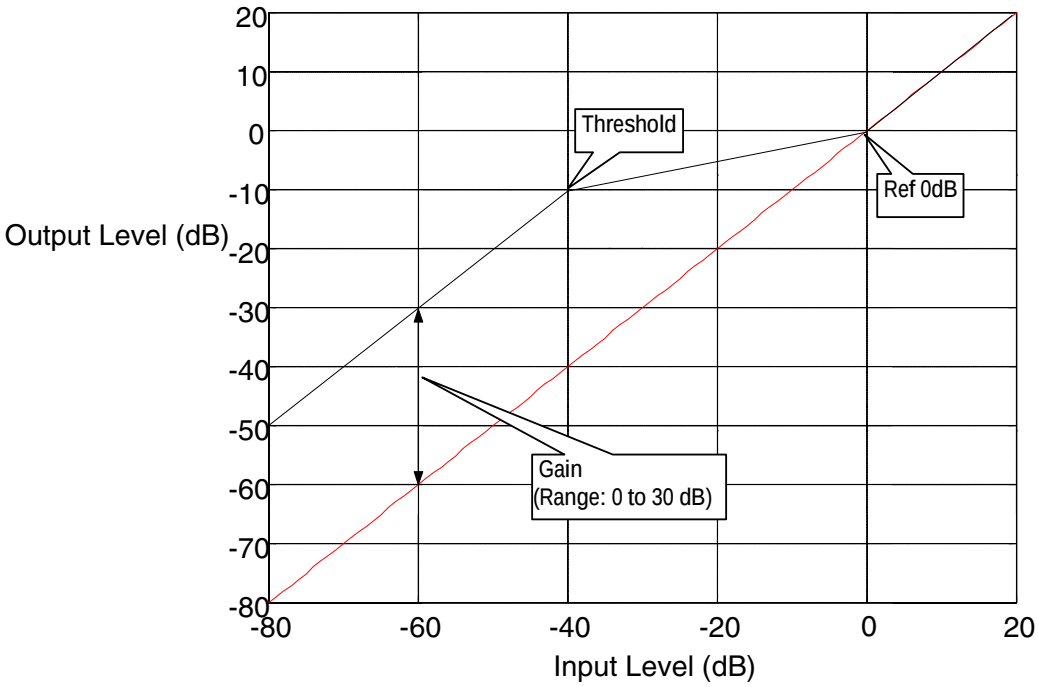


Figure 6-10. Compression Characteristic

Table 6-17. Compression Configuration Register Symbolic Opcodes

Symbol	Description	Value
setCompressionConfig		0xc81e01
setLoudnessConfigDisable	Disable Compression.	0xe78500
setLoudnessConfigEnable	Enable Compression.	0xe78501
setCompressionCoeffPtr		0xc81e02
setCompressionDecayCoeff1		0xc81e03
setCompressionAttackCoeff1		0xc81e05
setCompressionAttackCoeff2		0xc81e06
setCompressionUpdatefreeze		0xc81e07
setCompressionBreakoverPointer		0xc81e08
setCompressionGain		0xc81e09
setCompressionRef0		0xc81e0a
setCompressionShiftB		0xc81e0c
setCompressionAxPBA0		0xc81e0f
setCompressionAxPBB0		0xc81e10
setCompressionAxPBA(N)	N range [0,1...16].	0xc81e0f+2*N
setCompressionAxPBB(N)		0xc81e10+2*N

Table 6-18. Compression Channel Mask Opcodes

Symbol	Description	Value
setCompressionChannelMask	Enable Compression Channel Mask.	0xe78600
sotBitCompressionChannelMaskLch		0x000001
sotBitCompressionChannelMaskRch		0x000002
sotBitCompressionChannelMaskLsch		0x000004
sotBitCompressionChannelMaskRsch		0x000008
sotBitCompressionChannelMaskCch		0x000010
sotBitCompressionChannelMaskSubch		0x000020
sotBitCompressionChannelMaskLach		0x000040
sotBitCompressionChannelMaskRach		0x000080
getCompressionChannelMask	Report Channel Mask register value.	0xa78600
gotBitCompressionChannelMaskLch		0x000001
gotBitCompressionChannelMaskRch		0x000002
gotBitCompressionChannelMaskLsch		0x000004
gotBitCompressionChannelMaskRsch		0x000008
gotBitCompressionChannelMaskCch		0x000010
gotBitCompressionChannelMaskSubch		0x000020
gotBitCompressionChannelMaskLach		0x000040
gotBitCompressionChannelMaskRach		0x000080

For example:

1. Send command ‘$e78501’ to enable Compression PPP, and the default selected channel are Lf/Rf
2. Send command ‘$e786ff ’ to select 4 pairs of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra
3. Send command ‘$e78500’ to disable Compression PPP

6.8 Compression Dynamic Range Control

The Compression Dynamic Range Control (DRC) PPP detects input level and provides dynamic compression for up to 8 channels in a multiple channel system. It detects the peak level first, and according to this level, adds a specified output level to boost each channel. Its characteristic is as follows: In the graph, the dash line represents the Input level, and the real line represents the Output level. The characteristic of the Compression DRC is like Compression’s in fact. When the input level is less than or equal to -48dB, output level is +15dB linear higher relative to the input. When the input level range is from –48dB to 0dB, the output level is boosted to –4dB in linear. The characteristics of the Compression DRC PPP is similar to that of the Compression PPP.

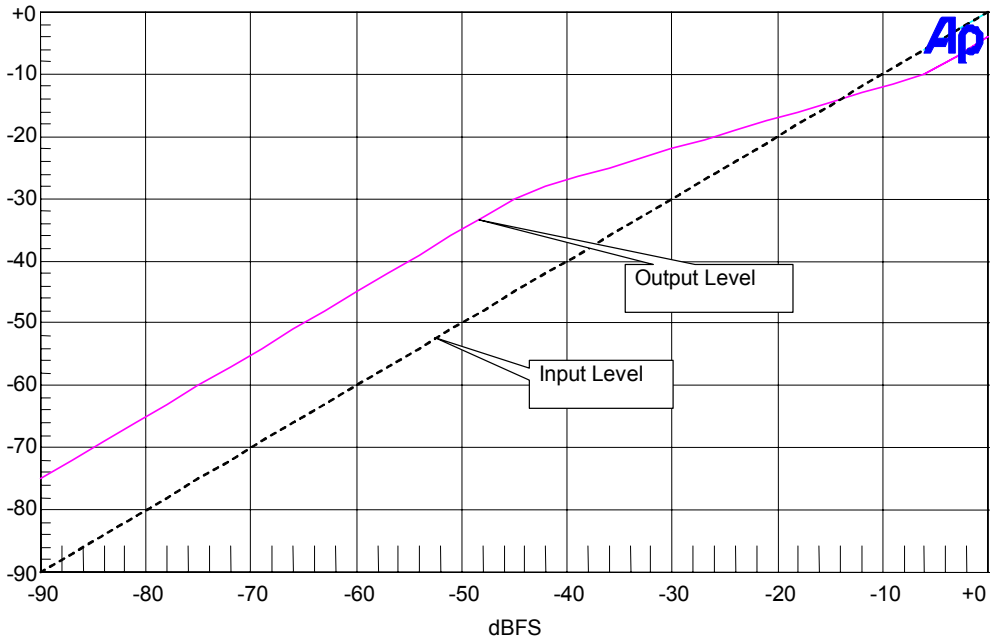


Figure 6-11. Compression Dynamic Range Control Characteristic

Table 6-19. Compression DRC Configuration Register Symbolic Opcodes

Symbol	Description	Value
setDRCConfig		0xc82001
sotBitDRCConfigDisable	Disable Compression DRC	0x000000
setBitDRCConfigEnable	Enable Compression DRC	0x000001
setDRCUserAttenuation	Unit: dB, in 0.5 dB step	0xc82002
getDRCStatus	Report DRC Status Register Value	0x882000
getDRCConfig	Report Configuration Register Value	0x882001
gotBitDRCConfigModeDisable		0x000000
gotBitDRCConfigModeEnable		0x000001

Table 6-20. Compression DRC Channel Mask Opcodes

Symbol	Description	Value
setDRCChannelMask	Enable Compression DRC Channel Mask	0xe80600
sotBitDRCChannelMaskLch		0x000001
sotBitDRCChannelMaskRch		0x000002
sotBitDRCChannelMaskLsch		0x000004
sotBitDRCChannelMaskRsch		0x000008
sotBitDRCChannelMaskCch		0x000010
sotBitDRCChannelMaskSubch		0x000020
sotBitDRCChannelMaskLach		0x000040
sotBitDRCChannelMaskRach		0x000080

Table 6-20. Compression DRC Channel Mask Opcodes (continued)

getDRCChannelMask	Report Channel Mask Register Value	0xa80600
gotBitDRCChannelMaskLch		0x000001
gotBitDRCChannelMaskRch		0x000002
gotBitDRCChannelMaskLsch		0x000004
gotBitDRCChannelMaskRsch		0x000008
gotBitDRCChannelMaskCch		0x000010
gotBitDRCChannelMaskSubch		0x000020
gotBitDRCChannelMaskLach		0x000040
gotBitDRCChannelMaskRach		0x000080

For example:

1. Send command '$c82001 $1' to enable Compression DRC PPP, and the default selected channel are Lf/Rf;
2. Send command '$e806ff ' to select 4 pair of channel, Lf/Rf, Ls/Rs, C/Sub, La/Ra;
3. Send command '$c82001 $0' to disable Compression DRC PPP;

6.9 Parametric EQ

The Parameter EQ (PEQ) PPP provides flexible structure for different requirements in a multiple channel audio system. Each band employs a peaking filter capable of applying a maximum boost or cut of 15 dB as outlined in the table below or shelving filter. The default setting of PEQ is 5Group and 5Band. Each Group is used on the specific channel: Group1-Lf, Group2-Rf, Group3-Ls, Group4-Rs, Group5-Cntr. PEQ doesn't support Sub/La/Ra channel processing in the default setting.

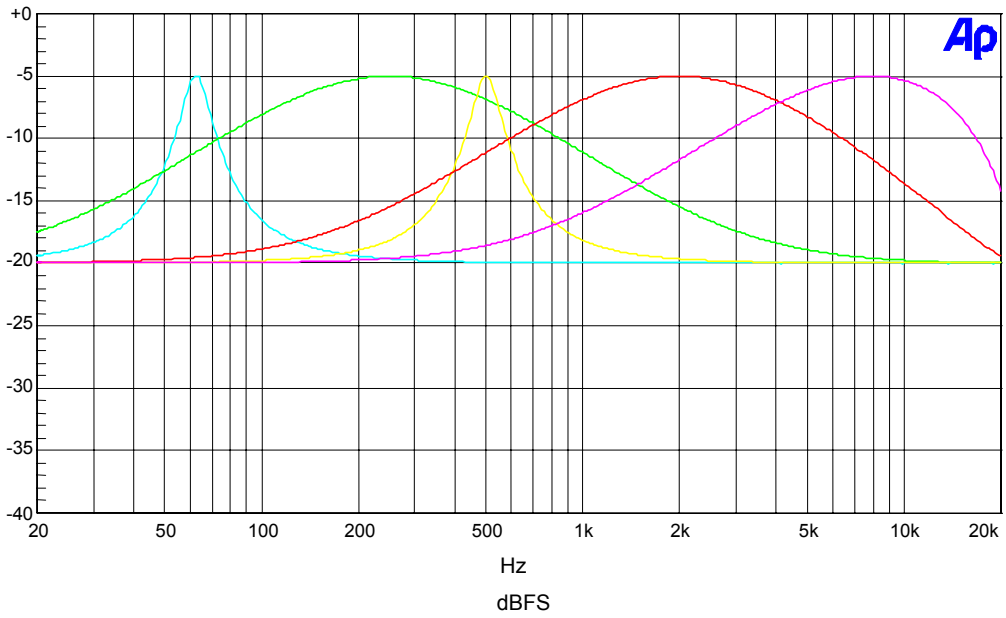
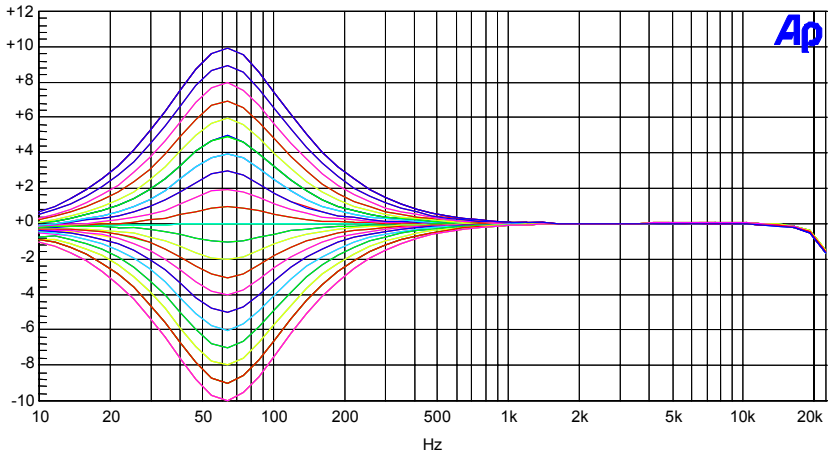


Figure 6-12. Fc (Hz)/Gain (dB)/Q=62.5/15/5, 250/15/0.5, 500/15/5, 2k/15/0.5, 8k/15/0.5

- Fc = 62.5 Hz, Q=1.0, Gain is from -10 dB ~ 10 dB with 1 dB/step

Audio Precision

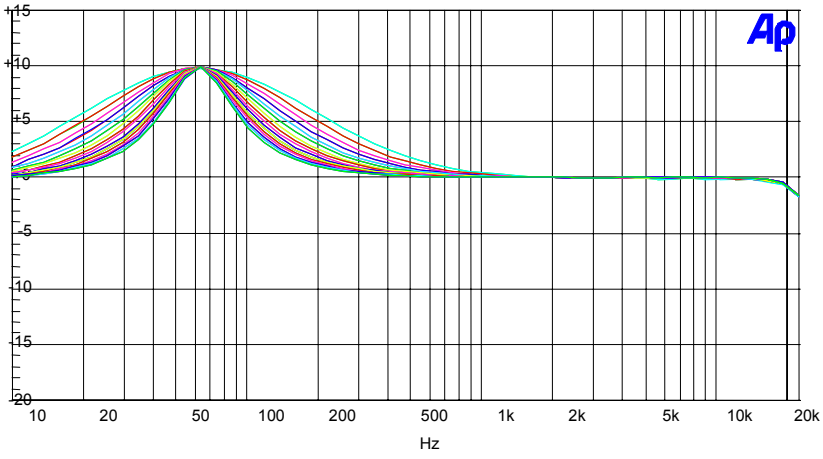


Color	Line Style	Thick	Data	Axis
Green	Solid	1	Anlr.Level A!Normalize	Left
Cyan	Solid	1	Anlr.Level B!Normalize	Left
Green	Solid	1	Anlr.Level A!Normalize	Left
Red	Solid	1	Anlr.Level B!Normalize	Left

D-A FREQ RESP.at2c

Figure 6-13. Fc = 62.5 Hz, Q=1.0, Gain is from -10 dB ~ 10 dB with 1 dB/step

Audio Precision



Color	Line Style	Thick	Data	Axis
Green	Solid	1	Anlr.Level A!Normalize	Left
Cyan	Solid	1	Anlr.Level B!Normalize	Left
Green	Solid	1	Anlr.Level A!Normalize	Left
Red	Solid	1	Anlr.Level B!Normalize	Left

D-A FREQ RESP.at2c

Figure 6-14. Fc =62.5Hz, Gain = 10dB, Q is from 0.5 ~ 2.0 with 0.1/step

Table 6-21. Parametric EQ Configuration Register Symbolic Opcodes

Symbol	Description	Value
setParaEQConfig		0xc82901
setParaEQConfigMode		0xea4700
sotBitParaEQConfigDisable	Disable Parametric EQ	0x000000
sotBitParaEQConfigEnableCalc	Enable Parametric EQ	0x000003
sotBitParaEQConfigEnableManual	Download Mode	0x000001
getParaEQConfig	Report Configuration Register Value	0x882901
getParaEQConfigMode		0xaa4700
gotBitParaEQConfigEnableCalc		0x000003
gotBitParaEQConfigEnableManual		0x000001
gotBitParaEQConfigDisable		0x000000

Table 6-22. Parametric EQ Channel Mask Opcodes

Symbol	Description	Value
setBitParaEQChannelMask	Enable Parametric EQ Channel Mask	0xea4600
sotBitParaEQChannelMaskLch		0x000001
sotBitParaEQChannelMaskRch		0x000002
sotBitParaEQChannelMaskLsch		0x000004
sotBitParaEQChannelMaskRsch		0x000008
sotBitParaEQChannelMaskCch		0x000010
sotBitParaEQChannelMaskSubch		0x000020
sotBitParaEQChannelMaskLach		0x000040
sotBitParaEQChannelMaskRach		0x000080
getBitParaEQChannelMask	Report Channel Mask Register Value	0xaa4600
gotBitParaEQChannelMaskLch		0x000001
gotBitParaEQChannelMaskRch		0x000002
gotBitParaEQChannelMaskLsch		0x000004
gotBitParaEQChannelMaskRsch		0x000008
gotBitParaEQChannelMaskCch		0x000010
gotBitParaEQChannelMaskSubch		0x000020
gotBitParaEQChannelMaskLach		0x000040
gotBitParaEQChannelMaskRach		0x000080
getParaEQEffectChannelMask	Report Actual Channel Mask with Audio Mode	0xaa4500

Table 6-22. Parametric EQ Channel Mask Opcodes (continued)

gotBitParaEQEffectChannelMaskLch		0x000001
gotBitParaEQEffectChannelMaskRch		0x000002
gotBitParaEQEffectChannelMaskLsch		0x000004
gotBitParaEQEffectChannelMaskRsch		0x000008
gotBitParaEQEffectChannelMaskCch		0x000010
gotBitParaEQEffectChannelMaskSubch		0x000020
gotBitParaEQEffectChannelMaskLach		0x000040
gotBitParaEQEffectChannelMaskRach		0x000080

For example:

1. Send command '$ea4703' to enable PEQ PPP, and the default selected channel are Lf/Rf
2. Send command '$ea46ff ' to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra
3. Send command '$ea4700' to disable PEQ PPP

Table 6-23. Parametric EQ Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setParaEQCalNumPerFrame		0xea52nn
setParaEQGroup1Band1Fc	ParaEQGroupNBandMPara2 refers to Table 6-24	0xc8290c+0x000000
setParaEQGroup1Band1Para2		0xc8290c+0x000001
sotParaEQGroup1Band1ParaChange		0x800000
setParaEQGroupNBandMFc		0xc8290c+0x000002*((N-1)*5+(M-1))+0
setParaEQGroupNBandMPara2		0xc8290c+0x000002*((N-1)*5+(M-1))+1
sotParaEQGroupNBandMParaChange		0x800000
setParaEQGroup1Band1Fc		0xc8290c
setParaEQGroup1Band1Para2		0xc8290d
setParaEQGroup1Band2Fc		0xc8290e
setParaEQGroup1Band2Para2		0xc8290f
setParaEQGroup2Band1Fc		0xc82916
setParaEQGroup2Band1Para2		0xc82917
setParaEQGroup2Band2Fc		0xc82918
setParaEQGroup2Band2Para2		0xc82919
.....		.....
setParaEQGroup5Band1Fc		0xc82934
setParaEQGroup5Band2Para2		0xc82935
getParaEQCalNumPerFrame		0xaa5200
getParaEQFilGroupNum		0xaa5100
getBitParaEQChannelFilInfo		0x882905
getParaEQFiltCoefPtr		0x882906
getParaEQGroup1BandNum		0x882907
getParaEQGroup2BandNum		0x882908
getParaEQGroup3BandNum		0x88290a
getParaEQGroup4BandNum		0x88290b

Table 6-23. Parametric EQ Parameter Configuration Symbolic Opcodes (continued)

getparaEQGroup5BandNum		0x88290c
getParaEQGroup1Band1Fc		0x88290c+0x000000
getParaEQGroup1Band1Para2		0x88290c+0x000001
gotParaEQGroup1Band1ParaChange		0x800000
getParaEQGroupNBandMFc	N=1,2.....5; M=1,2.....5; Default Fc (Hz): 63, 250, 500, 2 k, 8 k;	0x88290c+0x000002*((N-1)*5+(M-1))+0
getParaEQGroupNBandMPara2		0x88290c+0x000002*((N-1)*5+(M-1))+1
gotParaEQGroupNBandMParaChange		0x800000
getParaEQGroup1Band1Fc		0x88290c
getParaEQGroup1Band1Para2		0x88290d
getParaEQGroup1Band2Fc		0x88290e
getParaEQGroup1Band2Para2		0x88290f
getParaEQGroup2Band1Fc		0x882916
getParaEQGroup2Band1Para2		0x882917
getParaEQGroup2Band2Fc		0x882918
getParaEQGroup2Band2Para2		0x882919
.....		.....
getParaEQGroup5Band1Fc		0x882934
getParaEQGroup5Band2Para2		0x882935

Table 6-24. Parametric EQ GroupNBandMPara2 Table

Bit	Description	
23	This bit represents the corresponding coefficients that should be updated. 0: No Update 1: Update	
22-19	Reserved.	
18	This bit represents filter function. It is NOT allowed to update on the fly. 0: Biquad (Single Precision) 1: Biquad2 (Mix Precision).	
17-16	Bit 16:17 has 4 values, 0,1,2 and 3. 00: Peak Filter 01: Shelving Filter 10: Reserved 11: Reserved	
15-7	Bit 7:15 represents Gain with 0.1 dB step, range from –15 dB to 15 dB.	
6-0	Peaking Filter	Bit 0:6 represents Q parameter with 0.1 step, range from 0.1 to 5.
	Shelving Filter	Bit 0:6 represents shelving filter type. 0: Low Frequency Shelving Filter 1: High Frequency Shelving Filter

For example:

1. Send command ‘$c8290d $844b32’ to set PEQGroup1Band1Para2, and the configuration is: Band1, Biquad2, Peaking filter, Gain=15dB, Q=5
2. Send command ‘$c8290c $3e8 ’ to set PEQGroup1Band1 filter Fc=100Hz, and then have to set the Band1’s Gain and Q to update the filter with new Fc parameter, such as ‘$c8209d $844b05’
3. Send command ‘$c8290d $854b00’ to change the filter type into low frequency Shelving filter
4. Send command ‘$c8290d $854b01’ to change the filter type into high frequency Shelving filter

6.10 Graphic EQ

The Graphic EQ (GEQ) PPP algorithm and characteristics are the same as the PEQ PPP. However, GEQ only has 1Group and 5Band, and it supports up to 5-channel processing in the default setting.

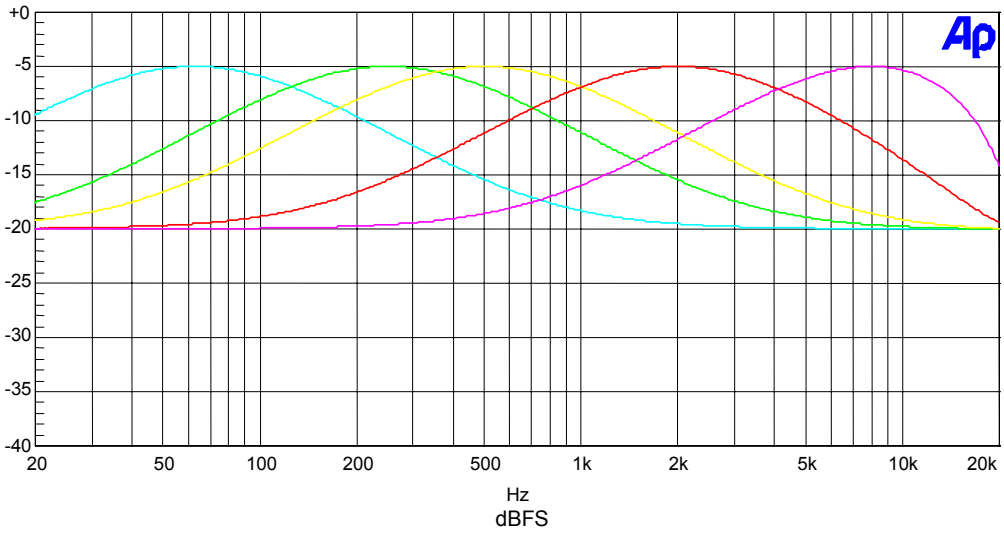


Figure 6-15. Fc (Hz)/Gain (dB)/Q=62.5/15/0.5, 250/15/0.5, 500/15/0.5, 2k/15/0.5, 8k/15/0.5

Table 6-25. Graphic EQ Configuration Register Symbolic Opcodes

Symbol	Description	Value
setGEQConfig		0xc82801
setGEQConfigMode		0xea0700
sotBitGEQConfigDisable	Disable Graphic EQ	0x000000
sotBitGEQConfigEnableCalc	Enable Graphic EQ	0x000003
sotBitGEQConfigEnableManual	Download Mode	0x000001
getGEQConfig	Report Configuration Register Value	0x882801
getGEQConfigMode		0xaa0700
gotBitGEQConfigEnableCalc		0x000003
gotBitGEQConfigEnableManual		0x000001
gotBitGEQConfigDisable		0x000000

Table 6-26. Graphic EQ Channel Mask Opcodes

Symbol	Description	Value
setGEQChannelMask	Enable Graphic EQ Channel Mask	0xea0600
sotBitGEQChannelMaskLch		0x000001
sotBitGEQChannelMaskRch		0x000002
sotBitGEQChannelMaskLsch		0x000004
sotBitGEQChannelMaskRsch		0x000008
sotBitGEQChannelMaskCch		0x000010
sotBitGEQChannelMaskSubch		0x000020
sotBitGEQChannelMaskLach		0x000040
sotBitGEQChannelMaskRach		0x000080
getGEQChannelMask	Report Channel Mask Register Value	0xaa0600
gotBitGEQChannelMaskLch		0x000001
gotBitGEQChannelMaskRch		0x000002
gotBitGEQChannelMaskLsch		0x000004
gotBitGEQChannelMaskRsch		0x000008
gotBitGEQChannelMaskCch		0x000010
gotBitGEQChannelMaskSubch		0x000020
gotBitGEQChannelMaskLach		0x000040
gotBitGEQChannelMaskRach		0x000080
getGEQEffectChannelMask	Report Actual Channel Mask with Audio Mode	0xaa0500
gotBitGEQEffectChannelMaskLch		0x000001
gotBitGEQEffectChannelMaskRch		0x000002
gotBitGEQEffectChannelMaskLsch		0x000004
gotBitGEQEffectChannelMaskRsch		0x000008
gotBitGEQEffectChannelMaskCch		0x000010
gotBitGEQEffectChannelMaskSubch		0x000020
gotBitGEQEffectChannelMaskLach		0x000040
gotBitGEQEffectChannelMaskRach		0x000080

For example:

1. Send command ‘$ea0703’ to enable GEQ PPP, and the default selected channel are Lf/Rf;
2. Send command ‘$ea06ff ’ to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra;
3. Send command ‘$ea0700’ to disable GEQ PPP;

Table 6-27. Graphic EQ Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setGEQCalNumPerFrame		0xea12nn
setGEQGroup1Band1Para2	GEQGroup1BandMPara2 Refers to Table 6-28	0xc82808+0x000001
sotGEQGroup1Band1ParaChange		0x800000
setGEQGroup1BandMPara2		0xc82808+0x000002*(M-1)+1
sotGEQGroup1BandMParaChange		0x800000
setGEQGroup1Band1Para2		0xc82809
setGEQGroup1Band2Para2		0xc8280b
……		……
setGEQGroup1Band5Para2		0xc82811
getGEQCalNumPerFrame		0xaa1200
getGEQFilGroupNum		0xaa1100
getGEQChanFilInfo		0x882805
getGEQFiltCoefPtr		0x882806
getGEQGroup1BandNum		0x882807
getGEQGroup1Band1Para2		0x882808+0x000001
gotGEQGroup1Band1ParaChange		0x800000
getGEQGroup1BandMPara2	M=1,2,.....5	0x882808+0x000002*(M-1)+1
gotGEQGroup1BandMParaChange		0x800000
getGEQGroup1Band1Para2		0x882809
getGEQGroup1Band2Para2		0x88280b
……		……
getGEQGroup1Band5Para2		0x882811

Table 6-28. Graphic EQ Group1BandMPara2 Table

Bit	Description	
23	This bit represents the corresponding coefficients that should be updated. 0: No Update 1: Update	
22-19	Reserved	
18	This bit represents filter function. It is NOT allowed to update on the fly. 0: Biquad (Single Precision) 1: Biquad2 (Mix Precision).	
17-16	Bit 16:17 has 4 values, 0,1, 2 and 3. 00: Peak Filter 01: Shelving Filter 10: Reserved 11: Reserved	
15-7	Bit 7:15 represents Gain with 0.1 dB step, range from –15 dB to 15 dB.	
6-0	Peaking Filter	Bit 0:6 represents Q parameter with 0.1 step, range from 0.1 to 5.
	Shelving Filter	Bit 0:6 represents shelving filter type. 0: Low Fequency Shelving Filter 1: High Frequency Shelving Filter

For example:

1. Send command ‘$c82809 $804b32’ to set GEQGroup1Band1Para2, and the configuration is: Band1, Biquad1, Gain=15dB, Q=5;
2. Send command ‘$c82809 $814b00’ to change the filter type into low frequency Shelving filter;
3. Send command ‘$c82809 $814b01’ to change the filter type into high frequency Shelving filter;

6.11 Speaker Compensation

The Speaker Compensation PPP algorithm and characteristic are the same as PEQ PPP. However, the Speaker Compensation only has 1Group and 7Band, and it supports up to 5-channel processing in the default setting.

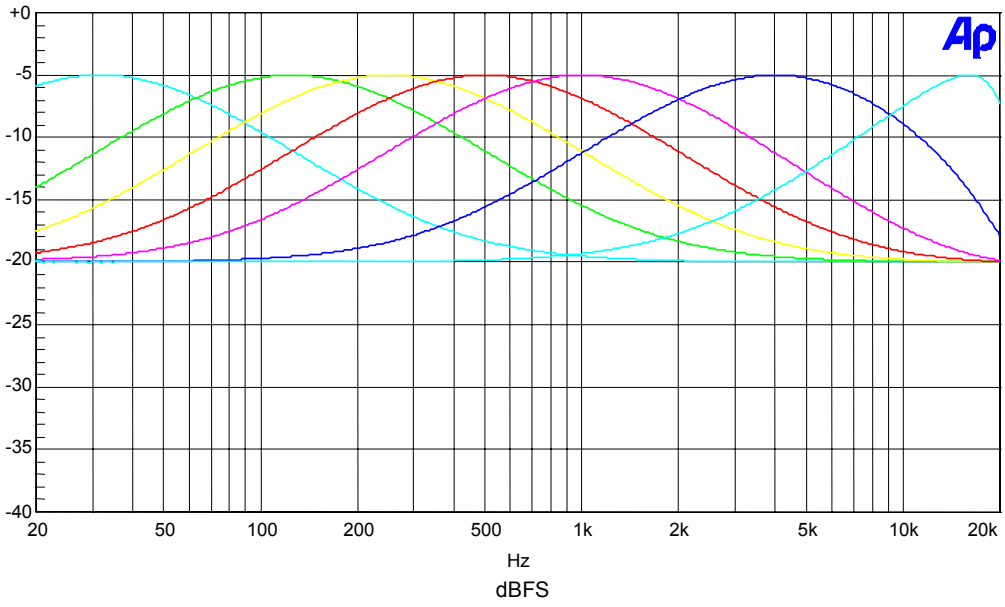


Figure 6-16. Fc (Hz)/Gain (dB)/Q=31.5/15/0.5, 125/15/0.5, 250/15/0.5, 500/15/0.5, 1k/15/0.5, 4k/15/0.5, 16k/15/0.5

Table 6-29. Speaker Compensation Configuration Register Symbolic Opcodes

Symbol	Description	Value
setSpkCompConfig		0xc82701
setSpkCompConfigMode		0xe9c700
sotBitSpkCompConfigDisable	Disable Speaker Compensation.	0x000000
sotBitSpkCompConfigEnableCalc	Enable Speaker Compensation.	0x000003
sotBitSpkCompConfigEnableManual	Download Mode.	0x000001
getSpkCompConfig	Report Configuration Register Value.	0x882701
getSpkCompConfigMode		0xa9c700
gotBitSpkCompConfigEnableCalc		0x000003
gotBitSpkCompConfigEnableManual		0x000001
gotBitSpkCompConfigDisable		0x000000

Table 6-30. Speaker Compensation Channel Mask Opcodes

Symbol	Description	Value
setSpkCompChannelMask	Enable Speaker Compensation Channel Mask	0xe9c600
sotBitSpkCompChannelMaskLch		0x000001
sotBitSpkCompChannelMaskRch		0x000002
sotBitSpkCompChannelMaskLsch		0x000004
sotBitSpkCompChannelMaskRsch		0x000008
sotBitSpkCompChannelMaskCch		0x000010
sotBitSpkCompChannelMaskSubch		0x000020
sotBitSpkCompChannelMaskLach		0x000040
sotBitSpkCompChannelMaskRach		0x000080
getSpkCompChannelMask	Report Channel Mask Register Value.	0xa9c600
gotBitSpkCompChannelMaskLch		0x000001
gotBitSpkCompChannelMaskRch		0x000002
gotBitSpkCompChannelMaskLsch		0x000004
gotBitSpkCompChannelMaskRsch		0x000008
gotBitSpkCompChannelMaskCch		0x000010
gotBitSpkCompChannelMaskSubch		0x000020
gotBitSpkCompChannelMaskLach		0x000040
gotBitSpkCompChannelMaskRach		0x000080
getSpkCompEffectChannelMask	Report Actual Channel Mask with Audio Mode.	0xa9c500
gotBitSpkCompEffectChannelMaskLch		0x000001
gotBitSpkCompEffectChannelMaskRch		0x000002
gotBitSpkCompEffectChannelMaskLsch		0x000004
gotBitSpkCompEffectChannelMaskRsch		0x000008
gotBitSpkCompEffectChannelMaskCch		0x000010
gotBitSpkCompEffectChannelMaskSubch		0x000020
gotBitSpkCompEffectChannelMaskLach		0x000040
gotBitSpkCompEffectChannelMaskRach		0x000080

For example:

1. Send command ‘$e9c703’ to enable Speaker Compensation PPP, and the default selected channel are Lf/Rf;
2. Send command ‘$e9c6ff ’ to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra;
3. Send command ‘$e9c700’ to disable Speaker Compensation PPP;

Table 6-31. Speaker Compensation Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setSpkCompCalNumPerFrame		0xe9d2nn
setSpkCompGroup1Band1Fc	SpkCompGroup1BandMPara2 refers to Table 6-32.	0xc82708+0x000000
setSpkCompGroup1Band1Para2		0xc82708+0x000001
sotSpkCompGroup1Band1ParaChange		0x800000
setSpkCompGroup1BandMFc		0xc82708+0x000002*(M-1)+0
setSpkCompGroup1BandMPara2		0xc82708+0x000002*(M-1)+1
sotSpkCompGroup1BandMParaChange		0x800000
setSpkCompGroup1Band1Fc		0xc82708
setSpkCompGroup1Band1Para2		0xc82709
setSpkCompGroup1Band2Fc		0xc8270a
setSpkCompGroup1Band2Para2		0xc8270b
……		……
setSpkCompGroup1Band7Fc		0xc82714
setSpkCompGroup1Band7Para2		0xc82715
getSpkCompCalNumPerFrame		0xa9d200
getSpkCompFilGroupNum		0xa9d100
getSpkCompChanFilInfo		0x882705
getSpkCompFiltCoefPtr		0x882706
getSpkCompGroup1BandNum		0x882707
getSpkCompGroup1Band1Fc		0x882708+0x000000
getSpkCompGroup1Band1Para2		0x882708+0x000001
gotSpkCompGroup1Band1ParaChange		0x800000
getSpkCompGroup1BandMFc	M=1,2.....7; Default Fc(Hz): 32, 125, 250, 500, 1K, 4K, 16K;	0x882708+0x000002*(M-1)+0
getSpkCompGroup1BandMPara2		0x882708+0x000002*(M-1)+1
gotSpkCompGroup1BandMParaChange		0x800000
getSpkCompGroup1Band1Fc		0x882708
getSpkCompGroup1Band1Para2		0x882709
getSpkCompGroup1Band2Fc		0x88270a
getSpkCompGroup1Band2Para2		0x88270b
……		……
getSpkCompGroup1Band7Fc		0x882714
getSpkCompGroup1Band7Para2		0x882715

Table 6-32. Speaker Compensation Group1BandMPara2 Table

Bit	Description	
23	This bit represents the corresponding coefficients that should be updated. 0: No Update 1: Update	
22-19	Reserved.	
18	This bit represents filter function. It is NOT allowed to update on the fly. 0: Biquad (Single Precision); 1: Biquad2 (Mix Precision).	
17-16	Bit 16:17 has 4 values, 0,1,2 and 3. 00: Peak Filter 01: Shelving Filter 10: Reserved 11: Reserved	
15-7	Bit 7:15 represents Gain with 0.1 dB step, range from –15 dB to 15 dB.	
6-0	Peaking Filter	Bit 0:6 represents Q parameter with 0.1 step, range from 0.1 to 5.
	Shelving Filter	Bit 0:6 represents shelving filter type. 0: Low Frequency Shelving Filter 1: High Frequency Shelving Filter

For example:

1. Send command ‘$c82709 $804b32’ to set SpkCompGroup1Band1Para2, and the configuration is: Band1, Biquad1, Gain=15dB, Q=5;
2. Send command ‘$c82708 $3e8 ’ to set SpkCompGroup1Band1 filter Fc=100Hz, and then have to set the Band1’s Gain and Q to update the filter with new Fc, such as ‘$c82709 $804b05’;
3. Send command ‘$c82709 $813200’ to change the filter type into low frequency Shelving filter;
4. Send command ‘$c82709 $813201’ to change the filter type into high frequency Shelving filter;

6.12 Bass-Boost

The Bass-Boost PPP algorithm and characteristics are the same as PEQ PPP. However, the Bass-Boost has 1Group and 3Band, and it supports up to 8-channel processing in the default setting.

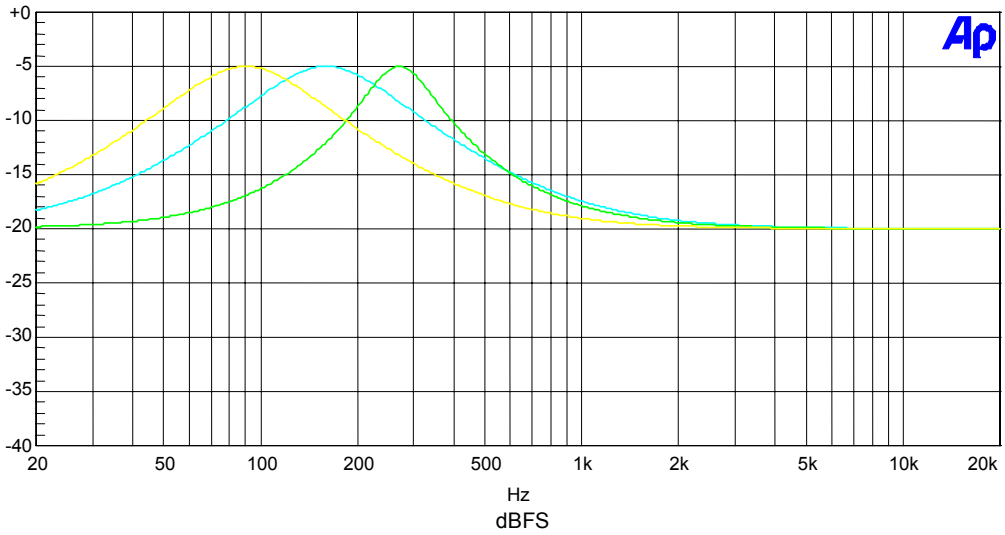


Figure 6-17. Fc (Hz)/Gain (dB)/Q=160/15/1, 270/15/2, 90/15/1

Table 6-33. Bass-Boost Configuration Register Symbolic Opcodes

Symbol	Description	Value
setBassBoostConfig		0xc82501
setBassBoostConfigMode		0xe94700
sotBitBassBoostConfigDisable	Disable Bass-Boost	0x000000
sotBitBassBoostConfigEnableCalc	Enable Bass-Boost	0x000003
sotBitBassBoostConfigEnableManual	Download Mode	0x000001
getBassBoostConfig	Report configuration register value	0x882501
getBassBoostConfigMode		0xa94700
gotBitBassBoostConfigEnableCalc		0x000003
gotBitBassBoostConfigEnableManual		0x000001
gotBitBassBoostConfigDisable		0x000000

Table 6-34. Bass-Boost Channel Mask Opcodes

Symbol	Description	Value
setBassBoostChannelMask	Enable Bass-Boost Channel Mask	0xe94600
sotBitBassBoostChannelMaskLch		0x000001
sotBitBassBoostChannelMaskRch		0x000002
sotBitBassBoostChannelMaskLsch		0x000004
sotBitBassBoostChannelMaskRsch		0x000008
sotBitBassBoostChannelMaskCch		0x000010
sotBitBassBoostChannelMaskSubch		0x000020
sotBitBassBoostChannelMaskLach		0x000040
sotBitBassBoostChannelMaskRach		0x000080
getBassBoostChannelMask	Report Channel Mask Register Value	0xa94600
gotBitBassBoostChannelMaskLch		0x000001
gotBitBassBoostChannelMaskRch		0x000002
gotBitBassBoostChannelMaskLsch		0x000004
gotBitBassBoostChannelMaskRsch		0x000008
gotBitBassBoostChannelMaskCch		0x000010
gotBitBassBoostChannelMaskSubch		0x000020
gotBitBassBoostChannelMaskRach		0x000040
gotBitSpkCompChannelMaskRach		0x000080
getBassBoostEffectChannelMask	Report Actual Channel Mask with Audio Mode	0xa94500
gotBitBassBoostEffectChannelMaskLch		0x000001
gotBitBassBoostEffectChannelMaskRch		0x000002
gotBitBassBoostEffectChannelMaskLsch		0x000004
gotBitBassBoostEffectChannelMaskRsch		0x000008
gotBitBassBoostEffectChannelMaskCch		0x000010
gotBitBassBoostEffectChannelMaskSubch		0x000020
gotBitBassBoostEffectChannelMaskLach		0x000040
gotBitBassBoostEffectChannelMaskRach		0x000080

For example:

1. Send command ‘$e94703’ to enable Bass-Boost PPP, and the default selected channel are Lf/Rf;
2. Send command ‘$e946ff ’ to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra;
3. Send command ‘$e94700’ to disable Bass-Boost PPP;

Table 6-35. Bass-Boost Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setBassBoostCalNumPerFrame		0xe952nn
setBassBoostGroup1Band1Para2	BassBoostGroup1BandMPara2 refers to Table 6-36.	0xc82508+0x000001
sotBassBoostGroup1Band1ParaChange		0x800000
SetBassBoostGroup1BandMPara2		0xc82508+0x000002*(M-1)+1
SotBassBoostGroup1BandMParaChange		0x800000
SetBassBoostGroup1Band1Para2		0xc82509
SetBassBoostGroup1Band2Para2		0xc8250b
SetBassBoostGroup1Band3Para2		0xc8250d
getBassBoostCalNumPerFrame		0xa95200
getBassBoostFilGroupNum		0xa95100
getBassBoostChanFilInfo		0x882505
getBassBoostFiltCoefPtr		0x882506
getBassBoostGroup1BandNum		0x882507
getBassBoostGroup1Band1Para2		0x882508+0x000001
gotBassBoostGroup1Band1ParaChange		0x800000
getBassBoostGroup1BandMPara2	M=1,2,3;	0x882508+0x000002*(M-1)+1
gotBassBoostGroup1BandMParaChange		0x800000
getBassBoostGroup1Band1Para2		0x882509
getBassBoostGroup1Band2Para2		0x88250b
getBassBoostGroup1Band3Para2		0x88250d

Table 6-36. Bass Boost Group1BandMPara2 Table

Bit	Description	
23	This bit represents the corresponding coefficients should be updated. 0: No Update 1: Update.	
22-19	Reserved.	
18	This bit represents filter function. It is NOT allowed to update on the fly. 0: Biquad (Single Precision) 1: Biquad2 (Mix Precision)	
17-16	Bit 16:17 has 4 values, 0,1,2 and 3. 00: Peak Filter 01: Shelving Filter 10: Reserved 11: Reserved	
15-7	Bit 7:15 represents Gain with 0.1dB step, range from –15dB to 15dB.	
6-0	Peaking Filter	Bit 0:6 represents Q parameter with 0.1 step, range from 0.1 to 5.
	Shelving Filter	Bit 0:6 represents shelving filter type. 0: Low Frequency Shelving Filter 1: High Frequency Shelving Filter

For example:

1. Send command ‘$c82509 $804b32’ to set BassBoostGroup1Band1Para2, and the configuration is: Band1, Biquad1, Gain=15dB, Q=5;
2. Send command ‘$c82509 $813200’ to change the filter type into low frequency Shelving filter;
3. Send command ‘$c82509 $813201’ to change the filter type into high frequency Shelving filter;

6.13 Bass Treble

The Bass Treble PPP algorithm and characteristics are the same as the PEQ PPP. However, the Bass Treble has 1Group and 2Band, and it supports up to 5-channel processing in the default setting.

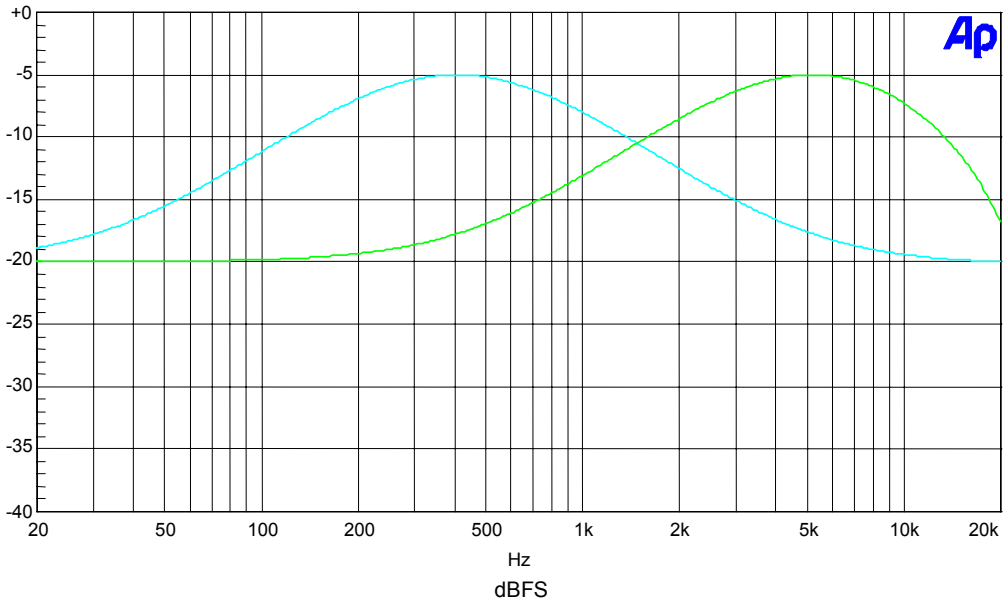


Figure 6-18. Fc (Hz)/Gain (dB)/Q=405/15/0.5 , 5.2k/15/0.5

Table 6-37. Bass Treble Configuration Register Symbolic Opcodes

Symbol	Description	Value
setBassTrebConfig		0xc82401
setBassTrebConfigMode		0xe90700
sotBitBassTrebConfigDisable	Disable Bass Treble	0x000000
sotBitBassTrebConfigEnableCalc	Enable Bass Treble	0x000003
sotBitBassTrebConfigEnableManual	Download Mode	0x000001
getBassTrebConfig	Report Configuration Register Value	0x882401
getBassTrebConfigMode		0xa90700
gotBitBassTrebConfigEnableCalc		0x000003
gotBitBassTrebConfigEnableManual		0x000001
gotBitBassTrebConfigDisable		0x000000

Table 6-38. Bass Treble Channel Mask Opcodes

Symbol	Description	Value
setBassTrebChannelMask	Enable Bass Treble Channel Mask	0xe90600
sotBitBassTrebChannelMaskLch		0x000001
sotBitBassTrebChannelMaskRch		0x000002
sotBitBassTrebChannelMaskLsch		0x000004
sotBitBassTrebChannelMaskRsch		0x000008
sotBitBassTrebChannelMaskCch		0x000010
sotBitBassTrebChannelMaskSubch		0x000020
sotBitBassTrebChannelMaskLach		0x000040
sotBitBassTrebChannelMaskRach		0x000080
getBassTrebChannelMask	Report Channel Mask Register Value	0xa90600
gotBitBassTrebChannelMaskLch		0x000001
gotBitBassTrebChannelMaskRch		0x000002
gotBitBassTrebChannelMaskLsch		0x000004
gotBitBassTrebChannelMaskRsch		0x000008
gotBitBassTrebChannelMaskCch		0x000010
gotBitBassTrebChannelMaskSubch		0x000020
gotBitBassTrebChannelMaskLach		0x000040
gotBitBassTrebChannelMaskRach		0x000080
getBassTrebEffectChannelMask	Report Actual Channel Mask with Audio Mode	0xa90500
gotBitBassTrebEffectChannelMaskLch		0x000001
gotBitBassTrebEffectChannelMaskRch		0x000002
gotBitBassTrebEffectChannelMaskLsch		0x000004
gotBitBassTrebEffectChannelMaskRsch		0x000008
gotBitBassTrebEffectChannelMaskCch		0x000010
gotBitBassTrebEffectChannelMaskSubch		0x000020
gotBitBassTrebEffectChannelMaskLach		0x000040
gotBitBassTrebEffectChannelMaskRach		0x000080

For example:

1. Send command ‘$e90703’ to enable Bass Treble PPP, and the default selected channel are Lf/Rf;
2. Send command ‘$e906ff ’ to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra;
3. Send command ‘$e90700’ to disable Bass Treble PPP;

Table 6-39. Bass Treble Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setBassTrebCalNumPerFrame		0xe912nn
setBassTrebGroup1Band1Para2	BassBoostGroup1BandMPara 2 refers to Table 6-40	0xc82408+0x000001
sotBassTrebGroup1Band1ParaChange		0x800000
setBassTrebGroup1BandMPara2		0xc82408+0x000002*(M-1)+1
sotBassTrebGroup1BandMParaChange		0x800000
setBassTrebGroup1Band1Para2		0xc82409
setBassTrebGroup1Band2Para2		0xc8240b
getBassTrebCalNumPerFrame		0xa91200
getBassTrebFilGroupNum		0xa91100
getBassTrebChanFilInfo		0x882405
getBassTrebFiltCoefPtr		0x882406
getBassTrebGroup1BandNum		0x882407
getBassTrebGroup1Band1Para2		0x882408+0x000001
gotBassTrebGroup1Band1ParaChange		0x800000
getBassTrebGroupNBandMPara2	M=1,2	0x882408+0x000002*(M-1)+1
gotBassTrebGroupNBandMParaChange		0x800000
getBassTrebGroup1Band1Para2		0x882409
getBassTrebGroup1Band2Para2		0x88240b

Table 6-40. Bass Treble Group1BandMPara2 Table

Bit	Description	
23	This bit represents the corresponding coefficients should be updated. 0: No Update 1: Update	
22-19	Reserved.	
18	This bit represents filter function. It is NOT allowed to update on the fly. 0: Biquad (Single Precision) 1: Biquad2 (Mix Precision).	
17-16	Bit 16:17 has 4 values, 0,1,2 and 3. 00: Peak Filter 01: Shelving Filter 10: Reserved 11: Reserved	
15-7	Bit 7:15 represents Gain with 0.1dB step, range from –15dB to 15dB.	
6-0	Peaking Filter	Bit 0:6 represents Q parameter with 0.1 step, range from 0.1 to 5.
	Shelving Filter	Bit 0:6 represents shelving filter type. 0: Low Frequency Shelving Filter 1: High Frequency Shelving Filter

For example:

1. Send command ‘$c82409 $814b32’ to set BassTrebGroup1Band1Para2, and the configuration is: Band1, Biquad2, Gain=15dB, Q=5;
2. Send command ‘$c82409 $813200’ to change the filter type into low frequency Shelving filter;
3. Send command ‘$c82409 $813201’ to change the filter type into high frequency Shelving filter;

6.14 Pause Detection

This PPP detects the absence of input audio data for 3 seconds. A Boolean flag represents the status whether music is absent or not.

If the value of the input data is bigger than the threshold, the music is considered to be present. If the value of the input data is less than the threshold for more than 3 seconds, the music is considered to be absent. The threshold is programmed and can be changed on the fly.

Table 6-41. Pause Detection Configuration Register Symbolic Opcodes

Symbol	Description	Value
setPauseDetectorConfig		0xc81d01
sotPauseDetectorConfigDisable	Disable Pause Detection	0x000000
sotPauseDetectorConfigEnable	Enable Pause Detection	0x000001
setPauseDetectorThreshold	Set Threshold	0xc81d03
getNoMusicFlag	Get No Music Flag	0x881d02
gotBitMusicPresent		0x000000
gotBitMusicAbsent		0x000001

For example:

1. Send command ‘$c81d01 $1’ to enable Pause Detection PPP;
2. Send command ‘$c81d03 $732ae ’ to set the threshold=0.05623413251903 (-25dB);
3. Send command ‘$c81d01 $0’ to disable Pause Detection PPP;

6.15 Spectrum Analyzer

The Spectrum Analyzer PPP calculates the levels of 13 Fc. The 13 Fc are fixed, at 63 Hz, 100 Hz, 160 Hz, 250 Hz, 400 Hz, 630 Hz, 1000 Hz, 1600 Hz, 2500 Hz, 4000 Hz, 6300 Hz, 10000 Hz, 16000Hz. These frequencies are supported for 32kHz, 44.1kHz, 48 kHz, 88.2kHz, and 96 kHz sample rates.

The Spectrum Analyzer PPP output range is from 0 to 64, which represents the input level.

Table 6-42. Spectrum Analyzer Configuration Register Symbolic Opcodes

Symbol	Description	Value
setSpectrumConfig		0xc81f01
sotBitSpectrumConfigDisable	Disable Spectrum Analyzer	0x000000
sotBitSpectrumConfigEnable	Enable Spectrum Analyzer	0x000001
getSpectrumConfig	Report configuration register value.	0x881f01
gotBitSpectrumConfigDisable		0x000000
gotBitSpectrumConfigEnable		0x000001

Table 6-43. Spectrum Analyzer Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setSpectrumPeakHoldPeriod		0xc81f03
setSpectrumReleaseTime		0xc81f11
setSpectrumBand1Fc		0xc81f04
setSpectrumBand2Fc		0xc81f05
setSpectrumBand3Fc		0xc81f06
setSpectrumBand4Fc		0xc81f07
setSpectrumBand5Fc		0xc81f08
setSpectrumBand6Fc		0xc81f09
setSpectrumBand7Fc		0xc81f0a
setSpectrumBand8Fc		0xc81f0b
setSpectrumBand9Fc		0xc81f0c
setSpectrumBand10Fc		0xc81f0d
setSpectrumBand11Fc		0xc81f0e
setSpectrumBand12Fc		0xc81f0f
setSpectrumBand13Fc		0xc81f10
getSpectrumPeakHoldPeriod		0x881f03
getSpectrumReleaseTime		0x881f11
getPointerofPeakHold		0x881f16
getSpectrumBand1Fc		0x881f04
getSpectrumBand2Fc		0x881f05
getSpectrumBand3Fc		0x881f06
getSpectrumBand4Fc		0x881f07
getSpectrumBand5Fc		0x881f08
getSpectrumBand6Fc		0x881f09
getSpectrumBand7Fc		0x881f0a
getSpectrumBand8Fc		0x881f0b
getSpectrumBand9Fc		0x881f0c
getSpectrumBand10Fc		0x881f0d
getSpectrumBand11Fc		0x881f0e
getSpectrumBand12Fc		0x881f0f
getSpectrumBand13Fc		0x881f10

For example:

1. Send command ‘$c81f01 $1’ to enable Spectrum Analyzer PPP;
2. Send command ‘$881f16 $0 ’ to get pointer to peak hold data;
3. Send command ‘$c81f06 $2710’ to set Band3 peak will be the highest level, and $2710 represents 1kHz;
4. Send command ‘$c81f06 $0’ to disable Spectrum Analyzer PPP;

6.16 Tone Control

The Tone Control PPP provides Bass band, Mid band and Treble band tone control processing in a multiple channel system. Tone Control provides up to 8-channel processing in Bass band, and up to 7 channels (without Subwoofer) in the Mid and Treble bands. Default filter parameters are as follows:

Band	Filter Type	Fc	Gain	Q
Bass	Peaking	1000Hz	0 (+/- 15 dB in 0.1dB step)	10 (0.5~5 in 0.1 step)
Mid	Peaking	10kHz	0 (+/- 15 dB in 0.1dB step)	10 (0.5~5 in 0.1 step)
Treble	Shelving	50kHz	0 (+/- 20 dB in 0.1dB step)	N/A

Table 6-44. Tone Control Configuration Register Symbolic Opcodes

Symbol	Description	Value
setCoeffBassPeakChange	Update Bass Band Coefficients	0xe68101
setCoeffMidPeakChange	Update Mid Band Coefficients	0xe68102
setCoeffTrebleChange	Update Treble Band Coefficients	0xe68104
setBassPeakGain	Gain of Bass Band	0xc81a03
setMidPeakGain	Gain of Mid Band	0xc81a06
setTrebleGain	Gain of Treble Band	0xc81a09

Table 6-45. Tone Control Channel Mask Configuration Symbolic Opcodes

Symbol	Description	Value
setChannelMask		0xc81a01
sotBitToneControlConfigDisable	PPP is Not Active	0x000000
sotBitToneControlChannelMaskLch		0x000001
sotBitToneControlChannelMaskRch		0x000002
sotBitToneControlChannelMaskLsch		0x000004
sotBitToneControlChannelMaskRsch		0x000008
sotBitToneControlChannelMaskCch		0x000010
sotBitToneControlChannelMaskSubch		0x000020
sotBitToneControlChannelMaskLach		0x000040
sotBitToneControlChannelMaskRach		0x000080
getChannelMask	Report Channel Mask Register Value.	0x881a01
gotBitToneControlConfigDisable		0x000000
gotBitToneControlChannelMaskLch		0x000001
gotBitToneControlChannelMaskRch		0x000002
gotBitToneControlChannelMaskLsch		0x000004
gotBitToneControlChannelMaskRsch		0x000008
gotBitToneControlChannelMaskCch		0x000010
gotBitToneControlChannelMaskSubch		0x000020
gotBitToneControlChannelMaskLach		0x000040
gotBitToneControlChannelMaskRach		0x000080

To use Tone Control PPP, follow the steps:

1. Use the channel mask command to enable the selected channel;
2. Use the Gain command of Bass/Mid/Treble band filter. After update the parameters, use '$e68101' to enable Bass band filter setting, '$e68102' to enable Mid band filter setting, '$e68104' to enable Treble band filter setting.

For example:

1. Send command '$c81a01 $ff' to enable Tone Control PPP on 4 pair of channel: Lf/Rf, Ls/Rs, C/Sub, La/Ra;
2. Send command '$c81a03 $96 ', '$e68101' to set the Gain of Bass Band filter 15dB;
3. Send command '$c81a06 $96', '$e68102' to set the Gain of Mid Band filter 15dB;
4. Send command '$c81a01 $0' to disable Tone Control PPP;

6.17 Fade Balance

The Fade Balance PPP provides fade/balance for up to 8 channels. It provides 8 independent volume controls. Each channel's volume change will take effect in fading effect. The fading time can be controlled by modifying the delay frame number.

Table 6-46. Fade Balance Configuration Register Symbolic Opcodes

Symbol	Description	Value
setFadeBalaneConfig		0xc83e01
sotBitFadeBalanceDisable	Disable Fade Balance PPP.	0x000000
sotBitFadeBalanceEnable	Enable Fade Balance PPP.	0x000001
setFadeFrameNumber	FrameNum >=0	0xc83e02

Table 6-47. Fade Balance Gain Configuration Symbolic Opcodes

Symbol	Description	Value
setTotalGain	Set Channel Gain (dB) Unit: Linear 1.	0xc83e03
setLeftGain		0xc83e04
setRghtGain		0xc83e05
setLSurGain		0xc83e06
setRSurGain		0xc83e07
setCntrGain		0xc83e08
setSubwGain		0xc83e09
setLAuxGain		0xc83e0a
setRAuxGain		0xc83e0b
getLeftGain	Get Current Gain Value	0x883e14
getRghtGain		0x883e15
getLSurGain		0x883e16
getRSurGain		0x883e17
getCntrGain		0x883e18
getSubwGain		0x883e19
getLAuxGain		0x883e1a
getRAuxGain		0x883e1b

For example:

1. Send command '$c83e01 $1' to enable Fade Balance PPP;

2. Send command ‘$c83e03 $400000 ’ to set the Gain of total 4 pair of channel down 6dB;
3. Send command ‘$c83e04 $400000 ’ to set the Gain of Lf channel down 6dB;
4. Send command ‘$c83e02 $41’ to set the fading time to 65 frame;
5. Send command ‘$c83e01 $0’ to disable the Fade Balance PPP;

6.18 Prescaler

The Prescale PPP provides 8-channel independent volume controls for scaling the input.

Table 6-48. Prescaler Configuration Register Symbolic Opcodes

Symbol	Description	Value
setPreScalerConfig		0xc81b01
sotBitPreScalerDisable	Disable Prescaler PPP.	0x000000
sotBitPreScalerEnable	Enable Prescaler PPP.	0x000001
setFadeFrameNumber	FrameNum >=0	0xc81b02

Table 6-49. Prescaler Gain Configuration Symbolic Opcodes

Symbol	Description	Value
setLeftGain	Set Channel Gain (dB) Unit: Linear 0.5.	0xc81b03
setRghtGain		0xc81b04
setLSurGain		0xc81b05
setRSurGain		0xc81b06
setCntrGain		0xc81b07
setSubwGain		0xc81b08
setLAuxGain		0xc81b09
setRAuxGain		0xc81b0a
getLeftGain	Get Current Gain Value	0x881b13
getRghtGain		0x881b14
getLSurGain		0x881b15
getRSurGain		0x881b16
getCntrGain		0x881b17
getSubwGain		0x881b18
getLAuxGain		0x881b19
getRAuxGain		0x881b1a

For example:

1. Send command ‘$c81b01 $1’ to enable Prescaler PPP;
2. Send command ‘$c81b03 $200000’ to set the Gain of Lf channel down 6dB;
3. Send command ‘$c81b01 $0’ to disable the Prescaler PPP;

6.19 Level Meter

The Level Meter PPP calculates each channel’s level. It performs a mean calculation on the absolute value of one block of samples.

Table 6-50. Level Meter Configuration Register Symbolic Opcodes

Symbol	Description	Value
setLevelConfig		0xc83f01
sotBitDisbableLevel	Disable Level Meter PPP	0x000000
sotBitEnableLevel	Enable Level Meter PPP	0x000001

Table 6-51. Level Meter Level Configuration Symbolic Opcodes

Symbol	Description	Value
getLeftLevel	Get Current Output Level; Range is From FFFFDC to FFFFFE FFFFDC: Minimum Input 000001. FFFFFE: Maximum Input 7FFFFF 800000: No Input	0x883f02
getRghtLevel		0x883f03
getLSurLevel		0x883f04
getRSurLevel		0x883f05
getCntrLevel		0x883f06
getSubwLevel		0x883f07
getLAuxLevel		0x883f08
getRAuxLevel		0x883f09

For example:

1. Send command '$c83f01 $1' to enable Level Meter PPP;
2. Send command '$883f02 $0 ' to get the Level word Lf channel;
3. Send command '$c83f01 $0' to disable the Level Meter PPP;

6.20 Beep

The Beep PPP generates one or two single sine tones and mixes them to the specified channel. No more than 2 tones may be generated simultaneously and the specified channel can be all channels except subwoofer. Beep provides two modes with linear/log attack & release according to input parameters: Single Beep or Double Beep (includes chord and rectangle), refer to Table 6-53. All input parameters must meet the following limitations.

- Beep type = 0: linear attack & release

  = 1: log attack & release
- Frequency: positive integer, range from 1Hz to SampleRate/2.
- Amplitude: range from 0 to 0.99999988 (1- 2^{-23}).
- Period number: positive integer.
- All time parameters: positive integer in millisecond (ms). Following figure specifies time parameters.

Period time: ranges from 0 ms to 8388 ms, and Period > (On time + Release time)

In linear type:

On time > Attack time

In log type

$$Ontime > \frac{Attacktime \times 9}{10^{0.63} - 1} + \frac{Releasetime \times 10^{0.63}}{10 - 10^{0.63}}$$

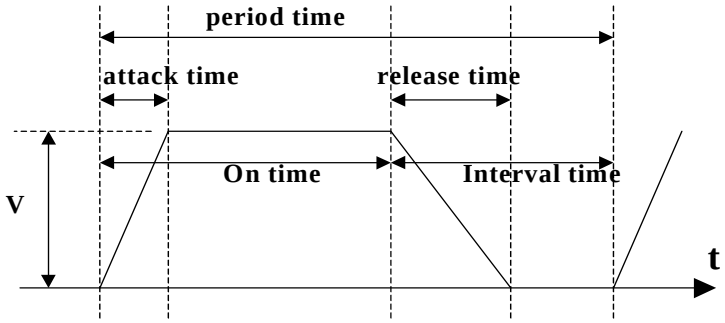


Figure 6-19. Linear Attack & Release for Beep Generator

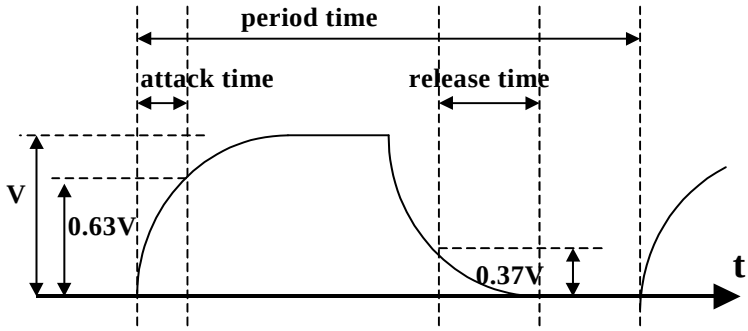


Figure 6-20. Log Attack & Release for Beep Generator

The Beep PPP generates one or double single sine tones and mixes them to specified channel.

- Support two Beep types: linear and log attack & release.
- Support controls of which channel will be mixed with beep.
- Support controls of the numbers of period.
- Support controls of the first and second frequency of generated beep.
- Support controls of the amplitude of first frequency and the second.
- Support controls of the size of attack time 1 and 2.
- Support controls of the size of release time 1 and 2.
- Support controls of the size of on frequency time 1 and 2.
- Only default configurations are provided in ROM, it can be changed by uC or boot-loader.
- Support controls of the size of Period time of the first and second frequency in ms.

Table 6-52. Beep Mode Configuration Table

Beep Mode / Parameters	Single Beep	Double Beep	
		Chord	Rectangle (Double Sequence)
BeepTypeLinear	Yes	Yes	Yes
BeepTypeLogarithm	Yes	Yes	Yes
BeepPeriodNum	Yes	Yes	Yes
BeepFrequency1	Yes	Yes	Yes
BeepFrequency2	N/A	Yes	Yes
BeepAmplitude1	Yes	Yes	Yes
BeepAmplitude2	N/A	Yes	Yes
BeepAttack1	Yes	Yes	Yes

Table 6-52. Beep Mode Configuration Table

BeepAttack2	N/A	N/A	Yes
BeepRelease1	Yes	Yes	Yes
BeepRelease2	N/A	N/A	Yes
BeepOnTime1	Yes	Yes	Yes
BeepOnTime2	N/A	N/A	Yes
BeepPeriod1	Yes	Yes	Yes
BeepPeriod2	N/A	N/A	Yes

Table 6-53. Beep Configuration Register Symbolic Opcodes

Symbol	Description	Value
setBeepConfig		0xc82e01
sotBitBeepConfigDisable	Disable Beep	0x000000
sotBitBeepConfigEnable	Enable Beep	0x000001
getBeepConfig	Report Configuration Register Value	0x882e01
gotBitBeepConfigDisable		0x000000
gotBitBeepConfigEnable		0x000001

Table 6-54. Beep Channel Mask Opcodes

Symbol	Description	Value
setBeepChannelMask	Enable Beep Channel Mask	0xc82e03
sotBitBeepChannelMaskLch		0x000001
sotBitBeepChannelMaskRch		0x000002
sotBitBeepChannelMaskLsch		0x000004
sotBitBeepChannelMaskRsch		0x000008
sotBitBeepChannelMaskCch		0x000010
sotBitBeepChannelMaskSubch		0x000020
sotBitBeepChannelMaskLach		0x000040
sotBitBeepChannelMaskRach		0x000080
getBeepChannelMask	Report Channel Mask Register Value	0x882e03
gotBitBeepChannelMaskLch		0x000001
gotBitBeepChannelMaskRch		0x000002
gotBitBeepChannelMaskLsch		0x000004
gotBitBeepChannelMaskRsch		0x000008
gotBitBeepChannelMaskCch		0x000010
gotBitBeepChannelMaskSubch		0x000020
gotBitBeepChannelMaskLach		0x000040
gotBitBeepChannelMaskRach		0x000080

For example:

1. Send command ‘$c82e01 $1’ to enable Beep PPP, and the default selected channel are Lf/Rf;
2. Send command ‘$c82e03 $ff ’ to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra;
3. Send command ‘$c82e01 $0’ to disable Beep PPP

Table 6-55. Beep Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setBeepType	Set the Beep's Type	0xc82e04
sotBitBeepTypeLinear		0x000000
sotBitBeepTypeLogarithm		0x000001
getBeepType	Get the Beep's Type	0x882e04
gotBitBeepTypeLinear		0x000000
gotBitBeepTypeLogarithm		0x000001
setBeepPeriodNum	Set the Beep's Period Number	0xc82e05
getBeepPeriodNum	Get the Beep's Period Number	0x882e05
setBeepFrequency1	Unit: 1 Hz	0xc82e06
setBeepFrequency2	Unit: 1 Hz	0xc82e07
setBeepAmplitude1	Unit: Linear Value	0xc82e08
setBeepAmplitude2	Unit: Linear Value	0xc82e09
setBeepAttack1	Unit: 1 ms.	0xc82e0e
setBeepAttack2	Unit: 1 ms.	0xc82e0f
setBeepRelease1	Unit: 1 ms.	0xc82e10
setBeepRelease2	Unit: 1 ms.	0xc82e11
setBeepOnTime1	Unit: 1 ms.	0xc82e12
setBeepOnTime2	Unit: 1 ms.	0xc82e13
setBeepPeriod1	Unit: 1 ms.	0xc82e14
setBeepPeriod2	Unit: 1 ms.	0xc82e15
setBeepStart		0xc82e02
sotBitBeepStart_1		0x000001

In order to repeat Beep, the user must set the Beep configuration again and use the command ' c82e02 $1' to enable Beep every time.

For example:

1. Send command '$c82e05 $20 ' to set Beep's period number=20;
2. Send command '$c82e06 $3e8' to set Beep's frequency1=1kHz;
3. Send command '$c82e07 $320' to set Beep's frequency2=800Hz;
4. Send command '$c82e08 $266666' to set Beep's amplitude1=0.3;
5. Send command '$c82e09 $199999' to set Beep's amplitude 2=0.2;
6. Send command '$c82e0e $32' to set Beep's attack time1=50ms;
7. Send command '$c82e0f $0' to set Beep's attack time2=0ms;
8. Send command '$c82e10 $46' to set Beep's release time1=70ms;
9. Send command '$c82e11 $0' to set Beep's release time2=0ms;
10. Send command '$c82e12 $258' to set Beep's on time1=600ms;
11. Send command '$c82e13 $0' to set Beep's on time2=0ms;
12. Send command '$c82e14 $320' to set Beep's period time1=800ms;
13. Send command '$c82e15 $320' to set Beep's period time2=800ms;
14. Send command '$c82e04 $0' to set Beep's linear mode;
15. Send command '$c82e03 $ff' to enable Beep's all channel output;
16. Send command '$c82e02 $1' to start Beep;

6.21 Chime

The Chime PPP generates a single or double frequency tone according to the input parameters, then mixes them to the specified channel. All input parameters should obey the following limitations.

- Chime type: Low Decay Mode or Fast Decay Mode.
- Frequency: positive integer, range from 1Hz to Sample Rate/2.
- Amplitude: range from 0 to 0.99999988 ($1-2^{23}$).
- Period number: positive integer.
- All time parameters: positive integer, range from 0 to 8,000,000 microseconds (us).

$$Tdf = \frac{Td \times 8}{3}$$

Tsh +Tdf + Trel < 8000000 and Tsh + Tsl < 8000000, where .

Time parameters are specified by the following figures.

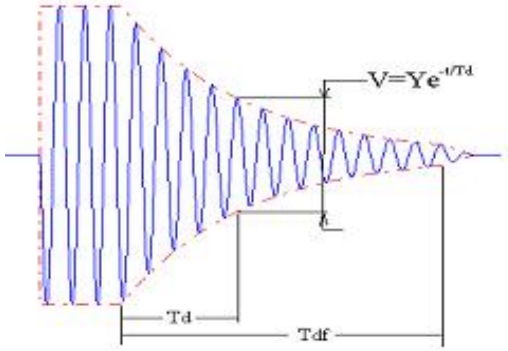


Figure 6-21. Single Chime

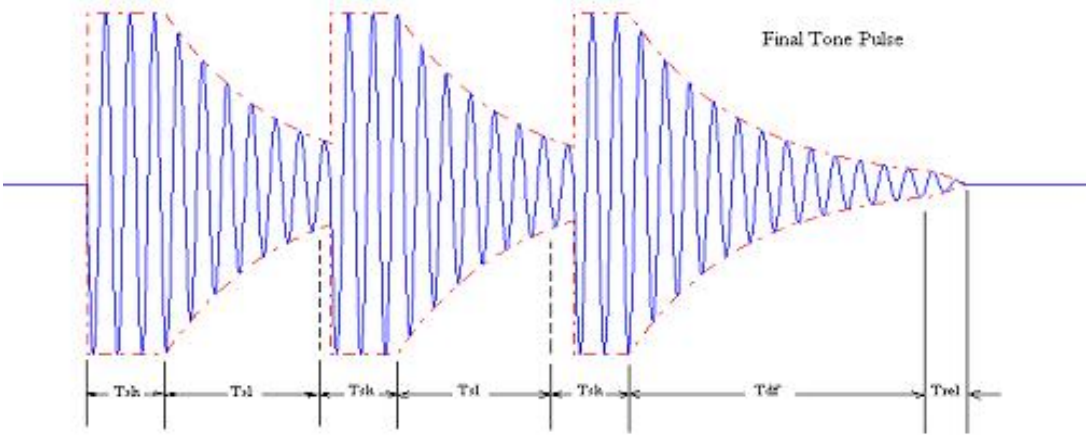


Figure 6-22. Chime with Slow Decay

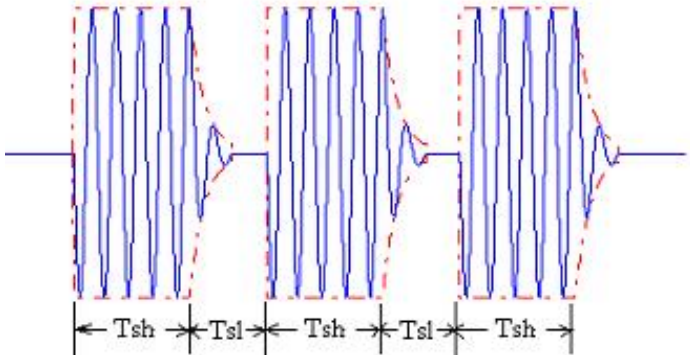


Figure 6-23. Chime with Fast Decay

- Support controls of the channel, which will be mixed with Chime.
- Support controls of the numbers of period
- Support two chime types: low or fast decay rate.
- Support controls of both the first and the second frequency of generated Chime.
- Support controls of the amplitude of both the first and second frequency.
- Support controls of the size of on time.
- Support controls of the size of repetition rate/off time.
- Support controls of the size of decay rate.
- Support controls of the size of decay release time when type is low decay mode.

Table 6-56. Chime Configuration Register Symbolic Opcodes

Symbol	Description	Value
setChimeConfig		0xc82a01
sotBitChimeConfigDisable	Disable Chime.	0x000000
sotBitChimeConfigEnable	Enable Chime	0x000001
getChimeConfig	Report Configuration Register Value	0x882a01
gotBitChimeConfigDisable		0x000000
gotBitChimeConfigEnable		0x000001

Table 6-57. Chime Channel Mask Opcodes

Symbol	Description	Value
setChimeChannelMask	Enable Chime Channel Mask	0xc82a03
sotBitChimeChannelMaskLch		0x000001
sotBitChimeChannelMaskRch		0x000002
sotBitChimeChannelMaskLach		0x000004
sotBitChimeChannelMaskRsch		0x000008
sotBitChimeChannelMaskCch		0x000010
sotBitChimeChannelMaskSubch		0x000020
sotBitChimeChannelMaskLach		0x000040
sotBitChimeChannelMaskRach		0x000080
getChimeChannelMask	Report Channel Mask Register Value	0x882a03

Table 6-57. Chime Channel Mask Opcodes

gotBitChimeChannelMaskLch		0x000001
gotBitChimeChannelMaskRch		0x000002
gotBitChimeChannelMaskLsch		0x000004
gotBitChimeChannelMaskRsch		0x000008
gotBitChimeChannelMaskCch		0x000010
gotBitChimeChannelMaskSubch		0x000020
gotBitChimeChannelMaskLach		0x000040
gotBitChimeChannelMaskRach		0x000080

For example:

1. Send command '$c82a01 $1' to enable Chime PPP, and the default selected channel are Lf/Rf;
2. Send command '$c82a03 $ff ' to select 4 pair of channel, Lf/Rf, Ls/Rs, Cntr/Sub, La/Ra;
3. Send command '$c82a01 $0' to disable Chime PPP;

Table 6-58. Chime Parameter Configuration Symbolic Opcodes

Symbol	Description	Value
setChimeType	Set the Chime's Type	0xc82a05
sotBitChimeTypeLowDecay		0x000000
sotBitChimeTypeFastDecay		0x000001
getChimeType	Get the Chime's Type	0x882a05
gotBitChimeTypeLowDecay		0x000000
gotBitChimeTypeFastDecay		0x000001
setChimePeriodNum	Set the Chime's Period Number	0xc82a04
getChimePeriodNum	Get the Chime's Period Number	0x882a04
setChimeFrequency1	Unit: 1 Hz	0xc82a06
setChimeFrequency2	Unit: 1 Hz	0xc82a07
setChimeAmplitude1	Unit: Linear Value	0xc82a08
setChimeAmplitude2	Unit: Linear Value	0xc82a09
setChimeTsh	Unit: 1 us	0xc82a0a
setChimeTsl	Unit: 1 us	0xc82a0b
setChimeTd	Unit: 1 us	0xc82a0c
setChimeTrel	Unit: 1 us	0xc82a0d
setChimeStart		0xc82a02
sotBitChimeStart_1		0x000001

In order to repeat Chime, you must set the Chime configuration again and use the command ' c82a02 $1' to enable Chime every time.

For example:

1. Send command '$c82a04 $20 ' to set Chime's period number=20;
2. Send command '$c82a06 $3e8' to set Chime's frequency1=1kHz;
3. Send command '$c82a07 $320' to set Chime's frequency2=800Hz;
4. Send command '$c82a08 $266666' to set Chime's amplitude1=0.3;

5. Send command ‘$c82a09 $199999’ to set Chime’s amplitude 2=0.2;
6. Send command ‘$c82a05 $0’ to set Chime’s low decay mode;
7. Send command ‘$c82a03 $ff’ to enable Chime’s all channel output;
8. Send command ‘$c82a02 $1’ to start Chime;

Chapter 7
Input and Output Drivers

The DSPB56374 provides several input and output drivers to support multiple interfaces and allows the user to map different pins to different channels.

Three input functions are supported:

- Multi-channel input driver support: 2 channel, 6 channel and 2 channel + 2 channel input driver in synchronous mode.
- 8 channel multiplexed.
- 8 channel multi-chip protocol.

Details of pin and I/O buffer refer to Table 7-1.

Table 7-1. DSPB56374 Input Driver Configuration

Input Driver	Pin	Corresponding I/O buffer
2ch	SDI0	Lf/Rf buffer
4ch	SDI0& SDI1	Lf/Rf & Ls/Rs buffer
6ch	SDI0& SDI1& SDI2	Lf/Rf & Ls/Rs & Cntr/Sub buffer
8ch	SDI0& SDI1& SDI2& SDI0_1	Lf/Rf & Ls/Rs & Cntr/Sub & La/Ra buffer
8ch - TDM	SDI0	Lf/Rf & Ls/Rs & Cntr/Sub & La/Ra buffer

Three output functions are supported:

- Multi-channel output driver supports 2 channel, 4 channel, 6 channel and 8 channel Output.
- 8 channel multiplexed.
- 8 channel multi-chip protocol.

Details of pin an I/O buffer refers to Table 7-2.

Table 7-2. DSPB56374 Output Driver Configuration

Output driver	Pin	Corresponding I/O buffer
2ch	SDO0	Lf/Rf buffer
4ch	SDO0& SDO1	Lf/Rf & Ls/Rs buffer
6ch	SDO0& SDO1& SDO2	Lf/Rf & Ls/Rs & Cntr/Sub buffer
8ch	SDO0& SDO1& SDO2& SDO0_1	Lf/Rf & Ls/Rs & Cntr/Sub & La/Ra buffer
8ch -TDM	SDO0	Lf/Rf & Ls/Rs & Cntr/Sub & La/Ra buffer

Chapter 8
GPIO Mode

The DSPB56374 provides LTH GPIO Mode.

Table 8-1. DSPB56374 LTH GPIO Mode

Logic Signal	Physic Signal	Direction (I/O)
Comm In 0	PG0	Input
Comm In 1	PG1	Input
Comm Out 0	PG2	Output
Comm Out 1	PG3	Output
Lock	PG4	Input
Mute	PG5	Output
Single/Double Speed	PG6	Output
Unused	PG7~PG10	

Commands to enable/disable GPIO Modes.

Appendix A
Memory Maps

A.1 Red HLX Memory Map

X Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$0001E5	$0001EF	11	unused
$0001F1	$00017FF	5647	unused

Y Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$00031C	$00039B	128	unused
$0003DC	$0007EC	1041	unused
$00080A	$0011FF	2550	unused

P Memory

START	END	LENGTH	SECTION
$0001E0	$0017FF	5664	unused

A.2 Blue HLX Memory Map

X Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$0001E5	$0001EF	11	unused
$0003F1	$0005FF	527	unused
$0007E0	$0007FF	32	unused
$000DA0	$000FFF	608	unused
$0015A0	$0017FF	608	unused

Y Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$00031C	$00039B	128	unused
$0004AE	$00067F	466	unused
$000783	$000783	1	unused
$00079C	$0007EC	81	unused
$000A9F	$000B47	169	unused
$000D42	$0011FF	1214	unused

P Memory

START	END	LENGTH	SECTION
$0001E0	$0017FF	5664	unused

A.3 Green HLX Memory Map

X Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$0001E5	$0001EF	11	unused
$0003F1	$0005FF	527	unused
$0007E0	$0007FF	32	unused
$000DA0	$000FFF	608	unused
$0015A0	$0017FF	608	unused

Y Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$00031C	$00039B	128	unused
$0004AE	$0004B7	10	unused
$0004F8	$00067F	392	unused
$000783	$000783	1	unused
$00079C	$0007EC	81	unused
$000D42	$0011FF	1214	unused

P Memory

START	END	LENGTH	SECTION
$0001E0	$0017FF	5664	unused

A.4 Orange HLX Memory Map

X Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$0001E5	$0001EF	11	unused
$000269	$0002CC	100	unused
$0003B9	$0005FF	583	unused
$0007E0	$0007FF	32	unused
$000DA0	$000FFF	608	unused
$0015A0	$0017FF	608	unused

Y Memory

START	END	LENGTH	SECTION
$000000	$0000FF	256	scratch
$00031C	$00039B	128	unused
$000459	$000471	25	unused
$0004A4	$0007EC	841	unused
$0009E4	$000B47	356	unused
$000D42	$0011FF	1214	unused

P Memory

START	END	LENGTH	SECTION
$0001E0	$0017FF	5664	unused

A.5 *Default PPP Memory Map*

X Memory

PPP	START	END	LENGTH
PEQ	$0001F1	$000268	120
GEQ	$000269	$0002CC	100
Speaker Compensation	$0002CD	$000358	140
Bass Boost	$000359	$0003B8	96
Bass Treble	$0003B9	$0003F0	56
DLM	$000600	$0007DF	480
Resend	$000800	$000D9F	1440
Resend	$001000	$00159F	1440

Y Memory

PPP	START	END	LENGTH
PEQ	X:$0001F1	X:$000268	120
Resend	Y:$0003DC	Y:$000458	125
GEQ	X:$000269	X:$0002CC	100
Resend	Y:$000459	Y:$000471	25
Speaker Compensation	X:$0002CD	X:$000358	140
Resend	Y:$000472	Y:$000494	35
Bass Boost	X:$000359	X:$0003B8	96
Resend	Y:$000495	Y:$0004A3	15
Bass Treble	X:$0003B9	X:$0003F0	56
Resend	Y:$0004A4	Y:$0004AD	10
DLM	X:$000600	X:$0007DF	480
Resend	X:$000800	X:$000D9F	1440
Resend	X:$001000	X:$00159F	1440
Beep	Y:$0004B8	Y:$0004F7	64
Tone Control	Y:$000680	Y:$0006E6	103
Spectrum Analyzer	Y:$0006E7	Y:$000782	156
De-emphasis & DC-Cut	Y:$000784	Y:$00079B	24
Loudness	Y:$000B48	Y:$000D41	506
SWM	Y:$00039C	Y:$0003DB	64
*Pause Decoder	*	*	*
*Compression	*	*	*

*DRC	*	*	*
*Fade Balance	*	*	*
*Pre-Scaler	*	*	*
*Gain	*	*	*
*Level Meter	*	*	*
*Chime	*	*	*
*Volum	*	*	*

Note: *A small quantity of memory is used by these PPPs as control block. As the part of SA, reclamation of PPP control block is not allowed.

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