

MC9S08PL60 Series Family Product Brief

Contents

1 Application examples

These are general-purpose devices suitable for a wide range of applications:

- Handheld devices
- Sensing systems
- Human input devices
- Large appliances
- Industrial control
- Small appliances
- Key pads
- Power tools
- Personal care appliance
- Electric Motor
- Remote control
- Low-end meter
- UPS
- Battery chargers
- HVAC
- Smart circuit breakers

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2 Features

2.1 Introduction

These device series are members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 central processor unit and are available with a variety of modules, memory sizes and types, and package types. The following table summarizes the peripheral availability per package type for the devices available.

Table 1. Memory and package availability

Feature	MC9S08PL60	MC9S08PL32
Flash size (bytes)	60,864	32,768
EEPROM size (bytes)	256	256
RAM size (bytes)	4,096	4,096
LQFP-64	Yes	Yes
QFP-64	Yes	Yes
LQFP-48	Yes	Yes
QFN-48	Yes	Yes
LQFP-44	Yes	Yes
LQFP-32	Yes	Yes

Table 2. Feature availability

Pin number	64-pin	48-pin	44-pin	32-pin
Bus frequency (MHz)	10	10	10	10
IRQ	Yes			
WDOG	Yes			
DBG	Yes			
IPC	Yes			
ICS	Yes			
XOSC	Yes			
RTC	Yes			
FTM0 channels	2-ch	2-ch	2-ch	2-ch
FTM1 channels	2-ch	2-ch	2-ch	2-ch
FTM2 channels	6-ch	6-ch	6-ch	6-ch
MTIM0	Yes			
MTIM1	Yes			

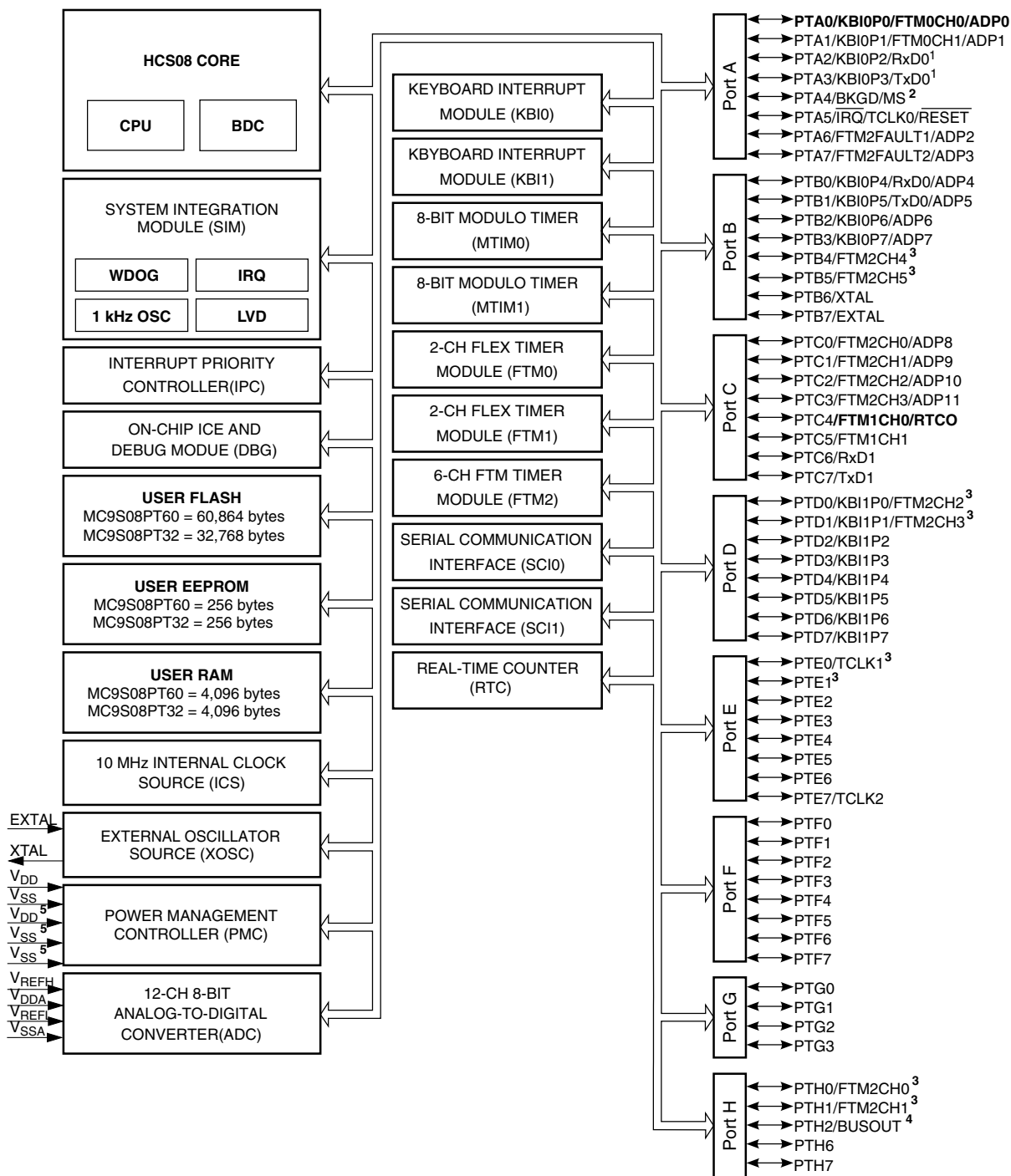
Table continues on the next page...

Table 2. Feature availability (continued)

Pin number	64-pin	48-pin	44-pin	32-pin
SCI0	Yes			
SCI1	Yes			
ADC channels	12	12	12	12
KBI pins	16	16	12	12
GPIO	57	41	37	30

2.2 MCU block diagram

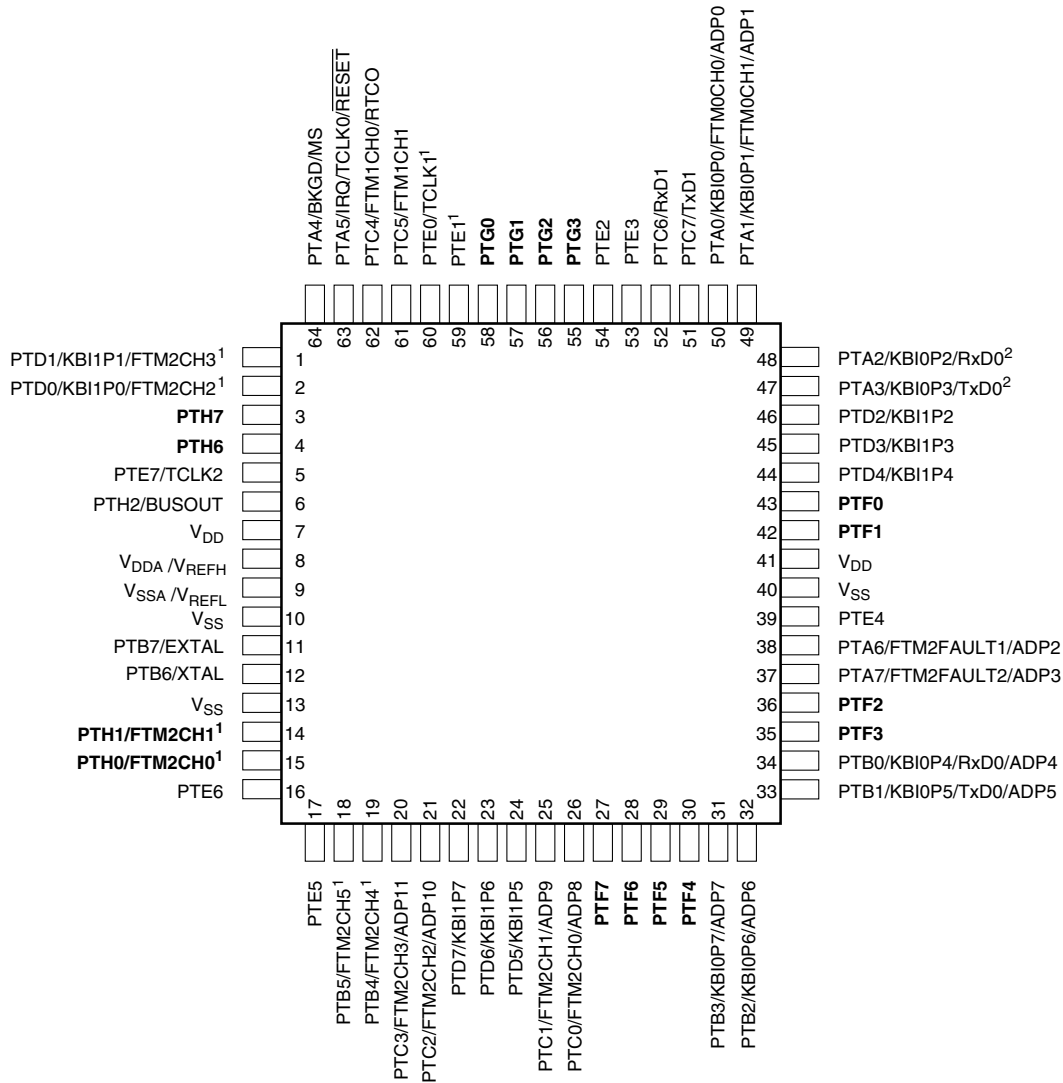
The block diagram in the following figure shows the structure of the MCUs.



1. PTA2 and PTA3 operate as true open drain when working as output.
2. PTA4/BKGD/MS is an output-only pin when used as port pin.
3. PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 can provide ultra-high source/sink current up to 20 mA.
4. The frequency of the clock from BUSOUT must be equal or less than 10 MHz with 25 pF loading at PAD.
5. The secondary power pair of V_{DD} and V_{SS} (pin 41 and pin 40 in 64-pin packages) and the third V_{SS} (pin 13 in 64-pin packages) are not bonded in 32-pin packages.

Figure 1. MCU block diagram

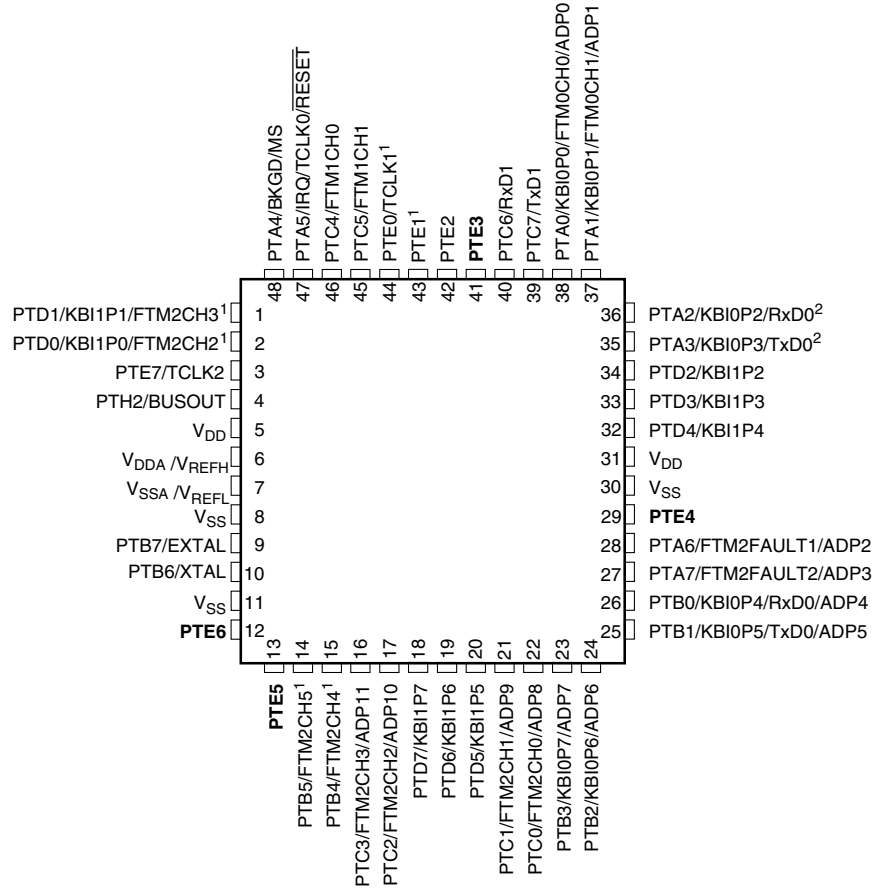
2.3 Device pin assignment



Pins in **bold** are not available on less pin-count packages.

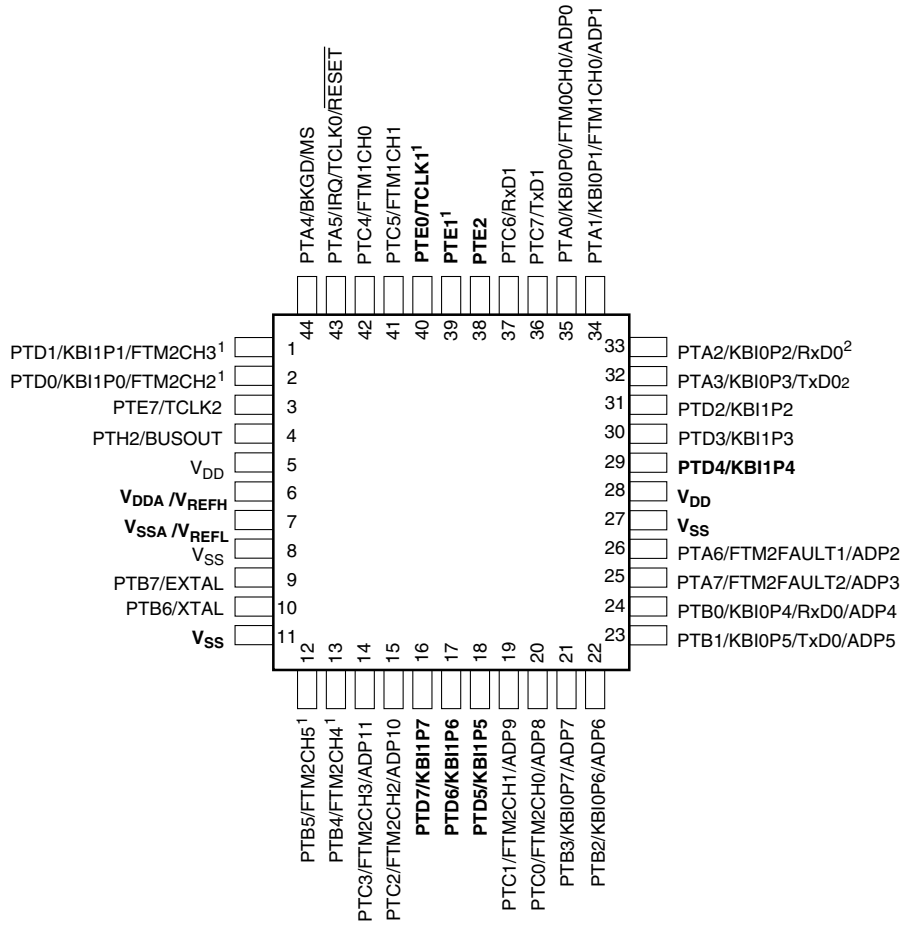
1. High source/sink current pins
2. True open drain pins

Figure 2. MC9S08PL60 64-pin QFP and LQFP packages



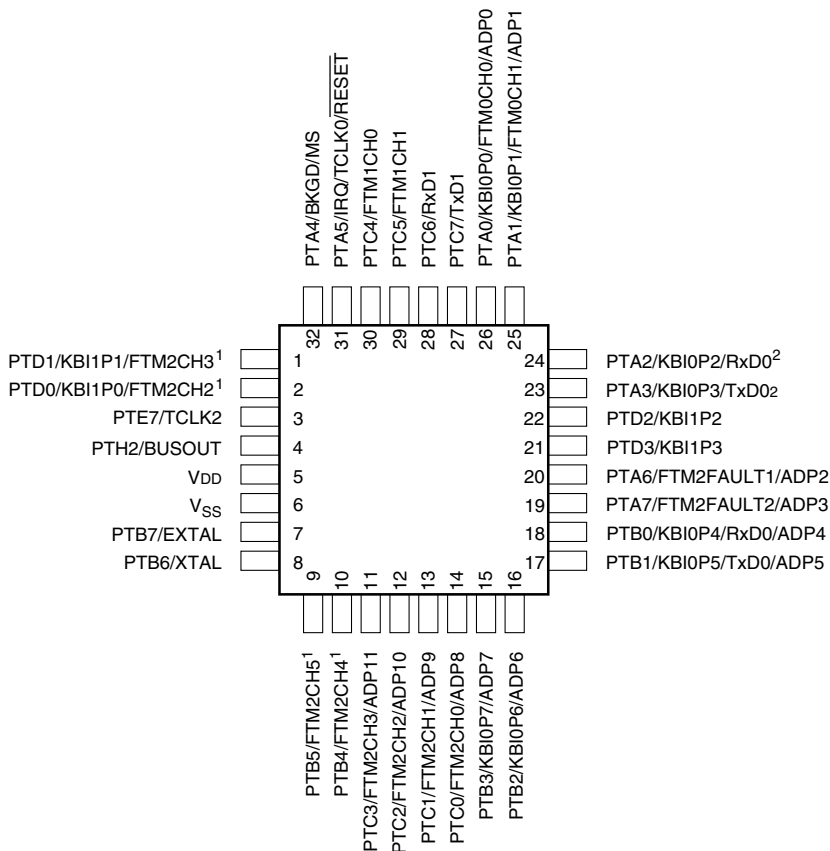
Pins in **bold** are not available on less pin-count packages.
 1. High source/sink current pins
 2. True open drain pins

Figure 3. MC9S08PL60 48-pin QFN and LQFP packages



Pins in **bold** are not available on less pin-count packages.
 1. High source/sink current pins
 2. True open drain pins

Figure 4. MC9S08PL60 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 5. MC9S08PL60 32-pin LQFP package

2.4 Module-by-module features

2.4.1 8-Bit HCS08 central processor unit (CPU)

- Up to 10 MHz bus at 4.5 V to 5.5 V across temperature range of -40 °C to 85 °C
- Support for up to 48 interrupt/reset sources
- Support up to four-level nested interrupt
- On-chip memory
- Up to 60 KB flash read/program/erase over full operating voltage and temperature
- Up to 256 Byte EEPROM; 2-byte erase sector; program and erase while executing flash
- 48-bit universally unique identification (UUID) to identify each device
- 4096-byte random-access memory (RAM)
- Flash and RAM access protection

2.4.2 Power-saving modes

- One low-power stop modes; reduced power wait mode
- Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode

2.4.3 Clocks

- Oscillator (XOSC)
 - Loop-controlled Pierce oscillator
 - Crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 4 MHz to 10 MHz
- Internal clock source (ICS)
 - Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference
 - Precision trimming of internal reference allowing 0.2% resolution
 - 1% deviation across temperature range of 0 °C to 70 °C and 1.5% deviation across temperature range of -40 °C to 85 °C
 - Up to 10 MHz

2.4.4 System protection

- Window watchdog with independent clock source
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal Opcode Detection with reset
- Illegal address Detection with reset
- Programmable cyclic redundancy check

2.4.5 ADC

- 12-channel, 8-bit resolution; 2.5 μ s conversion time
- Data buffers with optional watermark
- Automatic compare function
- 1.7 mV/°C temperature sensor
- Internal bandgap reference channel
- Operation in stop
- Optional hardware trigger

2.4.6 FTM

- Three flex timer modulators (FTM) modules including one 6-channel and two 2-channel ones
- 16-bit counter; each channel can be configured for input capture
- Output compare
- Edge- or center-aligned PWM mode

2.4.7 MTIM

Two modulo timers with 8-bit prescaler and overflow interrupt

2.4.8 RTC

16-bit real timer counter.

2.4.9 SCI

- Two serial communications interface (SCI/ UART) modules optional 13-bit break
- Full duplex non-return to zero (NRZ)
- LIN extension support

3 Development support

- Single-wire background debug interface
- Breakpoint capability to allow three breakpoint setting during in-circuit debugging
- On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes

4 Revision history

The following table provides a revision history for this document.

Table 3. Revision history

Rev. No.	Date	Substantial Changes
0	8/29/2011	Initial published
1	9/19/2011	Updated block diagram figure, feature availability table, CPU feature, and system protection sections.

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