Compal Confidential

DH5AV_JV_0V Schematics Document

AMD Raven Ridge Platform

AMD R17M-P1-50/R18M-M2-60/R18M-G1-90

LA-G021P REV:1.B

2017-12-25

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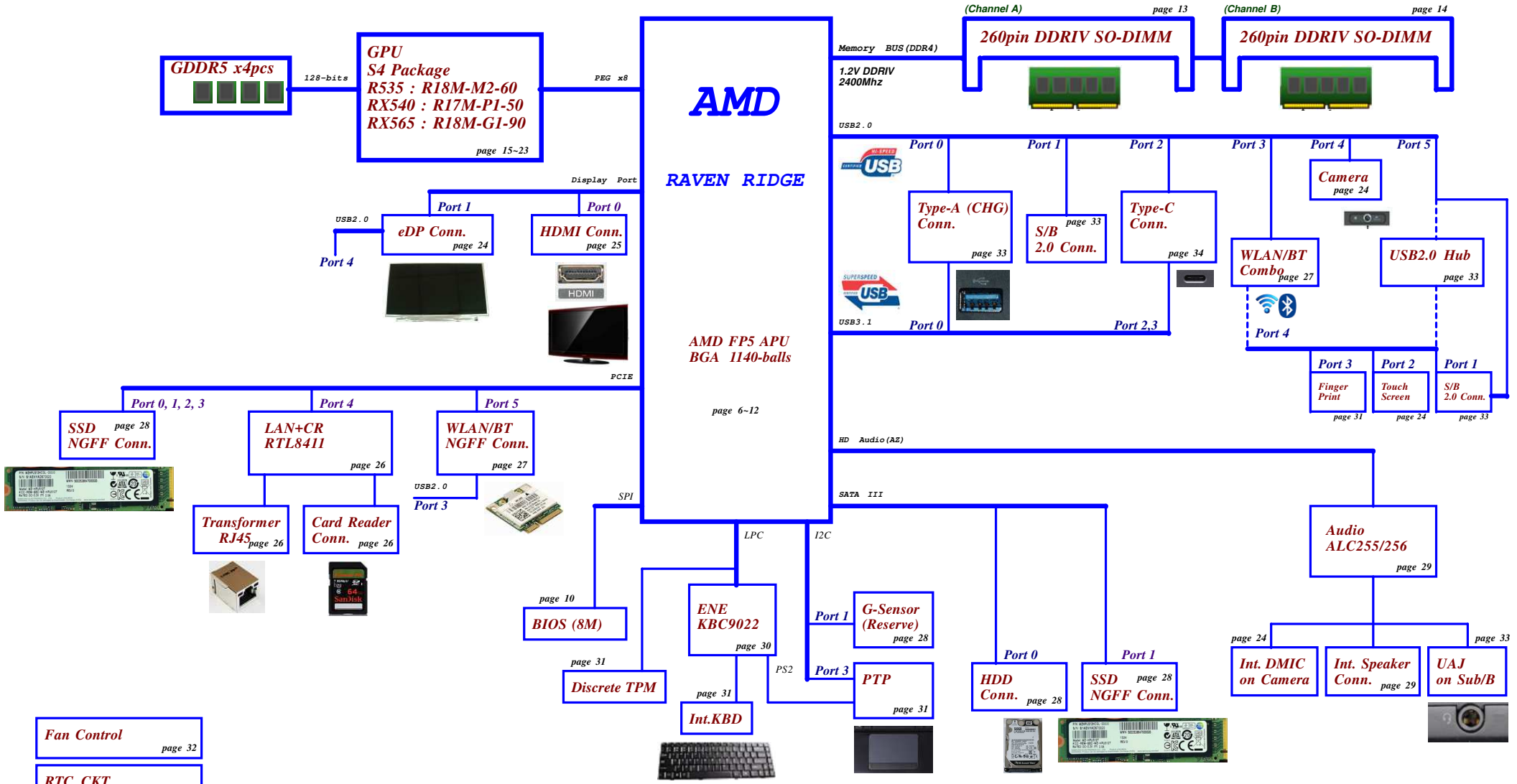
Model Name : DH5AV_JV_0V



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Title: BLOCK DIAGRAMS

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Voltage Rails

Power Plane	Description	S0	S3	S5
+19V_VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+0.8VALW	0.8V always on power rail	ON	ON	OFF
+0.8VS	0.8V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail for APU and DDR	ON	ON	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+0.6VS	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	AC:ON DC:OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN IC power	ON	ON	OFF
+TP_VCC	3.3V Touch Pad power	ON	ON	OFF
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+0.8VSDGPU	VGA power	ON	OFF	OFF
+VDDCI	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF
+FP_VCC	3.3V Finger Print power	ON	ON	OFF

APU SMBus/I2C Address Table

Master	Device	Address[7:1]	Address [7:0] Write	Address [7:0] Read
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)	G-Sensor (Reserver)	0001 1000b 18h	0011 0000b 30h	0011 0001b 31h
I2C Port 2 (+3VS)				
SBMus Port 0 (+3VS)	JDIMM1	0101 0000b 50h	1010 0000b A0h	1010 0001b A1h
	JDIMM2	0101 0001b 51h	1010 0010b A2h	1010 0011b A3h
I2C Port 3 (+3VALW)	PTP (Synaptics)	0010 1100b 2Ch	0101 1000b 58h	0101 1001b 59h
	PTP (ELAN)	0001 1111b 15h	0011 1110b 3Eh	0011 1111b 3Fh
SMBus Port 1 (+3VALW)				

EC SMBus Address Table

SMBus Port 1 (+3VALW)	Smart Battery	0000 1011b 0Bh	0001 0110b 16h	0001 0111b 17h
	Charger IC (BQ24735)	0000 1001b 09h	0001 0010b 12h	0001 0011b 13h
SMBus Port 2 (+3VS)	APU Temp. (TSI)	0100 1100b 4Ch	1001 1000b 98h	1001 1001b 99h
	GPU Temp.	0100 0001b 41h	1000 0010b 82h	1000 0011b 83h
	CC-Logic	1100 0000b C0h	1000 0000b 80h	1000 0001b 81h

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DH5JV
2	DH5AV
3	DH50V

ZZZ @ — DA8001E9010 — PCB 28Z LA-G021P REV1 MB 2

ZZZ PCB@ — DAZ28Z00100 — PCB DH5JV LA-G021P LS-G021P/E911P

ZZZ PCB1A@ — DAZ28Z00101 — PCB DH5JV LA-G021P LS-G021P/E911P 1A

ZZZ PCB1B@ — DAZ28Z00102 — PCB DH5JV LA-G021P LS-G021P/E911P 1B

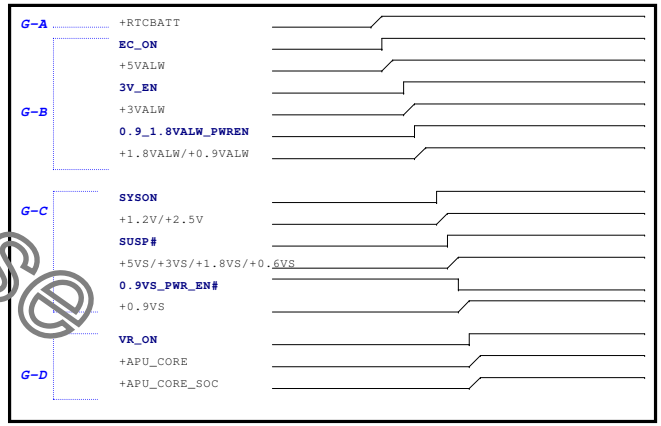
Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

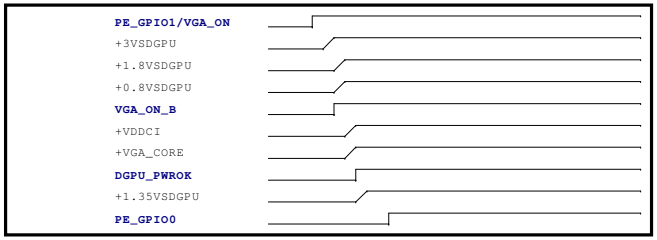
BOM Structure Table

BOM Structure	BTO Item
@	Unpop
EMC@/NEMC@	EMI/ESD Pop/Unpop
4D@	HDMI Royalty
CONN@	Mechanical Connector
JP@	Jump
RS@	R-Short
TP@	Test Point
TPM@	TPM Circuits
PCIE@/T1PCIE@	PCIE Gen2/Gen3-1 APU PCIE SSD
SATA@	SATA HDD
GS@	G-Sensor Circuits
LDO@/SWR@	RTL8411 LDO Mode/Switching Mode
PAR@/TI@	SATA Redriver PARADE/TI Solution
CHG@/NCHG@	USB Charger/Non-Charger
255@	Audio Codec AL255 Design
256@/256EMC@	Audio Codec AL256 Design
UMA@	UMA Config
R3/R5/R7APU@	APU PN Refer p.6
15W@/25W@/35W@	APU Watt Config
T1@/T2@	APU Type Config
EJ@/EA@/VX@	EJ/EA/VX Project Config
DIS@/T1DIS@	VGA Circuits/Type1-APU VGA Circuits
	GPU and VRAM Config Refer p.23
R535@	R18M-M2-60 GPU
RX540@	R17M-P1-50 GPU
RX565@	R18M-G1-90 GPU
LEXA@	LEXA Series VGA
VRAM7G@/VRAM6G@	VRAM7G and VRAM6G
HUB@/NHUB@	USB20 HUB/Non-HUB
FP@/FPEMC@	Finger Print
DMIC2@/DMIC4@	2 or 4 DMIC Design
HDT@	HDT Circuits
TYPEC@	TYPEC Circuits
TYPECEMC@	TYPEC EMC Circuits
NTYPEC@	No TYPEC Circuits

POWER SEQUENCE



VGA POWER SEQUENCE



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Title: NOTES LIST

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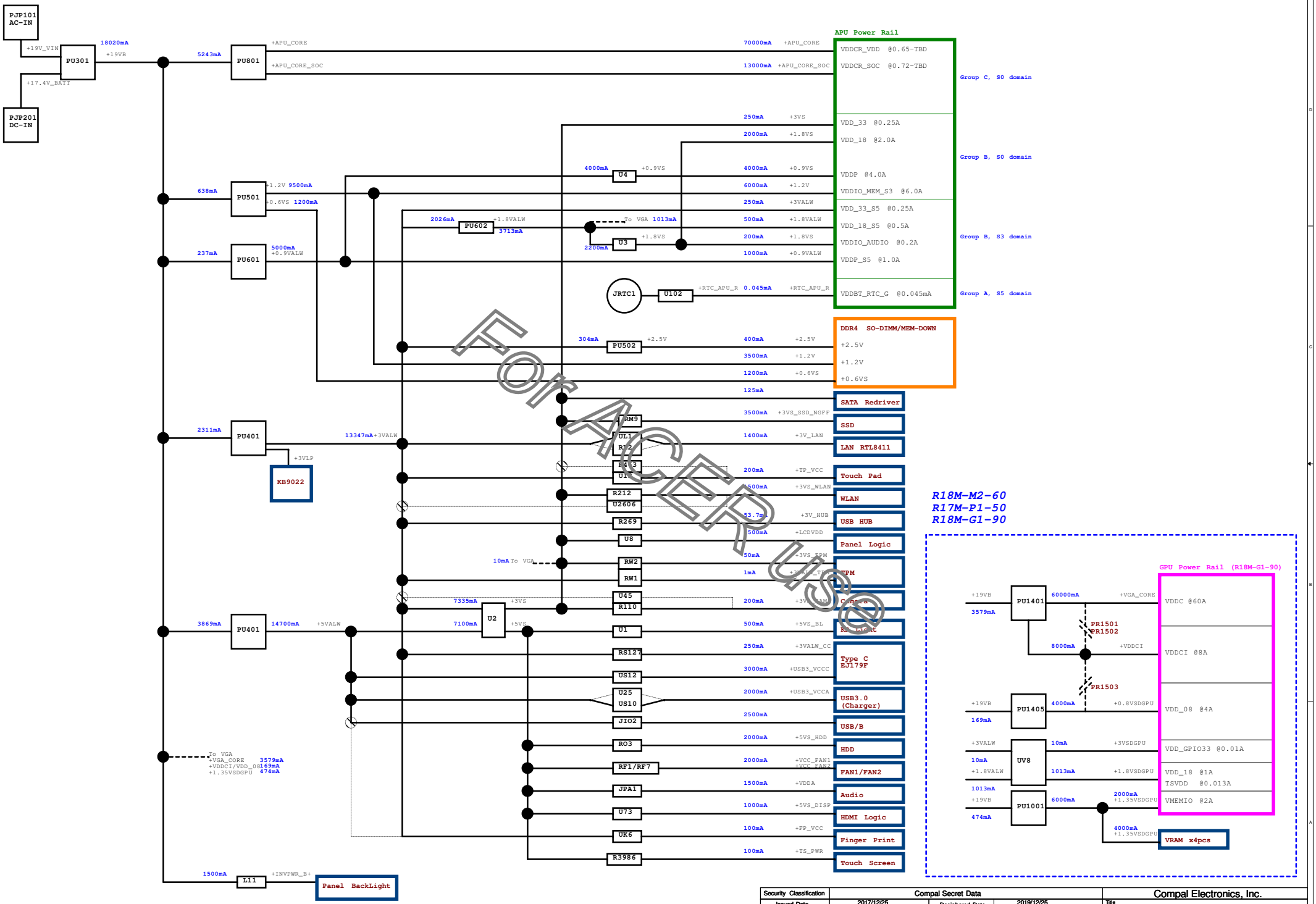

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Title: POWER MAP

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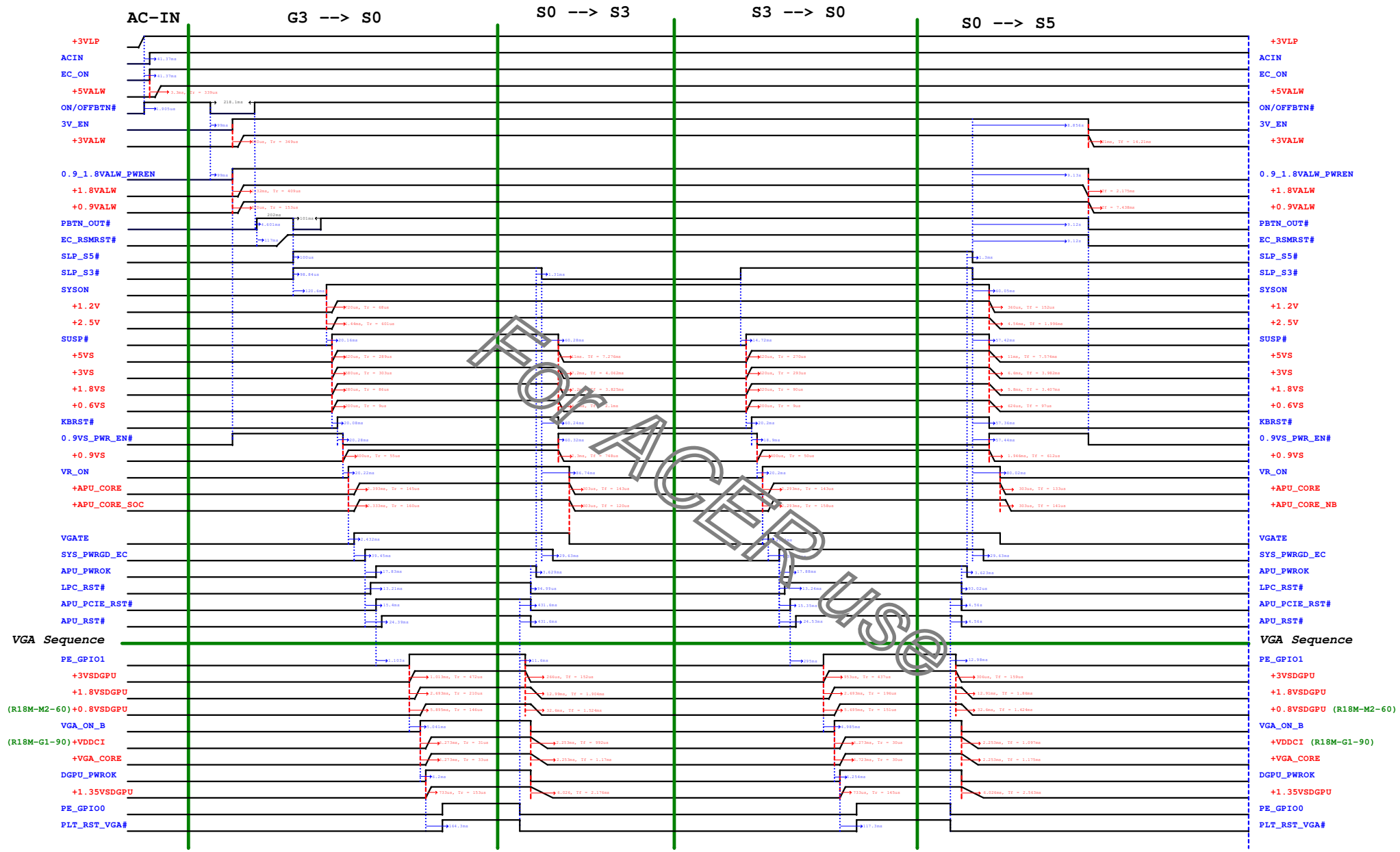
Raven Ridge Platform Power Sequence



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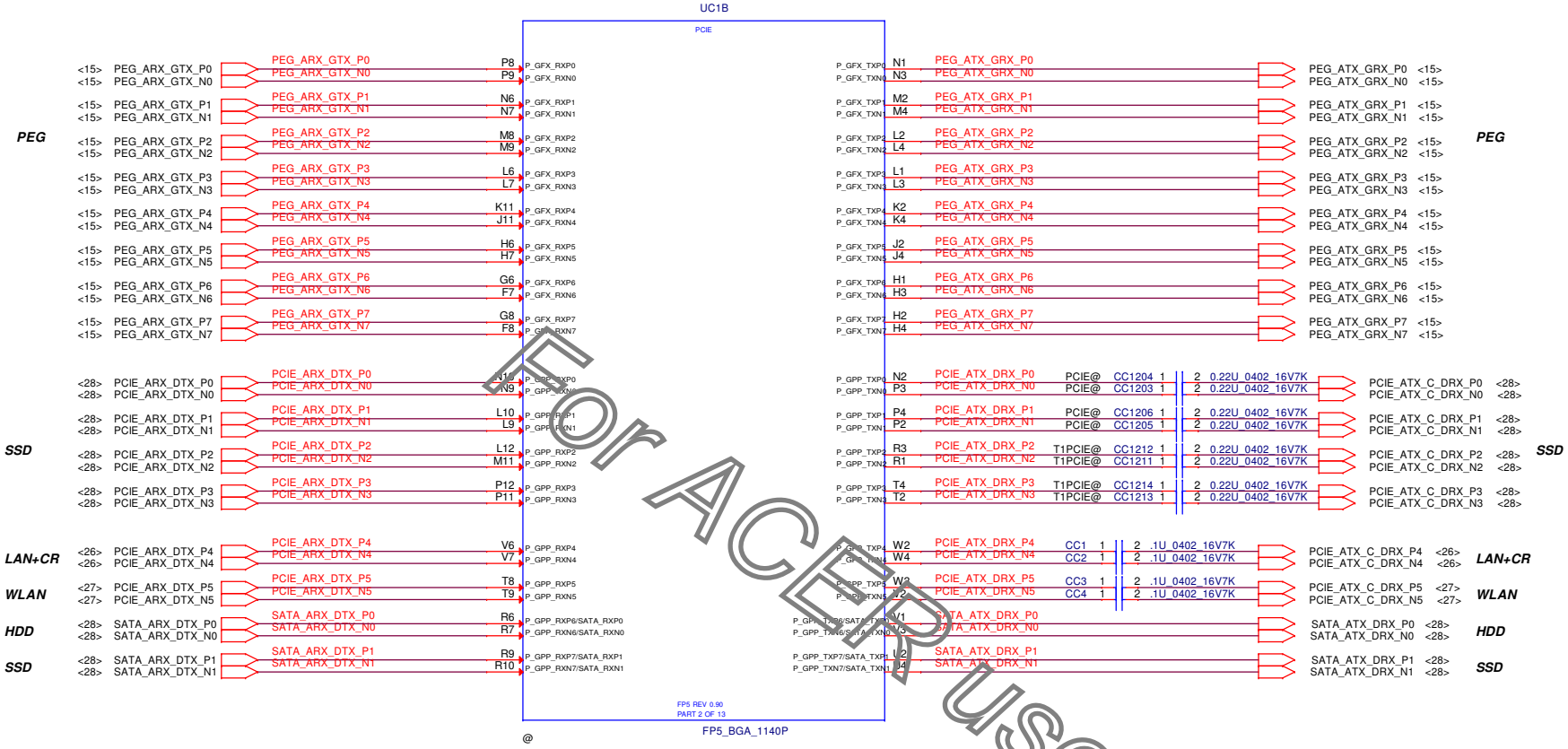
Main Func = CPU



APU PN Table

APU Platform	R3 PN	R3 PN	R3 PN	R3 PN
Raven	UC1 R3APUDC@  S IC RAVEN3 YM2200C4T2OFB 2G BGA ABO! SA0000BBJ30	UC1 R3APUQC@  S IC RAVEN3 YM2300C4T4MFB 2G BGA ABO! SA0000BIT20	UC1 R5APU@  S IC RAVEN5 YM2500C4T4MFB 2G BGA ABO! SA0000A8R30	UC1 R7APU@  S IC RAVEN7 YM2700C4T4MFB 2.2G BGA ABO! SA0000ASA20

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Title: FP5_(1/7)_PEG/PCIE/SATA

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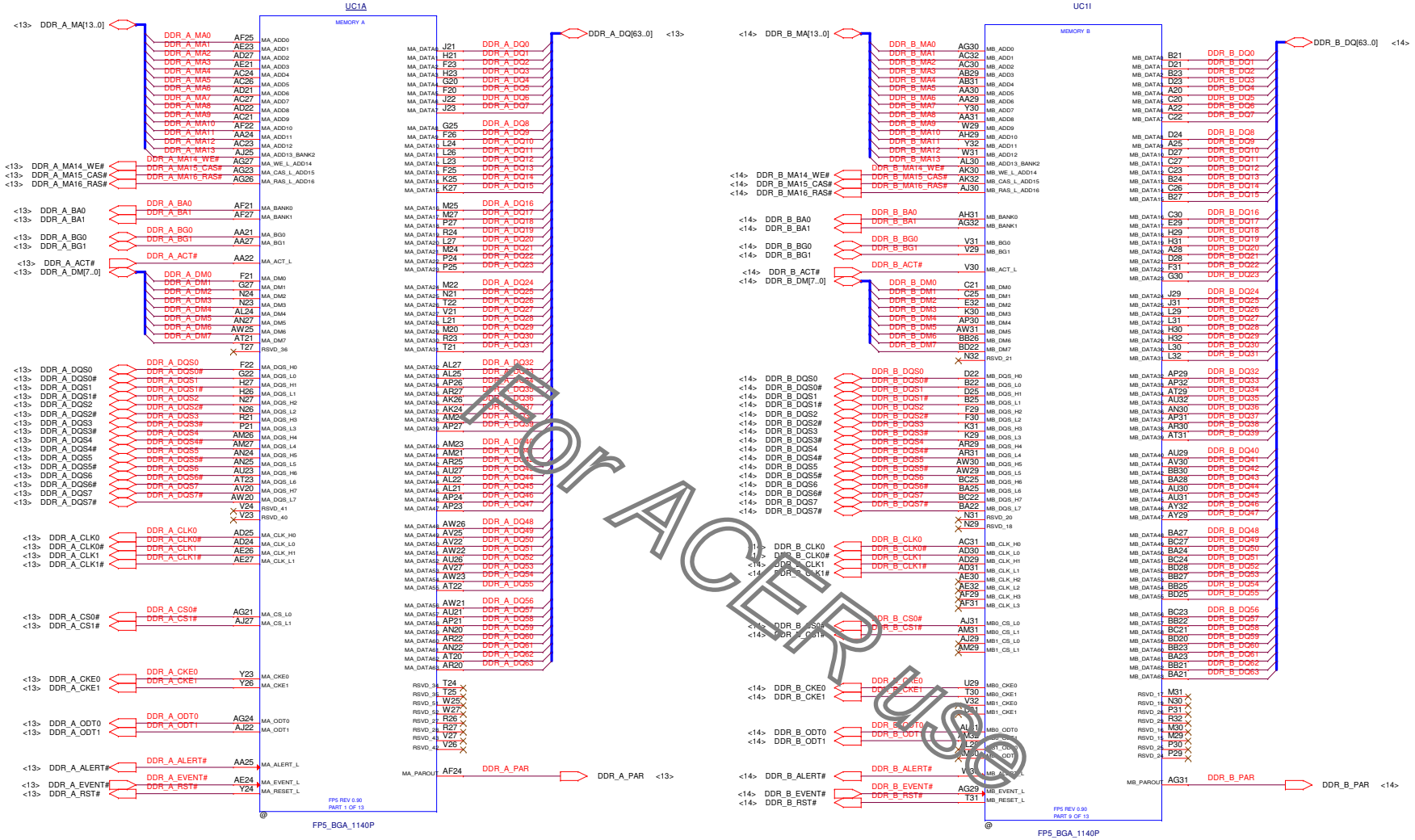
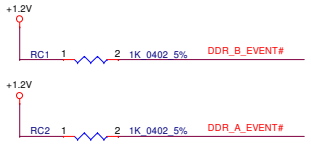


EVENT# pull high



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Compal Electronics, Inc.

Title: FP5_(2/7)_DDR4

Size	Document Number	Rev
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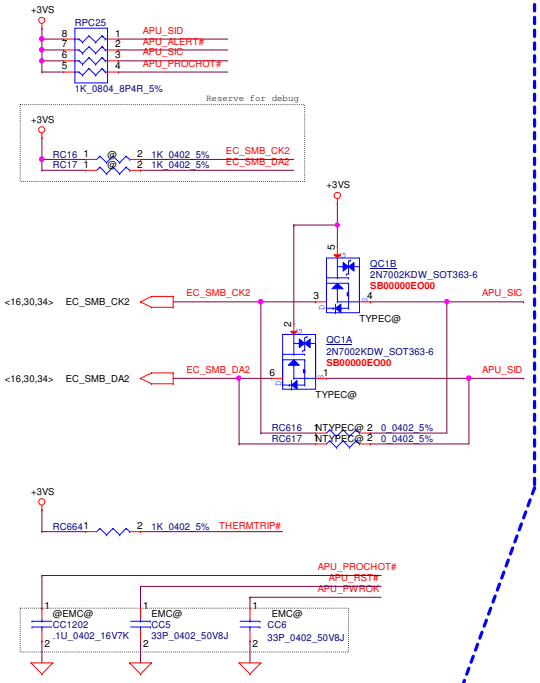
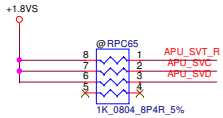
Main Func = CPU

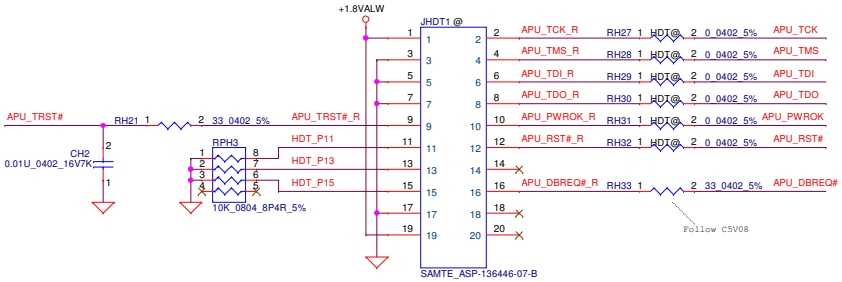
EC/THERM

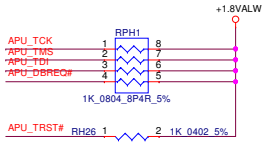


SVID

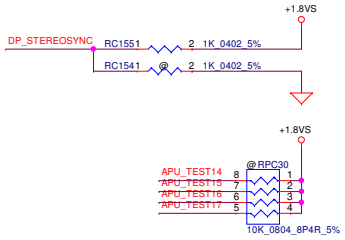


HDT+

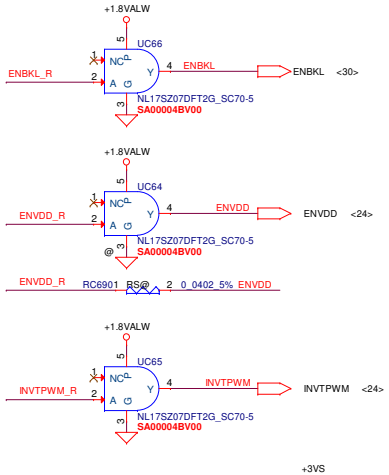




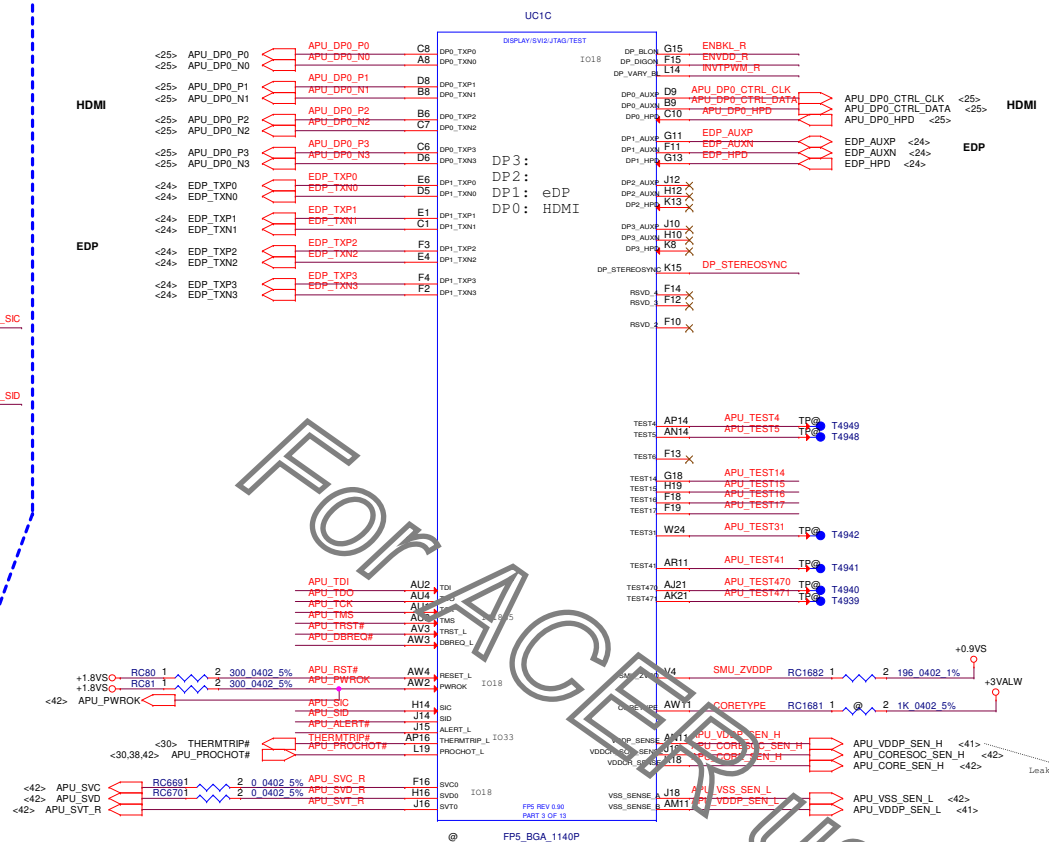
TESTPOINT



DISP



UC1C



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Title: (3/7)_DISP/MISC/HDT

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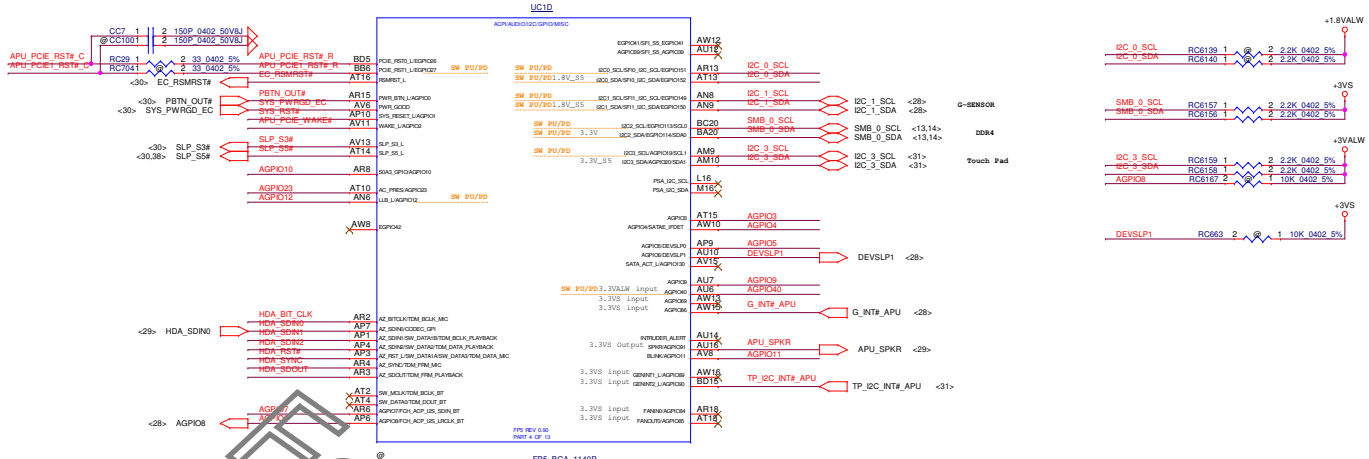
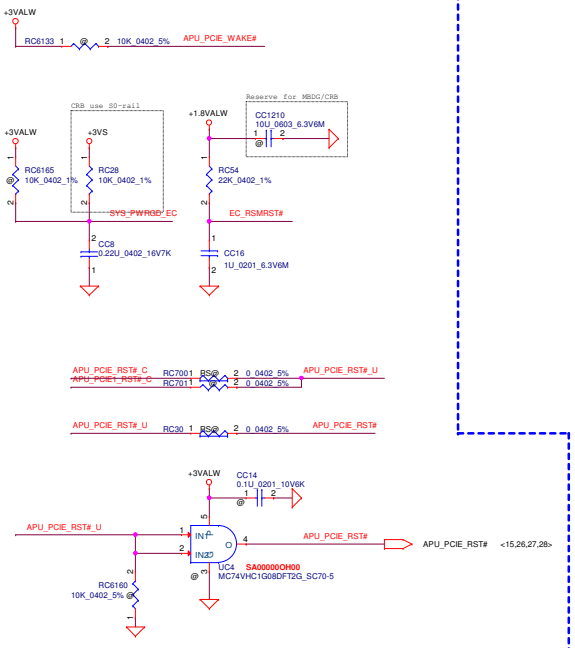
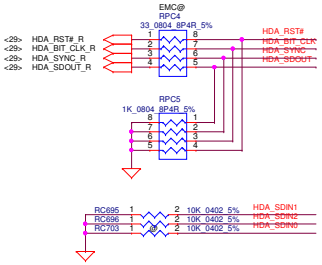


ACPI

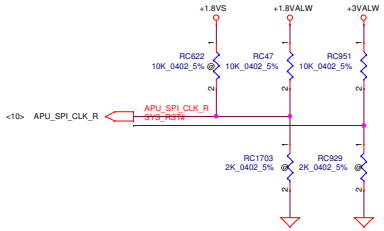


HDA



Strap Pin

	APU_SPI_CLK_R	SYS_RST#
H	USE 48MHZ CRYSTAL CLOCK (Default)	NORMAL RESET MODE (Default)
L	USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK	SHORT RESET MODE



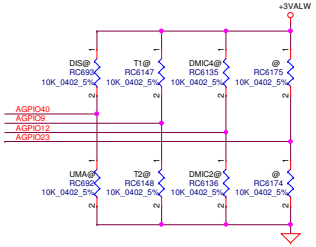
GPIO Table

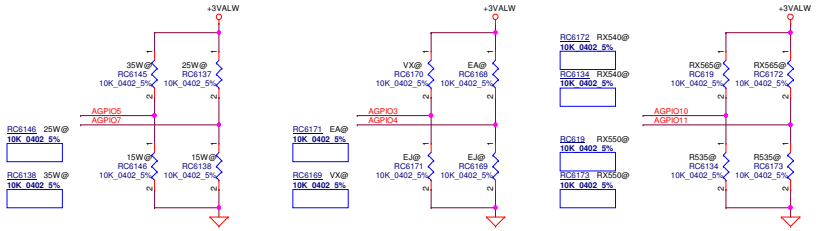
AGPIO5	AGPIO7	
L	L	15W
L	H	25W
H	L	35W

AGPIO3	AGPIO4	
L	L	EJ
L	H	EA
H	L	VX

AGPIO10	AGPIO11	
L	L	R535
L	H	RX540
H	L	RX550
H	H	RX565

	AGPIO40	AGPIO9	AGPIO12	AGPIO23
H	DIS	Type1	DMIC x4	RSV
L	UMA	Type2	DMIC x2	RSV





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Title: FP5_(4/7)_GPIO/HDA/STRAP

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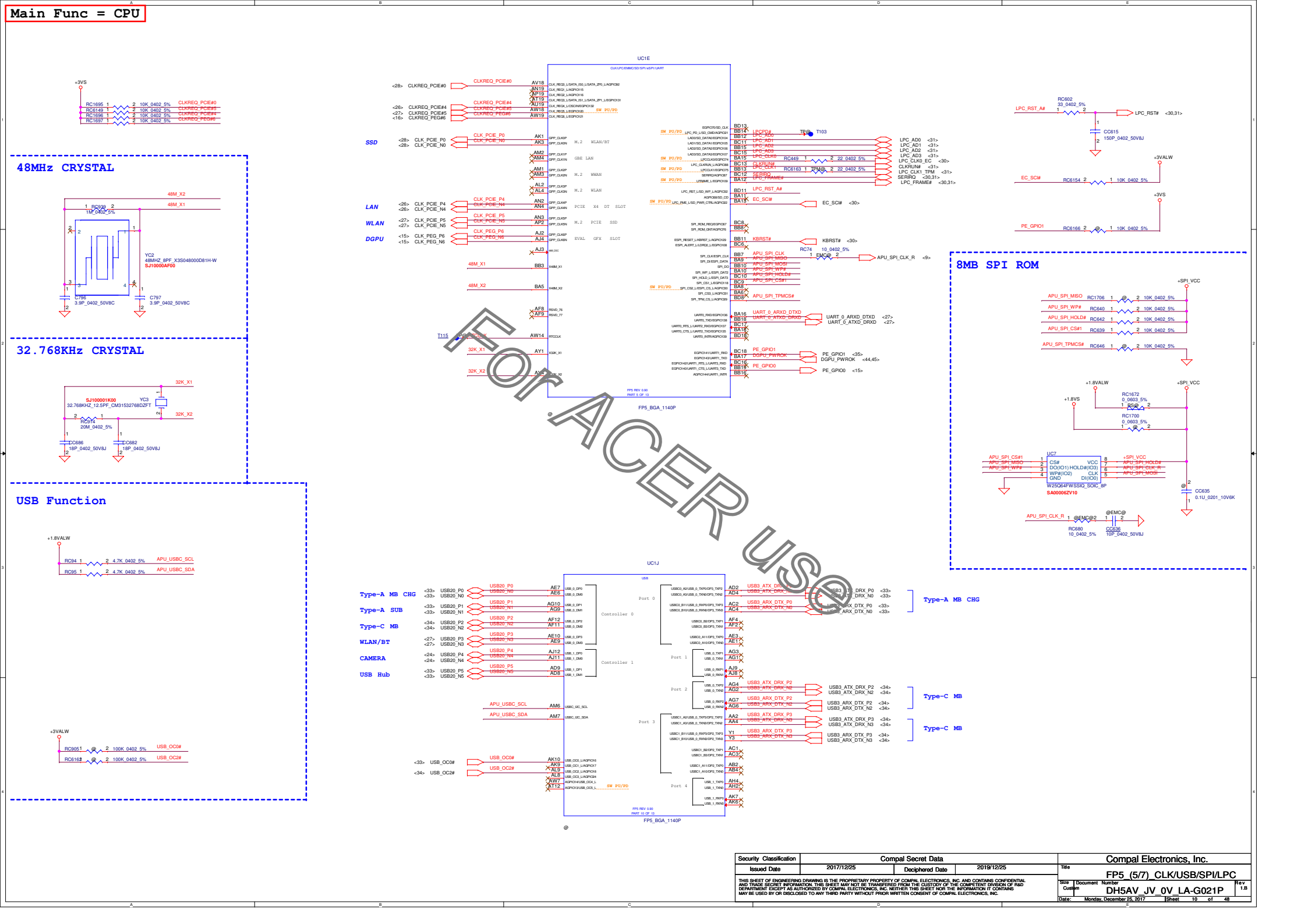
Main Func = CPU



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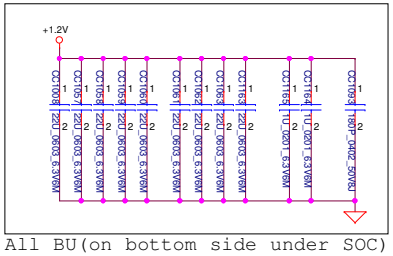
Main Func = CPU

+APU_CORE_SOC Cap
place at Power Side

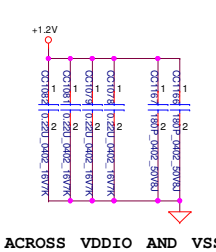
SCL/MBDG:
7*22uF (BU)
1*1uF (BU)
1*180pF (BU)

+APU_CORE Cap place at Power Side

SCL/MBDG:
16*22uF (BU)
1*180pF (BU)

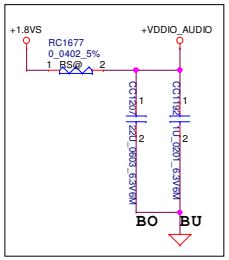


All BU(on bottom side under SOC)

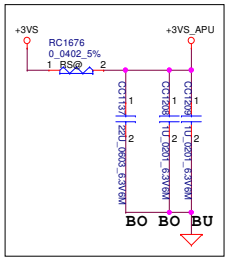


ACROSS VDDIO AND VSS SPLIT

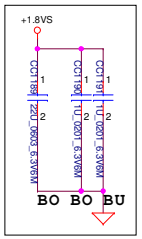
SCL/MBDG:
9*22uF (BU)
2*1uF (BU)
4*0.22uF
1*180pF (BU)
2*180pF



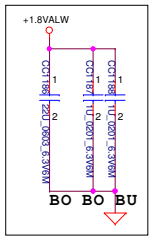
SCL/MBDG:
1 *22uF (BO)
1*1uF (BU)



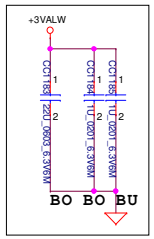
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



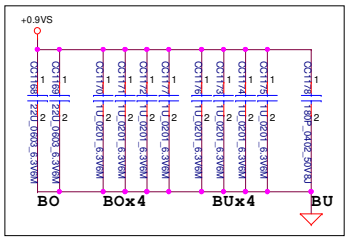
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



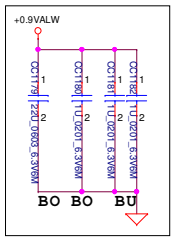
SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)



SCL/MBDG:
1 *22uF (BO)
2*1uF (BO+BU)

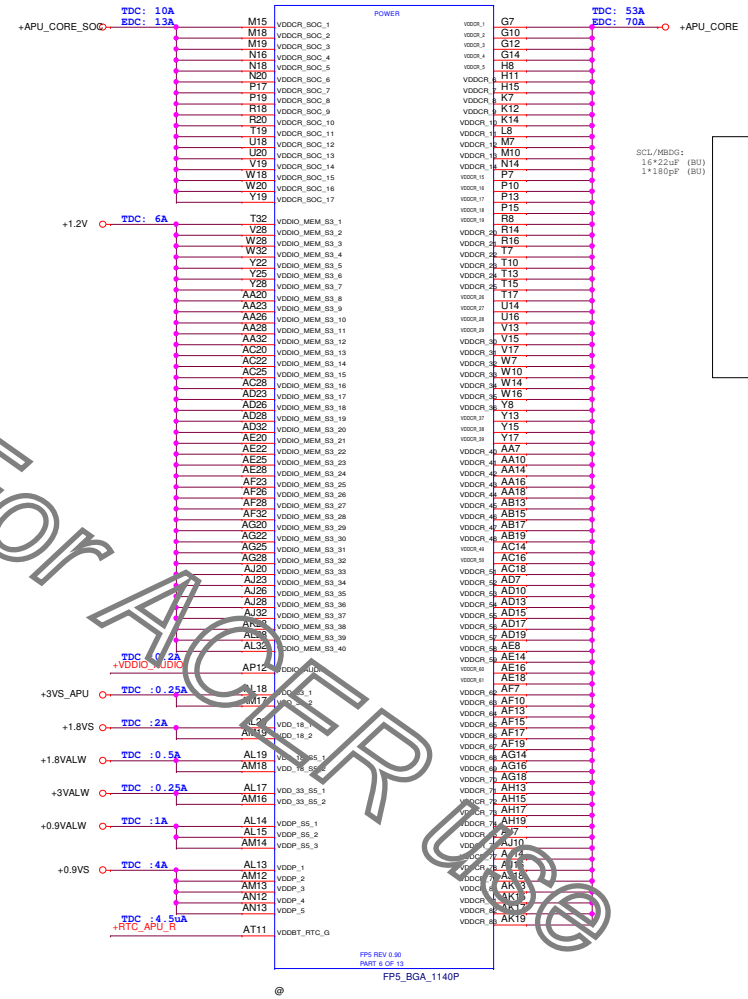


SCL/MBDG:
2 *22uF (BO)
8*1uF (BOx4+BUx4)
1*180pF (BU)

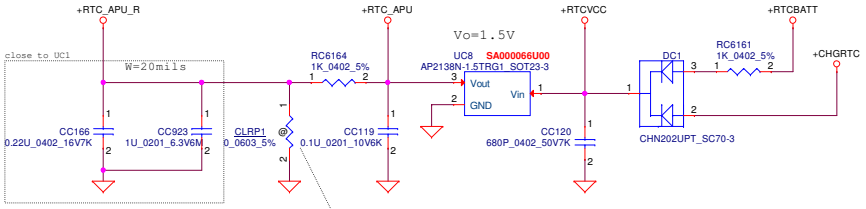


SCL/MBDG:
1 *22uF (BO)
3*1uF (BOx1+BUx2)

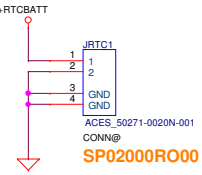
UC1F



RTC OF APU



Need OPEN
for Clear CMOS



Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

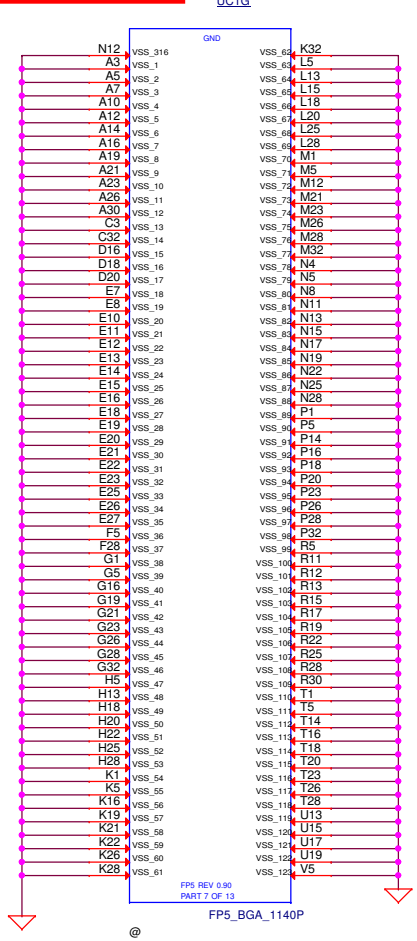
Compal Electronics, Inc.

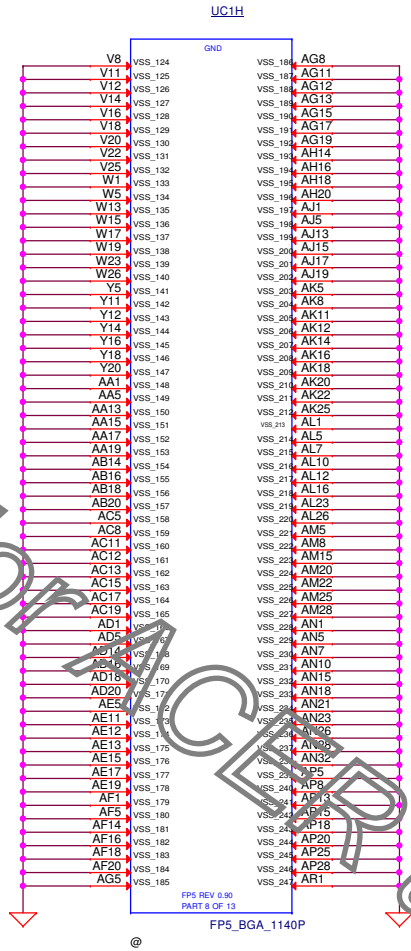
Title: (6/7)_PWR

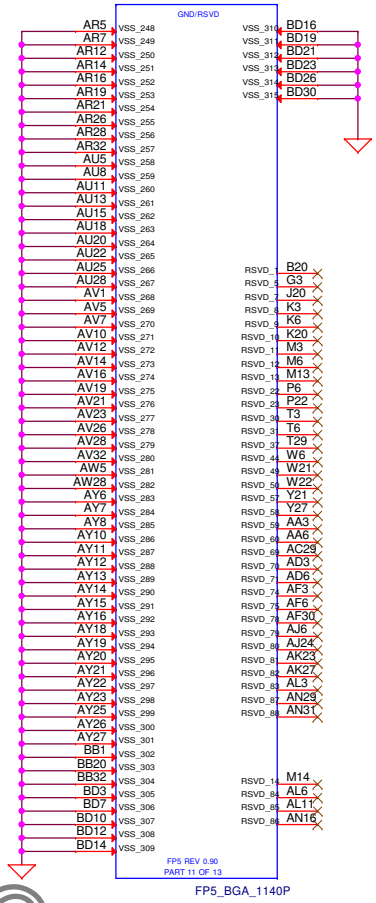
Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

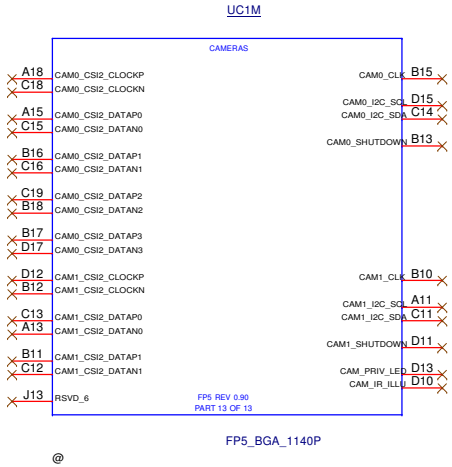
Date: Monday, December 25, 2017 Sheet 11 of 48

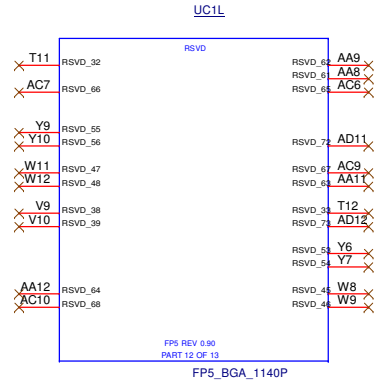
Main Func = CPU











Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: FP5_(7/7)_GND/RSVD/CSI

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

Date: Monday, December 25, 2017 Sheet 12 of 48

Reverse Type-4H

2-3A to 1 DIMMs/channel

Address : A0

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

DDR4 support Even Parity check in DRAMs.

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.255

Follow MA51

SGA00009S00
330U 2V H1.9
9mohm POLY

Follow CRB design

15mil

Place near to SO-DIMM connector.

Layout Note:
Place near JDIMM1.258

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: DDR4 SO-DIMM

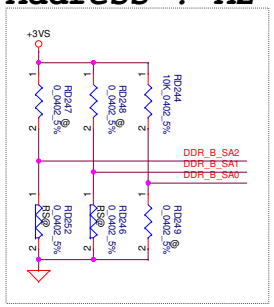
Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

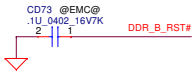
Date: Monday, December 25, 2017 Sheet 13 of 48

Reverse Type-8H

2-3A to 1 DIMMs/channel

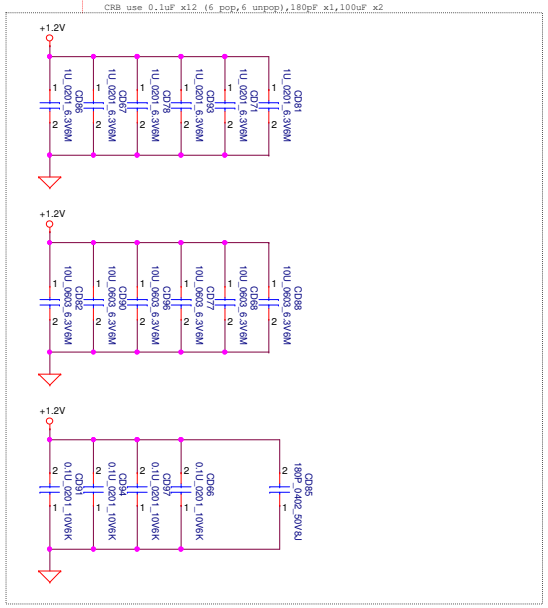
Address : A2



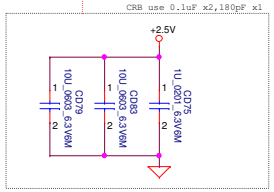


Layout Note:
Place near JDIMM2

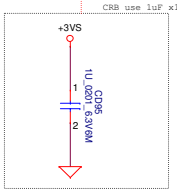
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

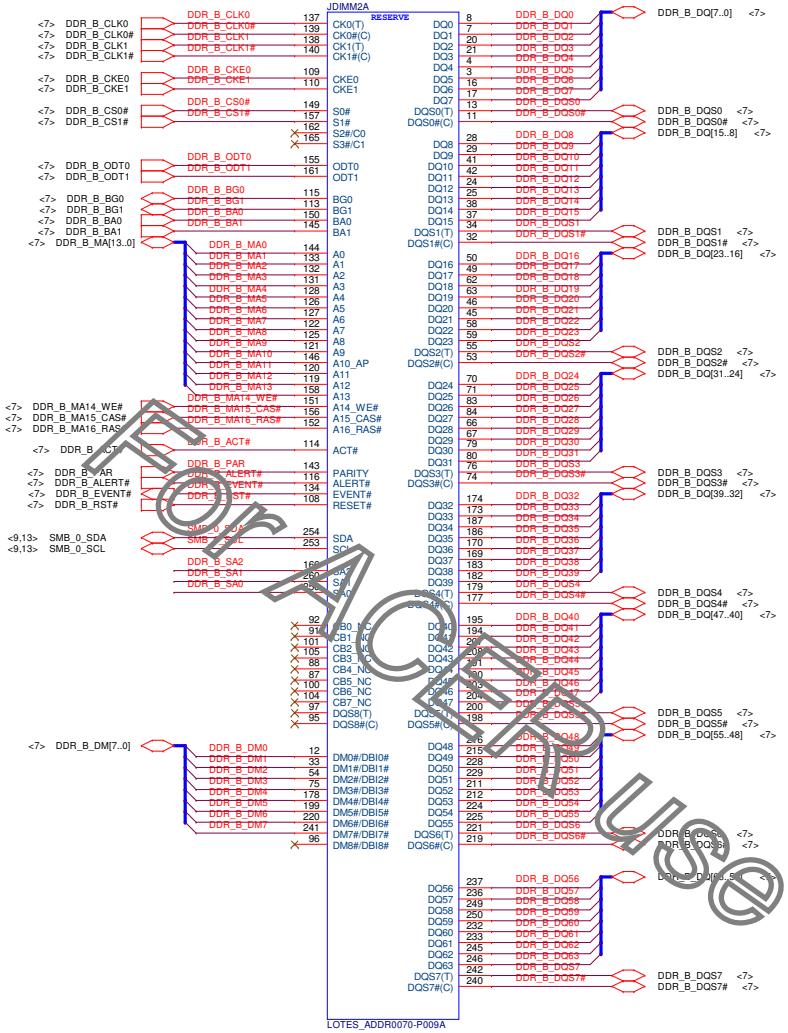


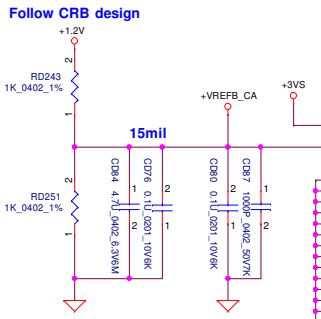
Layout Note:
Place near JDIMM2.257,259

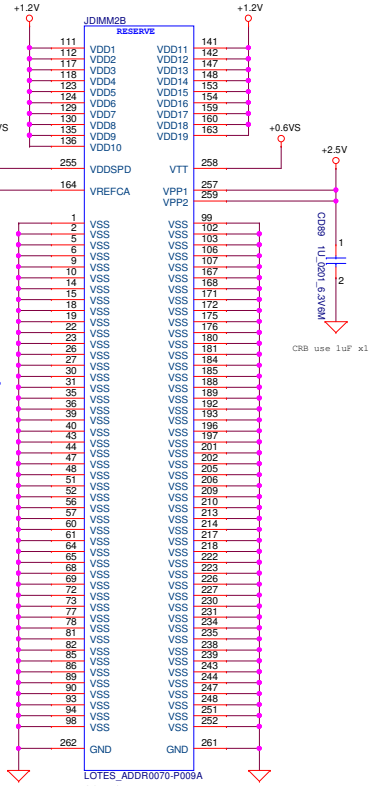


Layout Note:
Place near JDIMM2.255

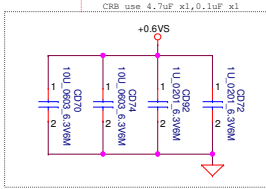






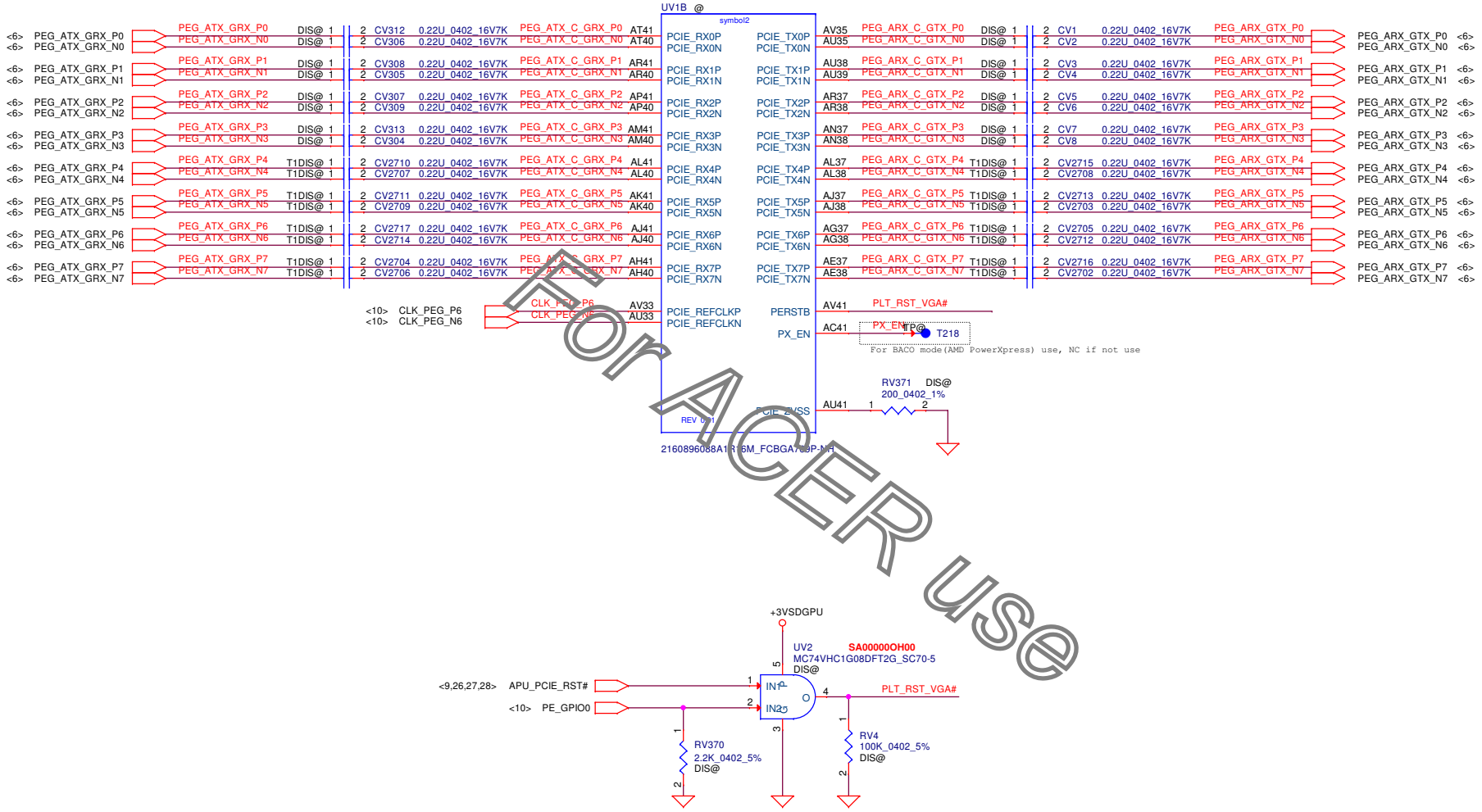


Layout Note:
Place near JDIMM2.258



Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.			
Title: DDR4 SO-DIMM			
Size: Custom	Document Number: DH5AV_JV_0V_LA-G021P		Rev: 1.B
Date: Monday, December 25, 2017	Sheet 14 of 48		



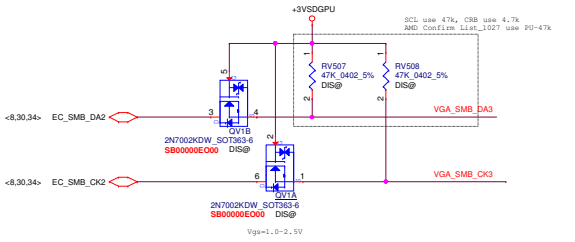
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

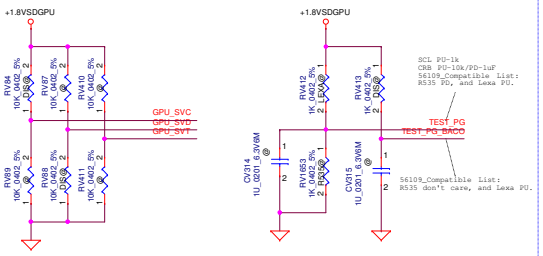
Compal Electronics, Inc.

Title: R18M-M260/G190_(1/9)_PCIE

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

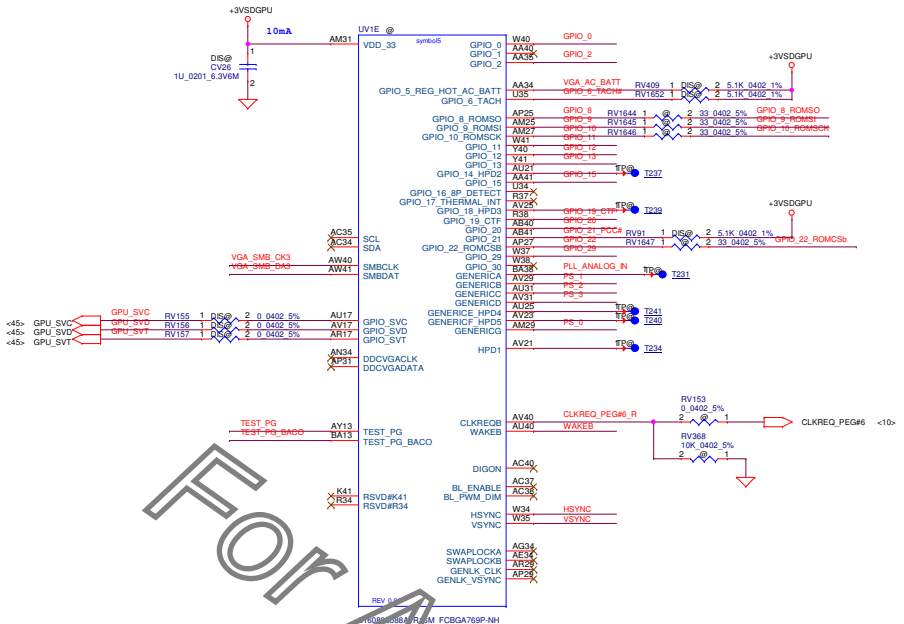
Date: Monday, December 25, 2017 Sheet 15 of 48



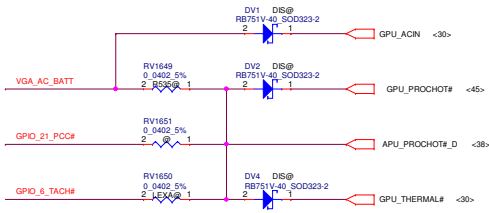


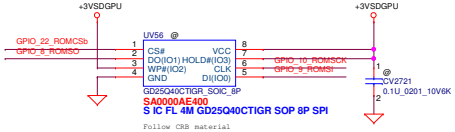
Boot-VID Code

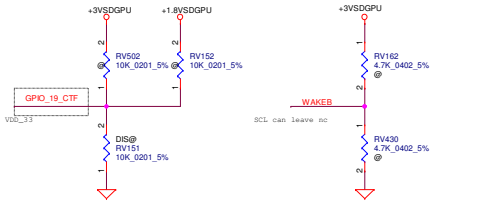
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Function Support	Pin	R18M-M2-60	R17M-G1-50/70 R17M-P1-50/70 R18M-G1-90
AC/DC Mode H:AC L:DC	GPIO5	Yes	Yes
Thermal VR_HOT# (Fan tachometer)	GPIO6	No	Yes
Peak Current Control	GPIO21	No	Yes







LEXA Strap

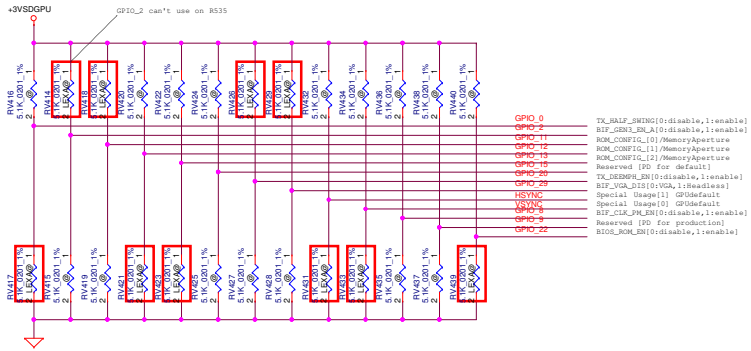


Table 3-27 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

3.22.2 ROM Configurations

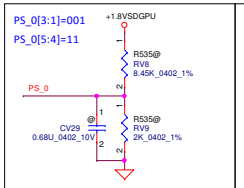
For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

R535 Strap

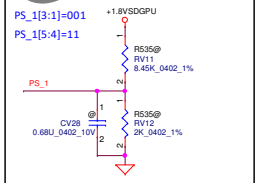
Resistor Divider Lookup Lable 0402 1% resistors are equired		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



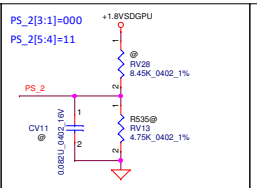
Strap Name :

PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



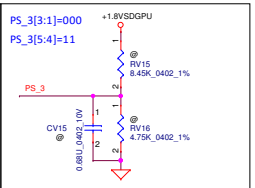
Strap Name :

PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN



Strap Name :

PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A



Strap Name :

PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

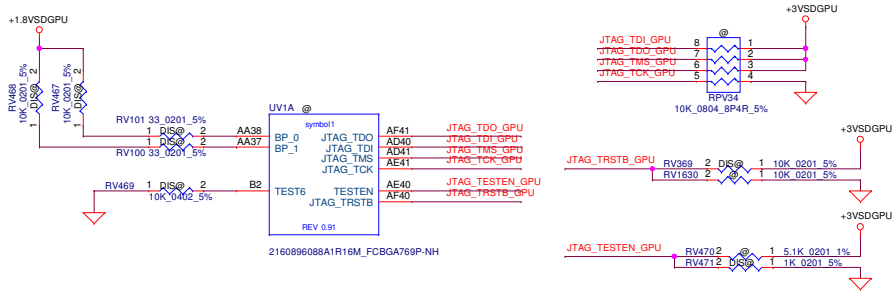
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: R18M-M260/G190_(2/9)_MSIC-1

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

Date: Monday, December 25, 2017 | Sheet 16 of 48



Polaris Memory ID

BOARD_CONFIG[2:0]	R_pu (ohm)	R_pd (ohm)	Bit3 [3:1]
000:SAM 256Mx32	NC	4.75k	000
001:HYN 256Mx32	8.45k	2k	001
010:SAM 128Mx32	4.53k	2k	010
011:HYX 128Mx32	6.98k	4.99k	011
100:MIC 256Mx32	4.53k	4.99k	100

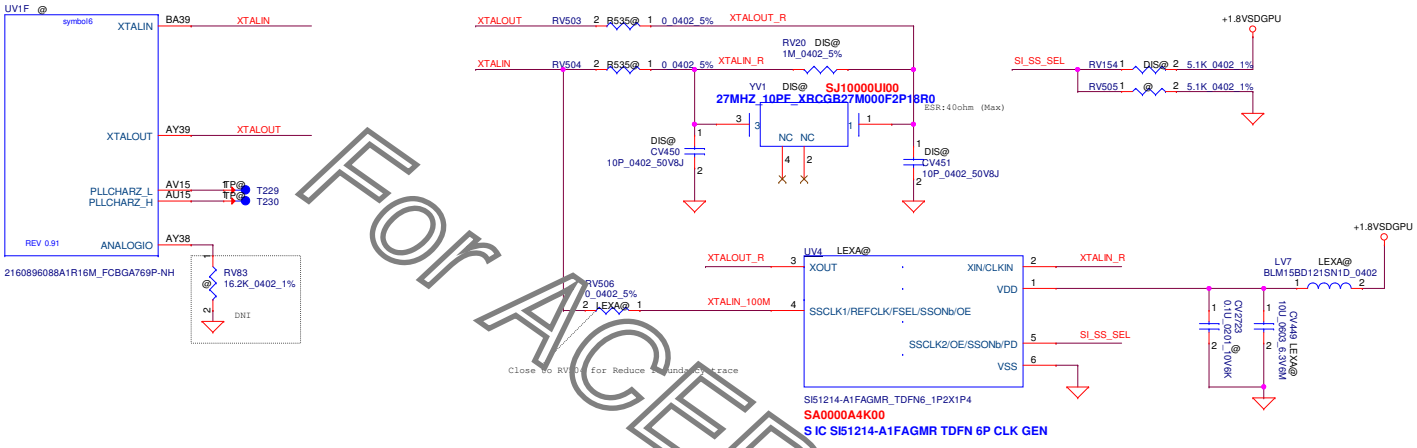
RV16 PV4G_S@
S RES 1/16W 4.75K +-1% 0402
SD034475180

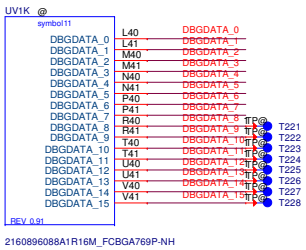
RV15 PV4G_H@ — S RES 1/16W 8.45K +-1% 0402 SD000000680
RV16 PV4G_H@ — S RES 1/16W 2K +-1% 0402 SD034200180

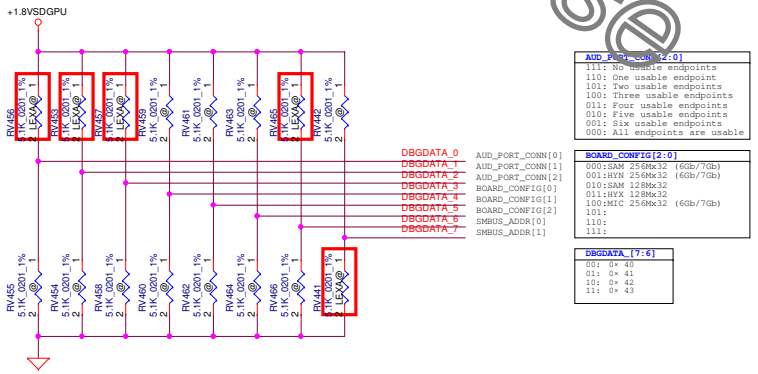
RV15 PV2G_S@ — S RES 1/16W 4.53K +-1% 0402 SD034453180
RV16 PV2G_S@ — S RES 1/16W 2K +-1% 0402 SD034200180

RV15 PV2G_H@ — S RES 1/16W 6.98K +-1% 0402 SD000002680
RV16 PV2G_H@ — S RES 1/16W 4.99K +-1% 0402 SD034499180

RV15 PV4G_M@ — S RES 1/16W 4.53K +-1% 0402 SD034453180
RV16 PV4G_M@ — S RES 1/16W 4.99K +-1% 0402 SD034499180







LEXA Memory ID

RV464 V4G_S@ / RV464 V4G_S7G@ / RV462 V4G_S@ / RV462 V4G_S7G@ / RV460 V4G_S@ / RV460 V4G_S7G@
S RES 1/20W 5.1K +-1% 0201
SD000008900

RV464 V4G_H@ / RV464 V4G_H7G@ / RV462 V4G_H@ / RV462 V4G_H7G@ / RV459 V4G_H@ / RV459 V4G_H7G@
S RES 1/20W 5.1K +-1% 0201
SD000008900

RV464 V2G_S@ / RV461 V2G_S@ / RV460 V2G_S@
S RES 1/20W 5.1K +-1% 0201
SD000008900

RV464 V2G_H@ / RV461 V2G_H@ / RV459 V2G_H@
S RES 1/20W 5.1K +-1% 0201
SD000008900

RV463 V4G_M@ / RV463 V4G_M7G@ / RV462 V4G_M@ / RV462 V4G_M7G@ / RV460 V4G_M@ / RV460 V4G_M7G@
S RES 1/20W 5.1K +-1% 0201
SD000008900

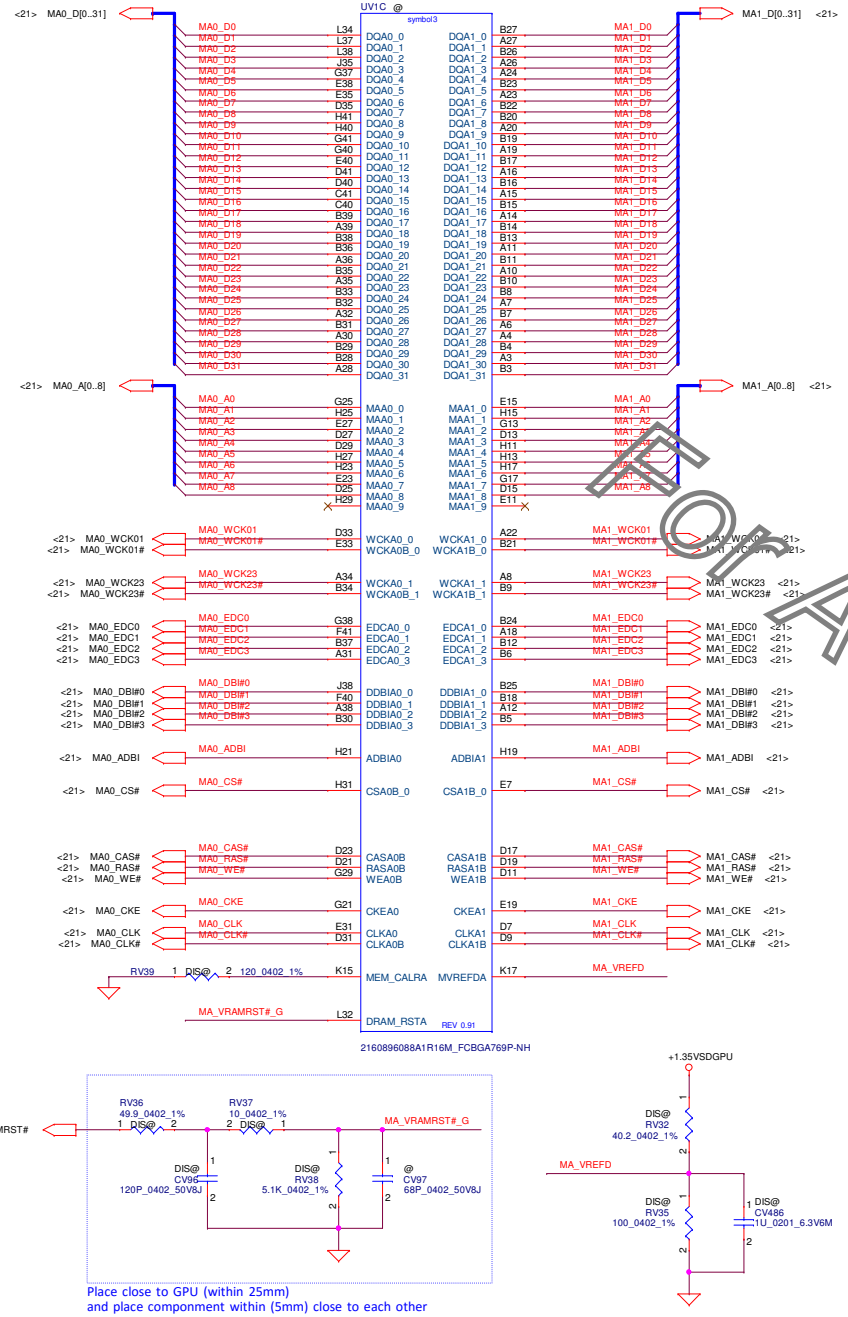
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

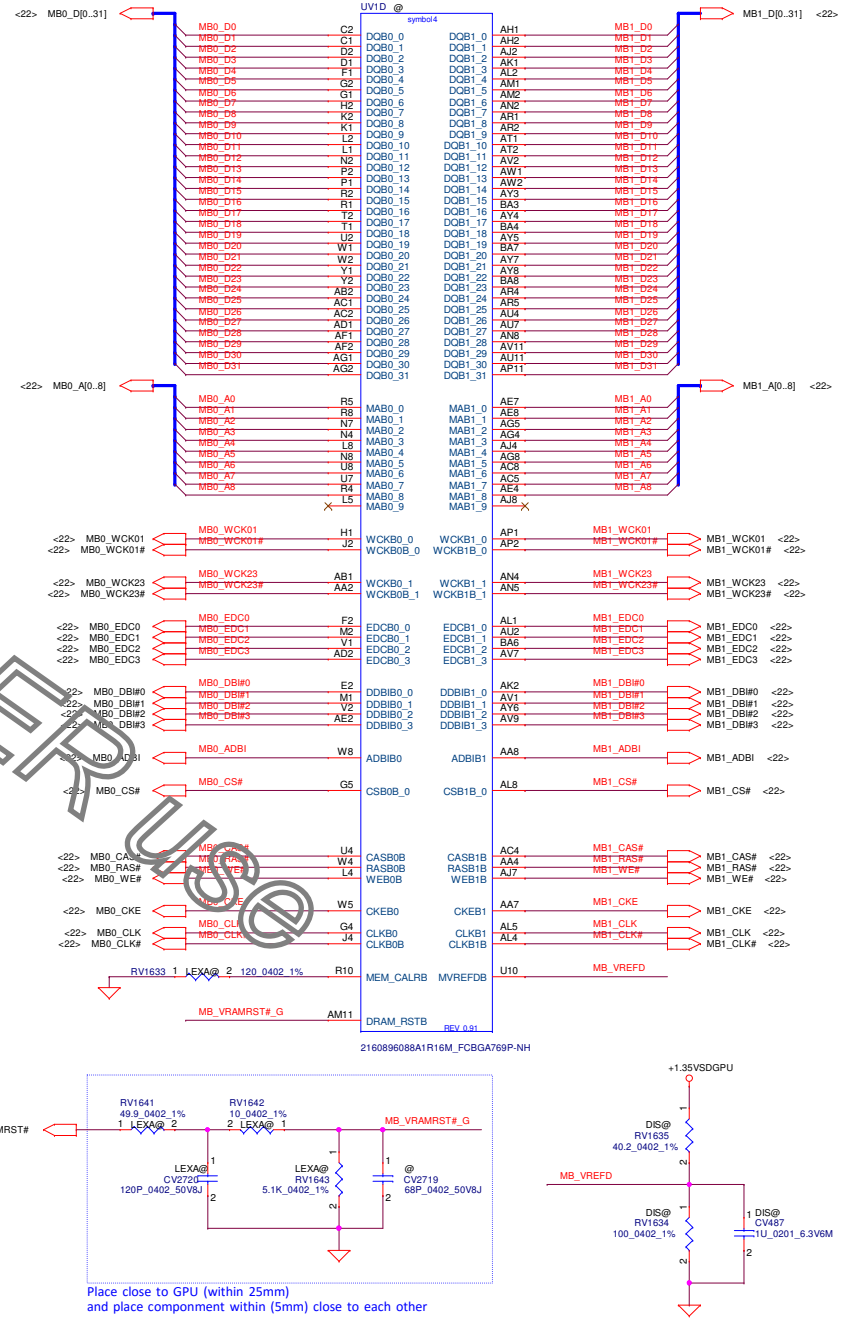
Compal Electronics, Inc.

Title: R18M-M260/G190_(3/9)_MSIC-2

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

Date: Monday, December 25, 2017 | Sheet 17 of 48





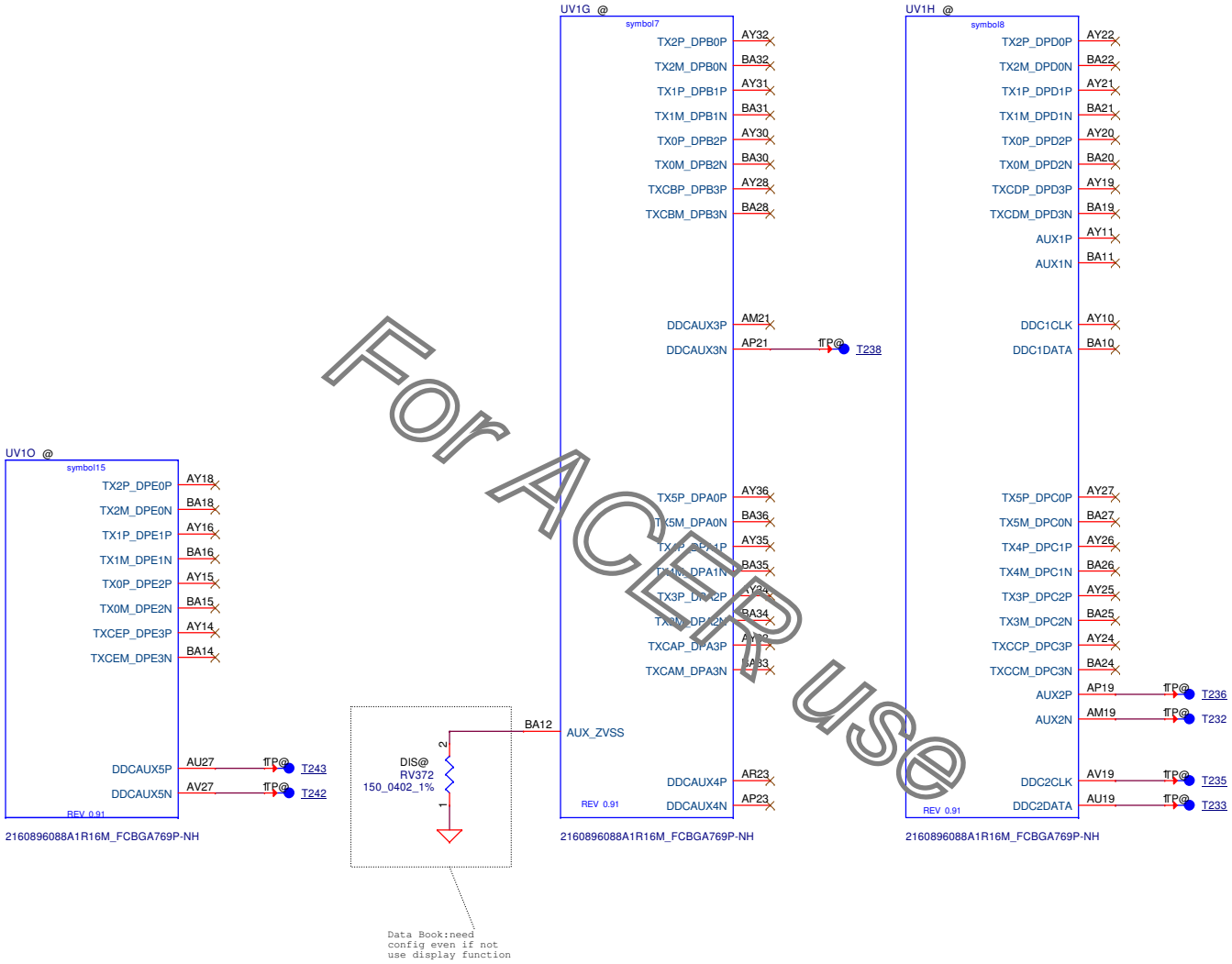
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: R18M-M260/G190_(4/9)_MEM

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

Date: Monday, December 25, 2017 | Sheet 18 of 48



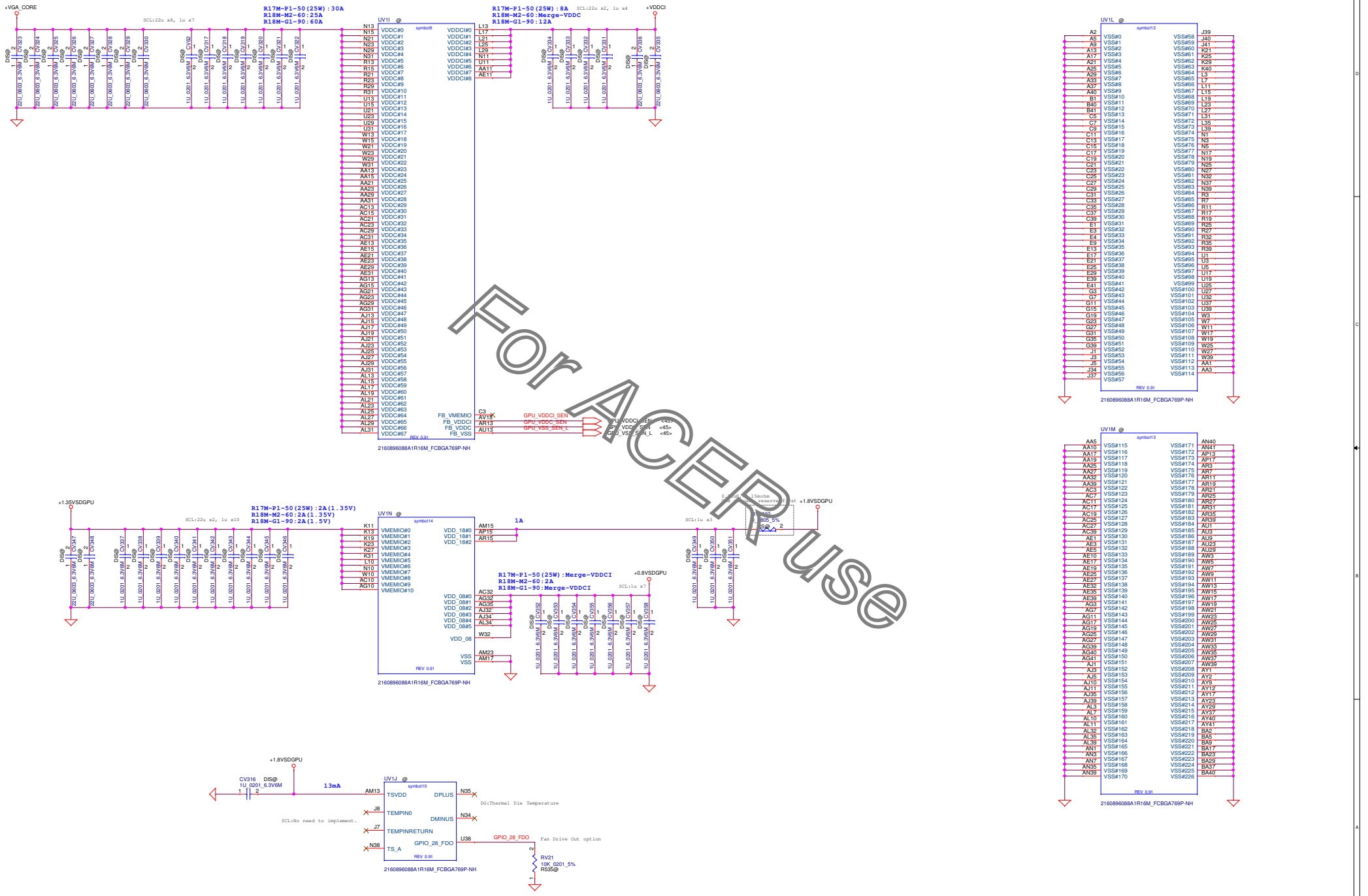
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: R18M-M260/G19_(5/9)_DISPLAY

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

Date: Monday, December 25, 2017 Sheet 19 of 48



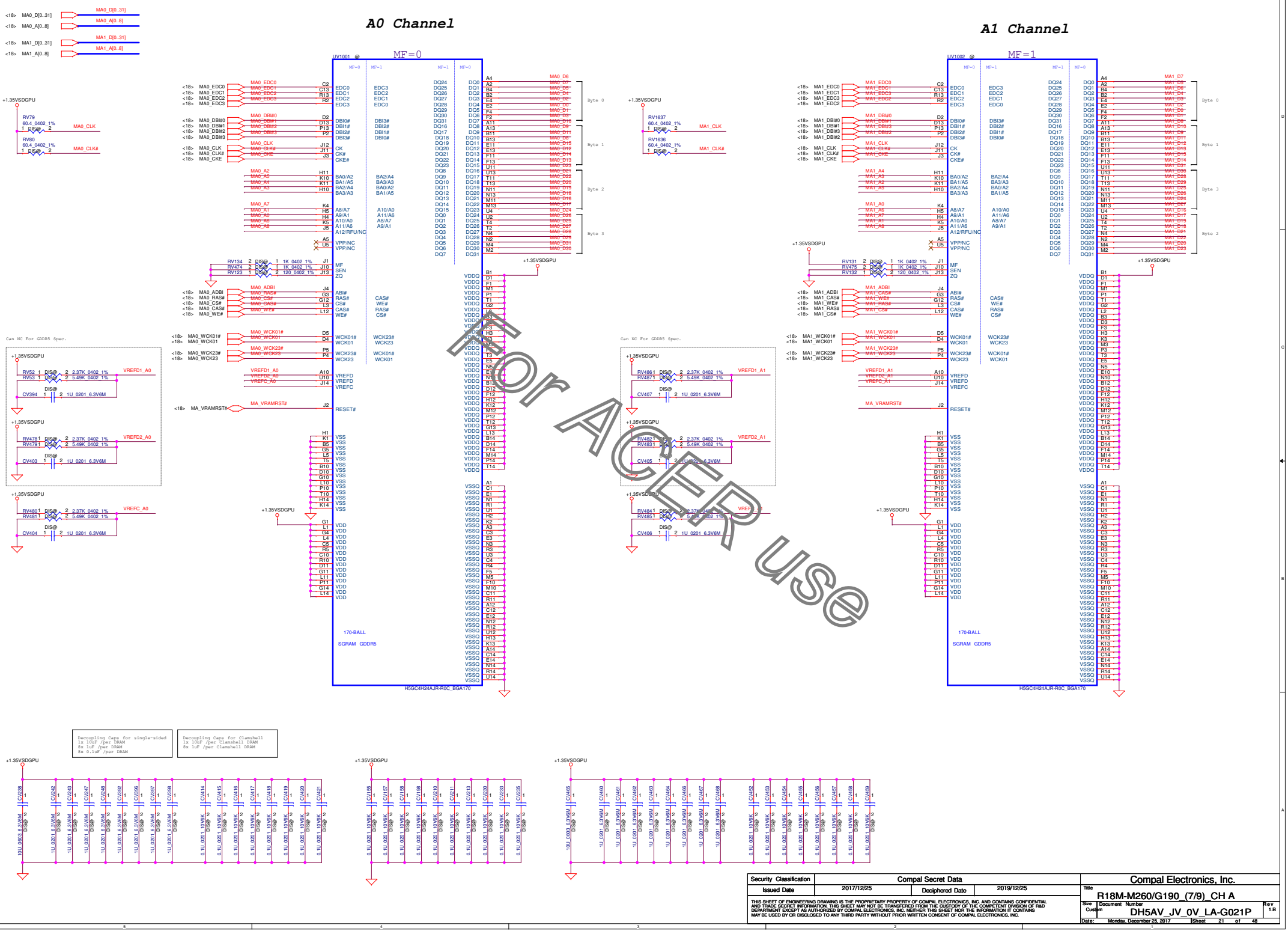
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: R18M-M260/G19_(6/9)_PWR/GND

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

Date: Monday, December 25, 2017 | Sheet 20 of 48



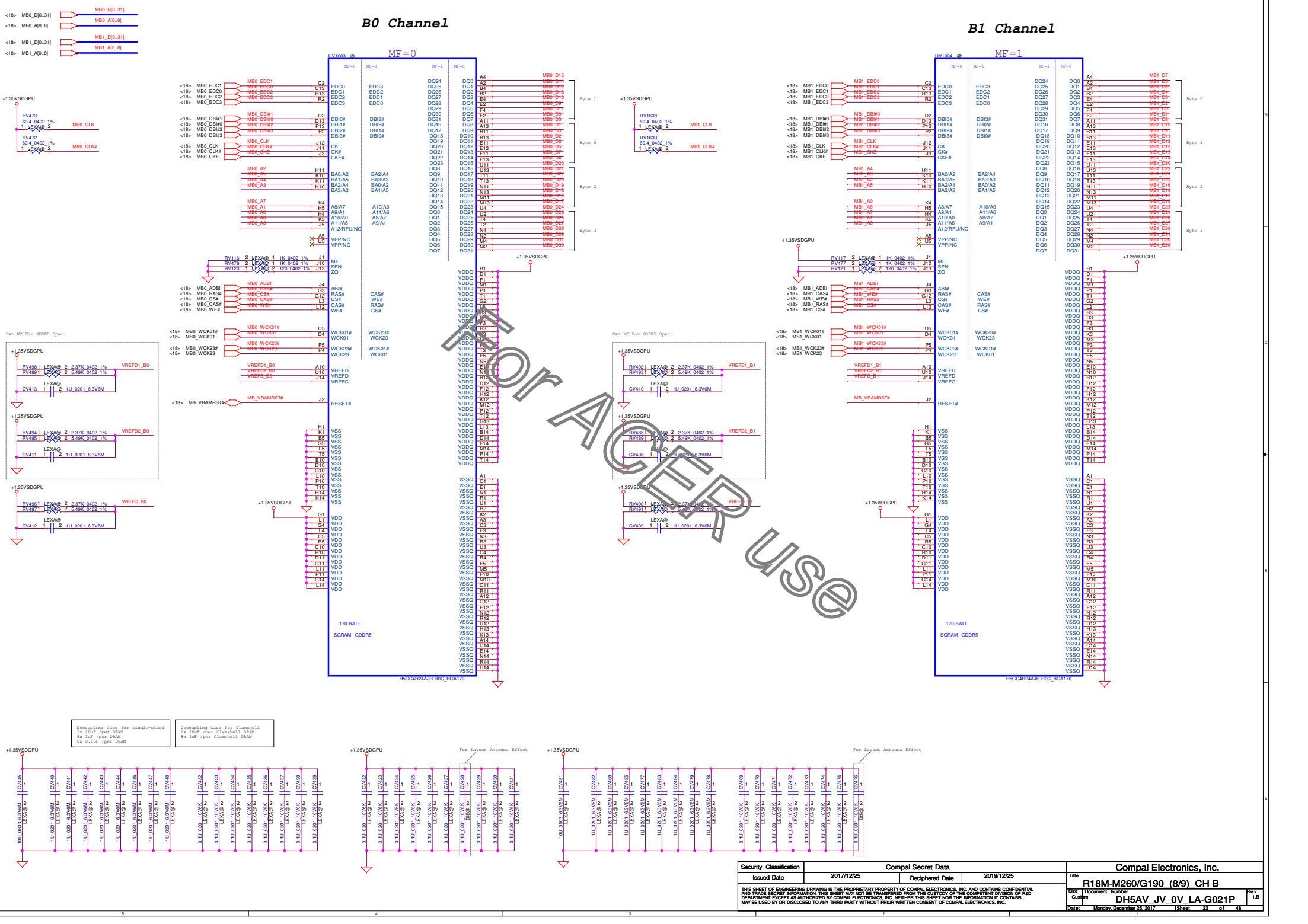
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: R18M-M260/G190_(7/9)_CH A

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

Date: Monday, December 25, 2017 Sheet 21 of 48



Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

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Compal Electronics, Inc.

Title: R18M-M260/G190_(8/9)_CH B

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

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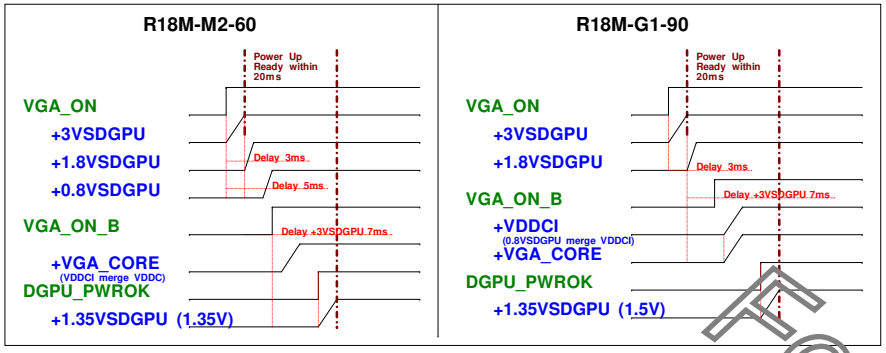
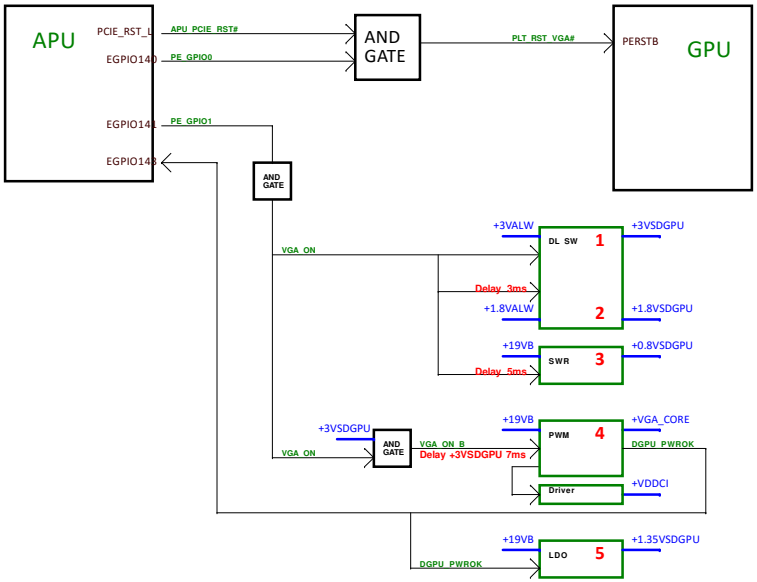
5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.





For AMD R17M-P1-50/R18M-M2-60/R18M-G1-90 VRAM

Memory ID/Vendor/Size	Memory PN R3(ABO!) A0	Memory PN R3(ABO!) A1	Memory PN R3(ABO!) B0	Memory PN R3(ABO!) B1
000 SAMSUNG (5Gb) (6Gb) 256M x32	UV1001 V4G_S@ UV1001 PV4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABO! SA00009HR30	UV1002 V4G_S@ UV1002 PV4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABO! SA00009HR30	UV1003 V4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABO! SA00009HR30	UV1004 V4G_S@ S IC D5 256M32 K4G80325FB-HC03 FBGA ABO! SA00009HR30
001 HYNIX (5Gb) (6Gb) 256M x32	UV1001 V4G_H@ UV1001 PV4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABO! SA00009ZG20	UV1002 V4G_H@ UV1002 PV4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABO! SA00009ZG20	UV1003 V4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABO! SA00009ZG20	UV1004 V4G_H@ S IC D5 256M32 H5GC8H24MJR-T2C BGA ABO! SA00009ZG20
010 SAMSUNG (5Gb) 128M x32	UV1001 V2G_S@ UV1001 PV2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABO! SA00009T130	UV1002 V2G_S@ UV1002 PV2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABO! SA00009T130	UV1003 V2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABO! SA00009T130	UV1004 V2G_S@ S IC D5 128M32 K4G41325FE-HC28 FBGA ABO! SA00009T130
011 HYNIX (5Gb) 128M x32	UV1001 V2G_H@ UV1001 PV2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABO! SA000085V70	UV1002 V2G_H@ UV1002 PV2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABO! SA000085V70	UV1003 V2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABO! SA000085V70	UV1004 V2G_H@ S IC D5 128M322.5G H5GC4H24AJR-T2C ABO! SA000085V70
100 MICRON (5Gb) (6Gb) 256M x32	UV1001 V4G_M@ UV1001 PV4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABO! SA000096K30	UV1002 V4G_M@ UV1002 PV4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABO! SA000096K30	UV1003 V4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABO! SA000096K30	UV1004 V4G_M@ S IC D5 256M32 MT51J256M32HF-60A ABO! SA000096K30

For AMD R18M-G1-90 VRAM Table (7Gb)

Memory ID/Vendor/Size	Memory PN R3(ABO!) A0	Memory PN R3(ABO!) A1	Memory PN R3(ABO!) B0	Memory PN R3(ABO!) B1
000 SAMSUNG (7Gb) 256M x32	UV1001 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABO! SA000092D00	UV1002 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABO! SA000092D00	UV1003 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABO! SA000092D00	UV1004 V4G_S7G@ S IC D5 256M32 K4G80325FB-HC28 FBGA ABO! SA000092D00
001 HYNIX (7Gb) 256M x32	UV1001 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABO! SA00009U110	UV1002 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABO! SA00009U110	UV1003 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABO! SA00009U110	UV1004 V4G_H7G@ S IC D5 256M32 H5GC8H24MJR-R0C BGA ABO! SA00009U110
100 MICRON (7Gb) 256M x32	UV1001 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABO! SA00009TV10	UV1002 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABO! SA00009TV10	UV1003 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABO! SA00009TV10	UV1004 V4G_M7G@ S IC D5 256M32 MT51J256M32HF-70A ABO! SA00009TV10

AMD GPU PN

R17M-P1-50 PN R3(ROH)

UV1 RX540@

S IC 216-0905018 A1 R17M-P1-50 ABO!
SA0000ALV20

R18M-M2-60 PN R1(ROH)

UV1 R535@

S IC 216-0915006 A0 R18M-M2-60 FCBGA 769P GPU 0FA
SA0000BFE00

R18M-G1-90 PN R1(ROH)

UV1 RX565@

S IC 215-090800[illegible] 769P GPU 0FA
SA0000BFF00

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: R18M-M260/G190 (9/9) NOTE

Size: | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.8

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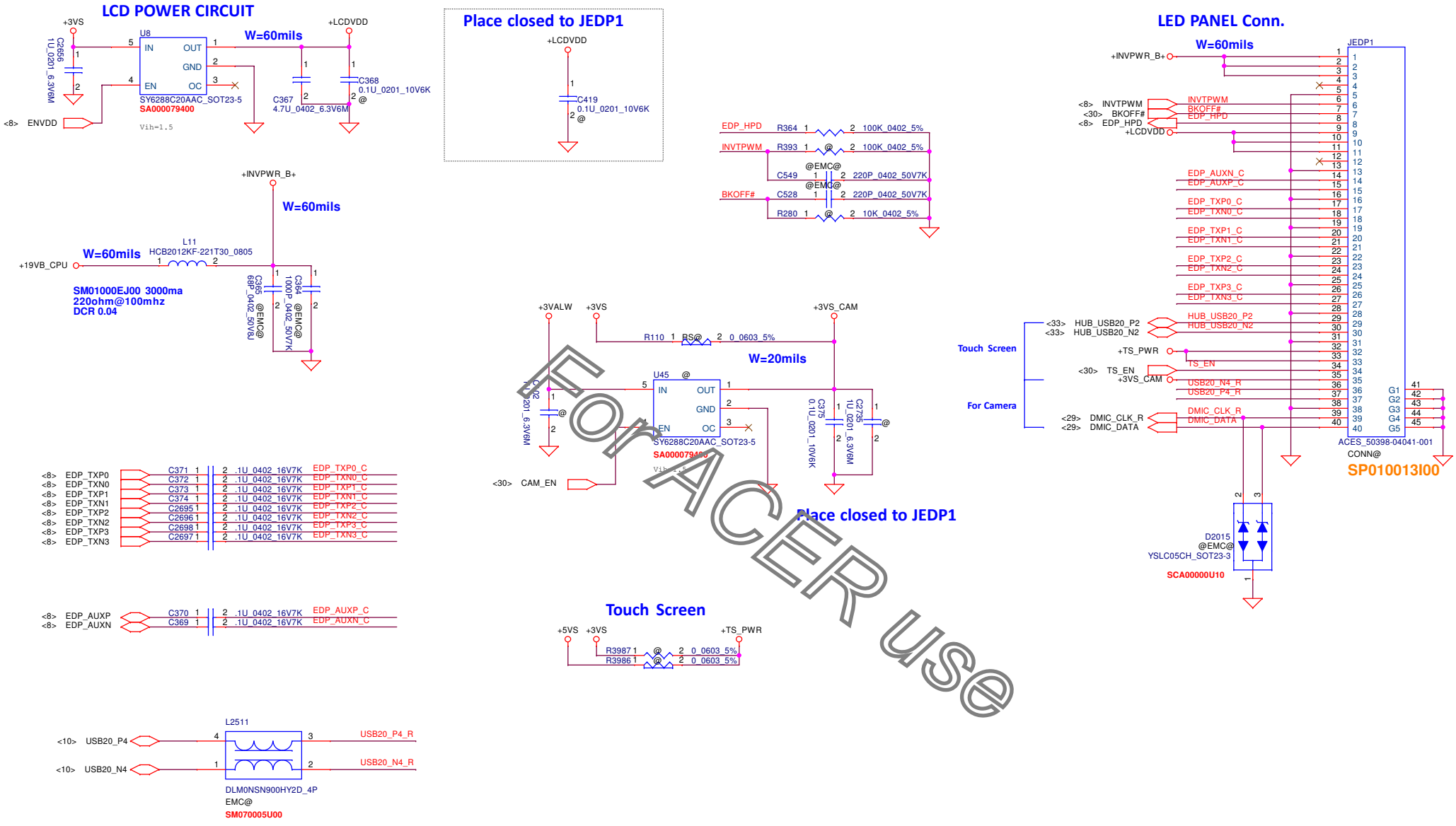

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: EDP/CAMERA/DMIC

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

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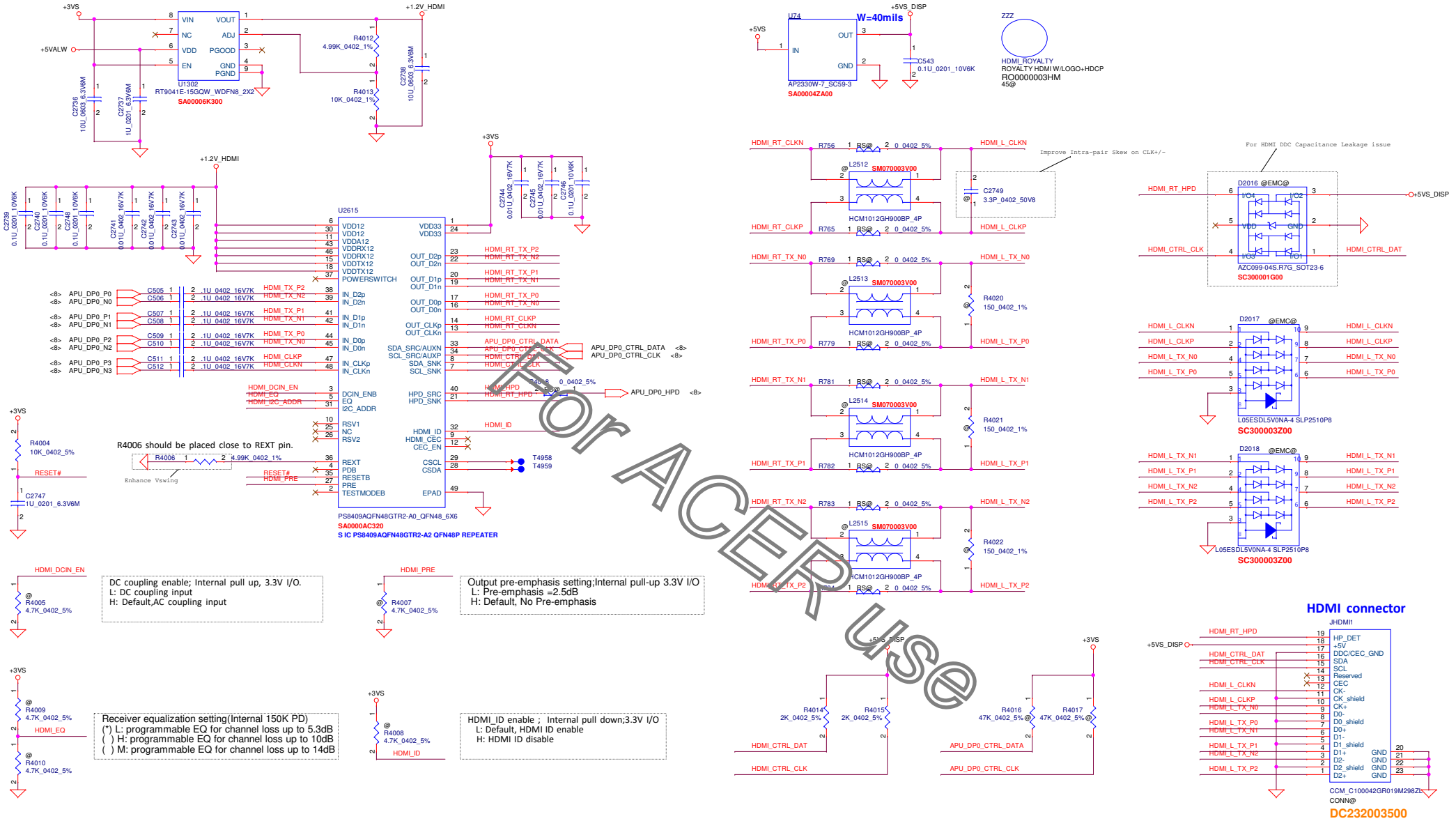

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: HDMI REDRIVER (PS8409)

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

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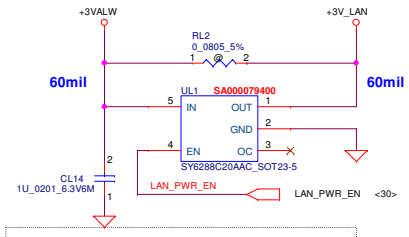
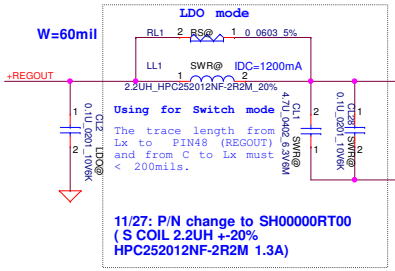
LAN-RTL8411B

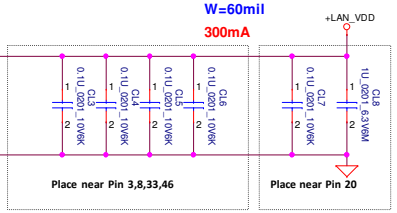


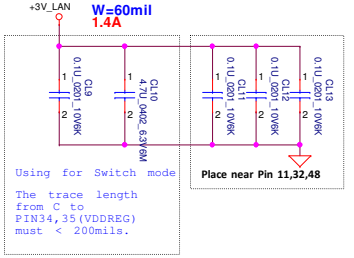
From EC

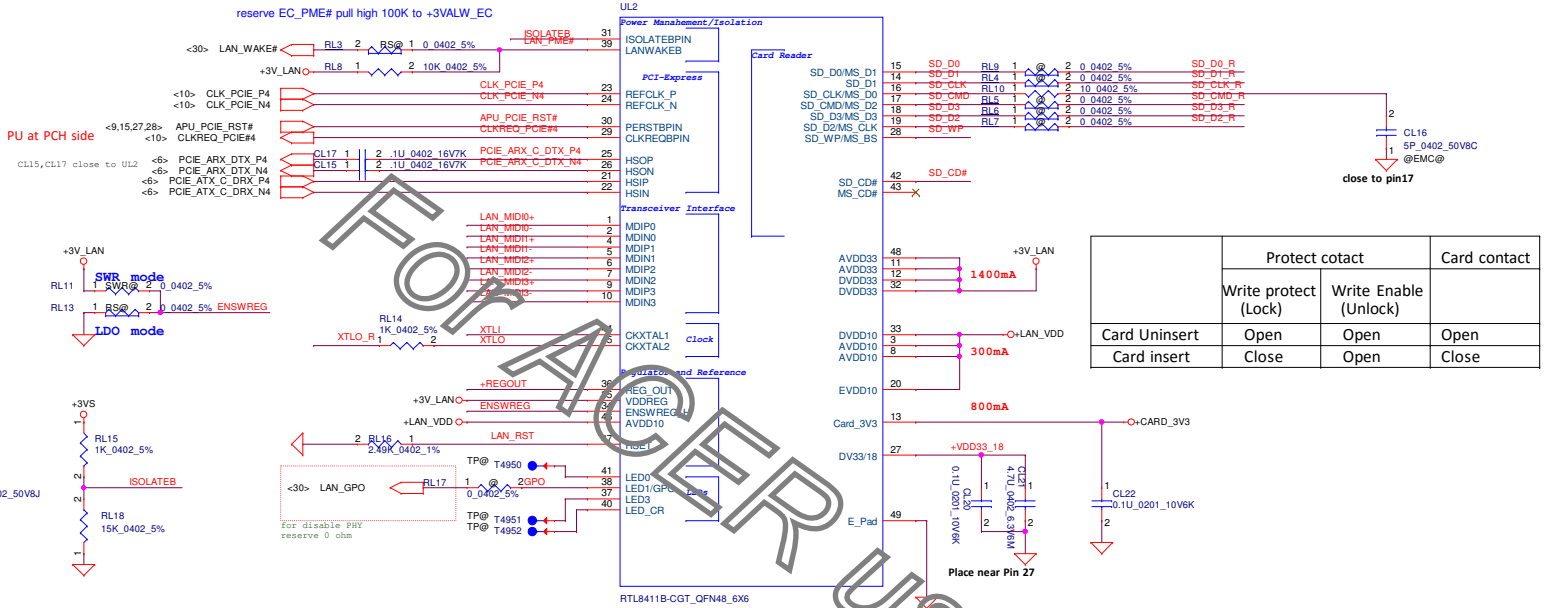
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms

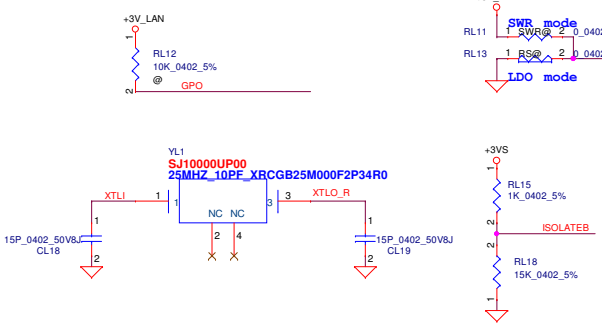


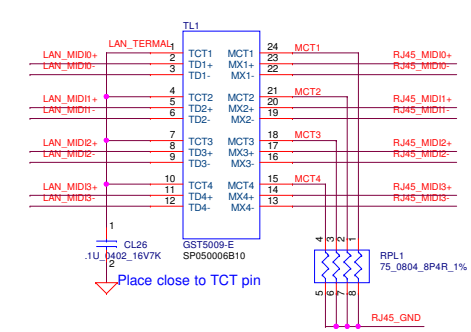




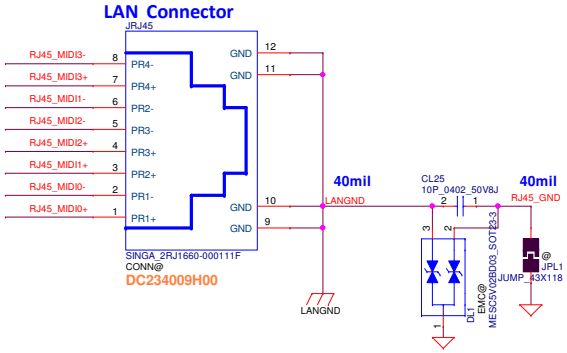


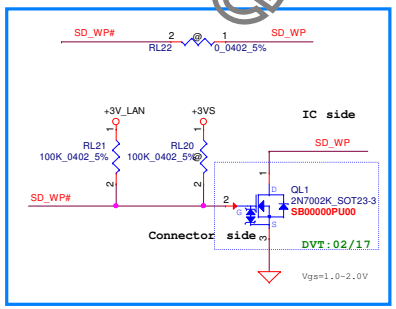
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Close	Open	Close



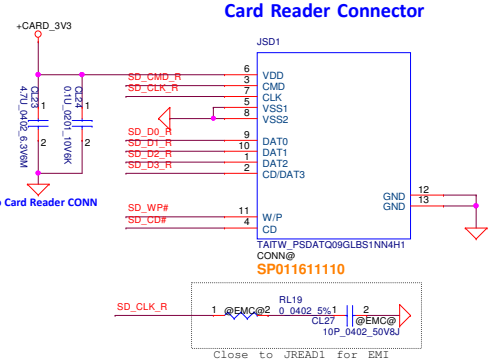


LAN Connector





Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title	LAN RTL8411-CG
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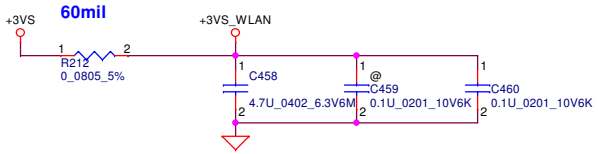
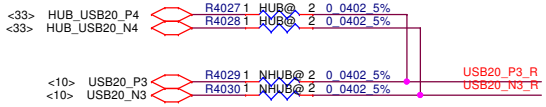
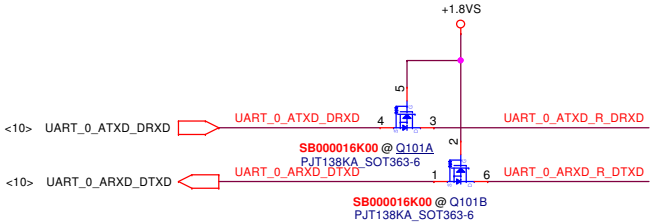
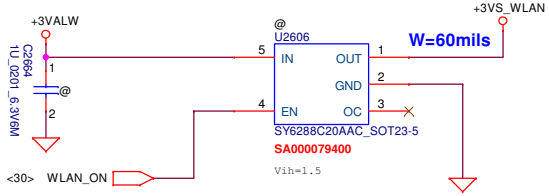
Wireless LAN

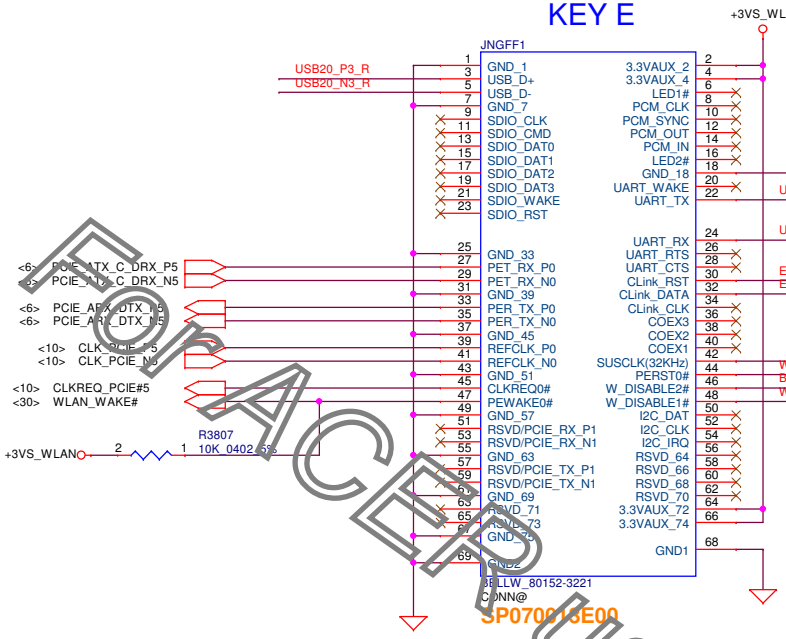


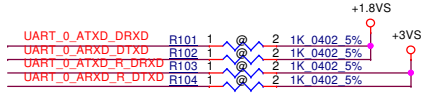






KEY E





NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_SRC/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I)(O/3.3)	GND	63
60	I2C CLK (O)(O/3.3)	Reserved/PETn1	61
58	I2C DATA (I/O)(O/3.3)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(O/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(O/3.3V)	PEWake0# (I/O)(O/3.3V)	55
52	PERST0# (O)(O/3.3V)	CLKREQ0# (I/O)(O/3.3V)	53
50	SUSCLK(32kHz) (O)(O/3.3V)	GND	51
48	COEX1 (I/O)(O/1.8V)	REFCLKN0	49
46	COEX2(I/O)(O/1.8V)	REFCLKP0	47
44	COEX3(I/O)(O/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(O/1.8V)	PETn0	37
34	UART CTS (I)(O/1.8V)	PETp0	35
32	UART Tx (O)(O/1.8V)	GND	33
	Reserved for Coex3	Reserved for Coex3	
	Reserved for Coex2	Reserved for Coex2	
	Reserved for Coex1	Reserved for Coex1	
	Reserved for Coex0	Reserved for Coex0	
	Reserved for WLAN/BT Antenna Control	Reserved for WLAN/BT Antenna Control	
22	UART Rx (I)(O/1.8V)	SDIO Reset# (O)(O/1.8V)	23
20	UART Wake# (I)(O/3.3V)	SDIO Wake# (I)(O/1.8V)	21
18	GND	SDIO DAT3(I/O)(O/1.8V)	19
16	LED#2 (I)(OD)	SDIO DAT2(I/O)(O/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(O/1.8V)	SDIO DAT1(I/O)(O/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(O/1.8V)	SDIO DAT0(I/O)(O/1.8V)	13
10	PCM_SYNC/I2S WS (O)(O/1.8V)	SDIO CMD(I/O)(O/1.8V)	11
8	PCM_CLK/I2S SCK (O)(O/1.8V)	SDIO CLK(O)(O/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: M.2 KEY-E (WLAN)

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

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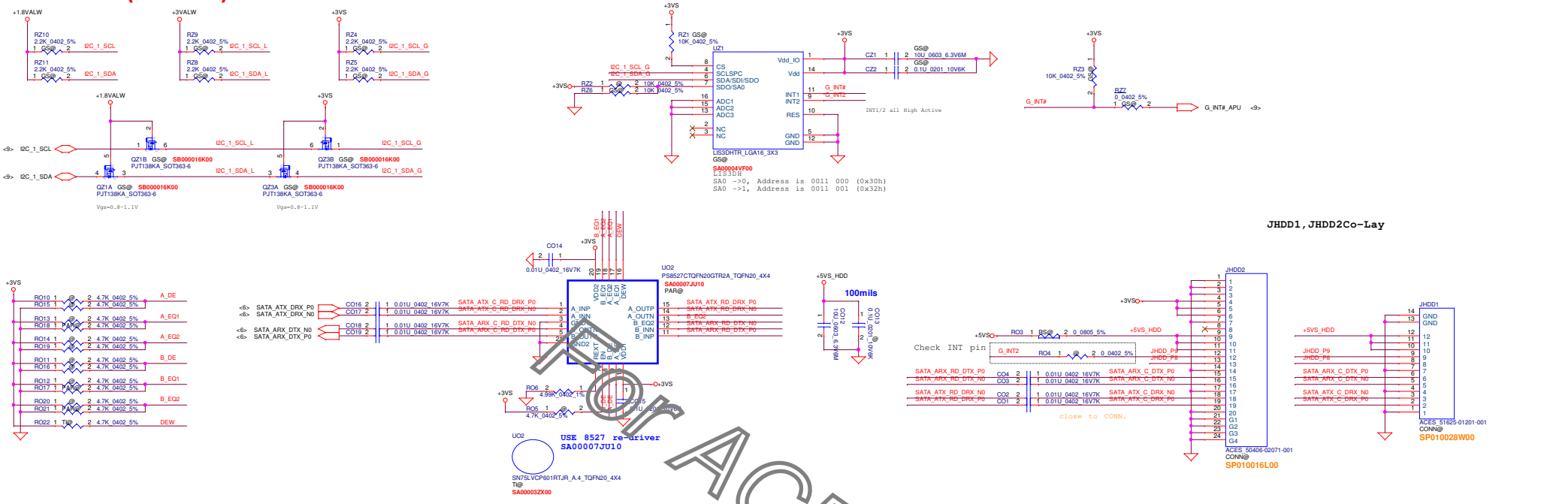
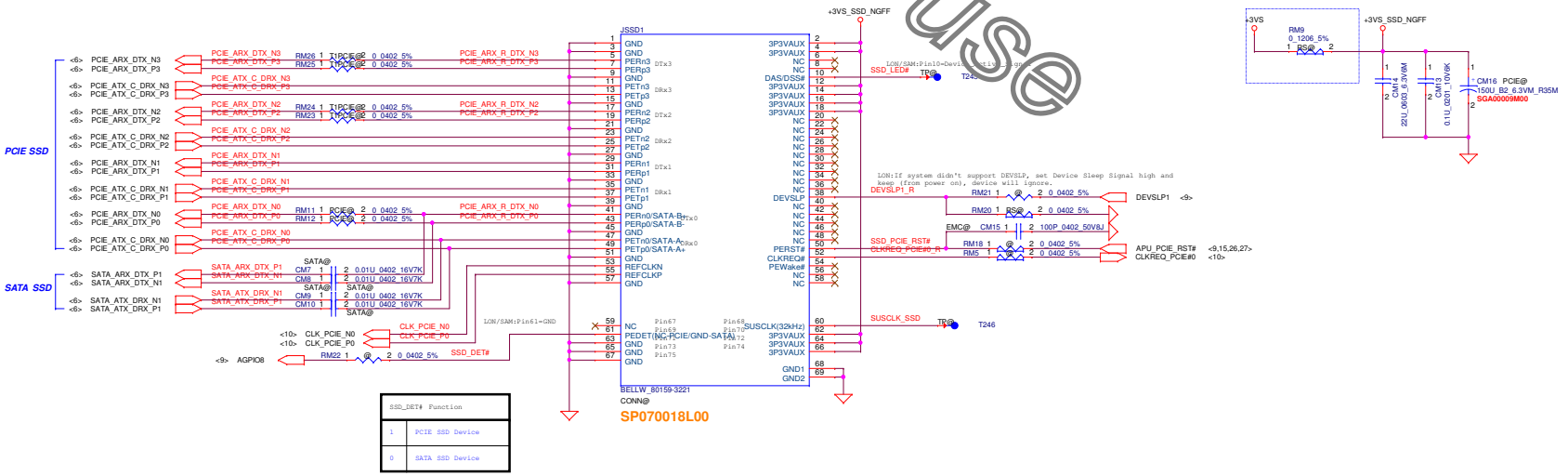
SATA Re-Driver and cable HDD Conn.

G-Sensor (reserved)



SATA NGFF SSD Conn.



SSD_DET# Function	
1	PCIE SSD Device
0	SATA SSD Device

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.	
Title	HDD/SSD
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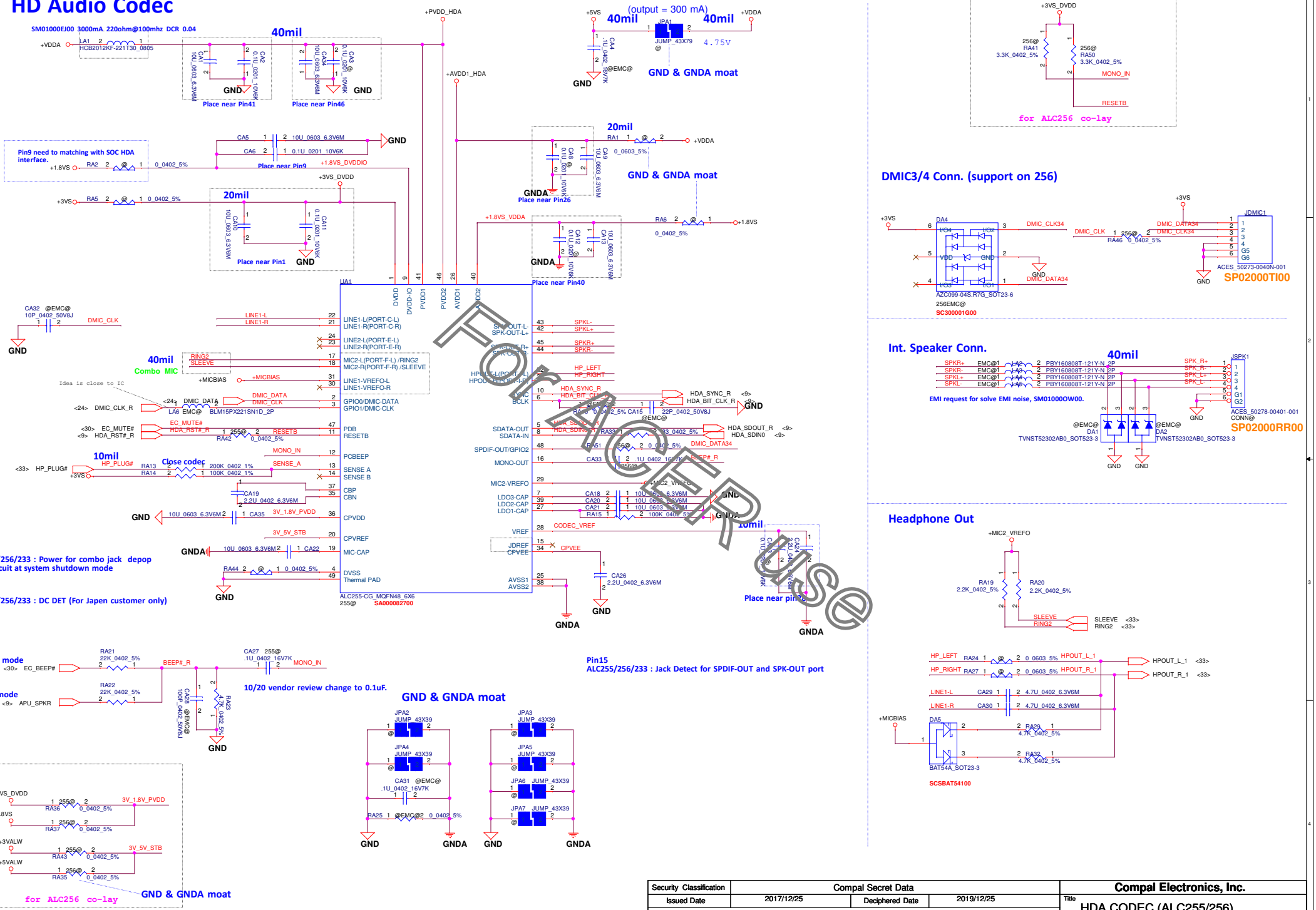
HD Audio Codec



DMIC3/4 Conn. (support on 256)

Int. Speaker Conn.

Headphone Out

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.	
Title	HDA CODEC (ALC255/256)
Size / Document Number	DH5AV_JV_0V_LA-G021P
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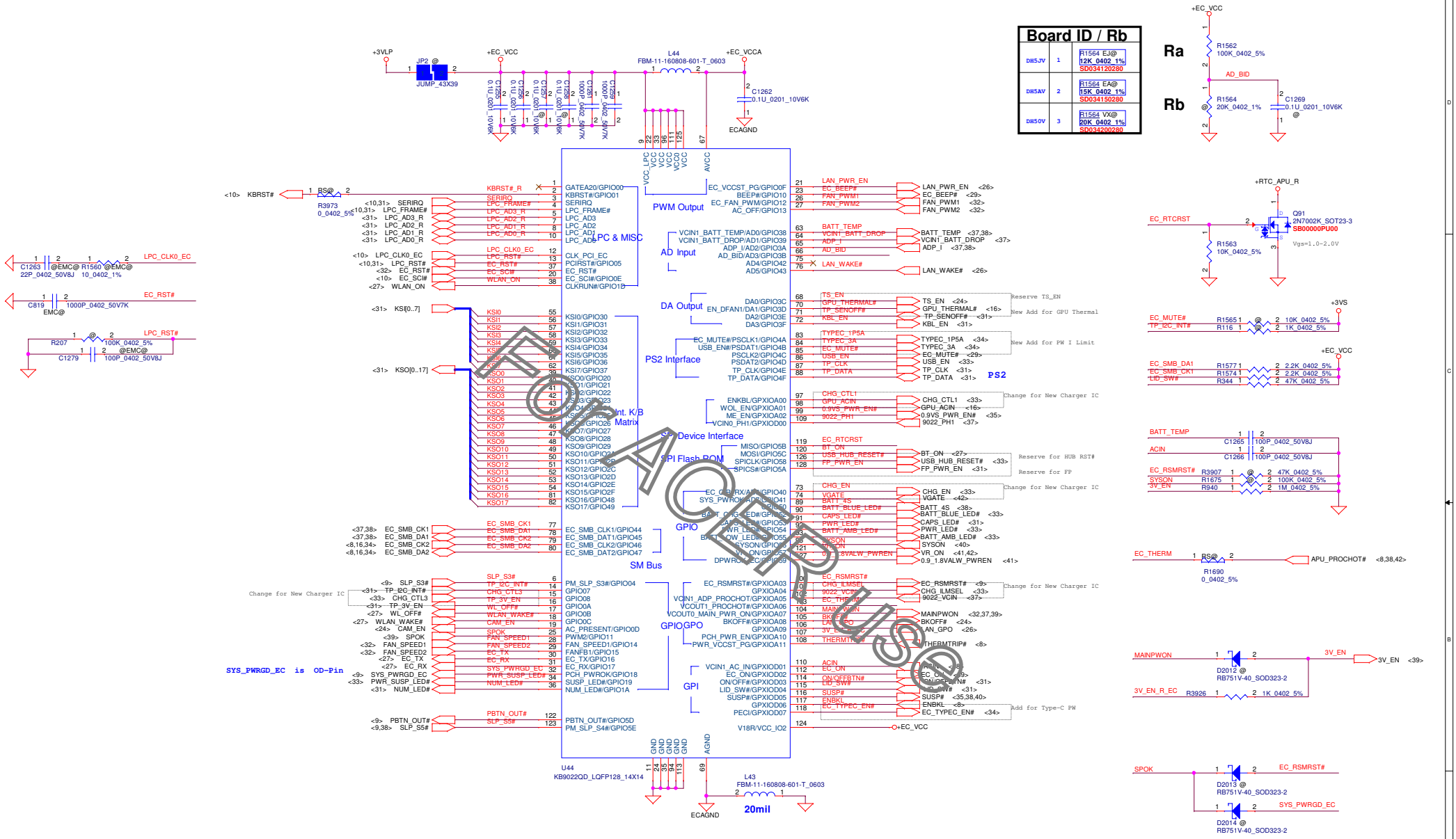
Board ID / Rb
DH5JV 1 R1564 EJ@ 12K_0402_1% SD034120280
DH5AV 2 R1564 EA@ 15K_0402_1% SD034150280
DH5OV 3 R1564 VX@ 20K_0402_1% SD034200280
Ra
Rb
+EC_VCC
R1562 100K_0402_5%
AD_BID
R1564 20K_0402_1%
C1269 0.1U_0201_10V6K
+3VLP
JP2 @
JUMPER_43X39
+EC_VCCA
L44 FBM-11-160808-601-T_0603
C1262 0.1U_0201_10V6K
ECAGND
KBRST#
R3973 0_0402_5%
SERIRQ
LPC_FRAME#
LPC_AD3_R
LPC_AD2_R
LPC_AD1_R
LPC_AD0_R
LPC_CLK0_EC
EC_RST#
EC_SCI#
WLAN_ON
KSI[0..7]
KSO[0..17]
EC_SMB_CK1
EC_SMB_DA1
EC_SMB_CK2
EC_SMB_DA2
SLP_S3#
TP_I2C_INT#
CHG_CTL3
TP_3V_EN
WL_OFF#
WLAN_WAKE#
CAM_EN
SPOK
FAN_SPEED1
FAN_SPEED2
EC_TX
EC_RX
SYS_PWRGD_EC
PWR_SUSP_LED#
NUM_LED#
PBTN_OUT#
SLP_S5#
SYS_PWRGD_EC is OD-Pin
Change for New Charger IC
U44
KB9022QD_LQFP128_14X14
PWM Output
PC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
LAN_PWR_EN
EC_BEEP#
FAN_PWM1
FAN_PWM2
BATT_TEMP
VCIN1_BATT_DROP
ADP_I
AD_BID
LAN_WAKE#
TS_EN
GPU_THERMAL#
TP_SENOFF#
KBL_EN
TYPEC_1P5A
TYPEC_3A
EC_MUTE#
USB_EN
TP_CLK
TP_DATA
CHG_CTL1
GPU_ACIN
0.9VS_PWR_EN#
9022_PH1
EC_RTCRST
BT_ON
USB_HUB_RESET#
FP_PWR_EN
CHG_EN
VGATE
BATT_4S
BATT_BLUE_LED#
CAPS_LED#
PWR_LED#
BATT_AMB_LED#
SYSON
VR_ON
0.9_1.8VALW_PWREN
EC_RSMRST#
CHG_ILMSEL
9022_VCIN
MAINPWON
BKOFF#
LAN_GPO
3V_EN
THERMTRIP#
ACIN
EC_ON
ON/OFFBTN#
LID_SW#
SUSP#
ENBKL
EC_TYPEC_EN#
+EC_VCC
Reserve TS_EN
New Add for GPU Thermal
New Add for PW I Limit
PS2
Reserve for HUB RST#
Reserve for FP
Change for New Charger IC
Add for Type-C PW
+RTC_APU_R
Q91 2N7002K_SOT23-3 SB00000PU00
Vgs=1.0~2.0V
EC_RTCRST
R1563 10K_0402_5%
+3VS
EC_MUTE#
TP_I2C_INT#
R1565 10K_0402_5%
R116 2K_0402_5%
+EC_VCC
EC_SMB_DA1
EC_SMB_CK1
LID_SW#
R1577 2.2K_0402_5%
R1574 2.2K_0402_5%
R344 47K_0402_5%
BATT_TEMP
ACIN
C1265 100P_0402_50V8J
C1266 100P_0402_50V8J
EC_RSMRST#
SYSON
3V_EN
R3907 47K_0402_5%
R1675 100K_0402_5%
R940 1M_0402_5%
EC_THERM
R1690 0_0402_5%
APU_PROCHOT#
MAINPWON
3V_EN
D2012 @ RB751V-40_SOD323-2
3V_EN_R_EC
R3926 1K_0402_5%
SPOK
EC_RSMRST#
D2013 @ RB751V-40_SOD323-2
SYS_PWRGD_EC
D2014 @ RB751V-40_SOD323-2
LPC_CLK0_EC
C1263 22P_0402_50V8J
@EMC@ R1560 10_0402_1%
@EMC@
EC_RST#
C819 1000P_0402_50V7K
EMC@
LPC_RST#
R207 100K_0402_5%
C1279 100P_0402_50V8J
@EMC@
20mil
Security Classification: Compal Secret Data
Issued Date: 2017/12/25
Deciphered Date: 2019/12/25
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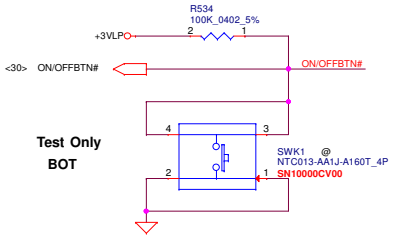
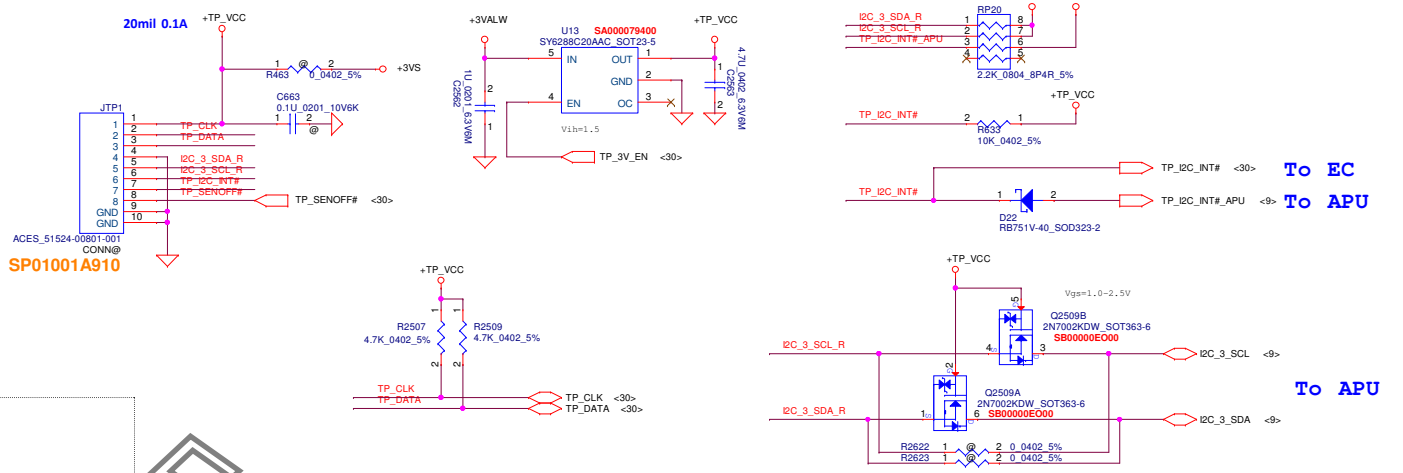
Title: EC ENE-KB9022
Size: Custom
Document Number: DH5AV_JV_0V_LA-G021P
Rev: 1.B
Date: Monday, December 25, 2017
Sheet 30 of 48

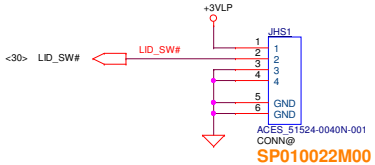
ON/OFF BTN



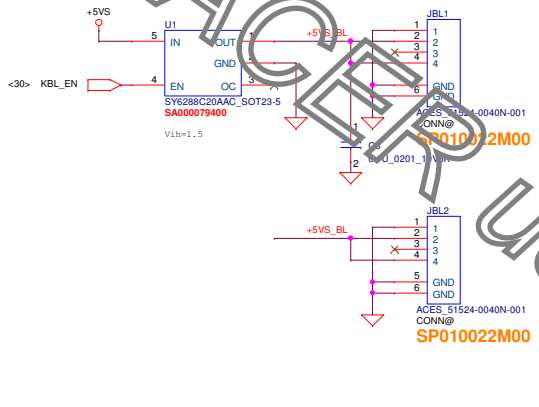
TP/B Conn.



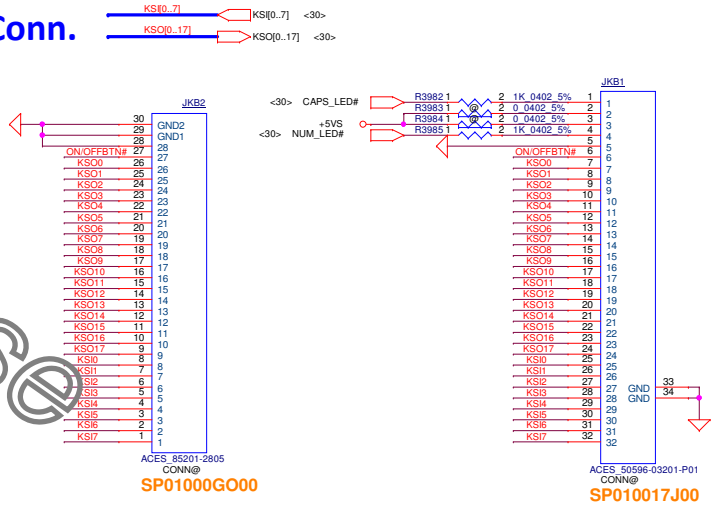
Lid Switch (Hall Effect Switch)



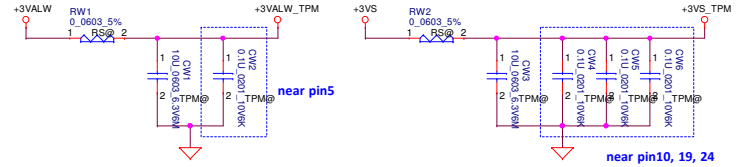
KB BackLight



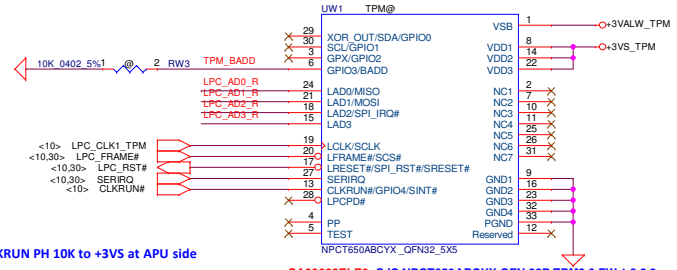
KB Conn.



TPM



BADD	SELECTION
* 1	AEh(write), AFh(read)

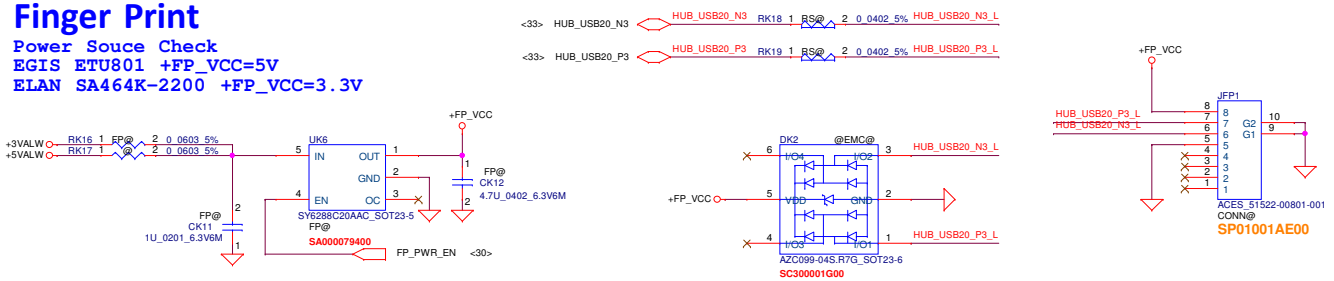


Finger Print

Power Souce Check

EGIS ETU801 +FP_VCC=5V

ELAN SA464K-2200 +FP_VCC=3.3V



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: KB/TP/TPM/LID

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

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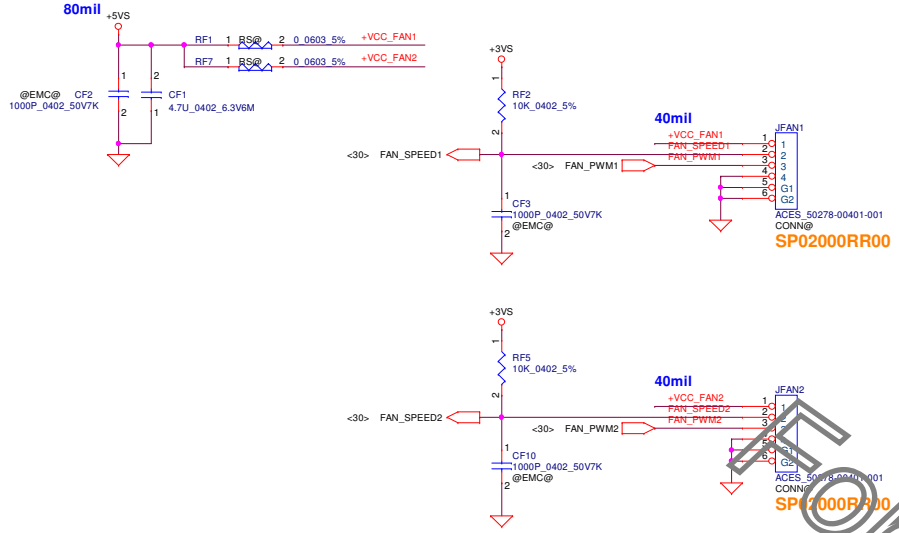
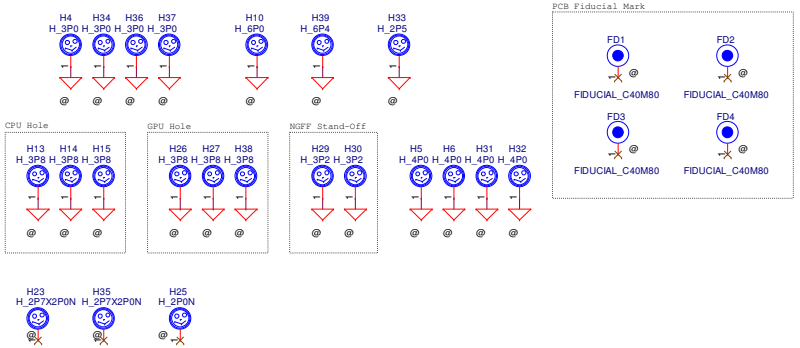
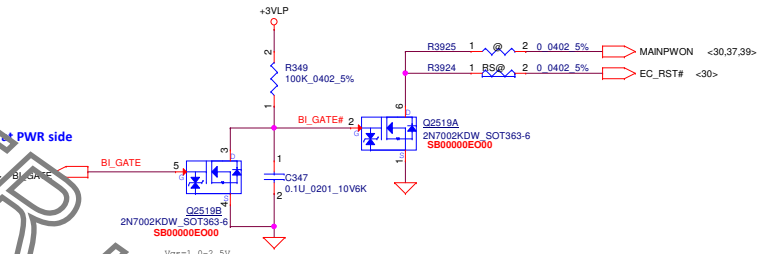
FAN Conn



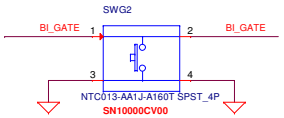
Screw Hole



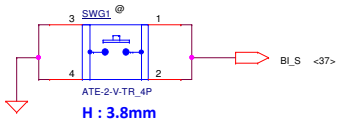
Reset Circuit



Reset Button



BI SW



Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: FAN/BATT RESET_DEGUB SW

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

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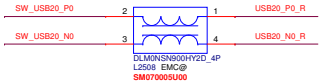
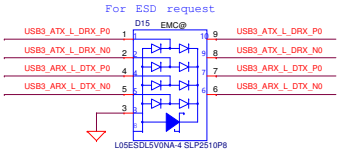
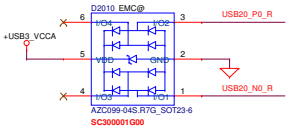
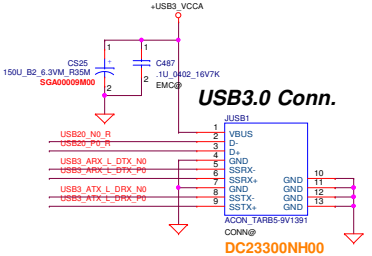
USB3.0 (Port 0)

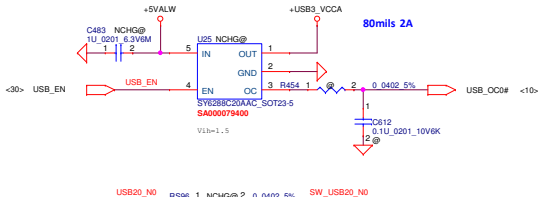


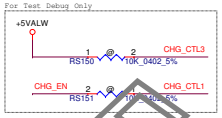


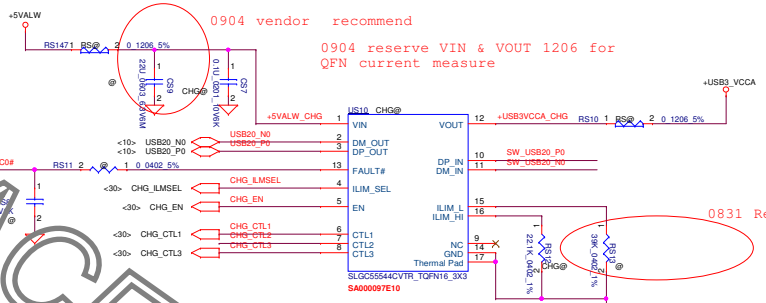


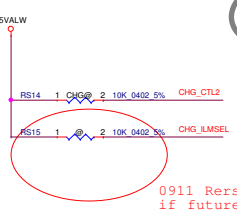


Non-Charger Co-lay





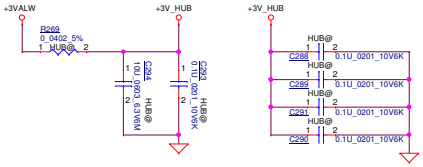




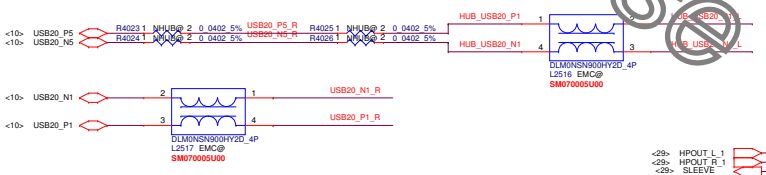
USB Host Charger Truth Table

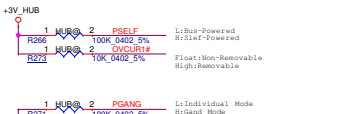
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

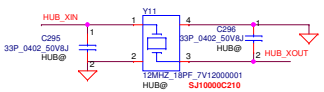
USB HUB

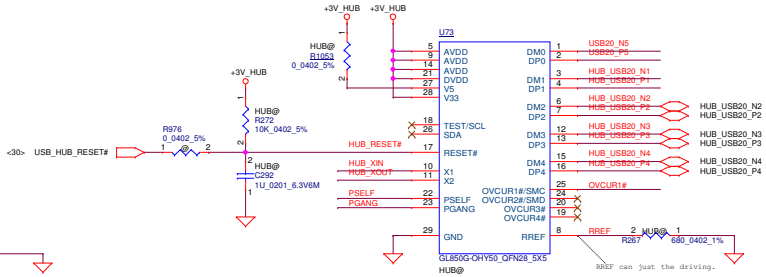


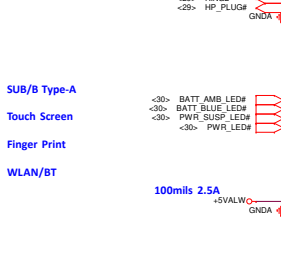
C279 close to U73 pin5
C280 close to U73 pin9
C283 close to U73 pin14
C284 close to U73 pin21

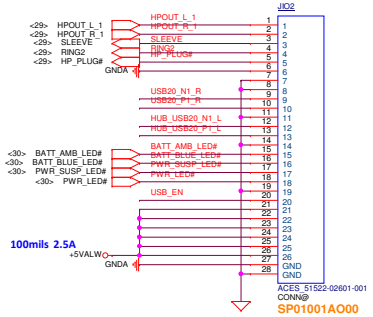












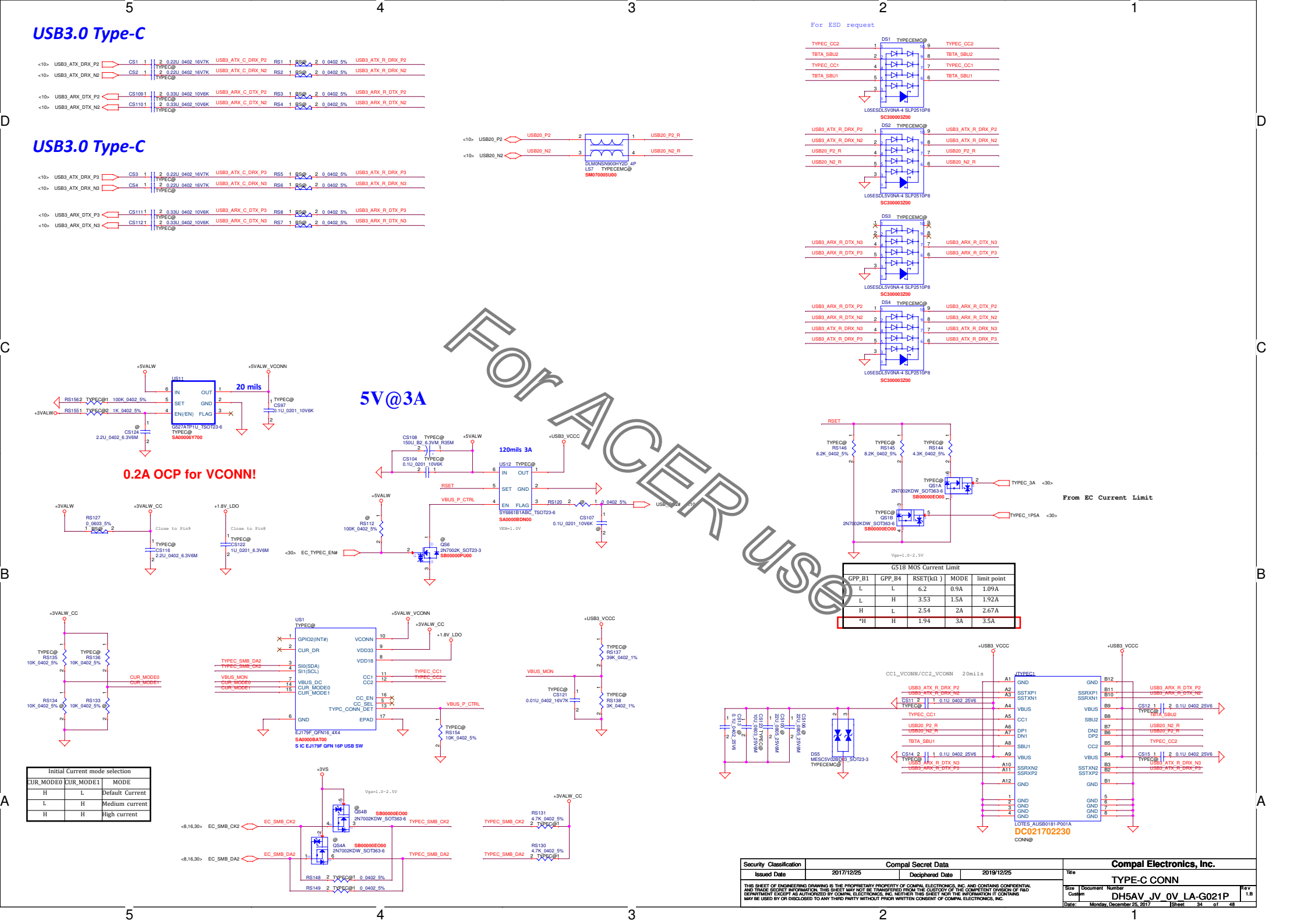
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: USB30/USB HUB/LED

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

Date: Monday, December 25, 2017 | Sheet 33 of 48


USB3.0 Type-C
USB3.0 Type-C
For ESD request
5V@3A
20 mils
120mils 3A
0.2A OCP for VCONN!
From EC Current Limit
For ACER use
G518 MOS Current Limit
GPP_B1 | GPP_B4 | RSET(kΩ) | MODE | limit point
L | L | 6.2 | 0.9A | 1.09A
L | H | 3.53 | 1.5A | 1.92A
H | L | 2.54 | 2A | 2.67A
*H | H | 1.94 | 3A | 3.5A
Initial Current mode selection
CUR_MODE0 | CUR_MODE1 | MODE
H | L | Default Current
L | H | Medium current
H | H | High current
Security Classification | Compal Secret Data
Issued Date | 2017/12/25 | Deciphered Date | 2019/12/25
Compal Electronics, Inc.
TYPE-C CONN
DH5AV_JV_0V_LA-G021P
Rev 1.B
Monday, December 25, 2017
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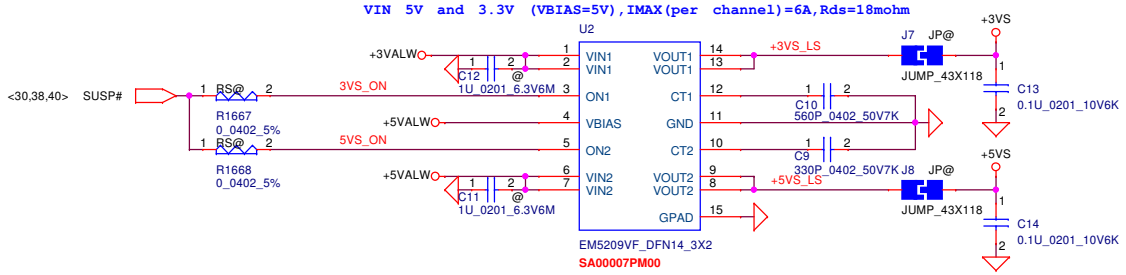

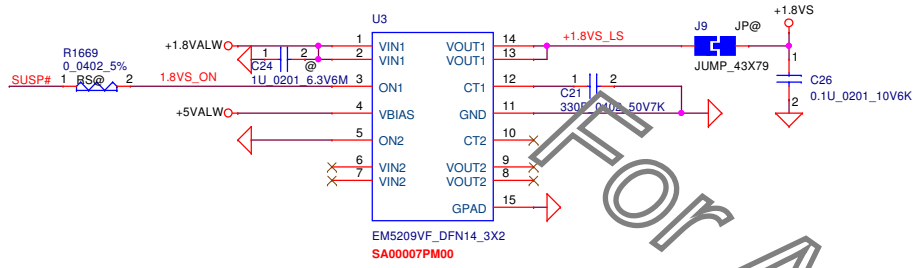

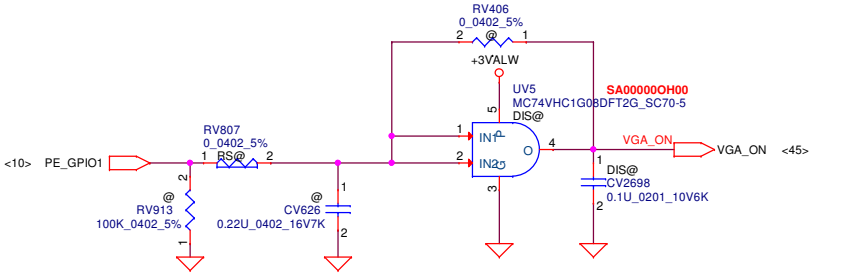

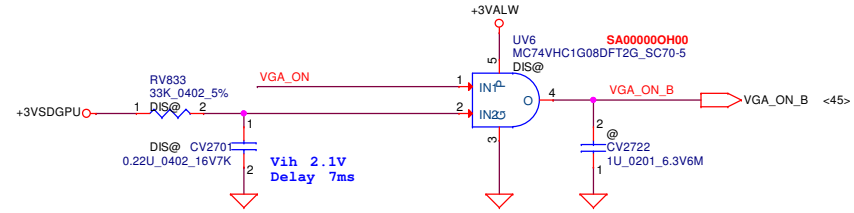

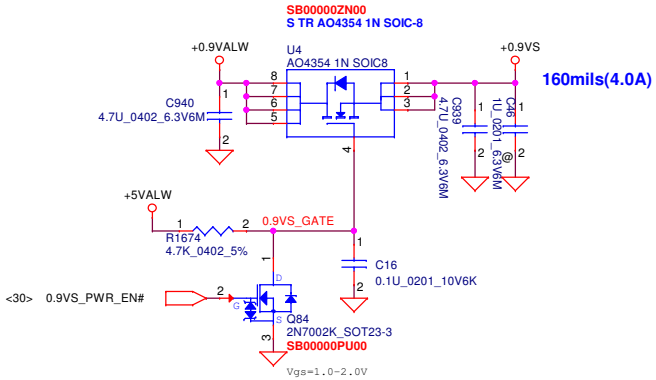

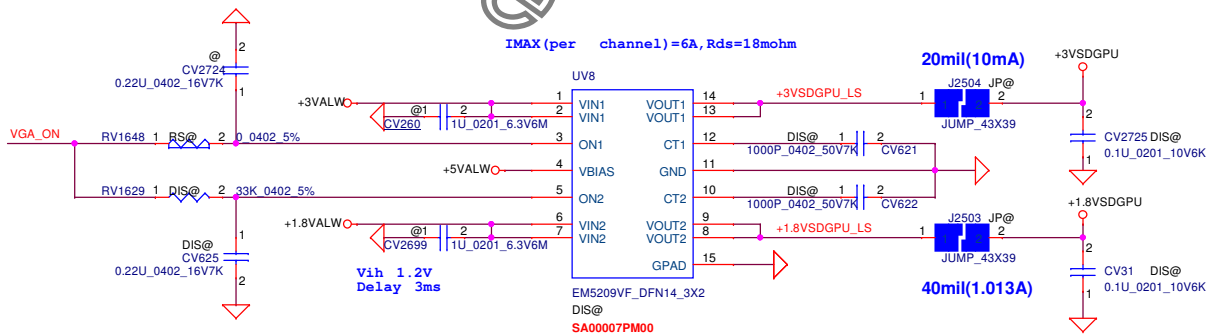

+3VALW TO +3VSDGPU
+1.8VALW TO +1.8VSDGPU

Security Classification	Compal Secret Data		
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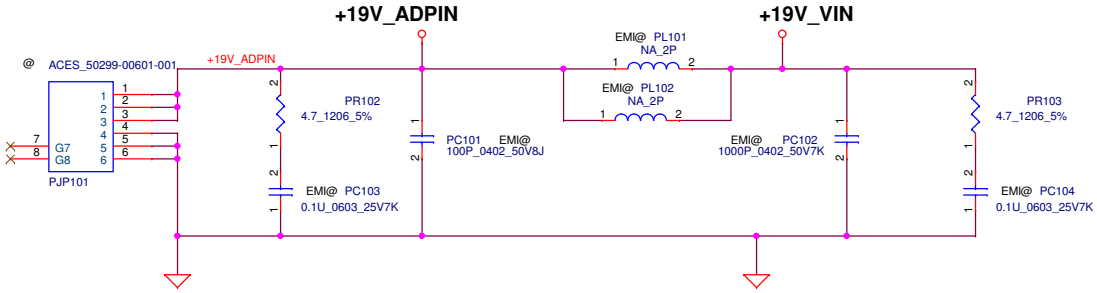
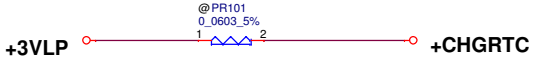
Compal Electronics, Inc.

Title: DC INTERFACE

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

Date: Monday, December 25, 2017 Sheet 35 of 48





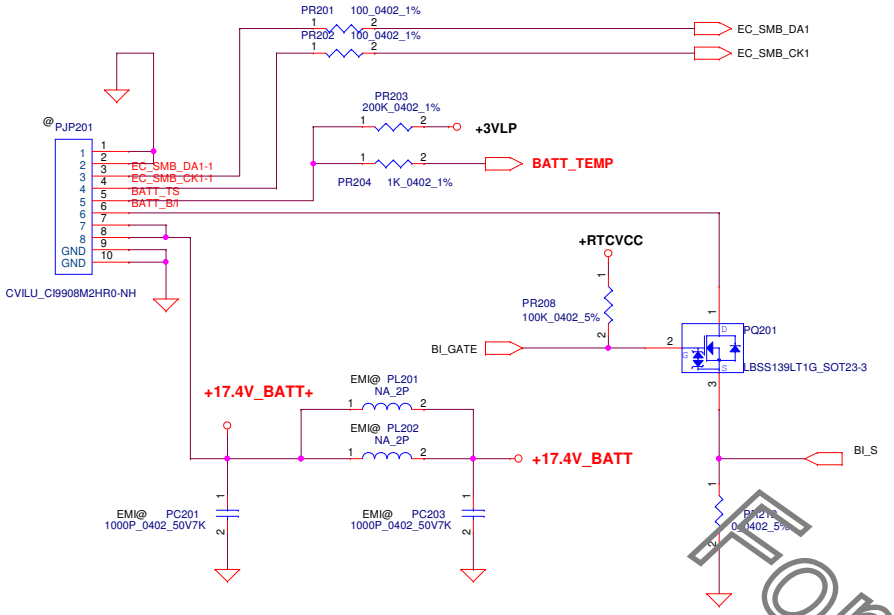
Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

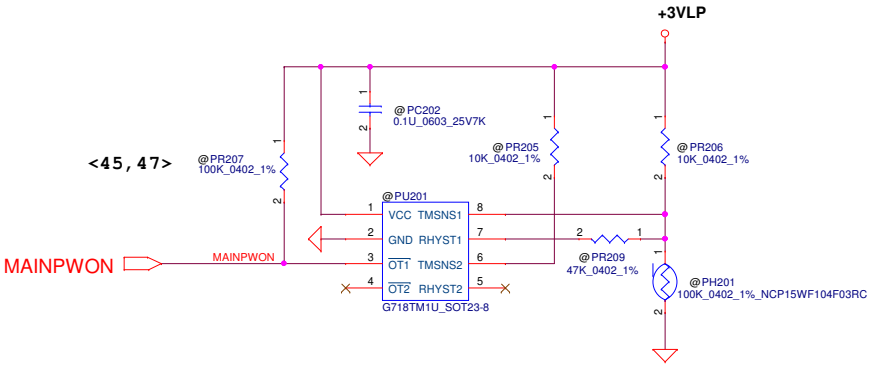
Compal Electronics, Inc.

Title: DCIN

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

Date: Monday, December 25, 2017 Sheet 36 of 48





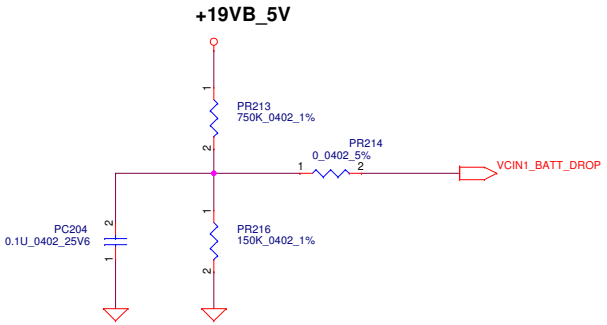
For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.V
PH202(ohm)	7.3092K	26.11K

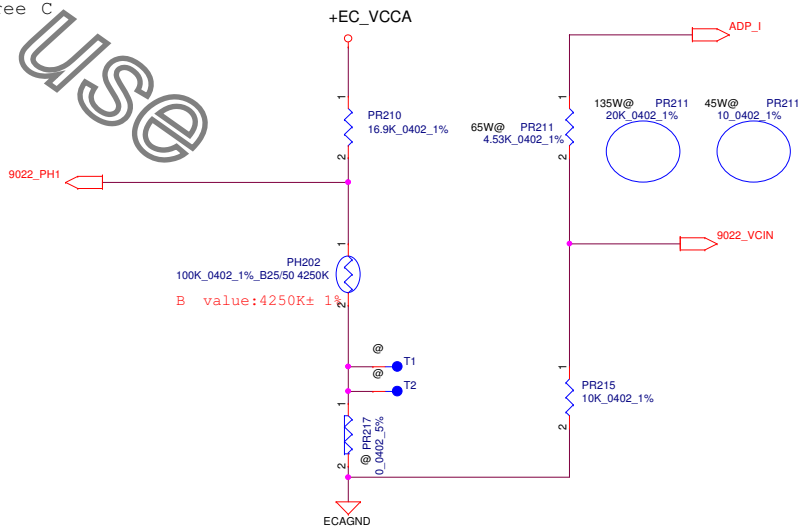
For KB9012 sense 20mΩ	Active	Recovery
SR 45W	58.5W, 0.61V	58.5W, 0.61V
BR 65W	84.5W, 0.61V	84.5W, 0.61V

PH202 under CPU bottom side :
CPU thermal protection at 96 degree C (shutdown)
Recovery at 56 degree C

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design





Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

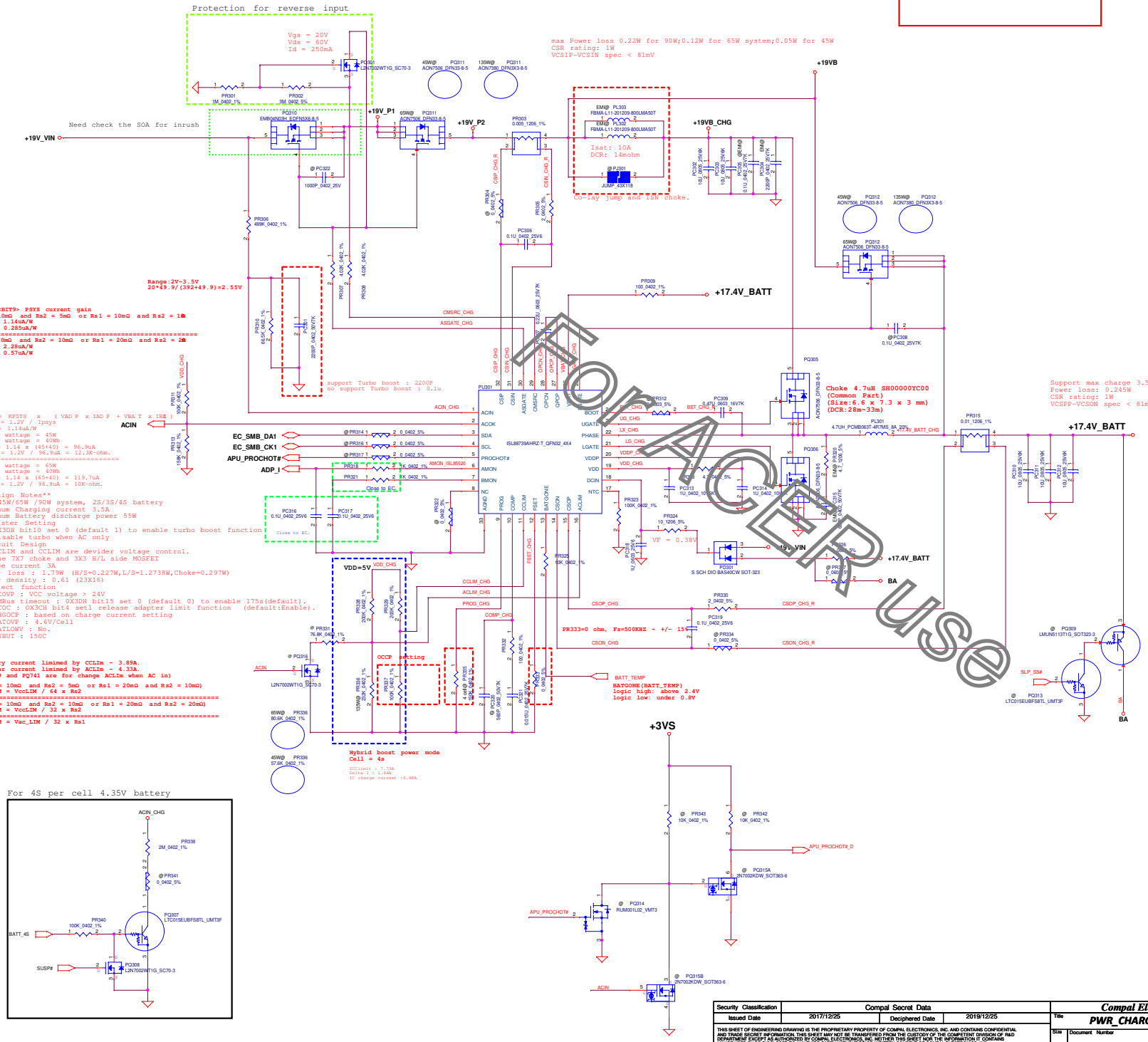
Title: BATTERY CONN / OTP

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

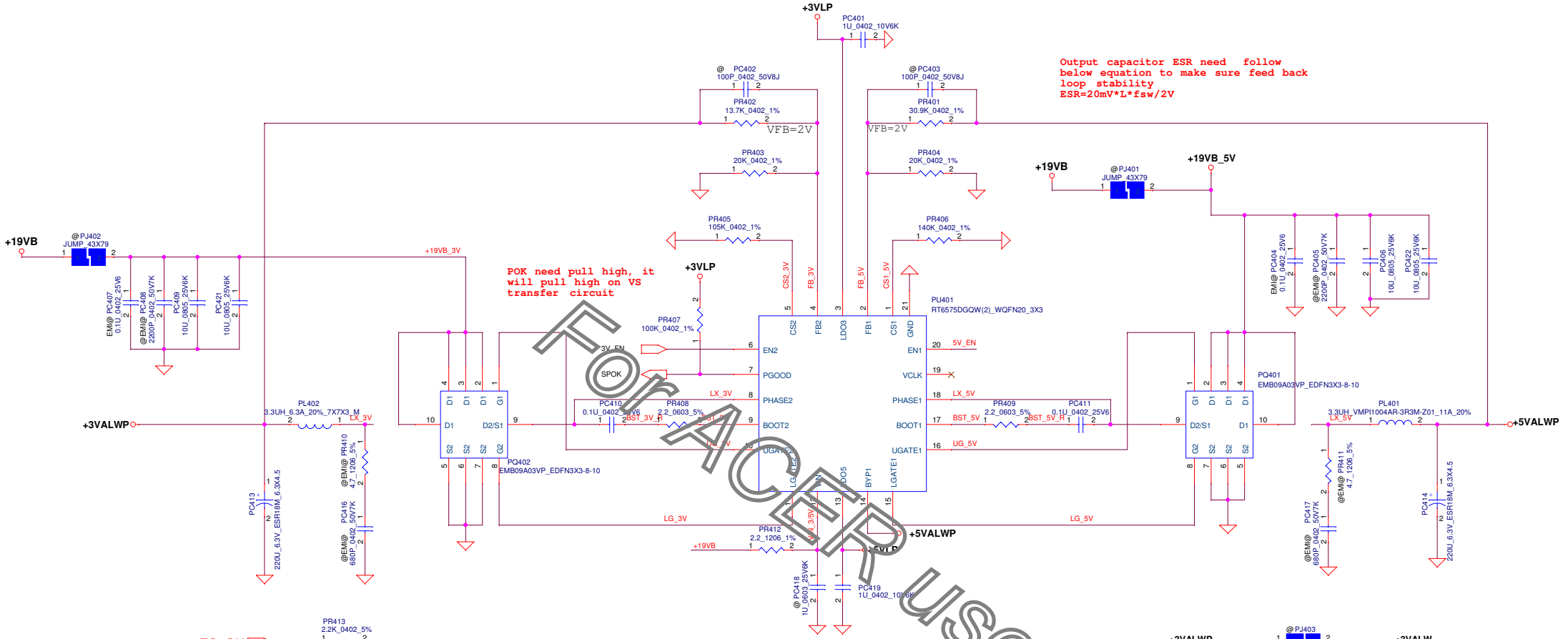
Date: Monday, December 25, 2017 | Sheet 37 of 48

Module model information

ISL95520_Hybrid_Boost_V2.mdd



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/12/25	Deciphered Date	2019/12/25
Title	PWR_CHARGER		
Size	Document Number		Rev 1.B
Date: Monday, December 25, 2017	Sheet 38 of 48		



3V Dual Mos AON7934
H/S (Q1) Rds(on) :typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A

L/S (Q2) Rds(on) :typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A(Typ), Idsm(TA=70)=9A(Typ)

Choke: 7x7x3
Rdc= 18mohm(Typ), 22mohm(Max)

Switching Frequency: 355kHz
Ipeak=9.4A
Iocp~11.3A
OVP: 113%

5V Dual Mos AON7934
H/S (Q1) Rds(on) :typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A

L/S (Q2) Rds(on) :typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A(Typ), Idsm(TA=70)=9A(Typ)

Choke: 10x10x3
Rdc= 14.5mohm(Typ), 16mohm(Max)

Switching Frequency: 300kHz
Ipeak=12A
Iocp~15A
OVP: 113%

1. Vout1=2V*(1+30.9k/20k)=5.09V; Vout2=2V*(1+13.7k/20k)= 3.37V
2. 5V current limit = (140K*10uA/8/11.6mohm)= 15A
3. 3.3V current limit = (105K*10uA/8/11.6mohm) =11.3A

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

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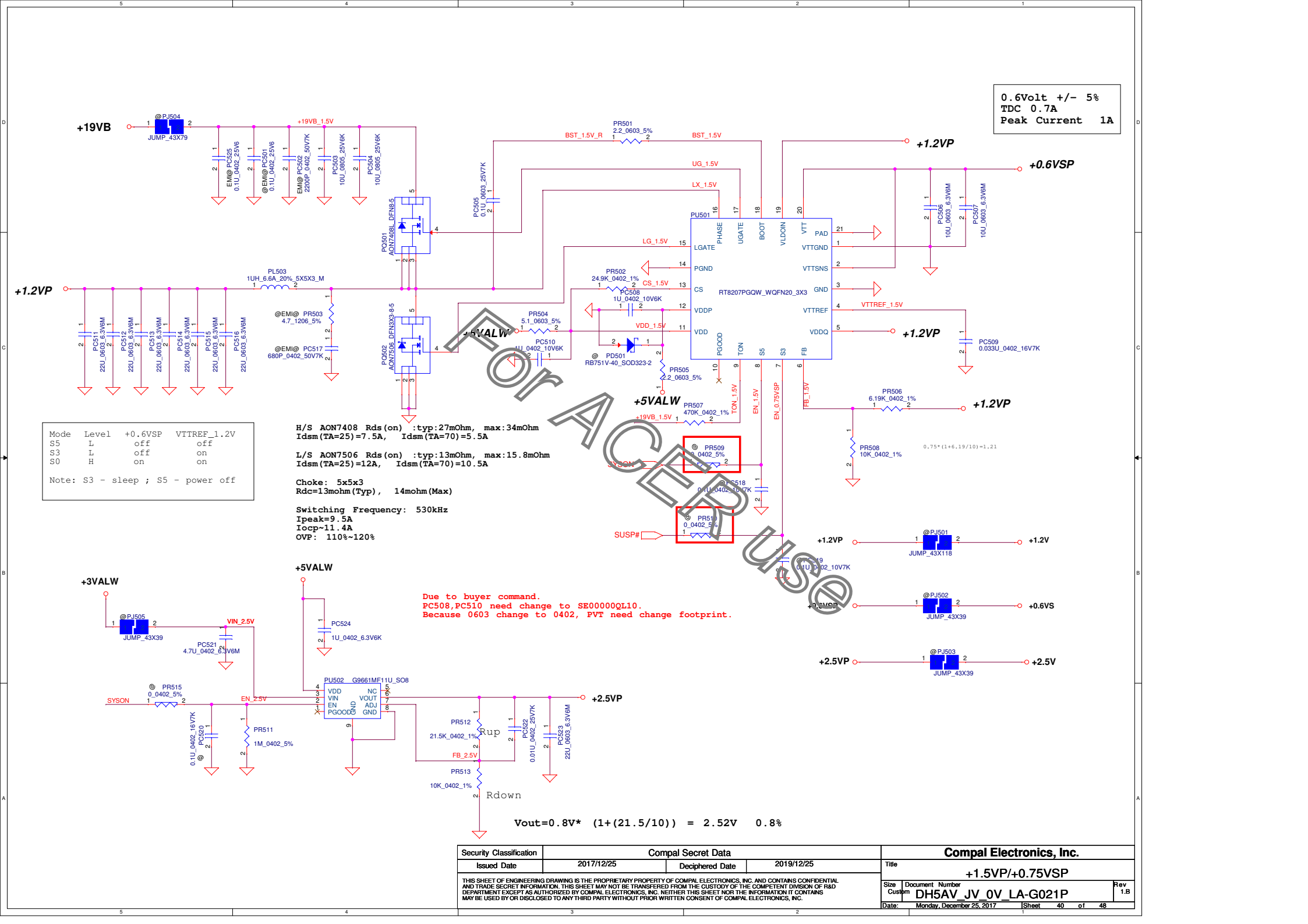

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

H/S AON7408 Rds(on) :typ:27mOhm, max:34mOhm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13mOhm, max:15.8mOhm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

Choke: 5x5x3
Rdc=13mohm(Typ), 14mohm(Max)

Switching Frequency: 530kHz
Ipeak=9.5A
Iocp~11.4A
OVP: 110%~120%

Due to buyer command.
PC508,PC510 need change to SE00000QL10.
Because 0603 change to 0402, PVT need change footprint.

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: +1.5VP/+0.75VSP

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

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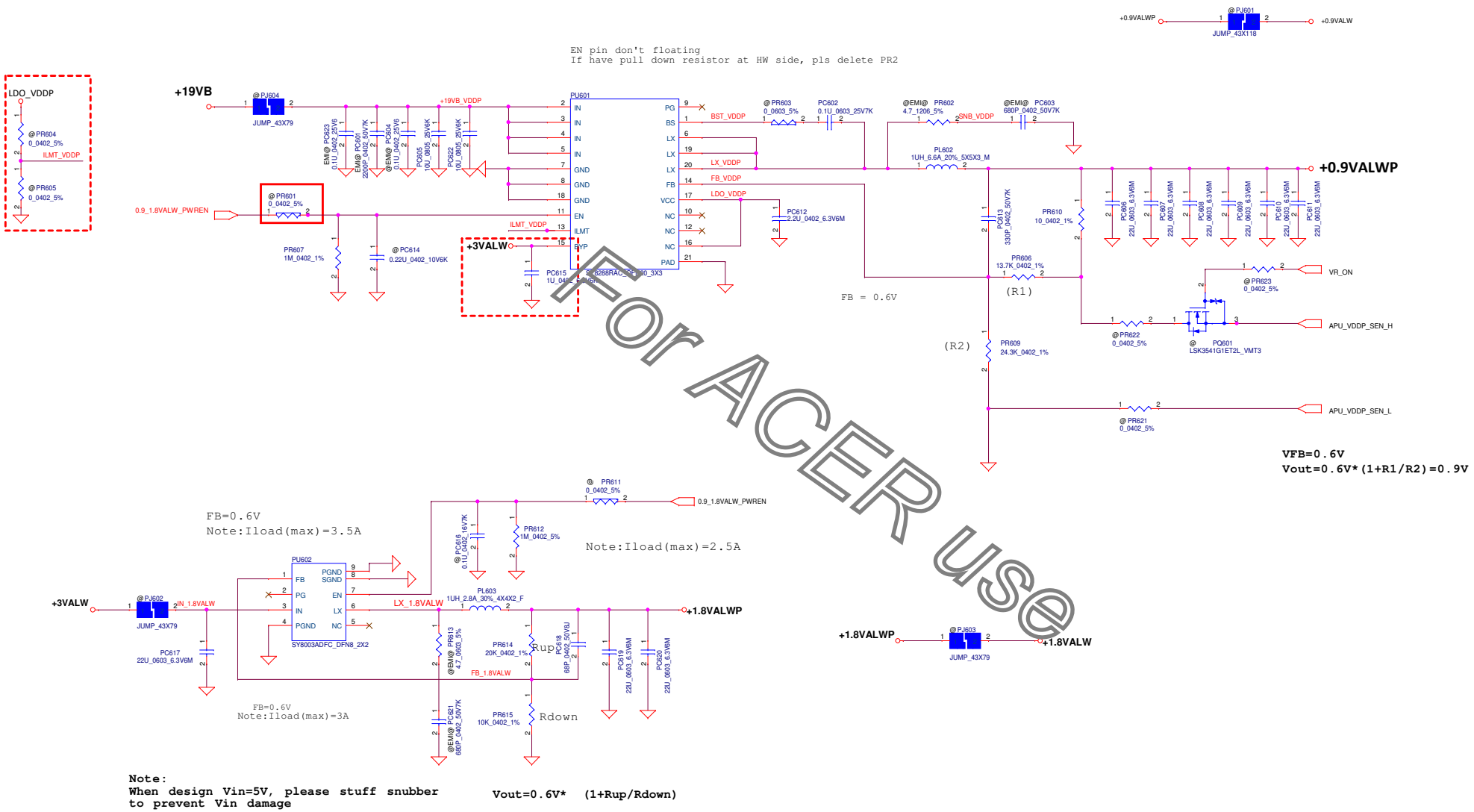

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: +0.95VALW/+1.8VALW

Size	Document Number	Rev
C	DH5AV_JV_0V_LA-G021P	1.B

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Module model information

RT8880C_CZ35W_V2A.mdd for IC portion

RT8880C_CZ35W_V2B.mdd for SW portion

CORE SW= 430KHz

LL CORE(Rdroop)=2.079m

Iocp_spikea = (3.19375 - 0.64)* PR755/ (2*DCR*Rimona)

Iocp_TDCA has relation between ocp_spikea and Δ VSET1

Δ VSET1 = +5VS*(PR788//PR784)

SVD_CPU and SVC_CPURC filter put CPU side.
SVT_CPU RC filter put controller side.

APU_PROCHOT#

Pull high at HW side

confirm HW side pull high resistor

EN: high > 2V, low < 0.8V
Can't be floating.

Iocp_spike = (3.19375 - 0.64)* PR709/ (DCR*Rimon)

Iocp_TDC has relation between ocp_spike and Δ VSET1

Δ VSET1 = +5VS*(PR788//PR784)

LL_SOC(Rdroop)=3.992m

APU_core
TDC 35A (15W & 25W), 53A (35W)
EDC 45A (15W & 25W), 70A (35W)
OCP current 63A (15W & 25W), 98A (35W)
Load line -2.1mV/A
FSW=430kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

+APU_CORE_SOC
TDC 10A (15W & 25W &35W)
EDC 13A (15W & 25W &35W)
OCP current 18.2A (15W & 25W &35W)
Load line -4mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/12/25	Deciphered Date	2019/12/25
Title	RT8880CGOW		
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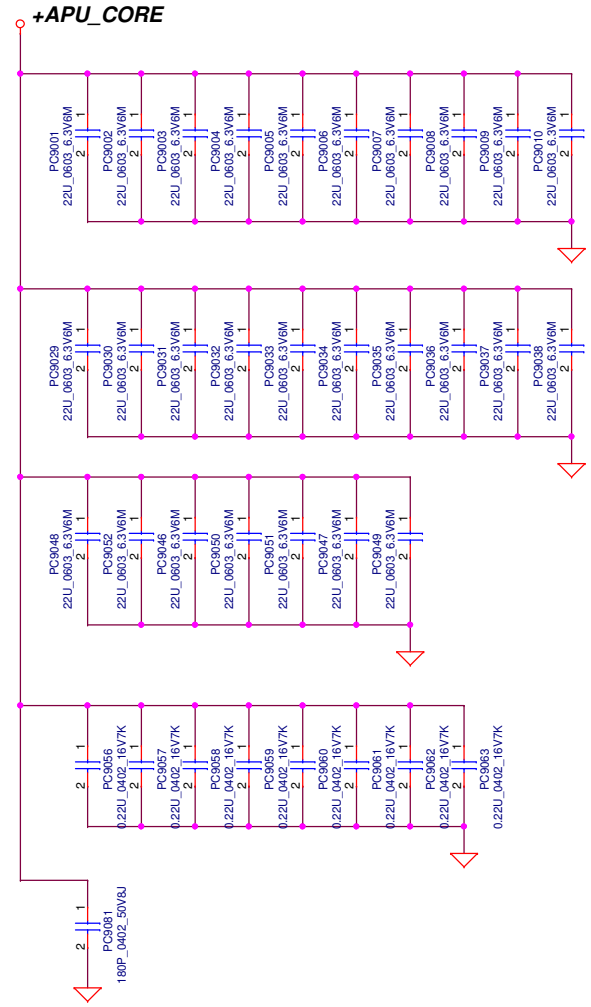
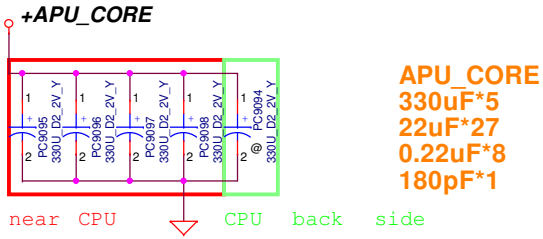
+APU_CORE

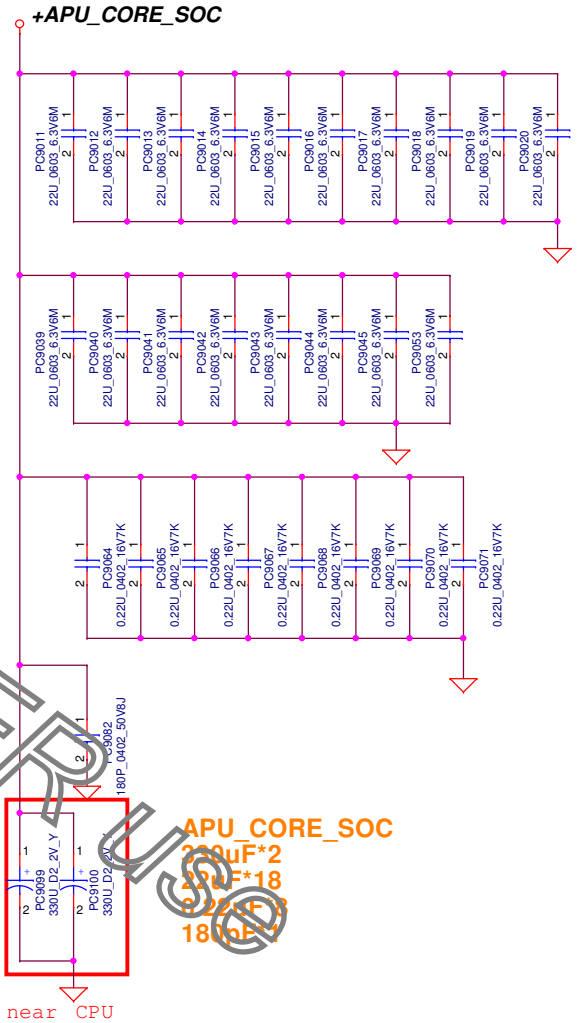




APU_CORE
330uF*5
22uF*27
0.22uF*8
180pF*1

330u is common part SGA00009S00

+APU_CORE_SOC



APU_CORE_SOC
330uF*2
22uF*18
0.22uF*13
180pF*1

330u is common part SGA00009S00

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: +APU_CORE Cap

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

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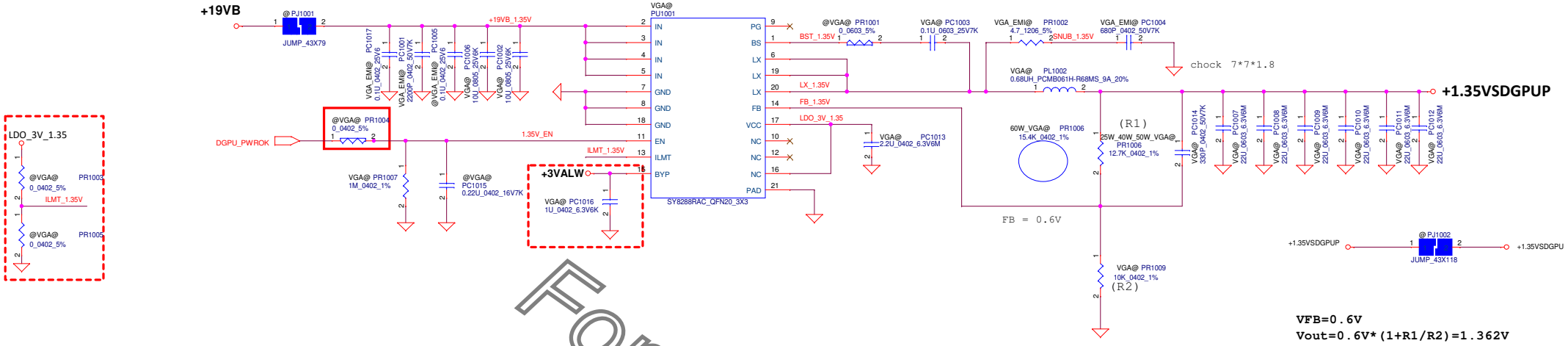
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

Module model information

SY8208D_V1.mdd



VFB=0.6V
Vout=0.6V*(1+R1/R2)=1.362V

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: +GFX_CORE

Size	Document Number	Rev
Custom	DH5AV_JV_0V_LA-G021P	1.B

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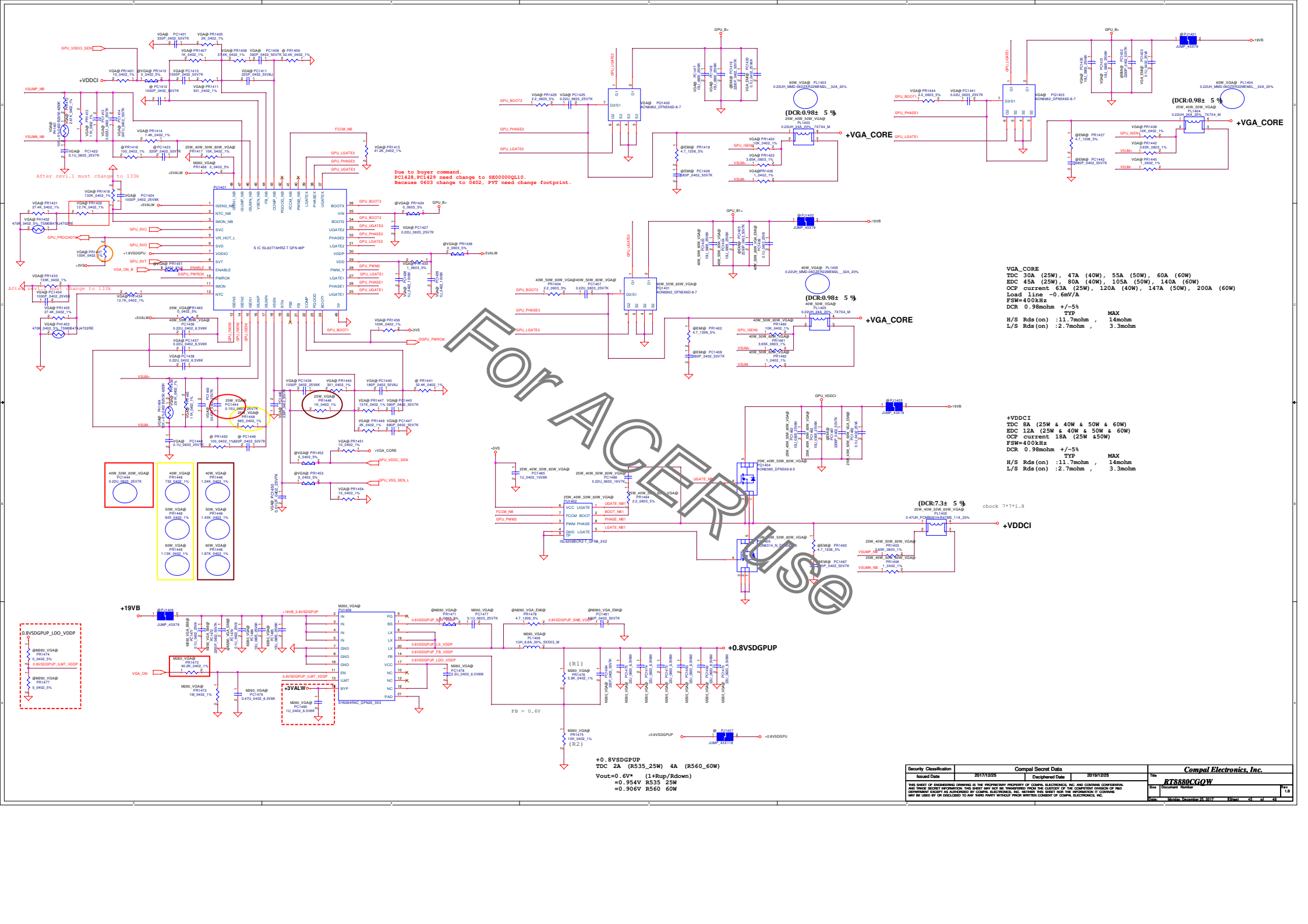

VGA_CORE
TDC 30A (25W), 47A (40W), 55A (50W), 60A (60W)
EDC 45A (25W), 80A (40W), 105A (50W), 140A (60W)
OCP current 63A (25W), 120A (40W), 147A (50W), 200A (60W)
Load line -0.6mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

+VDDCI
TDC 8A (25W & 40W & 50W & 60W)
EDC 12A (25W & 40W & 50W & 60W)
OCP current 18A (25W &50W)
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

+0.8VSDGPUP
TDC 2A (R535_25W) 4A (R560_60W)
Vout=0.6V* (1+Rup/Rdown)
=0.954V R535 25W
=0.906V R560 60W

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/12/25	Deciphered Date	2019/12/25
Title	RT8880CGQW		
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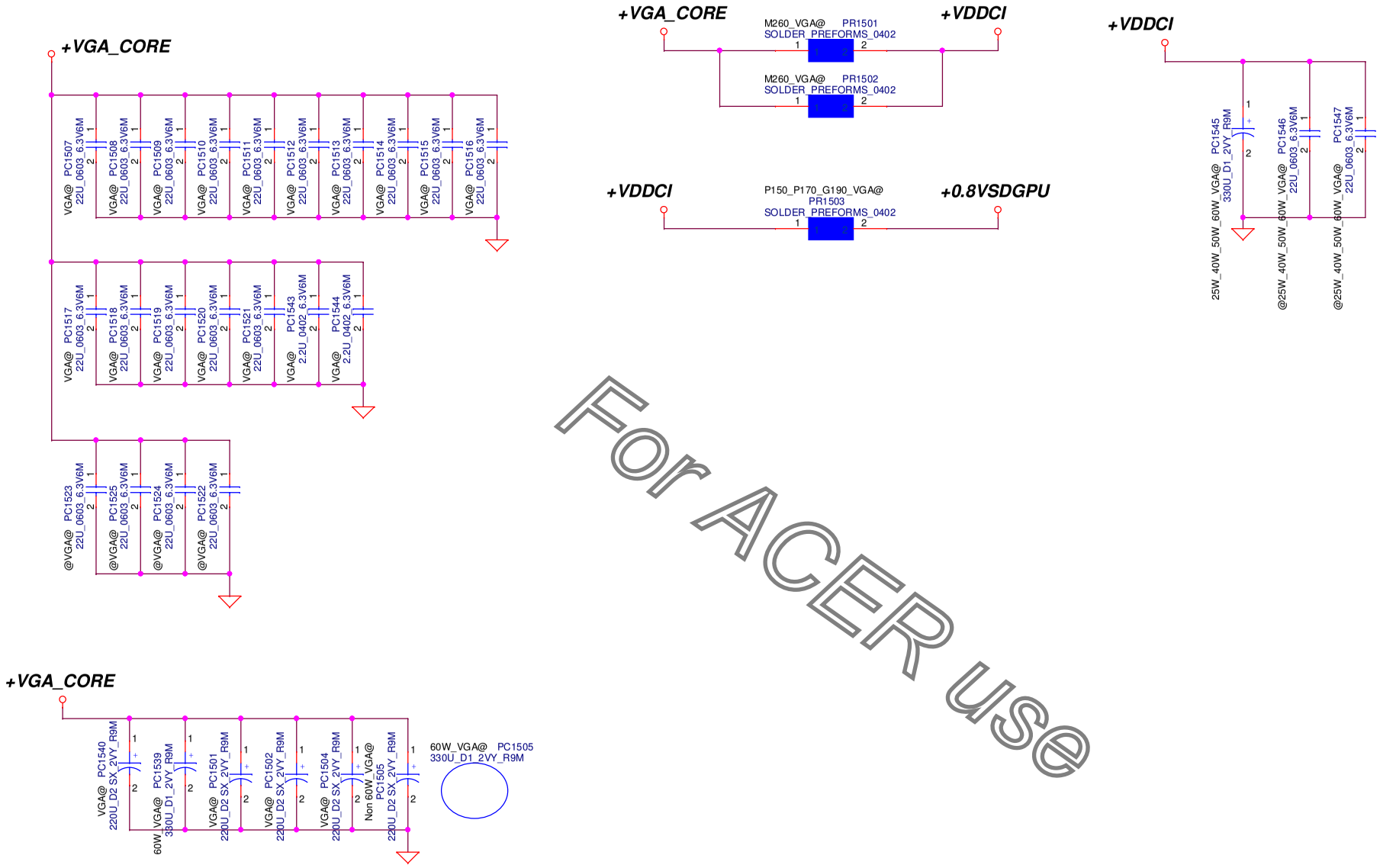

Title	<Title>	
Size B	Document Number DH5AV_JV_0V_LA-G021P	Rev 1.B
Date: Monday, December 25, 2017	Sheet 46 of 48	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Down Size for EMI Cap	1.0	39, 41, 42, 44, 45	Change PC315, PC603, PC811, PC826, PC843, PC849, PC1408, PC1426, PC1467, PC1004, PC1442, PC1481 from 680P_50V_K_X7R_0603 (SE025681K80) to 680P_50V_K_X7R_0402 (SE074681K80).	2017/10/20	B
02	Design Update	Down Size for VGA Cap	1.0	45	Change PC1443 from 0.047U_0603_25V7M (SE042473M80) to 0.047U_0402_25V7K (SE00000MJ00)	2017/10/20	B
03	Design Update	Solution Change	1.0	38	Change PQ310 from AON6366E (SB00001D800) to EMB04N03H (SB00001C500) Change 135W Adapter PQ311, PQ312 from AON7506 (SB000010A00) to AON7380 SB00001GM00) Delete the PC323 10U_0805_25V (SE00000QK00)	2017/10/20	B
04	Design Update	Down Size for EMI Cap	1.0	36	Change PC101 from 100P_50V_J_NPO_0603 (SE024101J80) to 100P_50V_J_NPO_0402 (SE071101J80). Change PC102 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80).	2017/10/20	B
05	Design Update	change to r-short	1.0	38, 39, 40, 41, 42	Change PR304, PR314, PR316, PR317, PR322, PR334, PR509, PR510, PR515, PR414, PR611, PR815 (0402) AND PR327, PR312 (0603) 0ohm to r-short	2017/11/1	B
06	Design Update	change HW sequence disable VDDCI	1.0	45	Change PC1476 from 0.22U_0402_10V6K (SE095224K00) to 0.47U_0402_6.3V6K (SE124474K80) Add PR1466 for disable VDDCI when ues R535 GPU	2017/11/1	B
07	Design Update	tune CPU transient and load line	1.0	42	Change PR809 from 2.49K_0402_1% (SD034249180) to 2.7K_0402_1% (SD034270180) Change PR826, PR841, PR856 from 2.26K_0603_1% (SD014226180) to 2.7K_0402_1% (SD034270180) Change PR806 from 53.6K_0402_1% (SD034536280) to 80.6K_0402_1% (SD034806280) 15W CPU Change PC807, PC830 from 330P_0402_50V8J (SE000006I80) to 270P_0402_50V7K (SE074271K80) Change PR859 from 18.2K_0402_1%(SD034182280) to 43K_0402_1% (SD034430280) Change PR858 from 30.9K_0402_1% (SD034309280) to 48.7K_0402_1% (SD034487280) Change PC828 to un pop	2017/11/6	B
08	Design Update	Down Size for EMI Cap	1.0	37	Change PC201, PC203 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80)	2017/11/14	B
09	Design Update	Down Size for Cap	1.0	40, 39	Change PC507, PC506 from 10U_0805_6.3V6K (SE093106K80) to 10U_0603_6.3V6M (SE000005T80) Change PC416, PC417 from 680P_0603_50V8J (SE074681K80) to 680P_0402_50V7K (SE074681K80)	2017/11/14	B
10	Design Update	Cap shortage	1.0	38, 45	Change PC313, PC314, PC1428, PC1429 from 1U_0402_16V6K (SE000006J00) to 1U_0402_10V6K (SE00000QL10)	2017/11/14	B
11	Design Update	Cap shortage	1.0	44, 46	Change PC1015, PC1476, PC9056, PC9057, PC9058, PC9059, PC9060, PC9061, PC9062, PC9063, PC9064, PC9065, PC9066, PC9067, PC9068, PC9069, PC9070, PC9071 from 0.22U_0402_10V6K (SE095224K00) to 0.22U_0402_16V7K (SE00000R700)	2017/11/14	B
12	Design Update	紅丹測試	1.0	46	Delete PC1538 330U_D1_2VY_R9M (SGA00009S00) Reserved 22U_0603_6.3V6M*4 (SE00000M000) Change PC1505 from 220U_D2 SX_2VY_R9M (SGA20221D40) to 330U_D1_2VY_R9M (SGA00009S00) for POW VGA	2017/11/14	B
13	Design Update	change to common part	1.0	42	Change PC820, PC834 from 33U_25V_NC_6.3X4.5 (SF000007700) to 33U_25V_NC_6.3X4.5 (SF000007200)	2017/11/14	B
14	Design Update	For sourcer request	1.0	42	Change PC820, PC834 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_NC_6.3X4.5 (SF000007700)	2017/11/23	B
15	Design Update	tune VDDP in AMD spec	1.0	41	Change PR609 from 26.7K_0402_1% (SD034267280) to 24.3K_0402_1% (SD00000AT80) PQ601 unpop	2017/11/23	B
16	Design Update	use SW solution in standby mode	1.0	38, 43	PR326 0_0603_5% pop PQ309 LMUN5113T1G_SOT323-3 un pop PQ313 LTC015EUBFS8TL_UMT3F un pop PC9094 330U_D2_2V_Y un pop	2017/11/23	B
17	Design Update	斷switch design reserve two cell low batt protect	1.0	37	pop PR212 0_0402_5% (SD028000080) pop PC204 0.1U 25V K X5R (SE00000G880) pop PR213 750K +-1% 0402 (SD00000AL80) pop PR214 0 +-5% 0402 (SD028000080) pop PR216 150K +-1% 0402 (SD034150380) pop PR212 0 +-5% 0402 (SD028000080)	2017/11/23	B
18	Design Update	change PQ307 and PQ313 source for source request	1.0	38	change PQ307 & PQ313 form LTC015EUBFS8TL (SB00000RM00) to LMUN5236T1G (SB000011K00)	2017/11/23	B
19	Design Update	adaject BATGONE Threshold	1.0	37	change PR203 from 6.49K_0402_1% (SD034649180) to 200K_0402_1% (SD034200380)	2017/11/23	B
20	Design Update	adaject bootst ability	1.0	38	change PC309 from 0.22U_0603_25V7K (SE000005Z80)to 0.47U_0603_16V7K (SE026474K80)	2017/11/23	B
21	Design Update	for EMI request	1.0	38	add PL302/PL303 FBMA-L11-201209-800LMA50T (SM01000U600)	2017/12/22	B
22	Design Update	for ACIN point	1.0	38	change PR306 392K_0402_1% (SD034392380) to 499K_0402_1% (SD034499380) change PR310 49.9K_0402_1% (SD034499280) to 66.5K_0402_1% (SD034665280)	2017/12/22	B

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: PWR_PIR1

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

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Version Change List (P. I. R. List)

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
1		07/31		1. Initial		0.1
2		09/30		EVT Final		0.1
3		11/02		1. UW1 change PN(SA00008ELE0) 2. US11,U74 change PN(SA00004ZA00) 3. L43,L44 change PN(SM01000K500) 4. US10 Pin2,3 swap Pin 10,11 (USB Charger modify) 5. RC6155 change location to CLRP1 6. RM23,RM24,RM25,RM26 add 0-ohm with T1PCIE@ 7. All 1uF_0402 capacitor change to 1uF_0201 (SE00000UC00) 8. CS123 change PN(SE00000X200) 9. CC16 change to 1uF (SE00000UC00) 10.RO18 change to pop with PAR@ 11.JDMIC1 change to 4pin connector (SP02000TI00) 12.R1562 pop, R1564 change to 20k (SD034200280) 13.R3_APU change PN(SA0000BBJ20) 14.US12 update value and part description 15.Q101,R101,R102,R103,R104 add with @ for UART0 debug 16.L2508,L2511,LS7 change to small size (SM070005U00) 17.PCB change PN(DAZ28Z00100) 18.SKU_ID change to AGPIO23, AGPIO40 will left N.C. 19.RC30,RC700,RC690,RC1676,RC1677,RC1672,RL1,RL13,RM20,RS10,RS127, RS147,RV807,RV1643,RV1632,R110,R4018 change to R-short 20.UV4 change PN(SA0000A4K00)	1.0
4		11/07		1. CV450,CV451 change to 10pF 2. C796,C797 change to 3.9pF 3. Combine power 11/06 4. R756,R765,R769,R779,R781,R782,R793,R794 change to R-short 5. L2516,L2517 add with EMC@ R4031,R4032 remove 6. RS150,RS151 add with @ for debug		1.0
5		11/15		1. CC120 change to 0402_50V7K (SE07461K80) 2. Combine power		1.0
6		11/20		1. Board ID set by project 2. VRAM table add MICRON VRAM 3. Memory strap pin add MICRON config PV4G_M@ 4. EVT@ change to @ 5. R3APU@ seperate to R3APUDC@ and R3APUQC@ 6. CS11,CS12,CS14,CS15 change to 0.1uF_0402_25V (SE00000G380) 7. TPM@,FP@,GS@,HDT@ remove from BOM PVT Final		1.0
7		12/18		1. C796,C797 change PN to SE07139AC80 (S CER CAP 3.9P 50V C NPO 0402) 2. RW5,RW6,RW7,RW8 change to pop 3. RC6175,RC6174 change to @, RC693 change to DIS@, RC692 change to UMA@ 4. VRAM config V4G_S7G@,V4G_H7G@,V4G_M7G@ add into table and strap-pin 5. RC6175 change to @, RC6174 change to @ 6. US11 change to Power Switch (SA00006Y700, S IC G527ATP1U TSOT-23 6P PW SW) 7. RS154,RS155,RS156 add with TYPEC@; CS124 add with @ 8. SWG1 change to @ 9. QS4 change to @; RS148,RS149 change to TYPEC@ 10.QC1 change to TYPEC@; RC616,RC617 change to NTYPEC@ 11.RS112,QS6 change to @ 12.Q2509,RC6158,RC6159 change to pop; R2622,R2623 change to @		1.B
8		12/22		1. RO19 remove from BOM. 2. DAZ28Z00102 add into NOTE LIST		1.B
9		12/22		1. PCB Location change to ZZZ1/ZZZ2/ZZZ3 2. D2016,D2017,D2018 change to EMC@		1.B

Compal Electronics, Inc.
Title: HW PIR
Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B
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Version Change List (P. I. R. List)

Item	Page#	Date	Request Owner	Issue Description	Solution Description	Rev.
10		12/25		1. PCB change location to ZZZ, and config to PCB1A@,PCB1B@ 2. BOM Loader without HUB@ 3. APU PN update to R3 PN 4. Update Schematic to 1B		1.B

Security Classification	Compal Secret Data		
Issued Date	2017/12/25	Deciphered Date	2019/12/25

Compal Electronics, Inc.

Title: HW PIR

Size: Custom | Document Number: DH5AV_JV_0V_LA-G021P | Rev: 1.B

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