3U cPCI
FOUR CHANNEL
DIGITAL to SYNCHRO/RESOLVER
OR
DIGITAL to LVDT/RVDT CONVERTER

Convection Cooled

FEATURES

- 1, 2, 3, or 4 D/S(R) or LVDT/RVDT Simulation (DLV) Channels
- 1 arc-minute (0.0167°) accuracy
- 16 bit resolution
- 1.5, 2.2 or 3 VA drive capability per Synchro channel.
- Automatic background BIT testing continually checks and reports the health of each channel.
- Optional on board 3 VA programmable reference supply.
- Connections via front panel, rear connector or both.
- Convection and Conduction cooled (Wedge Lock) models
- Wrap-around converters for reading actual commanded outputs.
- No adjustments or trimming required.
- Wide Operating Temperature Range.
- Software Support Kit and Drivers are available.

Conduction Cooled

DESCRIPTION

The 75DS2 is a 3U cPCI board which incorporates up to four Digital-to-Synchro/Resolver converters with 1.5, 2.2 or 3 VA drive capability, or either 2 or 4 isolated DLV converters. The board features continuous background BIT testing, reference and Signal loss detection. Each channel is independent, isolated and enables the user to ground one of the outputs without affecting performance. This model drives passive or active loads. In addition, the card provides for an optional on-board reference supply.

Automatic background BIT testing, an important feature, is always enabled and continually checks the health of each channel. There is no need to guess or make assumptions about system performance. A fault is immediately reported and the specific channel is identified. This diagnostic capability is of tremendous benefit because it immediately identifies and reports a failure, without the need to shut down the equipment for troubleshooting. Testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of the card. (See Operations Manual for more details).

SPECIFICATIONS

General

Signal Logic Level:	Automatically supports either 5V or 3.3V CPCI bus.
Power (Mother board):	+5 VDC @ 750mA and ±12V @ 15mA, then add power for each individual module.
Temperature, operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (see part number)
Storage temperature:	-55°C to +105°C
Temperature cycling:	Each board is cycled from -40°C to +85°C for 24 hrs for options “E” or “H” (See part number)
Size:	Height - 3.94" / 100 mm (3U) Width - 0.8" / 20.3 mm (4HP) Depth - 6.3 “/ 160 mm deep
Weight:	4 oz. (115g) unpopulated. add weight for each module (typically 1 oz. each) add 2 oz. (57g) for reference supply add 2 oz. (57g) for wedgelocks

For the Mother Board

D/S (Module D/S*)

Single channel, 3.0 VA output

***See P/N**

(Will drive torque receivers. Applies to each channel unless noted otherwise)

Resolution:	16 bits (.0055°)
Accuracy:	0.067º (4 arc minutes) for passive loads; 30 arc minutes for TR’s
Output format:	Synchro or Resolver, (see part number), galvanic isolation
Output voltage:	(See code table and part number).
Output load:	3.0 VA max./Channel. Short circuit protected.
Output control:	Channel output can be turned ON/OFF
Regulation (VL-L):	5% max. No load to Full load
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.15°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference input voltage:	(See part number), Galvanic isolated. Uses 1 ma max/Channel
Reference frequency:	47 Hz to 10 kHz (See part number)
Phase shift:	0.5° max. (Between output and reference) (Programmable phase shift)
Settling time:	Less than 100 microseconds
Module Power:	+5VDC @ 50 mA ±12VDC @ 115 mA (no-load); (Add 1.1 watts of ±12V for every VA of output). Therefore, a 3.0 VA Load adds to ±12VDC 138 mA average, or 157 mA peak). External ±12VDC input power can be utilized.

D/S (Module D/S*) — Two channel, 1.5/2.2 VA outputs

***See P/N**

(Applies to each channel unless noted otherwise)

Resolution:	16 bits (.0055°)
Accuracy:	±1 arc-minute (.017°) from No Load to Full Load
Output format:	Synchro or Resolver (see part number), galvanic isolation
Output voltage:	(See code table and part number).
Output load:	1.5 VA @ 11.8 VLL or 28 VLL, and 2.2 VA @ 90 VLL max. per Channel. Short circuit protected.
Output control:	Module outputs can be turned ON/OFF
Regulation (VL-L):	5% max. No load to Full load
Ratio:	Dual speed, Programmable, Set any ratio between 2 and 255
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.015°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference input voltage:	(See part number), Galvanic isolated. Uses 1 ma max/Channel
Reference frequency:	47 Hz to 10 kHz (See part number)
Phase shift:	0.5° max. (Between output and reference) (Programmable phase shift)
Settling time:	Less than 100 microseconds
Module Power:	+5VDC @ 500 mA ±12VDC @ 125 mA (no-load) per channel. (Add 2.6 watts of ±12VDC for every VA of output per channel). Therefore, a 1.5 VA Load adds to ±12V 160 mA average, or 226 mA peak per channel. External ±12V input power can be utilized.

DLV Stimulus (Module*) — LVDT or RVDT Position, Programmable 3/4 or 2-Wire

***See P/N**

(Applies to each channel unless noted otherwise)
LVDT or RVDT outputs, programmable 3/4 or 2-Wire

Resolution:	16 bits (.001526% FS)
Linearity:	0.1% FS for .2 <= TR <= 2.0
Output format:	Configurable for either 3/4-wire or 2-wire.Galvanically isolated. Output voltage is programmable fixed or ratio-metric.
Output voltage:	Programmable (See code table and part number).
Output load:	10 Kohm minimum. Short circuit protected.
Regulation (VL-L):	5% max. No load to Full load
Excitation input voltage:	(See part number), Galvanic isolated. Uses 1 ma max/Channel
Excitation frequency:	47 Hz to 10 kHz (See part number)
Phase shift (A/B):	0.5° max. (Between output and reference) (Programmable phase shift)
Settling time:	Less than 100 microseconds
Module Power:	+5V @ 500 mA (quiescent, no-load) ±12V @ 125 mA (quiescent, no-load) 1.5 VA Full Load (adds ±12V @ 160 mA avg./ ±12V @ 226 mA peak per channel)

Module M7 — Optional On-Board Reference Supply

Voltage:	2.0-28 Vrms programmable, resolution 0.1Vrms, or 115Vrms fixed.
Frequency:	360Hz to 10 KHz ±1% with 1 Hz resolution.
Accuracy:	±2%
Regulation:	10% max. No load to full load.
Output power:	3 VA max. @ 40° min. inductive; 115 mA RMS @ 2-26 VAC or 45 mA RMS @ 115 VAC Note: Power is reduced linearly as the Output Voltage decreases.
Power:	±12 VDC @ 500 mA
Ground:	Isolated from system ground.
Weight:	1 oz. (28g)

PRODUCT CONFIGURATION AND MEMORY MAP

This design provides multiple functions on a single cPCI (3U) card. When ordering, the customer selects an assortment of up to 2 modules to populate this 2-slot "mother board." The memory map follows the order of modules specified in the part number.

To address the register of any module, use the *Base* address to the entire card, add the *Module Offset* depending upon its slot (000 or 800), and then add the *Register Offset* of interest (see module memory map.) The memory map of each selected module counts from, or is superimposed over its respective module offset. Thus, **Address = Base + Module Offset + Register Offset**.

For example, if a Digital I/O module were selected to populate module 1 and a Discrete I/O module were selected to populate module 2:

Address = Base + Module 1 Offset 000 + Digital I/O register 010 = Base + 010 hex
Address = Base + Module 2 Offset 800 + Discrete I/O register 024 = Base + 824 hex.

MEMORY MAP

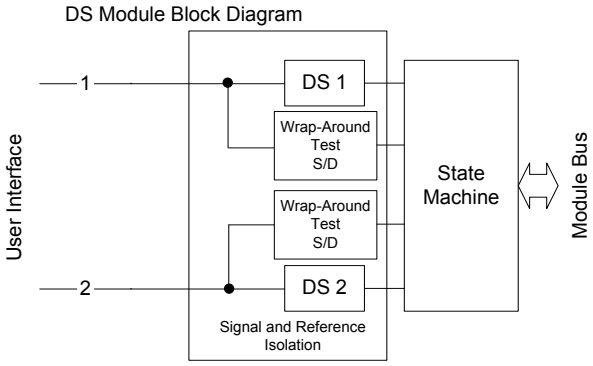
000	Module 1 Register…	800	Module 2 Register…	3000	Unit Level General Register…
004		804		3004	
008		808		3008	
00C		80C		300C	
010	Slot 1	810	Slot 2	3010	General
.	Offset 000	.	Offset 800	.	Offset 3000
.		.		.	
.		.		.	
7FE		FFE		37FE	
7FF		FFF		37FF	

Any address NOT SPECIFIED within 4096 byte block (up to 3FFFh) is reserved.
The memory map of each module type is described hereafter:

D/S (MODULE ##*)

***See P/N**

Principle of Operation



These new D/S modules are solid state designs that eliminate the need for external transformers. Since these modules operate down to 50 Hz, deleting the previously large external transformers offers huge space savings. The reduced size and lower power consumption of these modules now makes it possible to supply 10 channels on a 6U card.

Two different modules are available within the same package size: The first is a two-channel 1.5VA/2.2VA design that contains two separate channels within one enclosure. The other is a single channel 3.0VA design that will also drive Torque Receivers. All outputs are short circuit protected and the S2 (Z) leg can be grounded without effecting performance. Any channel can be programmed for rotation (either continuous or with start/stop angles). External amplifiers can be added to drive up to 30 VA with a frequency range of 50 to 400 Hz. Two-speed (up to 1:255 ratio) outputs can be programmed (dual channel module).

New features in these modules now include a wrap capability for measuring each channel's commanded output angle, velocity and carrier frequency. The module's extensive programmability now includes format selection (synchro or resolver). A background calibration feature (pending), that is totally transparent to the operation of the channels, constantly adjusts outputs for all load and environmental conditions. Each channel can be programmed for a different output voltage, which can be programmed for either ratio-metric or absolute (fixed) output. Module power ON/OFF capability provided for shutting down inactive channels.

Built-In Test (BIT) / Diagnostic Capability

Two different tests (one on-line and one off-line) can be selected:

The on-line (D2) Test initiates automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output angle to the commanded angle. Each channel is individually checked to an accuracy of 0.2° and each D/S Signal output and Reference input is continually monitored. User can periodically clear to 00h and then read Test (D2) verification register again, after 0.1 seconds, to verify that background bit testing is activated. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled.

The off-line (D3) Test initiates a BIT test that generates and tests 24 different angles to a test accuracy of 0.2°. Results can be read from registers. External reference is required and outputs must be on. Any failure triggers an Interrupt (if enabled). Testing requires no external programming, and can be initiated or stopped at any time.

CAUTION: Outputs must be ON and Reference supplied during this test and therefore active. Check connected loads for possible interaction.

D/S Specific Registers

D/S Active Channels

Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel Register for the particular D/S channel. "1" = Active; "0" = not used. Omitting this step will produce false alarms because unused channels will set faults.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Active Channels	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Torque Driver Select (Applies only to the single channel modules)

Normal = "0"; Torque Receiver = "1"

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Torque Receiver Select	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH1

D/S Synchro / Resolver Select

When required, write a "11" or "00" (Synchro = 11; Resolver = 00) to each corresponding channel bit pair, representing a channel commanded output format, of the Synchro/Resolver Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	CH2		CH1	
D/S Synchro / Resolver Select	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	D1	D0

D/S Set Reference Voltage

Set required input reference voltage "VREF" to a corresponding register. The input voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. For example, if channel 1 expected input REF voltage is 26.0 Vrms, the set word to the corresponding register would be 2600.

D/S Set Signal Voltage

Set required output signal voltage "VL-L" to a corresponding register. The output voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. For example, if channel 1 Signal (VL-L) voltage is to be 11.8 Vrms, the set word to the corresponding register would be 1180.

D/S Write Angle – Single Speed

For single-speed applications (Ratio=1), write an "up to" 24-bit integer (24-bit 2's compliment integer) to the corresponding channel D/S Data Register. (ex. 330° (in 16bit resolution) = EAABh written to Data Hi register only); 330° (in 24bit resolution) = EAAAAB – note that "EAAA" is written to Data Hi register and "AB00" is written to Data Lo register).

WORD = (Angle ÷ (360/224)).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Write Data (°) Hi	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
D/S Write Data (°) Lo	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X

Note: Writing to an Input Angle Register will stop any rotation initiated on that channel

D/S Write Angle – Two Speed

The dual channel module can automatically simulate two-speed applications (applies only to dual channel modules). Write an "up to" 24-bit integer (24-bit 2's compliment integer) to the corresponding channel D/S Write Angle Register to the coarse (channel 1) channel. By entering a ratio in the D/S Ratio 1/2 register, the fine (channel 2) channel will automatically output a signal proportional to the programmed coarse channel times the ratio programmed.

D/S Ratio 1/2

(Only applies to dual channel module). Set desired ratio between coarse (channel 1) and fine (channel 2) channels. Enter the desired ratio, as an integer number, in the D/S Ratio Register corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = integer 36. (Ratio range from 1 to 255). By entering a ratio in the D/S Ratio 1/2 register, the fine (channel 2) channel will automatically output a signal proportional to the programmed coarse channel times the ratio programmed.

D/S Output Mode

The D/S Output Mode register is utilized for selecting either ratio-metric or absolute (fixed) mode voltages. Ratio-metric Mode, when selected, will cause the output signal voltage of the channel to vary with the input Reference Voltage. Fixed Mode, when selected, will cause the output signal voltage of the channel NOT to vary with the input Reference Voltage. Set corresponding channel bit to “0” for Ratio-metric Mode. Set corresponding channel bit to “1” for Fixed Mode.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	CH2		CH1	
D/S Output Mode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Module Power Enable

The D/S Module Power Enable is utilized for module channel output/power control. Set the bit, corresponding to either channel, to enable the power output stage of the D/S channel(s). “1” = Enable; “0” = Disabled. For dual channel modules, writing a “1” to either or both channel bits will enable and turn the output stage power “on”. To disable, or turn off power to the output stage, all channels (both) bits must be set to “0”. Initialized default is “00”.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Module Power Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Rotation

Each channel may be configured for either start/stop or continuous rotation for applications that require it. In start/stop mode, the user can program a rotational velocity and a stop angle. When triggered, either via a software command or external pulse (selectable trigger mode), the output signal will start at the current position and simulate rotation at the specified rotation rate and stop at the programmed stop angle. Re-initiating the trigger will repeat the rotation. In continuous mode, the user will program a rotation rate and trigger the start of the rotation either via software command or external trigger. Stopping rotation can be accomplished by either issuing a stop rotation command or setting a commanded angle. Clockwise or counter-clockwise rotation is accomplished by setting either a positive or negative 2’s complement word in the velocity register.

D/S Rotation Mode, Continuous or Start/Stop

For continuous rotation, set the corresponding channel bit to "0" in the Rotation Mode Register. For rotation to cease at a designated stop angle, set the bit to "1". For 2-speed applications, only the odd (coarse) channel needs to be programmed (CH1).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Rotation Mode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Rotation Rate

Write to the corresponding Rotation Rate Registers (Hi and Lo) a 2’s complement number representing the desired rotation rate, LSB = 0.015°/sec.

Ex: 12 RPS = (12 x 360°/0.015° = 288000 = 46500h), -12 RPS = (-12 x 360°/0.015° = -288000 = B9B00h)

Step size is 16 bits (0.0055°) for up to 1.5 RPS, and then linearly decreases to 12 bits (0.088°) at 13.6 RPS.

D/S Stop Angle

Write the desired stop angle to appropriate channel Stop Angle Register. Write a 16-bit integer (or 16-bit 2’s compliment integer) to the corresponding channel D/S Data Register. (ex. 330° = EAABh).

WORD = (Angle ÷ (360/216)).

Note: Writing to an Input Angle Register will stop any rotation initiated on that channel

Start Rotation

First set the Rotation Rate and Rotation Mode Registers for each channel that is to rotate. Then, to start rotation for the corresponding channel, write a “1” to the corresponding channel D/S Start Rotation register.

Stop Rotation

To stop rotation for the corresponding channel, write a “1” to the corresponding channel D/S Stop Rotation register. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated. Note: An in-process rotation can also be stopped by commanding a new angle (D/S Write Angle).

D/S Rotation Status

Check the corresponding bit of the D/S Rotation Status Register for status of rotation (Done or Not Done) for each channel. A ”1” means Rotation Done (output is static), “0” means Rotation Not Done (output is rotating) on channel. Rotation monitoring is always enabled.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Rotation	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Trigger Source Select

Internal = “0x29”; External = “0x28”

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Source Select	X	X	X	X	X	X	X	X	X	X	D	X	D	X	X	D

D/S Trigger Slope Select

For positive slope, set the corresponding channel bit to "0" in the Trigger Slope Select Mode Register. For negative slope, set the bit to "1".

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Slope Select	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Wrap (S/D) Registers

Wrap S/D Angle (Read)

Read individual channels 1 or 2.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Wrap S/D Data (°) Hi	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Wrap S/D Data (°) Lo	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X

Wrap S/D Bandwidth Adjust

The wrap S/D type II servo loop read bandwidth response may be adjusted for optimal reading of the D/S output angle. For typical applications, it is recommended that the wrap S/D bandwidth be set to 1/20 of the carrier frequency. Program the desired bandwidth response in the corresponding channel register in integer format with a resolution of 1 Hz. For example, for a 400 Hz carrier (Reference frequency) system, the typical bandwidth should be programmed to 20 (14h). Bandwidth range 10 <= x <= 1200

Input Signal Voltage (V_{L-L}) Measurement

Each individual channel input signal voltage “VL-L” is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180.

Input Reference Voltage Measurement

Each individual channel input signal voltage “VREF” is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input REF voltage is 26.0 Vrms, the output measurement word from the corresponding register would be 2600.

Signal Loss Threshold

Each individual channel input signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The signal loss detection circuitry can be tailored to report a signal loss (at Signal Loss Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. For example, if channel 1 input signal loss voltage threshold is to be 7 Vrms, the programmed word to the corresponding register would be 700 (2BCh).

Reference Loss Threshold

Each individual channel input reference voltage "VREF" is measured and the value reported to a corresponding read register. The reference loss detection circuitry can be tailored to report a reference loss (at Reference Loss Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. For example, if channel 1 input reference loss voltage threshold is to be 20 Vrms, the programmed word to the corresponding register would be 2000 (7D0h).

Status, Signal Loss

Type: binary word

Range: N/A

Read/Write: R

Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. A Signal input loss to that channel will trigger a bit failure (=1) on a per channel basis; Passing status (=0). Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent, will latch the Signal Status register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D/S Status, Signal Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Ch2**	**Ch1**	CHANNEL STATUS BIT

D/S Status, Reference Loss

Check the corresponding bit of the D/S Reference Status Register for status of the reference input for each active channel. A "1" means Reference Lost, "0" means Reference OK on active channels. Channels that are inactive are also set to "0". (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any D/S reference loss detection, transient or intermittent, will latch the D/S Reference Status Register. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Reference Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Status, Phase Lock Loss

Check the corresponding bit of the D/S Phase Lock Loss Register for status of the phase lock between the reference input and signal output for each active channel. A "1" means Phase Lock Loss has occurred, "0" means Phase Lock OK on active channels. Channels that are inactive are also set to "0". (Phase Lock loss is detected after 2 seconds). Phase Lock monitoring is always enabled. Any D/S Phase Lock Loss status failure, transient or intermittent, will latch the D/S Phase Lock Loss Status Register. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Phase Lock Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

D/S Phase

The phase of each individual channel may be offset from Reference. The phase may be adjusted at a resolution of 0.1 deg / bit. Program the desired lead or lag in integer as a 2's complement word format. For example, if channel 1 output signal is to lead the reference signal by 1.6 degrees, program the corresponding channel phase register to 16 (10h). If channel 1 output signal is to lag the reference signal by 1.6 degrees, program the corresponding channel phase register to -16 (FFF0h). Phase shift range is -90 <= x <= 90.

D/S Status, BIT Test

Check the corresponding bit of the D/S BIT Test Status Register for status of BIT (Test-Accuracy) Testing for each active channel. A ”1” means Accuracy OK; “0” means Accuracy Failed. Accuracy defaulted to ± 0.5 degrees output as compared to commanded angle. Channels that are inactive are also set to “0”. The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from D/S Status Registers within 2 seconds and, if enabled, an interrupt will be generated (See Interrupt Register).

This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured angle has an error greater the 0.2º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.2º during a test cycle, the test cycle will not generally indicate an error. Any D/S test status failure, transient or intermittent, will latch the *D/S Test Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, BIT Test	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Reference Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a reference input loss (D/S Status, Reference) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Reference Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reference Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Signal Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal input loss (D/S Status, Signal Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Signal Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Signal Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

BIT Test Fail Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a BIT Test Failure (D/S Status, BIT Test) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the BIT Test Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Test Fail Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Phase Lock Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a Phase Lock Loss (D/S Status, Phase Lock Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Phase Lock Loss Interrupt Vector.

	D1	D1	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Phase Lock Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Interrupt Vector

Write 16-bit integer (0-255). Used for failure reports.

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. If the same vector is loaded into each register, the same interrupt routine will be invoked by all interrupts. If unique vectors are loaded into the registers, a different Interrupt Service Routine (ISR) can be invoked by each interrupt.

- The Signal Loss interrupt vector will be serviced when the Signal Loss status is set and the interrupt has been enabled.
- The Reference Loss interrupt vector will be serviced when the Reference Loss status is set and the interrupt has been enabled.
- The BIT interrupt vector will be serviced when the Bit (failure) status is set and the interrupt has been enabled.
- The Lock Loss interrupt vector will be serviced when the Lock Loss status is set and the interrupt has been enabled.

D/S Test Enable

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X

Set bit to enable associated Built-In Self Test D2 or D3.

The on-line (D2) Test - Writing "1" to the D2 bit of the D/S Test Enable Register initiates status reporting of the automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output angle to the commanded angle. The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from *D/S Status Registers* within 2 seconds and if enabled, an interrupt will be generated (See Interrupt Register). Writing a "0" deactivates the status reporting. The testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of this card. Note: Outputs must be ON and Reference supplied for test to function. Card will write 55h (every 0.1 seconds) to the D/S Test (D2) Verify Register when D2 is enabled. User can periodically clear to 00h and then read the D/S Test (D2) Verify Register again, after 0.1 seconds, to verify that BIT Testing is activated. This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured angle has an error greater the 0.2º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.2º during a test cycle, the test cycle will not generally indicate an error. In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *D/S Signal* and *D/S Reference Status Registers.*

The off-line (D3) Test - Writing "1" to the D3 bit of the D/S Test Enable Register initiates a BIT Test that generates and tests 24 different angles to an accuracy of 0.2°. External reference is required and outputs must be ON. The D/S Status bits will be set to indicate an accuracy problem. Results are available in the *D/S Test Status Registers* and if enabled, an interrupt will be generated (See Interrupt Register). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the D/S Test Enable Register.

CAUTION: Outputs must be ON and Reference must be supplied during this test. The outputs are therefore active. Check connected loads for possible interaction.

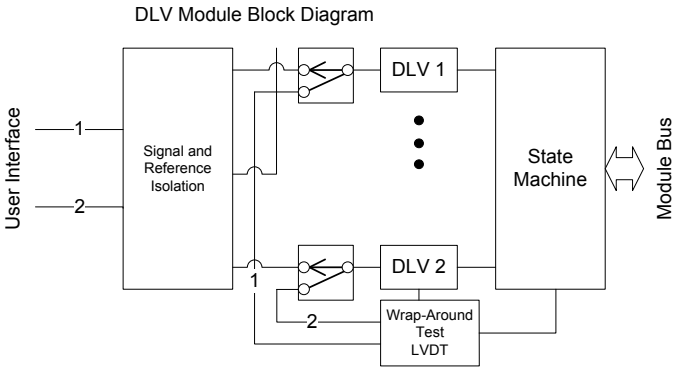
D/S (##) (PCI) MODULE MEMORY MAP

000	Wrap S/D Angle Lo CH1	R	140	D/S Set Reference Volt Lo CH1	W/R	1D0	D/S Phase Lock Status CH1/2	R
004	Wrap S/D Angle Hi CH1	R	144	D/S Set Reference Volt Hi CH1	W/R	1E8	D/S Set Phase Offset CH1	W/R
008	Wrap S/D Angle Lo CH2	R	148	D/S Set Reference Volt Lo CH2	W/R	1EC	D/S Set Phase Offset CH2	W/R
00C	Wrap S/D Angle Hi CH2	R	14C	D/S Set Reference Volt Hi CH2	W/R	1F4	D/S Rotation Status CH1/2	R
040	Wrap S/D Bandwidth CH1	W/R	160	D/S Set Signal Volt Lo CH1	W/R	3A0	D/S Start Rotation CH1	W
044	Wrap S/D Bandwidth CH2	W/R	164	D/S Set Signal Volt Hi CH1	W/R	3A4	D/S Start Rotation CH2	W
064	Wrap S/D REF Voltage CH1	R	168	D/S Set Signal Volt Lo CH2	W/R	3B0	D/S Stop Rotation CH1	W
068	Wrap S/D REF Voltage CH2	R	16C	D/S Set Signal Volt Hi CH2	W/R	3B4	D/S Stop Rotation CH2	W
070	Wrap S/D Signal Voltage CH1	R						
074	Wrap S/D Signal Voltage CH2	R	180	D/S BIT Test Enable	W/R	700	D/S Status, BIT Test	R
080	Wrap Signal Loss Threshold CH1	W/R	184	D/S Ratio 1/2	W/R	704	D/S Reference Loss Interrupt Enable	W/R
084	Wrap Signal Loss Threshold CH2	W/R	188	D2 Test Verify	W/R	708	D/S Signal Loss Interrupt Enable	W/R
08C	Wrap REF Loss Threshold CH1	W/R				70C	D/S BIT FAIL Interrupt Enable	W/R
090	Wrap REF Loss Threshold CH2	W/R	18C	D/S Output Mode	W/R	710	D/S Phase Lock Loss Interrupt Enable	W/R
0B0	Status, Signal Loss	R	190	D/S Rotation Mode	W/R			
0C0	D/S Write Angle Lo CH1	W/R	198	D/S SYN/RSL Select	W/R	768	Module Design Version	R
0C4	D/S Write Angle Hi CH1	W/R	19C	D/S Torque Rx Select	W/R	76C	Module Design Revision	R
0C8	D/S Write Angle Lo CH2	W/R	1A0	D/S Trigger Source Select CH1	W/R	770	Module DSP Revision	R
0CC	D/S Write Angle Hi CH2	W/R	1A4	D/S Trigger Source Select CH2	W/R	774	Module FPGA Revision	R
0E4	D/S Stop Angle CH1	R	1AC	D/S Trigger Slope Select	W/R	778	Module ID Revision	R
0E8	D/S Stop Angle CH2	R						
100	D/S Set Rotation Rate Lo CH1	W/R	1B0	D/S Output Enable	W/R	7C0	Vector Interrupt BIT Fail	W/R
104	D/S Set Rotation Rate Hi CH1	W/R	1C0	D/S Module Power Enable	W/R	7C4	Vector Interrupt Signal Loss	W/R
108	D/S Set Rotation Rate Lo CH2	W/R	1C8	D/S Active Channel Select	W/R	7C8	Vector Interrupt REF Loss	W/R
10C	D/S Set Rotation Rate Hi CH2	W/R	1CC	D/S Reference Status	R	7CC	Vector Interrupt Phase Lock Loss	W/R

DLV (Module ##*)

***See P/N**

Principle of Operation



This DLV Stimulus Module offers sixteen (16) two-wire or eight (8) three/four-wire "Programmable" LVDT/RVDT outputs with wrap-around self test and optional excitation supply. This card can be programmed and re-programmed in the field for any excitation and signal voltage between 2.0 and 28 volts. Operating frequency between 400 Hz and 10 KHz can be specified (See part number). One excitation is supplied for each A, B output pair. The output format can be programmed to simulate either two-wire or three/four-wire LVDT's. The transformation ratio (TR), same for each pair of outputs, sets the maximum output voltage with relation to the excitation voltage (TR = Max Output Voltage/Excitation Voltage). Use of a ratiometric design eliminates errors caused by excitation voltage variations, however, an absolute output (one that does not vary with excitation) can be programmed.

New features include a wrap for measuring, of each channel, the output position, velocity, current and carrier frequency (Pending). A background calibration feature (pending) will constantly adjust the outputs for load and environmental condition.

Built-in Test/Diagnostic Capability

Extensive Built-In-Test (BIT) diagnostics are implemented which include continuous transparent background accuracy testing as well as user-invoked testing. Two different tests (one on-line and one off-line) can be selected:

The on-line (D2) Test initiates automatic background BIT testing (on-line) that checks the output accuracy of each channel by comparing the measured output position to the commanded position. This test continuously checks each channel individually over the programmed signal range to an accuracy of 0.2% FS. Each DLV Signal output and Excitation input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in registers. User can periodically clear to 00h and then read *Test (D2) verification register* again, after 30 seconds, to verify that background bit testing is activated. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled.

The off-line (D3) Test initiates a BIT Test that generates and tests 20 different positions to an accuracy of 0.2%. External excitation is required and outputs must be ON. The DLV Status bits will be set to indicate an accuracy problem. Results are available in the *DLV Test Status Registers* and if enabled, an interrupt will be generated. The testing requires no external programming and can be initiated or terminated at any time.

CAUTION: Outputs must be ON and Excitation supplied during this test and therefore active. Check connected loads for possible interaction.

Wrap LVDT Position (Read)

Wrap-around positions are read from the *Wrap-around Channel Registers*. Each enabled DLV channel is measured and can be read from the corresponding *Wrap-around Channel Register*. The generated result is a 16-bit binary word (or 16-bit 2's compliment word) that represents position. The data is available at any time. **Note:** In 3/4-wire mode, only channels 1A, 2A need to be read.

Wrap (LVDT) Velocity

Type: One 16 bit 2's complement words

Range: 0x7FFF Maximum forward stroke (FWD) to 0x8000 maximum reverse (REV) stroke

Read/Write: R

Initialized Value: N/A

Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum FWD stroke, and 8000h being maximum REV stroke.

- When max. velocity is set to 190.7348 SPS, an actual speed of 10 SPS FWD would be read as 06B5h
- When max. velocity is set to 190.7348 SPS, an actual speed of 10 SPS REV would be read as F94Bh.
- When max. velocity is set to 63.5783 SPS, an actual speed of 10 SPS FWD would be read as 1421h.
- When max. velocity is set to 63.5783 SPS, an actual speed of 10 SPS REV would be read as EBDFh.

To convert a velocity word to SPS: Velocity in SPS = Maximum x Output / Full Scale
If Velocity Output were EBDFh, and maximum velocity were 63.5783 SPS;
then Velocity in SPS = 63.5783 x EBDFh / 32,768 = 63.5783 x -5153 / 32,768 = -10 SPS

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY High (VEL HI)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT, 2's Complement
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION

DLV Channel Excitation Voltage

Each individual channel input Excitation voltage "V_{EXC}" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180.

DLV Channel Signal Voltage

Each individual channel input signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180.

Signal Loss Threshold

Each individual channel input signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The signal loss detection circuitry can be tailored to report a signal loss (at SIG Status register Ch.1-4) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. For example, if channel 1 input signal loss voltage threshold is to be 7 Vrms, the programmed word to the corresponding register would be 700 (2BCh).

Excitation Loss Threshold

Each individual channel input excitation voltage "V_{EXC}" is measured and the value reported to a corresponding read register. The excitation loss detection circuitry can be tailored to report a excitation loss (at EXC Status Ch.1-4) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. For example, if channel 1 input excitation loss voltage threshold is to be 20 Vrms, the programmed word to the corresponding register would be 2000 (7D0h).

DLV Write Position

Enter the position as a 2's complement number in the corresponding Position Ch. Data Register within the range of -1.00 < Position < (+1.00 – lsb). In 3/4-wire mode, position is written only to the A channel of that number pair; the B channel register is ignored. In 2-wire mode the A and B channels are set independently. Factory default: POSITION = 0

Calculate using: register value = POSITION * 32768

Example: For a POSITION = -0.5 -> register value = -0.5 * 32768 = -16384 (0xC000)

Example: For a POSITION = 0.75 -> register value = 0.75 * 32768 = 24576 (0x6000)

The Output voltages in 3/4-wire mode are related to the position by:

Va = Excitation Voltage * TR * [Position/2 + 0.5]

Vb = Excitation Voltage * TR * [1 – (Position/2 + 0.5)]

The Output voltage in 2-wire mode is related to the position by:

V = Excitation Input * TR * Position

Note: Writing to an Input Position Register will stop any rotation initiated on that channel

DLV Response / Filter Time

(Pending)

Status, Signal Loss

Type: binary word

Range: N/A

Read/Write: R

Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. A Signal input loss to that channel will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent, will latch the Signal Status register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the *Open Status Interrupt Vector* in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Ch2**	**Ch1**	CHANNEL STATUS BIT

DLV Channel Frequency

Each individual channel excitation frequency is measured and the value reported to a corresponding read register. The input excitation frequency is reported to a resolution of 1 Hz. The output is in integer decimal format. For example, if channel 1 input excitation is 400 Hz, the output measurement word from the corresponding register would be 400.

DLV Set Channel Excitation Voltage

Set expected channel input Reference voltage "VREF" to a corresponding register. The input voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. For example, if channel 1 expected input REF voltage is 26.0 Vrms, the set word to the corresponding register would be 2600.

DLV Set Channel Signal Voltage

Set expected channel output signal voltage "V_{L-L}" to a corresponding register. The output voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. For example, if channel 1 Signal (V_{L-L}) voltage is to be 11.8 Vrms, the set word to the corresponding register would be 1180.

DLV Test Enable

Set bit to enable associated Built-In Self Test D2 or D3.

The on-line (D2) Test - Writing "1" to the D2 bit of the *DLV Test Enable Register* initiates status reporting of the automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output position to the commanded position. The status bits will be set to indicate an accuracy (0.05º) problem and the results can be read from DLV Status Registers within 2 seconds and if enabled, an interrupt will be generated (See Interrupt Register). Writing a "0" deactivates the status reporting. The testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of this card. Note: Outputs must be ON and Excitation supplied for test to function. Card will write 55h (every 0.1 seconds) to the DLV Test (D2) Verify Register when D2 is enabled. User can periodically clear to 00h and then read the *DLV Test (D2) Verify Register* again, after 0.1 seconds, to verify that BIT Testing is activated. This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured position has an error greater the 0.05º, a flag will be set in the appropriate register. If the input position is stepped more than 0.05º during a test cycle, the test cycle will not generally indicate an error.

In addition, each DLV Excitation input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *DLV Signal* and *DLV Excitation Status Registers.*

The off-line (D3) Test - Writing "1" to the D3 bit of the *DLV Test Enable Register* initiates a BIT Test that generates and tests 72 different positions to an accuracy of 0.05°. External excitation is required and outputs must be ON. The DLV Status bits will be set to indicate an accuracy problem. Results are available in the *DLV Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *DLV Test Enable Register.*

CAUTION: Outputs must be ON and Excitation must be supplied during this test. Output is therefore active. Check connected loads for possible interaction.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X

DLV Output Mode

The DLV Output Mode register is utilized for selecting either ratio-metric or absolute (fixed) mode voltages. Ratio-metric Mode, when selected, will cause the output signal voltage of the channel to vary with the input Excitation. Fixed Mode, when selected, will set the output to a required magnitude that will not vary with excitation input and set in the DLV Signal Voltage register regardless of the actual input excitation voltage applied. Set register to "0" for Ratio-metric Mode. Set register to "1" for Fixed Mode.

DLV 2-wire or 3/4-Wire Select

Where applicable, write an "01" or "10" (4-Wire = 01; 2-Wire = 10) to each corresponding channel bit pair, representing a channel commanded output format, of the *DLV 2-Wire or 3/4 Wire Select Register.*

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	CH2		CH1	
Synchro / Resolver Select	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	D1	D0

DLV Output Enable

(Pending – Outputs are always enabled)

Set the bit corresponding to each channel to be turned on, to "1" in the *Output On/Off Register.* To turn OFF a channel, set corresponding bit to "0". Default: Set to OFF. (OFF = "0"; ON = "1")

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Source Select	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

DLV Current

(Pending)

Each individual channel current output is measured and the value reported to a corresponding read register. The output current being delivered is reported to a resolution of 0.1 mA rms. The output is in integer decimal format. For example, if channel 1 output current delivered is 100 mA rms, the output measurement word from the corresponding register would be 1000.

DLV Active Channels

Set the bit, corresponding to each channel to be monitored during BIT testing, in the *Active Channel Register* for the particular DLV channel. "1" = Active; "0" = not used.

IMPORTANT: Omitting this step will produce false alarms because unused channels will set faults.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Active Channels	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

DLV Status, Excitation

Check the corresponding bit of the DLV Excitation Status Register for status of the excitation input for each active channel. A "1" means Excitation ON, "0" means Excitation Loss on active channels. Channels that are inactive are also set to "0". (Excitation loss is detected after 2 seconds). Excitation monitoring is always enabled. Any DLV excitation status failure, transient or intermittent, will latch the DLV Excitation Status Register. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DLV Status, Excitation	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

DLV Status, Excitation Loss

Check the corresponding bit of the *DLV Excitation Status Register* for status of the excitation input for each active channel. A "1" means Excitation Lost, "0" means Excitation OK on active channels. Channels that are inactive are also set to "0". (Excitation loss is detected after 2 seconds). Excitation monitoring is always enabled. Any DLV excitation loss detection, transient or intermittent will latch the DLV Excitation Status Register. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Excitation	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

DLV Status, Phase Lock Loss

Check the corresponding bit of the *DLV Phase Lock Loss Register* for status of the phase lock between the excitation input and signal output for each active channel. A "1" means In-Phase, "0" means Phase Lock Loss on active channels. Channels that are inactive are also set to "0". (Phase Lock loss is detected after 2 seconds). Phase Lock monitoring is always enabled. Any DLV Phase Lock Loss status failure, transient or intermittent, will latch the *DLV Phase Lock Loss Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DLV Status, Phase Lock Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

DLV Phase

Each individual channel Phase State is measured and the value reported to a corresponding read register.
(Pending)

DLV Current Threshold

(Pending)

DLV Status, BIT Test

Check the corresponding bit of the *DLV BIT Test Status Register* for status of BIT (Test-Accuracy) Testing for each active channel. A "1" means Accuracy OK; "0" means Accuracy Failed. Accuracy defaulted to ± 0.5 degrees output as compared to commanded position. Channels that are inactive are also set to "0". The status bits will be set to indicate an accuracy (0.05º) problem and the results can be read from *DLV Status Registers* within 2 seconds and if enabled, an interrupt will be generated (See *Interrupt Register)*.

This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured position has an error greater the 0.05º, a flag will be set in the appropriate register. If the input position is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error. Any DLV test status failure, transient or intermittent, will latch the *DLV Test Status Register.* Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DLV Status, BIT Test	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Excitation Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a excitation input loss (DLV Status, Excitation) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Excitation Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Excitation Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Signal Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal input loss (DLV Status, Signal Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Signal Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Signal Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

BIT Test Fail Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a BIT Test Failure (DLV Status, BIT Test) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the BIT Test Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Test Fail Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Phase Lock Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a Phase Lock Loss (DLV Status, Phase Lock Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Phase Lock Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Phase Lock Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CH2	CH1

Interrupt Vector

Write 16-bit integer (0-255). Used for failure reports.

The *Interrupt Vector Registers* store the vectors for the specific interrupts generated by the module. If the same vector is loaded into each register, the same interrupt routine will be invoked by all interrupts. If unique vectors are loaded into the registers, a different Interrupt Service Routine (ISR) can be invoked by each interrupt.

- The Signal Loss interrupt vector will be serviced when the Signal Loss status is set and the interrupt has been enabled.
- The Reference Loss interrupt vector will be serviced when the Reference Loss status is set and the interrupt has been enabled.
- The BIT interrupt vector will be serviced when the Bit (failure) status is set and the interrupt has been enabled.
- The Lock Loss interrupt vector will be serviced when the Lock Loss status is set and the interrupt has been enabled

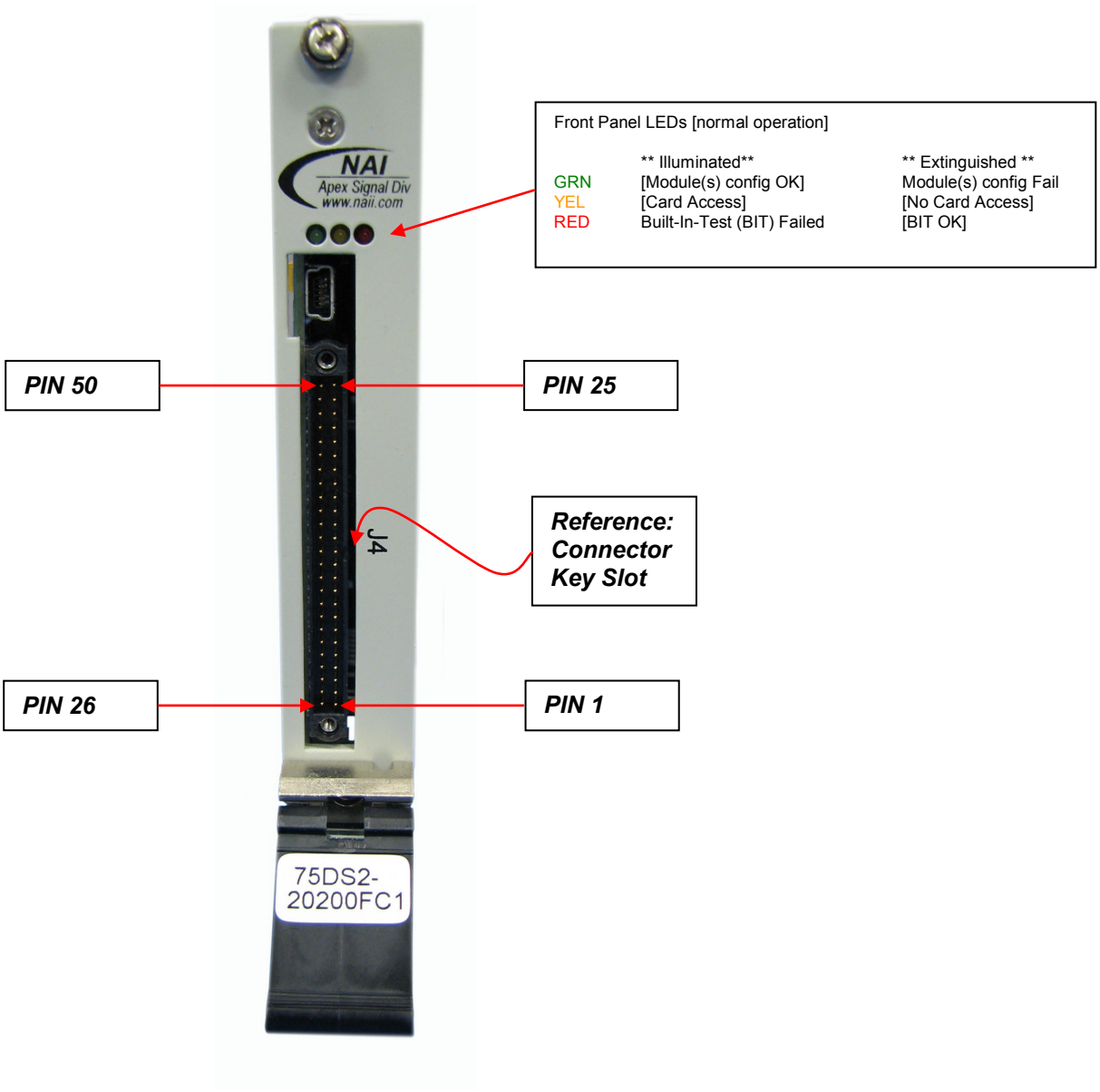
DLV (##) (PCI) MODULE MEMORY MAP

000	Wrap DLV Angle Lo CH1A	R	140	DLV Set Excitation Volt Lo CH1	W/R	300	DLV Position Lo CH1A	W/R
004	Wrap DLV Angle Hi CH1A	R	144	DLV Set Excitation Volt Hi CH1	W/R	304	DLV Position Hi CH1A	W/R
008	Wrap DLV Angle Lo CH2A	R	148	DLV Set Excitation Volt Lo CH2	W/R	308	DLV Position Lo CH1B	W/R
00C	Wrap DLV Angle Hi CH2A	R	14C	DLV Set Excitation Volt Hi CH2	W/R	30C	DLV Position Hi CH1B	W/R
010	Wrap DLV Angle Lo CH1B	R	160	DLV Set Signal Volt Lo CH1	W/R	310	DLV Position Lo CH2A	W/R
014	Wrap DLV Angle Hi CH1B	R	164	DLV Set Signal Volt Hi CH1	W/R	314	DLV Position Hi CH2A	W/R
018	Wrap DLV Angle Lo CH2B	R	168	DLV Set Signal Volt Lo CH2	W/R	318	DLV Position Lo CH2B	W/R
01C	Wrap DLV Angle Hi CH2B	R	16C	DLV Set Signal Volt Hi CH2	W/R	31C	DLV Position Hi CH2B	W/R
020	Wrap DLV Velocity Lo CH1 A	R	180	DLV BIT Test Enable	W/R			
024	Wrap DLV Velocity Hi CH1A	R				700	DLV Status, BIT Test	R
028	Wrap DLV Velocity Lo CH2 A	R	18C	DLV Output Mode	W/R	704	DLV Excitation Loss Interrupt Enable	W/R
02C	Wrap DLV Velocity Hi CH2A	R	198	DLV 2 or 4-Wire Select Mode	W/R	708	DLV Signal Loss Interrupt Enable	
030	Wrap DLV Velocity Lo CH1B	R				70C	DLV BIT FAIL Interrupt Enable	W/R
034	Wrap DLV Velocity Hi CH1B	R	1B0	DLV Output Enable	W/R	710	DLV Phase Lock Loss Interrupt Enable	W/R
038	Wrap DLV Velocity Lo CH2B	R	1B4	DLV Current CH1	R			
03C	Wrap DLV Velocity Hi CH2B	R	1B8	DLV Current CH2	R	768	Module Design Version	R
064	Wrap DLV Signal Voltage CH1	R	1C8	DLV Active Channel Select	W/R	76C	Module Design Revision	R
068	Wrap DLV Signal Voltage CH2	R	1CC	DLV Status, Excitation Loss	R	770	Module DSP Revision	R
070	Wrap DLV EXC Voltage CH1	R	1D0	DLV Phase Lock Status CH1/2	R	774	Module FPGA Revision	R
074	Wrap DLV EXC Voltage CH2	R	1E8	DLV Set Phase Offset CH1	W/R	778	Module ID Revision	R
080	Wrap Signal Loss Threshold	W/R	1EC	DLV Set Phase Offset CH2	W/R	7C0	Vector Interrupt BIT Fail	W/R
08C	Wrap Excitation Loss Threshold	W/R	200	DLV Current Threshold CH1	W/R	7C4	Vector Interrupt EXC Loss	W/R
0B0	Status, Signal Loss	R	204	DLV Current Threshold CH2	W/R	7C8	Vector Interrupt Signal Loss	W/R
0D8	DLV Response / Filter Time CH1	W/R				7CC	Vector Interrupt Phase Lock Loss	W/R
0DC	DLV Response / Filter Time CH2	W/R						

FRONT AND REAR PANEL CONNECTORS

Front Panel Connector J4: J4 Front I/O Connector: Harwin M80-5415022;
Mate: Harwin M80-486 product family (mating connector kit is available from Harwin as P/N M80-9415005)

Rear Panel Connectors J1, J2: J1 – cPCI interface only
J2 – I/O defined (see module slot pin-out configuration)



NAI Synchro / Resolver naming convention:

Signal	Resolver	Synchro
S1	SIN(-)	X
S2	COS(+)	Z
S3	SIN(+)	Y
S4	COS(-)	(No connect)

I/O CONNECTORS – PIN OUTS

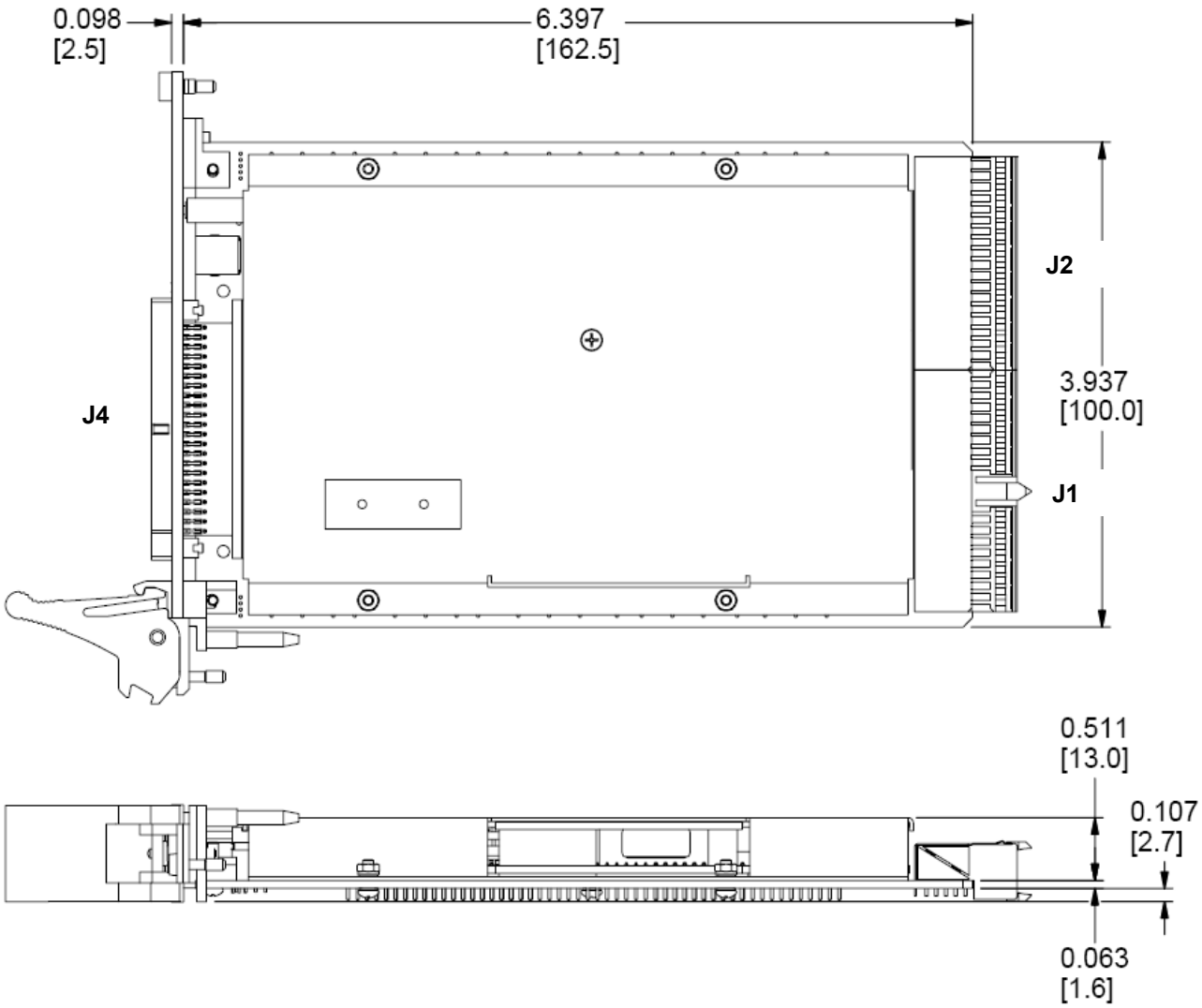
SLOT 1 - D/S OR DLV

Front I/O J4	Rear I/O J2	Slot 1 Single Channel D/S-R	Slot 1 Dual Channel D/S-R	Slot 1 Dual Channel DLV
1	E1		Ch.1-S1	Ch1 A Lo
2	E3	Ch1 S3	Ch.1-S3	Ch1 A Hi
3	E2	Ch1 S1	Ch.1-S2	Ch1 B Hi
4	E4		Ch.1-S4	Ch1 B Lo
5	D1	Ch1 RHI	Ch.1-RHi	Ch1 Exc Hi
30	D2	Ch1 RLO	Ch.1-RLo	Ch1 Exc Lo
26	C1		Ch.1- Sense S1	
27	C3	Ch.1- Sense S3	Ch.1- Sense S3	
28	C2	Ch.1- Sense S1	Ch.1- Sense S2	
29	C4		Ch.1- Sense S4	
6	E7		Ch.2-S1	Ch2 A Lo
7	E9	Ch1 S4	Ch.2-S3	Ch2 A Hi
8	E8	Ch1 S2	Ch.2-S2	Ch2 B Hi
9	E10		Ch.2-S4	Ch2 B Lo
10	D5		Ch.2-RHi	Ch2 Exc Hi
35	D6		Ch.2-RLo	Ch2 Exc Lo
31	C7		Ch.2- Sense S1	
32	C9	Ch.1- Sense S4	Ch.2- Sense S3	
33	C8	Ch.1- Sense S2	Ch.2- Sense S2	
34	C10		Ch.2- Sense S4	
21	D21	RHI-OUT	RHI-OUT	RHI-OUT
22	B21	+12V Ext	+12V Ext	+12V Ext
23	F1	GND	GND	GND
24	B19	-12V Ext	-12V Ext	-12V Ext
25	---	TRIG1+	TRIG1+	TRIG1+
---	B3		Ch1 EXT-SIN-HI	
---	B2		Ch1 EXT-COS-HI	
---	B1		Ch1 EXT-GND	
---	B7		Ch2 EXT-SIN-HI	
---	B6		Ch2 EXT-COS-HI	
---	B5		Ch2 EXT-GND	
---	A2		Ch 1 ON-OFF-HI (+5V)	
---	A1		Ch1 ON-OFF-LO	
---	A6		Ch 2 ON-OFF-HI (+5V)	
---	A5		Ch2 ON-OFF-LO	
---	A4		Ch1 BIT HI	
---	A3		Ch1 BIT -LO (GND)	
---	A8		Ch2 BIT HI	
---	A7		Ch2 BIT -LO (GND)	

SLOT 2 - D/S OR DLV

Front I/O J4	Rear I/O J2	Slot 2 Single Channel D/S-R	Slot 2 Dual Channel D/S-R	Slot 2 Dual Channel DLV
11	E13		Ch.3-S1	Ch3 A Lo
12	E15	Ch2 S3	Ch.3-S3	Ch3 A Hi
13	E14	Ch2 S1	Ch.3-S2	Ch3 B Hi
14	E16		Ch.3-S4	Ch3 B Lo
15	D11	Ch2 RHI	Ch.3-RHi	Ch3 Exc Hi
40	D12	Ch2 RLO	Ch.3-RLo	Ch3 Exc Lo
36	C13		Ch.3- Sense S1	
37	C15	Ch.2- Sense S3	Ch.3- Sense S3	
38	C14	Ch.2- Sense S1	Ch.3- Sense S2	
39	C16		Ch.3- Sense S4	
16	E19		Ch.4-S1	Ch4 A Lo
17	E21	Ch2 S4	Ch.4-S3	Ch4 A Hi
18	E20	Ch2 S2	Ch.4-S2	Ch4 B Hi
19	E18		Ch.4-S4	Ch4 B Lo
20	D17		Ch.4-RHi	Ch4 Exc Hi
45	D18		Ch.4-RLo	Ch4 Exc Lo
41	C19		Ch.4- Sense S1	
42	C21	Ch.2- Sense S4	Ch.4- Sense S3	
43	C20	Ch.2- Sense S2	Ch.4- Sense S2	
44	C18		Ch.4- Sense S4	
46	D20	RLO-0UT	RLO-0UT	RLO-0UT
47	A21	+12V Ext	+12V Ext	+12V Ext
48	F2	GND	GND	GND
49	A19	-12V Ext	-12V Ext	-12V Ext
50	---	TRIG1-	TRIG1-	TRIG1-
---	B11		Ch3 EXT-SIN-HI	
---	B10		Ch3 EXT-COS-HI	
---	B9		Ch3 EXT-GND	
---	B15		Ch4 EXT-SIN-HI	
---	B14		Ch4 EXT-COS-HI	
---	B13		Ch4 EXT-GND	
---	A10		Ch 3 ON-OFF-HI (+5V)	
---	A9		Ch3 ON-OFF-LO	
---	A14		Ch 4 ON-OFF-HI (+5V)	
---	A13		Ch4 ON-OFF-LO	
---	A12		Ch1 BIT HI	
---	A11		Ch3 BIT -LO (GND)	
---	A16		Ch4 BIT HI	
---	A15		Ch4 BIT -LO (GND)	

Dimensions



PART NUMBER DESIGNATION

75DS2 - XX XX X X X X - XX

Slot 1
(Enter code – D/S or DLV See module codes)
(Enter **Z0** if not populated)

Slot 2
(Enter code – D/S or DLV See module codes)
(Enter **Z0** if not populated)

ON-BOARD REFERENCE SUPPLY (M7)
Does not use up a Module slot.
0 = No On-Board Reference Module
1 = 2-28Vrms, 360-10kHz Programmable On-Board Reference Module
2 = Reserved for future use
3 = 115Vrms Fixed, 360-10kHz Programmable On-Board Reference Module

MECHANICAL
F = Front Panel (J4) I/O only
P = Rear (J2) I/O only
W = P with Wedge locks
B = Front Panel (J4) and Rear (J2) I/O

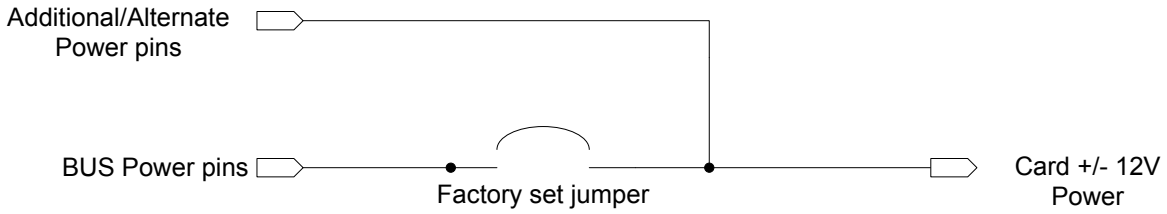
ENVIRONMENTAL
C = 0 TO 70°C
E = -40 TO +85°C
H = E with conformal coating
K = C with conformal coating

CODE
(Reserved for special configurations – leave open for standard

±12V DC POWER OPTION Note 1
0 = cPCI Power is used
1 = cPCI ±12VDC Power is isolated from PCB power planes. User to connect external power via J4 Front Panel connector (See Pin Outs tables)

Note 1: ±12 VDC Power Option

Additional or alternate ±12V power pins are available that may be specified at time of order (See part number). The additional power pins are provided in case the available ±12VDC bus power is insufficient for the card configuration. When the factory installed jumpers are connected, ±12VDC power is derived from the backplane power planes. The additional power pins will now be HOT. When the jumper is disconnected, the card will derive its ±12VDC from the external power pins.



Factory set jumper configuration:
INSTALLED: +/-12 VDC Power Option "0" (Default)
REMOVED: +/-12 VDC Power Option "1"

D/S Module Codes – Single Channel

Code	Format	Output (V_{L-L}) (Vrms)	Ref (V_{REF}) (Vrms)	Frequency (Hz)	Max Load (VA)	Notes
30	SYN	11.8	2 – 115	400 – 1K	3.0	
31	RSL	2 – 28	2 – 115	400 – 1K	3.0	
35	SYN	11.8	2 – 115	47 - 440	3.0	
36	RSL	2 – 28	2 – 115	47 - 440	3.0	
3A	RSL	2 – 28	2 – 115	1K – 3K	3.0	
3B	RSL	2 – 28	2 – 115	3K – 5K	3.0	
3C	RSL	2 – 28	2 – 115	5K – 7K	3.0	
3D	RSL	2 – 28	2 – 115	7K – 10K	3.0	
3E	SYN	2 - 11.8	2-115	1K – 3K	3.0	(verify application loading)
3F	SYN	2 - 11.8	2-115	3K – 5K	3.0	(verify application loading)
3G	SYN	2 - 11.8	2-115	5K – 7K	3.0	(verify application loading)
3H	SYN	2 - 11.8	2-115	7K – 10K	3.0	(verify application loading)
3J	SYN	2 – 28	2 – 115	1K – 3K	3.0	(verify application loading)
3K	SYN	2 – 28	2 – 115	3K – 5K	3.0	(verify application loading)
3L	SYN	2 – 28	2 – 115	5K – 7K	3.0	(verify application loading)
3M	SYN	2 – 28	2 – 115	7K – 10K	3.0	(verify application loading)
40	SYN	90	2 – 115	400 – 1K	3.0	
41	RSL	90	2 – 115	400 – 1K	3.0	
45	SYN	90	2 – 115	47 - 440	3.0	
46	RSL	90	2 – 115	47 - 440	3.0	

D/S Module Codes – Two Channel

Code	Format	Output (V_{L-L}) (Vrms)	Ref (V_{REF}) (Vrms)	Frequency (Hz)	Max load (VA)	Notes
10	SYN	2 – 28	2 – 115	400 – 1K	1.5	
11	RSL	2 – 28	2 – 115	400 – 1K	1.5	
12*	PRG S / R	2 – 28	2 – 115	400 – 1K	1.5	Programmable – Synchro/Resolver
13	SYN / RSL	2 – 28	2 – 115	400 – 1K	1.5	Channel 1 = SYN Dual Op Amp, Channel 2 = RSL
14	RSL / SYN	2 – 28	2 – 115	400 – 1K	1.5	Channel 1 = RSL, Channel 2 = SYN Dual Op Amp
15	SYN	2 – 28	2 – 115	47 - 440	1.5	
16	RSL	2 – 28	2 – 115	47 - 440	1.5	
17*	PRG S / R	2 – 28	2 – 115	47 - 440	1.5	Programmable – Synchro/Resolver
18	SYN / RSL	2 – 28	2 – 115	47 - 440	1.5	Channel 1 = SYN Dual Op Amp, Channel 2 = RSL
19	RSL / SYN	2 – 28	2 – 115	47 - 440	1.5	Channel 1 = RSL, Channel 2 = SYN Dual Op Amp
1A	RSL	2 – 28	2 – 115	1K – 3K	1.5	
1B	RSL	2 – 28	2 – 115	3K – 5K	1.5	
1C	RSL	2 – 28	2 – 115	5K – 7K	1.5	
1D	RSL	2 – 28	2 – 115	7K – 10K	1.5	
1E	PRG S / DLV	2 - 11.8	2 – 115	400 – 1K	1.5	
1F	SYN	2 - 11.8	2 – 115	47 – 400	1.5	
1G	SYN	2 - 11.8	2-115	1K – 3K	1.5	
1H	SYN	2 - 11.8	2-115	3K – 5K	1.5	
1J	SYN	2 - 11.8	2-115	5K – 7K	1.5	
1K	SYN	2 - 11.8	2-115	7K – 10K	1.5	
1L	SYN	2 – 28	2 – 115	1K – 3K	1.5	
1M	SYN	2 – 28	2 – 115	3K – 5K	1.5	
1N	SYN	2 – 28	2 – 115	5K – 7K	1.5	
1P	SYN	2 – 28	2 – 115	7K – 10K	1.5	
20	SYN	90	2 – 115	400 – 1K	2.2	
21	RSL	90	2 – 115	400 – 1K	2.2	
22*	PRG S / R	90	2 – 115	400 – 1K	2.2	Programmable – Synchro/Resolver
23	SYN / RSL	90	2 – 115	400 – 1K	2.2	Channel 1 = SYN, Channel 2 = RSL
24	RSL / SYN	90	2 – 115	400 – 1K	2.2	Channel 1 = RSL, Channel 2 = SYN
25	SYN	90	2 – 115	47 - 440	2.2	
26	RSL	90	2 – 115	47 - 440	2.2	
27*	PRG S / R	90	2 – 115	47 - 440	2.2	Programmable – Synchro/Resolver
28	SYN / RSL	90	2 – 115	47 - 440	2.2	Channel 1 = SYN, Channel 2 = RSL
29	RSL / SYN	90	2 – 115	47 - 440	2.2	Channel 1 = RSL, Channel 2 = SYN

*Note: Synchro or Resolver programmability uses a miniature mechanical relay for this task. This capability is not recommended for Military embedded applications

DLV Module Codes

Code	Format	Output (V_{L-L}) (Vrms)	Ref (V_{REF}) (Vrms)	Frequency (Hz)	Max Load (VA)	Notes
50	DLV	2 – 28	2 – 28	400 – 1K	50	2 channels avail in 4-wire mode, 4 channels avail in 2-wire mode
51	DLV	2 – 28	2 – 28	47 - 440	51	2 channels avail in 4-wire mode, 4 channels avail in 2-wire mode
52	DLV	2 – 28	2 – 28	1K – 3K	52	2 channels avail in 4-wire mode, 4 channels avail in 2-wire mode
53	DLV	2 – 28	2 – 28	3K – 5K	53	2 channels avail in 4-wire mode, 4 channels avail in 2-wire mode
54	DLV	2 – 28	2 – 28	5K – 7K	54	2 channels avail in 4-wire mode, 4 channels avail in 2-wire mode
55	DLV	2 – 28	2 – 28	7K – 10K	55	2 channels avail in 4-wire mode, 4 channels avail in 2-wire mode
5A	DLV	2 – 28	2 – 28	400 – 1K	0.1	Programmable 2 or 4 wire mode
5B	DLV	2 – 28	2 – 28	47 - 440	0.1	Programmable 2 or 4 wire mode
5C	DLV	2 – 28	2 – 28	1K – 3K	0.1	Programmable 2 or 4 wire mode
5D	DLV	2 – 28	2 – 28	3K – 5K	0.1	Programmable 2 or 4 wire mode
5E	DLV	2 – 28	2 – 28	5K – 7K	0.1	Programmable 2 or 4 wire mode
5F	DLV	2 – 28	2 – 28	7K – 10K	0.1	Programmable 2 or 4 wire mode

REVISION PAGE

Revision	Description of Change	Engineer	Date
A	Preliminary Specification	FR	6/26/08
A1	Sales Release	FR	9/26/08
A2	Product Configuration page, Correction to front panel connector pinouts (rotated 180 deg)	AS	12/18/08