

TX Family Computer On Module

- Processor ARM® Cortex®-A7 based
NXP i.MX6 UltraLite
MCIMX6G2, 528 MHz
- RAM 256MB 16-bit DDR3 SDRAM
- ROM 128MB NAND Flash / 4GB eMMC
- Power supply Single 3.1V to 5.5V
- Size 26mm SO-DIMM
- Temperature -40°C/-25°C to 85°C

Key Features

- ARM® Cortex®-A7 Core
 - ARM TrustZone
 - NEON Multimedia Architecture
 - VFP
 - 128 Kbyte L2 Cache
- Display support:
 - LCD TFT controller, 24bpp
 - Pixel-processing pipeline (PXP)
- Crypto Engine (AES/TDES/SHA), Secure Boot

Connectivity

- Two 10/100Mbps Ethernet ports
- Two High Speed USB 2.0 ports
- 8-bit Parallel CSI Camera Interface
- Up to 8x UART, 3x on standard TXCoM pinout
- SDIO interface
- Synchronous Serial Audio Interface (I2S/SAI)
- Two-wire Interface up to 400 Kbits/s (I2C)
- Master/Slave Serial Peripheral Interface (SPI)
- 2x Controller Area Network (FlexCAN)
- 12-bit ADC
- 3.3V I/O

OS Support

- Windows Embedded Compact 7
- Linux



528MHz
Cortex®-A7



Processor

Expanding the i.MX 6 series, the i.MX 6UltraLite is a high performance, ultra-efficient processor family featuring an advanced implementation of a single ARM® Cortex®-A7 core, which operates at speeds up to 528 MHz.

- The single ARM® Cortex®-A7 core can provide a more cost-effective and more power efficient solution
- Processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, On-The-Fly DRAM encryption, secure boot and secure software downloads
- Processor supports connections to a variety of interfaces: two high-speed USB on-the-go with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), two 12-bit ADC modules with up to 10 total input channels, two CAN ports and a variety of other popular interfaces (such as UART, I2C, and I2S serial audio)

Power Supply

The TXUL accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (up to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

Standard TXCOM pinout:

- 4-wire UARTs (x3)
- LCD
- I2C / PWM
- Serial Audio Interfaces
- 4-wire SD-Card/SDIO
-

High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

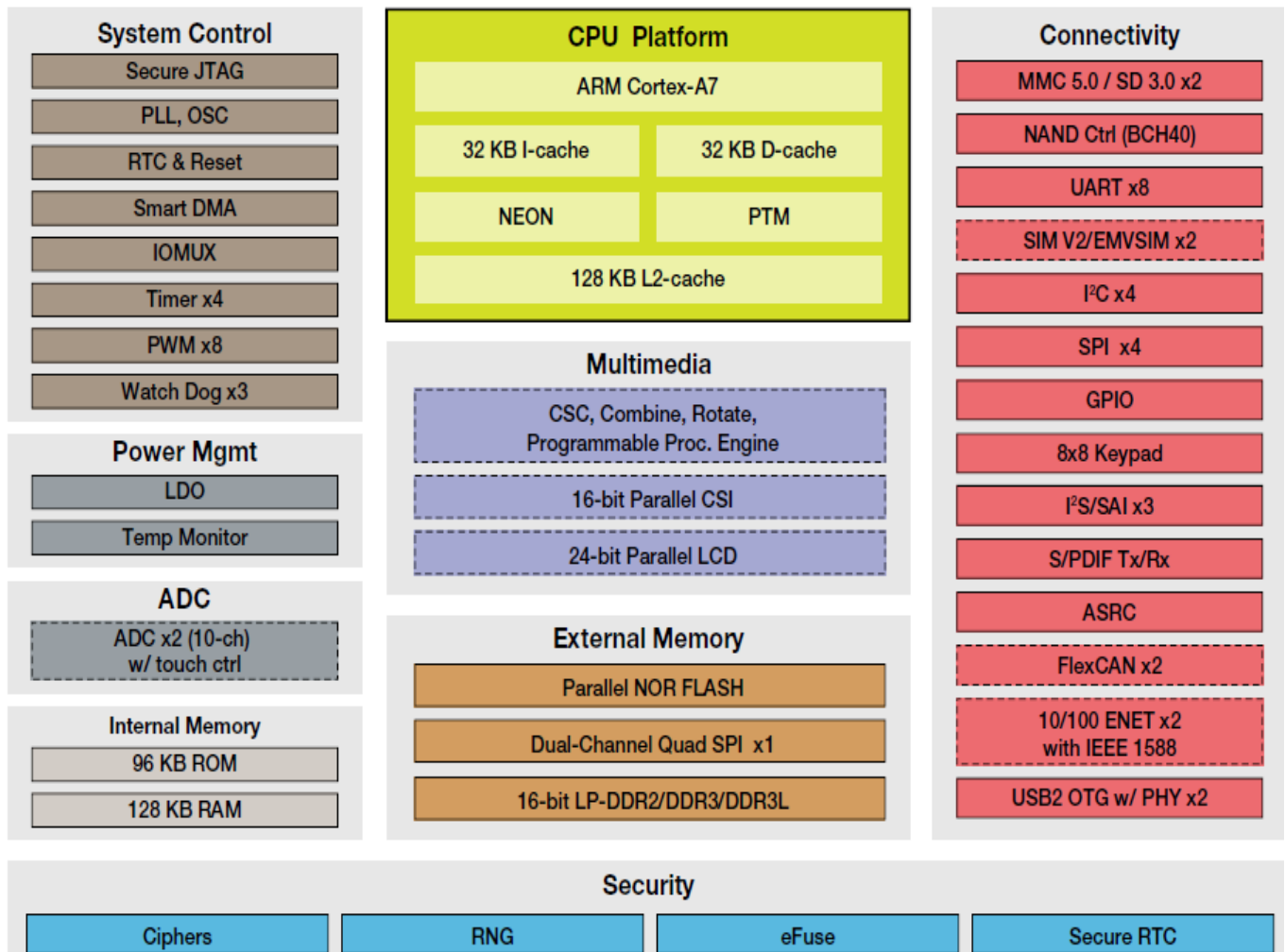
- 10/100 Mbps Ethernet
- 480 Mbps USB OTG (Host or Device)
- 480 Mbps USB Host

Read more in our TX-Guide:

www.karo-electronics.com/TX-Guide

Software and Tools

The TXUL Computer on Module is supported by standard TX development kits. The TX Mainboard 7 comes with an pre-installed Linux® operating system.



| Order Number | CPU | SDRAM | Flash | Temp. Grade |
|------------------------|-----------------|-------|----------------|------------------------|
| TX6UL/528/256S/128F/I | 528MHz MCIMX6G2 | 256MB | 128MB SLC NAND | industrial -40°C..85°C |
| TX6UL/528/256S/4GF/E85 | 528MHz MCIMX6G2 | 256MB | 4GB EMMC | industrial -25°C..85°C |

| PINOUT | | | | | | |
|-------------------------------------|--------|--------------|--|---|--------------------|--|
| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
| POWER SUPPLY & RESET | | | | | | |
| 1-4 | power | VIN | | | | Module power supply input (3.3V-5V) |
| 5-7, 9-12 | power | VOUT | | | | 3.3V power supply output. Supplied by RN5T567 DCDC4 (max. 300mA, VIN>4.3V) |
| 8 | 3V3 | BOOTMODE | | | 10K-PU | Boot mode select H: Boot from NAND/eMMC / L: Boot from UART/USB |
| 13 | power | | Connected through a 240 Ohms resistor to VDD_SNV5_IN | | | i.MX6UL SNVS backup power supply. Supply voltage must be held between 2.9V and 3.3V if the system requires keeping real time and other data on OFF state. This pin is connected to RN5T567 LDORTC1 (3V/30mA) through an onboard 240R resistor. Leave unconnected if the system does not require keeping real time and other data on OFF state. |
| 14 | VIN | PMIC_PWR_BTN | | | 10K-PU | Connected to RN5T567 PWRON Leave unconnected, if not used. |
| 15 | 3V3 | #RESET_OUT | | | 10K-PU | Connected to RN5T567 RESET0 May be used to reset peripherals on the carrier board. |
| 16 | VIN | #POR | POR_B | | 10K-PU | Power On Reset — Active low input signal Leave unconnected, if not used. |
| 17 | | #RESET_IN | POR_B | | | Wire ored to pin 16 |
| 18 | GND | GND | | | | |
| Ethernet | | | | | | |
| 19 | analog | ETN_TXN | | | | Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics. |
| 20 | 3V3 | #ETN_LED2 | | | | Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation. |
| 21 | analog | ETN_TXP | | | | Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics. |
| 22 | power | ETN_3V3 | | | | +3.3V analog power supply output to magnetics |
| 23 | analog | ETN_RXN | | | | Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics. |
| 24 | 3V3 | #ETN_LED1 | | | | Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity. |
| 25 | analog | ETN_RXP | | | | Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics. |
| 26 | GND | GND | | | | |
| USB-HOST | | | | | | |
| 27 | 3V3 | USBH_VBUSEN | GPIO1_IO02 | I2C1_SCL GPT1_COMPARE2 USB_OTG2_PWR ENET1_REF_CLK_25M USDHC1_WP SDMA_EXT_EVENT00 SRC_ANY_PU_RESET UART1_TX | GPIO1[2] | Active high external 5V supply enable. This pin is used to enable the external VBUS power supply. |
| 28 | 3V3 | #USBH_OC | GPIO1_IO03 | I2C1_SDA GPT1_COMPARE3 USB_OTG2_OC USDHC1_CD_B CCM_DIO_EXT_CLK SRC_TESTER_ACK UART1_RX | GPIO1[3] 10K-PU | Active low over-current indicator input connected to a GPIO. |
| 29 | analog | USBH_DM | USB_OTG2_DN | | | D- pin of the USB cable |
| 30 | analog | USBH_VBUS | USB_OTG2_VBUS | | | VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs. |
| 31 | analog | USBH_DP | USB_OTG2_DP | | | D+ pin of the USB cable |
| 32 | GND | GND | | | | |
| USB-OTG / 2nd CAN | | | | | | |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|--|--------|-------------------------|--------------------------|---|---------------------|---|
| 33 | | | | | | Not connected |
| 34 | 3V3 | USBOTG_VBUSEN CAN_TX | UART3_CTS_B | ENET2_RX_CLK FLEXCAN1_TX CSI_DATA10 ENET1_1588_EVENT1_IN EPIT2_OUT | GPIO1[26] | Active high external 5V supply enable. This pin is used to enable the external VBUS power supply. |
| 35 | analog | USBOTG_DM | USB_OTG1_DN | | | D- pin of the USB cable |
| 36 | 3V3 | #USBOTG_OC CAN_RX | UART3_RTS_B | ENET2_TX_ER FLEXCAN1_RX CSI_DATA11 ENET1_1588_EVENT1_OUT WDOG1_WDOG_B | GPIO1[27] 10K-PU | Active low over-current indicator input connected to a GPIO. |
| 37 | analog | USBOTG_DP | USB_OTG1_DP | | | D+ pin of the USB cable |
| 38 | analog | USBOTG_VBUS | USB_OTG1_VBUS | | | VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs. |
| 39 | GND | GND | | | | |
| I2C | | | | | | |
| 40 | 3V3 | I2C_DATA | GPIO1_IO01 | I2C2_SDA GPT1_COMPARE1 USB_OTG1_OC ENET2_REF_CLK2 MQS_LEFT ENET1_1588_EVENT0_OUT SRC_EARLY_RESET WDOG1_WDOG_B | GPIO1[1] | I2C Data |
| 41 | 3V3 | I2C_CLK | GPIO1_IO00 | I2C2_SCL / MQS_RIGHT GPT1_CAPTURE1 ANATOP_OTG1_ID ENET1_REF_CLK1 ENET1_1588_EVENT0_IN SRC_SYSTEM_RESET WDOG3_WDOG_B | GPIO1[0] | I2C Clock |
| PWM | | | | | | |
| 42 | 3V3 | PWM | NAND_DQS | RAWNAND_DQS CSI_FIELD / EIM_WAIT QSPI_A_SS0_B PWM5_OUT SDMA_EXT_EVENT01 SPDIF_EXT_CLK | GPIO4[16] | PWM Output |
| 1-WIRE | | | | | | |
| 43 | | | | | | Not connected |
| CSPI – Configurable Serial Peripheral Interface | | | | | | |
| 44 | 3V3 | CSPI_SS | UART4_RX_DATA | ENET2_TDATA03 I2C1_SDA CSI_DATA13 CSU_CSU_ALARM_AUT01 ECSPI2_SS0 | GPIO1[29] | Slave Select (Selectable polarity) signal |
| 45 | 3V3 | CSPI_SS | JTAG_MOD | SJC_MOD GPT2_CLK SPDIF_OUT ENET1_REF_CLK_25M CCM_PMIC_RDY SDMA_EXT_EVENT00 | GPIO1[10] 1K-PD | Slave Select (Selectable polarity) signal |
| 46 | 3V3 | CSPI_MOSI | UART5_TX_DATA | ECSPI2_MOSI ENET2_CRS I2C2_SCL CSI_DATA14 CSU_CSU_ALARM_AUT00 | GPIO1[30] | Master Out/Slave In signal |
| 47 | 3V3 | CSPI_MISO | UART5_RX_DATA | ENET2_COL I2C2_SDA CSI_DATA15 CSU_CSU_INT_DEB ECSPI2_MISO | GPIO1[31] | Master In/Slave Out signal |
| 48 | 3V3 | CSPI_SCLK | UART4_TX_DATA | ENET2_TDATA02 I2C1_SCL CSI_DATA12 CSU_CSU_ALARM_AUT02 ECSPI2_SCLK | GPIO1[28] | Serial Clock signal |
| 49 | | | | | | Not connected |
| 50 | GND | GND | | | | |
| SD – Secure Digital Interface 1 | | | | | | |
| 51 | 3V3 | SD1_CD | NAND_CE1_B | RAWNAND_CE1_B USDHC1_DATA6 | GPIO4[14] | SD Card Detect – connected to a GPIO |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|----------------------------|------|----------|--------------------------|--|-----------|---|
| | | | | QSPI_A_DATA02 ECSPI3_MOSI EIM_ADDR18 UART3_CTS_B | | |
| 52 | 3V3 | SD1_D[0] | SD1_DATA0 | USDHC1_DATA0 GPT2_COMPARE3 SAI2_TX_SYNC FLEXCAN1_TX EIM_ADDR21 ANATOP_OTG1_ID | GPIO2[18] | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added. |
| 53 | 3V3 | SD1_D[1] | SD1_DATA1 | USDHC1_DATA1 GPT2_CLK SAI2_TX_BCLK FLEXCAN1_RX EIM_ADDR22 USB_OTG2_PWR | GPIO2[19] | |
| 54 | 3V3 | SD1_D[2] | SD1_DATA2 | USDHC1_DATA2 GPT2_CAPTURE1 SAI2_RX_DATA FLEXCAN2_TX EIM_ADDR23 CCM_CLKO1 USB_OTG2_OC | GPIO2[20] | |
| 55 | 3V3 | SD1_D[3] | SD1_DATA3 | USDHC1_DATA3 GPT2_CAPTURE2 SAI2_TX_DATA FLEXCAN2_RX EIM_ADDR24 CCM_CLKO2 ANATOP_OTG2_ID | GPIO2[21] | |
| 56 | 3V3 | SD1_CMD | SD1_CMD | USDHC1_CMD GPT2_COMPARE1 SAI2_RX_SYNC SPDIF_OUT EIM_ADDR19 SDMA_EXT_EVENT00 USB_OTG1_PWR | GPIO2[16] | |
| 57 | 3V3 | SD1_CLK | SD1_CLK | USDHC1_CLK GPT2_COMPARE2 SAI2_MCLK SPDIF_IN EIM_ADDR20 USB_OTG1_OC | GPIO2[17] | SD Output Clock. |
| 58 | GND | GND | | | | |
| 1st UART | | | | | | |
| 59 | 3V3 | TXD | UART1_TX_DATA | ENET1_RDATA02 I2C3_SCL CSI_DATA02 GPT1_COMPARE1 SPDIF_OUT | GPIO1[16] | Application UART 1 Transmit Data output signal |
| 60 | 3V3 | RXD | UART1_RX_DATA | ENET1_RDATA03 I2C3_SDA CSI_DATA03 GPT1_CLK SPDIF_IN | GPIO1[17] | Application UART 1 Receive Data input signal |
| 61 | 3V3 | RTS | UART1_RTS_B | ENET1_TX_ER USDHC1_CD_B CSI_DATA05 ENET2_1588_EVENT1_OUT USDHC2_CD_B | GPIO1[19] | Application UART 1 Request to Send input signal Alternate function USDHC2 used for eMMC |
| 62 | 3V3 | CTS | UART1_CTS_B | ENET1_RX_CLK USDHC1_WP CSI_DATA04 ENET2_1588_EVENT1_IN USDHC2_WP | GPIO1[18] | Application UART 1 Clear to Send output signal |
| 2nd UART | | | | | | |
| 63 | 3V3 | TXD | UART2_TX_DATA | ENET1_TDATA02 I2C4_SCL CSI_DATA06 GPT1_CAPTURE1 ECSPI3_SS0 | GPIO1[20] | Application UART 2 Transmit Data output signal |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|------------------------------------|------|-----------|--------------------------|--|-----------|--|
| 64 | 3V3 | RXD | UART2_RX_DATA | ENET1_TDATA03 I2C4_SDA CSI_DATA07 GPT1_CAPTURE2 SJC_DONE ECSPI3_SCLK | GPIO1[21] | Application UART 2 Receive Data input signal |
| 65 | 3V3 | RTS | UART3_RX_DATA | ENET2_RDATA03 SIM2_PORT0_PD CSI_DATA00 UART2_RTS_B EPIT1_OUT | GPIO1[25] | Application UART 2 Request to Send input signal |
| 66 | 3V3 | CTS | UART3_TX_DATA | UART3_TX ENET2_RDATA02 SIM1_PORT0_PD CSI_DATA01 UART2_CTS_B SJC_JTAG_ACT ANATOP_OTG1_ID | GPIO1[24] | Application UART 2 Clear to Send output signal |
| 3rd UART | | | | | | |
| 67 | 3V3 | TXD | GPIO1_IO04 | ENET1_REF_CLK1 PWM3_OUT USB_OTG1_PWR USDHC1_RESET_B ENET2_1588_EVENT0_IN UART5_TX uart5 | GPIO1[4] | Application UART 5 Transmit Data output signal |
| 68 | 3V3 | RXD | GPIO1_IO05 | ENET2_REF_CLK2 PWM4_OUT ANATOP_OTG2_ID CSI_FIELD USDHC1_VSELECT ENET2_1588_EVENT0_OUT UART5_RX | GPIO1[5] | Application UART 5 Receive Data input signal |
| 69 | 3V3 | RTS | GPIO1_IO08 | PWM1_OUT WDOG1_WDOG_B SPDIF_OUT CSI_VSYNC USDHC2_VSELECT CCM_PMIC_RDY UART5_RTS_B | GPIO1[8] | Application UART 5 Request to Send input signal |
| 70 | 3V3 | CTS | GPIO1_IO09 | PWM2_OUT WDOG1_WDOG_ANY SPDIF_IN CSI_HSYNC USDHC2_RESET_B USDHC1_RESET_B UART5_CTS_B | GPIO1[9] | Application UART 5 Clear to Send output signal |
| 71 | GND | GND | | | | |
| KEYPAD / 1st CAN | | | | | | |
| 72 | 3V3 | KP_COL[0] | ENET2_RX_DATA1 | UART6_RX SIM1_PORT0_CLK I2C3_SDA ENET1_MDC KPP_COL04 USB_OTG1_OC | GPIO2[9] | |
| 73 | 3V3 | KP_COL[1] | ENET2_TX_DATA0 | UART7_RX SIM1_PORT0_SVEN I2C4_SDA EIM_EB_B02 KPP_COL05 | GPIO2[11] | |
| 74 | 3V3 | KP_COL[2] | ENET2_TX_EN | UART8_RX SIM2_PORT0_CLK ECSPI4_MOSI EIM_ACLK_FREERUN KPP_COL06 USB_OTG2_OC | GPIO2[13] | |
| 75 | 3V3 | KP_COL[3] | ENET2_RX_ER | UART8_RTS_B SIM2_PORT0_SVEN ECSPI4_SS0 EIM_ADDR25 KPP_COL07 WDOG1_WDOG_ANY | GPIO2[15] | |
| 76 | 3V3 | TXCAN | UART2_CTS_B | ENET1_CRIS FLEXCAN2_TX CSI_DATA08 GPT1_COMPARE2 SJC_DE_B ECSPI3_MOSI | GPIO1[22] | |
| 77 | 3V3 | KP_ROW[0] | ENET2_RX_DATA0 | UART6_TX SIM1_PORT0_TRXD I2C3_SCL | GPIO2[8] | |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|-----|------|-----------|--------------------------|---|-----------|--|
| | | | | ENET1_MDIO KPP_ROW04 USB_OTG1_PWR | | |
| 78 | 3V3 | KP_ROW[1] | ENET2_RX_EN | UART7_TX SIM1_PORT0_RST_B I2C4_SCL EIM_ADDR26 KPP_ROW05 ENET1_REF_CLK_25M | GPIO2[10] | |
| 79 | 3V3 | KP_ROW[2] | ENET2_TX_DATA1 | UART8_TX SIM2_PORT0_TRXD ECSPI4_SCL EIM_EB_B03 KPP_ROW06 USB_OTG2_PWR | GPIO2[12] | |
| 80 | 3V3 | KP_ROW[3] | ENET2_TX_CLK | UART8_CTS_B SIM2_PORT0_RST_B ECSPI4_MISO ENET2_REF_CLK2 KPP_ROW07 ANATOP_OTG2_ID | GPIO2[14] | |
| 81 | 3V3 | RXCAN | UART2_RTS_B | ENET1_COL FLEXCAN2_RX CSI_DATA09 GPT1_COMPARE3 SJC_FAIL ECSPI3_MISO | GPIO1[23] | |
| 82 | GND | GND | | | | |

SSI 1 - Serial Audio Port 1

| | | | | | | |
|----|-----|----------|-------------|---|-----------|---|
| 83 | 3V3 | SSI1_INT | JTAG_TMS | SJC_TMS GPT2_CAPTURE1 SAI2_MCLK CCM_CLKO1 CCM_WAIT SDMA_EXT_EVENT01 EPIT1_OUT | GPIO1[11] | GPIO |
| 84 | 3V3 | SSI1_RXD | JTAG_TCK | SJC_TCK GPT2_COMPARE2 SAI2_RX_DATA PWM7_OUT SIM2_POWER_FAIL | GPIO1[14] | Serial Audio Interface serial data line 1 |
| 85 | 3V3 | SSI1_TXD | JTAG_TRST_B | SJC_TRSTB GPT2_COMPARE3 SAI2_TX_DATA PWM8_OUT CAAM_RNG_OSC_OBS | GPIO1[15] | Serial Audio Interface serial data line 0 |
| 86 | 3V3 | SSI1_CLK | JTAG_TDI | SJC_TDI GPT2_COMPARE1 SAI2_TX_BCLK PWM6_OUT MQS_LEFT SIM1_POWER_FAIL | GPIO1[13] | Serial Audio Interface serial bit clock |
| 87 | 3V3 | SSI1_FS | JTAG_TDO | SJC_TDO GPT2_CAPTURE2 SAI2_TX_SYNC CCM_CLKO2 CCM_STOP MQS_RIGHT EPIT2_OUT | GPIO1[12] | Serial Audio Interface left/right clock |
| 88 | GND | GND | | | | |

SSI 2 - Serial Audio Port 2

| | | | | | | |
|----|-----|-----|--|--|--|---------------|
| 89 | | | | | | Not connected |
| 90 | | | | | | Not connected |
| 91 | | | | | | Not connected |
| 92 | | | | | | Not connected |
| 93 | | | | | | Not connected |
| 94 | GND | GND | | | | |

Secure Digital Interface 2

| | | | | | | |
|-----|--|--|--|--|--|---------------|
| 95 | | | | | | Not connected |
| 96 | | | | | | Not connected |
| 97 | | | | | | Not connected |
| 98 | | | | | | Not connected |
| 99 | | | | | | Not connected |
| 100 | | | | | | Not connected |
| 101 | | | | | | Not connected |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|------------------------------|------|-------------|--------------------------|---|-----------|--|
| 102 | GND | GND | | | | |
| CMOS Sensor Interface | | | | | | |
| 103 | 3V3 | CSI0_DAT12 | CSI_DATA00 | CSI_DATA02 USDHC2_DATA0 SIM1_PORT1_RST_B ECSPI2_SCLK EIM_AD00 SRC_INT_BOOT / UART5_TX | GPIO4[21] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 104 | 3V3 | CSI0_DAT13 | CSI_DATA01 | CSI_DATA03 USDHC2_DATA1 SIM1_PORT1_SVEN ECSPI2_SS0 EIM_AD01 SAI1_MCLK / UART5_RX | GPIO4[22] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 105 | 3V3 | CSI0_DAT14 | CSI_DATA02 | CSI_DATA04 USDHC2_DATA2 SIM1_PORT1_TRXD ECSPI2_MOSI EIM_AD02 / UART5_RTS_B SAI1_RX_SYNC | GPIO4[23] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 106 | 3V3 | CSI0_DAT15 | CSI_DATA03 | CSI_DATA05 USDHC2_DATA3 SIM2_PORT1_PD ECSPI2_MISO EIM_AD03 / UART5_CTS_B SAI1_RX_BCLK | GPIO4[24] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 107 | 3V3 | CSI0_DAT16 | CSI_DATA04 | CSI_DATA06 USDHC2_DATA4 SIM2_PORT1_CLK ECSPI1_SCLK EIM_AD04 / USDHC1_WP SAI1_TX_SYNC | GPIO4[25] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 108 | 3V3 | CSI0_DAT17 | CSI_DATA05 | CSI_DATA07 USDHC2_DATA5 SIM2_PORT1_RST_B ECSPI1_SS0 EIM_AD05 / USDHC1_CD_B SAI1_TX_BCLK | GPIO4[26] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 109 | 3V3 | CSI0_DAT18 | CSI_DATA06 | CSI_DATA08 USDHC2_DATA6 SIM2_PORT1_SVEN ECSPI1_MOSI EIM_AD06 / SAI1_RX_DATA USDHC1_RESET_B | GPIO4[27] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 110 | 3V3 | CSI0_DAT19 | CSI_DATA07 | CSI_DATA09 USDHC2_DATA7 SIM2_PORT1_TRXD ECSPI1_MISO EIM_AD07 / SAI1_TX_DATA USDHC1_VSELECT | GPIO4[28] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 111 | GND | GND | | | | |
| 112 | 3V3 | CSI0_HSYNC | CSI_HSYNC | USDHC2_CMD SIM1_PORT1_PD I2C2_SCL / EIM_LBA_B PWM8_OUT / UART6_CTS_B | GPIO4[20] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 113 | 3V3 | CSI0_VSYNC | CSI_VSYNC | USDHC2_CLK SIM1_PORT1_CLK I2C2_SDA / EIM_RW PWM7_OUT / UART6_RTS_B | GPIO4[19] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 114 | 3V3 | CSI0_PIXCLK | CSI_PIXCLK | USDHC2_WP / UART6_RX RAWNAND_CE3_B I2C1_SCL / EIM_OE SNVS_HP_VIO_5 | GPIO4[18] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 115 | 3V3 | CSI0_MCLK | CSI_MCLK | USDHC2_CD_B RAWNAND_CE2_B I2C1_SDA / EIM_CS0_B SNVS_HP_VIO_5_CTL UART6_TX | GPIO4[17] | IO supply (NVCC_CSI) powered by RN5T567 LDO4 |
| 116 | GND | GND | | | | |
| LCD Controller | | | | | | |
| 117 | 3V3 | LD0 | LCD_DATA00 | PWM1_OUT ENET1_1588_EVENT2_ I2C3_SDA SRC_BT_CFG00 SAI1_MCLK | GPIO3[5] | TX6DL standard version: LCD Data Bus |
| 118 | 3V3 | LD1 | LCD_DATA01 | PWM2_OUT ENET1_1588_EVENT2_OUT I2C3_SCL | GPIO3[6] | TX6DL standard version: LCD Data Bus |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|-----|------|----------|--------------------------|---|-----------|--|
| | | | | SRC_BT_CFG01 SAI1_TX_SYNC | | |
| 119 | 3V3 | LD2 | LCD_DATA02 | PWM3_OUT ENET1_1588_EVENT3_IN I2C4_SDA SRC_BT_CFG02 SAI1_TX_BCLK | GPIO3[7] | TX6DL standard version: LCD Data Bus |
| 120 | 3V3 | LD3 | LCD_DATA03 | PWM4_OUT ENET1_1588_EVENT3_OUT I2C4_SCL SRC_BT_CFG03 SAI1_RX_DATA | GPIO3[8] | TX6DL standard version: LCD Data Bus |
| 121 | 3V3 | LD4 | LCD_DATA04 | UART8_CTS_B ENET2_1588_EVENT2_IN SPDIF_SR_CLK SRC_BT_CFG04 SAI1_TX_DATA | GPIO3[9] | TX6DL standard version: LCD Data Bus |
| 122 | 3V3 | LD5 | LCD_DATA05 | UART8_RTS_B ENET2_1588_EVENT2_OUT SPDIF_OUT SRC_BT_CFG05 ECSP11_SS1 | GPIO3[10] | TX6DL standard version: LCD Data Bus |
| 123 | 3V3 | LD6 | LCD_DATA06 | UART7_CTS_B ENET2_1588_EVENT3_IN SPDIF_LOCK SRC_BT_CFG06 ECSP11_SS2 | GPIO3[11] | TX6DL standard version: LCD Data Bus |
| 124 | 3V3 | LD7 | LCD_DATA07 | UART7_RTS_B ENET2_1588_EVENT3_OUT SPDIF_EXT_CLK SRC_BT_CFG07 ECSP11_SS3 | GPIO3[12] | TX6DL standard version: LCD Data Bus |
| 125 | 3V3 | LD8 | LCD_DATA08 | SPDIF_IN CSI_DATA16 EIM_DATA00 SRC_BT_CFG08 FLEXCAN1_TX | GPIO3[13] | TX6DL standard version: LCD Data Bus |
| 126 | 3V3 | LD9 | LCD_DATA09 | SAI3_MCLK CSI_DATA17 EIM_DATA01 SRC_BT_CFG09 FLEXCAN1_RX | GPIO3[14] | TX6DL standard version: LCD Data Bus |
| 127 | 3V3 | LD10 | LCD_DATA10 | SAI3_RX_SYNC CSI_DATA18 EIM_DATA02 SRC_BT_CFG10 FLEXCAN2_TX | GPIO3[15] | TX6DL standard version: LCD Data Bus |
| 128 | 3V3 | LD11 | LCD_DATA11 | SAI3_RX_BCLK CSI_DATA19 EIM_DATA03 SRC_BT_CFG11 FLEXCAN2_RX | GPIO3[16] | TX6DL standard version: LCD Data Bus |
| 129 | GND | GND | | | | |
| 130 | 3V3 | LD12 | LCD_DATA12 | SAI3_TX_SYNC CSI_DATA20 EIM_DATA04 SRC_BT_CFG12 ECSP11_RDY | GPIO3[17] | TX6DL standard version: LCD Data Bus |
| 131 | 3V3 | LD13 | LCD_DATA13 | SAI3_TX_BCLK CSI_DATA21 EIM_DATA05 SRC_BT_CFG13 USDHC2_RESET_B | GPIO3[18] | TX6DL standard version: LCD Data Bus |
| 132 | 3V3 | LD14 | LCD_DATA14 | SAI3_RX_DATA CSI_DATA22 EIM_DATA06 SRC_BT_CFG14 USDHC2_DATA4 | GPIO3[19] | TX6DL standard version: LCD Data Bus |
| 133 | 3V3 | LD15 | LCD_DATA15 | SAI3_TX_DATA CSI_DATA23 EIM_DATA07 SRC_BT_CFG15 USDHC2_DATA5 | GPIO3[20] | TX6DL standard version: LCD Data Bus |
| 134 | 3V3 | LD16 | LCD_DATA16 | UART7_TX CSI_DATA01 EIM_DATA08 SRC_BT_CFG24 | GPIO3[21] | TX6DL standard version: LCD Data Bus |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|--------------------------------|------|----------|--------------------------|--|-----------|--|
| | | | | USDHC2_DATA6 | | |
| 135 | 3V3 | LD17 | LCD_DATA17 | UART7_RX CSI_DATA00 EIM_DATA09 SRC_BT_CFG25 USDHC2_DATA7 | GPIO3[22] | TX6DL standard version: LCD Data Bus |
| 136 | 3V3 | LD18 | LCD_DATA18 | PWM5_OUT CA7_MX6UL_EVENTO CSI_DATA10 EIM_DATA10 SRC_BT_CFG26 USDHC2_CMD | GPIO3[23] | TX6DL standard version: LCD Data Bus |
| 137 | 3V3 | LD19 | LCD_DATA19 | EIM_DATA11 SRC_BT_CFG27 USDHC2_CLK PWM6_OUT WDOG1_WDOG_ANY CSI_DATA11 | GPIO3[24] | TX6DL standard version: LCD Data Bus |
| 138 | 3V3 | LD20 | LCD_DATA20 | EIM_DATA12 SRC_BT_CFG28 USDHC2_DATA0 UART8_TX ECSPI1_SCLK CSI_DATA12 | GPIO3[25] | TX6DL standard version: LCD Data Bus |
| 139 | 3V3 | LD21 | LCD_DATA21 | UART8_RX ECSPI1_SS0 CSI_DATA13 EIM_DATA13 SRC_BT_CFG29 USDHC2_DATA1 | GPIO3[26] | TX6DL standard version: LCD Data Bus |
| 140 | 3V3 | LD22 | LCD_DATA22 | MQS_RIGHT ECSPI1_MOSI CSI_DATA14 EIM_DATA14 SRC_BT_CFG30 USDHC2_DATA2 | GPIO3[27] | TX6DL standard version: LCD Data Bus |
| 141 | 3V3 | LD23 | LCD_DATA23 | MQS_LEFT ECSPI1_MISO CSI_DATA15 EIM_DATA15 SRC_BT_CFG31 USDHC2_DATA3 | GPIO3[28] | TX6DL standard version: LCD Data Bus |
| 142 | GND | GND | | | | |
| 143 | 3V3 | HSYNC | LCD_HSYNC | LCDIF_RS UART4_CTS_B SAI3_TX_BCLK WDOG3_WDOG_RST_B_DEB ECSPI2_SS1 | GPIO3[2] | |
| 144 | 3V3 | VSYNC | LCD_VSYNC | LCDIF_BUSY UART4_RTS_B SAI3_RX_DATA WDOG2_WDOG_B ECSPI2_SS2 | GPIO3[3] | |
| 145 | 3V3 | OE_ACD | LCD_ENABLE | LCDIF_RD_E UART4_RX SAI3_TX_SYNC EIM_CS3_B ECSPI2_RDY | GPIO3[1] | |
| 146 | 3V3 | LSCLK | LCD_CLK | LCDIF_WR_RWN UART4_TX SAI3_MCLK EIM_CS2_B WDOG1_WDOG_RST_B_DEB | GPIO3[0] | |
| 147 | GND | GND | | | | |
| Module Specific Signals | | | | | | |
| 148 | 3V0 | | SNVS_TAMPER2 | | GPIO5[2] | |
| 149 | 3V0 | | SNVS_TAMPER3 | | GPIO5[3] | |
| 150 | 3V3 | | LCD_RESET | LCDIF_CS CA7_MX6UL_EVENTI SAI3_TX_DATA WDOG1_WDOG_ANY ECSPI2_SS3 | GPIO3[4] | |
| 151 | 3V0 | | SNVS_TAMPER4 | | GPIO5[4] | |
| 152 | 3V0 | | SNVS_TAMPER8 | | GPIO5[8] | |

| PIN | Type | Function | i.MX6 UltraLite Pad Name | Alternate functions | GPIO | Description (refer to i.MX6 UltraLite manuals for details) |
|-----|------|----------|--------------------------|---------------------|----------|--|
| 153 | 3V0 | | SNVS_TAMPER9 | | GPIO5[9] | |
| 154 | | | | Not connected | | |
| 155 | | | | Not connected | | |
| 156 | | | | Not connected | | |
| 157 | | | | Not connected | | |
| 158 | | | | Not connected | | |
| 159 | | | | Not connected | | |
| 160 | GND | GND | | | | |
| 161 | | | | Not connected | | |
| 162 | | | | Not connected | | |
| 163 | | | | Not connected | | |
| 164 | | | | Not connected | | |
| 165 | | | | Not connected | | |
| 166 | LVDS | | CCM_CLK1_P | | | General purpose differential high speed clock input/output |
| 167 | | | | Not connected | | |
| 168 | LVDS | | CCM_CLK1_N | | | General purpose differential high speed clock input/output |
| 169 | | | | Not connected | | |
| 170 | | | | Not connected | | |
| 171 | GND | GND | | | | |
| 172 | | | | Not connected | | |
| 173 | | | | Not connected | | |
| 174 | | | | Not connected | | |
| 175 | | | | Not connected | | |
| 176 | | | | Not connected | | |
| 177 | | | | Not connected | | |
| 178 | | | | Not connected | | |
| 179 | | | | Not connected | | |
| 180 | | | | Not connected | | |
| 181 | | | | Not connected | | |
| 182 | | | | Not connected | | |
| 183 | GND | GND | | | | |
| 184 | | | | Not connected | | |
| 185 | | | | Not connected | | |
| 186 | | | | Not connected | | |
| 187 | | | | Not connected | | |
| 188 | | | | Not connected | | |
| 189 | | | | Not connected | | |
| 190 | | | | Not connected | | |
| 191 | | | | Not connected | | |
| 192 | | | | Not connected | | |
| 193 | | | | Not connected | | |
| 194 | | | | Not connected | | |
| 195 | | | | Not connected | | |
| 196 | | | | Not connected | | |
| 197 | 3V3 | | | | 10K-PU | Connected to RN5T567 INTB Leave unconnected, if not used. |
| 198 | 3V3 | | GPIO1_IO07 | | | Fixed function ENET_MDC used for Ethernet PHY |
| 199 | 3V3 | | GPIO1_IO06 | | 1K-PU | Fixed function ENET_MDIO used for Ethernet PHY |
| 200 | GND | GND | | | | |

The TXUL Computer on Module contains a limited number of pins, most of which have multiple signal options. The following table lists alternate functions and instances which are already used onboard:

| Instance | i.MX6 UltraLite Pad Name | Mux Mode | Alternate Function | Description |
|----------|--------------------------|----------|--------------------|--------------------|
| ENET1 | GPIO1_IO07 | ALT0 | ENET1_MDC | |
| | GPIO1_IO06 | ALT0 | ENET1_MDIO | |
| | ENET1_RX_DATA0 | ALT0 | ENET1_RDATA00 | |
| | ENET1_RX_DATA1 | ALT0 | ENET1_RDATA01 | |
| | ENET1_RX_ER | ALT0 | ENET1_RX_ER | |
| | ENET1_TX_EN | ALT0 | ENET1_TX_EN | |
| | ENET1_TX_DATA0 | ALT0 | ENET1_TDATA00 | |
| | ENET1_TX_DATA1 | ALT0 | ENET1_TDATA01 | |
| | ENET1_RX_EN | ALT0 | ENET1_RX_EN | |
| GPIO | SNVS_TAMPER5 | ALT5 | GPIO5_IO05 | ENET1 Interrupt |
| GPIO | SNVS_TAMPER6 | ALT5 | GPIO5_IO06 | ENET1 PHY Reset |
| GPIO | SNVS_TAMPER7 | ALT5 | GPIO5_IO07 | ENET1 Power Enable |
| GPIO | SNVS_TAMPER0 | ALT5 | GPIO5_IO00 | PMIC SCL |
| GPIO | SNVS_TAMPER1 | ALT5 | GPIO5_IO01 | PMIC SDA |
| | | | | |