Intel® Xeon Phi™ Coprocessor x100 Product Family

Registers

December 2014

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Revision History

Document Number	Revision Number	Description	Revision Date
330991	1.0	Initial Release	December 2014

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1 Overview

This document provides the core, GBOX, and SBOX register information for the Intel® Xeon Phi™ Coprocessor x100 Product Family. Core registers fetch and decode instructions from four hardware thread execution contexts. The Intel® Xeon Phi™ coprocessor memory controller (GBOX) accesses external memory devices (local physical memory on the coprocessor card) to read and write data. Each memory controller has 2 channels, which together can operate two 32-bit memory channels. A Gen2 PCI Express client logic (SBOX) is the system interface to the host CPU or PCI Express switch which supports x8 and x16 configurations.

Terminology

Word/Acronym	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level
AFE	Analog Front End
APIC	Advanced Programmable Interrupt Controller
ASPM	Active State Power Management
BTM	Branch Trace Message
CSR	Control and Status Registers
DMA	Direct Memory Access
DP	Dual Processors
ECC	Error Correcting Code
EMON	Event Monitoring
GDDR	Graphics Double Data Rate
Host	This term is used synonymously with processor
I/O	1. Input/Output 2. When used as a qualifier to a transaction type, specifies that transaction targets Intel© architecture-specific I/O space. (for example, I/O read)
IIO	Integrated I/O Controller in the processor die providing I/O components
Integrated Memory Controller (IMC)	A memory controller that is integrated in the processor silicon
Intel® 64	Intel® 64 Instruction Set Architecture. The instruction set architecture and programming environment of Intel's 64-bit processors which is a superset of, and compatible with IA-32
Legacy	Functional requirements handed down from previous chipsets or PC compatibility requirements from the past
LRU	Least Recently Used. A term used in conjunction with cache allocation policy
MBOX	The request scheduler of the GBOX
MCA	Machine Check Architecture
MMIO	Memory Mapped I/O. Any memory access to PCI Express*
MTRR	Memory Type Range Register
Multi-Core Processor	A physical package that contains more than one processor core
MSR	Model Specific Register (MSR) as the name implies is model specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64 bits of the MSR in the EDX:EAX register pair. The WRMSR writes the contents of the EDX:EAX register pair into the MSR

Word/Acronym	Definition
PBOX	Physical layer that interfaces with the GDDR devices
PCU	Power Control Unit
Ring	refers to the interface between the processor core and rest of the uncore components
SKU	Stock Keeping Unit (SKU) is a subset of a processor type with specific features, electrical, power and thermal specifications. Not all features are supported on all SKUs. A SKU is based on specific use condition assumption
TDP	Thermal Design Power
Thread	A Logical Processor
Uncore	The portion of the processor comprising the IMC, IIO and related components
UP	Uni-processor

1.1 Notational Conventions

Base 16 numbers are represented by the character "h" and then followed by a string of hexadecimal digits that would represent the value of the field (for example, 12'h218). The number before the apostrophe indicates the length of the field. So for example, in this case, the field is 12 bits long. A hexadecimal digit is a character from the following set: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F.

Base 2 (binary) numbers are represented by the length of the bit, the character "b" and a string of 1s and 0s (for example, 1'b0). The "b" designation is only used in situations where confusion as to the type of the number might arise.

Base 10 numbers are represented by the length of the field in bits, the character "d", and a string of decimal digits (for example, 3'd6). The "d" designation is only used in situations where confusion as to the type of the number might arise.

1.2 Related Documents

Document Title	Document Number/Location
Intel® Xeon Phi™ Coprocessor System Software Developers Guide	http://intel.com/content/www/us/en/processors/xeon/xeon-technical-resources.html
Intel® Xeon Phi™ Coprocessor x100 Product Family Specification Update	http://intel.com/content/www/us/en/processors/xeon/xeon-technical-resources.html
Intel® Xeon Phi™ Coprocessor Instruction Set Architecture Reference Manual	https://software.intel.com/mic-developer

Document Title	Document Number/Location
Intel® 64 and IA-32 Architecture Software Developer's Manual (SDM) Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide, Part 1 Volume 3B: System Programming Guide, Part 2	 253665 253666 253667 253668 253669
ACPI Specifications	www.acpi.info
PCIe® Base 2.1 Specification	www.pcisig.com

2 Core Registers

The core fetches and decodes instructions from four hardware thread execution contexts. It supports a 32-bit and 64-bit execution environment similar to those found in the Intel64® Intel® Architecture Software Developer's Manual, along with the Intel Initial Many Core Instructions. It contains a 32KB, 8-Way set associative L1 Lcache and Dcache, and interfaces with the CRI/L2 block to request access to memory. The core can execute 2 instructions per clock cycle, one on the U-pipe, and one on the V-pipe. The V-pipe cannot execute all instruction types, and simultaneous execution is governed by pairing rules. The core does not support Intel® Streaming SIMD Extensions (Intel® SSE) or MMX™ instruction execution.

2.1 MC1_CTRL

IA32_CR MCA Control Register

MSR Address: 32'h00000404

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	core	UL1_TAG_CORR_ERR	Enables reporting of L2 Correctable Tag errors on hits
1	1'b0	core	UL1_TAG_HIT_UNCORR_ERR	Enables reporting of L2 Uncorrectable Tag errors on hits: (true hit OR eviction) AND ((tag parity error on hit way AND valid state) OR (multiple match))
2	1'b0	core	UL1_TAG_MISS_UNCORR_ERR	Enables reporting of L2 Uncorrectable Tag errors on misses : true miss AND ((any way has tag parity error AND valid state) OR (multiple match))
3	1'b0	core	UL1_DATA_UNCORR_ERR	Enables reporting of L2 Data ECC double bit uncorrectable errors
4	1'b0	core	UL1_DATA_CORR_ERR	Enables reporting of L2 Data ECC single bit correctable errors
5	1'b0	core	SNP_MISS_UNCORR_ERR	Enables reporting of coherency snoops that miss the L2
6	1'b0	core	INCLUSION_ERR	Enables reporting of memory/coherency transactions that incur inclusion errors between the L1 and L2
7	1'b0	core	ILLEGAL_ADDR_ERR	Enables reporting of illegal address errors in the L2

2.2 MC1_STAT

IA32_CR MCA Status Register

MSR Address: 32'h00000405

Range	Default	Scope	Bit Name	Bit Description
15:0	16'h0000	core	MCACOD	Specifies the machine check architecture defined error code for the machine check error condition detected. The MCACOD is the same for all Intel Architecture processors that implement MCA.
31:16	16'h0000	core	MSCOD	Specifies the model specific error code that uniquely identifies the machine check error condition detected. The model specific error codes may differ among Intel Architecture processors for the same Machine Check Error condition.
56:32	25'h0000000	core	OTHER	The functions of the bits in this field are implementation specific and are not part of the machine check architecture. Software that is intended to be portable among Intel Architecture processors should not rely on the values in this field. Unimplemented on Coprocessor.
57	1'b0	core	PCC	This bit is the Processor Contact Corrupt Flag. Indicates (when set) that the state of the processor might have been corrupted by the error condition detected and that reliable restarting of the processor may not be possible. When clear, this flag indicates that the error did not affect the processor's state. This is synonymous to the Damage bit described earlier. The name was changed to PCC for external visibility.
58	1'b0	core	ADDRV	This is the MCi Address Register valid Flag. Indicates (when set) that the MCi_ADDR register contains the address where the error occurred. When clear, this flag indicates that the MCi_ADDR register does not contain the address where the error occurred. The MCi_ADDR register should not be read if the ADDRV bit is clear.
59	1'b0	core	MISCV	This is the MCi Miscellaneous Register valid Flag. Indicates (when set) that the MCi_MISC register contains additional information regarding the error. When clear, this flag indicates that the MCi_MISC register does not contain additional information regarding the error. MCi_MISC should not be read if it is not implemented in the processor.

Range	Default	Scope	Bit Name	Bit Description
60	1'b0	core	EN	This is the Error Enabled Flag. Indicates (when set) that reporting of the machine check exception for this error was enabled by the associated flag bit of the MCi_CTL register.
61	1'b0	core	UC	This is the Error Uncorrected Flag. Indicates (when set) that the processor did not correct the error condition. When clear, this flag indicates that the processor was able to correct the error condition.
62	1'b0	core	OVER	This is the Machine Check Overflow Flag. Indicates (when set) that a machine check error occurred while the results of a previous error were still in the register bank (i.e., the VAL bit was already set in the MCi_STATUS register). The processor sets the OVER flag and software is responsible for clearing it. Enabled errors over write data for disabled errors, and uncorrected errors over write data for corrected errors. Uncorrected errors do not over write data for previous valid uncorrected errors and disabled errors do not over write data for any valid error.
63	1'b0	core	VAL	This is the MCi_STATUS Register valid Flag. Indicates (when set) that the information within the MCi_STATUS register is valid. When this flag is set, the processor follows the rules given for the OVER flag in the MCi_STATUS register when overwriting previously valid entries. The processor sets the VAL flag and software is responsible for clearing it.

2.3 MC1_ADDR

IA32_CR MCA Address Register

MSR Address: 32'h00000406

Range	Default	Scope	Bit Name	Bit Description
3:0	4'b0000	core	WAY	L2 Way
5:4	2'b00	core	THREAD	Thread ID
39:6	34'h000000000	core	ADDR	Address

2.4 MC1_MISC

IA32_CR MCA Miscellaneous Register

MSR Address: 32'h00000407

Range	Default	Scope	Bit Name	Bit Description
3:0	4'b0000	core	STATE	State of the Cacheline that encountered an error
6:4	3'b000	core	SRC	Source of the Error, 0-RSVD, 1-P54C, 2-RSVD, 3-Snoop (TD), 4-RSVD
16:7	10'h000	core	REQTYPE	L2 Arbiter request type encoding
22:17	6'h00	core	REQID	BSQ or SNPQ entry ID that received the error
31:23	9'h000	core	DSTAGENTID	NOT IMPLEMENTED: SNPQ entry Destination Agent ID that received the error

2.5 TUNE_PREFQ

Hardware PrefQ Tuning Register

MSR Address: 32'h00000337

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	core	HWP_DISABLE	Setting this bit disables/clears the hardware prefetcher. A '1 indicates that the prefetcher is disabled, a '0 indicates the prefetcher is enabled.
1	1'b0	core	CRD_PREF_DISABLE	This bit disables the hardware prefetcher from generating new prefetches as a result of code (J-unit) reads. A '1 indicates that code prefetching is disabled, a '0 indicates code prefetching is enabled.
2	1'b0	core	DRD_PREF_DISABLE	This bit disables the hardware prefetcher from generating new prefetches as a result of non-RFO data (K-unit) reads. A ' indicates that non-RFO data read prefetching is disabled, a '0 indicates that non-RFO data read prefetching is enabled.
3	1'b0	core	RFO_PREF_DISABLE	This bit disables the hardware prefetcher from generating new prefetches as a result of RFO data (K-unit) reads (i.e. stores/store intent). A '1 indicates that RFO data prefetching is disabled, a '0 indicates that RFO data prefetching is enabled.

Range	Default	Scope	Bit Name	Bit Description
4	1'b0	core	SW_PREF_ENABLE	This bit enables the hardware prefetcher to generate new prefetches as a result of SW prefetch requests (vprefetch0,vprefetche0).

2.6 APIC_BASE

IA32_CR APIC Base Physical Address MSR Register

MSR Address: 32'h0000001B

Range	Default	Scope	Bit Name	Bit Description
8	1'b0	thread	BSP	Set by microcode if this core is the bootstrap processor (BSP).
11	1'b0	thread	EN	Enable, if not set the address field is invalid
35:12	1'b1	thread	ADDR	Address

2.7 CC6_STATUS

Core C6 Status Register

MSR Address: 32'h00000342

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	core	CC6_EN	Enable CC6 Function (core power down when core is in special halt state)
1	1'b0	core	THRD_0_CC6_REQ	Thread 0 is ready (and requesting) to enter CC6 mode
2	1'b0	core	THRD_1_CC6_REQ	Thread 1 is ready (and requesting) to enter CC6 mode
3	1'b0	core	THRD_2_CC6_REQ	Thread 2 is ready (and requesting) to enter CC6 mode
4	1'b0	core	THRD_3_CC6_REQ	Thread 3 is ready (and requesting) to enter CC6 mode
5	1'b0	core	THRD_0_CC6_STATUS	Read-only bit. Thread 0 is active and the core entered CC6 mode
6	1'b0	core	THRD_1_CC6_STATUS	Read-only bit. Thread 1 is active and the core entered CC6 mode
7	1'b0	core	THRD_2_CC6_STATUS	Read-only bit. Thread 2 is active and the core entered CC6 mode
8	1'b0	core	THRD_3_CC6_STATUS	Read-only bit. Thread 3 is active and the core entered CC6 mode
9	1'b0	core	CORE_ENTERED_CC6	Read-only bit. The core entered CC6 mode

2.8 CC6_EIP

Core C6 Restart EIP Register

Range	Default	Scope	Bit Name	Bit Description
7:0	26'h0000000	core	CC6_EIP	Core C6 Restart EIP Offset

2.9 IA32_MTRRCAP

Additional information about MTRRs Default Value = 0x00000000

MSR Address: 32'hFE

Range	Default	Scope	Bit Name	Bit Description
63:11	53'h0	package	RSVD	Reserved
10	1'h0	package	WC	The write-combining (WC) memory type is supported when set. The WC type is not supported when clear
9	1'h0	package	RSVD	Reserved
8	1'h0	package	FIX	Fixed range MTRRs (IA32_MTRR_FIX64K_00000 through IA32_MTRR_FIX4K_0F8000) are supported when set. No fixed range registers are supported when clear.
7:0	8'h0	package	VCNT	Indicates the number of variable ranges implemented on the processor. The Pentium 4, Intel Xeon, and P6 family processors have eight pairs of MTRRs for setting up eight variable ranges

2.10 IA32_MTRR_DEF_TYPE

Sets the default properties of the regions of physical memory that are not encompassed by MTRRs Default Value = 0x00000000

MSR Address: 32'h2FF

Range	Default	Scope	Bit Name	Bit Description
63:12	52'h0	package	RSVD	Reserved
11	1'h0	package	Enable	MTRRs are enabled when set; all MTRRs are disabled when clear, and the UC memory type is applied to all of physical memory. When this flag is set, the FE flag can disable the fixed-range MTRRs when the flag is clear, the FE flag has no affect. When the E flag is set, the type specified in the default memory type field is used for areas of memory not already mapped by either a fixed or variable MTRR

Range	Default	Scope	Bit Name	Bit Description
10	1'h0	package	FE	Fixed-range MTRRs are enabled when set. Fixed- range MTRRs are disabled when clear. When the fixed-range MTRRs are enabled, they take priority over the variable-range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable-range MTRRs can still be used and can map the range ordinarily covered by the fixed-range MTRRs
9:8	2'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Indicates the default memory type used for those physical memory address ranges that do not have a memory type specified for them by an MTRR (see Table 10-8 of SDM v3 for the encoding of this field). The legal values for this field are 0, 1, 4, 5, and 6. All other values result in a general-protection exception (#GP) being generated. Intel recommends the use of the UC (uncached) memory type for all physical memory addresses where memory does not exist. To assign the UC type to nonexistent memory locations, it can either be specified as the default type in the Type field or be explicitly assigned with the fixed and variable MTRRs.

2.11 IA32_MTRR_PHYSBASE0

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h200

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4KB boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.12 IA32_MTRR_PHYSMASK0

Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h201

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.13 IA32_MTRR_PHYSBASE1

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h202

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.14 IA32_MTRR_PHYSMASK1

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h203

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.15 IA32_MTRR_PHYSBASE2

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h204

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.16 IA32_MTRR_PHYSMASK2

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h205

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved

Range	Default	Scope	Bit Name	Bit Description
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.17 IA32_MTRR_PHYSBASE3

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h206

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.18 IA32_MTRR_PHYSMASK3

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h207

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.

Range	Default	Scope	Bit Name	Bit Description
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.19 IA32_MTRR_PHYSBASE4

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h208

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.20 IA32_MTRR_PHYSMASK4

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h209

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.21 IA32_MTRR_PHYSBASE5

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h20A

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.22 IA32_MTRR_PHYSMASK5

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h20B

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.23 IA32_MTRR_PHYSBASE6

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h20C

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low

				end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.24 IA32_MTRR_PHYSMASK6

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h20D

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.25 IA32_MTRR_PHYSBASE7

Variable Range Base MTRR Default Value = 0x00000000

MSR Address: 32'h20E

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysBase	Base address of range. Specifies the base address of the address range. This value is extended by 12 bits at the low end to form the base address (this automatically aligns the address on a 4-KByte boundary)
11:8	4'h0	package	RSVD	Reserved
7:0	8'h0	package	Type	Memory type for range. Specifies the memory type for the range (see Table 10-8 of SDM v3 for the encoding of this field).

2.26 IA32_MTRR_PHYSMASK7

- Variable Range Mask MTRR Default Value = 0x00000000

MSR Address: 32'h20F

Range	Default	Scope	Bit Name	Bit Description
63:40	24'h0	package	RSVD	Reserved
39:12	28'h0	package	PhysMask	Sets range mask. Specifies a mask. The mask determines the range of the region being mapped, according to the following relationships: - Address_Within_Range AND PhysMask = PhysBase AND PhysMask - This value is extended by 12 bits at the low end to form the mask value. For more information: see Section 10.11.3, "Example Base and Mask Calculations" of SDM v3. - The width of the PhysMask field depends on the maximum physical address size supported by the processor.
11	1'h0	package	Valid	Enables the register pair when set; disables register pair when clear
10:0	11'h0	package	RSVD	Reserved

2.27 IA32_MTRR_FIX64K_00000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h250

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	70000-7FFFF Range type
55:48	8'h0	package	Range_6	60000-6FFFF Range type
47:40	8'h0	package	Range_5	50000-5FFFF Range type
39:32	8'h0	package	Range_4	40000-4FFFF Range type
31:24	8'h0	package	Range_3	30000-3FFFF Range type
23:16	8'h0	package	Range_2	20000-2FFFF Range type
15:8	8'h0	package	Range_1	10000-1FFFF Range type
7:0	8'h0	package	Range_0	00000-0FFFF Range type

2.28 IA32_MTRR_FIX16K_80000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h258

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	9C000-9FFFF Range type
55:48	8'h0	package	Range_6	98000-98FFF Range type

Range	Default	Scope	Bit Name	Bit Description
47:40	8'h0	package	Range_5	94000-97FFF Range type
39:32	8'h0	package	Range_4	90000-93FFF Range type
31:24	8'h0	package	Range_3	8C000-8FFFF Range type
23:16	8'h0	package	Range_2	88000-8BFFF Range type
15:8	8'h0	package	Range_1	84000-87FFF Range type
7:0	8'h0	package	Range_0	80000-83FFF Range type

2.29 IA32_MTRR_FIX16K_A0000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h259

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	BC000-BFFFF Range type
55:48	8'h0	package	Range_6	B8000-BBFFF Range type
47:40	8'h0	package	Range_5	B4000-B7FFF Range type
39:32	8'h0	package	Range_4	B0000-B3FFF Range type
31:24	8'h0	package	Range_3	AC000-AFFFF Range type
23:16	8'h0	package	Range_2	A8000-ABFFF Range type
15:8	8'h0	package	Range_1	A4000-A7FFF Range type
7:0	8'h0	package	Range_0	A0000-A3FFF Range type

2.30 IA32_MTRR_FIX4K_C0000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h268

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	C7000-C7FFF Range type
55:48	8'h0	package	Range_6	C6000-C6FFF Range type
47:40	8'h0	package	Range_5	C5000-C5FFF Range type
39:32	8'h0	package	Range_4	C4000-C4FFF Range type
31:24	8'h0	package	Range_3	C3000-C3FFF Range type
23:16	8'h0	package	Range_2	C2000-C2FFF Range type
15:8	8'h0	package	Range_1	C1000-C1FFF Range type
7:0	8'h0	package	Range_0	C0000-C0FFF Range type

2.31 IA32_MTRR_FIX4K_C8000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h269

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	CF000-CFFFF Range type
55:48	8'h0	package	Range_6	CE000-CEFFF Range type
47:40	8'h0	package	Range_5	CD000-CDFFF Range type
39:32	8'h0	package	Range_4	CC000-CCFFF Range type
31:24	8'h0	package	Range_3	CB000-CBFFF Range type
23:16	8'h0	package	Range_2	CA000-CAFFF Range type
15:8	8'h0	package	Range_1	C9000-C9FFF Range type
7:0	8'h0	package	Range_0	C8000-C8FFF Range type

2.32 IA32_MTRR_FIX4K_D0000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h26A

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	D7000-D7FFF Range type
55:48	8'h0	package	Range_6	D6000-D6FFF Range type
47:40	8'h0	package	Range_5	D5000-D5FFF Range type
39:32	8'h0	package	Range_4	D4000-D4FFF Range type
31:24	8'h0	package	Range_3	D3000-D3FFF Range type
23:16	8'h0	package	Range_2	D2000-D2FFF Range type
15:8	8'h0	package	Range_1	D1000-D1FFF Range type
7:0	8'h0	package	Range_0	D0000-D0FFF Range type

2.33 IA32_MTRR_FIX4K_D8000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h26B

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	DF000-DFFFF Range type
55:48	8'h0	package	Range_6	DE000-DEFFF Range type
47:40	8'h0	package	Range_5	DD000-DDFFF Range type

Range	Default	Scope	Bit Name	Bit Description
39:32	8'h0	package	Range_4	DC000-DCFFF Range type
31:24	8'h0	package	Range_3	DB000-DBFFF Range type
23:16	8'h0	package	Range_2	DA000-DAFFF Range type
15:8	8'h0	package	Range_1	D9000-D9FFF Range type
7:0	8'h0	package	Range_0	D8000-D8FFF Range type

2.34 IA32_MTRR_FIX4K_E0000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h26C

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	E7000-E7FFF Range type
55:48	8'h0	package	Range_6	E6000-E6FFF Range type
47:40	8'h0	package	Range_5	E5000-E5FFF Range type
39:32	8'h0	package	Range_4	E4000-E4FFF Range type
31:24	8'h0	package	Range_3	E3000-E3FFF Range type
23:16	8'h0	package	Range_2	E2000-E2FFF Range type
15:8	8'h0	package	Range_1	E1000-E1FFF Range type
7:0	8'h0	package	Range_0	E0000-E0FFF Range type

2.35 IA32_MTRR_FIX4K_E8000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h26D

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	EF000-EFFFF Range type
55:48	8'h0	package	Range_6	EE000-EEFFF Range type
47:40	8'h0	package	Range_5	ED000-EDFFF Range type
39:32	8'h0	package	Range_4	EC000-ECFFF Range type
31:24	8'h0	package	Range_3	EB000-EBFFF Range type
23:16	8'h0	package	Range_2	EA000-EAFFF Range type
15:8	8'h0	package	Range_1	E9000-E9FFF Range type
7:0	8'h0	package	Range_0	E8000-E8FFF Range type

2.36 IA32_MTRR_FIX4K_F0000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h26E

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	F7000-F7FFF Range type
55:48	8'h0	package	Range_6	F6000-F6FFF Range type
47:40	8'h0	package	Range_5	F5000-F5FFF Range type
39:32	8'h0	package	Range_4	F4000-F4FFF Range type
31:24	8'h0	package	Range_3	F3000-F3FFF Range type
23:16	8'h0	package	Range_2	F2000-F2FFF Range type
15:8	8'h0	package	Range_1	F1000-F1FFF Range type
7:0	8'h0	package	Range_0	F0000-F0FFF Range type

2.37 IA32_MTRR_FIX4K_F8000

- Fixed Range MTRR Default Value = 0x00000000

MSR Address: 32'h26F

Range	Default	Scope	Bit Name	Bit Description
63:56	8'h0	package	Range_7	FF000-FFFFF Range type
55:48	8'h0	package	Range_6	FE000-FEFFF Range type
47:40	8'h0	package	Range_5	FD000-FDFFF Range type
39:32	8'h0	package	Range_4	FC000-FCFFF Range type
31:24	8'h0	package	Range_3	FB000-FBFFF Range type
23:16	8'h0	package	Range_2	FA000-FAFFF Range type
15:8	8'h0	package	Range_1	F9000-F9FFF Range type
7:0	8'h0	package	Range_0	F8000-F8FFF Range type

2.38 PAT

PAT - Page Attributes Table

MSR Address: 32'h277

Range	Default	Scope	Bit Name	Bit Description
2:0	3'd6	thread	PA0	PAT0 entry
7:3	5'd0	thread	RSVD	Reserved
10:8	3'd4	thread	PA1	PAT1 Entry
15:11	5'd0	thread	RSVD	Reserved

Range	Default	Scope	Bit Name	Bit Description
18:16	3'd7	thread	PA2	PAT2 Entry
23:19	5'd0	thread	RSVD	Reserved
26:24	3'd0	thread	PA3	PAT3 Entry
31:27	5'd0	thread	RSVD	Reserved
34:32	3'd6	thread	PA4	PAT4 Entry
39:35	5'd0	thread	RSVD	Reserved
42:40	3'd4	thread	PA5	PAT5 Entry
47:43	5'd0	thread	RSVD	Reserved
50:48	3'd7	thread	PA6	PAT6 Entry
55:51	5'd0	thread	RSVD	Reserved
58:56	3'd0	thread	PA7	PAT7 Entry
63:59	5'd0	thread	RSVD	Reserved

2.39 PRR

Parity Reversal Register

MSR Address: 32'h00000002

Range	Default	Scope	Bit Name	Bit Description
0	1'd0	core	PARERR_STATUS	Parity Error
1	1'dx	core	PARERR_SHUTDOWN	Shutdown on Parity Error
2	1'dx	core	JCACHE_TAG	Instruction Cache Tag Parity Reversal
6:3	4'dx	core	JCACHE_DATA	Instruction Cache Data Parity Reversal
7	1'dx	core	JTLB_TAG	Instruction TLB Tag Parity Reversal
8	1'dx	core	JTLB_DATA	Instruction TLB Data Parity Reversal
9	1'dx	core	KCACHE_TAG	Data Cache Tag Parity Reversal
10	1'dx	core	KCACHE_DATA	Data Cache Data Parity Reversal
11	1'dx	core	KTLB_TAG	Data TLB Tag Parity Reversal
12	1'dx	core	KTLB_DATA	Data TLB Data Parity Reversal
13	1'dx	core	MC	Reverse CROM Parity Logic
14	1'd0	core	CRPERR	CROM Parity Error
15	1'd0	core	KTUPERR	K TLB U-pipe access Parity Error
16	1'd0	core	KTVPERR	K TLB V-pipe access Parity Error
17	1'd0	core	KCTPERR	K Cache Tag Parity Error
18	1'd0	core	KCDPERR	K Cache Data Parity Error

Range	Default	Scope	Bit Name	Bit Description
19	1'd0	core	JTTPERR	J TLB Tag Parity Error
20	1'd0	core	JTDPERR	J TLB Data Parity Error
21	1'd0	core	JCTPERR	J Cache Tag Parity Error
22	1'd0	core	JCDPERR	J Cache Data Parity Error
23	1'dx	core	PTTPRB	L2 TLB tag parity reversal bit
24	1'dx	core	PTDPRB	L2 TLB data parity reversal bit

2.40 MCGCAP

MCG_CAP Control Register - Reports Machine Check Arch capabilities

MSR Address: 32'h00000179

Range	Default	Scope	Bit Name	Bit Description
7:0	32'd0	core	COUNT	Number of MC Banks
8	8'd3	core	MCG_CTL_P	MCG_CTL register present

2.41 MCGSTAT

MCG_STATUS Control Register - State of processor after a Machine check.

MSR Address: 32'h0000017A

Range	Default	Scope	Bit Name	Bit Description
0	1'b1	thread	RIPV	Restart IP valid flag
1	1'd0	thread	EIPV	Error IP valid flag
2	1'd0	thread	MCIP	Machine check in progress flag

2.42 MCGCTL

MCG_CTL Control Register - Enables Machine Error Reporting

MSR Address: 32'h0000017B

Range	Default	Scope	Bit Name	Bit Description
0	1'd0	thread	MC0_EN	Enable MC Bank 0 Reporting
1	1'd0	thread	MC1_EN	Enable MC Bank 1 Reporting
2	1'd0	thread	MC2_EN	Enable MC Bank 2 Reporting

2.43 MC0CTRL

Machine Check 0 Control Register

MSR Address: 32'h00000400

Range	Default	Scope	Bit Name	Bit Description
0	1'd0	core	UROM_ERR_EN	UROM Error Enable
1	1'd0	core	JTLB_ERR_EN	Instruction TLB Error Enable
2	1'd0	core	KTLB_ERR_EN	Data TLB Error Enable
3	1'd0	core	JCACHE_ERR_EN	Instruction Cache Error Enable
4	1'd0	core	KCACHE_ERR_EN	Data Cache Error Enable

2.44 MC0_STAT

Machine Check 0 Status Register

MSR Address: 32'h00000401

Range	Default	Scope	Bit Name	Bit Description
15:0	1'd0	core	ERR_CODE	MCA Error Code
31:16	16'd0	core	MODEL_CODE	MCA Model Specific error code (Not implemented)
57	16'd0	core	PCC	Processor context corrupt
58	1'd0	core	ADDRV	Reserved
59	1'd0	core	MISCV	Reserved
60	1'd0	core	EN	MC Error Enabled
61	1'd0	core	UC	Un-cacheable Error
62	1'd0	core	OVER	Error Overflow
63	1'd0	core	VAL	MC0_STATUS register valid

2.45 TMEL

Time Stamp Counter Low - Lower 32 bits

MSR Address: 32'h00000010

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	core	TME_LO	Time Stamp Counter - Bits 31:0

2.46 TMEH

Time Stamp Counter Hi - Higher 32 bits

MSR Address: 32'h00000010

Range	Default	Scope	Bit Name	Bit Description
63:32	32'd0	core	TME_HI	Time Stamp Counter - Bits 63:32

2.47 PERFCNT0

Performance Event Counter 0

MSR Address: 32'h00000020

Range	Default	Scope	Bit Name	Bit Description
39:0	64'dx	thread	COUNT0	Count of Performance Event Counter 0

2.48 PERFCNT1

Performance Event Counter 1

MSR Address: 32'h00000021

Range	Default	Scope	Bit Name	Bit Description
39:0	40'd0	thread	COUNT1	Count of Performance Event Counter 1

2.49 EVSEL0

Performance Event Selection Register 0

MSR Address: 32'h00000028

Range	Default	Scope	Bit Name	Bit Description
7:0	40'd0	thread	EVENT_SEL	Event Select - H/W Event to count
15:8	8'd0	thread	UMASK	Unit Mask - Qualifies the Event to be counted
16	8'd0	thread	USR	User Mode - When set, events are counted only in User Mode (CPL123)
17	1'd0	thread	OS	Operating System Mode - When set, events are counted only in OS Mode (CPL0)
18	1'd0	thread	E	Event Edge Detect Enable
20	1'd0	thread	INT	APIC Interrupt Enable. When set exception is generated on counter overflow
21	1'd0	thread	ALL_THR	MyThr (0) / AllThr (1)

Range	Default	Scope	Bit Name	Bit Description
22	1'd0	thread	EN	Enable Counter - When set, performance counting is enabled if the corresponding bit in IA32_PERF_GLOBAL_CTRL bit is also set.
23	1'd0	thread	INV	Invert - Inverts the result of the counter-mask comparison when set, so that both greater-than and less-than comparisons can be made
31:24	1'd0	thread	CMASK	Counter Mask - When non-zero, the counter is incremented by 1 if the number When zero, counter is incremented by the number of events counted in that cycle.

2.50 EVSEL1

Performance Event Selection Register 1

MSR Address: 32'h00000029

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	thread	EVENT_SEL	Event Select - H/W Event to count
15:8	8'd0	thread	UMASK	Unit Mask - Qualifies the Event to be counted
16	8'd0	thread	USR	User Mode - When set, events are counted only in User Mode (CPL123)
17	1'd0	thread	OS	Operating System Mode - When set, events are counted only in OS Mode (CPL0)
18	1'd0	thread	E	Event Edge Detect Enable
20	1'd0	thread	INT	APIC Interrupt Enable. When set exception is generated on counter overflow
21	1'd0	thread	ALL_THR	MyThr (0) / AllThr (1)
22	1'd0	thread	EN	Enable Counter - When set, performance counting is enabled if the corresponding bit in IA32_PERF_GLOBAL_CTRL bit is also set.
23	1'd0	thread	INV	Invert - Inverts the result of the counter-mask comparison when set, so that both greater-than and less-than comparisons can be made
31:24	1'd0	thread	CMASK	Counter Mask - When non-zero, the counter is incremented by 1 if the number When zero, counter is incremented by the number of events counted in that cycle.

2.51 SPFLT_CTRL

PERF SPFLT Control

MSR Address: 32'h0000002C

Range	Default	Scope	Bit Name	Bit Description
0	8'd0	thread	CNTR0_SPFLT_EN	SPFLT is enabled for Perf Counter 0 when bit is set
1	1'd0	thread	CNTR1_SPFLT_EN	SPFLT is enabled for Perf Counter 1 when bit is set
63	1'd0	thread	USR_PREF	User Preference. Counter is enabled when bit is set and is disabled SPFLT is enabled for that counter.

2.52 OVFSTAT

Performance Counter Overflow Status

MSR Address: 32'h0000002D

Range	Default	Scope	Bit Name	Bit Description
0	1'd0	thread	PCNTR0_OVF	Perf Counter 0 overflow. Counter overflowed if the bit is set
1	1'd0	thread	PCNTR1_OVF	Perf Counter 1 overflow. Counter overflowed if the bit is set

2.53 OVFCTRL

Performance Counter Overflow Control

MSR Address: 32'h0000002E

Range	Default	Scope	Bit Name	Bit Description
0	1'd0	thread	PCNTR0_OVF_CLR	Clear overflow bit for Perf Counter 0. Set this bit to clear Perf Counter 0 overflow indication in OVFSTAT Register
1	1'd0	thread	PCNTR1_OVF_CLR	Clear overflow bit for Perf Counter 1. Set this bit to clear Perf Counter 1 overflow indication in OVFSTAT Register

2.54 PERFCTRL

Global Performance Counter Control

MSR Address: 32'h0000002F

Range	Default	Scope	Bit Name	Bit Description
0	4'b1000	thread	CNTR0_EN	Enables Perf counter 0
1	1'd0	thread	CNTR1_EN	Enables Perf counter 1

2.55 EFER

Architectural EFER Register

MSR Address: 32'hC0000080

Range	Default	Scope	Bit Name	Bit Description
0	32'hx	thread	SCE	System Call Enable Bit
8	1'dx	thread	LME	Long Mode Enable
10	1'dx	thread	LMA	Long Mode Active
11	1'dx	thread	NXE	Execute Disable Bit Enable

2.56 STAR

SYSCALL/SYSRET selectors and legacy SYSCALL target EIP

MSR Address: 32'hC0000081

Range	Default	Scope	Bit Name	Bit Description
31:0	1'dx	thread	SYSCALL_TARGET_EIP	Legacy SYSCALL target EIP
47:32	32'dx	thread	SYSCALL_CS_SS	SYSCALL CS/SS Selector
63:48	16'dx	thread	SYSRET_CS_SS	SYSRET CS/SS Selector

2.57 LSTAR

64-bit-mode SYSCALL target RIP

MSR Address: 32'hC0000082

Range	Default	Scope	Bit Name	Bit Description
63:0	16'dx	thread	SC_RIP	Target RIP

2.58 FMASK

SYSCALL flag mask

MSR Address: 32'hC0000084

Range	Default	Scope	Bit Name	Bit Description
31:0	64'dx	thread	MASK	SYSCALL flag mask

3 GBOX Registers

The Intel® Xeon Phi™ coprocessor memory controller (GBOX) accesses external memory devices (local physical memory on the coprocessor card) to read and write data. Each memory controller has 2 channels, which together can operate two 32-bit memory channels. The memory controller comprises three main units: the FBOX (interface to the ring interconnect), the MBOX (request scheduler) and the PBOX (physical layer that interfaces with the GDDR devices). The MBOX comprises two CMCs (or Channel Memory Controllers) that are completely independent from each other. The MBOX provides the connection between agents in the system and the DRAM I/O block. It is connected to the PBOX and to the FBOX. Each CMC operates independently from the other CMCs in the system.
There are 8 GBOX channels with the Base addresses listed below:

Controller name	Base Address
MMIO_GBOX0_BASE	0x08007A0000
MMIO_GBOX1_BASE	0x0800790000
MMIO_GBOX2_BASE	0x0800700000
MMIO_GBOX3_BASE	0x08006F0000
MMIO_GBOX4_BASE	0x08006D0000
MMIO_GBOX5_BASE	0x08006C0000
MMIO_GBOX6_BASE	0x08006B0000
MMIO_GBOX7_BASE	0x08006A0000

Base Address Table 1

To locate each of the following registers for a specific channel, add the specified offset to the corresponding Base address listed in the table above.

3.1 GBOX_MBOX_GDDR_MRS01_STATUS

Offset: 0x640 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
12:0	13'h0	package	MRS0	Last value of MRS0 register
25:13	13'h0	package	MRS1	Last value of MRS1 register

3.2 GBOX_MBOX_GDDR_MRS23_STATUS

Offset: 0x644 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
12:0	13'h0	package	MRS2	Last value of MRS2 register
25:13	13'h0	package	MRS3	Last value of MRS3 register

Range	Default	Scope	Bit Name	Bit Description
27:26	2'h0	package	MRS3WCKINV_EVEN	MRS3 WCKINV state to deposit (training result from EDC0,2)
29:28	2'h0	package	MRS3WCKINV_ODD	MRS3 WCKINV state to deposit (training result from EDC1,3)
30	1'b0	package	MRS3DRAMINFOVALID	A valid bit indicating DRAM_INFO and VENDOR_ID. Cleared by hardware or DRAM reset assertion
31	1'b0	package	MRS3TEMPINFOVALID	A valid bit indicating TEMP read from DRAM. Cleared by hardware or DRAM reset assertion

3.3 GBOX_MBOX_GDDR_MRS45_STATUS

Offset: 0x648 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
12:0	13'h0	package	MRS4	Last value of MRS4 register
25:13	13'h0	package	MRS5	Last value of MRS5 register

3.4 GBOX_MBOX_GDDR_MRS67_STATUS

Offset: 0x64c Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
12:0	13'h0	package	MRS6	Last value of MRS6 register
25:13	13'h0	package	MRS7	Last value of MRS7 register

3.5 GBOX_MBOX_GDDR_MRS8_N_STATUS

Offset: 0x650 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
12:0	13'h0	package	MRS8	Last value of MRS8 register
25:13	13'h0	package	MRSn	Last value of MRS n register
29:26	4'h0	package	INDEX	Index of MRS register

3.6 GBOX_MBOX_UC_COUNTER0_STATUS

Offset: 0x654 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
11:0	12'h0	package	PI	Value of PI counter
23:12	12'h0	package	REP	Value of REP counter

3.7 GBOX_MBOX_UC_COUNTER1_STATUS

Offset: 0x658 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
11:0	12'h0	package	REF_BURST	Value of REF_BURST counter
23:12	12'h0	package	TR	Value of TR counter

3.8 GBOX_MBOX_UC_COUNTER2_STATUS

Offset: 0x65c Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
11:0	12'h0	package	MISC0	Value of MISC0 counter
23:12	12'h0	package	MISC1	Value of MISC1 counter

3.9 GBOX_MBOX_UC_COUNTER3_STATUS

Offset: 0x660 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
11:0	12'h0	package	DM_REQ	Value of DM_REQ counter
23:12	12'h0	package	STEP_LIMIT	Value of STEP_LIMIT counter
31:24	8'h0	package	FRM	Value of FRM counter

3.10 GBOX_MBOX_GDDR_VENDOR_ID

Offset: 0x124 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
15:0	15'd0	package	VENDOR_ID	Rev, VENDOR_ID
31:16	8'd0	package	DRAM_INFO	DRAM_INFO; FIFO Depth, 512Mb/1Gb

3.11 GBOX_MBOX_GDDR_TEMP

Offset: 0x128 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TEMP	GDDR temperature
31:16	16'd0	package	RFU	DRAM_INFO; FIFO Depth, 512Mb/1Gb

3.12 GBOX_MBOX_MCA_CRC_ADDR

When # of CRC errors trigger MCA event, capture transaction address

Offset: 0x7c Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
25:0	1'b0	package	addr	address for transaction, which caused re-train due to CRC errors
27:26	26'd0	package	retrain_status	Encoding for RetrainStatus for MCA Event MCATrainFailAfterDMReq. Log first training fail. 2'b00 - NIL 2'b01 - Long Retraining Fail 2'b10 - M2/M3 Exit Fail 2'b11 - MemPrsv Exit Fail
31:28	2'd0	package	retrain_trsummary	Tr Summary of First Training Fail that was logged by MCA Event MCATrainFailAfterDMReq. {wrtr, rdtr, cktr, adtr}

3.13 GBOX_MBOX_MCA_CAPE_ADDR

When # of CAPE errors trigger MCA event, capture transaction address

Offset: 0xdc Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
25:0	4'd0	package	addr	address for transaction, which caused re-train due to CAPE errors

3.14 GBOX_MBOX_UNCORR_ECC_ERROR_ADDR

When Uncorrectable ECC errors trigger MCA event, capture transaction address

Offset: 0x1a4 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
25:0	26'd0	package	addr	address for transaction, which caused MCA event due to Uncorrectable ECC error

3.15 GBOX_MBOX_CORR_ECC_ERROR_ADDR

When Correctable ECC errors trigger MCA event, capture transaction address

Offset: 0x1e0 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
25:0	26'd0	package	addr	address for transaction, which caused MCA event due to Correctable ECC error

3.16 GBOX_MBOX_PWD_M1CNT_CONFIG

m1 counter configuration

Offset: 0x80 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
31:0	2'h0	package	m1cntvalue	Ideal counter value for entering m1 state

3.17 GBOX_MBOX_PWD_M2CNT_CONFIG

m2 counter configuration

Offset: 0x84 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd200	package	m2cntvalue	Ideal counter value for entering m2 state

3.18 GBOX_MBOX_PWD_M3CNT_CONFIG

m3 counter configuration

Offset: 0x88 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd400	package	m3cntvalue	Ideal counter value for entering m3 state

3.19 GBOX_PBOX_PM_CONTROL

LGIO Power Management Control

Offset: 0x4d0 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	M2DQPIOffEn	Enable DQPI ShutOff During M2
1	1'h0	package	M3DQPIOffEn	Enable DQPI ShutOff During M3
2	1'h0	package	M2WCKPIOffEn	Enable WCKPI ShutOff During M2
3	1'h0	package	M3WCKPIOffEn	Enable WCKPI ShutOff During M3
4	1'h0	package	M2DQByteDistOffEn	Enable DQByte PGClk Distribution ShutOff During M2
5	1'h0	package	M3DQByteDistOffEn	Enable DQByte PGClk Distribution ShutOff During M3
6	1'h0	package	M2CmdAdrPIOffEn	Enable CmdAdr PI ShutOff During M2
7	1'h0	package	M3CmdAdrPIOffEn	Enable CmdAdr PI ShutOff During M3
8	1'h0	package	M2CmdAdrDistOffEn	Enable CmdAdr PGClk Distribution ShutOff During M2
9	1'h0	package	M3CmdAdrDistOffEn	Enable CmdAdr PGClk Distribution ShutOff During M3
10	1'h0	package	M2PGClkGateEn	Enable PGClk Gating at PLL output during M2
11	1'h0	package	M3PGClkGateEn	Enable PGClk Gating at PLL output during M3
12	1'h0	package	M2DQDrvOffEn	Enable DQ Drive ShutOff during M2
13	1'h0	package	M3DQDrvOffEn	Enable DQ Drive ShutOff during M3

Range	Default	Scope	Bit Name	Bit Description
14	1'h0	package	M2DQRXOffEn	Enable DQ Sampler and AFE ShutOff during M2
15	1'h0	package	M3DQRXOffEn	Enable DQ Sampler and AFE ShutOff during M3
16	1'h0	package	M2WCKDrvOffEn	Enable WCK Drive ShutOff during M2
17	1'h0	package	M3WCKDrvOffEn	Enable WCK Drive ShutOff during M3
18	1'h0	package	M2CmdAdrDrvOffEn	Enable CmdAdr Driver ShutOff during M2
19	1'h0	package	M3CmdAdrDrvOffEn	Enable CmdAdr Drive ShutOff during M3
20	1'h0	package	M2HCKDrvOffEn	Enable HCK Drive ShutOff during M2
21	1'h0	package	M3HCKDrvOffEn	Enable HCK Drive ShutOff during M3
22	1'h0	package	DataTrClkGateEn	Enable Clock gating to Module lgpregpidatas
23	1'b0	package	EDCTrClkGateEn	Enable Clock gating to Module lgpregpiredcs
24	1'b0	package	AdrTrClkGateEn	Enable Clock gating to Module lgpregpiads
25	1'b0	package	WCKTrClkGateEn	Enable Clock gating to Module lgpregpicks
26	1'b0	package	PICmpsTrClkGateEn	Enable Clock gating to Module lgpregcmps
27	1'b0	package	OnDemandFifoGatingEn	Enable Fifo Clock gating during M0
28	1'b0	package	M1ClkGatingEn	Enable Coarse Grain Clock Gating during M1
29	1'b0	package	M2M3ClkGatingEn	Enable Coarse Graing Clock Gating during M2 and M3
30	1'b0	package	RSVD	Reserved
31	1'b0	package	HckCmdDCCFreezeEn	Stop DCC calibration for Hck and Cmd after wait time

3.20 GBOX_PBOX_PM_CONTROL

LGIO Power Management Control

Offset: 0x3d0 Base Address: Please see *Base Address Table 1*

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	M2DQPIOffEn	Enable DQPI ShutOff During M2
1	1'h0	package	M3DQPIOffEn	Enable DQPI ShutOff During M3
2	1'h0	package	M2WCKPIOffEn	Enable WCKPI ShutOff During M2
3	1'h0	package	M3WCKPIOffEn	Enable WCKPI ShutOff During M3

Range	Default	Scope	Bit Name	Bit Description
4	1'h0	package	M2DQByteDistOffEn	Enable DQByte PGClk Distribution ShutOff During M2
5	1'h0	package	M3DQByteDistOffEn	Enable DQByte PGClk Distribution ShutOff During M3
6	1'h0	package	M2CmdAdrPIOffEn	Enable CmdAdr PI ShutOff During M2
7	1'h0	package	M3CmdAdrPIOffEn	Enable CmdAdr PI ShutOff During M3
8	1'h0	package	M2CmdAdrDistOffEn	Enable CmdAdr PGClk Distribution ShutOff During M2
9	1'h0	package	M3CmdAdrDistOffEn	Enable CmdAdr PGClk Distribution ShutOff During M3
10	1'h0	package	M2PGClkGateEn	Enable PGClk Gating at PLL output during M2
11	1'h0	package	M3PGClkGateEn	Enable PGClk Gating at PLL output during M3
12	1'h0	package	M2DQDrvOffEn	Enable DQ Drive ShutOff during M2
13	1'h0	package	M3DQDrvOffEn	Enable DQ Drive ShutOff during M3
14	1'h0	package	M2DQRXOffEn	Enable DQ Sampler and AFE ShutOff during M2
15	1'h0	package	M3DQRXOffEn	Enable DQ Sampler and AFE ShutOff during M3
16	1'h0	package	M2WCKDrvOffEn	Enable WCK Drive ShutOff during M2
17	1'h0	package	M3WCKDrvOffEn	Enable WCK Drive ShutOff during M3
18	1'h0	package	M2CmdAdrDrvOffEn	Enable CmdAdr Driver ShutOff during M2
19	1'h0	package	M3CmdAdrDrvOffEn	Enable CmdAdr Drive ShutOff during M3
20	1'h0	package	M2HCKDrvOffEn	Enable HCK Drive ShutOff during M2
21	1'h0	package	M3HCKDrvOffEn	Enable HCK Drive ShutOff during M3
22	1'h0	package	DataTrClkGateEn	Enable Clock gating to Module lgpregpidatas
23	1'b0	package	EDCTrClkGateEn	Enable Clock gating to Module lgpregpiredcs
24	1'b0	package	AdrTrClkGateEn	Enable Clock gating to Module lgpregpiads
25	1'b0	package	WCKTrClkGateEn	Enable Clock gating to Module lgpregpicks
26	1'b0	package	PICmpsTrClkGateEn	Enable Clock gating to Module lgpregcmps
27	1'b0	package	OnDemandFifoGatingEn	Enable Fifo Clock gating during M0
28	1'b0	package	M1ClkGatingEn	Enable Coarse Grain Clock Gating during M1
29	1'b0	package	M2M3ClkGatingEn	Enable Coarse Graing Clock Gating during M2 and M3
30	1'b0	package	RSVD	Reserved
31	1'b0	package	HckCmdDCCFreezeEn	Stop DCC calibration for Hck and Cmd after wait time

4 SBOX Registers

Gen2 PCI Express* client logic (SBOX) is the system interface to the host CPU or PCI Express switch which supports x8 and x16 configurations.

Note: PCI Express* client logic comprises of DMA engine and limited power management capabilities

4.1 DSTAT

Device Status Register

Offset: 0x4014 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
1:0	2'h0	package	SUPPL_CONN1	The 2-bit field is the inverted value of the xxconn1_sns0_n and xxconn1_sns1_n pins captured at the rising edge of PERST. These pins are used to calculate available power for GrpB
3:2	2'h0	package	SUPPL_CONN2	The 2-bit field is the inverted value of the xxconn2_sns0_n and xxconn2_sns1_n pins captured at the rising edge of PERST
5:4	2'h0	package	SUPPL_CONN3	The 2-bit field is the inverted value of the xxconn3_sns0_n and xxconn3_sns1_n pins captured at the rising edge of PERST
6	1'h0	package	DeviceReady	This bit is set by the device when the complete LRB system has come out of HW reset process. The host driver should poll this bit and should start normal flow when this bit is sampled set.
8	1'h0	package	Reserved	Reserved
9	1'h0	package	Reserved	Reserved

4.2 C3WakeUp_Timer

C3 WakeUp Timer Control for autoC3

Offset: 0x4120 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'hFFFF	package	C3WakeTime	This 16-bit field represents the load value, in ~31.25us granularity, of the C3WakeUp timer. This value must be non-zero, and the enable bit must be set to 1 for the timer to begin counting down. Values of 0xFFFF will essentially disable the timer along with C3WakeTimer_En.
17	1'b0	package	C3Wake_TimeOut	When this read-only bit is set, it means that the timer has counted down and reached 0. Once

				this bit is set, it can only be cleared by reloading and restarting the timer. While this bit is set, coprocessor cannot enter C3. If PcuControl.PreventAutoC3 bit is set, for example Deeper C3, this field will never assert.

4.3 L1_Entry_Timer

L1 Entry Timer

Offset: 0x4124 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
5:0	6'h3F	package	L1_TIMER	This register contains the start value for the SCLK-based timer which blocks L1 entry. When programmed to 0h, the timer is disabled and there is no delay for L1 entry. A value of 3Fh, the timer is frozen and prevents entry into L1 indefinitely. A value of 0001h indicates a delay of ~2µs and a value of eEh indicates ~124µs. A value of (n+1) programmed to this register will give you a minimum delay of 2n µs before L1. So, a programmed value of 5 will give a delay of 8µs, 6 will give a delay of 10µs and so on.

4.4 C3_Timers

C3 Entry and Exit Timers

Offset: 0x4128 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'hFF	package	C3_ENTRY_TIMER	Programmable 8-bit timer with a ~1µs granularity which blocks C3 entry. Value of 0=~1µs
18:16	3'h3	package	C3_EXIT_TIMER	Programmable 8-bit timer with a 4~µs granularity which blocks C3 entry. Value of 0=~4µs

4.5 uOS_PCUCONTROL

Coprocessor OS PCU Control CSR

Offset: 0x412C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	C3WakeTimer_En	This bit, when set, loads the C3WakeUp timer with the 16-bit C3WakeTime field and enables the C3WakeUp timer to begin decrementing, while in AutoC3. Clearing the disables the timer. HW will automatically clear this bit when the timer reaches zero, PreventAutoC3Exit is set or if AutoC3 exits. Writing a value of 0xFFFF to the C3WakeTimer will also clear this bit.

Range	Default	Scope	Bit Name	Bit Description
1	1'b0	package	EnableMclkPllShutdown	This bit is set by Host OS to allow disabling of MCLK PLL to enter C3-state. It is cleared by the Host OS to prevent the MCLK PLL from being shut down by the PCU. MCLK PLL will only be disabled if this bit is set AND all internal idle requirements have been met. 0=Disable MCLK Shutdown, 1-Allow MCLK Shutdown. For PkgC6, this should be cleared when ready to cause the autoC3 exit to start the GrpBReset. (bit is also in PCUCONTROL CSR)
2	1'b0	package	SPI_CLK_DISABLE	Clock gate: This bit shuts down the SPI Clock output to Flash component. 1=SPI Flash Clock Off

4.6 GboxPMControl

GBOX PM Control

Offset: 0x413C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	RSVD	Reserved
1	1'b0	package	In_PkgC6	When set, this bit is an indicator to all GBOXes that the system has entered Pkg-C6 state. Used to help GOBX State machines know to ignore inputs from core-power.
2	1'b0	package	Gbox_InM3	When this register bit is 1, all GBOXes in system are in M3.

4.7 GPIO_Input_Status

GPIO Input Status

Offset: 0x4140 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'b0	package	GPIO_Input	This read-only bit represents the inverted value received on the input of GPIO[3:0] pin. A value of 0 means the input is high. A value of 1 means the input is low.

4.8 GPIO_Output_Control

GPIO Output Control

Offset: 0x4144 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	GPIO_OE0	This register bit controls the inverted output value which is driven on the GPIO[3:0] pin. 0=Output will be driven high. 1=Output will be driven low. The associated output-enable bit must also be set to 1 to actually drive the value out on the pin.
3:1	3'b0	package	GPIO_OE	This register bit controls the inverted output value which is driven on the GPIO[3:0] pin. 0=Output will be driven high. 1=Output will be driven low. The associated output-enable bit must also be set to 1 to actually drive the value out on the pin.
16	1'b0	package	GPIO_Output0	This register bit controls the inverted output value which is driven on the GPIO[3:0] pin. 0=output will be driven high. 1=Output will be driven low. The associated output-enable bit must also be set to 1 to actually drive the value of the pin.
19:17	3'b0	package	GPIO_Output	This register bit controls the inverted output value which is driven on the GPIO[3:0] pin. 0=output will be driven high. 1=Output will be driven low. The associated output-enable bit must also be set to 1 to actually drive the value of the pin.

4.9 EMON_Control

EMON Control Register

Offset: 0x4160 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	EnableMonitor	Enable for EMON Counter
1	1'b0	package	Counter0Overflow	EMON Counter 0 Overflow Indicator, resetting the counter will clear this bit
2	1'b0	package	Counter0PulseLevelSelect	Selects Pulse or Level events for counting
3	1'b0	package	Counter0Reset	Counter 0 Reset Control. 1=Reset
4	1'b0	package	Counter0OverflowInt	Enabled Interrupt on Overflow of Counter 0
10:5	6'b0	package	Counter0EventSelect	Event Selection Field

4.10 EMON_Counter0

EMON Counter 0

Offset: 0x4164 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'h0	package	emon_counter0	EMON counter 0

4.11 MSI_VECTOR [0:15]

MSI(-X) Vector Assignment Register 0-15 - Each of these registers assigns Interrupt sources from the System Interrupt Status register to one of the 16 possible MSI(-X) Vectors. The bits set in a given register define the collection of Interrupt sources (from System Interrupt Status register) that are assigned to a particular Interrupt Vector. Register 0 assigns Interrupt sources to Vector 0, Register 1 assigns Interrupt sources to Vector 1, and so on. NOTE: SW must ensure that no interrupts are enabled (in System Interrupt Disable) before modifying the value of any MSI(-X) Vector Assignment register, otherwise the behavior is undefined. NOTE: SW shall be responsible for assigning each interrupt source to a unique Vector, or otherwise must handle multiple interrupts for a given source. NOTE: SW must ensure that interrupts sharing the same vector have the corresponding bits disabled System Interrupt Status Auto-clear register, otherwise the behavior is undefined.

Offset: 0x9044 to 0x9080 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	TCU_DOORBELL	TCU Doorbell 3:0 Interrupt Status Auto Clear
4	1'b0	package	RSVD	Reserved
15:8	1'b0	package	DMA	DMA Channels 7:0 Interrupt Status Auto Clear
25:24	1'b0	package	DBOXDONE	DBOX Done 1:0 Interrupt Status Auto Clear
26	1'b0	package	DBOXERR	DBOX Err Interrupt Status Auto Clear
30	1'b0	package	SBOXERR	SBOX Error Interrupt Status Auto Clear
31	1'b0	package	SPIDONE	SPI Done Interrupt Status Auto Clear

4.12 DCAR_0

DMA Channel Attributes Register

Offset: 0xA000 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.

Range	Default	Scope	Bit Name	Bit Description
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	RSVD

4.13 DHPR_0

Descriptor Head Pointer Register

Offset: 0xA004 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.14 DTPR_0

Descriptor Tail Pointer Register

Offset: 0xA008 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.15 DAUX_LO_0

DMA Auxiliary Register 0

Offset: 0xA00C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATALO	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.16 DAUX_HI_0

DMA Auxiliary Register 0

Offset: 0xA010 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.17 DRAR_LO_0

Descriptor Ring Attributes Register

Offset: 0xA014 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.18 DRAR_HI_0

Descriptor Ring Attributes Register

Offset: 0xA018 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / descriptor) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.19 DITR_0

DMA Interrupt Timer Register

Offset: 0xA01C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.20 DMA_DSTAT_0

DMA Channel Status Register

Offset: 0xA020 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.

Range	Default	Scope	Bit Name	Bit Description
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.21 DSTATWB_LO_0

DMA Tail Pointer Write Back Register Lo

Offset: 0xA024 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.22 DSTATWB_HI_0

DMA Tail Pointer Write Back Register

Offset: 0xA028 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.23 DCHERR_0

DMA Channel Error Register

Offset: 0xA02C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.

Range	Default	Scope	Bit Name	Bit Description
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.24 DCHERRMSK_0

DMA Channel Error Register

Offset: 0xA030 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'b0	package	RSVD	Reserved

Range	Default	Scope	Bit Name	Bit Description
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.25 DCAR_1

DMA Channel Attributes Register

Offset: 0xA040 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	Reserved

4.26 DHPR_1

Descriptor Head Pointer Register

Offset: 0xA044 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.27 DTPR_1

Descriptor Tail Pointer Register

Offset: 0xA048 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.28 DAUX_LO_1

DMA Auxiliary Register 0

Offset: 0xA04C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATALO	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.29 DAUX_HI_1

DMA Auxiliary Register 0

Offset: 0xA050 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.30 DRAR_LO_1

Descriptor Ring Attributes Register

Offset: 0xA054 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.31 DRAR_HI_1

Descriptor Ring Attributes Register

Offset: 0xA058 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / desc) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.32 DITR_1

DMA Interrupt Timer Register

Offset: 0xA05C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.33 DMA_DSTAT_1

DMA Channel Status Register

Offset: 0xA060 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.34 DSTATWB_LO_1

DMA Tail Pointer Write Back Register Lo

Offset: 0xA064 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.35 DSTATWB_HI_1

DMA Tail Pointer Write Back Register

Offset: 0xA068 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.36 DCHERR_1

DMA Channel Error Register

Offset: 0xA06C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.37 DCHERRMSK_1

DMA Channel Error Register

Offset: 0xA070 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.38 DCAR_2

DMA Channel Attributes Register

Offset: 0xA080 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System

Range	Default	Scope	Bit Name	Bit Description
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	Reserved

4.39 DHPR_2

Descriptor Head Pointer Register

Offset: 0xA084 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.40 DTPR_2

Descriptor Tail Pointer Register

Offset: 0xA088 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.41 DAUX_LO_2

DMA Auxiliary Register 0

Offset: 0xA08C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.42 DAUX_HI_2

DMA Auxiliary Register 0

Offset: 0xA090 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.43 DRAR_LO_2

Descriptor Ring Attributes Register

Offset: 0xA094 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeroes to align the base to a cacheline.

4.44 DRAR_HI_2

Descriptor Ring Attributes Register

Offset: 0xA098 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16GB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / desc) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.45 DITR_2

DMA Interrupt Timer Register

Offset: 0xA09C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.46 DMA_DSTAT_2

DMA Channel Status Register

Offset: 0xA0A0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.

Range	Default	Scope	Bit Name	Bit Description
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.47 DSTATWB_LO_2

DMA Tail Pointer Write Back Register Lo

Offset: 0xA0A4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.48 DSTATWB_HI_2

DMA Tail Pointer Write Back Register

Offset: 0xA0A8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.49 DCHERR_2

DMA Channel Error Register

Offset: 0xA0AC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.

Range	Default	Scope	Bit Name	Bit Description
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.50 DCHERRMSK_2

DMA Channel Error Register

Offset: 0xA0B0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1’b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved

Range	Default	Scope	Bit Name	Bit Description
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.51 DCAR_3

DMA Channel Attributes Register

Offset: 0xA0C0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.

Range	Default	Scope	Bit Name	Bit Description
30	1'b0	package	RSVD	Reserved

4.52 DHPR_3

Descriptor Head Pointer Register

Offset: 0xA0C4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.53 DTPR_3

Descriptor Tail Pointer Register

Offset: 0xA0C8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.54 DAUX_LO_3

DMA Auxiliary Register 0

Offset: 0xA0CC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATALO	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.55 DAUX_HI_3

DMA Auxiliary Register 0

Offset: 0xA0D0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.56 DRAR_LO_3

Descriptor Ring Attributes Register

Offset: 0xA0D4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.57 DRAR_HI_3

Descriptor Ring Attributes Register

Offset: 0xA0D8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / descriptor) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.58 DITR_3

DMA Interrupt Timer Register

Offset: 0xA0DC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.59 DMA_DSTAT_3

DMA Channel Status Register

Offset: 0xA0E0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.60 DSTATWB_LO_3

DMA Tail Pointer Write Back Register Lo

Offset: 0xA0E4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.61 DSTATWB_HI_3

DMA Tail Pointer Write Back Register

Offset: 0xA0E8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.62 DCHERR_3

DMA Channel Error Register

Offset: 0xA0EC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.63 DCHERRMSK_3

DMA Channel Error Register

Offset: 0xA0F0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'b0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.64 DCAR_4

DMA Channel Attributes Register

Offset: 0xA100 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System

Range	Default	Scope	Bit Name	Bit Description
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	Reserved

4.65 DHPR_4

Descriptor Head Pointer Register

Offset: 0xA104 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.66 DTPR_4

Descriptor Tail Pointer Register

Offset: 0xA108 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.67 DAUX_LO_4

DMA Auxiliary Register 0

Offset: 0xA10C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATALO	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.68 DAUX_HI_4

DMA Auxiliary Register 0

Offset: 0xA110 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.69 DRAR_LO_4

Descriptor Ring Attributes Register

Offset: 0xA114 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.70 DRAR_HI_4

Descriptor Ring Attributes Register

Offset: 0xA118 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / descriptor) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.71 DITR_4

DMA Interrupt Timer Register

Offset: 0xA11C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.72 DMA_DSTAT_4

DMA Channel Status Register

Offset: 0xA120 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively

				processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.73 DSTATWB_LO_4

DMA Tail Pointer Write Back Register Lo

Offset: 0xA124 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.74 DSTATWB_HI_4

DMA Tail Pointer Write Back Register

Offset: 0xA128 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.75 DCHERR_4

DMA Channel Error Register

Offset: 0xA12C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.

Range	Default	Scope	Bit Name	Bit Description
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.76 DCHERRMSK_4

DMA Channel Error Register

Offset: 0xA130 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.

Range	Default	Scope	Bit Name	Bit Description
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.77 DCAR_5

DMA Channel Attributes Register

Offset: 0xA140 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	Reserved

4.78 DHPR_5

Descriptor Head Pointer Register

Offset: 0xA144 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.79 DTPR_5

Descriptor Tail Pointer Register

Offset: 0xA148 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.80 DAUX_LO_5

DMA Auxiliary Register 0

Offset: 0xA14C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.81 DAUX_HI_5

DMA Auxiliary Register 0

Offset: 0xA150 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.82 DRAR_LO_5

Descriptor Ring Attributes Register

Offset: 0xA154 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.83 DRAR_HI_5

Descriptor Ring Attributes Register

Offset: 0xA158 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / descriptor) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.84 DITR_5

DMA Interrupt Timer Register

Offset: 0xA15C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.85 DMA_DSTAT_5

DMA Channel Status Register

Offset: 0xA160 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.86 DSTATWB_LO_5

DMA Tail Pointer Write Back Register Lo

Offset: 0xA164 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.87 DSTATWB_HI_5

DMA Tail Pointer Write Back Register

Offset: 0xA168 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.88 DCHERR_5

DMA Channel Error Register

Offset: 0xA16C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.89 DCHERRMSK_5

DMA Channel Error Register

Offset: 0xA170 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.

Range	Default	Scope	Bit Name	Bit Description
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.90 DCAR_6

DMA Channel Attributes Register

Offset: 0xA180 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.

Range	Default	Scope	Bit Name	Bit Description
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	Reserved

4.91 DHPR_6

Descriptor Head Pointer Register

Offset: 0xA184 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that software uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.92 DTPR_6

Descriptor Tail Pointer Register

Offset: 0xA188 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.93 DAUX_LO_6

DMA Auxiliary Register 0

Offset: 0xA18C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATALO	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.94 DAUX_HI_6

DMA Auxiliary Register 0

Offset: 0xA190 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.95 DRAR_LO_6

Descriptor Ring Attributes Register

Offset: 0xA194 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.96 DRAR_HI_6

Descriptor Ring Attributes Register

Offset: 0xA198 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / descriptor) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.97 DITR_6

DMA Interrupt Timer Register

Offset: 0xA19C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.98 DMA_DSTAT_6

DMA Channel Status Register

Offset: 0xA1A0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.99 DSTATWB_LO_6

DMA Tail Pointer Write Back Register Lo

Offset: 0xA1A4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.100 DSTATWB_HI_6

DMA Tail Pointer Write Back Register

Offset: 0xA1A8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.101 DCHERR_6

DMA Channel Error Register

Offset: 0xA1AC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.102 DCHERRMSK_6

DMA Channel Error Register

Offset: 0xA1B0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.103 DCAR_7

DMA Channel Attributes Register

Offset: 0xA1C0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
17	1'b0	package	TWB	Tail-Pointer Write Back - When set, this bit enable Tail Pointer Write Back to the memory location identified in the DTPWBR register.
24	1'b0	package	IM0	Interrupt Mask0 - This masks APIC interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
25	1'b0	package	IM1	Interrupt Mask1 - This masks MSI-X interrupts. A value of 1 disable interrupts to the Interrupt Sub-System
26	1'b0	package	IS0	Interrupt status - Applicable only when the DMA channel interrupts are destined to LRB. This bit is of type write-1-to-clear. That is when 1 is written by coprocessor OS, it gets cleared. When 0 is written, the current value does not change. It is set by DMA channel when an interrupt even
27	1'b0	package	IT	Interrupt Throttle - The sending of Interrupt Opcode + Data from the Interrupt Descriptor, will be throttled. The DMA Channel will wait until the current interrupt message is retrieved by S/W before sending the next one.
28	1'b0	package	TPA	Tail Pointer Adjust - When set, in conjunction with the Q bit, the DMA will load the Tail Pointer with the value contained in the DAR, and resume operation. Setting this bit without the PS has no effect on operation.
29	1'b0	package	Q	Quiesce - When set, the DMA Channel will begin to halt operation by completing all outstanding data and descriptor requests. Once data movement has ceased, the Q bit in the DSTAT register will be set to indicate the Quiesce state has been entered. The pause is released by setting this bit to a zero, or automatically when the TPA bit is set.
30	1'b0	package	RSVD	Reserved

4.104 DHPR_7

Descriptor Head Pointer Register

Offset: 0xA1C4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HPI	Head Pointer Index - This is the pointer to the descriptor ring that s/w uses to write descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.105 DTPR_7

Descriptor Tail Pointer Register

Offset: 0xA1C8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	TPI	Tail Pointer Index - This is the pointer used by the DMA Channel to read descriptors. This is not an address, but rather a pointer (in descriptors) relative to the base of the descriptor ring.

4.106 DAUX_LO_7

DMA Auxiliary Register 0

Offset: 0xA1CC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	Low-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.107 DAUX_HI_7

DMA Auxiliary Register 0

Offset: 0xA1D0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	AUXDATAHI	High-Order Auxiliary Data -- This register is typically used in conjunction with the programming of other register such that its content is context specific.

4.108 DRAR_LO_7

Descriptor Ring Attributes Register

Offset: 0xA1D4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	BA	Low-Order 32 bits of the Base Address into the descriptor ring. The last 6 bits are all zeros to align the base to a cacheline.

4.109 DRAR_HI_7

Descriptor Ring Attributes Register

Offset: 0xA1D8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'd0	package	BA	High-Order bits of the Base Address into the descriptor ring. BA[3:2] = PA[35:34] if SYS=0, else 'Reserved'. BA[1:0] = PA[33:32]. NOTE: System Memory address "pages" are 16 GiB each.
20:4	17'd0	package	SZ	Descriptor Ring Size - identifies the size of the descriptor ring descriptors up 128K descriptors. The size is in multiples of 4 descriptors (16B / desc) to keep the size on a cacheline boundary.
25:21	5'd0	package	PAGENO	System memory page
26	1'b0	package	SYS	Base address lives in system memory when set; otherwise base address lives in local GDDR memory

4.110 DITR_7

DMA Interrupt Timer Register

Offset: 0xA1DC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
15:0	16'd0	package	TIMER_VALUE	Timer Value. This is an unsigned value, that when set to a non-zero value, will stall the issuing of an interrupt back to the Host when the data transfer was to a remote Coprocessor. This is used to circumvent a race condition where interrupt could arrive back to the Host before the data is received on the remote Coprocessor.

4.111 DMA_DSTAT_7

DMA Channel Status Register

Offset: 0xA1E0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
16:0	17'd0	package	HW_Cmp_Cnt	Tail Pointer Index captured just before halting due to affiliated error.
28	1'b0	package	Q	Channel Quiesced - This bit is set when the DMA Channel finally enters a quiescent State in response to the to the DCAR.Q bit being set.

Range	Default	Scope	Bit Name	Bit Description
29	1'b0	package	A	Channel Active- This bit is set when the DMA is in an Active State, which is defined as the DMA is actively processing descriptors or is in an idle and awaiting all outstanding transaction associated with previous descriptor, to complete.
30	1'b0	package	RSVD	Reserved
31	1'b0	package	ERR	DMA Channel has encountered an error. Bit is set when an error is logged in DCHERR and not masked in DCHERRMSK.

4.112 DSTATWB_LO_7

DMA Tail Pointer Write Back Register Lo

Offset: 0xA1E4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	ADDR	Low-Order 32 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.113 DSTATWB_HI_7

DMA Tail Pointer Write Back Register

Offset: 0xA1E8 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
7:0	8'd0	package	ADDR	High-Order 8 bits of the 40-bit Coprocessor address that points to either System Memory or GDDR Memory to where the Tail Pointer should be written back.

4.114 DCHERR_7

DMA Channel Error Register

Offset: 0xA1EC Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR	Set when the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR	Set when the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR	Set when the current descriptor has an illegal destination address.

Range	Default	Scope	Bit Name	Bit Description
3	1'b0	package	SYS_MEM_TRANSFER_ERR	Set when the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR	Set when the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR	Set when SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR	Set when SW attempts to write a Head Pointer value larger than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR	Set when SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.115 DCHERRMSK_7

DMA Channel Error Register

Offset: 0xA1F0 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	DESCR_ADDR_ERR_MASK	Mask reporting the current descriptor is located at an illegal address.
1	1'b0	package	SRC_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal source address.
2	1'b0	package	DEST_ADDR_ERR_MASK	Mask reporting the current descriptor has an illegal destination address.
3	1'b0	package	SYS_MEM_TRANSFER_ERR_MASK	Mask reporting the current descriptor has both a source and destination address that maps to system memory.
4	1'b0	package	DESCR_CONTROL_ERR_MASK	Mask reporting the current descriptor contains an illegal or unsupported control field value not covered be a more specific error.
28:5	24'd0	package	RSVD	Reserved
29	1'b0	package	DSTATWB_ADDR_ERR_MASK	Mask reporting SW writes an illegal address value to DSTATWB.
30	1'b0	package	HEAD_PTR_SIZE_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value larger

				than allowed by the size of the Descriptor Ring.
31	1'b0	package	HEAD_PTR_OVERRUN_ERR_MASK	Mask reporting SW attempts to write a Head Pointer value that would overrun the Tail Pointer.

4.116 DMA_REQUEST_SIZE

DMA Request control

Offset: 0xA200 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
2:0	3'd4	package	REQ_SIZE	DMA Request Size in Cachelines

4.117 DCR

DMA Configuration Register

Offset: 0xA280 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
0	1'b0	package	CO0	DMA Channel 0 Owner
1	1'b0	package	CE0	DMA Channel 0 Enable
2	1'b0	package	CO1	DMA Channel 1 Owner
3	1'b0	package	CE1	DMA Channel 1 Enable
4	1'b0	package	CO2	DMA Channel 2 Owner
5	1'b0	package	CE2	DMA Channel 2 Enable
6	1'b0	package	CO3	DMA Channel 3 Owner
7	1'b0	package	CE3	DMA Channel 3 Enable
8	1'b0	package	CO4	DMA Channel 4 Owner
9	1'b0	package	CE4	DMA Channel 4 Enable
10	1'b0	package	CO5	DMA Channel 5 Owner
11	1'b0	package	CE5	DMA Channel 5 Enable
12	1'b0	package	CO6	DMA Channel 6 Owner
13	1'b0	package	CE6	DMA Channel 6 Enable
14	1'b0	package	CO7	DMA Channel 7 Owner
15	1'b0	package	CE7	DMA Channel 7 Enable
23:16	8'b0	package	ARB_H	Arb H
30:24	7'b0	package	ARB_L	Arb L
31	1'b0	package	P	Priority EN

4.118 DQAR

Descriptor Queue Access Register

Offset: 0xA284 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
2:0	3'd0	package	DQI	Descriptor Queue Index - Provides an index into the descriptor queue when accessing descriptors.
5:3	3'd0	package	RSVD	Reserved
6	1'b0	package	WR	Write / Read bit - A 0b1 performs a write; a 0b0 performs a read
7	1'b0	package	CMT	Commit bit - When written, access into the Descriptor Queue is performed.
8	1'b0	package	RSVD	Reserved
29	1'b0	package	Q	All Channels Quiesced
30	1'b0	package	GQ	Global Quiesce
31	1'b0	package	SE	SBQ Empty

4.119 DQDR_TL

Descriptor Queue Data Register Top Left

Offset: 0xA288 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	DESC_TL	Descriptor Tail Top Left

4.120 DQDR_TR

Descriptor Queue Data Register Top Right

Offset: 0xA28C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	DESC_TR	Descriptor Tail Top Right

4.121 DQDR_BL

Descriptor Queue Data Register Bottom Left

Offset: 0xA290 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	DESC_BL	Descriptor Tail Bottom Left

4.122 DQDR_BR

Descriptor Queue Data Register Bottom Right

Offset: 0xA294 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	DESC_BR	Descriptor Tail Bottom Right

4.123 DMA_MISC

Misc DMA configuration

Offset: 0xA2A4 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3	1'b1	package	DMA_DSTATWB_A_ENABLE	Enable SW notification feature when affiliated error occurs in ACTIVE states.
2	1'b0	package	DMA_CH_ERROR_CHECKING_DISABLE	Disable all DMA channel error checking logic
1	1'b0	package	HEAD_PTR_ERROR_MASK	Mask head pointer greater than descr ring size error
0	1'b0	package	AES_DESC_EN	Enable AES Descriptors for DMA CHNL7

4.124 RDMASR0

Remote DMA register

Offset: 0xB180 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.125 RDMASR1

Remote DMA register

Offset: 0xB184 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.126 RDMASR2

Remote DMA register

Offset: 0xB188 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.127 RDMASR3

Remote DMA register

Offset: 0xB18C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.128 RDMASR4

Remote DMA register

Offset: 0xB190 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.129 RDMASR5

Remote DMA register

Offset: 0xB194 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.130 RDMASR6

Remote DMA register

Offset: 0xB198 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.131 RDMASR7

Remote DMA register

Offset: 0xB19C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
31:0	32'd0	package	data	data written by descriptor

4.132 APR_PHY_BASE

Aperture Physical Base

Offset: 0xC11C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
23:0	24'h0	package	APR_PHY_BASE	Physical APR address

4.133 EMON_TCU_CONTROL

TCU EMON Control

Offset: 0xCC84 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
3:0	4'b0	package	Counter_Enable	Assert to Enable the EMON Counters 3 to 0
5:4	2'b0	package	CNT0_EVENT_GROUP	For the EMON counter 0, you can select between the RS events and other TCU events.
6	1'b0	package	CNT1_EVENT_GROUP	For the EMON counter 1, you can select between the RS events and RSVD.
8	1'b0	package	CNT2_EVENT_GROUP	For the EMON counter 2, you can select between the RS events and RSVD.
10	1'b0	package	CNT3_EVENT_GROUP	For the EMON counter 3, you can select between the RS events and RSVD.
19:16	4'b0	package	CNT0_TCU_SELECT	TCU events.

4.134 Doorbell_INT

System Doorbell Interrupt Command Register 0 to 3

Offset: 0xCC90 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
29:0	30'd0	package	DATA	Data Field - The coprocessor OS can write to this field to communicate any arbitrary interrupt inform host.
30	1'b0	package	DSTAT	Delivery Status - This bit is read only and represents a pending Marker Message at TCU SYSINT. 0=idle, 1=pending
31	1'b0	package	DBREQ	Doorbell Request - the coprocessor OS sets this bit to initiate a new doorbell request interrupt to the host driver.

4.135 Doorbell_INT

System Doorbell Interrupt Command Register 0 to 3

Offset: 0xCC94 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
29:0	30'd0	package	DATA	Data Field - The coprocessor OS can write to this field to communicate any arbitrary interrupt inform host.
30	1'b0	package	DSTAT	Delivery Status - This bit is read only and represents a pending Marker Message at TCU SYSINT. 0=idle, 1=pending
31	1'b0	package	DBREQ	Doorbell Request - the coprocessor OS sets this bit to initiate a new doorbell request interrupt to the host driver.

4.136 Doorbell_INT

System Doorbell Interrupt Command Register 0 to 3

Offset: 0xCC98 Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
29:0	30'd0	package	DATA	Data Field - The coprocessor OS can write to this field to communicate any arbitrary interrupt inform host.
30	1'b0	package	DSTAT	Delivery Status - This bit is read only and represents a pending Marker Message at TCU SYSINT. 0=idle, 1=pending
31	1'b0	package	DBREQ	Doorbell Request - the coprocessor OS sets this bit to initiate a new doorbell request interrupt to the host driver.

4.137 Doorbell_INT

System Doorbell Interrupt Command Register 0 to 3

Offset: 0xCC9C Base Address: 0x08007D0000

Range	Default	Scope	Bit Name	Bit Description
29:0	30'd0	package	DATA	Data Field - The coprocessor OS can write to this field to communicate any arbitrary interrupt inform host.
30	1'b0	package	DSTAT	Delivery Status - This bit is read only and represents a pending Marker Message at TCU SYSINT. 0=idle, 1=pending
31	1'b0	package	DBREQ	Doorbell Request - the coprocessor OS sets this bit to initiate a new doorbell request interrupt to the host driver.