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CYTVII-B-E-1M-176-CPU

Evaluation Board User Guide

Document Number. 002-22883 Rev. *C

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Contents

1. Introduction

This user guide provides instructions to use the CYTVII-B-E-1M-176-CPU and CYTVII-B-E-176-SO evaluation boards, collectively referred to as 'CPU board' in this document. This is an evaluation platform for the CYT2B78CABES Traveo II device. The board can be used standalone for basic validation or in combination with the CYTVII-B-E-BB Traveo II baseboard (available separately from Cypress). This document assumes that you will work with the combination (CPU board + baseboard), and provides guidance to use features of the evaluation platform. The Device Port Pin Connections on Baseboard and CPU board schematic used in this document is for CYTVII-B-E-1M-176-CPU Rev C and Rev 1.0 boards and CYTVII-B-E-176-SO Rev C and Rev 1.0 boards only.

1.1 Precautions and Warnings

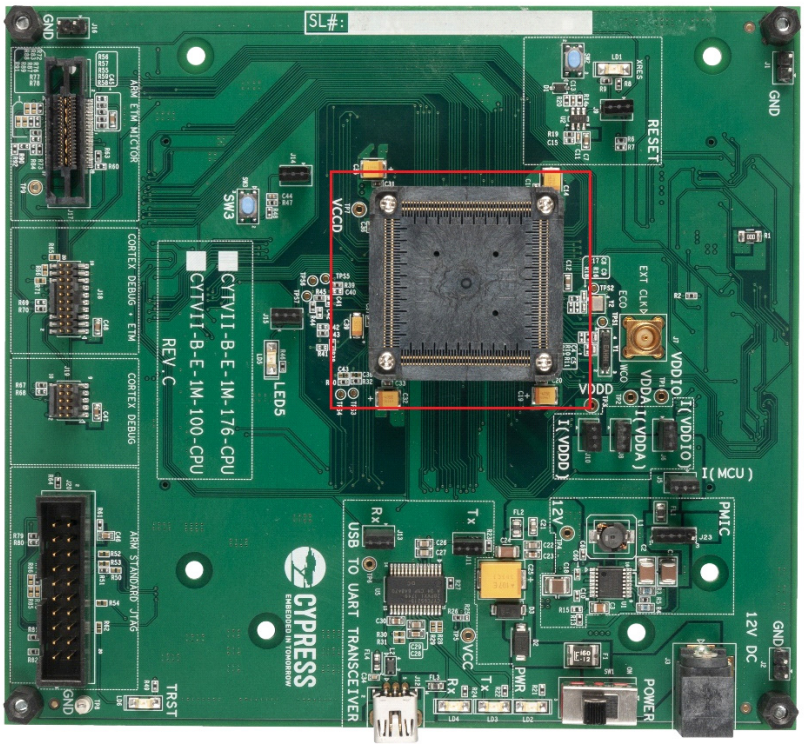
The evaluation board must be handled by qualified personnel who are aware of the capabilities of the boards. You must ensure your own safety arising from electrical hazards and other sources. You must carefully handle the board, which is a delicate PCB, and ensure that it is not subjected to bending or other stresses.

The CPU board is shipped with a 12 V DC power adapter. This adapter can be plugged into the AC mains supply anywhere in the world and is designed to receive 100-240 V AC V @ 50/60 Hz. While powering the board, you must connect only the power adapter supplied with the evaluation board and not any other part.

2. Overview

Figure 2-1 shows the CYTVII-B-E-176-SO board. Insert a Traveo II device into the IC socket (marked in red) while the evaluation board is powered OFF.

Figure 2-1. CYTVII-B-E-176-SO Board

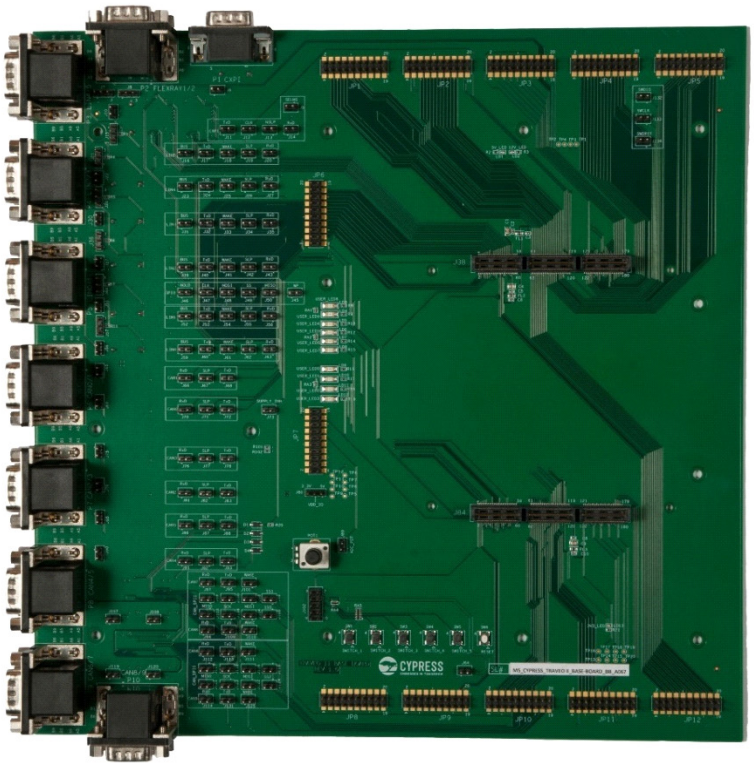


A variant of the CPU board (CYTVII-B-E-1M-176-CPU) is also available, where the Traveo II device is soldered directly onto the PCB. Functionally, the CYTVII-B-E-1M-176-CPU and CYTVII-B-E-176-SO boards are identical, except that the device can be easily replaced in the latter. Figure 2-3 shows the CYTVII-B-E-1M-176-CPU mounted on baseboard.

Another variant of the CPU board is available which has 100-pin socket mounted on it. The CPU board referred as a CYTVII-B-E-1M-100-SO board.

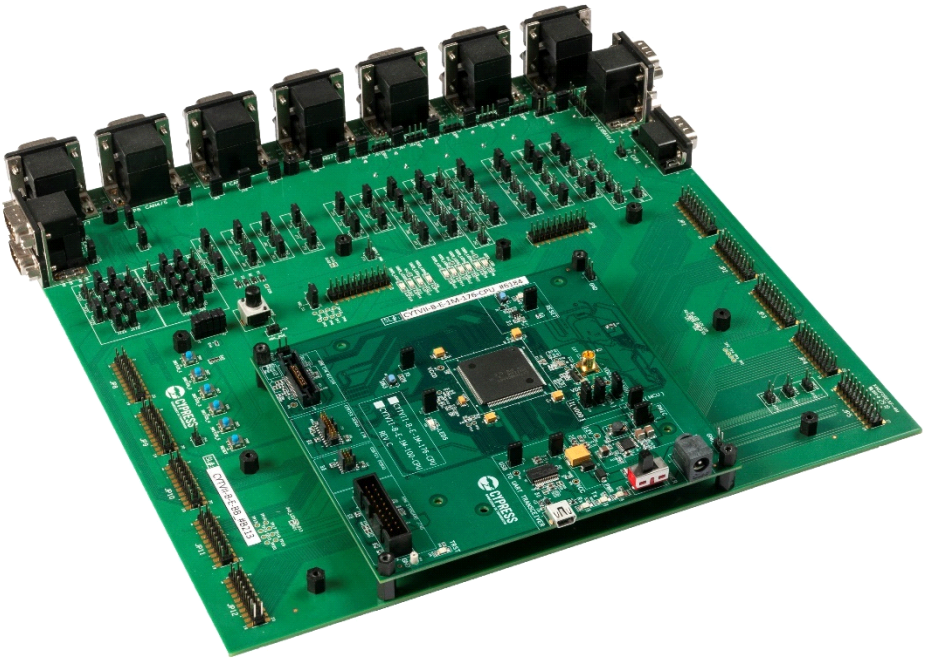
The CPU board is meant to be used along with a Traveo II baseboard (CYTVII-B-E-BB). The baseboard brings out all important interface connections such as CAN, LIN, SPI EEPROM, CXPI, and Flexray, and can be used in conjunction with several CPU boards of the Traveo II family. Figure 2-2 shows the baseboard.

Figure 2-2. Traveo II Base board (CYTVII-B-E-BB)



Two Samtec connectors on the CPU board and corresponding mating connectors on the baseboard are used to connect signals across the two boards. When put together, the boards appear as shown in Figure 2-3.

Figure 2-3. Combination of CPU Board and TVII Base Board



2.1 Functional Overview

The CPU board has the following features:

1. One Traveo II device, either soldered or mounted on a socket (U4).
2. PMIC to generate the 5 V and 3.3 V output depending on the Jumper J23 selection, which powers the CPU board and the baseboard (if connected).
3. Programming interface (JTAG-20, MiniProg3, SWD, and IDC-20, Mictor trace port) to connect several programming tools such as IAR I-jet, Green Hills GHS, MiniProg.
4. USB-UART interface for terminal logging (J12).
5. One user switch (SW3) and one user LED (LED5) for standalone operation without the baseboard.
6. Reset controller with manual reset switch (SW2) and voltage supervision.
7. Measurement of device current on VDDIO, VDDA, and VDDD using jumpers J6, J8, and J10 respectively.
8. Samtec connector interface (J21 and J22) for connecting to the baseboard CYTVII-B-E-BB.

The Traveo II baseboard has the following features:

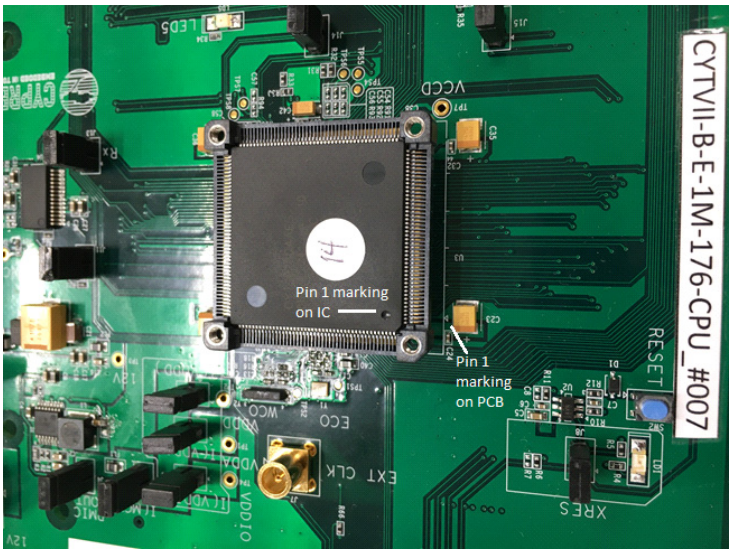
1. Six CAN-FD transceivers based on TJA1057GT (Dual connectors P6, P7, P8).
2. Four CAN-FD transceivers based on TJA1145T, with SPI-based transceiver configuration (Dual connectors P9, P10).
3. Six LIN transceivers based on TJA1021T (Dual connectors (Dual connectors P3, P4, P5).
4. Two Flexray transceivers based on TJA1081TS (Dual connector P2).
5. One CXPI transceiver based on S6BT112A01 (Connector P1).
6. One SPI EEPROM 25LC320A (U9).
7. Five user switches (SW1 through SW5), 10 user LEDs (USER_LED0 through USER_LED9) and one potentiometer (POT1) for analog input.
8. Pin headers to access all I/Os of the TVII device (when a CPU board is connected to the baseboard).
9. Samtec connector interface (J38 and J84) for connecting to a CPU board.

3. Operation

This section describes the operation of the CPU board and the baseboard. It is assumed that you have connected the CPU board to the baseboard using the Samtec interface and inserted a TVII device into the IC socket (applicable to SO boards only). The following method can be used to operate the CPU board and the baseboard.

1. For socketed CPU board, ensure that the device is inserted into the socket. Remove the four screws on the socket using the screwdriver provided in the box and open the socket cover. If the device is not present, place one carefully using a vacuum picker or a pair of tweezers.
2. Ensure that the pin 1 of the device is near the arrow mark (near C14) as shown in Figure 3-1. You must also ensure that the angle of placing the device is such that the pins on all four sides of the LQFP package match well with the socket pins. Align the device slightly if required.

Figure 3-1. Orientation of Device when Inserted in Socket



3. Put the socket cover and fix the four screws such that the socket cover tightly sits on the socket base.
4. A 12V wall adapter board is supplied along with the CPU board. Connect the 12 V wall adapter to the barrel connector marked “12V DC” on the CPU board. Connect its plug to a mains socket using one of the four plug adapters provided in the white box (depending on the geographical location and the socket type available).
5. Ensure that jumpers J23 (default 5 V: J23_1 and J23_2), J5, J6, J8, J10 (current measurement jumpers) are inserted on the CPU board. You can select the 3.3 V power rails for CPU board by shorting J23_2 and J23_2 as per their application or hardware setup.

6. Turn ON the mains supply to the wall adapter. Turn ON the switch SW1 on the CPU board. The LED labelled PWR should light up.
7. Connect an appropriate programming tool to one of the programming interfaces (J17, J18, J19, J20). Programming tool options are:
   - GHS Trace on J20
   - IAR I-jet on J18 or J19
   - MiniProg3 on J19
8. Install the appropriate programming IDE on a PC. The programming IDE (GHS Multi, IAR EWB, CYP, and so on) should be able to detect a device (read the device ID) and to load a firmware HEX file (.sreg) into the device flash successfully.
   As part of the release package, various firmware examples compiled in several programming IDEs are available. Some examples use specific transceivers on the baseboard.
9. To start with, use the LED blink example provided with the release package to test the functioning of the board.
10. Connect a USB-mini cable to J12 and the other end to a PC. Open Tera Term or your preferred terminal logging application and set the appropriate port and baud rate (typically 115,200 baud, 8, N, 1). Ensure that jumpers J11 and J13 are inserted on the CPU board. Some firmware examples provide data logs from the device or ask for user inputs over the terminal.

4. Connections and Settings

Ensure that the following jumpers are inserted on the baseboard to use each transceiver on the baseboard with respective firmware examples which activate each functionality of the device.

1. CAN0.0 from the device uses the CAN0 and CAN6 transceiver on the baseboard. These transceivers are selectable through jumpers on baseboard. (connect jumpers J70, J71, J72 for CAN0 and J94, J109, J110, J105, J104, J106 and J103 for CAN6)
2. CAN0.1 from the device uses the CAN1 and CAN7 transceiver on the baseboard. These transceivers are selectable through jumpers on baseboard.(connect jumpers J66, J67, J68 for CAN1 and J97, J95, J101, J96, J98, J99 and J100 for CAN7)
3. CAN0.2 from the device uses the CAN2 and CAN8 transceiver on the baseboard. These transceivers are selectable through jumpers on baseboard.(connect jumpers J81, J82, J83 for CAN2 and J111, J112, J113, J115, J116, J118 and J117 for CAN8)
4. CAN1.0 from the device uses the CAN3 and CAN9 transceiver on the baseboard. These transceivers are selectable through jumpers on baseboard.(connect jumpers J76, J77, J78 for CAN3 and J114, J131, J125, J121, J122, J123 and J124 for CAN9)
5. CAN1.1 from the device uses the CAN4 transceiver on the baseboard (connect jumpers J91, J92, J93)
6. CAN1.2 from the device uses the CAN5 transceiver on the baseboard (connect jumpers J86, J87, J88)
7. LIN0 from the device uses the LIN0 transceiver on the baseboard (connect jumpers J58, J59, J60, J63)
8. LIN1 from the device uses the LIN1 transceiver on the baseboard (connect jumpers J51, J52, J53, J56)
9. LIN2 from the device uses the LIN2 transceiver on the baseboard (connect jumpers J37, J39, J40, J43)
10. LIN3 from the device uses the LIN3 transceiver on the baseboard (connect jumpers J30, J31, J32, J35)
11. LIN4 from the device uses the LIN4 transceiver on the baseboard (connect jumpers J22, J23, J24, J27)
12. LIN6 from the device uses the LIN5 transceiver on the baseboard (connect jumpers J10, J16, J17, J20)
13. EEPROM on the baseboard is enabled by connecting jumpers J47, J48, J49.
14. The user switch functionality is enabled by connecting jumper J102.
15. The potentiometer functionality is enabled by connecting jumper J89.

In addition, power is supplied to the baseboard by connecting jumper J80 in the '5V' position and must always be connected. Once a specific functionality is chosen by connecting the jumpers listed above, ensure that the appropriate firmware is loaded onto the device. Incorrect firmware can result in port pins being configured incorrectly leading to bus contention and damage to hardware. For example, if you connect jumpers related to CAN0.0, you must ensure that firmware configures the related ports as CAN pins. **Contact Cypress technical support for firmware examples**.

Apart from these interface transceivers that can be used for specific functions, all pins of the device are also accessible on the baseboard using pin headers JP1 through JP12.

The device port pins are connected to pin headers on the baseboard as listed in Table 4-1.

Table 4-1. Device Port Pin Connections on Baseboard

Port Pin	Pin Function	Access Pin on Baseboard
P0.0	PWM_18/PWM_22_N/TC_18_TR0/TC_22_TR1/SCB0_RX/SCB7_SDA/SCB0_MISO/ LIN1_RX	JP6.15
P0.1	PWM_17/PWM_18_N/TC_17_TR0/TC_18_TR1/SCB0_TX/SCB7_SCL/SCB0_MOSI/ LIN1_TX	JP6.14
P0.2	PWM_14/PWM_17_N/TC_14_TR0/TC_17_TR1/SCB0_RTS/SCB0_SCL/SCB0_CLK/ LIN1_EN/CAN0_1_TX	JP6.9
P0.3	PWM_13/PWM_14_N/TC_13_TR0/TC_14_TR1/SCB0_CTS/SCB0_SDA/SCB0_- SEL0/CAN0_1_RX	JP6.8
P1.0	PWM_12/PWM_13_N/TC_12_TR0/TC_13_TR1/SCB0_SCL/SCB0_MISO	JP8.4
P1.1	PWM_11/PWM_12_N/TC_11_TR0/TC_12_TR1/SCB0_SDA/SCB0_MOSI	JP8.3
P1.2	PWM_10/PWM_11_N/TC_10_TR0/TC_11_TR1/SCB0_CLK/TRIG_IN[0]	JP8.6
P1.3	PWM_8/PWM_10_N/TC_8_TR0/TC_10_TR1/SCB0_SEL0/TRIG_IN[1]	JP8.5
P10.0	PWM_28/PWM_27_N/TC_28_TR0/TC_27_TR1/SCB4_RX/SCB4_MISO/ TRIG_IN[18]	JP9.16
P10.1	PWM_29/PWM_28_N/TC_29_TR0/TC_28_TR1/SCB4_TX/SCB4_SDA/SCB4_MOSI/ TRIG_IN[19]	JP9.15
P10.2	PWM_30/PWM_29_N/TC_30_TR0/TC_29_TR1/SCB4_RTS/SCB4_SCL/SCB4_CLK	JP6.13
P10.3	PWM_31/PWM_30_N/TC_31_TR0/TC_30_TR1/SCB4_CTS/SCB4_SEL0	JP6.16
P10.4	PWM_32/PWM_31_N/TC_32_TR0/TC_31_TR1/SCB4_SEL1/ADC[1]_0	JP6.17
P10.5	PWM_33/PWM_32_N/TC_33_TR0/TC_32_TR1/SCB4_SEL2/ADC[1]_1	JP1.7
P10.6	PWM_34/PWM_33_N/TC_34_TR0/TC_33_TR1/ADC[1]_2	JP1.8
P10.7	PWM_35/PWM_34_N/TC_35_TR0/TC_34_TR1/ADC[1]_3	JP1.13
P11.0	ADC[0]_M	JP9.6
P11.1	ADC[1]_M	JP9.5
P11.2	ADC[2]_M	JP9.8
P12.0	PWM_36/PWM_35_N/TC_36_TR0/TC_35_TR1/CAN0_2_TX/TRIG_IN[20]/ADC[1]_4	JP10.8
P12.1	PWM_37/PWM_36_N/TC_37_TR0/TC_36_TR1/LIN6_EN/CAN0_2_RX/TRIG_IN[21]/ ADC[1]_5	JP10.7
P12.2	PWM_38/PWM_37_N/TC_38_TR0/TC_37_TR1/EXT_MUX[1]_EN/LIN6_RX/ ADC[1]_6	JP1.9
P12.3	PWM_39/PWM_38_N/TC_39_TR0/TC_38_TR1/EXT_MUX[1]_0/LIN6_TX/ADC[1]_7	JP1.10
P12.4	PWM_40/PWM_39_N/TC_40_TR0/TC_39_TR1/EXT_MUX[1]_1/ADC[1]_8	JP10.13
P12.5	PWM_41/PWM_40_N/TC_41_TR0/TC_40_TR1/EXT_MUX[1]_2/ADC[1]_9	JP1.14
P12.6	PWM_42/PWM_41_N/TC_42_TR0/TC_41_TR1/ADC[1]_10	JP2.18
P12.7	PWM_43/PWM_42_N/TC_43_TR0/TC_42_TR1/ADC[1]_11	JP2.17
P13.0	PWM_M_8/PWM_43_N/TC_M_8_TR0/TC_43_TR1/EXT_MUX[2]_0/SCB3_RX/ SCB3_MISO/ADC[1]_12	JP10.4

Table 4-1. Device Port Pin Connections on Baseboard *(continued)*

Port Pin	Pin Function	Access Pin on Baseboard
P13.1	PWM_44/PWM_M_8_N/TC_44_TR0/TC_M_8_TR1/EXT_MUX[2]_1/SCB3_TX/ SCB3_SDA/SCB3_MOSI/ADC[1]_13	JP10.3
P13.2	PWM_M_9/PWM_44_N/TC_M_9_TR0/TC_44_TR1/EXT_MUX[2]_2/SCB3_RTS/ SCB3_SCL/SCB3_CLK/ADC[1]_14	JP10.16
P13.3	PWM_45/PWM_M_9_N/TC_45_TR0/TC_M_9_TR1/EXT_MUX[2]_EN/SCB3_CTS/ SCB3_SEL0/ADC[1]_15	JP1.5
P13.4	PWM_M_10/PWM_45_N/TC_M_10_TR0/TC_45_TR1/SCB3_SEL1/ADC[1]_16	JP6.4
P13.5	PWM_46/PWM_M_10_N/TC_46_TR0/TC_M_10_TR1/SCB3_SEL2/ADC[1]_17	JP2.7
P13.6	PWM_M_11/PWM_46_N/TC_M_11_TR0/TC_46_TR1/SCB3_SEL3/TRIG_IN[22]/ ADC[1]_18	JP2.11
P13.7	PWM_47/PWM_M_11_N/TC_47_TR0/TC_M_11_TR1/TRIG_IN[23]/ADC[1]_19	JP2.15
P14.0	PWM_48/PWM_47_N/TC_48_TR0/TC_47_TR1/SCB2_RX/SCB2_MISO/ CAN1_0_TX/ADC[1]_20	JP3.12
P14.1	PWM_49/PWM_48_N/TC_49_TR0/TC_48_TR1/SCB2_TX/SCB2_SDA/SCB2_MOSI/ CAN1_0_RX/ADC[1]_21	JP3.14
P14.2	PWM_50/PWM_49_N/TC_50_TR0/TC_49_TR1/SCB2_RTS/SCB2_SCL/SCB2_CLK/ LIN6_RX/ADC[1]_22	JP1.11
P14.3	PWM_51/PWM_50_N/TC_51_TR0/TC_50_TR1/SCB2_CTS/SCB2_SEL0/LIN6_TX/ ADC[1]_23	JP7.8
P14.4	PWM_52/PWM_51_N/TC_52_TR0/TC_51_TR1/SCB2_SEL1/LIN6_EN/ADC[1]_24	JP7.12
P14.5	PWM_53/PWM_52_N/TC_53_TR0/TC_52_TR1/SCB2_SEL2/ADC[1]_25	JP7.16
P14.6	PWM_54/PWM_53_N/TC_54_TR0/TC_53_TR1/TRIG_IN[24]/ADC[1]_26	JP7.17
P14.7	PWM_55/PWM_54_N/TC_55_TR0/TC_54_TR1/TRIG_IN[25]/ADC[1]_27	JP3.3
P15.0	PWM_56/PWM_55_N/TC_56_TR0/TC_55_TR1/ADC[1]_28	JP3.5
P15.1	PWM_57/PWM_56_N/TC_57_TR0/TC_56_TR1/ADC[1]_29	JP3.7
P15.2	PWM_58/PWM_57_N/TC_58_TR0/TC_57_TR1/ADC[1]_30	JP3.9
P15.3	PWM_59/PWM_58_N/TC_59_TR0/TC_58_TR1/ADC[1]_31	JP3.11
P16.0	PWM_60/PWM_59_N/TC_60_TR0/TC_59_TR1/PWM_H_0	JP3.13
P16.1	PWM_61/PWM_60_N/TC_61_TR0/TC_60_TR1/PWM_H_0_N	JP3.15
P16.2	PWM_62/PWM_61_N/TC_62_TR0/TC_61_TR1/PWM_H_1	JP3.17
P16.3	PWM_62/PWM_62_N/TC_62_TR0/TC_62_TR1/PWM_H_1_N	JP4.3
P17.0	PWM_61/PWM_62_N/TC_61_TR0/TC_62_TR1/CAN1_1_TX	JP11.8
P17.1	PWM_60/PWM_61_N/TC_60_TR0/TC_61_TR1/PWM_H_2/SCB3_RX/SCB3_MISO/ CAN1_1_RX	JP11.7
P17.2	PWM_59/PWM_60_N/TC_59_TR0/TC_60_TR1/PWM_H_2_N/SCB3_TX/ SCB3_SDA/SCB3_MOSI	JP2.3
P17.3	PWM_58/PWM_59_N/TC_58_TR0/TC_59_TR1/PWM_H_3/SCB3_RTS/SCB3_SCL/ SCB3_CLK/TRIG_IN[26]	JP4.5
P17.4	PWM_57/PWM_58_N/TC_57_TR0/TC_58_TR1/PWM_H_3_N/SCB3_CTS/SCB3_- SEL0/TRIG_IN[27]	JP4.11
P17.5	PWM_56/PWM_57_N/TC_56_TR0/TC_57_TR1/SCB3_SEL1	JP3.10
P17.6	PWM_M_4/PWM_56_N/TC_M_4_TR0/TC_56_TR1/SCB3_SEL2	JP3.8
P17.7	PWM_M_5/PWM_M_4_N/TC_M_5_TR0/TC_M_4_TR1	JP3.6

Table 4-1. Device Port Pin Connections on Baseboard *(continued)*

Port Pin	Pin Function	Access Pin on Baseboard
P18.0	PWM_M_6/PWM_M_5_N/TC_M_6_TR0/TC_M_5_TR1/PWM_H_0/SCB1_RX/ SCB1_MISO/FAULT_OUT_0/ADC[2]_0	JP3.18
P18.1	PWM_M_7/PWM_M_6_N/TC_M_7_TR0/TC_M_6_TR1/PWM_H_0_N/SCB1_TX/ SCB1_SDA/SCB1_MOSI/ FAULT_OUT_1/ADC[2]_1	JP3.16
P18.2	PWM_55/PWM_M_7_N/TC_55_TR0/TC_M_7_TR1/PWM_H_1/SCB1_RTS/ SCB1_SCL/SCB1_CLK/ADC[2]_2	JP9.17
P18.3	PWM_54/PWM_55_N/TC_54_TR0/TC_55_TR1/PWM_H_1_N/SCB1_CTS/SCB1_- SEL0/TRACE_CLOCK/ADC[2]_3	JP4.4
P18.4	PWM_53/PWM_54_N/TC_53_TR0/TC_54_TR1/PWM_H_2/SCB1_SEL1/TRACE_- DATA_0/ADC[2]_4	JP9.18
P18.5	PWM_52/PWM_53_N/TC_52_TR0/TC_53_TR1/PWM_H_2_N/SCB1_SEL2/ TRACE_DATA_1/ADC[2]_5	JP12.4
P18.6	PWM_51/PWM_52_N/TC_51_TR0/TC_52_TR1/PWM_H_3/SCB1_SEL3/ CAN1_2_TX/TRACE_DATA_2/ADC[2]_6	JP11.6
P18.7	PWM_50/PWM_51_N/TC_50_TR0/TC_51_TR1/PWM_H_3_N/CAN1_2_RX/ TRACE_DATA_3/ADC[2]_7	JP11.5
P19.0	PWM_M_3/PWM_50_N/TC_M_3_TR0/TC_50_TR1/TC_H_0_TR0/SCB2_RX/ SCB2_MISO/FAULT_OUT_2	JP7.9
P19.1	PWM_26/PWM_M_3_N/TC_26_TR0/TC_M_3_TR1/TC_H_0_TR1/SCB2_TX/ SCB2_SDA/SCB2_MOSI/FAULT_OUT_3	JP7.13
P19.2	PWM_27/PWM_26_N/TC_27_TR0/TC_26_TR1/TC_H_1_TR0/SCB2_RTS/ SCB2_SCL/SCB2_CLK/TRIG_IN[28]	JP6.5
P19.3	PWM_28/PWM_27_N/TC_28_TR0/TC_27_TR1/TC_H_1_TR1/SCB2_CTS/SCB2_- SEL0/TRIG_IN[29]	JP6.10
P19.4	PWM_29/PWM_28_N/TC_29_TR0/TC_28_TR1/TC_H_2_TR0/SCB2_SEL1	JP3.4
P20.0	PWM_30/PWM_29_N/TC_30_TR0/TC_29_TR1/TC_H_2_TR1/SCB2_SEL2/LIN5_RX	JP7.4
P20.1	PWM_49/PWM_30_N/TC_49_TR0/TC_30_TR1/TC_H_3_TR0/LIN5_TX	JP7.5
P20.2	PWM_48/PWM_49_N/TC_48_TR0/TC_49_TR1/TC_H_3_TR1/LIN5_EN	JP4.14
P20.3	PWM_47/PWM_48_N/TC_47_TR0/TC_48_TR1/SCB1_RX/SCB1_MISO/ CAN1_2_TX	JP4.15
P20.4	PWM_46/PWM_47_N/TC_46_TR0/TC_47_TR1/SCB1_TX/SCB1_SDA/SCB1_MOSI/ CAN1_2_RX	JP5.8
P20.5	PWM_45/PWM_46_N/TC_45_TR0/TC_46_TR1/SCB1_RTS/SCB1_SCL/SCB1_CLK	JP5.9
P20.6	PWM_44/PWM_45_N/TC_44_TR0/TC_45_TR1/SCB1_CTS/SCB1_SEL0	JP5.7
P20.7	PWM_43/PWM_44_N/TC_43_TR0/TC_44_TR1/SCB1_SEL1	JP5.6
P2.0	PWM_7/PWM_8_N/TC_7_TR0/TC_8_TR1/SCB7_RX/SCB0_SEL1/SCB7_MISO/ LIN0_RX/CAN0_0_TX/ SWJ_TRSTN/TRIG_IN[2]	#NA
P2.1	PWM_6/PWM_7_N/TC_6_TR0/TC_7_TR1/SCB7_TX/SCB7_SDA/SCB0_SEL2/ SCB7_MOSI/LIN0_TX/ CAN0_0_RX/TRIG_IN[3]	JP1.4
P2.2	PWM_5/PWM_6_N/TC_5_TR0/TC_6_TR1/SCB7_RTS/SCB7_SCL/SCB0_SEL3/ SCB7_CLK/LIN0_EN/TRIG_IN[4]	JP1.6
P2.3	PWM_4/PWM_5_N/TC_4_TR0/TC_5_TR1/SCB7_CTS/SCB7_SEL0/LIN5_RX/ TRIG_IN[5]	JP10.11
P2.4	PWM_3/PWM_4_N/TC_3_TR0/TC_4_TR1/SCB7_SEL1/LIN5_TX/TRIG_IN[6]	JP8.8

Table 4-1. Device Port Pin Connections on Baseboard *(continued)*

Port Pin	Pin Function	Access Pin on Baseboard
P2.5	PWM_2/PWM_3_N/TC_2_TR0/TC_3_TR1/SCB7_SEL2/LIN5_EN/TRIG_IN[7]	JP8.7
P21.0	PWM_42/PWM_43_N/TC_42_TR0/TC_43_TR1/SCB1_SEL2/WCO_IN	#N/A
P21.1	PWM_41/PWM_42_N/TC_41_TR0/TC_42_TR1/WCO_OUT	#N/A
P21.2	PWM_40/PWM_41_N/TC_40_TR0/TC_41_TR1/TRIG_DBG[1]/EXT_CLK/ECO_IN	#N/A
P21.3	PWM_39/PWM_40_N/TC_39_TR0/TC_40_TR1/ECO_OUT	#N/A
P21.4	PWM_38/PWM_39_N/TC_38_TR0/TC_39_TR1/HIBERNATE_WAKEUP[0]	JP5.5
P21.5	PWM_37/PWM_38_N/TC_37_TR0/TC_38_TR1/LIN0_RX	JP1.3
P21.6	PWM_36/PWM_37_N/TC_36_TR0/TC_37_TR1/LIN0_TX	JP5.10
P21.7	PWM_35/PWM_36_N/TC_35_TR0/TC_36_TR1/LIN0_EN/CAL_SUP_NZ/RTC_CAL	JP5.18
P22.0	PWM_34/PWM_35_N/TC_34_TR0/TC_35_TR1/SCB6_RX/SCB6_MISO/ CAN1_1_TX/TRACE_DATA_0	JP4.6
P22.1	PWM_33/PWM_34_N/TC_33_TR0/TC_34_TR1/SCB6_TX/SCB6_SDA/SCB6_- MOSI/ CAN1_1_RX/TRACE_DATA_1	JP4.8
P22.2	PWM_32/PWM_33_N/TC_32_TR0/TC_33_TR1/SCB6_RTS/SCB6_SCL/SCB6_CLK/ TRACE_DATA_2	JP4.10
P22.3	PWM_31/PWM_32_N/TC_31_TR0/TC_32_TR1/SCB6_CTS/SCB6_SEL0/TRACE_- DATA_3	JP4.12
P22.4	PWM_30/PWM_31_N/TC_30_TR0/TC_31_TR1/SCB6_SEL1/TRACE_CLOCK	JP5.11
P22.5	PWM_29/PWM_30_N/TC_29_TR0/TC_30_TR1/SCB6_SEL2/LIN7_RX	JP5.12
P22.6	PWM_28/PWM_29_N/TC_28_TR0/TC_29_TR1/LIN7_TX	JP5.13
P22.7	PWM_27/PWM_28_N/TC_27_TR0/TC_28_TR1/LIN7_EN	JP5.14
P23.0	PWM_M_8/PWM_27_N/TC_M_8_TR0/TC_27_TR1/SCB7_RX/SCB7_MISO/ CAN1_0_TX/FAULT_OUT_0	JP5.15
P23.1	PWM_M_9/PWM_M_8_N/TC_M_9_TR0/TC_M_8_TR1/SCB7_TX/SCB7_SDA/ SCB7_MOSI/CAN1_0_RX/FAULT_OUT_1	JP5.16
P23.2	PWM_M_10/PWM_M_9_N/TC_M_10_TR0/TC_M_9_TR1/SCB7_RTS/SCB7_SCL/ SCB7_CLK/FAULT_OUT_2	JP5.17
P23.3	PWM_M_11/PWM_M_10_N/TC_M_11_TR0/TC_M_10_TR1/SCB7_CTS/SCB7_- SEL0/FAULT_OUT_3/TRIG_IN[30]	JP7.10
P23.4	PWM_25/PWM_M_11_N/TC_25_TR0/TC_M_11_TR1/SCB7_SEL1/TRIG_DBG[0]/ SWJ_SWO_TDO/TRIG_IN[31]	JP4.7
P23.5	PWM_24/PWM_25_N/TC_24_TR0/TC_25_TR1/SCB7_SEL2/SWJ_SWCLK_TCLK	#N/A
P23.6	PWM_23/PWM_24_N/TC_23_TR0/TC_24_TR1/SWJ_SWDIO_TMS	#N/A
P23.7	PWM_22/PWM_23_N/TC_22_TR0/TC_23_TR1/CAL_SUP_NZ/SWJ_SWDOE_TDI/ EXT_CLK/HIBERNATE_WAKEUP[1]	JP4.9
P3.0	PWM_1/PWM_2_N/TC_1_TR0/TC_2_TR1/SCB6_RX/SCB6_MISO/TRIG_DBG[0]	JP10.14
P3.1	PWM_0/PWM_1_N/TC_0_TR0/TC_1_TR1/SCB6_TX/SCB6_SDA/SCB6_MOSI/ TRIG_DBG[1]	JP11.4
P3.2	PWM_M_3/PWM_0_N/TC_M_3_TR0/TC_0_TR1/SCB6_RTS/SCB6_SCL/SCB6_- CLK	JP8.10
P3.3	PWM_M_2/PWM_M_3_N/TC_M_2_TR0/TC_M_3_TR1/SCB6_CTS/SCB6_SEL0	JP8.9
P3.4	PWM_M_1/PWM_M_2_N/TC_M_1_TR0/TC_M_2_TR1/SCB6_SEL1	JP8.12
P3.5	PWM_M_0/PWM_M_1_N/TC_M_0_TR0/TC_M_1_TR1/SCB6_SEL2	JP8.11

Table 4-1. Device Port Pin Connections on Baseboard *(continued)*

Port Pin	Pin Function	Access Pin on Baseboard
P4.0	PWM_4/PWM_M_0_N/TC_4_TR0/TC_M_0_TR1/EXT_MUX[0]_0/SCB5_RX/ SCB5_MISO/ LIN1_RX/TRIG_IN[10]	JP8.14
P4.1	PWM_5/PWM_4_N/TC_5_TR0/TC_4_TR1/EXT_MUX[0]_1/SCB5_TX/SCB5_SDA/ SCB5_MOSI/LIN1_TX/TRIG_IN[11]	JP8.13
P4.2	PWM_6/PWM_5_N/TC_6_TR0/TC_5_TR1/EXT_MUX[0]_2/SCB5_RTS/SCB5_SCL/ SCB5_CLK/LIN1_EN/TRIG_IN[12]	JP8.16
P4.3	PWM_7/PWM_6_N/TC_7_TR0/TC_6_TR1/EXT_MUX[0]_EN/SCB5_CTS/SCB5_- SEL0/ CAN0_1_TX/TRIG_IN[13]	JP8.15
P4.4	PWM_8/PWM_7_N/TC_8_TR0/TC_7_TR1/SCB5_SEL1/CAN0_1_RX	JP8.18
P5.0	PWM_9/PWM_8_N/TC_9_TR0/TC_8_TR1/SCB5_SEL2/LIN7_RX	JP11.3
P5.1	PWM_10/PWM_9_N/TC_10_TR0/TC_9_TR1/LIN7_TX	JP10.15
P5.2	PWM_11/PWM_10_N/TC_11_TR0/TC_10_TR1/LIN7_EN	JP10.18
P5.3	PWM_12/PWM_11_N/TC_12_TR0/TC_11_TR1/LIN2_RX	JP2.5
P5.4	PWM_13/PWM_12_N/TC_13_TR0/TC_12_TR1/LIN2_TX	JP8.17
P5.5	PWM_14/PWM_13_N/TC_14_TR0/TC_13_TR1/LIN2_EN	JP10.6
P6.0	PWM_M_0/PWM_14_N/TC_M_0_TR0/TC_14_TR1/SCB4_RX/SCB4_MISO/ LIN3_RX/ADC[0]_0	JP2.9
P6.1	PWM_0/PWM_M_0_N/TC_0_TR0/TC_M_0_TR1/SCB4_TX/SCB4_SDA/SCB4_- MOSI/LIN3_TX/ADC[0]_1	JP2.10
P6.2	PWM_M_1/PWM_0_N/TC_M_1_TR0/TC_0_TR1/SCB4_RTS/SCB4_SCL/SCB4_- CLK/LIN3_EN/ CAN0_2_TX/ADC[0]_2	#NA
P6.3	PWM_1/PWM_M_1_N/TC_1_TR0/TC_M_1_TR1/SCB4_CTS/SCB4_SEL0/LIN4_RX/ CAN0_2_RX/ CAL_SUP_NZ/ADC[0]_3	#NA
P6.4	PWM_M_2/PWM_1_N/TC_M_2_TR0/TC_1_TR1/SCB4_SEL1/LIN4_TX/ADC[0]_4	JP2.14
P6.5	PWM_2/PWM_M_2_N/TC_2_TR0/TC_M_2_TR1/SCB4_SEL2/LIN4_EN/ADC[0]_5	JP2.16
P6.6	PWM_M_3/PWM_2_N/TC_M_3_TR0/TC_2_TR1/SCB4_SEL3/TRIG_IN[8]/ADC[0]_6	JP10.5
P6.7	PWM_3/PWM_M_3_N/TC_3_TR0/TC_M_3_TR1/TRIG_IN[9]/ADC[0]_7	JP11.11
P7.0	PWM_M_4/PWM_3_N/TC_M_4_TR0/TC_3_TR1/SCB5_RX/SCB5_MISO/LIN4_RX/ ADC[0]_8	JP12.3
P7.1	PWM_15/PWM_M_4_N/TC_15_TR0/TC_M_4_TR1/SCB5_TX/SCB5_SDA/SCB5_- MOSI/LIN4_TX/ADC[0]_9	JP12.6
P7.2	PWM_M_5/PWM_15_N/TC_M_5_TR0/TC_15_TR1/SCB5_RTS/SCB5_SCL/SCB5_- CLK/LIN4_EN/ADC[0]_10	JP12.5
P7.3	PWM_16/PWM_M_5_N/TC_16_TR0/TC_M_5_TR1/SCB5_CTS/SCB5_SEL0/ ADC[0]_11	JP10.10
P7.4	PWM_M_6/PWM_16_N/TC_M_6_TR0/TC_16_TR1/SCB5_SEL1/ADC[0]_12	JP10.9
P7.5	PWM_17/PWM_M_6_N/TC_17_TR0/TC_M_6_TR1/SCB5_SEL2/ADC[0]_13	JP10.12
P7.6	PWM_M_7/PWM_17_N/TC_M_7_TR0/TC_17_TR1/TRIG_IN[16]/ADC[0]_14	JP11.12
P7.7	PWM_18/PWM_M_7_N/TC_18_TR0/TC_M_7_TR1/TRIG_IN[17]/ADC[0]_15	JP11.9
P8.0	PWM_19/PWM_18_N/TC_19_TR0/TC_18_TR1/LIN2_RX/CAN0_0_TX	JP6.12
P8.1	PWM_20/PWM_19_N/TC_20_TR0/TC_19_TR1/LIN2_TX/CAN0_0_RX/TRIG_IN[14]/ ADC[0]_16	JP6.11
P8.2	PWM_21/PWM_20_N/TC_21_TR0/TC_20_TR1/LIN2_EN/TRIG_IN[15]/ADC[0]_17	JP2.8

Table 4-1. Device Port Pin Connections on Baseboard *(continued)*

Port Pin	Pin Function	Access Pin on Baseboard
P8.3	PWM_22/PWM_21_N/TC_22_TR0/TC_21_TR1/TRIG_DBG[0]/ADC[0]_18	JP11.10
P8.4	PWM_23/PWM_22_N/TC_23_TR0/TC_22_TR1/TRIG_DBG[1]/ADC[0]_19	JP9.9
P9.0	PWM_24/PWM_23_N/TC_24_TR0/TC_23_TR1/ADC[0]_20	JP9.12
P9.1	PWM_25/PWM_24_N/TC_25_TR0/TC_24_TR1/ADC[0]_21	JP9.11
P9.2	PWM_26/PWM_25_N/TC_26_TR0/TC_25_TR1/ADC[0]_22	JP9.14
P9.3	PWM_27/PWM_26_N/TC_27_TR0/TC_26_TR1/ADC[0]_23	JP9.13
VCCD	VCCD	#NA
VDDA	VDDA	JP1.17
VDDD	VDDD	JP1.15
VDDIO	VDDIO	JP1.16
VREFH	VREFH	#NA
VREFL	VREFL	#NA
VSSA	VSSA / VSSD / VSSIO/ Ground	JP1.19
XRES	XRES	JP12.16

A. Schematics of CPU Board

This appendix contains the schematics of TVII-B-E-1M board.

Figure A-1. Block Diagram of CPU Board

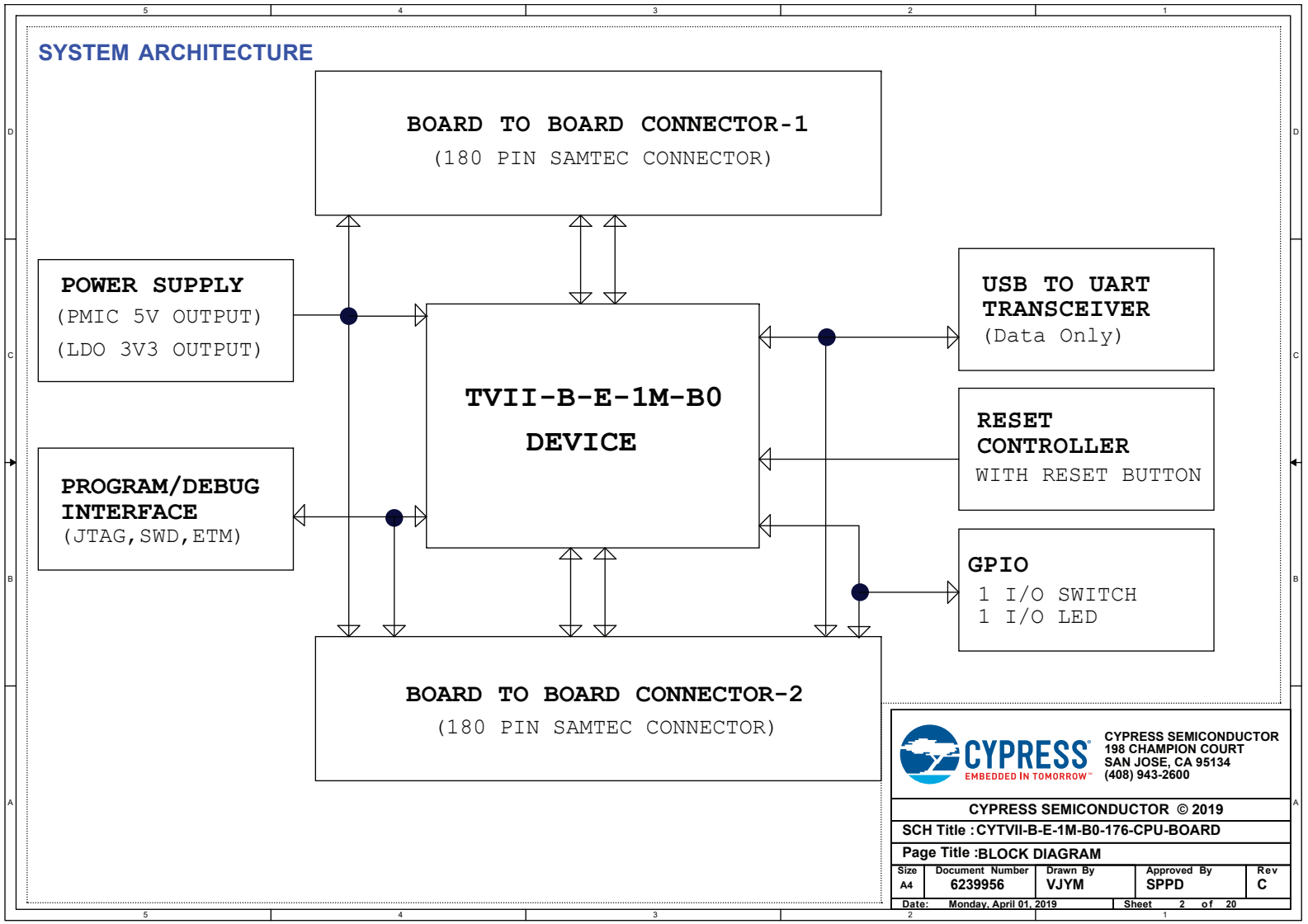


Figure A-2. Power Architecture

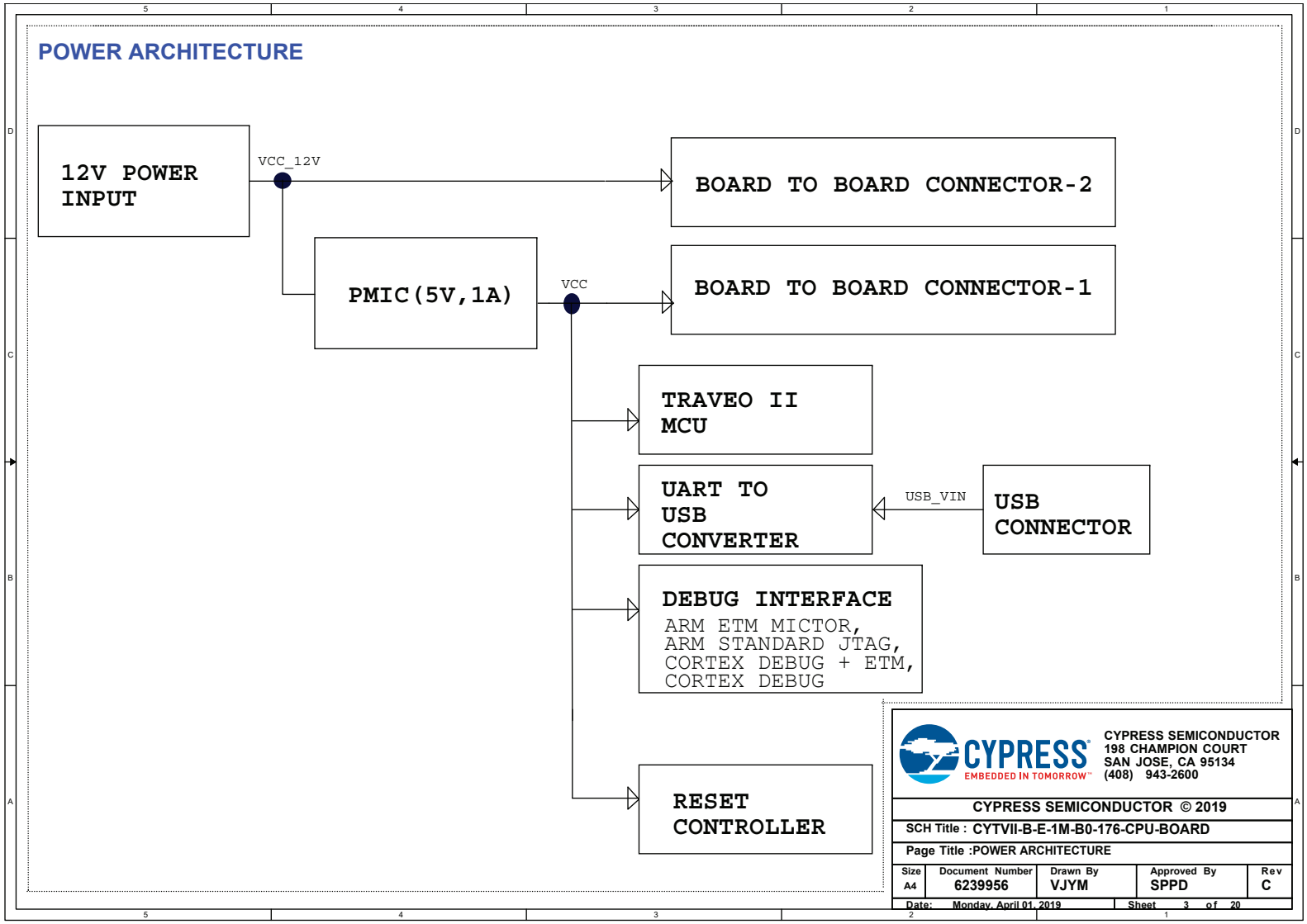


Figure A-3. 5V Power Input

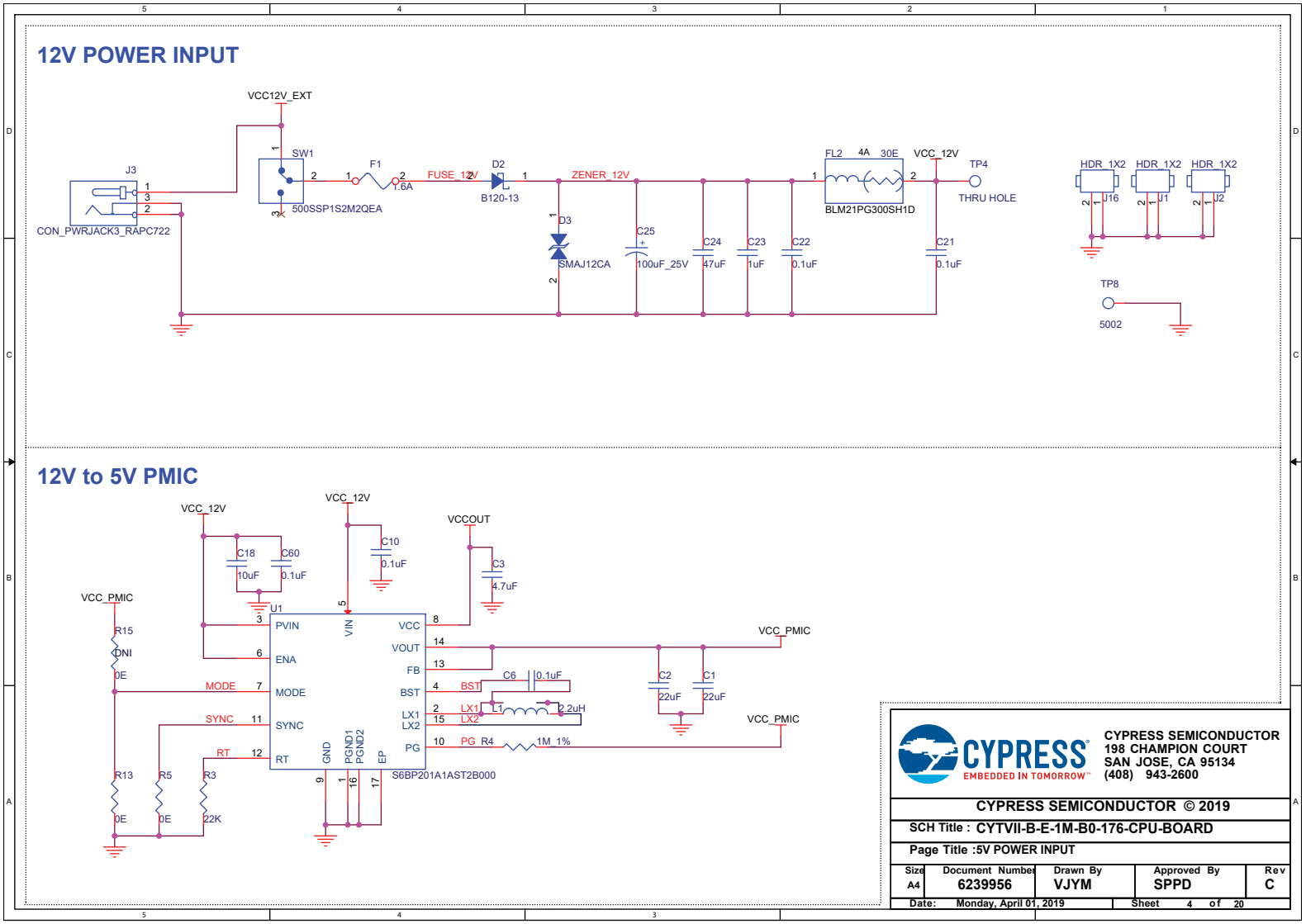


Figure A-4. 3V3 LDO Regulator

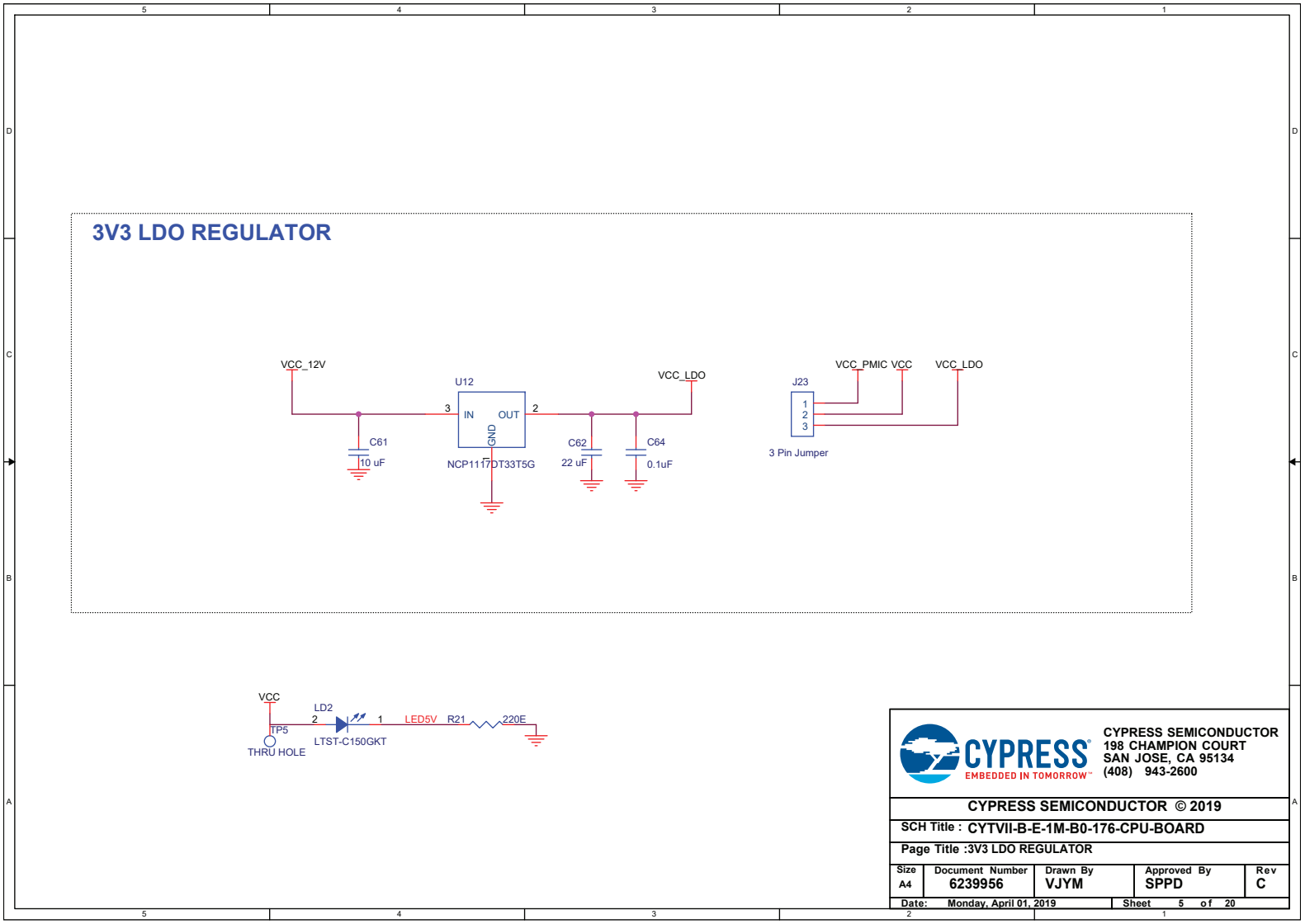


Figure A-5. Debug Interface

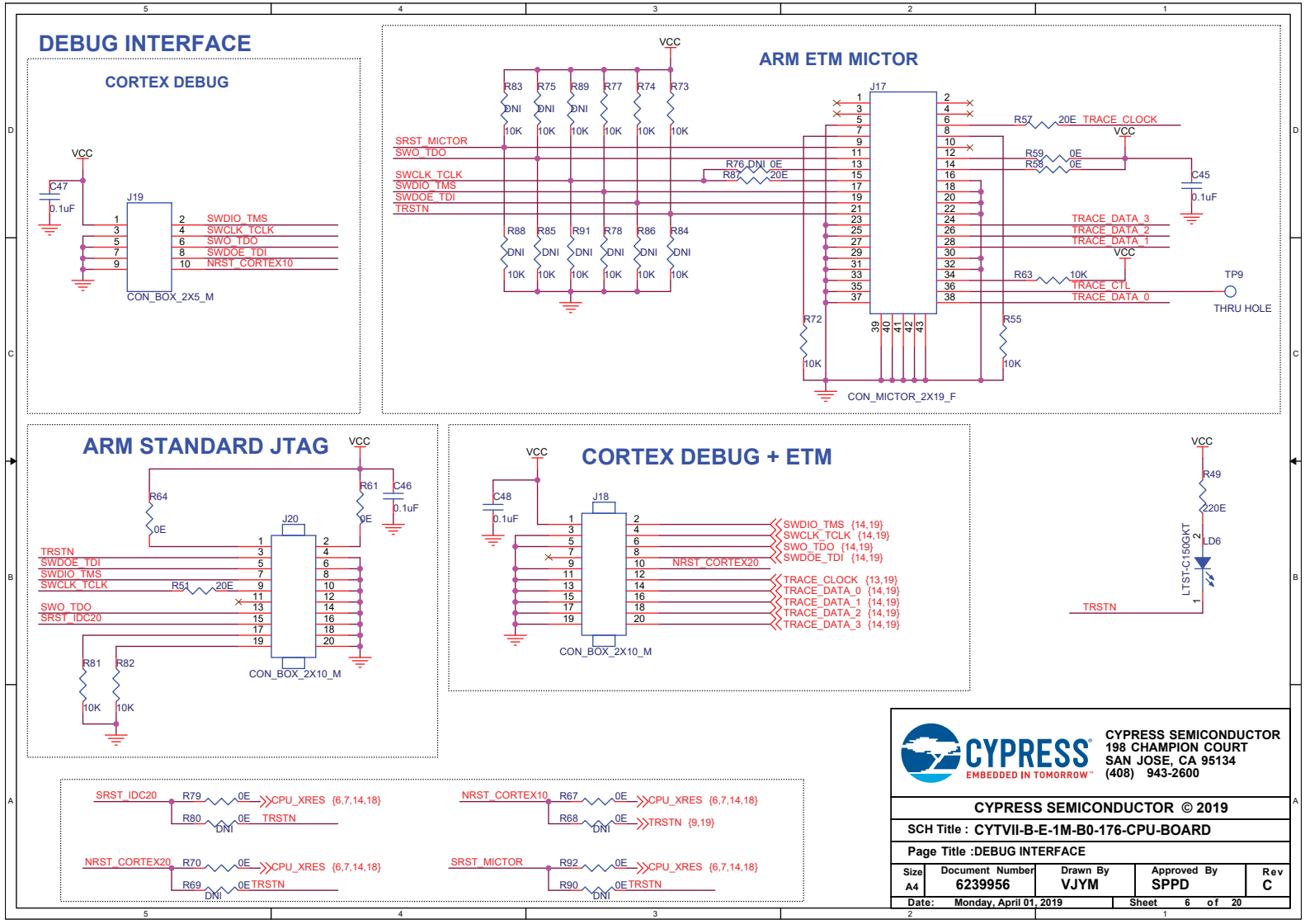


Figure A-6. UART to USB & RESERT

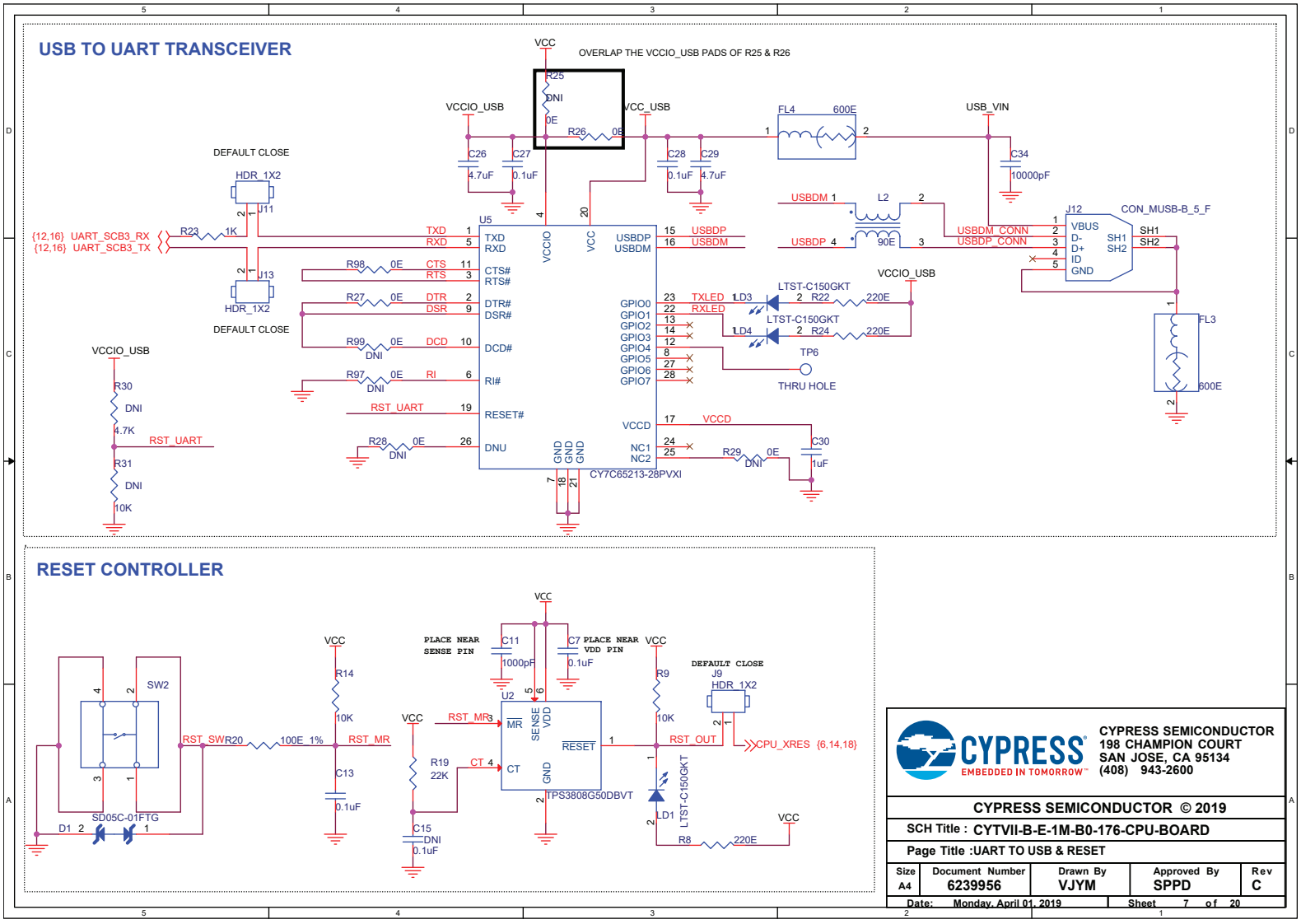


Figure A-7. GPIO, Clock, and Filter

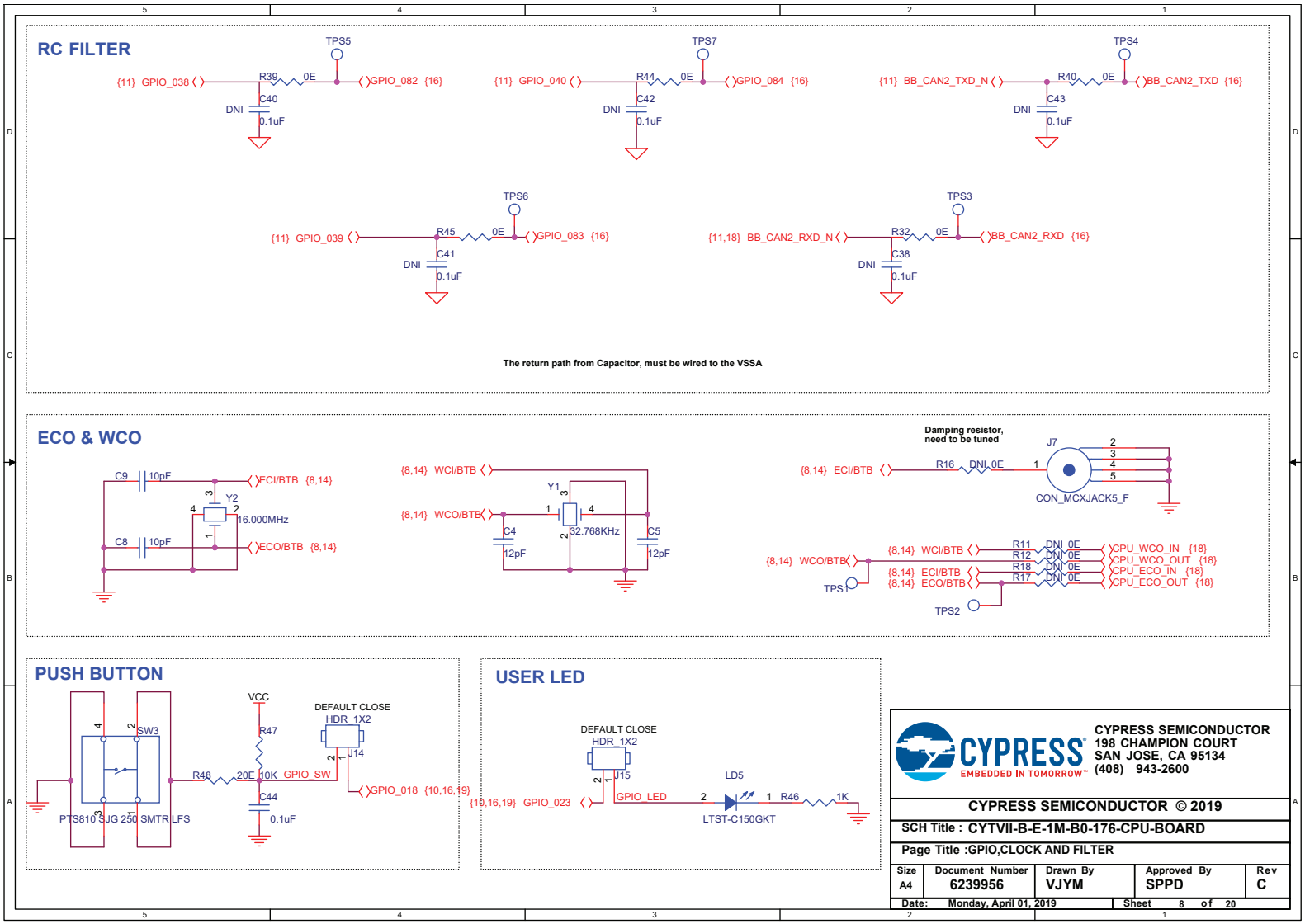


Figure A-8. LQFP-176 P1

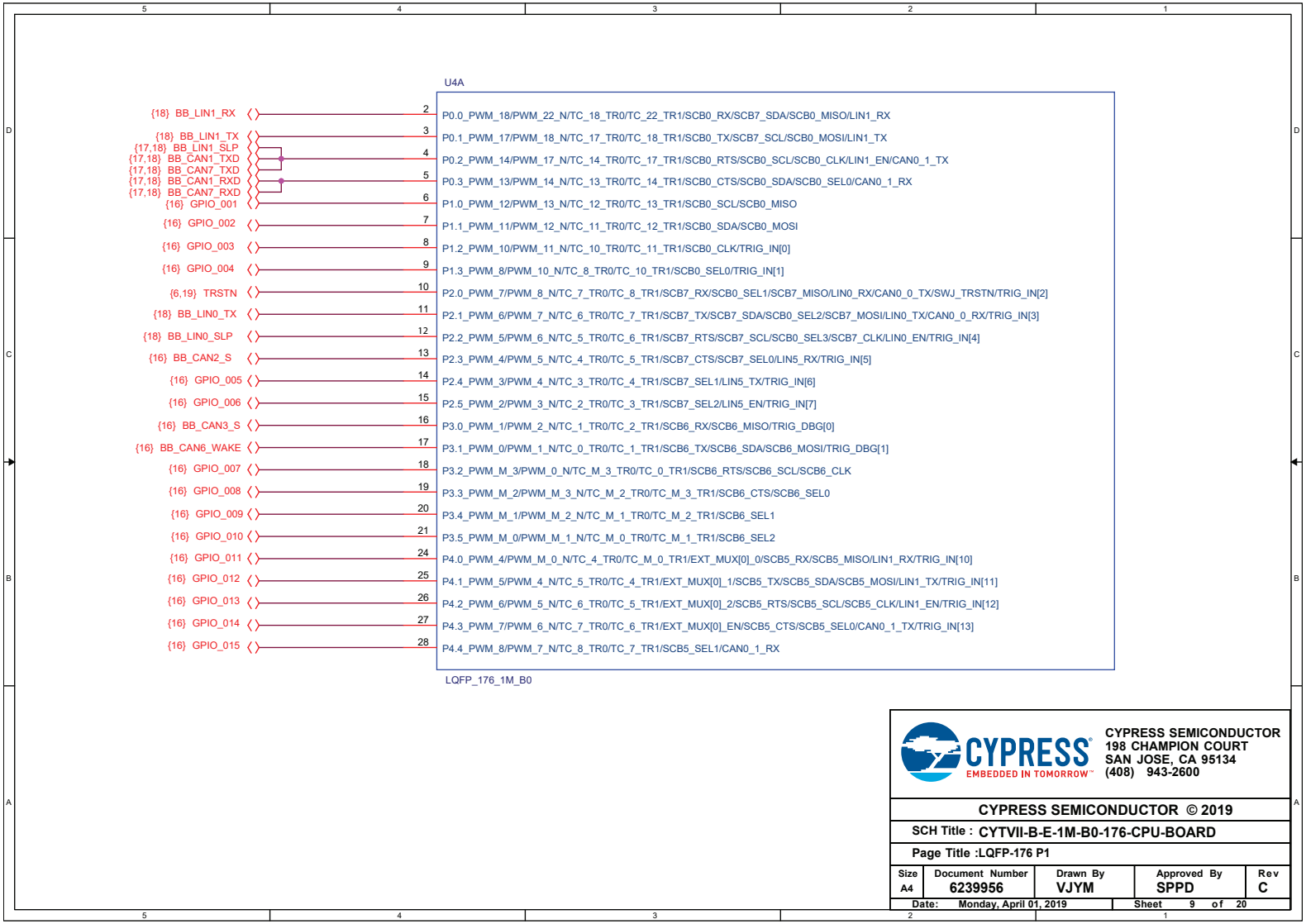


Figure A-9. LQFP-176 P2

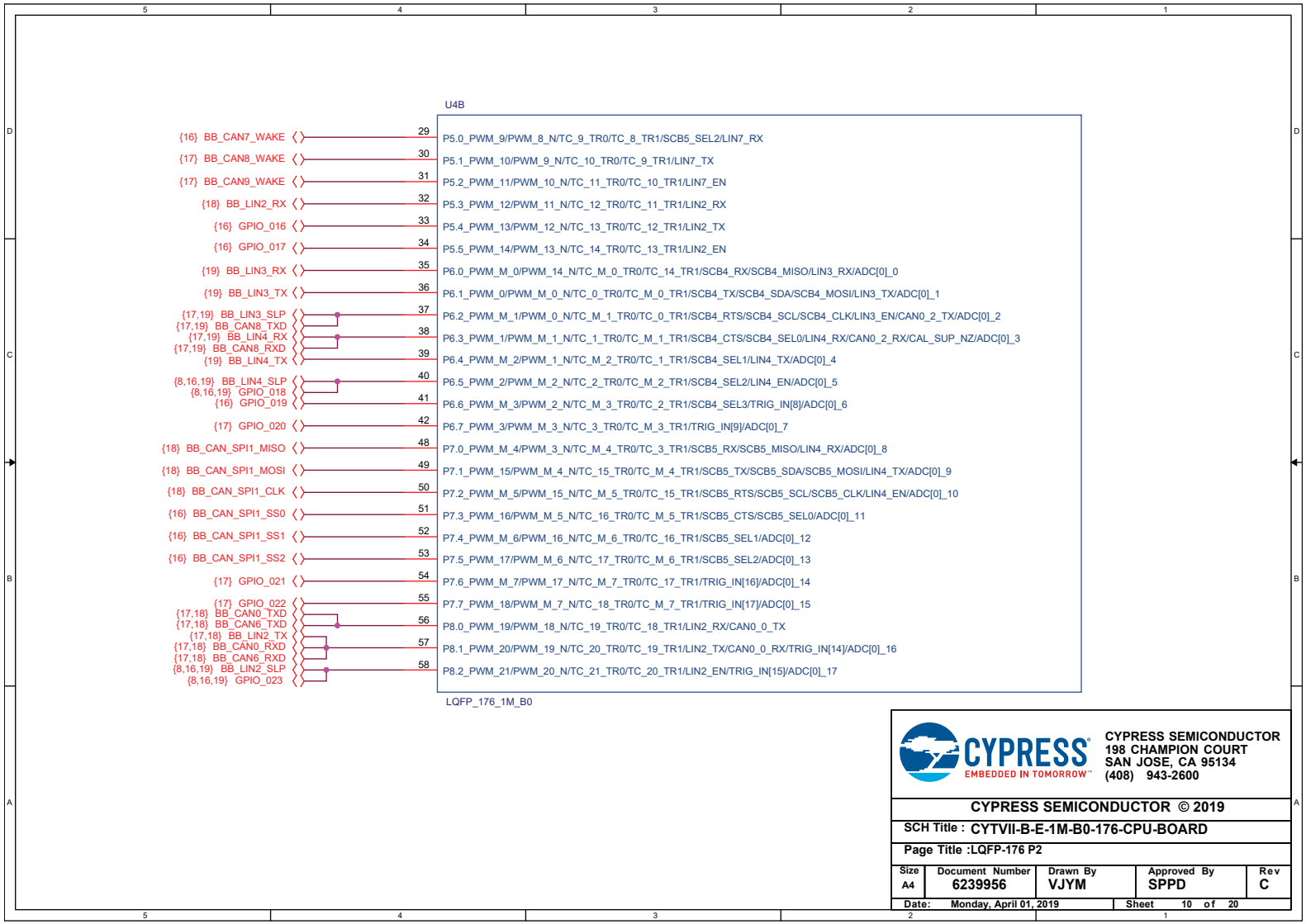


Figure A-10. LQFP-176 P3

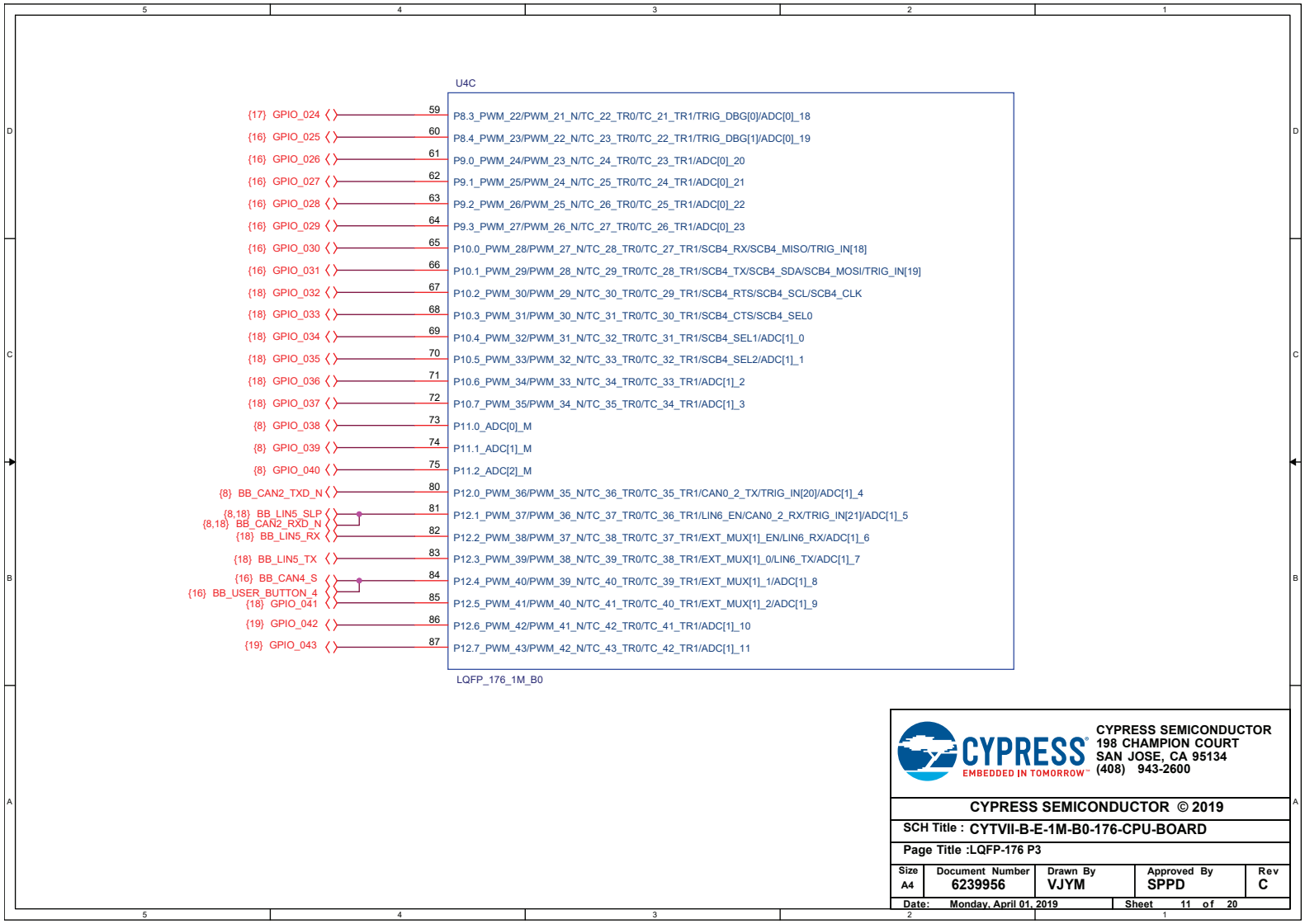


Figure A-11. LQFP-176 P4

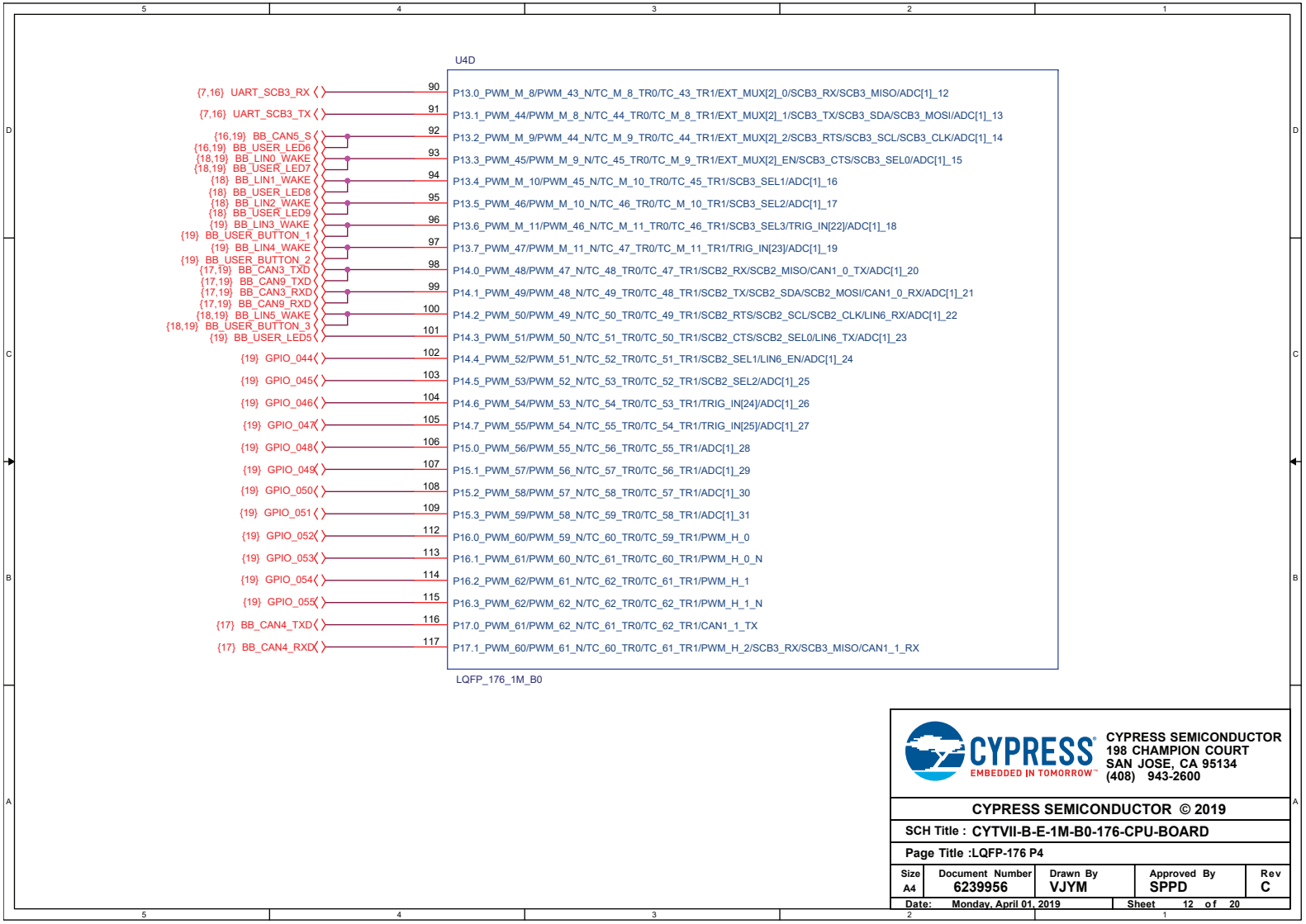


Figure A-12. LQFP-176 P5

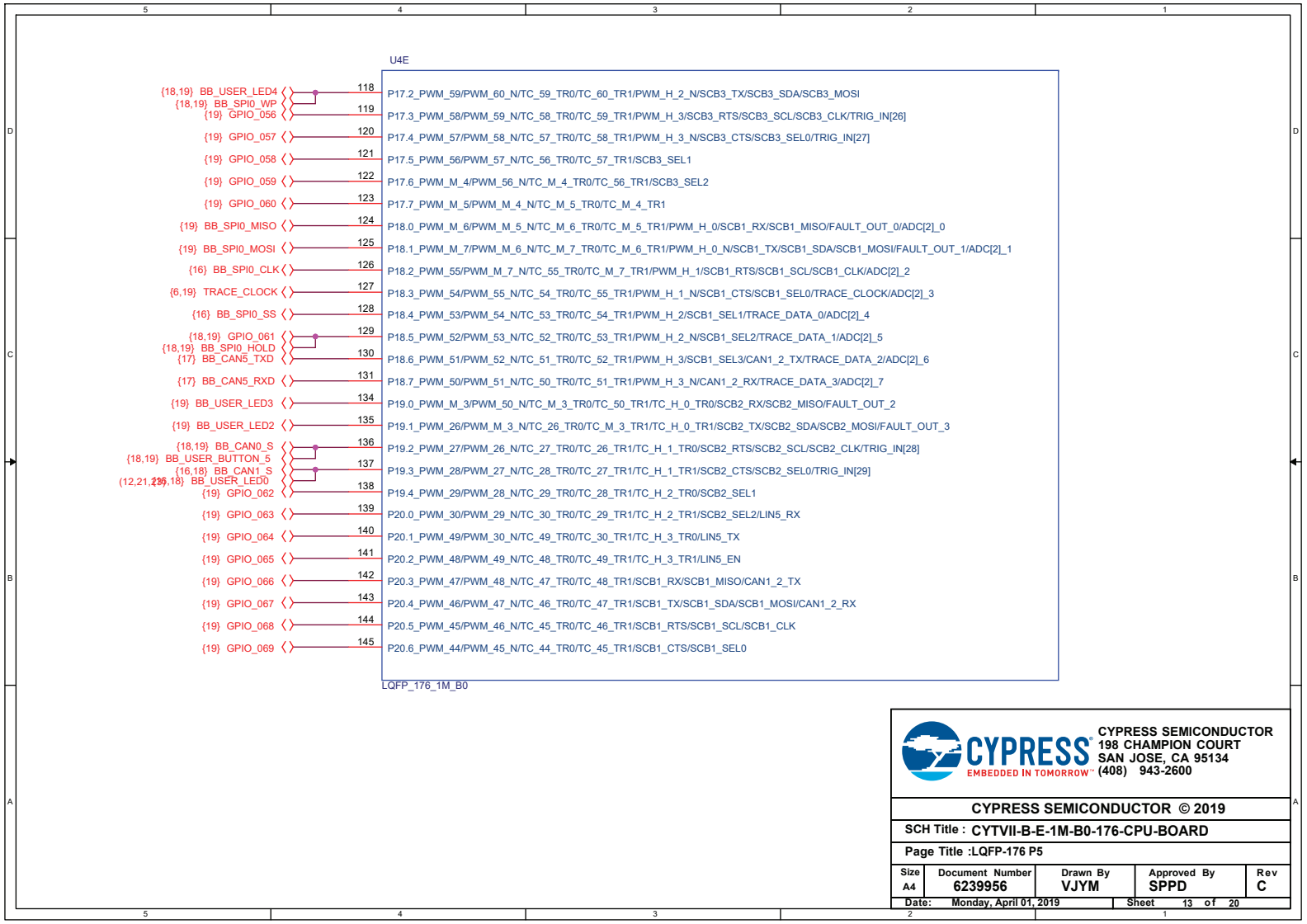


Figure A-13. LQFP-176 P6

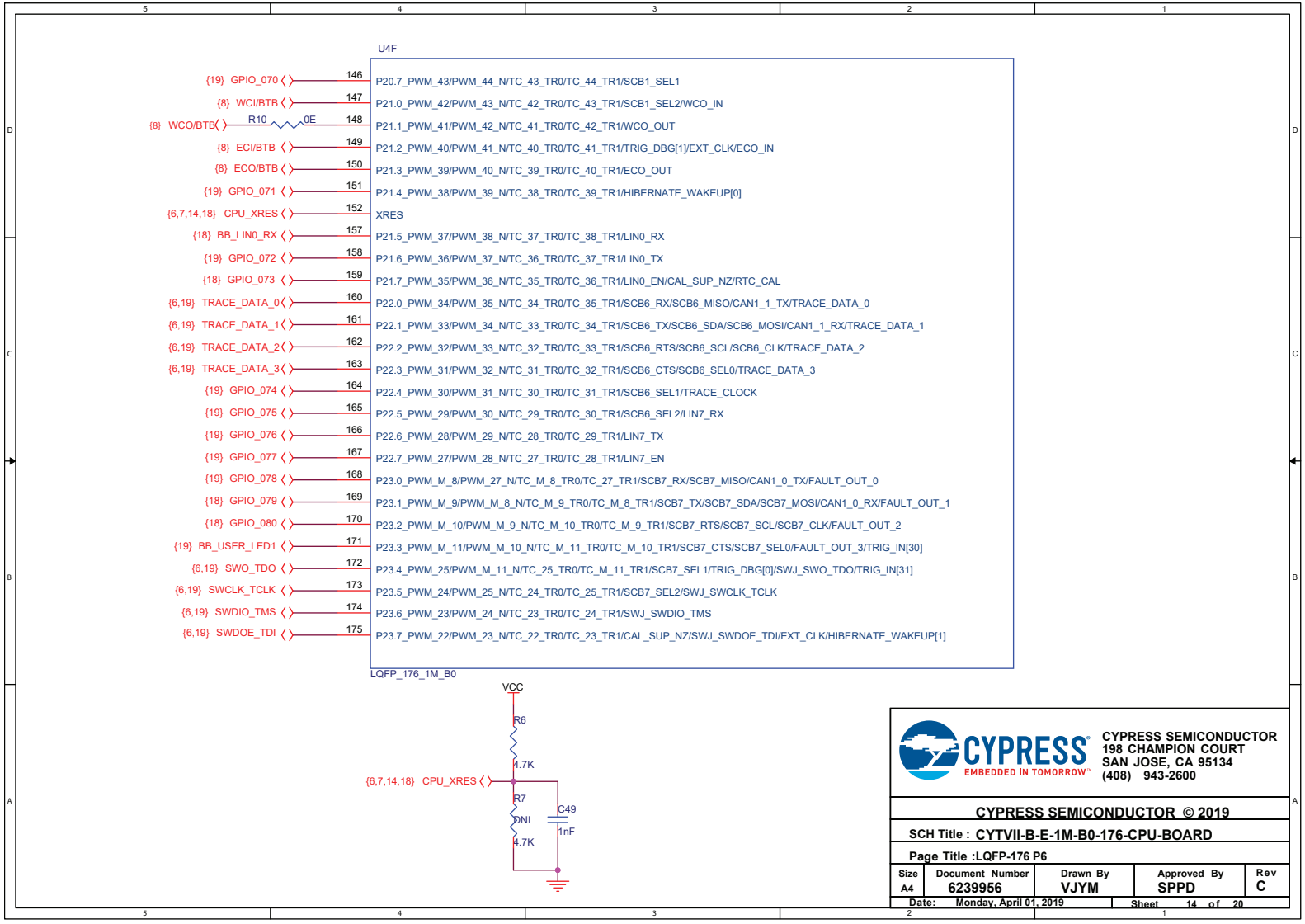


Figure A-14. LQFP-176 P7

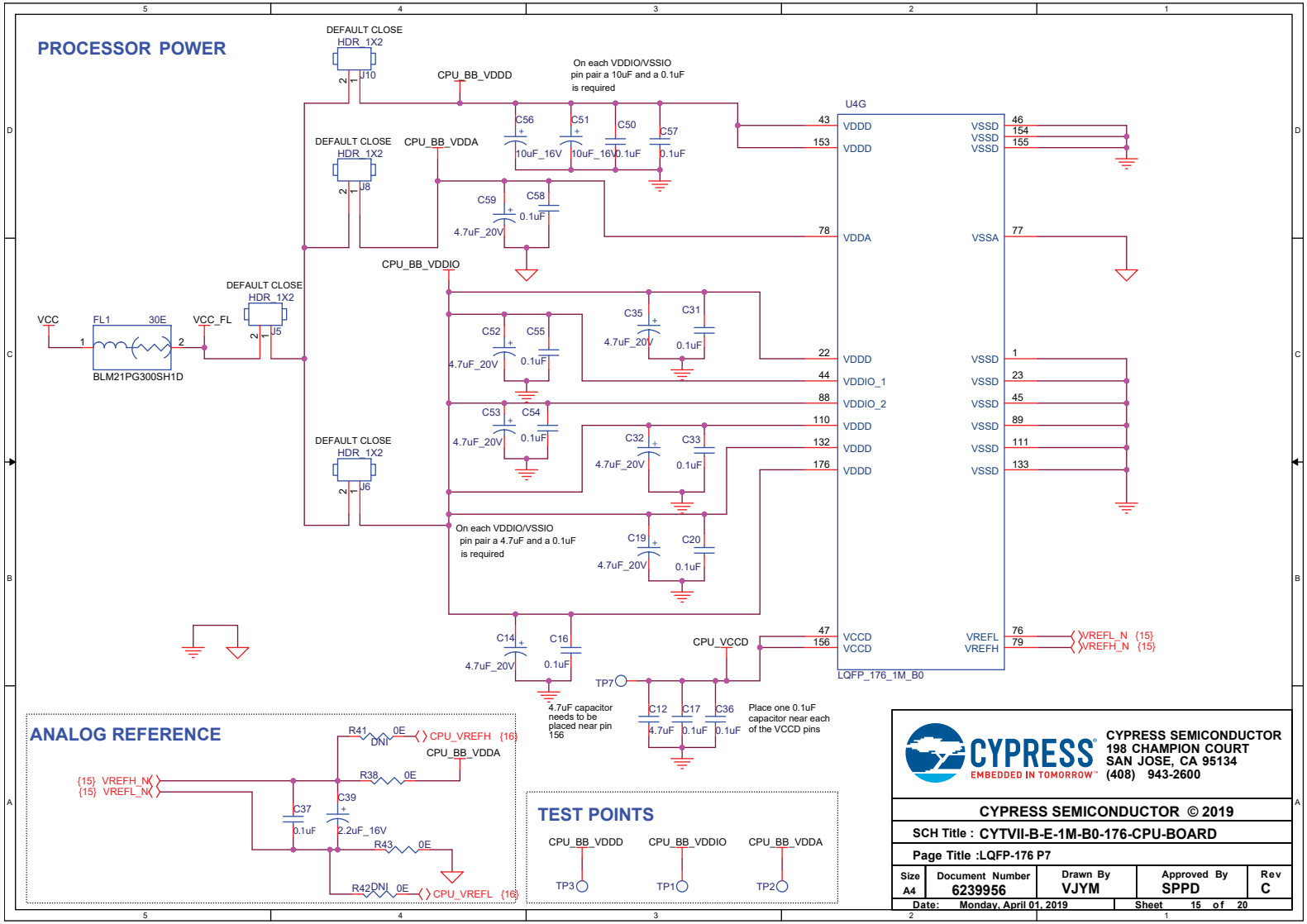


Figure A-15. Board to Board Connector- J22A

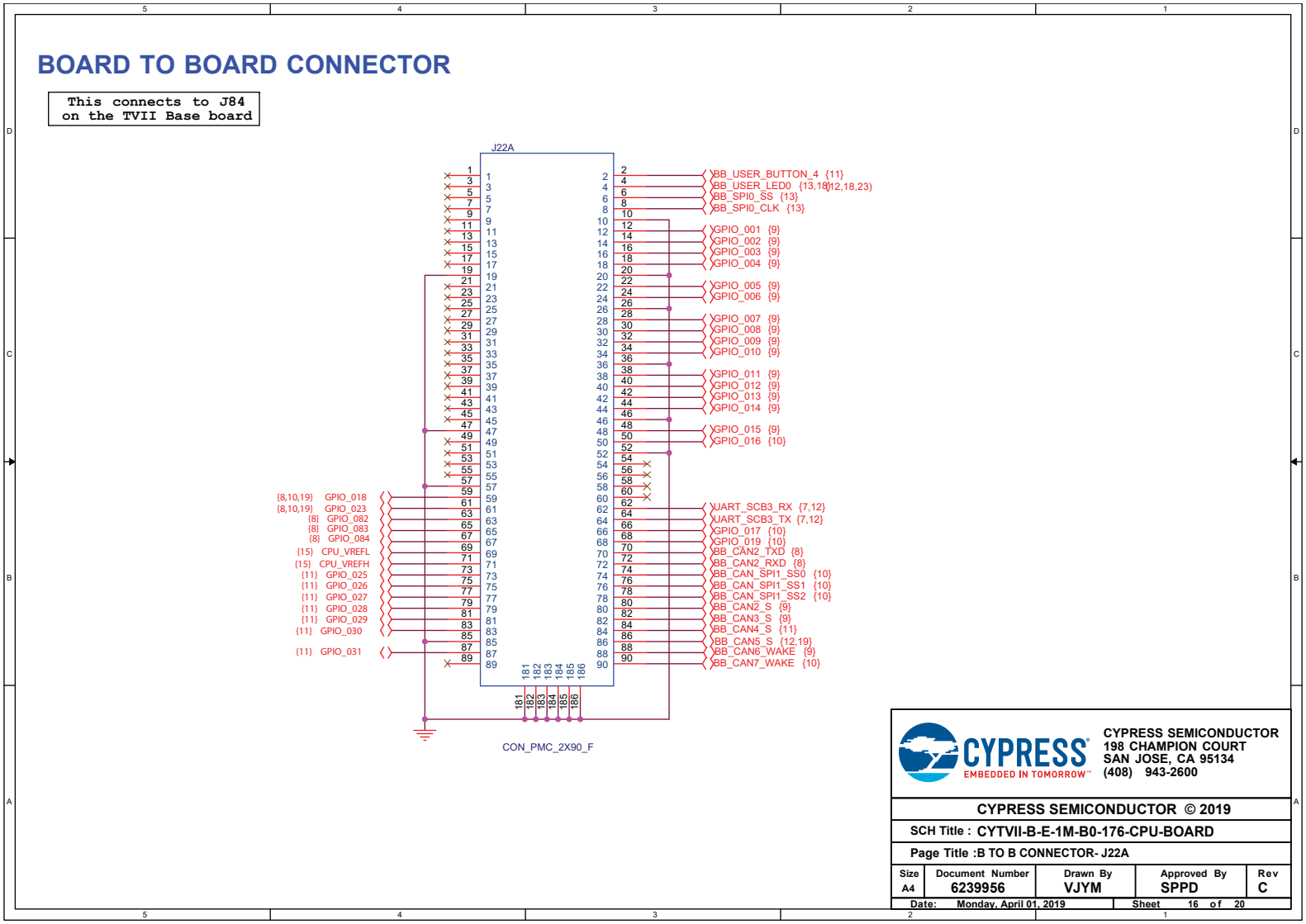


Figure A-16. Board to Board Connector- J22B

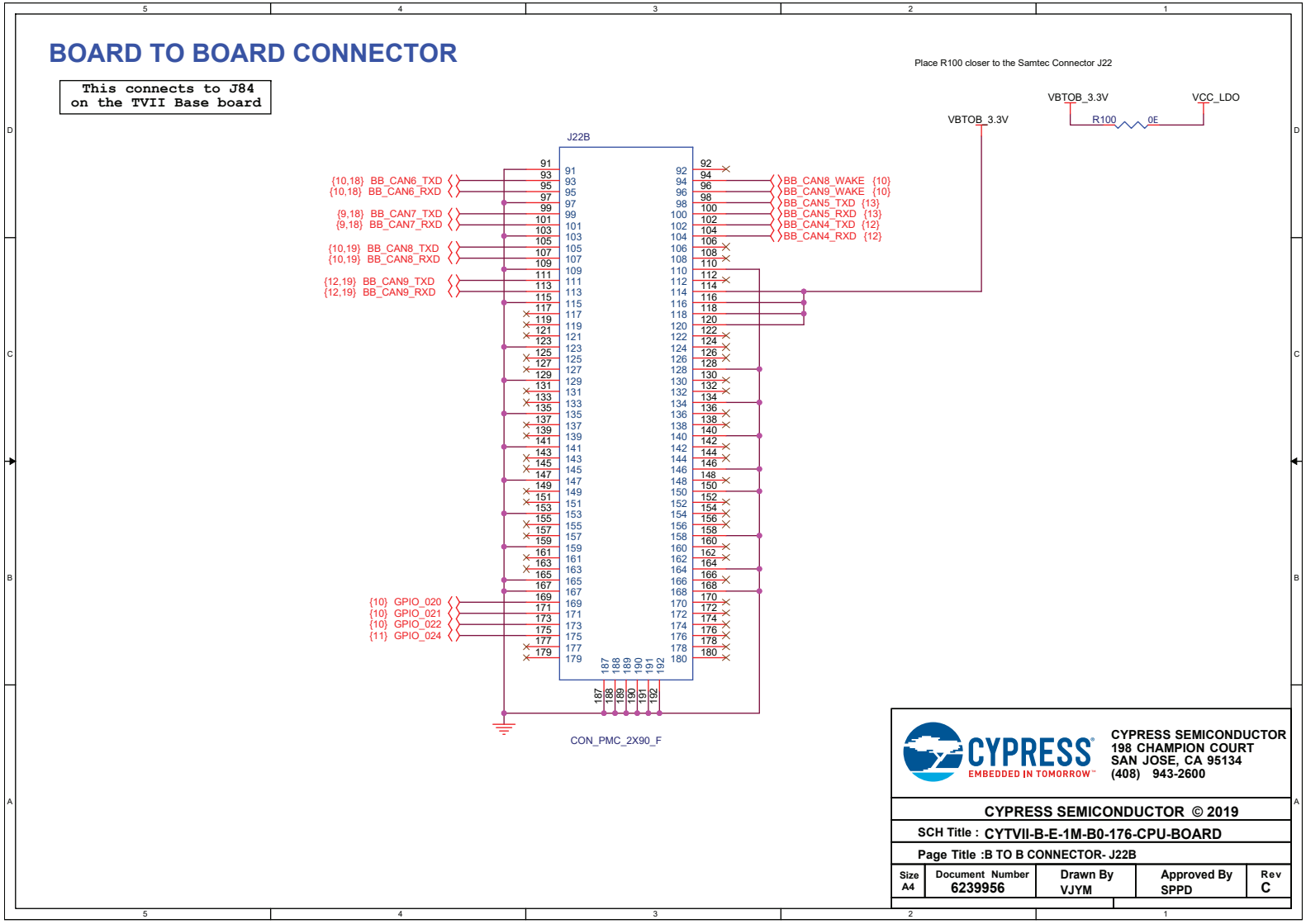


Figure A-17. Board to Board Connector- J21A

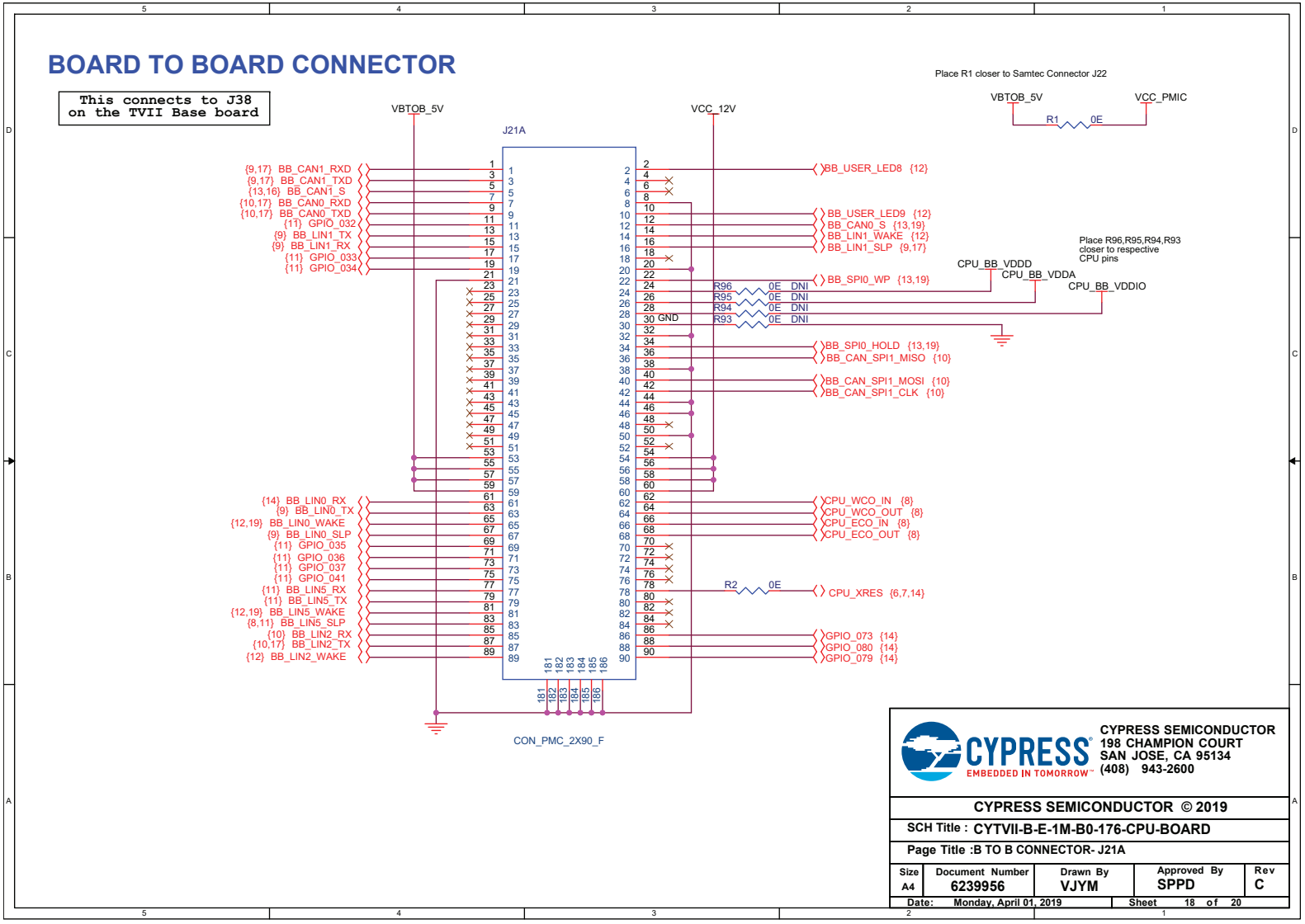
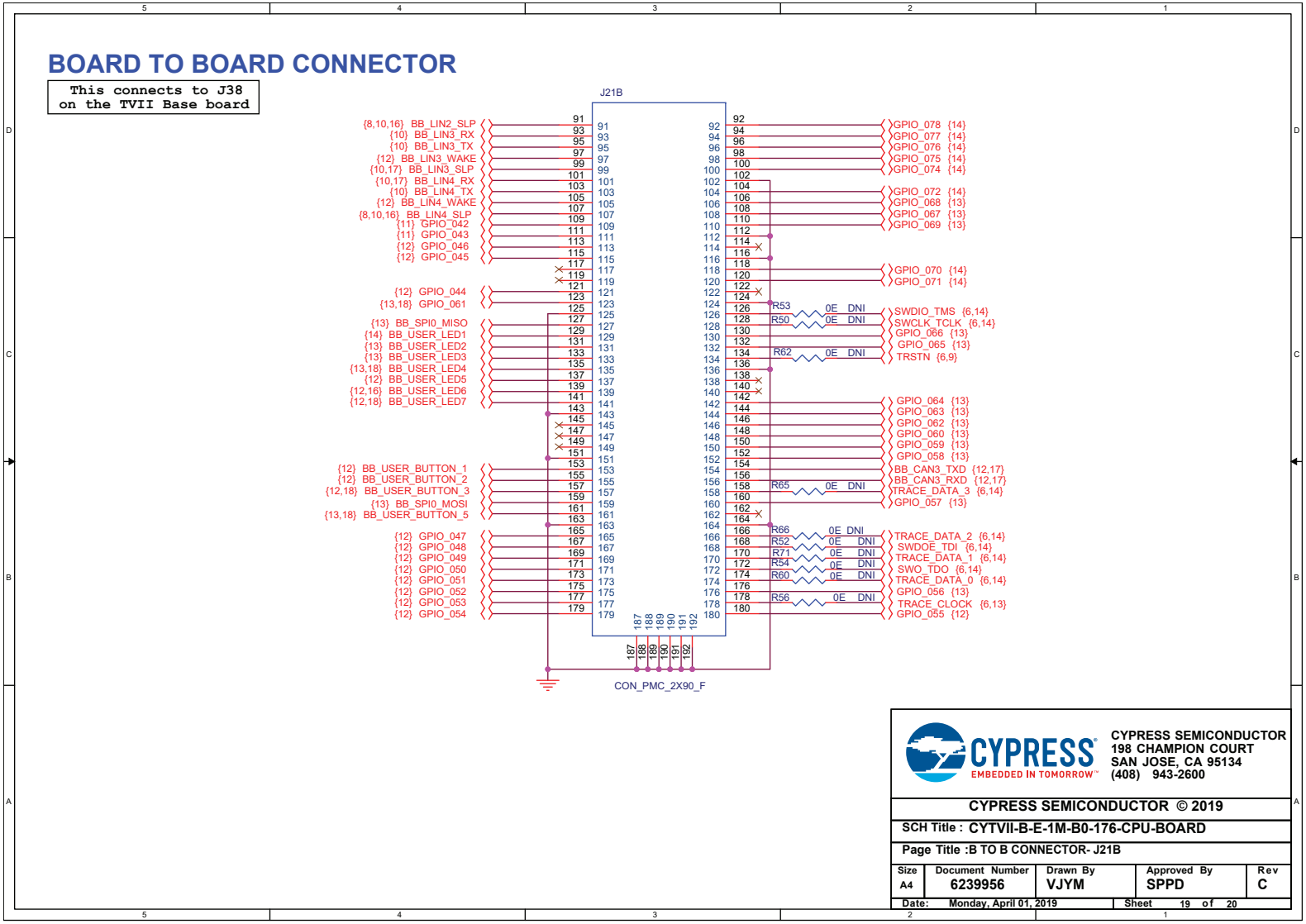


Figure A-18. Board to Board Connector- J21B



B. Component Assembly on CPU Board

This appendix shows the top and bottom assembly of the PCB.

Figure B-1. Top Assembly of the PCB

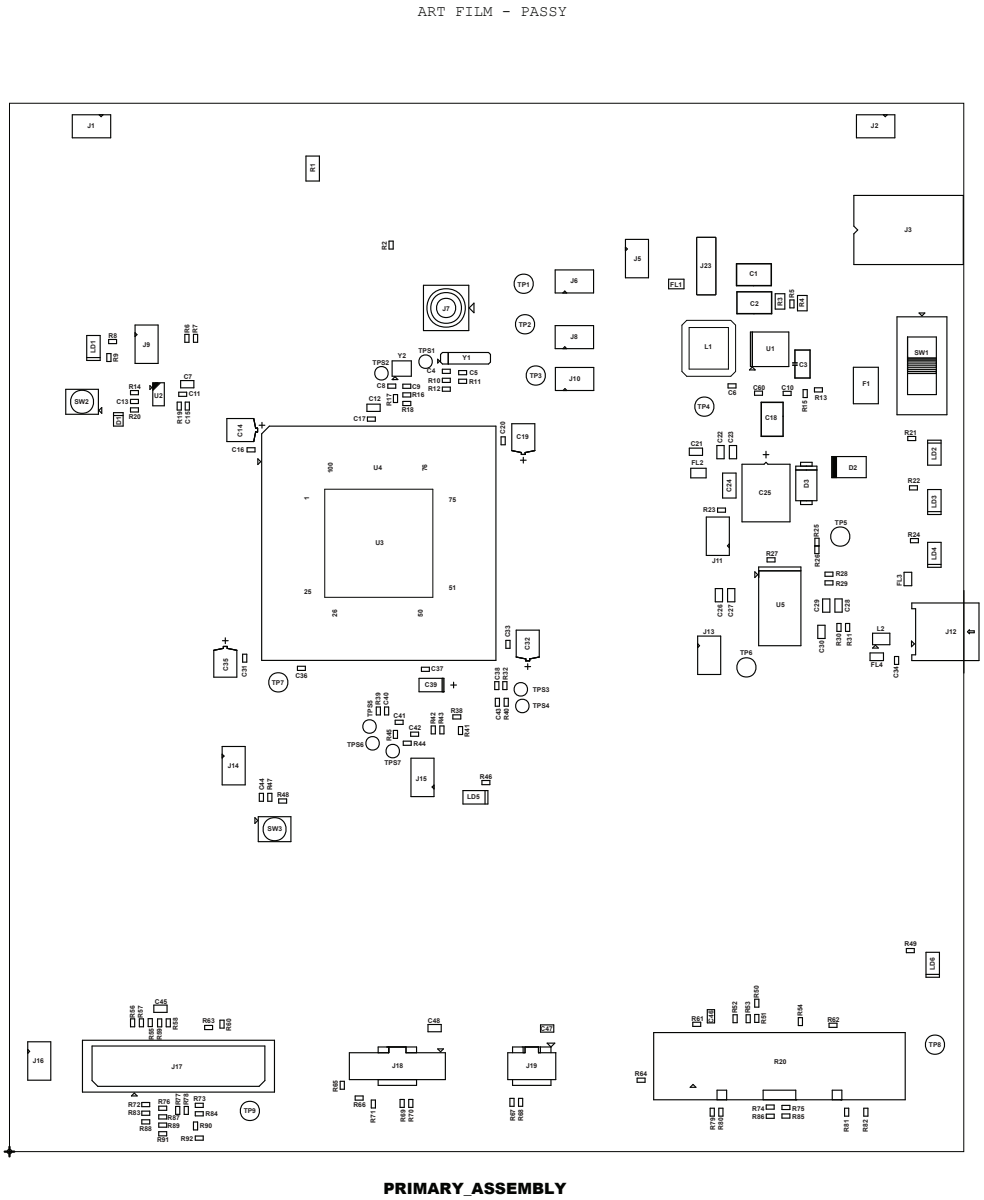
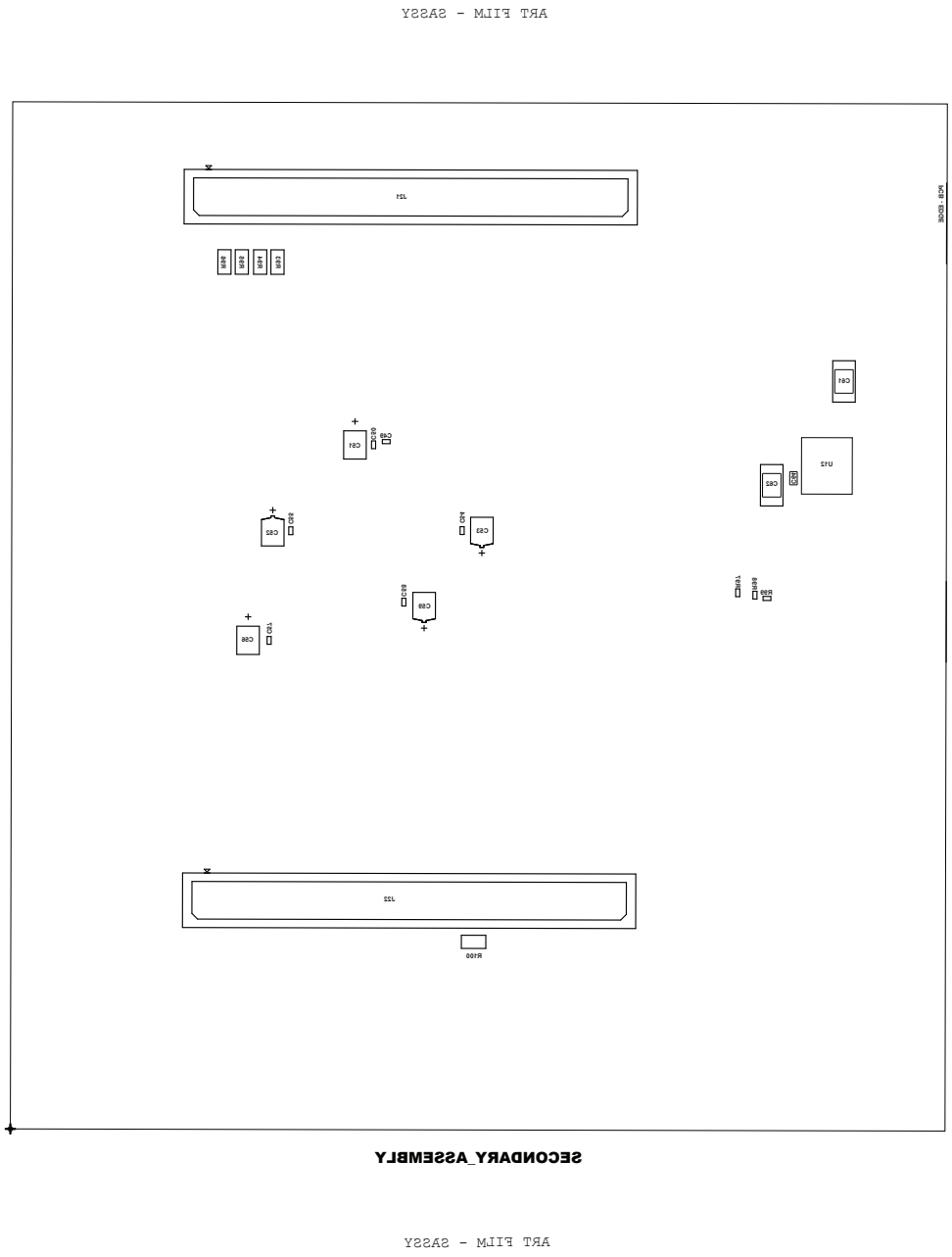


Figure B-2. Bottom Assembly of the PCB



C. Schematics of Base Board

This appendix contains the schematics of the Base board on which CPU Board is mounted.

Figure C-1. Block Diagram of Base Board

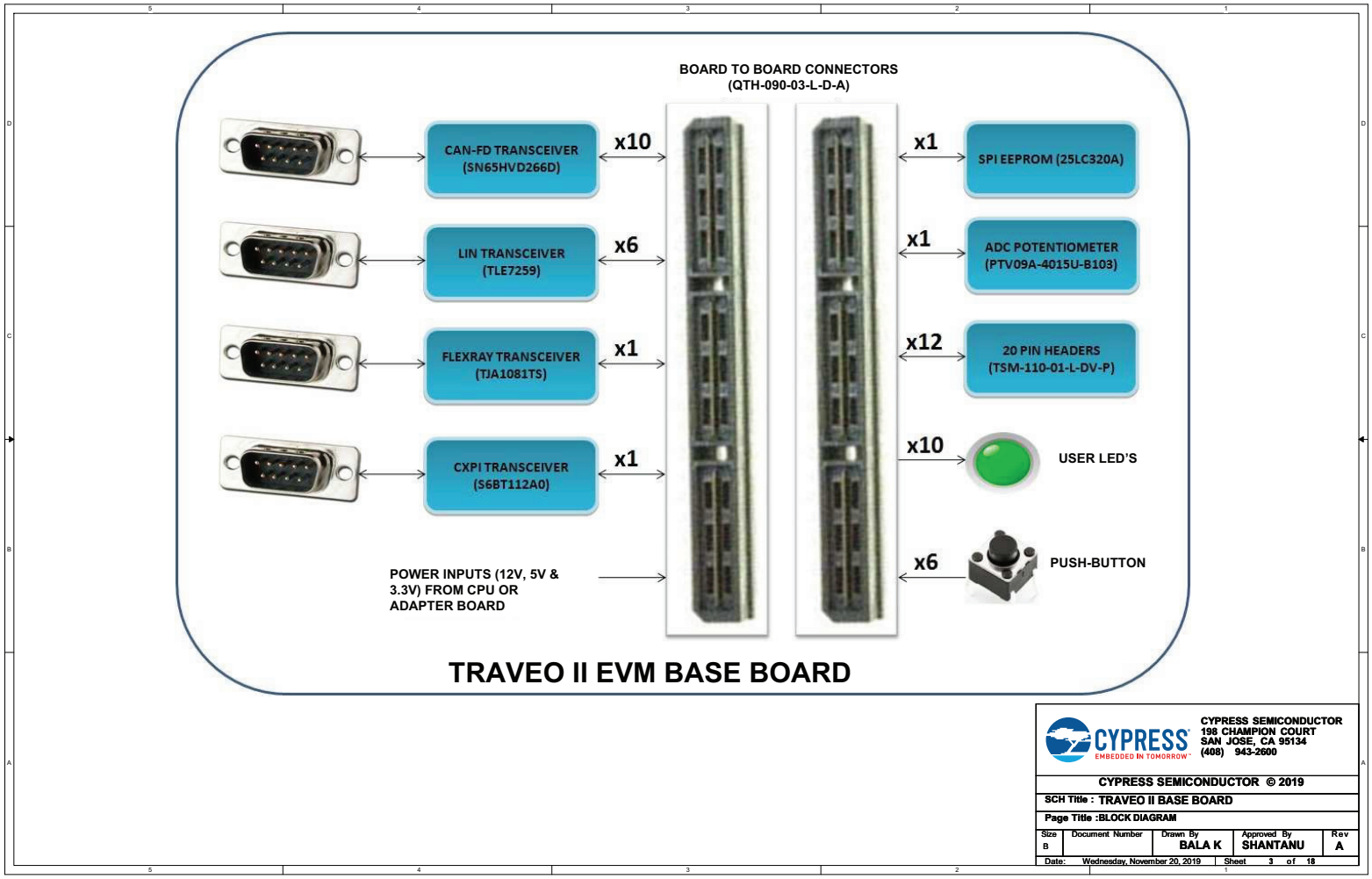


Figure C-2. BTOB Connector-01

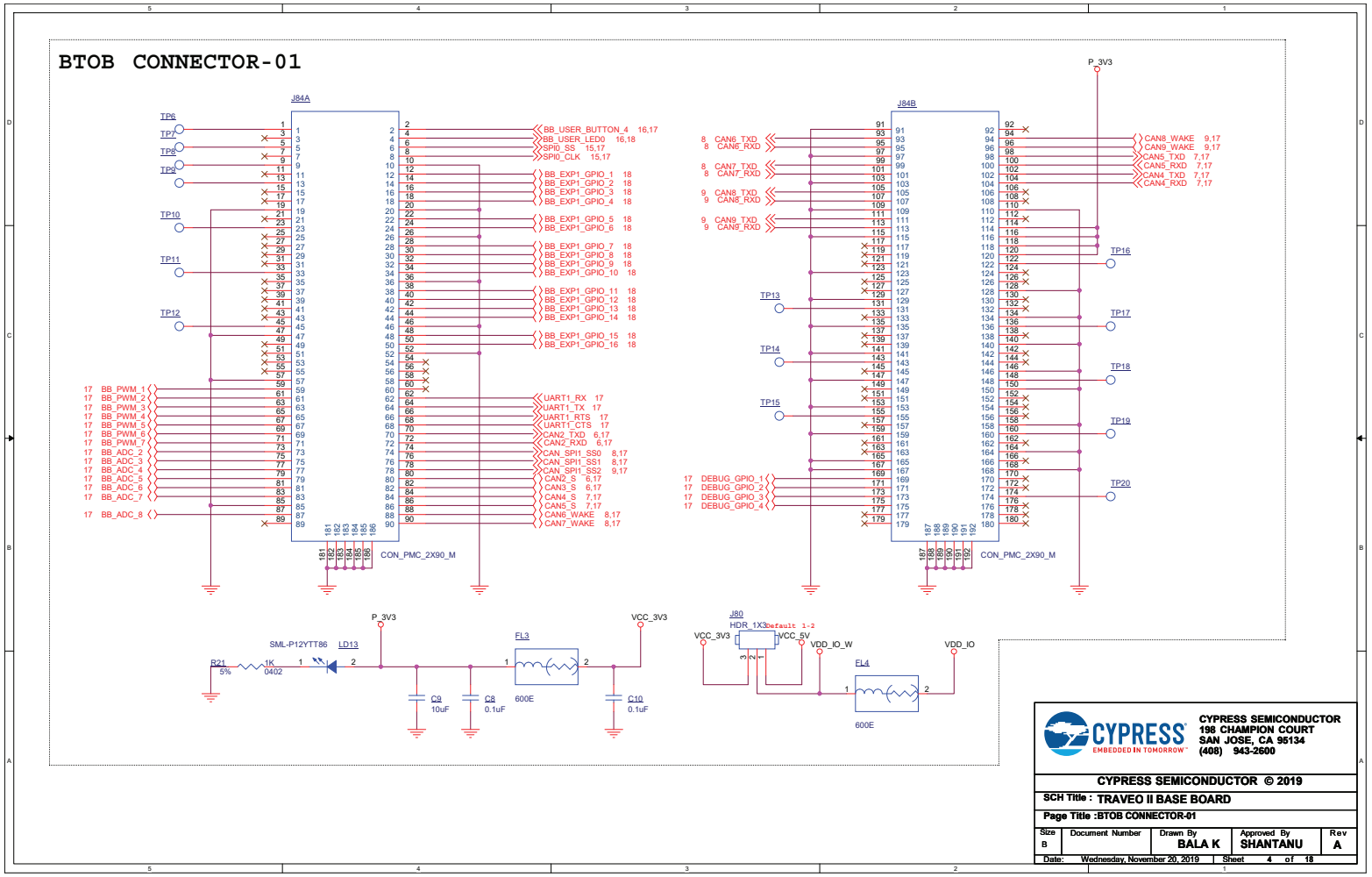


Figure C-3. BTOB Connector-02

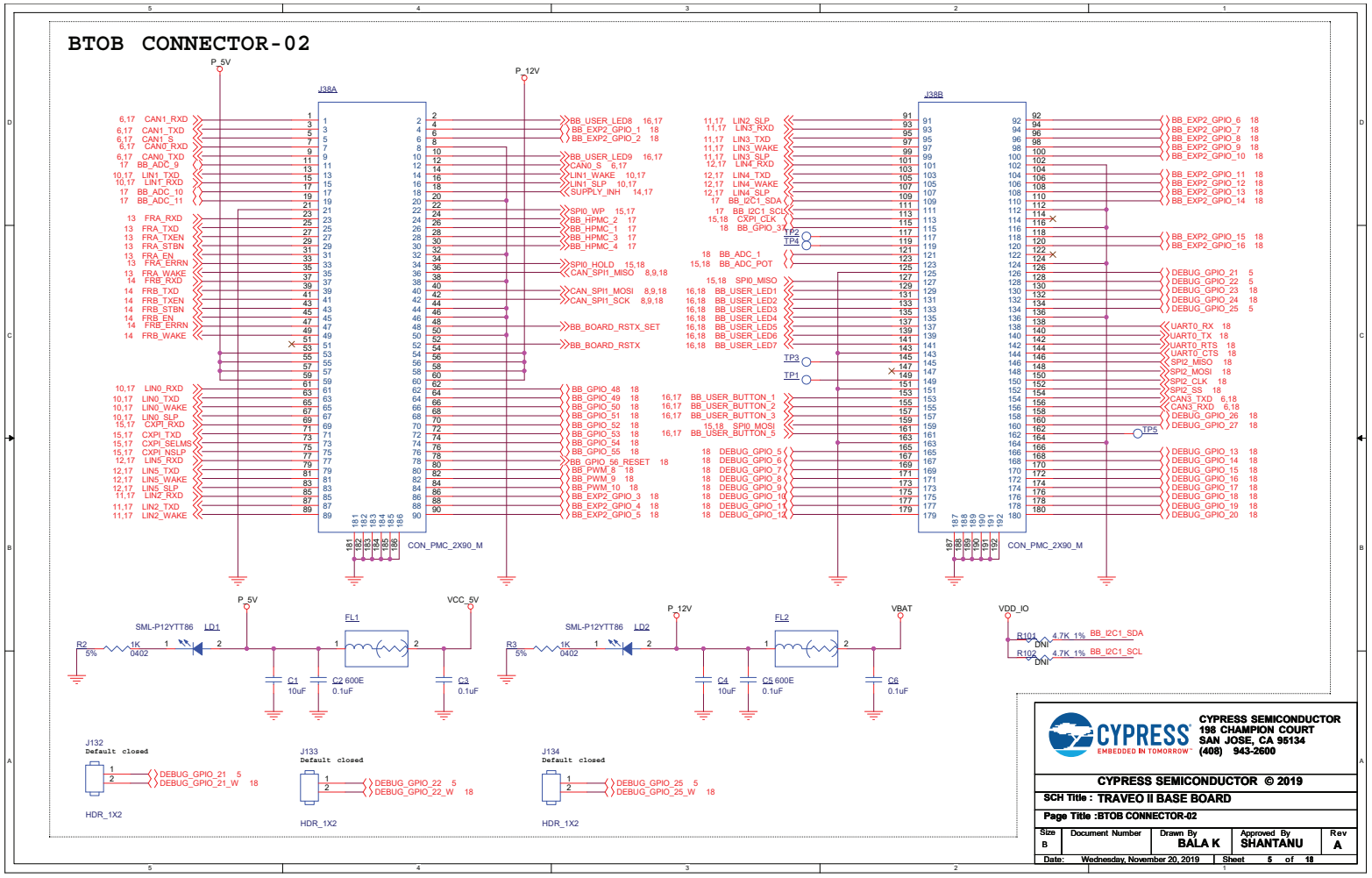


Figure C-4. CAN-FD_0 to 3

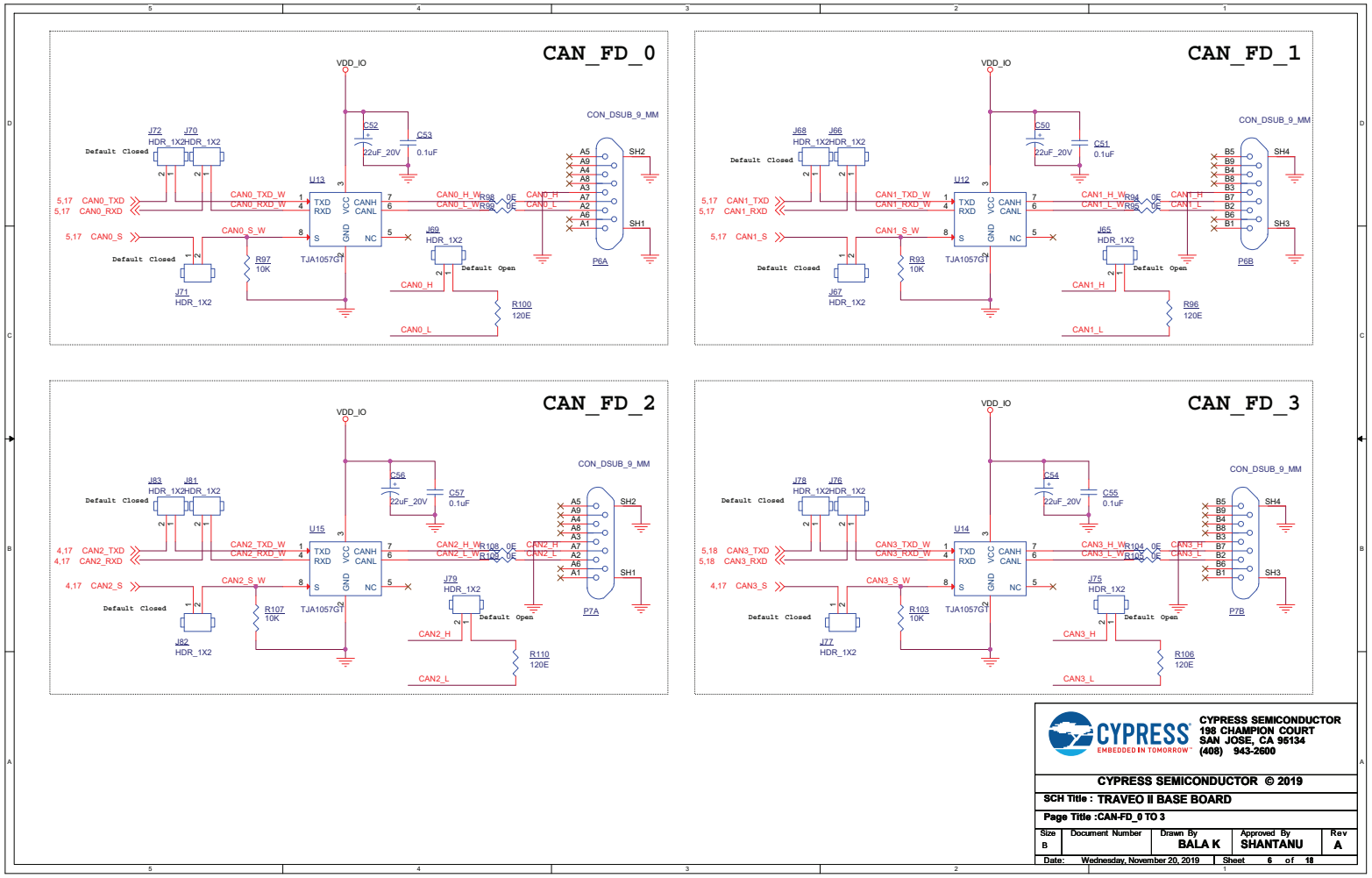


Figure C-5. CAN-FD_4 to 7

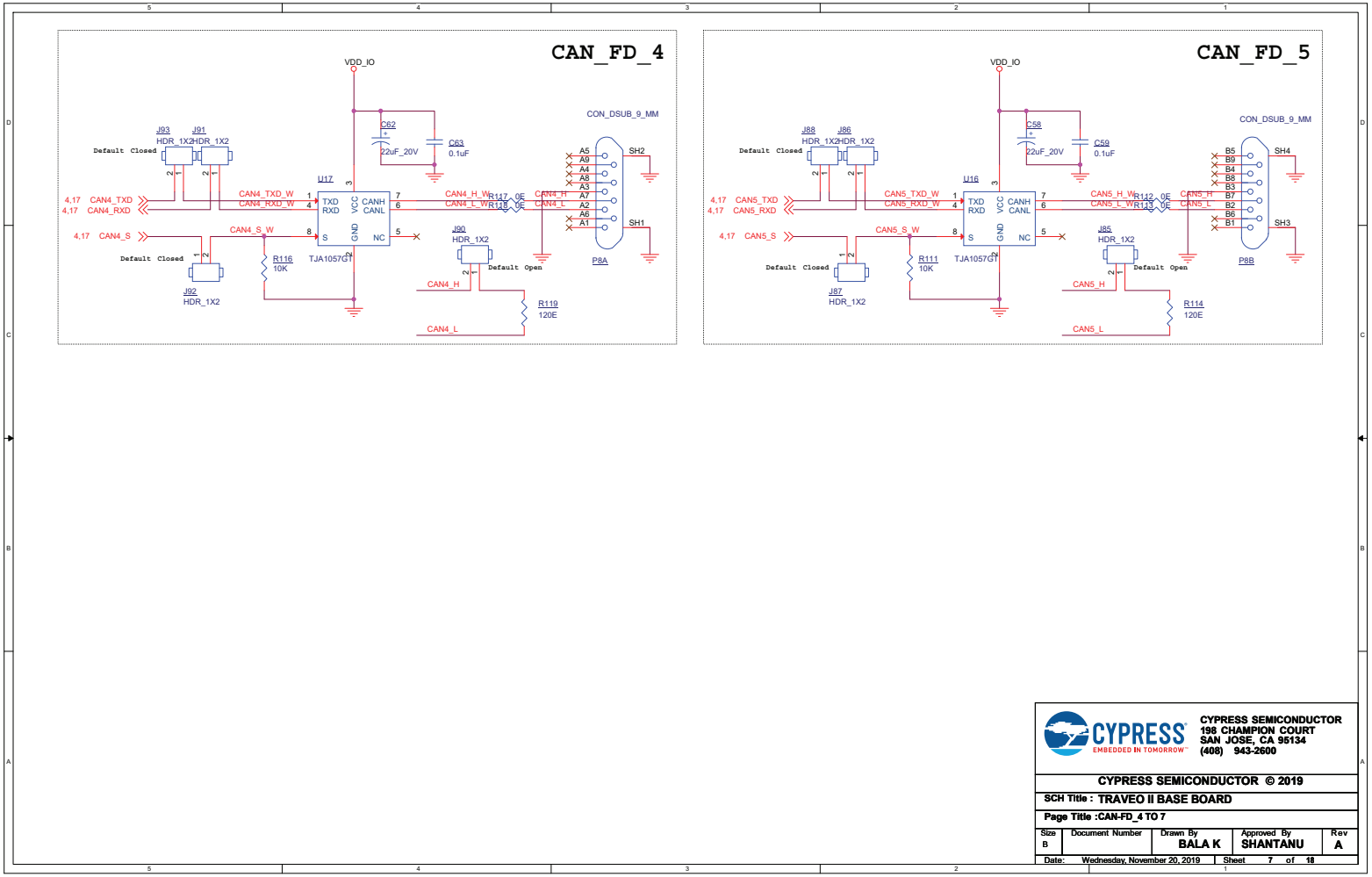


Figure C-6. CAN-FD_6 & 7

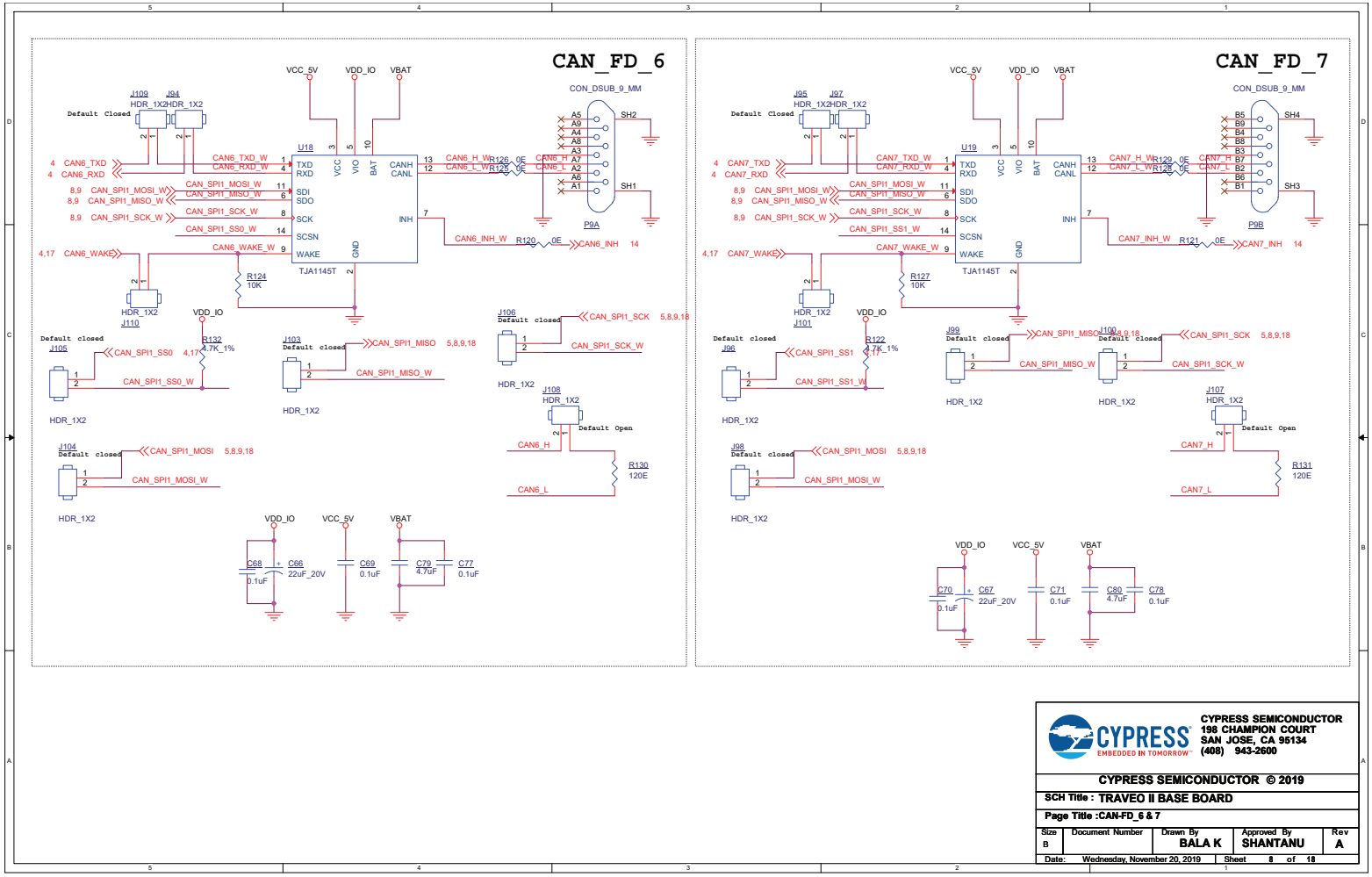


Figure C-7. CAN-FD_8 & 9

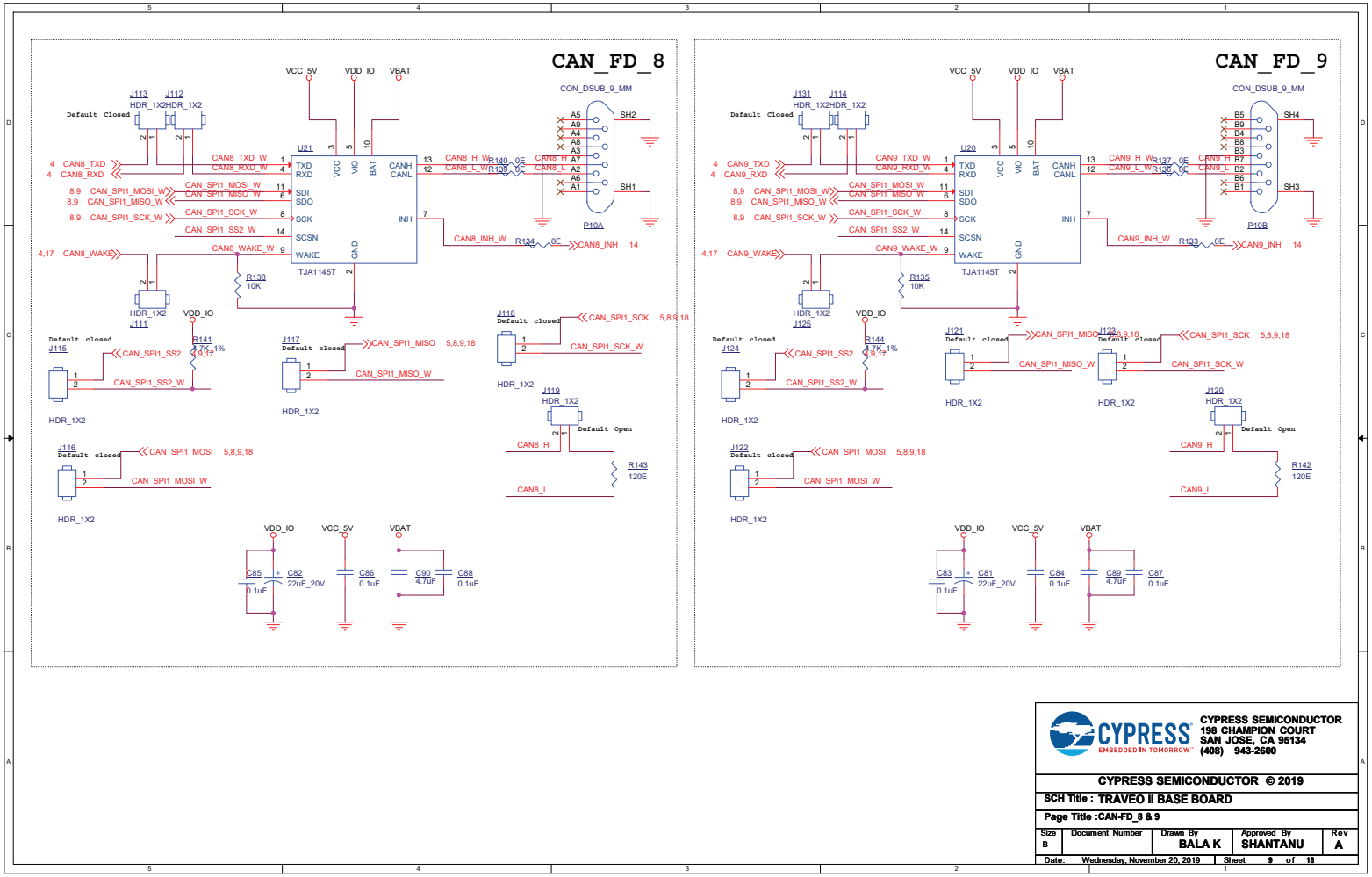


Figure C-8. LIN INTERFACE_0 to 1

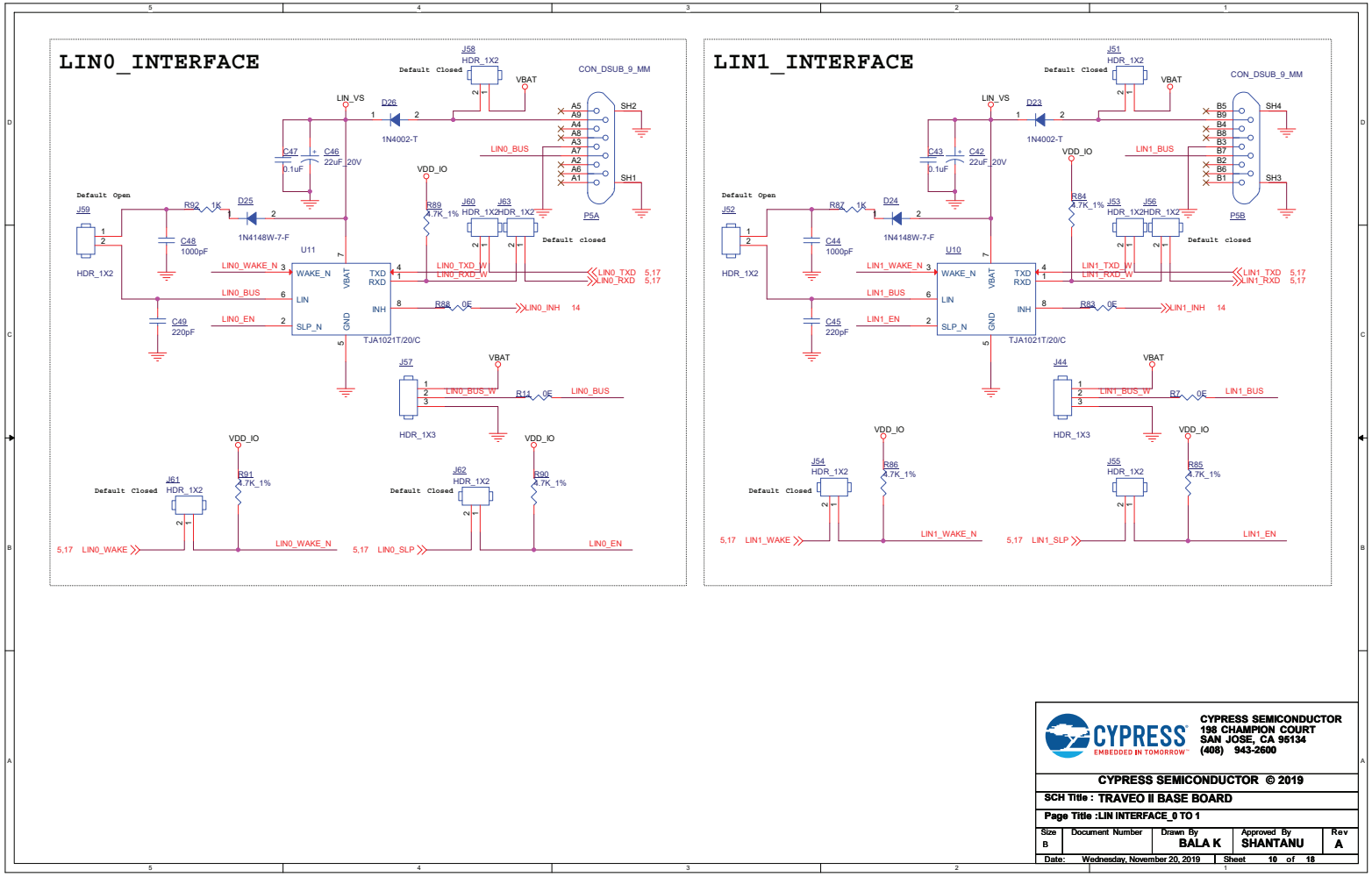


Figure C-9. LIN INTERFACE_2 to 3

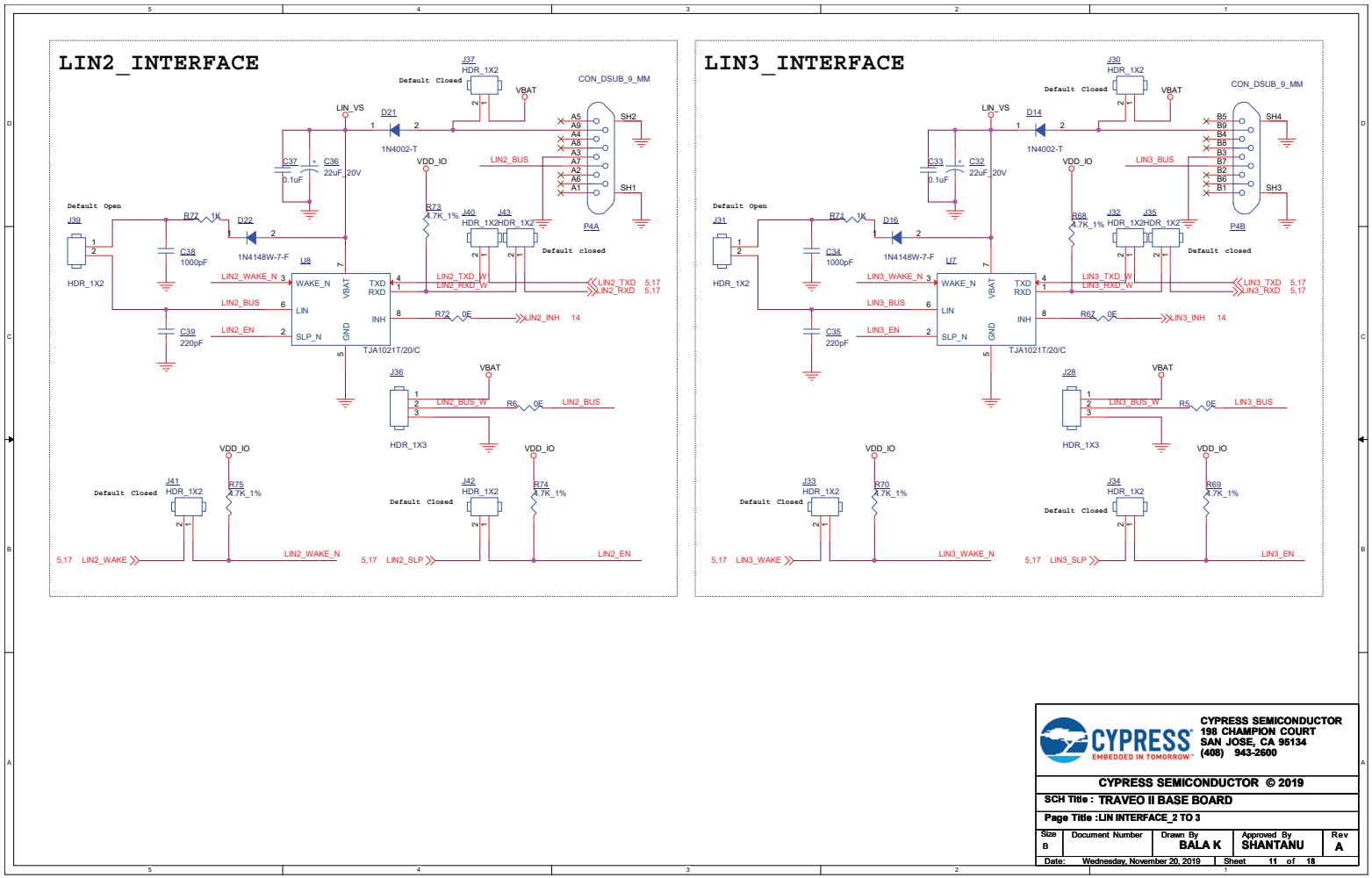


Figure C-10. LIN INTERFACE_4 to 5

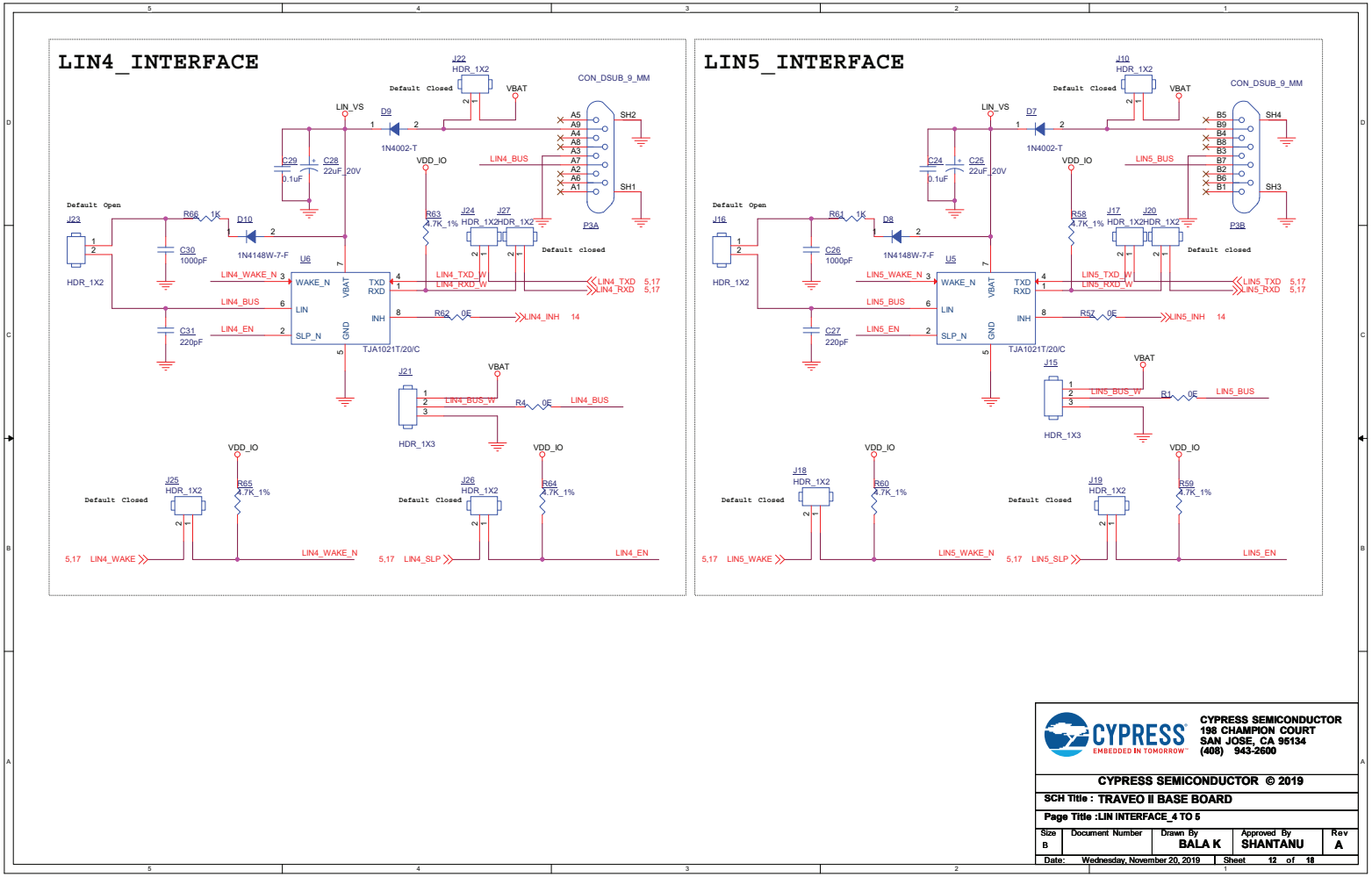


Figure C-11. Flexray-01 & RESET

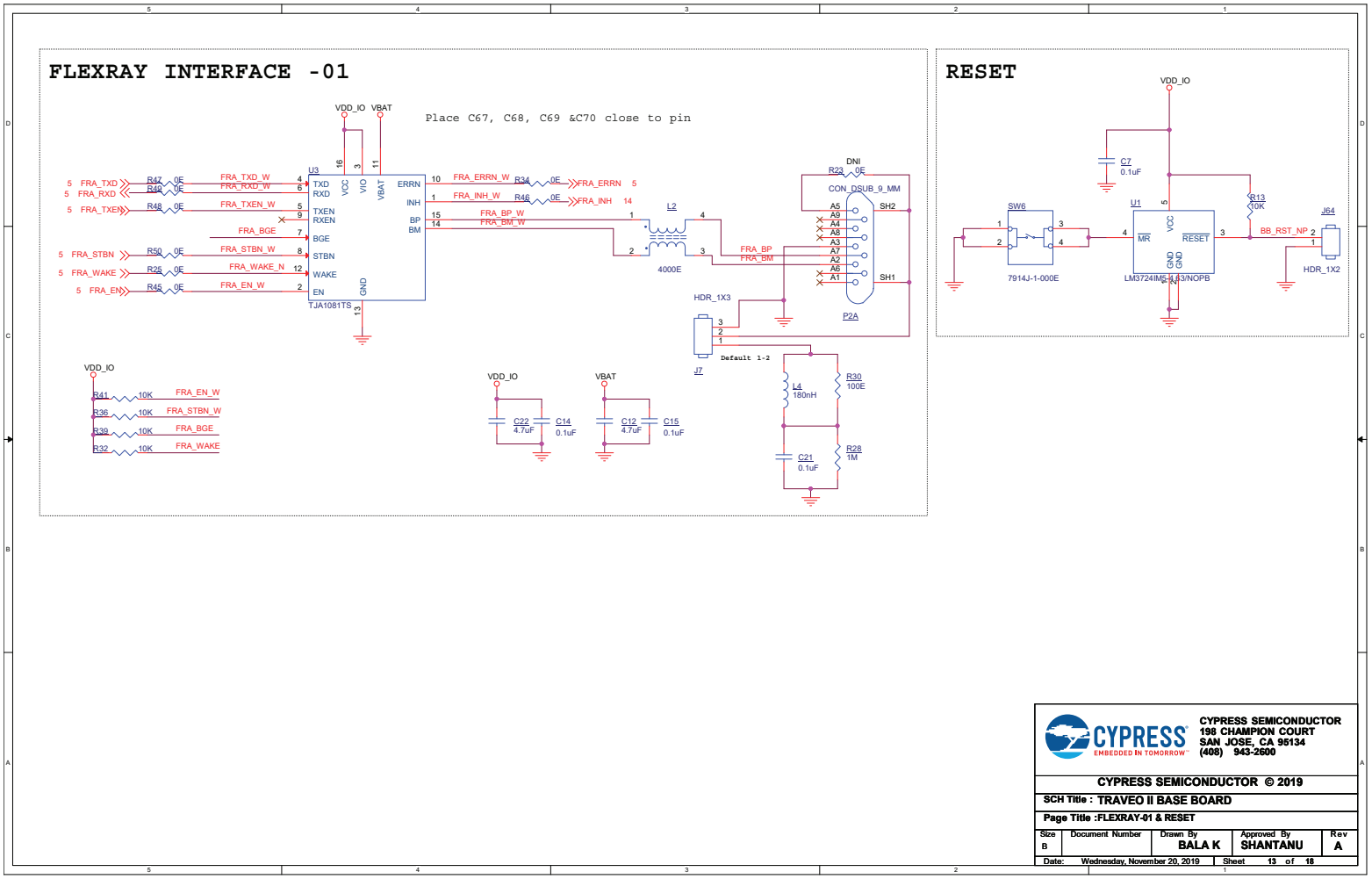


Figure C-12. Flexray-02 & INH

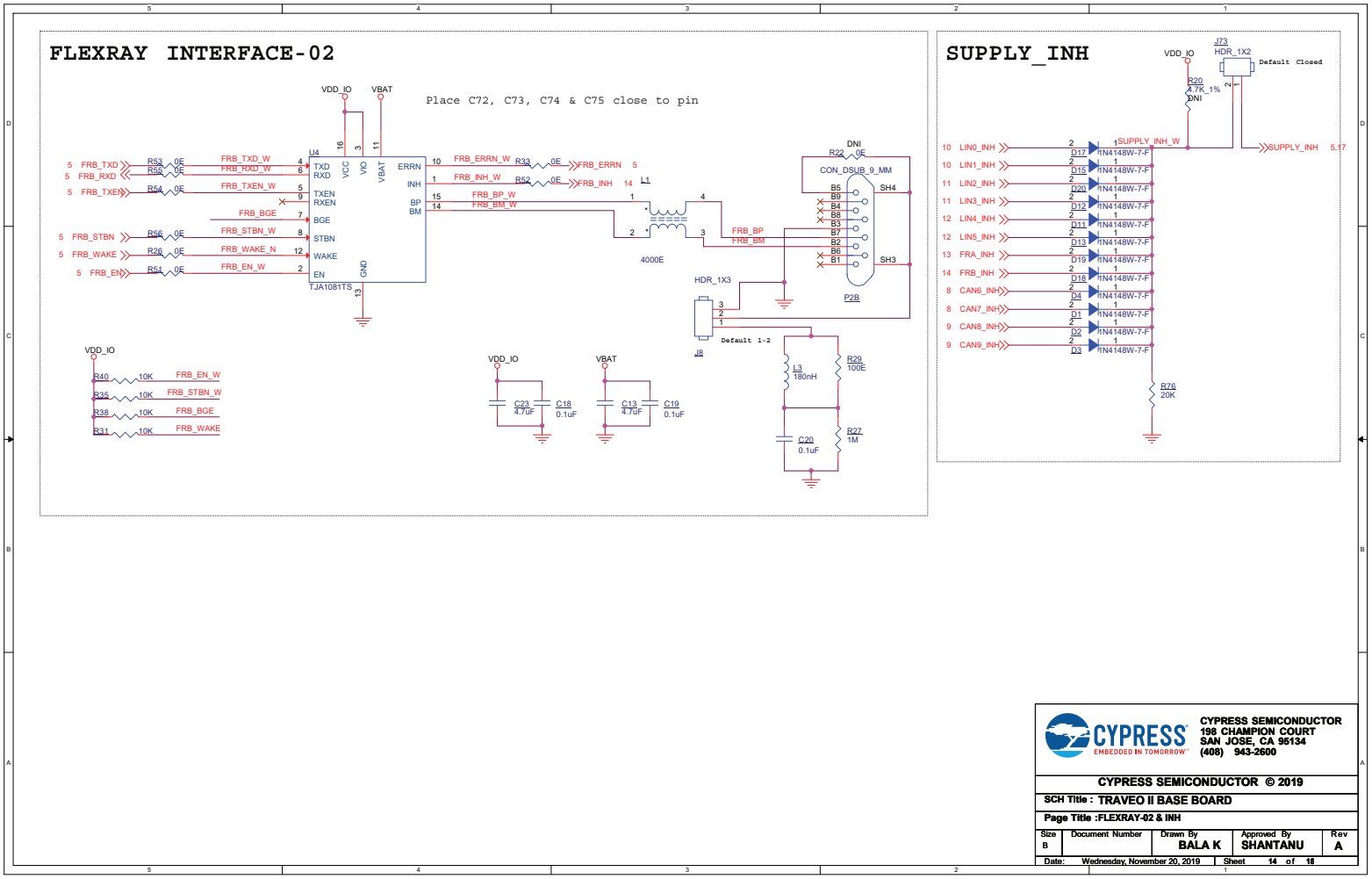


Figure C-13. CXPI, EEPROM & POT

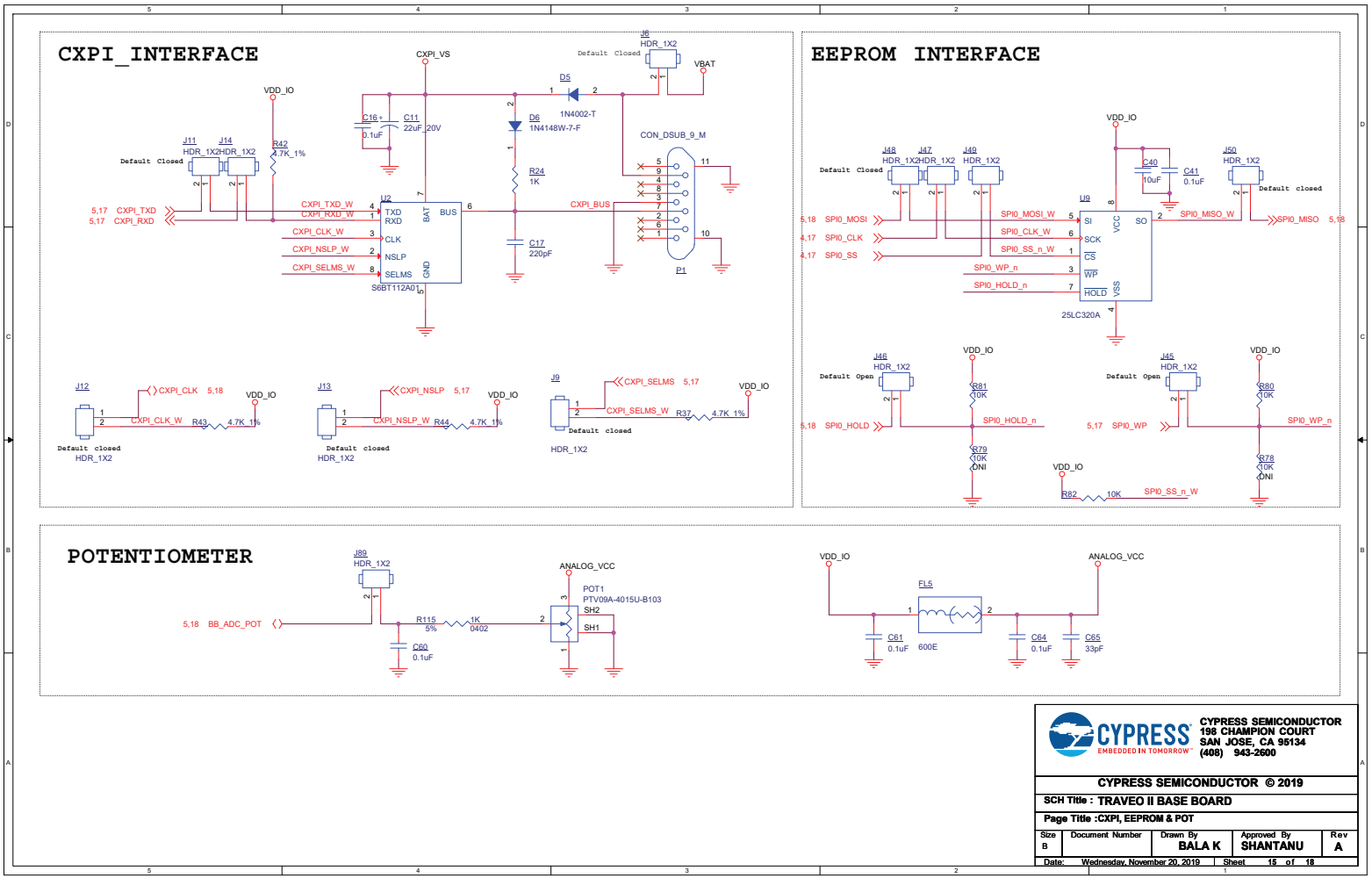


Figure C-14. USER_LED & PUSHBUTTON

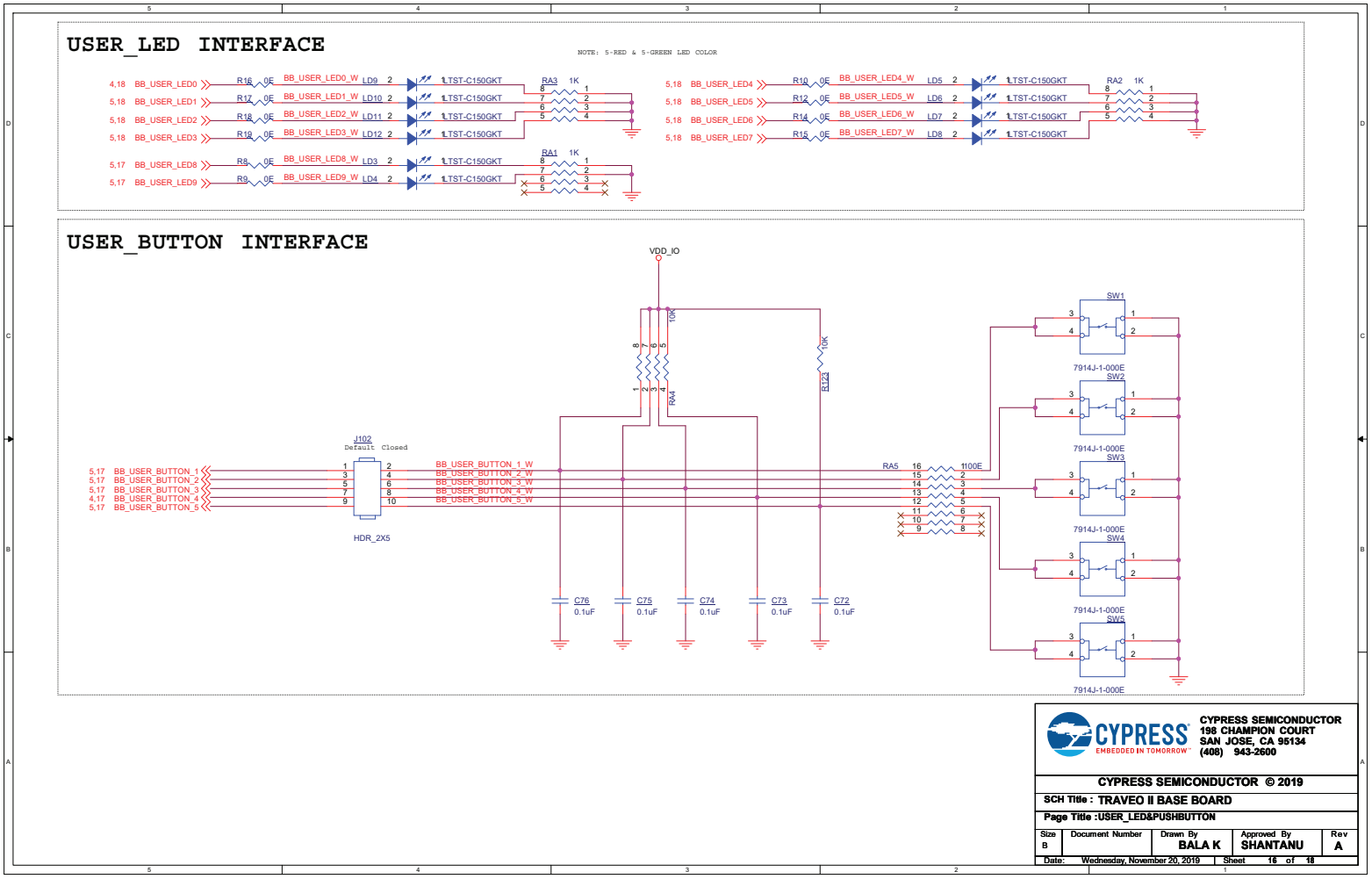


Figure C-15. Pin Header Section-01

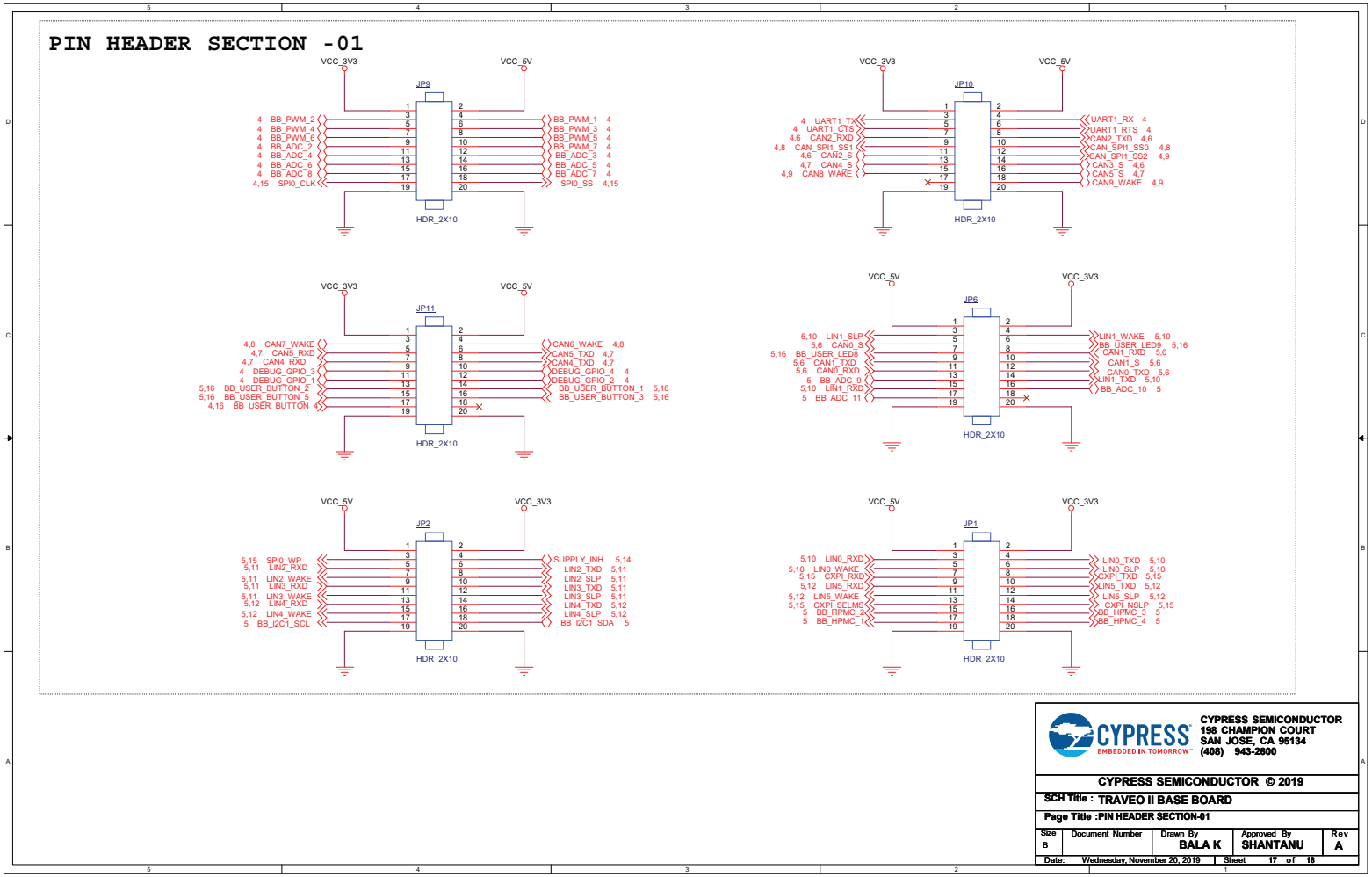
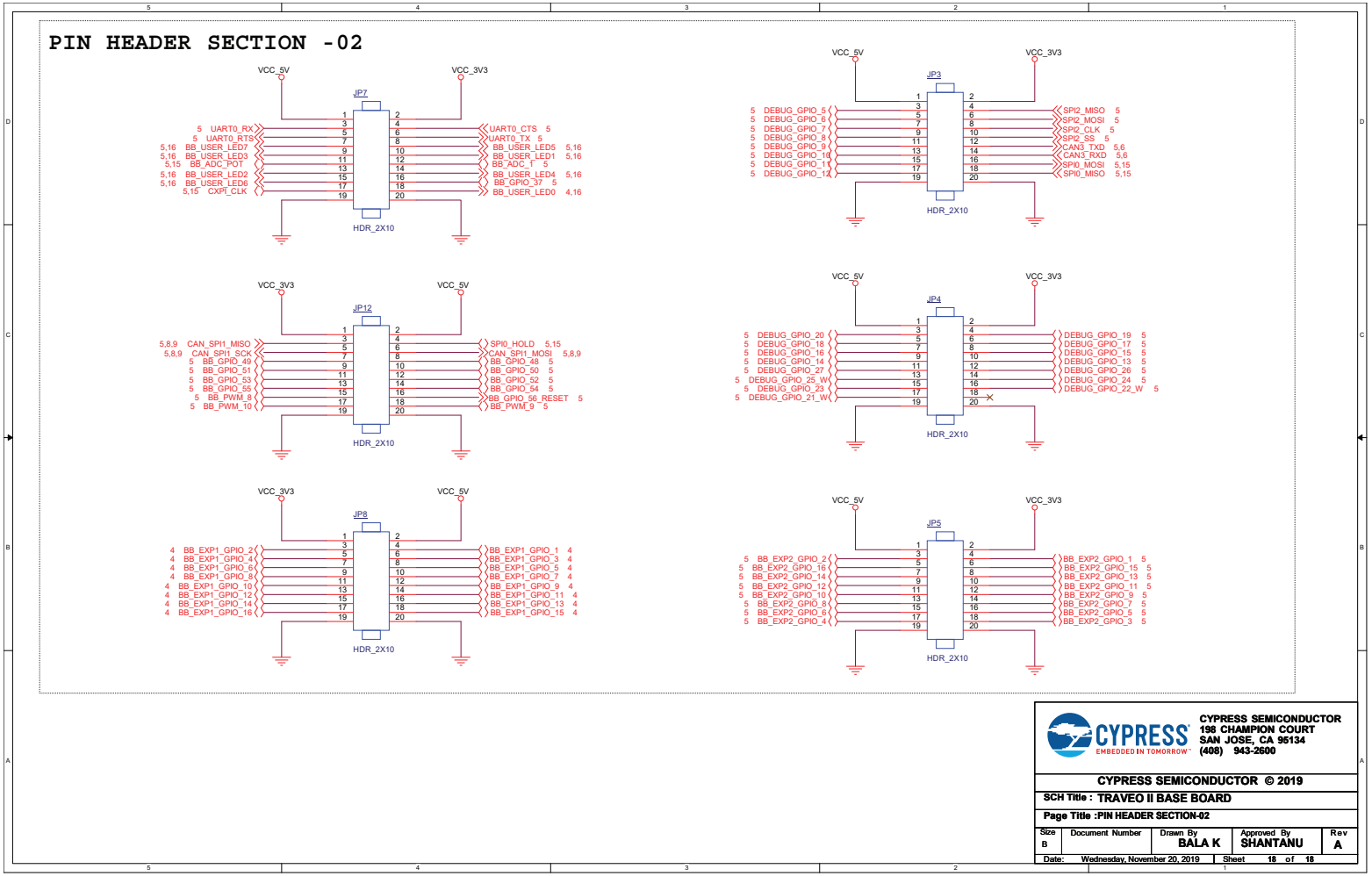


Figure C-16. Pin Header Section-02



D. Component Assembly on Base Board

This appendix shows the top and bottom assembly of the PCB.

Figure D-1. Top Assembly of the PCB

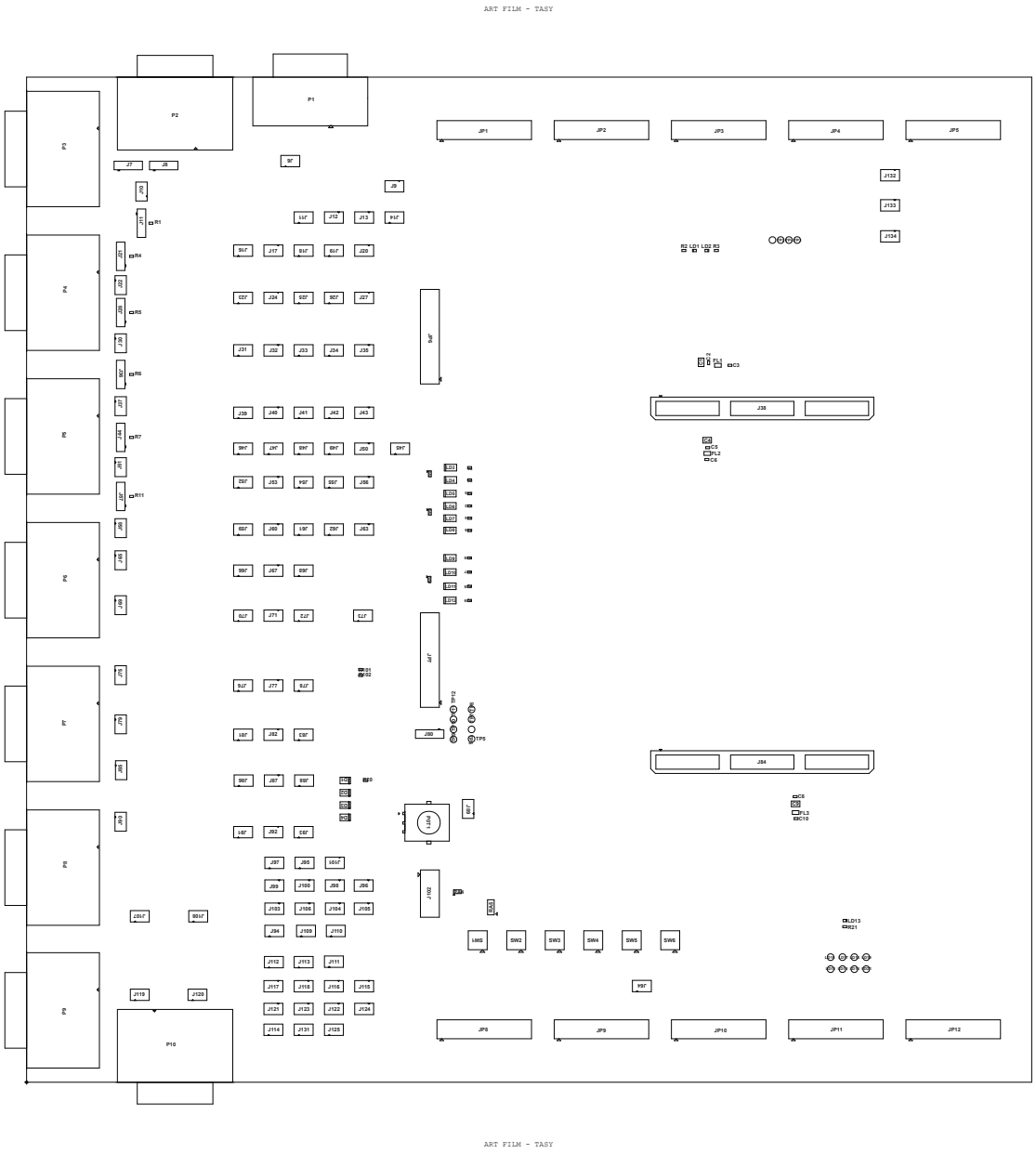
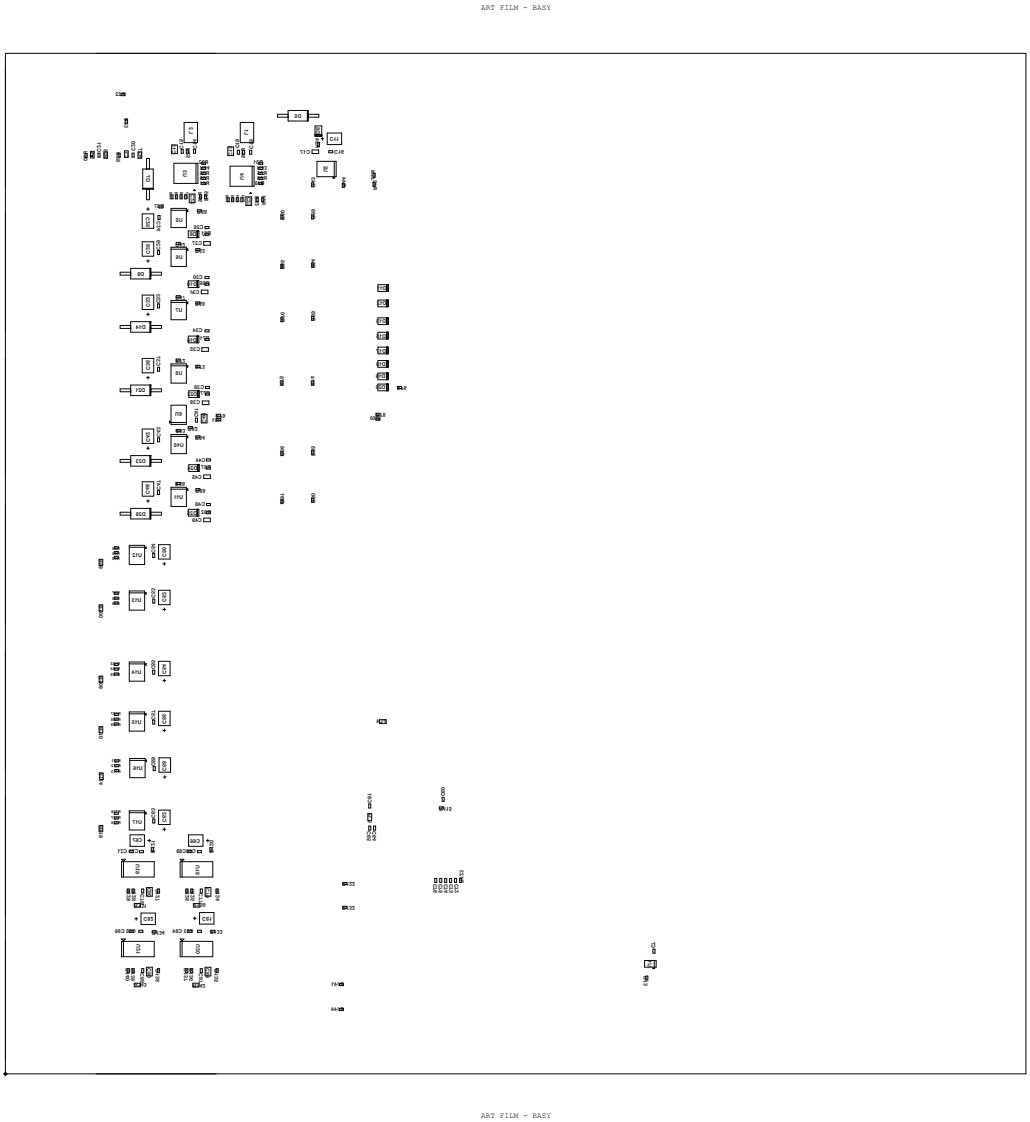


Figure D-2. Bottom Assembly of the PCB



Revision History

Document Revision History

Document Title: CYTVII-B-E-1M-176-CPU Evaluation Board User Guide Document Number: 002-22883			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	6186303	05/25/2018	New user guide for TVII CPU board.
*A	6501207	03/05/2019	Sunset Review TVII-B-E-1M-176-CPU board user guide updated as per Rev C board designs. 1. Added 5 V and 3.3 V selectable power supply for CPU board using J23. 2.CPU board to base board pin connection are updated in Table 4-1.
*B	6759586	12/23/2019	Updated content in section 1. Introduction and 2. Overview. Updated Figure 2-1 and Figure 3-1. Updated A. Schematics of CPU Board, B. Component Assembly on CPU Board, C. Schematics of Base Board, and D. Component Assembly on Base Board with text searchable content.
*C	6785957	01/24/2020	Fixed Figure A-12. Updated content in section 2. Overview.