

# EZ-PD<sup>™</sup> PAG1S-1P based 65 W ATQ GAN USB PD dual-C charger and adapter solution user guide

#### About this document

#### Scope and purpose

This document provides instructions and a quick start guide for EZ-PD<sup>™</sup> PAG1S-1P-based 65 W ATQ GAN PD dual-C charger and adapter solution (REF\_65W\_2C\_GAN\_PAG1).

#### **Intended audience**

This document is primarily intended for EZ-PD<sup>™</sup> PAG1S-1P multiport charger and adapter solution developers.



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Table of contents

#### **Table of contents**

Abo	About this document				
Tab	le of contents				
1	Introduction				
2	Specification				
3	Board overview				
4	Procedure to program EZ-PD™ CCG7DC-based daughter board	7			
5	Test setup				
5.1	Test equipment	8			
5.2	Power adapter tester (PAT)				
6	Quick steps for demo	10			
Refe	erences	11			
Revi	ision history	12			
	claimer				



Introduction

## 1 Introduction

As portable electronic devices such as smartphones, tablets, and laptops require faster charging, the Power Delivery (PD) technology is designed to provide the fastest charging possible through a USB Type-C (USB-C) cable. The USB PD Standard Power Range (SPR) standard defines the maximum power to deliver over a USB-C cable up to 100 W. This allows for providing multiple USB-C ports (Figure 1) on universal AC-DC adapters that can charge a wide range of devices such as smartphones, gaming laptops, power tools, and e-bikes.

However, these new requirements for higher power and multi-port have presented challenges for the converter topologies used till now. Considering a few factors such as electromagnetic compatibility, power factor correction, standby power, and average efficiency ensures that the chargers and adapters are effective and efficient. The size (power density), load sharing, and scaling up multiple ports became critical factors for design engineers and end-users. The power efficiency of USB-C chargers and adapters is a crucial role in determining their power density. Therefore, converter topology, usage model, integration, and flexibility of controller functionalities are all key factors to consider when selecting the right adapter architecture for the needs.

Figure 1 shows a typical block diagram of a multi-port adapter. The front-end AC-DC converter produces the requested output voltage. On the other hand, the buck converter (connected at the output of the AC-DC converter) ensures that the defined USB-C PD specifications and performance are achieved for multi-port adapter applications. Figure 1 shows a high-level block diagram of the EZ-PD<sup>™</sup> PAG1S-1P based 65 W dual-C adapter and charger solution.

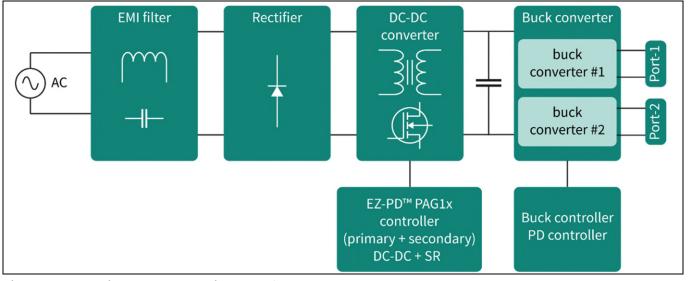


Figure 1 High-level block diagram of a dual-port adapter

Infineon provides a comprehensive solution for both sections of adapters, i.e., AC-DC and buck converters. Specifically, for AC-DC conversion, Infineon's EZ-PD<sup>™</sup> PAG1x-based solution, along with the EZ-PD<sup>™</sup> CCG7DCbased buck converter, ensure compatibility with USB PD/Programmable Power Supply (PPS) standards. The EZ-PD<sup>™</sup> CCG7DC supports a dual PD/PPS port, capable of controlling two buck controllers with integrated drivers, which makes it an ideal choice for dual or multi ports (multiples of 2) applications.



#### Introduction

Designator	Description	Part number	Manufacturer	
U1	EZ-PD <sup>™</sup> PAG1S USB PD power adapter secondary side controller	CYPAS111A1-24LQXQ	Infineon Technologies	
U2 EZ-PD <sup>™</sup> PAG1P primary side startup controller		CYPAP112A3-10SXQ	Infineon Technologies	
U3 EZ-PD™ CCG7DC dual-port USB Type-C with PD and buck-boost controller		CYPD7271-68LQXQES	Infineon Technologies	
Q4	CoolGaN™ IGLD60R190D1AUMA1 600 V 190 mΩ 10 A thinPAK8x8	IGLD60R190D1AUMA1	Infineon Technologies	
Q3	Nmos BSC050N10NS5 100 V 5 mR 16 A PG-TDSON-8 for SR	BSC050N10NS5	Infineon Technologies	
Q7, Q8	Nmos BSZ0902NS 30 V 3.5 mΩ 58 A PG- TSDSON-8_3.3*3.3	BSZ0902NS	Infineon Technologies	
Q1, Q5, Q6, Q9	Nmos BSZ063N04LS6 40 V 6.3 mΩ 40 A PG-TSDSON-8_3.3*3.3	BSZ063N04LS6	Infineon Technologies	
T1	350 uH ATQ power transformer	-	-	
Т2	Pulse edge transformer	LCL-T6-5138A	JQH Technologies	
EC1, EC5, EC6	CAP ALUM 33 uF 20% 400 V	KCXD2402G330MF	Yingming Electronic	
EC4	CAP ALUM 22 uF 20% 400 V	KCXD2402G220MF	Yingming Electronic	
EC2, EC3	Solid CAP ALUM POLY 680 uF 20% 25 V	NPXC1401E681MJTM	Yingming Electronic	
EC4	Solid CAP ALUM POLY 330 uF 20% 25 V	NPXC0901E331MJTM	Yingming Electronic	
L2, L3	22 μH ring inductor	TCH040125-W220M	SAYES Technologies	

#### Table 1 Critical components bill of materials (BOM)



Specification

# 2 Specification

Table 2 Test specifications				
Parameter	Value			
Input voltage and frequency	90 to 264 V AC, 47 to 63 Hz			
Max output power	65 W system power with dual-C and a max load current of 3.25 A			
	65 W on each port with a max load current of 3.25 A			
Output voltage	Single port:			
	Fixed PDOs: 5.0 V / 3.0 A, 9.0 V / 3.0 A, 15.0 V / 3.0 A, 20.0 V / 3.25 A			
	PPS: 3.3 V to 21.0 V, 3.25 A with PPS power limit			
	Dual port:			
	20W: 5V/3A, 9V/2.22A, 3.3V-5.9V/3A, 3.3V-11V/2.2A			
	32.5W: 5V/3A, 9V/3A, 12V/2.7A, 3.3V-11V/3A, 3.3V-16V/2.15A			
	45W: 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/2.25A, 3.3V-16V/3A			
Peak efficiency	> 93%			
Protections	1. Input overvoltage protection			
	2. Input undervoltage protection			
	3. V <sub>BUS_C</sub> overvoltage protection (OVP)			
	4. V <sub>BUS_C</sub> undervoltage protection (UVP)			
	5. Overcurrent protection (OCP)			
	6. Short-circuit protection (SCP)			
	7. Over-temperature protection (OTP)			
	8. $V_{BUS_C}$ to CC short protection			
Charging standards	1. USB-C PD v3.1 including programmable power supply (PPS) mode			
supported	2. Apple Charging 2.4 A			
	3. Qualcomm QC 2.0, 3.0, 4.0, 5.0			
	4. Samsung AFC			
	5. USB BC 1.2			
EMI/EMC	1. CE, CISPR32 CLASS B			
	2. ESD, IEC61000-4-2			
	3. Surge, IEC61000-4-5			
	4. Harmonics, IEC61000-3-2			



**Board overview** 

#### 3 Board overview

The EZ-PD<sup>™</sup> PAG1S-1P based 65 W USB PD dual-C charger and adapter solution (REF\_65W\_2C\_GAN\_PAG1 + CCG7DC 65W\_2C with ATQ) shown in Figure 2 solution board is designed to meet the specifications shown in Table 2. Baseboard with dual-C operates up to 65 W and each port operates up to 65 W.



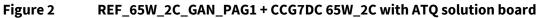


Figure 3 shows the schematic diagram for the EZ-PD<sup>™</sup> PAG1x-based with dual-port output. In this solution, the EZ-PD<sup>™</sup> PAG1x operates with about 70-kHz and functions as a secondary-side flyback, and SR controller. Additionally, the EZ-PD<sup>™</sup> CCG7DC functions as a buck controller, regulating the output voltage to a lower level than the input voltage, and a PD controller, negotiating with the connected device to provide the required power and voltage levels. The communication link between EZ-PD<sup>™</sup> PAG1S and EZ-PD<sup>™</sup> CCG7DC ensures optimal operation and efficiency by enabling a seamless optimization of the system's performance.

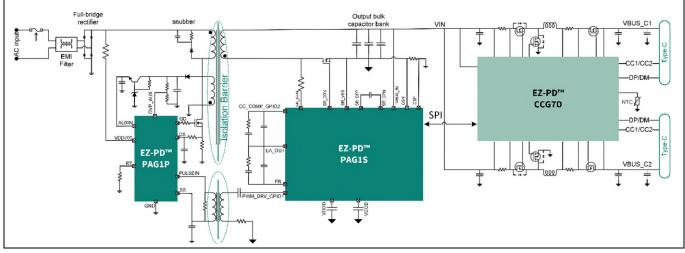


Figure 3

Schematic diagram of EZ-PD™ PAG11P-1S + EZ-PD™ CCG7DC design



Procedure to program EZ-PD<sup>™</sup> CCG7DC-based daughter board

#### **4** Procedure to program EZ-PD<sup>™</sup> CCG7DC-based daughter board

EZ-PD<sup>™</sup> PAG1S and EZ-PD<sup>™</sup> CCG7DC support PSoC<sup>™</sup> MiniProg4 (CY8CKIT-005) as a programmer to program the EZ-PD<sup>™</sup> controllers. The EZ-PD<sup>™</sup> PAG1S-based main board and EZ-PD<sup>™</sup> CCG7DC-based daughter board can be programmed using a PSoC<sup>™</sup> MiniProg4 five-pin connection.



Figure 4 PSoC<sup>™</sup> MiniProg4 (CY8CKIT-005) Programmer Kit

#### **Programming interface and settings**

The CYPRESS<sup>™</sup> Programmer software is used as a programming interface to program the firmware (*.hex* file) in an EZ-PD<sup>™</sup> PAG1S-based main board and EZ-PD<sup>™</sup> CCG7DC-based daughter board. For programming, select the "CCGx" platform and make other settings, as shown in Figure 5.

Settings		
Program Settings		
		-
File Reset Chip	C:/User/IR/Downloads/RCP6.hex	
Venity Regions		
Probe Settings		
Interface	SWD	
Voltage (V)	33	
Reset Type	Seft	
Sflash Restrictions	Drass Silash prohisted	
Log		
Tafe : flash 'mod	found at 0x0ffff200	,
	a rouna at exeminate 4 (Jash_prof. found at 0x90400000	
	ash probed value, using configured bank size	
	4_flash_prot found at 0x90600000	
	mflash (psoc4) at 0x00000000, size 0x00010000, buswidth 0, chipwidth 0	
	sflash (psoc4) at 0x8ffff200, size 0x00000200, buswidth 0, chipwidth 0	
	flashe (psoci_flash_prot) at 0:00400000, size 0:00000040, busadith 0, chipwidth 0 chipp (psoci_flash_prot) at 0:00500000, size 0:00000001, busadith 1	
Info : cyp status:		
Info : erase_device	e de la constante de	
Info : ShD DPIDR 8x		
	cquiring the device (mode: power-cycle)	
	alted due to debug-request, current mode: Thread 00000 pr: 04:100003a mp: 04:2001f46	
	neeree p: stassess map: stassestres courted successfully	
	proc4 mars erase 0 **	
Info : psoc mass er		
Info : cyp status:		
Info : cyp_get_mpn		
	arget psock-pu failed, trying to reexamine From connecting DP: cannot read IDR	
Error: Error: E	Error connecting Dr: cannot read IDA	
	wild not find MEN-AP to control the core	
	on failed, GDB will be halted. Polling again in 100ms	
	Error connecting DP: cannot read IDR	
	arget psoc4.cpu failed, trying to reexamine	
	Error connecting DP: cannot read IDR Error connecting DP: cannot read IDR	
	troor connecting w: cannot read lum uid not find MBH-AP to control the core	
	and more tailed rest to concrete the concrete the concrete the second seco	
	Error connecting DP: cannot read IDR	
Info : Polling ta	arget psc4.cpu failed, trying to reexamine From connection RP: cannot read IDR	



Programming interface to program EZ-PD™ CCG7DC 65-W daughter board

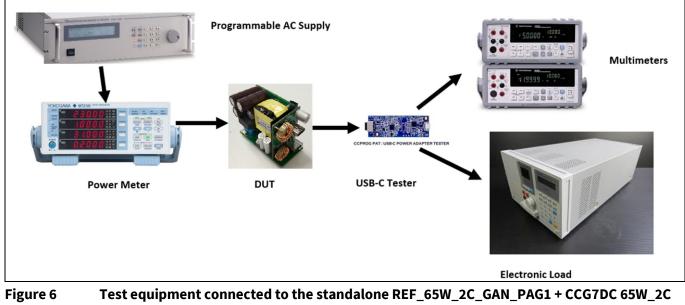


Test setup

#### 5 Test setup

Figure 6 shows the test setup to capture the electrical data of the DUT. The following setup is the optimal one to capture efficiency by capturing:

- Input power using a power meter
- Output power using high-resolution output multimeters



with ATQ) board

#### 5.1 Test equipment

Table 3 shows the test equipment to measure performance parameters such as efficiency, ripple, regulation, and transient response.

#### Table 3Test equipment details

Test setup	Description
Programmable AC source	Chroma 61501
AC power meter	Yokogawa WT310E
PAT tester	USBCEE PAT
Electronic load	Chroma 63102A
Multimeters	Keysight 34465A



#### Test setup

#### 5.2 Power adapter tester (PAT)

Connect the DUT to a USB-C power adapter tester (PAT) using a USB Type-C cable. After the connection is established, the PAT UI does a PDO discovery and displays the results.

The EZ-PD<sup>™</sup> EZ-PD<sup>™</sup> PAG1S-1P based 65 W USB PD dual-C charger and adapter solution is pre-configured with seven PDOs:

#### Single output: Port1 or Port2:

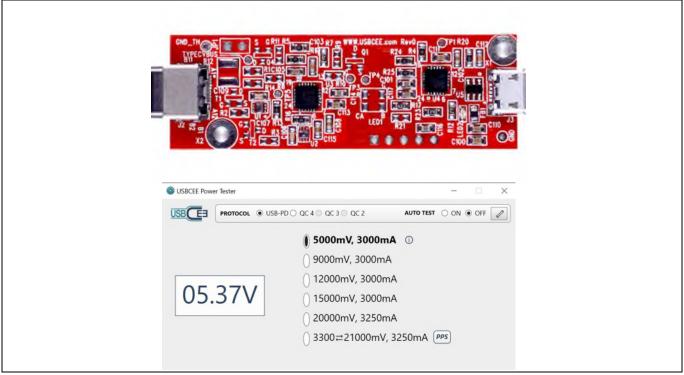
- Fixed PDOs: 5.0 V / 3.0 A; 9.0 V / 3.0 A; 15.0 V / 3.0 A; 20.0 V / 3.25 A
- PPS: 3.3 V to 21.0 V, 3.25 A (PPS power limited)

#### **Dual output: Port1 and Port2:**

- 20 W: 5 V/3 A, 9 V/2.22 A, 3.3 V to 5.9 V/3 A, 3.3 V-11 V/2.2 A
- 32.5 W: 5 V/3 A, 9 V/3 A, 12 V/2.7 A, 3.3 V to 11 V/3 A, 3.3 V to 16 V/2.15 A
- **45 W**: 5 V/3 A, 9 V/3 A, 12 V/3 A, 15 V/3 A, 20 V/2.25 A, 3.3 V to 16 V/3 A

Choose a suitable pre-configured PDO or configure a new one using the EZ-PD<sup>™</sup> Configuration Utility. Tests in the following sections use pre-configured PDOs.

To know more about the PAT tester, see USBCEE.







Quick steps for demo

### 6 Quick steps for demo

- 1. Connect the 65 W solution board to the power meter AC terminal (which is already connected to the programmable AC supply) as in Figure 6.
- 2. Connect a USB PD tester or a power adapter tester (PAT) to the port and ensure that the USB PD tester gets into a successful Power Delivery contract as shown in Figure 7.
- 3. Connect the electronic load at the PAT tester load terminal as in Figure 6.
- 4. Select the desired voltage on PAT UI and ramp up the load on the electronic load.



References

#### References

#### Datasheets

- [1] EZ-PD<sup>™</sup> PAG1P, Primary side startup controller
- [2] EZ-PD<sup>™</sup> PAG1S CYPAS111, USB PD power adapter secondary side controller
- [3] CYPD7271, EZ-PD<sup>™</sup> CCG7DC dual-port USB-C Power Delivery and DC-DC controller



**Revision history** 

### **Revision history**

Document revision	Date	Description of changes
**	2023-04-04	Initial release
*A	2023-04-21	Post to web

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