# CYW4335 OTP Programming and NVRAM

**Associated Part Family: CYW4335**

This application note describes the method for creating and programming an nvram.txt file. This file is used to test a new board design, optimize NVRAM values, and program the one-time programmable (OTP) nonvolatile memory in the CYW4335 device.

# Contents

# 1 Introduction

The Cypress CYW4335 is a single-chip IEEE802.11 a/b/g/n/ac + BT4.0/FM Rx device for embedded applications. One-time programmable (OTP) nonvolatile memory is included in the WLAN section of the device to store board-specific information such as product ID, manufacturer ID, MAC address. Excluding the header information, up to 502 bytes of OTP memory is available on the CYW4335 for WLAN information. Although the WLAN section provides the option of using a SDIO or HSIC host interface, this application note addresses only SDIO applications.

The OTP memory content, along with an editable NVRAM file (nvram.txt file), provides a complete card information structure (CIS) used by the device driver to initialize and configure the CYW4335.

## 1.1 Purpose and Audience

This document is intended for design and applications engineers. It contains information on:

■ NVRAM content development and OTP programming flow

■ SDIO Windows® XP driver installation

■ Customizing the nvram.txt file

■ OTP programming procedure

## 1.2 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

**Table 1. Mapping Table for Part Number between Broadcom and Cypress**

| Broadcom Part Number | Cypress Part Number |
|---|---|
| BCM4335 | CYW4335 |

## 1.3 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

## 1.4 Before You Begin

It is recommended that the users of this application note request the following items from Cypress's Customer Support Portal (http://community.cypress.com/):

- A CYW4335 board reference design package that contains:
  - The reference board schematic, bill of materials, and layout. Be sure to specify either the WLBGA or WLCSP package, and either single-band (2.4 GHz only) or dual-band (2.4 GHz and 5 GHz).
  - An nvram.txt template file for the reference board.
- A Windows XP or Linux® device driver for the relevant SDIO device
- Cypress transmit signal strength indicator (TSSI) calibration tools

Refer to IoT Resources for details on accessing Cypress CSP. If necessary, contact your Sales or Engineering support representative.

# 2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

# 3  OTP Programming Considerations

In designs where the host and device are permanently connected together, which is typically done using a hard-wired SDIO interface, programming the OTP memory during production is optional. It is equally acceptable to store all NVRAM parameters in the host firmware and keep the OTP blank in production. For devices that may be installed on different hosts, the OTP memory can be programmed to protect the unique MAC address and prevent end-users from altering the power control parameters such as maximum output power.

It is not necessary to program the OTP memory during board bring-up and hardware tuning on host platforms that run the Linux® or Windows® XP operating systems. Instead, all required board variables can be stored in the nvram.txt file. Although programming the OTP memory is not required for devices running these host operating systems, the nvram.txt file development is still required.

The initial state of all OTP bits in an unprogrammed device is 0. Individual bits can be set to 1, but once set, they can never be reset to 0. The entire OTP array can be programmed in a single-write cycle using the wl commands provided with the SDIO driver. As an alternative, multiple write cycles can be used to selectively program specific fields. However, only the bits that are still in the 0 state can be set to the 1 state during each programming cycle.

Because the OTP programming process is irreversible, Broadcom recommends that board designers finalize all parameters before programming the OTP memory. Boards and modules should be tested using only the editable nvram.txt file.

The parameters stored in the nvram.txt file are loaded into on-chip RAM by the driver, allowing the chip to be tested even if the OTP memory has not been programmed. This method lets board designers tune the RF components and alter critical parameters using different versions of the nvram.txt file while testing boards. Optionally, a few basic parameters, such as the board type and MAC address, can be programmed into the OTP memory prior to board testing during development. If a parameter is present in both the on-chip OTP memory and the nvram.txt file, the value in the OTP memory takes priority over the value in the nvram.txt file.

**Note:** The OTP programming process is irreversible. Broadcom strongly recommends conducting development on boards with blank OTP memory using the parameters provided in the editable nvram.txt file. Do not program the OTP memory until the contents of the nvram.txt file have been verified and the file has been finalized for production use.

# 4  NVRAM Content Development and OTP Programming Flow

Figure 1 shows the nvram.txt file content development and the OTP memory programming flow. Parameters in the nvram.txt file can be divided into basic and advanced categories. Relevant OTP programming details for each phase are discussed in Programming OTP Memory .

**Note:** The NVRAM development and OTP programming flow shown in Figure 1 should be conducted on small quantities of boards/modules during the product development stage. Once this process is complete and the production version of the nvram.txt file and OTP memory file is approved for production use, programming can be begin for high volume mass production as defined by each manufacturer.

Figure 1. NVRAM Development and OTP Programming Flow
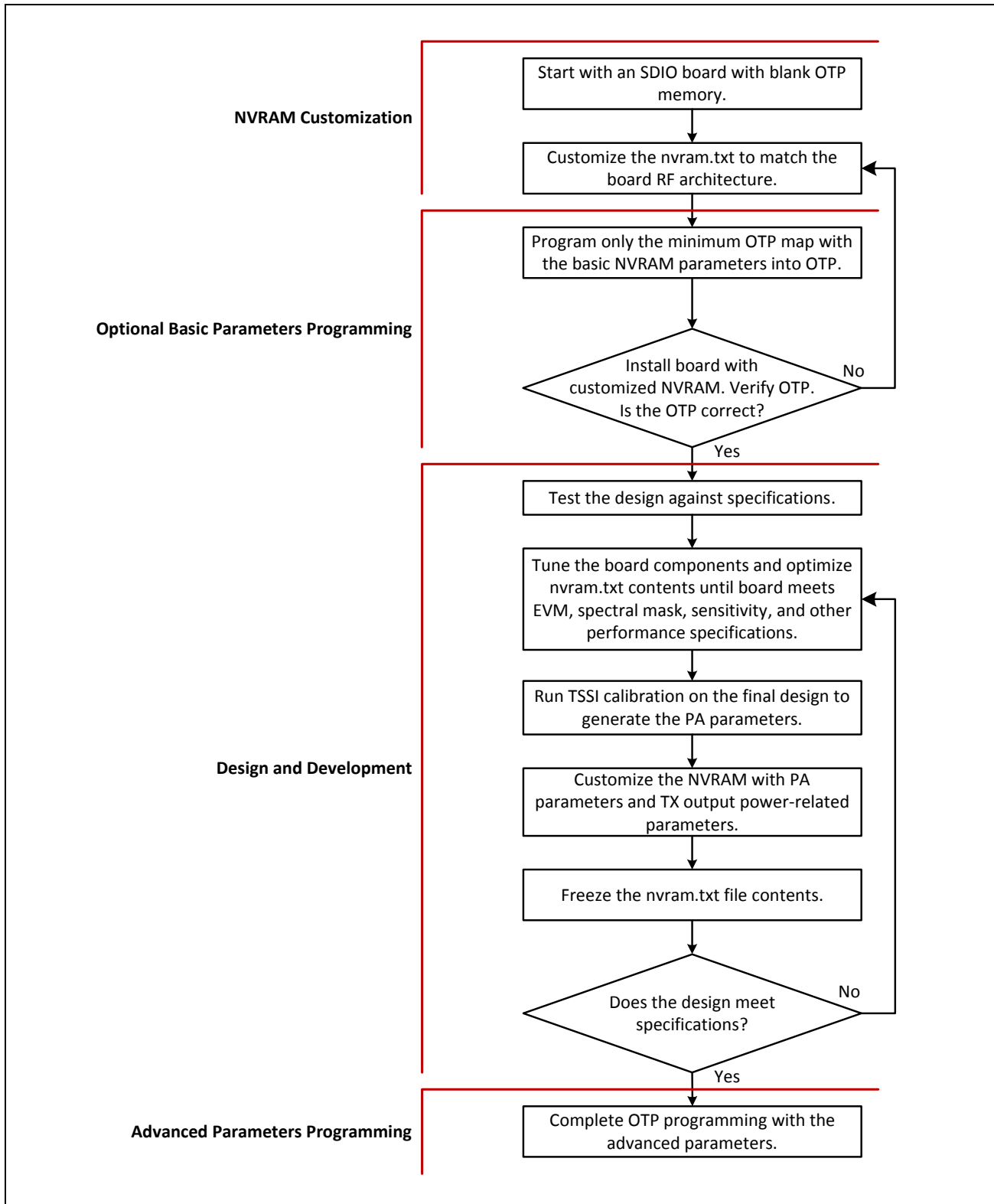
# 5 Customizing the nvram.txt File

This section describes customizing, editing, and finalizing the nvram.txt file for OTP memory programming.

## 5.1 Using the nvram.txt File Template

For each Broadcom reference board design, Broadcom provides an nvram.txt file for the specific board design. Typically, the file is named in accordance with the board it supports (for example, bcm4335wlcsp.txt).

The nvram.txt file might be included with the reference board design package or the driver release. The latest version of the file can be downloaded from the Broadcom CSP (see "IoT Resources ").

**Note:** When the nvram.txt file is edited, the file must be saved and the wireless device driver must be disabled and reenabled in Windows Device Manager for the change to take effect. Save the file as nvram.txt and store it in the C:\Windows\system32\drivers\ directory. Delete or overwrite any previous version of the file located in this directory.

Table 2 and Table 3 provide a list of parameters in a typical nvram.txt file that are common to Broadcom dual-band SDIO reference design boards.

Parameters in the nvram.txt file do no need to be entered in any specific order.

The parameters listed in Table 2 are used and specified by Cypress-specific only and should not be changed.

Table 2.  Cypress-Specific NVRAM Parameters

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| sromrev | 11 | SROM revision for 802.11ac chips |
| boardrev | 0x1100 | Board revision tracked by the used by the WLAN driver. Examples: 0x1100 corresponds to P100 0x1208 corresponds to P208 |
| boardtype | 0x064d | Identifies the board being used as follows: 0x064c: WLBGA package + ePA/eLNA for both bands 0x064d: WLCSP package + ePA/eLNA for both bands **Note**: This is a critical parameter that should be copied from a similar Broadcom reference board design. |
| tssipos2g | 1 | Defines the slope of the 2.4 GHz Transmission Signal Strength Indicator (TSSI). 0 = Negative slope 1 = Positive slope |
| tssipos5g | 1 | Defines 5 GHz TSSI slope. 0 = Negative slope 1 = Positive slope |
| rxchain | 1 | Specifies the number of Rx paths. |
| txchain | 1 | Specifies the number of Tx paths. |
| antswitch | 0 | Specifies the availability of antenna diversity. 0 = No diversity 1 = Diversity |
| NVRAMRev | $Rev: 349428 $ | NVRAM revision. **Note**: This parameter is for Cypress internal use only. |
| pdgain2g | 1 | Power detector parameter used by the driver to program the TSSI loopback path.  **Note:** The value of the pdgain2g parameter ranges from 1 to 6, depending on the TX power saturation point. In turn, TX power saturation point depends the layout and FEM selection. |

Table 2.  Cypress-Specific NVRAM Parameters (Continued.)

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| pdgain5g | 1 | Power detector parameter used by the driver to program the TSSI loopback path.<br><br>**Note:** The Value Of The Pdgain5g Parameter Ranges From 1 To 6, Depending On The Tx Power Saturation Point. In Turn, Tx Power Saturation Point Depends The Layout And Fem Selection. |
| vendid | 0x14e4 | Vendor ID |
| devid | 0x43ae | Chip ID 4335 |
| manfid | 0x2d0 | Manufacturer ID |
| nocrc | 1 | Flag for checking CRC.<br>Check CRC error when loading firmware. |

The design variables listed in Table 3 must be reviewed prior to beginning board or module testing. Specifically, the boardflags and swctrlmap variables and the number of antennas must be customized to match the board's RF architecture. During the development phase, start with the default power amplifier (PA) parameters contained in the provided nvram.txt file. The PA parameters are eventually optimized using Broadcom TSSI calibration tools.

**Note:** The parameters in Table 3 typically require tuning for each specific-board or module design. This is not an exhaustive list. Additional parameters may be added by Broadcom at any time to control the RF performance-related attributes of the driver. Always check with Broadcom for the latest version of the nvram.txt file for the reference design before starting for any board customization efforts.

**Note:** To avoid unexpected operating results, contact a technical support representative before attempting to add NVRAM parameters.

Table 3.  NVRAM Parameters Requiring Customizing

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| boardflags | 0x10401001 | Board configuration flag that defines the power topology, external components (ePA, eLNA), etc. |
| boardflags2 | 0x0 | |
| boardflags3 | 0x4 | |
| ccode | 0 | The country code (ccode) parameter is for regulatory use and specifies which regulatory tables are to be loaded.<br>**Note:** Together, the ccode and regrev parameters set the power limitations necessary to meet the country-specific regulatory specifications. |
| regrev | 0 | The regulatory revision (regrev) code parameter is for regulatory use and specifies which regulatory tables are to be loaded.<br>**Note:** Together, the regrev and ccode parameters set the power limitations necessary to meet the country-specific regulatory specifications. |
| pdgain5g<br>pdgain2g | 1 | Power detector parameter used by the driver to program the TSSI loopback path. |
| tworangetssi2g<br>tworangetssi5g | 0 | TSSI dual power range flag, which iPA chips support. |
| femctrl | 4 | Defines the front-end RF switch or front-end module (FEM) control logic for both bands. |
| xtalfreq | 37400 | Describes the reference oscillator frequency (kHz). |
| extpagain2g | 1 | Enables support for the 2.4 GHz external PA. |
| extpagain5g | 1 | Enables support for the 5 GHz external PA. |
| rxgains2gelnagaina0 | 3 | Defines the 2G eLNA gain (dB). |
| rxgains2gtrisoa0 | 3 | Defines the gain gap between RX mode and RX Atten mode. |
| rxgains2gtrelnabypa0 | 1 | Defines the isolation that eLNA provides in Bypass mode. |
| rxgains5gelnagaina0 | 3 | Defines the 5G eLNA gain (dB) |
| rxgains5gtrisoa0 | 4 | Defines the isolation that TR switch provides in T mode. |

Table 3.  NVRAM Parameters Requiring Customizing (Continued.)

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| rxgains5gtrelnabypa0 | 1 | Defines the isolation that eLNA provides in Bypass mode. |
| aa2g<br>aa5g | 1 | Number of antennas available for the 2.4 GHz and 5 GHz bands, respectively, in bit-mapped binary format:<br>1 = 01b for one antenna<br>3 = 11b for two antennas |
| ag0<br>ag1 | 0x82 | Antenna gain (dBi) is defined by converting its hexadecimal value to 8-bit binary, then follow the following rule:<br>Lower 0 – 5 bits: 6-bit signed 2's complement number in whole dB units.<br>Higher 6 – 7 bits:2-bit unsigned number in quarter dB units.<br>Examples:<br>0x82 (10000010) = 2.5 dB (2 + 2 × 0.25)<br>0x7f (01111111) = –0.75 dB (–1 + 1 × 0.25) |
| pa2ga0<br>pa2ga1 | –148, 5828, –679 | PA parameters for the 2.4 GHz band based on TSSI calibration.<br>**Note**: The pa2ga0 parameter is for the Orthogonal Frequency Division Multiplexing (OFDM) and MCS rates. The pa2ga1 parameter for the CCK rate. |
| pa5ga0<br>pa5ga1<br>pa5ga2 | 83, 6045, –553, 57, 5940, –566, 12, 5919, –605, –17, 5899, –640 | PA parameters for the 5 GHz band are based on TSSI calibration (Low/Mid/High/X1) (subband5gver = 4).<br>Subband Frequency RangeChannel Range<br>Low: 5180 to 524036 to 48<br>Mid: 5260 to 532052 to 64<br>High:5500 to 5700100 to 140<br>X1:  5745 to 5825149 to 165<br>**Note:**<br><br>■ The pa5ga0 parameter is for 20 MHz BW. The pa5ga1 parameter is for 40 MHz BW. The pa5ga2 parameter is for the 80 MHz bandwidth.<br>■ Each of the four subbands has three parameters (total of twelve parameters). |
| maxp2ga0 | 0x46 | Maximum output power for the 2.4 GHz band in hexadecimal format (quarter dB units).<br>This value applies to all complementary code keying (CCK) rates measured at the antenna port. The nominal target power (dBm) for CCK packets is –1.5 dB from maxp2ga0 (converted in dB units).<br>**Note:** The value can be entered in either hexadecimal or decimal format.<br><br>In the example shown for 0x46, maximum output power is 17 dBm ((16 x 4 + 6)/4). Nominal output power is 15.5 dBm (17 – 1.5). |
| cckbw202gpo | 0x0000 | CCK power offsets for 20 MHz rates<br>(11, 5.5, 2, 1 Mbps) |
| cckbw20ul2gpo | 0x0000 | CCK power offsets for 20 U/L rates<br>(11, 5.5, 2, 1 Mbps) |
| dot11agofdmhrbw202gpo | 0x6666 | OFDM power offset (in half dBm units)<br>54M/48/36M/24M |
| ofdmlrbw202gpo | 0x0033 | OFDM power offset (in half dBm units)<br>MCS1 and MCS2:11n and 11ac 40M<br>MCS1 and MCS2:11n and 11ac 20M<br>12 and 18 Mbps:11a/g<br>6 and 9 Mbps:11a/g |
| mcsbw202gpo | 0xAA886664 | 11n/ac MCS0/1/2, 3-7, C8,C9 power offset (in half dBm units)<br>C9/C8/M7/M6/M5/M4/M3/M0-2 |

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Table 3.  NVRAM Parameters Requiring Customizing (Continued.)

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| maxp5ga0 | 0x4A, 0x4A, 0x4A, 0x4A | Maximum output power for the 5 GHz band in hexadecimal format (quarter dB units). Theses values apply to all legacy OFDM rates measured at antenna port. The nominal target power is −1.0 dB from maxp5ga0 (converted in dB units). **Note:** Values can be entered in either hexadecimal or decimal format. |
| mcslr5glpo | 0x0000 | 5G low and mid subband 11ag/11n/11ac QPSK power offset with respect to BPSK: MCS 1/2 with respect to MCS 0/1/2  12/18 Mbps with respect to 6/9 Mbps  LSB to MSB nibble: (0) 20 MHz  (1) 40 MHz  (2) 80 MHz  (3) 160 MHz |
| mcsbw205glpo | 0xAA886664 | 5G low and mid subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 20 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcsbw405glpo | 0xAA886664 | 5G low and mid subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 40 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcsbw805glpo | 0xAA886664 | 5G low and mid subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 80 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcslr5gmpo | 0x0000 | 5G high subband 11ag/11n/11ac QPSK power offset with respect to BPSK: MCS 1/2 with respect to MCS 0/1/2  12/18 Mbps with respect to 6/9 Mbps  LSB to MSB nibble: (0) 20 MHz  (1) 40 MHz  (2) 80 MHz  (3) 160 MHz |
| mcsbw205gmpo | 0xAA886664 | 5G high subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 20 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcsbw405gmpo | 0xAA886664 | 5G high subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 40 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcsbw805gmpo | 0xAA886664 | 5G high subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 80 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcslr5ghpo | 0x0000 | 5G X1 subband 11ag/11n/11ac QPSK power offset with respect to BPSK: MCS 1/2 with respect to MCS 0/1/2  12/18 Mbps with respect to 6/9 Mbps  LSB to MSB nibble: (0) 20 MHz  (1) 40 MHz  (2) 80 MHz  (3) 160 MHz |
| mcsbw205ghpo | 0xAA886664 | 5G X1 subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 20 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |
| mcsbw405ghpo | 0xAA886664 | 5G X1 subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 40 MHz C9/C8/M7/M6/M5/M4/M3/M0-2 |

Table 3.  NVRAM Parameters Requiring Customizing (Continued.)

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| mcsbw805ghpo | 0xAA886664 | 5G X1 subband 11n/ac MCS0/1/2, 3-7, C8, C9 power offset for 80 MHz<br>C9/C8/M7/M6/M5/M4/M3/M0-2 |
| sb20in40hrpo | 0xAA886664 | 20 in 40 OFDM signed power offsets with respect to 20 in 20 for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 2G band<br>(1) 5G low subband<br>(2) 5G mid subband<br>(3) 5G high subband |
| sb20in80and160hr5glpo | 0xAA886664 | 5G low and mid subband 20 in 80, 20 in 160 OFDM signed power offsets for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 20 in 80 with respect to 20 in 20<br>(1) 20 in 160 with respect to 20 in 20<br>(2) 20 in 80 – 20LL/UU with respect to 20LU/UL<br>(3) 20 in 160 – 20LLL/UUU with respect to other 20 in 160 subbands |
| sb40and80hr5glpo | 0xAA886664 | 5G low and mid subband 40 in 80, 40 in 160 OFDM signed power offsets for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 40 in 80 with respect to 40 in 40<br>(1) 40 in 160 with respect to 40 in 40<br>(2) 80 in 160 with respect to 80 in 80<br>(3) 40 in 160 – 40LL/UU with respect to 40LU/UL |
| sb20in80and160hr5gmpo | 0xAA886664 | 5G high subband 20 in 80, 20 in 160 OFDM signed power offsets for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 20 in 80 with respect to 20 in 20<br>(1) 20 in 160 with respect to 20 in 20<br>(2) 20 in 80 – 20LL/UU with respect to 20LU/UL<br>(3) 20 in 160 – 20LLL/UUU with respect to other 20 in 160 subbands |
| sb40and80hr5gmpo | 0xAA886664 | 5G high subband 40 in 80, 40 in 160 OFDM signed power offsets for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 40 in 80 with respect to 40 in 40<br>(1) 40 in 160 with respect to 40 in 40<br>(2) 80 in 160 with respect to 80 in 80<br>(3) 40 in 160 – 40LL/UU with respect to 40LU/UL |
| sb20in80and160hr5ghpo | 0xAA886664 | 5G X1 subband 20 in 80, 20 in 160 OFDM signed power offsets for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 20 in 80 with respect to 20 in 20<br>(1) 20 in 160 with respect to 20 in 20<br>(2) 20 in 80 – 20LL/UU with respect to 20LU/UL<br>(3) 20 in 160 – 20LLL/UUU with respect to other 20 in 160 subbands |
| sb40and80hr5ghpo | 0xAA886664 | 5G X1 subband 40 in 80, 40 in 160 OFDM signed power offsets for 64 QAM and above.<br>LSB nibble to MSB nibble:<br>(0) 40 in 80 with respect to 40 in 40<br>(1) 40 in 160 with respect to 40 in 40<br>(2) 80 in 160 with respect to 80 in 80<br>(3) 40 in 160 – 40LL/UU with respect to 40LU/UL |

Table 3.  NVRAM Parameters Requiring Customizing (Continued.)

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| sb20in40lrpo | 0xAA886664 | 20 in 40 OFDM signed power offsets with respect to 20 in 20 for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 2G band<br>(1) 5G low subband<br>(2) 5G mid subband<br>(3) 5G high subband |
| sb20in80and160lr5glpo | 0xAA886664 | 5G low and mid subband 20 in 80, 20 in 160 OFDM signed power offsets for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 20 in 80 with respect to 20 in 20<br>(1) 20 in 160 with respect to 20 in 20<br>(2) 20 in 80 – 20LL/UU with respect to 20LU/UL<br>(3) 20 in 160 – 20LLL/UUU with respect to other 20 in 160 subbands |
| sb40and80lr5glpo | 0xAA886664 | 5G low and mid subband 40 in 80, 40 in 160 OFDM signed power offsets for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 40 in 80 with respect to 40 in 40<br>(1) 40 in 160 with respect to 40 in 40<br>(2) 80 in 160 with respect to 80 in 80<br>(3) 40 in 160 – 40LL/UU with respect to 40LU/UL |
| sb20in80and160lr5gmpo | 0xAA886664 | 5G high subband 20 in 80, 20 in 160 OFDM signed power offsets for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 20 in 80 with respect to 20 in 20<br>(1) 20 in 160 with respect to 20 in 20<br>(2) 20 in 80 – 20LL/UU with respect to 20LU/UL<br>(3) 20 in 160 – 20LLL/UUU with respect to other 20 in 160 subbands |
| sb40and80lr5gmpo | 0xAA886664 | 5G high subband 40 in 80, 40 in 160 OFDM signed power offsets for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 40 in 80 with respect to 40 in 40<br>(1) 40 in 160 with respect to 40 in 40<br>(2) 80 in 160 with respect to 80 in 80<br>(3) 40 in 160 – 40LL/UU with respect to 40LU/UL |
| sb20in80and160lr5ghpo | 0xAA886664 | 5G X1 subband 20 in 80, 20 in 160 OFDM signed power offsets for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 20 in 80 with respect to 20 in 20<br>(1) 20 in 160 with respect to 20 in 20<br>(2) 20 in 80 – 20LL/UU with respect to 20LU/UL<br>(3) 20 in 160 – 20LLL/UUU with respect to other 20 in 160 subbands |
| sb40and80lr5ghpo | 0xAA886664 | 5G X1 subband 40 in 80, 40 in 160 OFDM signed power offsets for 16 QAM and below.<br>LSB nibble to MSB nibble:<br>(0) 40 in 80 with respect to 40 in 40<br>(1) 40 in 160 with respect to 40 in 40<br>(2) 80 in 160 with respect to 80 in 80<br>(3) 40 in 160 – 40LL/UU with respect to 40LU/UL |

Table 3.  NVRAM Parameters Requiring Customizing (Continued.)

| NVRAM Parameter | Example Data | Description |
|---|---|---|
| dot11agduphrpo | 0xAA886664 | 11a/g Duplicate mode signed power offsets for 64 QAM. Common power offset for:<br>• Dup40, Dup40 in 80, and Dup40 in 160 with respect to 40 in 40 11n/11ac<br>• Quad80 and Quad80 in 160 with respect to 11ac 80in80<br>• Oct160 with respect to 11ac 160 in 160<br>LSB to MSB nibble:<br>(0) 2G band<br>(1) 5G low subband<br>(2) 5G mid subband<br>(3) 5G high subband |
| dot11agduplrpo | 0xAA886664 | Bits 11a/g duplicate mode signed power offsets for 16 QAM and below. Common power offset for:<br>• Dup40, Dup40 in 80, and Dup40 in 160 with respect to 40 in 40 11n/11ac<br>• Quad80 and Quad80 in 160 with respect to 11ac 80in80<br>• Oct160 with respect to 11ac 160 in 160<br>LSB to MSB nibble:<br>(0) 2G band<br>(1) 5G low subband<br>(2) 5G mid subband<br>(3) 5G high subband |

## 5.2 Editing the nvram.txt File

The nvram.txt file should be edited using a properly formatted text editor such as Notepad++ or WordPad++ to preserve the original format of the file. Using a non-formatted text editor such as Notepad could corrupt the format of the NVRAM map, causing the driver to incorrectly read the nvram.txt file.

## 5.3 Finalizing the nvram.txt File

After the final PA parameters have been generated, edit the nvram.txt file to update the PA parameters derived using the Broadcom TSSI tool, and then adjust the Tx output power-related parameters in the file. Using the updated nvram.txt file, run output power tests to verify that the parameters are providing the correct output power. Also, verify that RF performance (EVM, spectral mask, and rxper) meets design specifications.

Broadcom recommends running a regulatory prescan to verify that the required output power can be delivered without violating the band-edge limits. If the band-edge limits cannot be met, it may be necessary to reduce the output power at the band-edge channels.

After all prototype tests have passed and all nvram.txt file parameters have been optimized and finalized, the needed parameters can be selected and the OTP memory programmed for production.

The CYW4335 has 502 bytes of space in the OTP memory available for user data. Given the limited space in the OTP memory, it is impossible to program the entire nvram.txt file to the OTP memory. The programmer must be very careful to select only the necessary parameters that go into the OTP memory. Parameters that typically go into the OTP memory are those that are unique to the board (such as MAC address) and those that are required to satisfy local regulatory requirements, which are usually output power-related parameters such as maximum output power, power offset per-rate, PA parameters, and country code.

# 6 Programming OTP Memory

Prior to programming the OTP memory, an OTP binary map file must be prepared and populated with the correct values. The OTP binary map completely defines the parameters that have to be programmed into the OTP memory. The SDIO OTP data format is based on the CIS as defined by the PCMCIA/SD Card Association. The CIS data contains the hardware header followed by one or more data blocks (tuples), where each tuple contains the type, length, and the value of the tuple (see Appendix A: "CIS Map" for details).

The SDIO hardware header string must be present at the beginning of the OTP binary map and must precede all NVRAM variables. When a driver detects content in the OTP memory, the SDIO hardware header is required to boot up the CYW4335 via the SDIO interface. Therefore, the SDIO hardware header must include the minimum set of parameters necessary to program the OTP memory.

The SDIO hardware header is described in Table 7. All other parameters that need to be programmed into the OTP memory are added after the SDIO hardware header (see Creating and Editing the OTP Binary Map ).

When an OTP binary map contains only the SDIO hardware header, the binary map is called a minimum OTP binary map.

Table 4 describes the minimum OTP binary map for the CYW4335, which is terminated at 0xff 0xff.

Table 4.  CYW4335 Minimum OTP Binary Map (502 Bytes)

| Offset | 0x0 | 0x1 | 0x2 | 0x3 | 0x4 | 0x5 | 0x6 | 0x7 | 0x8 | 0x9 | 0xa | 0xb | 0xc | 0xd | 0xe | 0xf |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 | 4b | 00 | ff | ff | 00 | 00 | 20 | 04 | d0 | 02 | 35 | 43 | 00 | 00 | 00 | 00 |
| 0x0010 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0020 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0030 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0040 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0050 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0060 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0070 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0080 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0090 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00a0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00b0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00c0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00d0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00e0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00f0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00100 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00110 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00120 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00130 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00140 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00150 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00160 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00170 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00180 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00190 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001a0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001b0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001c0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001d0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001e0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001f0 | 00 | 00 | 00 | 00 | ff | ff | | | | | | | | | | |

## 6.1 Programming Basic Parameters into OTP Memory

Parameters in the nvram.txt file that are to be programmed into the OTP memory must be entered in the OTP binary map after the SDIO hardware header. A CIS tuple is required for each parameter in the CIS structure. Most parameters in the nvram.txt file have a unique identifier called the CIS tuple tag. The driver recognizes and parses each CIS tuple by its tag number. For a list of the CIS tuples and associated tag numbers, see Appendix A: "CIS Map" .

Table 5 lists the basic NVRAM parameters, the associated tag number, and the number of bytes each parameter occupies in the OTP memory. Basic parameters typically have fixed values specific to a particular device or board. The value of these parameters is often retained throughout the life of the device/board. For this reason, it is generally acceptable to program these basic parameters into the OTP memory early in the development, before the design is finalized.

Table 5.  Basic NVRAM Parameters and CIS Tuple Tags

| NVRAM Parameter | CIS Tuple Tag | Length of Value (in Bytes) |
|---|---|---|
| sromrev | 0x00 | 1 |
| boardrev | 0x02 | 2 |
| boardtype | 0x1b | 2 |
| macaddr | 0x19 | 6 |
| ccode[a] | 0x0a | 2 |

a. The value for ccode in the nvram.txt file is in ASCII format. It must be converted to hexadecimal format before entering it into the OTP binary map (for example, "US" = "0x55 0x53").

In the OTP binary map, each tuple is formed by the four fragments described in Table 6.

Table 6.  CIS Tuple Format

| Fragment | Description |
|---|---|
| 80 | Indicates the beginning of a new tuple. 0x80 is specific to Broadcom tuple subtags. |
| Length | Defines the total size (in bytes) of the tag plus the value of the tuple that occupies the OTP memory space. |
| Tag | Identifies a parameter in the nvram.txt file. A tag usually takes one byte in memory. |
| Value | Specifies the value of the parameter in little-endian format (first byte is the least-significant byte (LSB)). |

For example, the following tuple is defined by the fragments that follow:

| 80 | 03 | 02 | 00 | 11 |
|---|---|---|---|---|

- ■ 80Beginning of a new tuple.
- ■ 03The tag (1 byte) and the value (2 bytes) occupy 3 bytes (total) in the OTP memory.
- ■ 02Tag of 0x02 is the identifier for boardrev in the nvram.txt file.
- ■ 00  11The value of boardrev in reverse hexadecimal byte or 0x1100.

Table 7 provides an example OTP binary map for a CYW4335 that contains some of the nvram.txt file parameters listed in Table 5.

**Table Legend:**
   (Table 7)

Hardware Header
SROMREV (0x0b)
BOARDREV(0x1100)
BOARDTYPE(0x064c)
MAC Address
End of Map

In this example, the value of each parameter is as follows:

- sromrev = 0x0B
- boardrev = 0x1100
- boardtype = 0x64c
- macaddr = 66:55:44:33:22:11

**Note:** CIS tuples do not have to be listed in any particular order because each tuple begins with a unique identifier.

**Note:** OTP bytes can be written to only once. Only blank and zero-programmed bytes can be programmed during subsequent write cycles.

Table 7.  Example CYW4335 Minimum OTP Binary Map (502 Bytes)

| Offset | 0x0 | 0x1 | 0x2 | 0x3 | 0x4 | 0x5 | 0x6 | 0x7 | 0x8 | 0x9 | 0xa | 0xb | 0xc | 0xd | 0xe | 0xf |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 4b | 00 | ff | ff | 00 | 00 | 20 | 04 | d0 | 02 | 35 | 43 | 80 | 02 | 00 | 0b |
| 0x0000 | 80 | 03 | 02 | 00 | 11 | 80 | 03 | 1b | 4c | 06 | 80 | 07 | 19 | 66 | 55 | 44 |
| 0x0010 | 33 | 22 | 11 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0020 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0030 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0040 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0050 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0060 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0070 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0080 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x0090 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00a0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00b0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00c0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00d0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00e0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00f0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00100 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00110 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00120 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00130 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00140 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00150 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00160 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00170 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00180 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x00190 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001a0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001b0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001c0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001d0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001e0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 0x001f0 | 00 | 00 | 00 | 00 | ff | ff | | | | | | | | | | |

## 6.2 Creating and Editing the OTP Binary Map

Use a hexadecimal text editor to create and edit an OTP binary map. A hexadecimal text editor preserves formatting of the nvram.txt file. Writing to the OTP memory requires a bin file that fits in the OTP memory space. For the CYW4335, the maximum size of the OTP memory is 502 bytes.

**Caution!** Do not use Notepad to edit the nvram.txt file. Edit the nvram.txt file using a properly formatted text editor such as Notepad++ or WordPad++ to preserve the original format of the file. Using a non-formatted text editor such as Notepad could corrupt the format of the NVRAM map, causing the driver to incorrectly read the nvram.txt file.

1. Add or edit each byte in the OTP binary map to populate the SDIO hardware header and the CIS tuple, as described in the OTP binary map instructions provided in Programming Basic Parameters into OTP Memory .
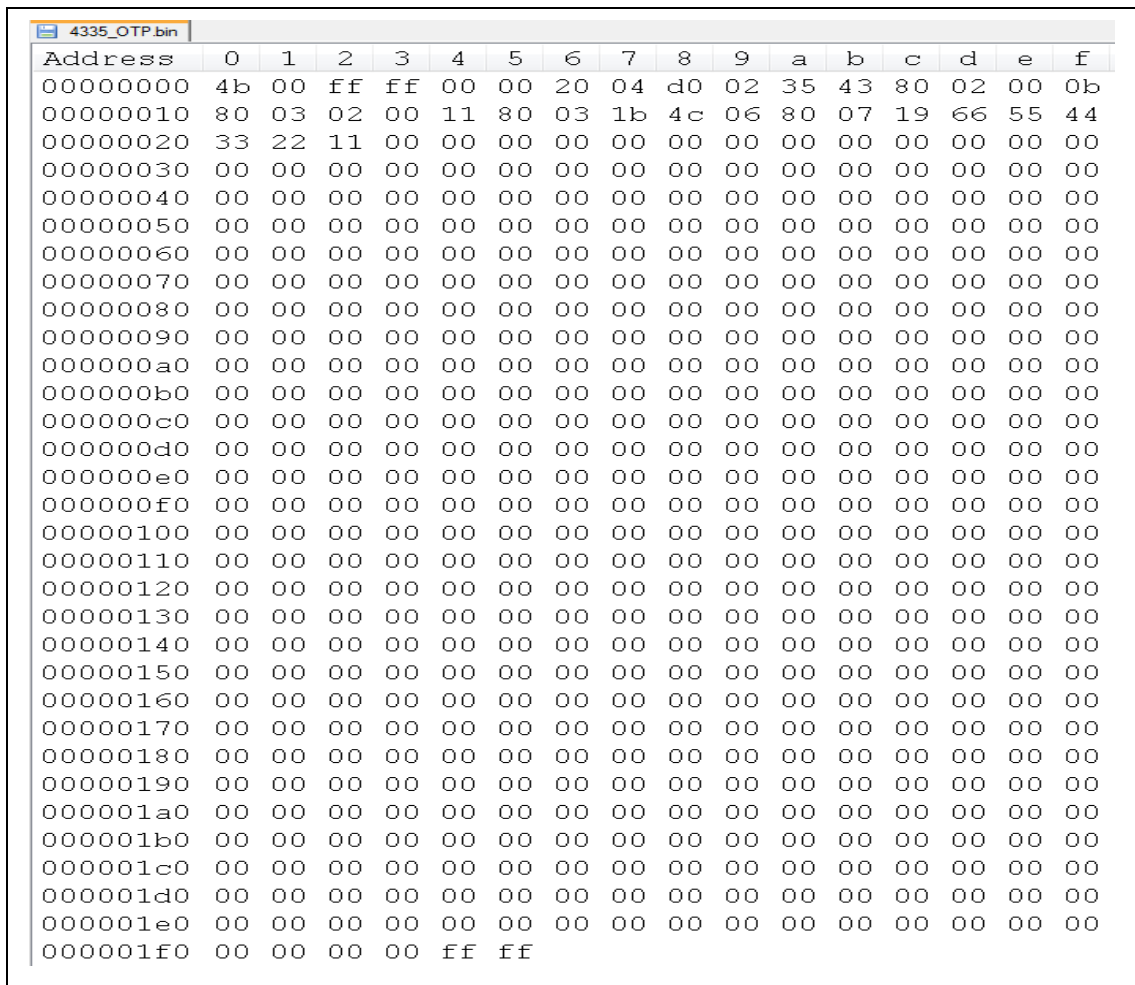
**Note:** The OTP binary map file (see Figure 2) has been edited to match the example CYW4335 OTP binary map described in Table 7.

2. Save the OTP binary map as a binary image file (.bin extension) to the directory containing the wl.exe file.

**Note:** The file name must be save with a .bin file extension so that the data it contains can be programmed into the OTP memory. For example purposes, this file is referred to as 4335_OTP.bin in the following instructions.

Figure 2 shows the hexadecimal OTP binary map template.

Figure 2. CYW4335 Hexadecimal OTP Binary Map Template

| 4335_OTP.bin | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | a | b | c | d | e | f |
| 00000000 | 4b | 00 | ff | ff | 00 | 00 | 20 | 04 | d0 | 02 | 35 | 43 | 80 | 02 | 00 | 0b |
| 00000010 | 80 | 03 | 02 | 00 | 11 | 80 | 03 | 1b | 4c | 06 | 80 | 07 | 19 | 66 | 55 | 44 |
| 00000020 | 33 | 22 | 11 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000030 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000040 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000050 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000060 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000070 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000080 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000090 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000000a0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000000b0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000000c0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000000d0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000000e0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000000f0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000100 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000110 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000120 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000130 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000140 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000150 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000160 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000170 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000180 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 00000190 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000001a0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000001b0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000001c0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000001d0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000001e0 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 | 00 |
| 000001f0 | 00 | 00 | 00 | 00 | ff | ff | | | | | | | | | | |

## 6.3    Programming the OTP Binary Map

To program the OTP binary map for the CYW4335 using wl commands, complete the following steps:

1.    Load the driver for the CYW4335 using the customized nvram.txt file.

2.    Execute a few wl commands (such as wl ver) to verify that the driver installation was successful.

3.    Execute the ciswrite 4335_OTP.bin command to program the 4335_OTP.bin to the OTP memory.

4.    In the Windows Device Manager, disable and then enable the wireless device.

5.    Execute the cisdump command to confirm that the OTP memory is programmed successfully.
Using 66 55 44 33 22 11 as the MAC address, the output should exactly match the OTP binary map shown in Figure 2.

Figure 3. An Example of a wl cisdump Output

```
[root@dhcpe6-sv1-141 ec_4335_driver]# wl cisdump
Source: 2 (Internal OTP)
Maximum length: 502 bytes
Byte   0: 0x4b 0x00 0xff 0xff 0x00 0x00 0x20 0x04
Byte   8: 0xd0 0x02 0x35 0x43 0x80 0x02 0x00 0x0b
Byte  16: 0x80 0x03 0x02 0x00 0x11 0x80 0x03 0x1b
Byte  24: 0x4c 0x06 0x80 0x07 0x19 0x66 0x55 0x44
Byte  32: 0x33 0x22 0x11 0x00 0x00 0x00 0x00 0x00
Byte  40: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  48: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  56: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  64: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  72: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  80: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  88: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte  96: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 104: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 112: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 120: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 128: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 136: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 144: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 152: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 160: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 168: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 176: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 184: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 192: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 200: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 208: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 216: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 224: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 232: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 240: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 248: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 256: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 264: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 272: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 280: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 288: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 296: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 304: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 312: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 320: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 328: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 336: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 344: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 352: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 360: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 368: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 376: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 384: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 392: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 400: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 408: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 416: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 424: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 432: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 440: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 448: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 456: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 464: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 472: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 480: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 488: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00
Byte 496: 0x00 0x00 0x00 0x00 0xff 0xff
[root@dhcpe6-sv1-141 ec_4339_driver]#
```

If the cisdump matches the OTP binary map, OTP memory programming is complete. Once programmed, additional blank spaces (00) in the OTP memory can be written by filling in those corresponding blank spaces in the OTP binary map. There is no restriction on how many times a device can be programmed, provided that each programming cycle is writes to only blank, unwritten spaces.

Follow the same procedure to program the additional blank spaces.

# Appendix A: CIS Map

Table 8 and Table 9 list the CIS map (standard tuple tags and Broadcom subtags) for SDIO devices.

Table 8.  Standard Tuple Tags

| Name | Tag | Length | Variable | Description |
|------|-----|--------|----------|-------------|
| CISTPL_VERS_1 | 0x15 | | manf | CIS version, manufacturer, device, and version strings |
| | | | productname | |
| CISTPL_MANFID | 0x20 | 4 | manfid | Manufacturer and device ID |
| | | | prodid | |
| CISTPL_FUNCID | 0x21 | – | – | Function identification |
| CISTPL_FUNCE | 0x22 | – | – | Function extensions |
| CISTPL_FUNCE | 0x22 | 8 | – | Subtype = FUNCE_mac(0x4)<br>Value: 6 byte MAC address |
| CISTPL_CFTABLE | 0x1b | 2 | regwindowsz | Configuration table entry |
| CISTPL_FID_SDIO | 0x0c | – | – | Extensions defined by SDIO specification |
| CISTPL_BRCM_HNBU | 0x80 | – | – | Broadcom-specific tuple subtag identifier |
| CISTPL_END | 0xff | – | – | End of the CIS tuple chain |

Table 9.  Broadcom Tuple Subtags

| Name | Tag | Length | Variable | Description |
|------|-----|--------|----------|-------------|
| HNBU_SROMREV | 0x00 | 1 | sromrev | SROM revision |
| HNBU_CHIPID | 0x01 | 4/6/8/10 | vendid<br>devid<br>chiprev<br>subvendid<br>subdevid<br>boardtype | PCI vendor and device IDs |
| HNBU_BOARDREV | 0x02 | 1/2 | boardrev | Board revision |
| HNBU_AA | 0x06 | 1/2 | aa2g<br>aa5g | Antennas available |
| HNBU_AG | 0x07 | 1/2/3/4 | ag0<br>ag1<br>ag2<br>ag3 | Antenna gain |
| HNBU_BOARDFLAGS | 0x08 | 2/4/6 | boardflags | Board flags |
| HNBU_CCODE | 0x0a | 3 | ccode<br>cctl | Country code (2 bytes ASCII + 1 byte cctl) in rev 2.<br>The cctl means indoor/outdoor, but it is never used. |
| HNBU_ANT5G | 0x0f | 2 | aa5g, ag1 | 5G antennas available/gain |
| HNBU_XTALFREQ | 0x13 | 4 | xtalfreq | Crystal frequency (kilohertz) |
| HNBU_BOARDNUM | 0x18 | 2 | boardnum | Board serial number (independent of MAC address) |
| HNBU_MACADDR | 0x19 | 6 | macaddr | MAC address override for the standard CIS LAN_NID |
| HNBU_BOARDTYPE | 0x1b | 2 | boardtype | Board type |
| HNBU_REGREV | 0x22 | 1 | regrev | – |

Table 9.  Broadcom Tuple Subtags (Continued.)

| Name | Tag | Length | Variable | Description |
|------|-----|--------|----------|-------------|
| HNBU_FEM | 0x23 | 2/4 | antswctl2g(15-11)<br>triso2g(10-8)<br>pdetrange2g(7-3)<br>extpagain2g(2-1)<br>tssipos2g(0)<br>antswctl5g(15-11)<br>triso5g(10-8)<br>pdetrange5g(7-3)<br>extpagain5g(2-1)<br>tssipos5g(0) | – |
| HNBU_CCKFILTTYPE | 0x36 | 1 | cckdigfilttype | CCK digital filter selection option |
| HNBU_CCKBW202GPO | 0x41 | 4(max) | cckbw202gpo<br>cckbw20ul2gpo | CCK Power offsets for 20 MHz rates (11, 5.5, 2, 1 Mbps) |
| HNBU_MCS5GLPO | 0x45 | 12(max) | mcsbw205glpo<br>mcsbw20ul5glpo<br>mcsbw405glpo | MCS 0-7 power-offset<br>LSB Nibble: m0<br>MSB nibble: m7 |
| HNBU_MCS5GMPO | 0x46 | 12(max) | mcsbw205gmpo<br>mcsbw20ul5gmpo<br>mcsbw405gmpo | MCS 0-7 power-offset<br>LSB Nibble: m0<br>MSB Nibble: m7 |
| HNBU_MCS5GHPO | 0x47 | 12(max) | mcsbw205ghpo<br>mcsbw20ul5ghpo<br>mcsbw405ghpo | MCS 0-7 power-offset<br>LSB Nibble: m0<br>MSB Nibble: m7 |
| HNBU_MUXENAB | 0x56 | 1 | muxenab | Enable mux options |
| HNBU_ACPA_C0 | 0x59 | 38 | subband5gver<br>maxp2ga0<br>pa2ga0<br>maxp5ga0<br>pa5ga0 | Subband 5GHz<br>Maximum power, PA parameters for chain 0 |
| HNBU_PDOFF | 0x5d | 12 | pdoffset40ma0<br>pdoffset40ma1<br>pdoffset40ma2<br>pdoffset80ma0<br>pdoffset80ma1<br>pdoffset80ma2 | PD offsets |
| HNBU_ACPPR_2GPO | 0x5e | 4 | dot11agofdmhrbw202gpo<br>ofdmlrbw202gpo | 2G power offsets |
| HNBU_ACPPR_5GPO | 0x5f | 30 | mcsbw805glpo<br>mcsbw1605glpo<br>mcsbw805gmpo<br>mcsbw1605gmpo<br>mcsbw805ghpo<br>mcsbw1605ghpo<br>mcslr5glpo<br>mcslr5gmpo<br>mcslr5ghpo | 5G power offsets |

Table 9.  Broadcom Tuple Subtags (Continued.)

| Name | Tag | Length | Variable | Description |
|------|-----|--------|----------|-------------|
| HNBU_ACPPR_SBPO | 0x60 | 32 | sb20in40hrpo<br>sb20in80and160hr5glpo<br>sb40and80hr5glpo<br>sb20in80and160hr5gmpo<br>sb40and80hr5gmpo<br>sb20in80and160hr5ghpo<br>sb40and80hr5ghpo<br>sb20in40lrpo<br>sb20in80and160lr5glpo<br>sb40and80lr5glpo<br>sb20in80and160lr5gmpo<br>sb40and80lr5gmpo<br>sb20in80and160lr5ghpo<br>sb40and80lr5ghpo<br>dot11agduphrpo<br>dot11agduplrpo | Subband power offsets |
| HNBU_RXGAIN_ERR | 0x62 | 15 | rxgainerr2ga0<br>rxgainerr2ga1<br>rxgainerr2ga2<br>rxgainerr5ga0<br>rxgainerr5ga1<br>rxgainerr5ga2 | Rx gain error |
| HNBU_AGBGA | 0x63 | 6 | agbg0<br>agbg1<br>agbg2<br>aga0<br>aga1<br>aga2 | Antenna gain G band |
| HNBU_ACRXGAINS_C0 | 0x67 | 4 | rxgains for chain 1<br>(rxgains5gtrelnabypa0<br>rxgains5gtrisoa0<br>rxgains5gelnagaina0<br>rxgains2gtrelnabypa0<br>rxgains2gtrisoa0<br>rxgains2gelnagaina0<br>rxgains5ghtrelnabypa0<br>rxgains5ghtrisoa0<br>rxgains5ghelnagaina0<br>rxgains5gmtrelnabypa0<br>rxgains5gmtrisoa0<br>rxgains5gmelnagaina0) | Word offset 112, 113 |
| HNBU_TXDUTY | 0x6a | 8 | tx_duty_cycle_ofdm_40_5g<br>tx_duty_cycle_thresh_40_5g<br>tx_duty_cycle_ofdm_80_5g<br>tx_duty_cycle_thresh_80_5g | Maximum Tx duty cycle for OFDM rate below threshold (in 500 Kbps) in AC 5G 40/80 band. |
| HNBU_PDOFF_2G | 0x6c | 2 | pdoffset2g40ma0<br>pdoffset2g40ma1<br>pdoffset2g40ma2<br>pdoffset2g40mvalid | 2G PD offset. |
| HNBU_TEMPTHRESH | 0x3A | 2/6 | tempthresh 1byte<br>temps_hysteresis 4 bits<br>temps_period 4 bits<br>tempoffset 8 bits<br>tempsenseslope 8 bits<br>tempcorrx 6 bits,<br>tempsense_option 2 bits<br>phycaltempdelta | Sets the values for temperature threshold, period, and hysteresis. |

Table 9.  Broadcom Tuple Subtags (Continued.)

| Name | Tag | Length | Variable | Description |
|------|-----|--------|----------|-------------|
| HNBU_ACPAPARAM | 0x84 | 85 | pa2ga0<br>pa5pa0<br>pa2ga1<br>pa5ga1<br>pa5ga2 | Enables PA trimming WAR for multiple BW support. |

# Document History Page

| | | | | |
|---|---|---|---|---|
| **Document Title: AN215294 - CYW4335 OTP Programming and NVRAM** | | | | |
| **Document Number: 002-15294** | | | | |
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | - | - | 03/18/2013 | 4335-AN200-R<br>Initial Release |
| *A | - | - | 05/03/2013 | 4335-AN201-R<br>Updated<br>• Table 2, "NVRAM Parameters Requiring Customizing,"<br>• Figure 2: "BCM4335 Hexadecimal OTP Binary Map Template,<br>Figure 3: "An Example of a wl cisdump Output, |
| *B | 5459791 | UTSV | 10/03/2016 | Added Cypress Part Numbering Scheme.<br><br>Updated to Cypress format. |
| *C | 5834576 | BENV | 07/27/2017 | Updated logo and copyright |

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