Further Consideration on the Concatenated FEC for 800G FR4 and LR4

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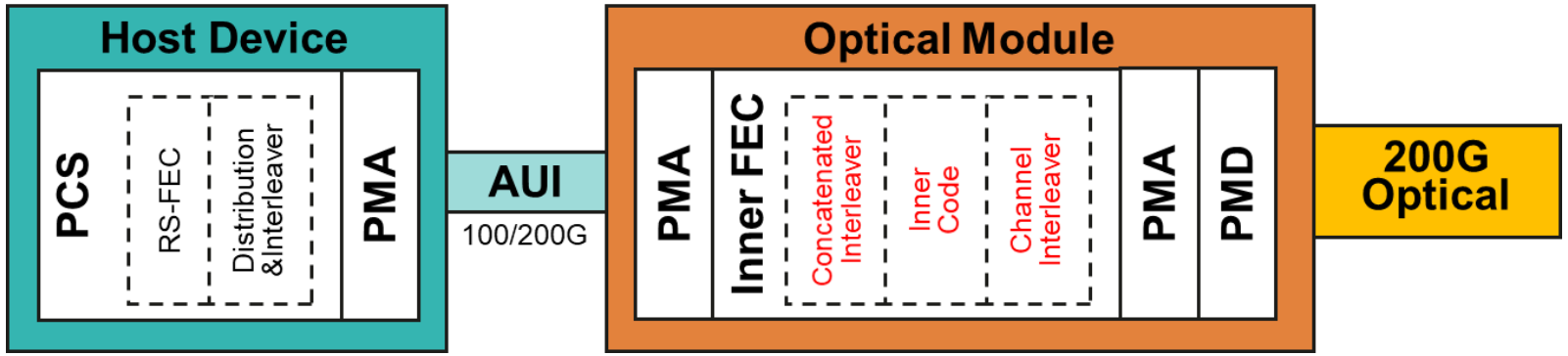
- Maxim Kuschnerov, Huawei
- Xiang Liu, Huawei
- Arash Farhood, Marvell
- Jamal Riani, Marvell

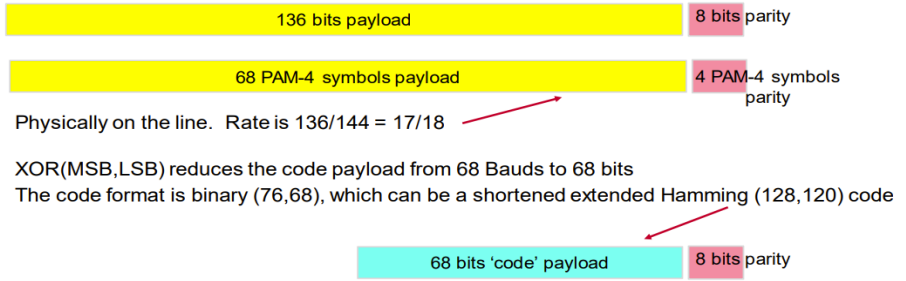
Background (1/2)



- This presentation is following up on a previous presentation, huang_3df_01_221011, in Oct 2022 Session
  - Continue to discuss the consideration on concatenated FEC for 800G FR4 and LR4
- In the concatenated FEC solution, concatenated interleaver (placed between inner and outer code) can be introduced to achieve a better performance
  - The NCG performance vs. latency was discussed in bliss_3df_01a_220517
  - Motivated by the idea in patra_3df_01a_2207, one class of concatenated interleaver comprised of "Lane MUX" and "Convolutional interleaver" was proposed in huang_3df_01_221011
- Channel interleaver can be used to decorrelate the noise introduced in the optical medium
  - bliss_3df_01_220929 proposes the 4-way or 8-way Hamming baud interleaving

Background (2/2)

- Soft inner code with short code length can be used to achieve low latency
  - Hamming(128,120) with rate 15/16 was proposed in bliss_3df_01a_220517, patra_3df_01a_2207, resulting in baud rate 113.33 GB
  - Hamming(144,136) with rate 17/18 was proposed in he_3df_01a_220308, resulting in baud rate 112.5 GB (=720x156.25 MHz)
  - bliss_3df_01_220929 suggested the baud rate being a multiple of 156.25 MHz (crystal reference), and proposed a "compromise" inner Hamming coding method to achieve rate 17/18, which can be viewed as a specific binary(144,136) code



From bliss_3df_01_220929

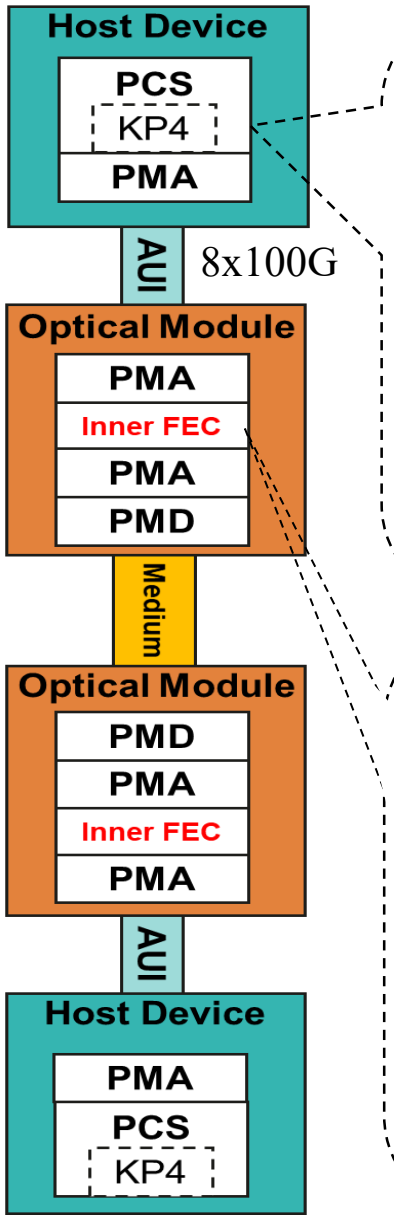
Inner codes	Inner codes Rate	Baudrate	Baudrate/156.25M
Hamming(128,120)	15/16	113.333..G	725.33…
Hamming(144,136)	17/18	112.5G	720
Binary(144,136) in bliss_3df_01_220929	17/18	112.5G	720

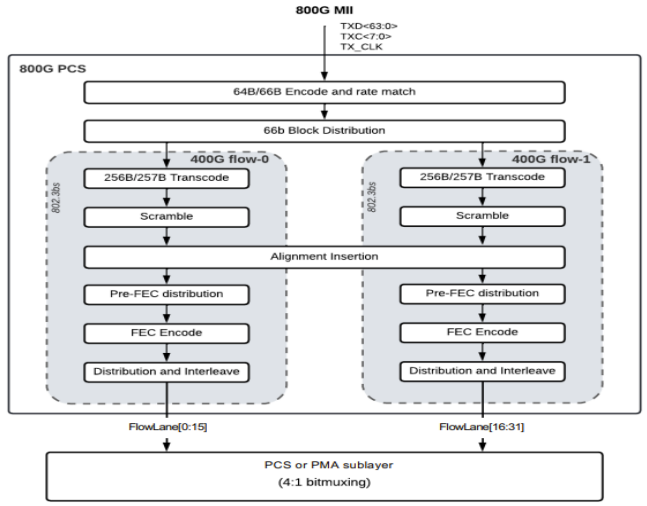
- In previous contributions, the baud rate of concatenated solutions were calculated assuming no additional overhead (other than the inner code overhead) is introduced in the optical module
  - Need to be evaluated carefully for the specific inner code designs, taking into account the functionality of the receiver optical module

First Part:

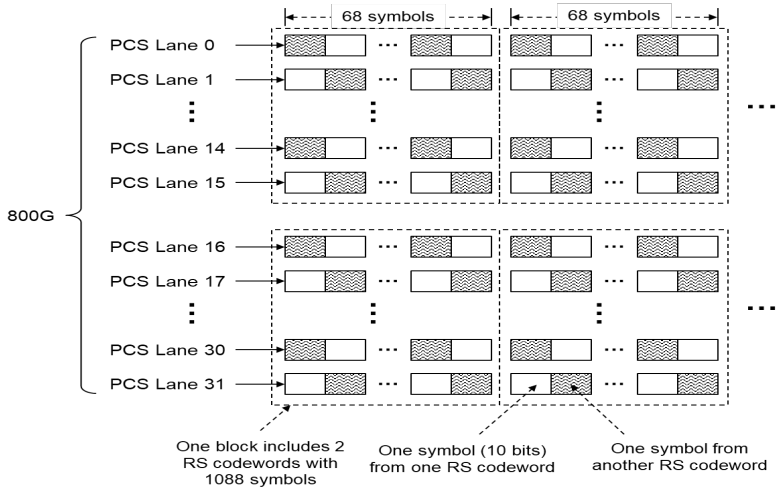
Design the concatenated FEC solution by taking into account the functionality of the receiver optical module

Concatenated FEC Solution in huang_3df_01_221011

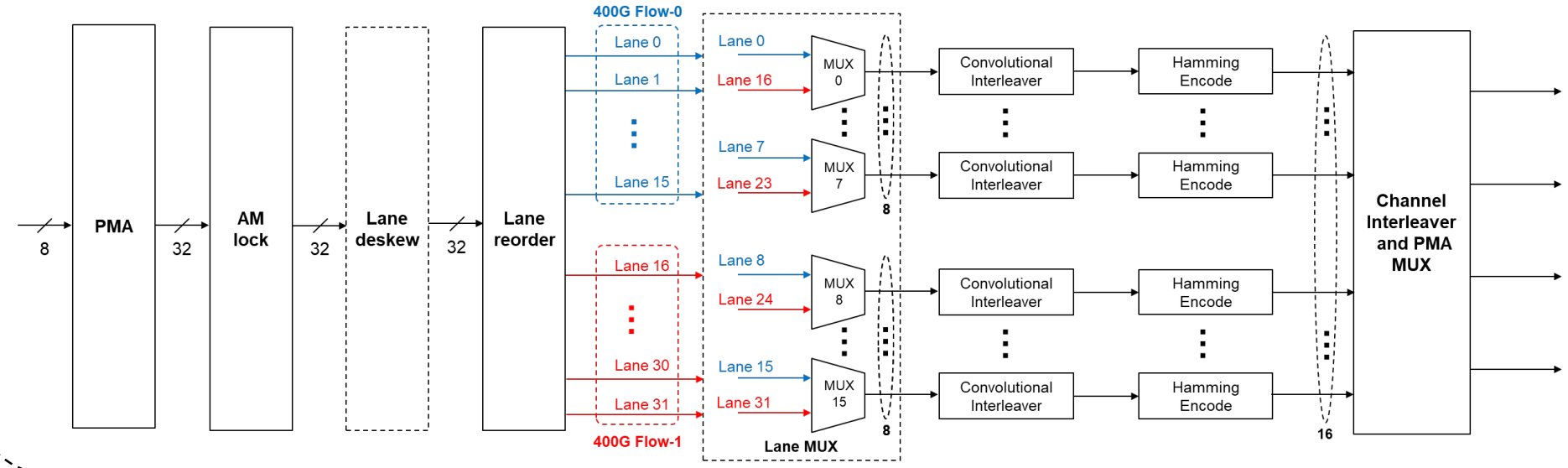




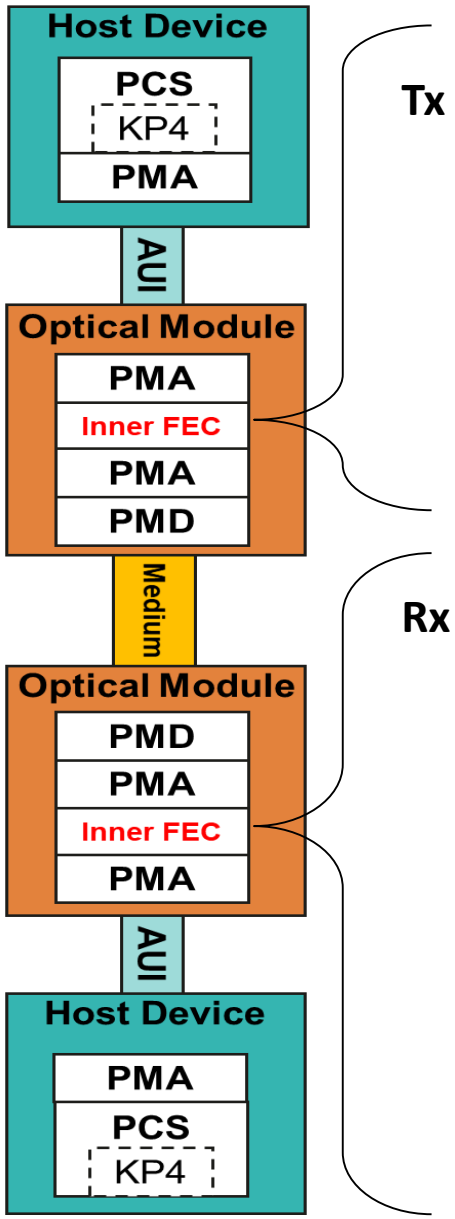
From [shrikhande_3df_01a_221004]

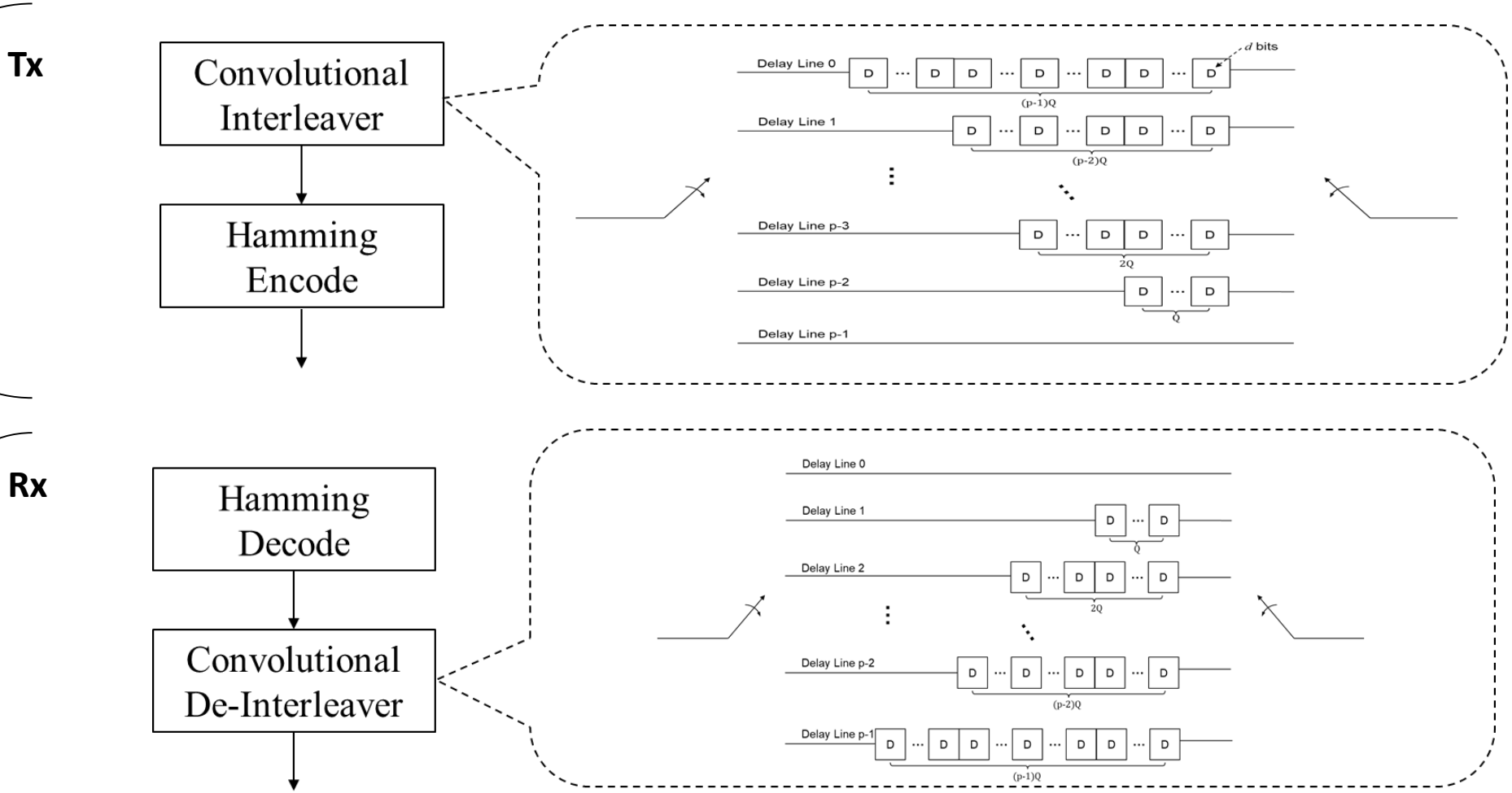


Details on the PCS bit streams



Consideration on Inner codes of Concatenated FEC

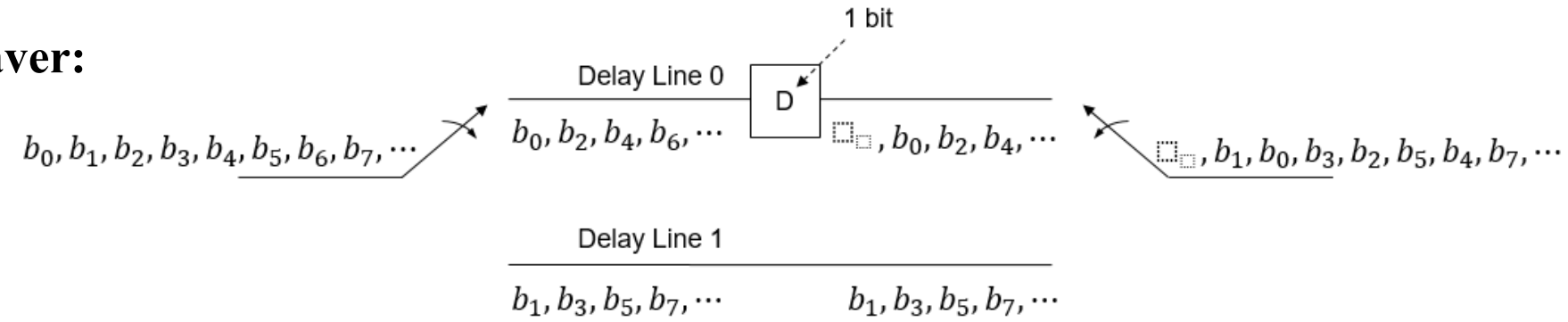




- On the Rx side, the Hamming codeword boundary should be recognized before Hamming decoding operation, which can be achieved by having the codeword synchronization
- The input and output switches of the FEC convolutional de-interleaver should be identified before convolutional de-interleaver operation.

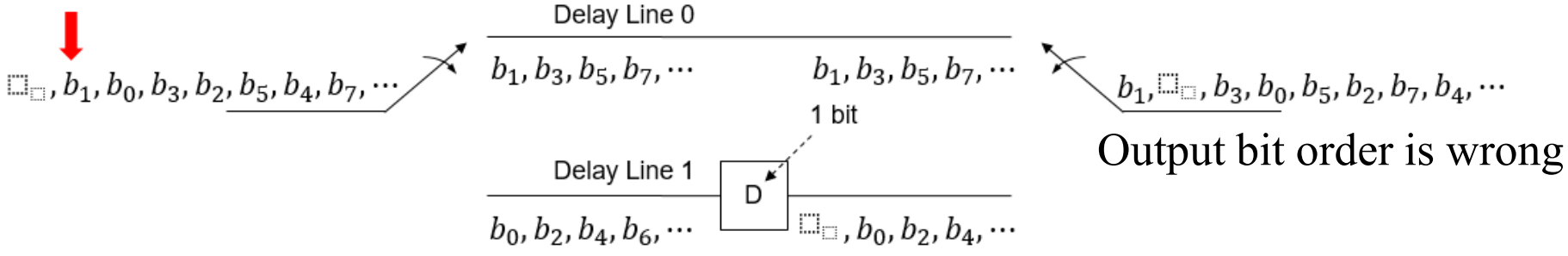
Toy Example: Convolutional Interleaver and De-Interlevaer

Convolutional Interleaver:



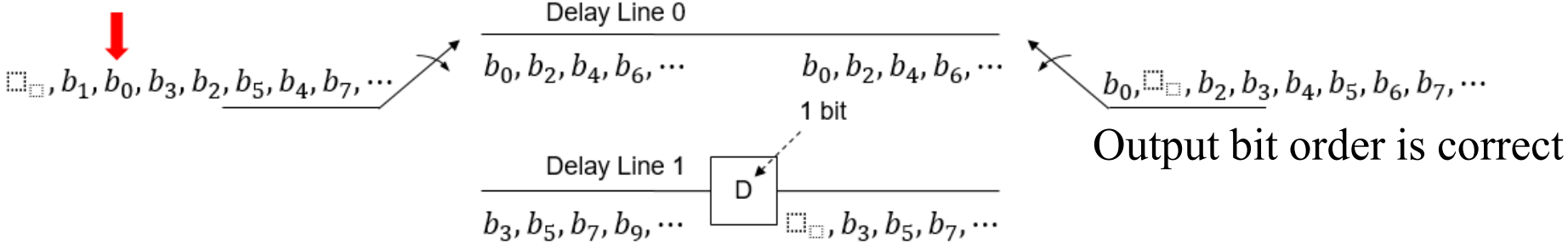
Convolutional De-Interleaver:

Option 1 for the input and output switches



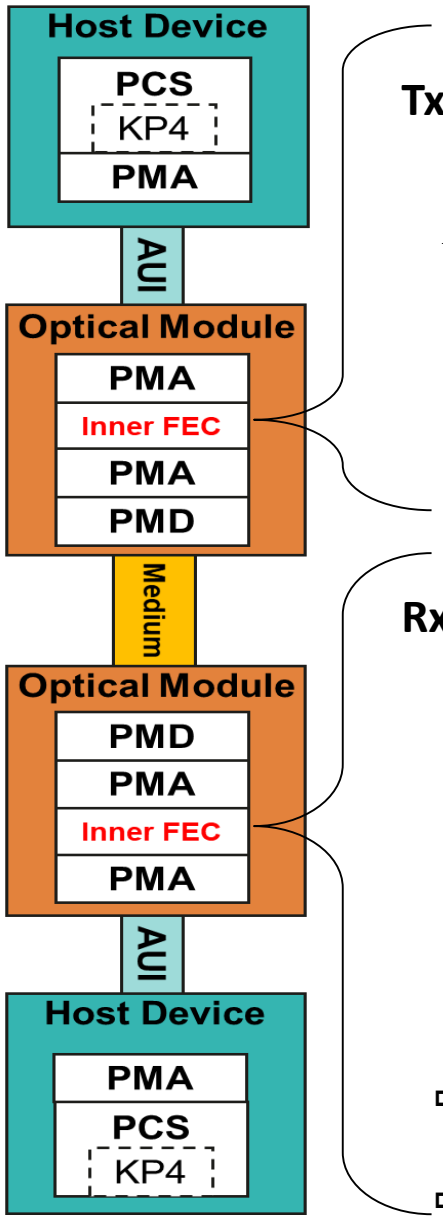
Output bit order is wrong

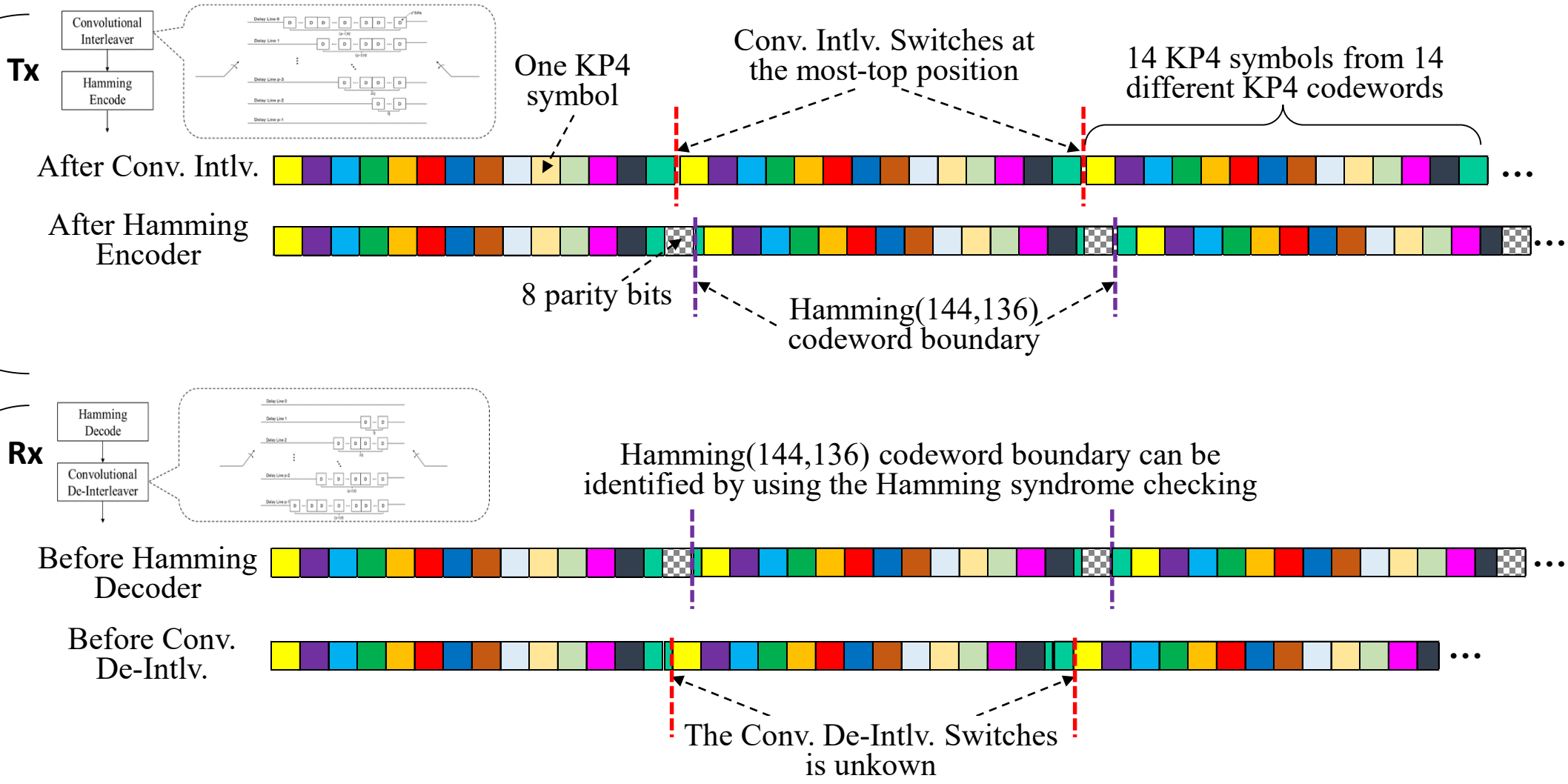
Option 2 for the input and output switches



Output bit order is correct

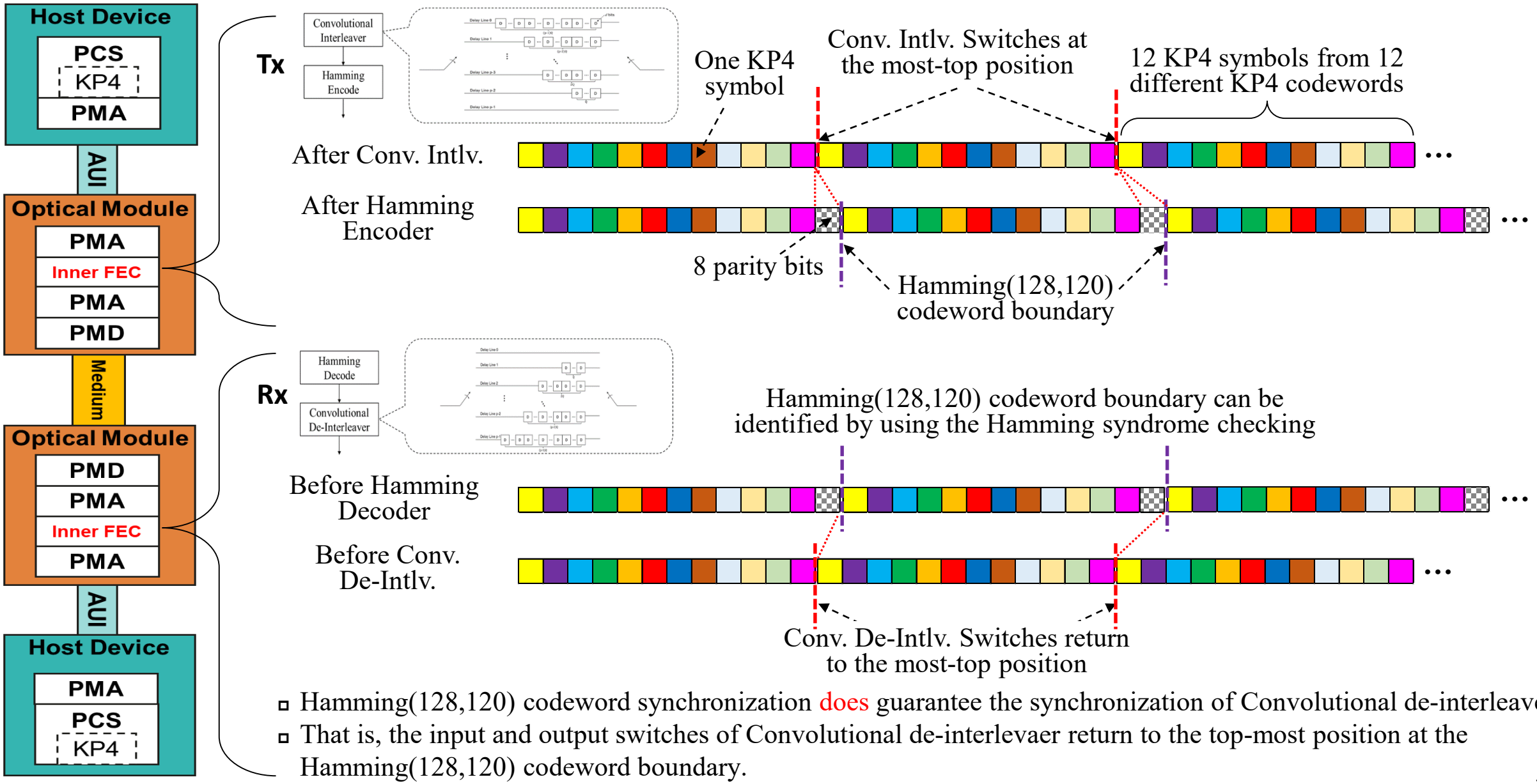
Consideration on KP4+Hamming(144,136)





- On the Rx side, Hamming(144,136) codeword synchronization does not guarantee the synchronization of convolutional de-interleaver. That is, the input and output switches of convolutional de-interleaver is unknown.
- The KP4 + Hamming(144,136) or Binary(144,136) solution needs more clarification and improvement.

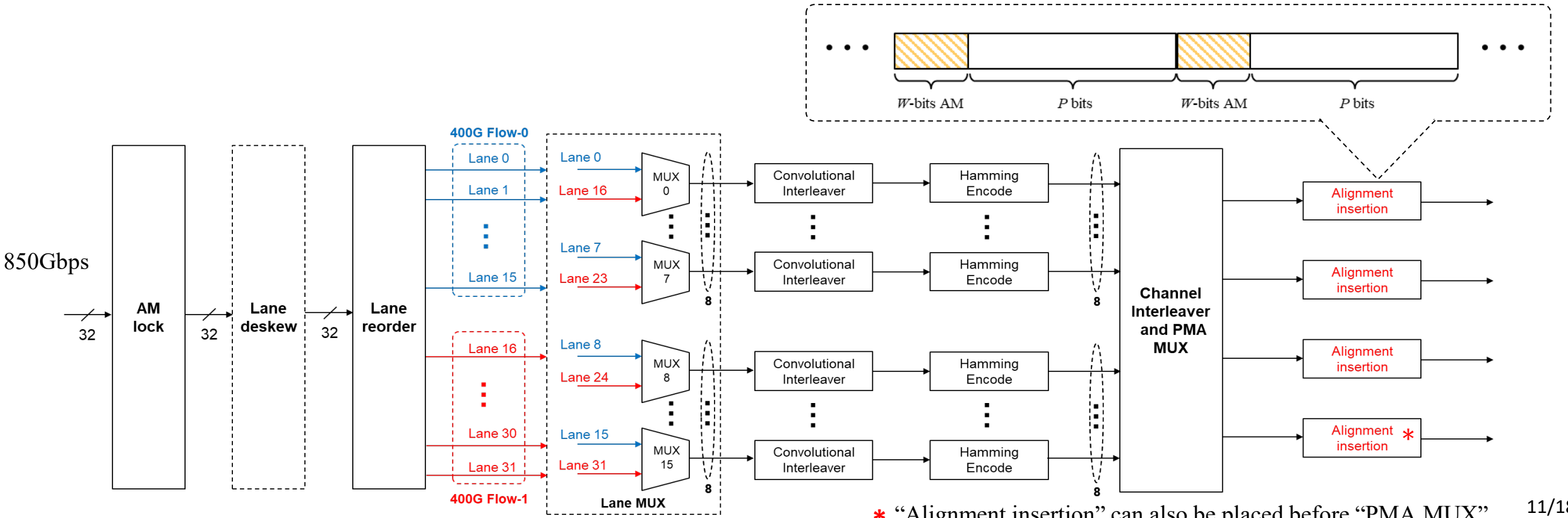
Details on KP4+Hamming(128,120)



- Hamming(128,120) codeword synchronization does guarantee the synchronization of Convolutional de-interleaver.
- That is, the input and output switches of Convolutional de-interlevaer return to the top-most position at the Hamming(128,120) codeword boundary.

Discussion on KP4+Hamming(128,120)

- If the Task Force prefers baud rate being a multiple of the 156.25 MHz, in the KP4 + Hamming(128,120) solution, a small overhead can be added after Hamming encoding to satisfy this baud rate constraint
  - The added overhead can be thought of as "alignment insertion": by adding W alignment bits per P bits, where $850\text{G} \times \frac{128}{120} \times \frac{W+P}{P} \times \frac{1}{8}$ is a multiple of 156.25 M
  - For example, $W = 64$, $P = 69632$, the corresponding baud rate is $850\text{G} \times \frac{128}{120} \times \frac{64+69632}{69632} \times \frac{1}{8} = 113.4375$ Gbaud (= 726 × 156.25 MHz)

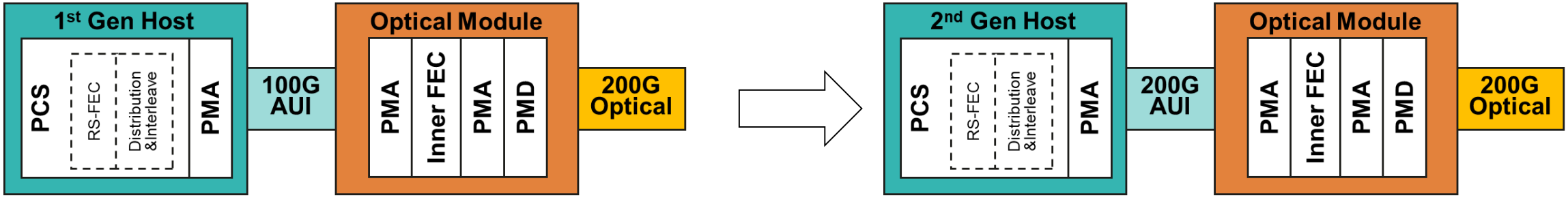


* "Alignment insertion" can also be placed before "PMA MUX".

Second Part:

Designing the concatenated FEC solution with forward compatibility

Evolution on 800G Concatenated FEC



First Generation Development based on 100G/lane AUI

Second Generation Development based on 200G/lane AUI

- The first generation development of 800G concatenated FEC is expected to be based on 100G/lane AUI, while the second generation is expected to be based on 200G/lane AUI
  - More detailed discussion on 800G evolution with Concatenated FEC can be found in ghiasi_3df_02a_2207
  - The 800G host for 100G-AUI has two 400G FEC flows, and 32 PCS lanes, see shrikhande_3df_01a_221004
  - The 800G host for 200G-AUI will be discussed in the Task Force
- Suggest to consider potential forward compatibility of the concatenated FEC solution
  - In optical module, the second generation development based on 200G/lane AUI of concatenated FEC solution can maximize reuse in hardware design and standard specifications of the first generation development based on 100G/lane AUI

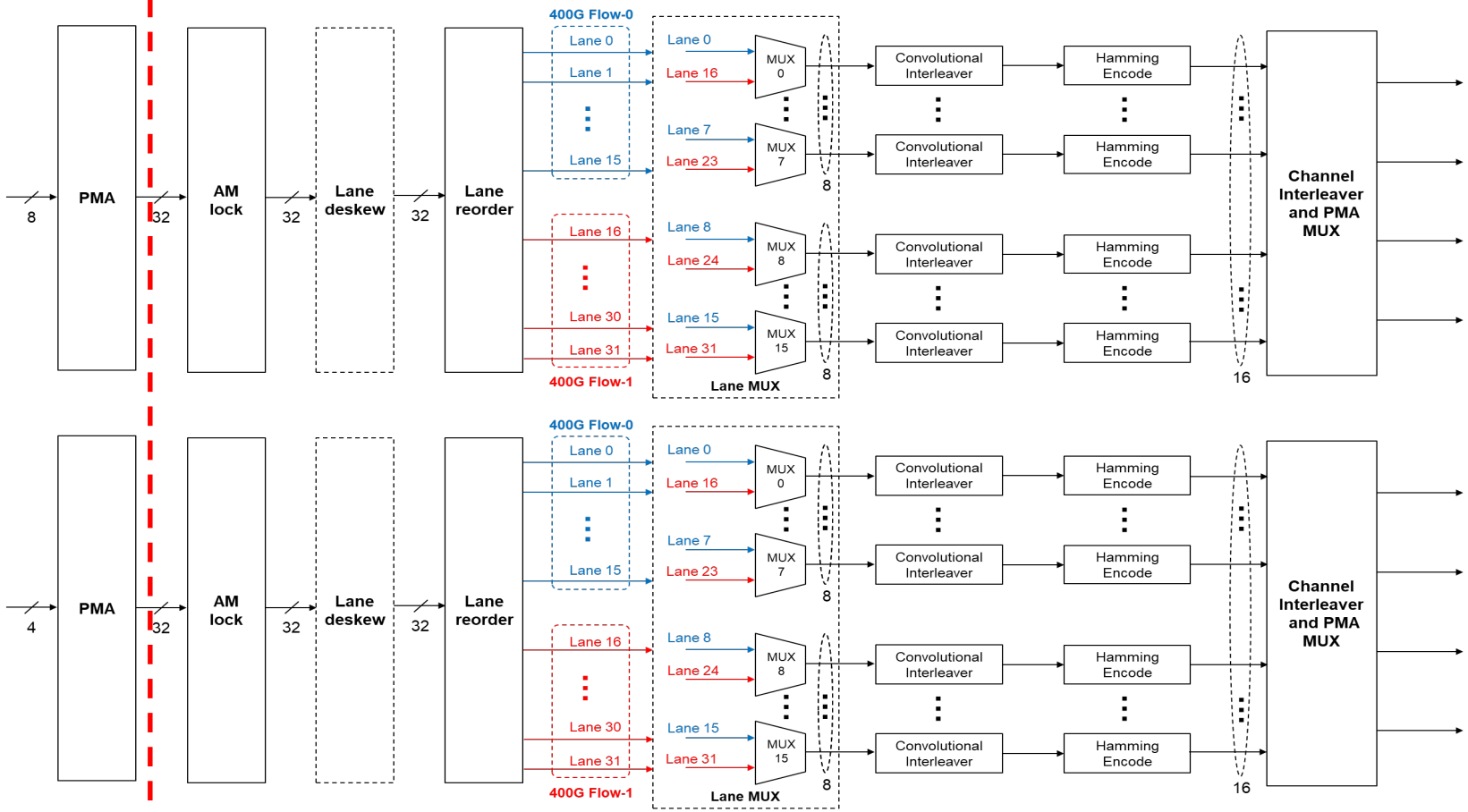
Potential Second Gen. Development for 200G-AUI (1/3)

- Potential Case 1: If the PCS definition in 800G host for 200G-AUI is the same as that for 100G-AUI (32 PCS lanes), the functions after PMA in second generation development in optical module can be the same as that in first generation development.

maximize reuse in hardware design and standards specification

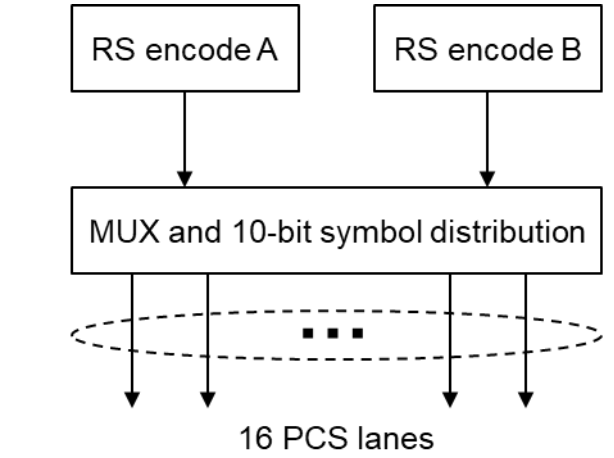
First Gen. Development for 100G-AUI:

Second Gen. Development for 200G-AUI:



Potential Second Gen. Development for 200G-AUI (2/3)

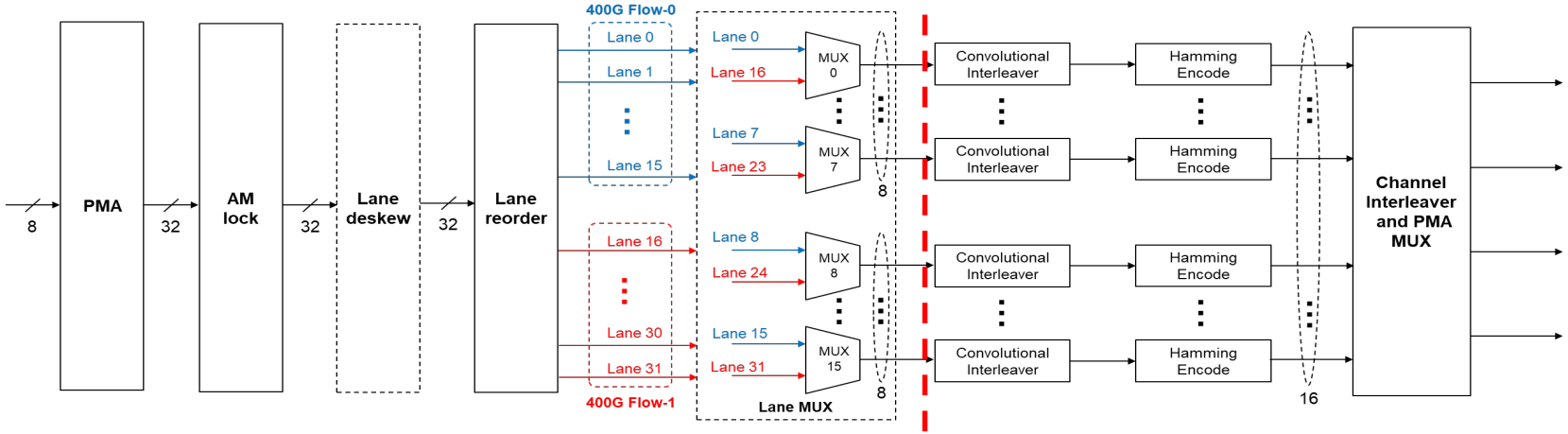
- Potential Case 2: If the PCS definition in 800G host for 200G-AUI is different than that for 100G-AUI, say 2X speed-up Clause 119 based on 400GbE with 16 PCS lanes.



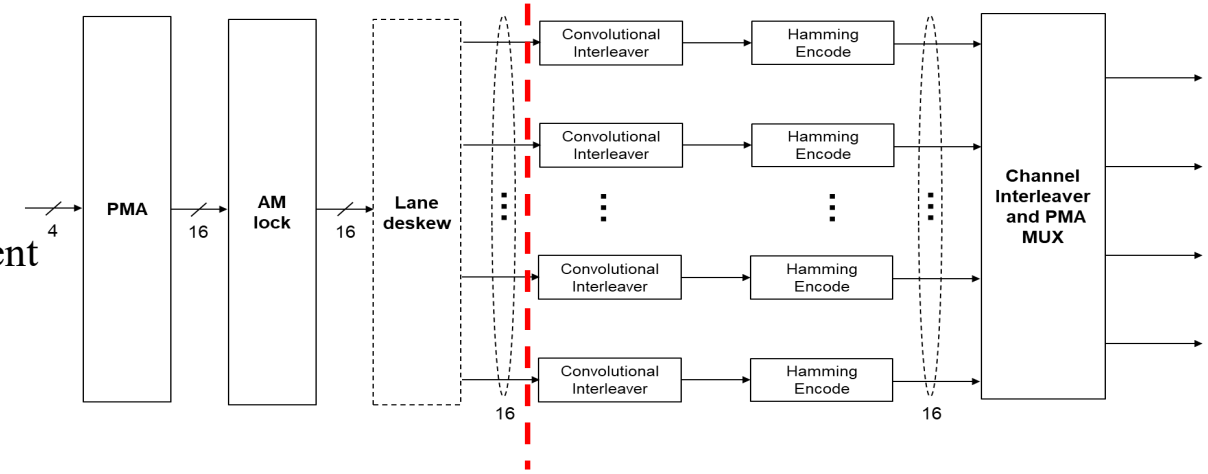
2X speed-up Clause 119 based on 400GbE

maximize reuse in hardware design and standards specifications

First Gen. Development for 100G-AUI:



Second Gen. Development for 200G-AUI:

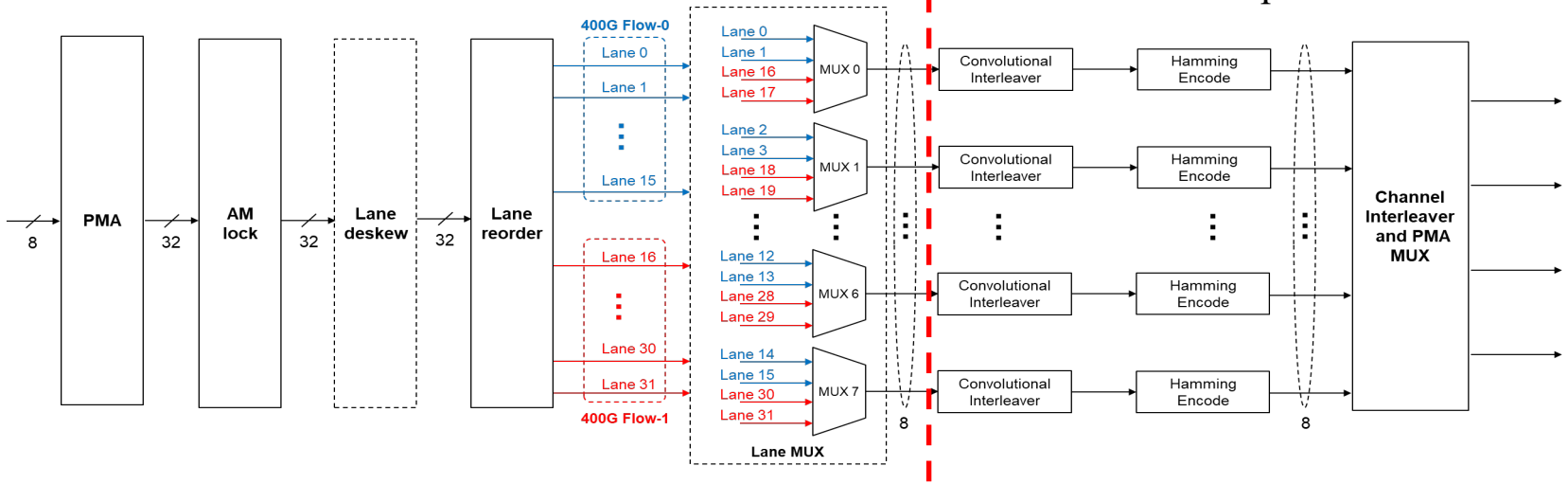


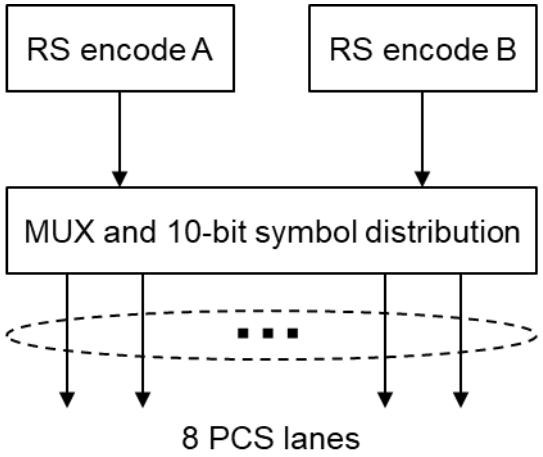
Potential Second Gen. Development for 200G-AUI (3/3)

- Potential Case 3: If the PCS definition in 800G host for 200G-AUI is different than that for 100G-AUI, say 4X speed-up Clause 119 based on 200GbE with 8 PCS lanes.
- The "Lane MUX" will multiplex 4 input lanes into 1 output lane.

maximize reuse in hardware design and standards specifications

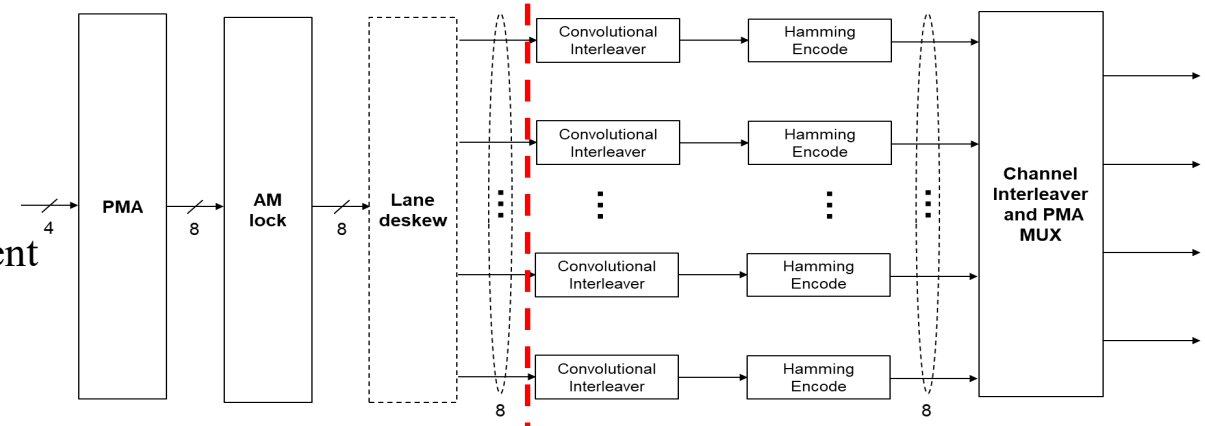
First Gen. Development for 100G-AUI:





4X speed-up Clause 119 based on 200GbE

Second Gen. Development for 200G-AUI:



Summary and Conclusions

- Concatenated FEC is discussed by taking into account the functionality of the receiver optical module
- KP4 + Hamming(144,136) solution needs more clarification and improvement
  - Hamming(144,136) codeword synchronization does not guarantee the synchronization of convolutional de-interleaver
  - More overhead in optical module need to be added for the synchronization of convolutional de-interleaver
  - The same comment also applied to the solution using Binary(144,136) inner code proposed in bliss_3df_01_220929
- KP4 + Hamming(128,120) solution has simple synchronization processing in Rx side
  - Hamming(128,120) codeword synchronization does guarantee the synchronization of convolutional de-interleaver
- If the Task Force prefers baud rate being a multiple of the 156.25 MHz, a small overhead as “alignment insertion” can be added after the Hamming encoding in KP4 + Hamming(128,120) solution
- The proposed KP4 + Hamming architecture, where concatenated interleaver includes “Lane MUX” and “convolutional interleaver”, has good forward compatibility
  - In the optical module, the second generation development based on 200G/lane AUI can maximize reuse in hardware design and standard specifications of the first generation development based on 100G/lane AUI

Thank you