SATURN V

Simplex Models

Laboratory Maintenance Instructions for LVDA

Volume I

Description and Theory

Space Guidance Center, Owego, New York IBM

VOLUME I OF II

Laboratory Maintenance Instructions

SATURN V
LAUNCH VEHICLE DATA ADAPTER

Simplex Models

NASA Part No. 50M35011
IBM Part Nos. 6112050 and 6112070

International Business Machines Corporation

Contract NAS 8-11561

VOLUME I OF II

GENERAL DESCRIPTION AND THEORY

26 FEBRUARY 1965

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

TOTAL NUMBER OF PAGES IN VOLUME I, OF THIS PUBLICATION IS 140 CONSISTING OF THE FOLLOWING:

Page No.	Issue
Title	Original
A	Original
i	Original
ii Blank	Original
iii thru v	Original
vi Blank	Original
vii thru viii	Original
1-1 thru 1-13	Original
1-14 Blank	Original
2-1 thru 2-68	Original
Glossary-1 thru -16	Original
Symbols-1 thru -30	Original
Index-1 thru -2	Original

*The asterisk indicates pages changed, added, or deleted by the current change.

NOTICE

Section V of this manual includes procedures which require the use of the Purging Cart (Tool Number 657900) and the Transport Dolly (Tool Number 656360). As of the publication date of this manual, this equipment has not been delivered; therefore the procedures cannot be performed. Although the procedures have not been verified on the equipment they have been included in the manual for informational purposes.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont)

LIST OF ILLUSTRATIONS (cont)

LIST OF RELATED MANUALS

Manual Title

Technical Manual, Laboratory Maintenance Instructions, Launch Vehicle Digital Computer (Simplex Models)

Technical Manual, Checkout Procedures, Saturn Launch Vehicle Digital Computer and Data Adapter

Technical Manual, Laboratory Maintenance Instructions, Saturn V Test Equipment

Signal Routing Lists, LVDA Simplex Models

(To be Supplied.)

Figure i. Launch Vehicle Data Adapter

SECTION I

INTRODUCTION AND DESCRIPTION

1-1. INTRODUCTION.

1-2. SCOPE.

1-3. This section describes the purpose and general features of this manual and the salient features and physical construction of the Launch Vehicle Data Adapter.

1-4. PURPOSE OF MANUAL.

1-5. This manual contains laboratory maintenance instructions for the simplex models of the Launch Vehicle Data Adapter (LVDA), NASA part number 50M35011, IBM part numbers 6112050 and 6112070, manufactured by International Business Machines Corporation, Federal Systems Division, Rockville, Maryland, under contract number NAS 8-11561. (See frontispiece.) In the remainder of this manual, the Launch Vehicle Data Adapter will be referred to as the data adapter.

1-6. This manual is divided into two volumes. Volume I, "General Description and Theory", describes the structure, contents and operation of the data adapter. Volume II, "Maintenance Data", contains all procedures for handling, troubleshooting and repairing the data adapter. Also included in volume II are detailed logic diagrams for analysis and signal tracing. Schematics are supplanted by signal routing lists (see List of Related Manuals) which are not included as part of this manual, but are provided separately. Logic diagrams typical of all data adapter circuits are provided with the descriptive material in volume I. Reference to corresponding detailed logic diagrams in volume II may be made through the index.

1-7. The index and appendices to this manual are provided in volume I. Included with the appendices are a number of comment sheets. Notice of any errors or omissions should be entered on one of these sheets and mailed to the address shown at the beginning of the comment sheets.

1-8. Inserted in the binder pocket of this manual is a plasticized timing diagram. This diagram is a duplicate of a diagram in the manual, and is included for convenient reference. Additional reference data is located on the back of the timing diagram.

1-9. The manual is divided into ten sections whose titles convey the layout of data in a general way. Specific data may be located in the index.

1-10. PURPOSE OF EQUIPMENT.

1-11. The simplex models of the data adapter consist of breadboard model I (6112050) and breadboard model II (6112070). The simplex models are engineering demonstration and evaluation models of a unit which will be part of the Saturn V Launch Vehicle Guidance System. In its ultimate form, the data adapter will adapt guidance system signals for use by the Launch Vehicle Digital Computer (LVDC), and will convert the computer output signals to a form usable by the guidance system. In addition, the data adapter will store computer and system data for subsequent telemetering, and will accumulate real-time and accelerometer data.

1-12. The ultimate version of the data adapter will contain triplicated circuits for reliability. Except for a few demonstration circuits, the simplex models are equipped with only a single set of circuits.

1-13. The breadboard I and breadboard II models of the data adapter are electrically identical. The physical construction of the two models is similar, except that the breadboard II model is liquid cooled, whereas the breadboard I model is forced-air cooled. The descriptions in this manual are for the breadboard II model data adapter. Differences are noted in the discussion.

1-14. STRUCTURAL DESCRIPTION. (See figure 1-1.)

1-15. GENERAL. The data adapter consists of three oblong frames which are stacked sandwich-fashion to form the complete unit. The two outer frames contain logic circuits and, accordingly, are called logic sections. The middle frame contains power circuits and is called the power section.

1-16. All the frames of the breadboard II model have been drilled to form small passageways for the flow of liquid coolant. The coolant enters and leaves the data adapter through couplings mounted on each end of the power section. Flexible hose assemblies carry the coolant from the power section to the logic sections.

1-17. Electrical connections between the power section and the logic sections are provided primarily by flat, flexible, printed cable assemblies called tape cables. (Some additional connections are provided through standard wire cables.)

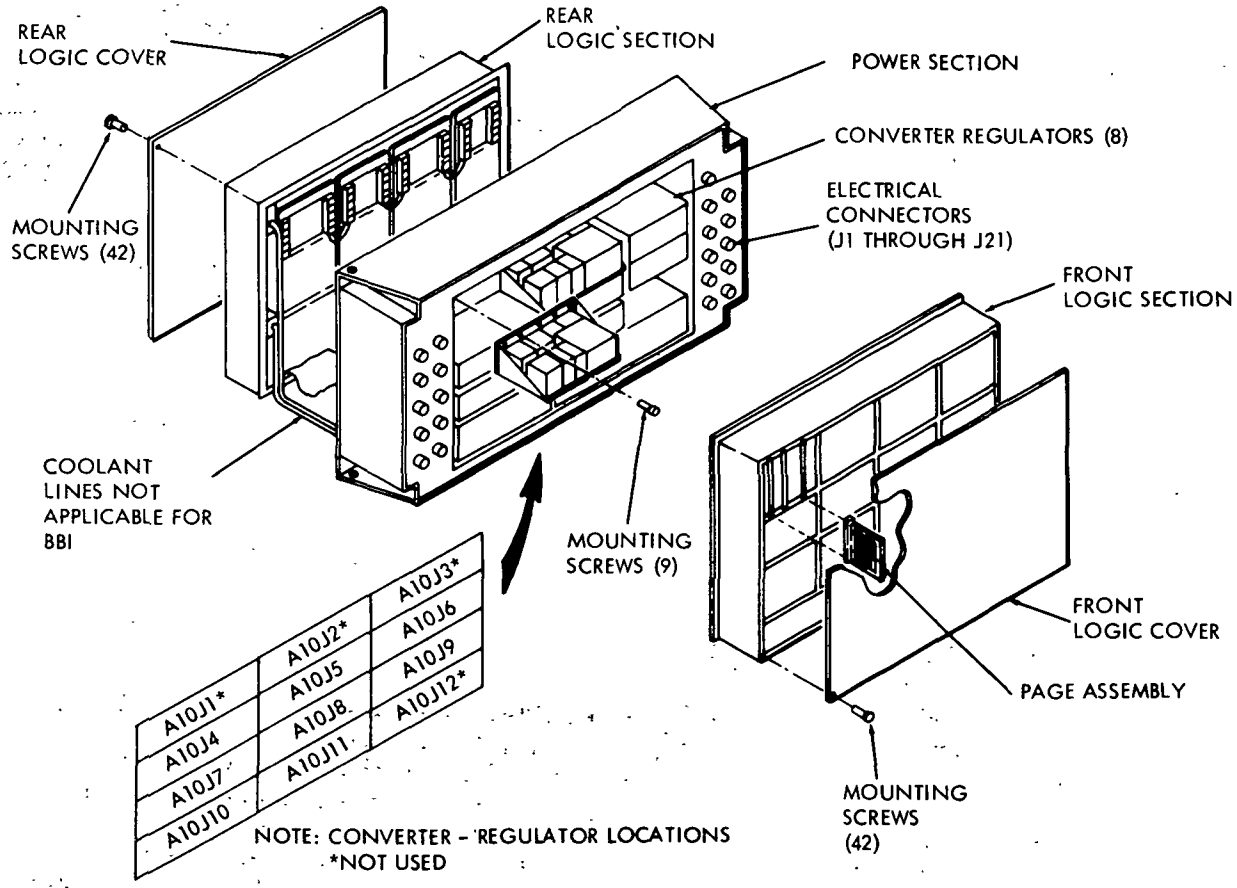


Figure 1-1. Data Adapter Exploded View

1-18. The coolant hose assemblies and the tape cables and wiring are situated at one end of the data adapter so that the logic sections may be opened like clamshells for access to the power section and to the inner sides of the logic sections.

1-19. Electrical connections to and from the data adapter itself are made through 21 system connectors mounted at the ends of the power section.

1-20. The maximum dimensions of both simplex models of the data adapter are 32" by 16-1/4" by 14-3/4". The breadboard model I weighs about 222 pounds and the breadboard model II weighs about 166 pounds.

1-21. LOGIC SECTIONS. Logic circuits in the data adapter are packaged in two basic forms: the unit logic device (ULD) and the circuit module (CM). The unit logic device consists of a 3/10 inch square ceramic wafer on which is deposited a printed wiring pattern and various deposited-film resistors (as required). Fused to the printed wiring at appropriate points are semiconductor "chips". All the components are covered with a potting compound, and the ULD is capped with a plastic wafer on which is imprinted the ULD identification code. Electrical connections to the ULD are made through 14 contacts (7 on each of two sides) along the bottom edge of the ULD. The contacts are referred to as pads.

1-22. The circuit module consists of a metal container in which is encapsulated various circuit components too large for ULDs. The average circuit module measures 1-1/4" long by 1/2" wide, and is approximately 1" high. The top of the module is covered with a sealing compound on which is imprinted the circuit module identification code. Connections to the circuit module are made through 16 pins which protrude from the bottom.

1-23. Both the unit logic devices and the circuit modules are electrically interconnected to one another by multilayer interconnection boards (MIBs). The multilayer interconnection board consists of a number of printed wiring sheets bonded together. Connections between sheets are made by flowing solder through holes drilled through the board at points where desired "lands" coincide. (A land is the pattern of metal which makes up the printed wiring.) Because of differences in the manner of mounting, separate MIBs are used for unit logic devices and circuit modules.

1-24. The unit logic devices are fused to 14-pad patterns on their MIBs. The ULD-type MIBs have 35 locations for ULDs, although not all locations are always used. The circuit modules are fastened to their MIBs by their 16 connector pins which protrude through holes in the MIB and are soldered in place. In addition, a screw extends through the MIB and into a tapped hole in the circuit module.

1-25. Connections to and from the MIB are made through 49 lands (connector lands) at one end of the MIB and 30 lands (thru-pin lands) at the other end. Test points are provided by 18 heavy lands, 9 on each side of the thru-pin lands.

1-26. MIBs are assembled into a frame with a pluggable connector to form a page assembly (figure 1-2). The page assembly consists of a page frame, a 98-pin connector, two guide pins, two captive screws, and either one or two MIBs and MIB insulators. The page assembly may also contain up to 30 thru-pins.

1-27. The connector is fastened to the page frame by the guide pins. The MIB insulator is positioned on the side of the page frame with both the page connector pins and the thru-pins projecting through its clearance holes. The MIB fits over the insulator with the pins projecting through holes in its connector and thru-pin lands. Solder is flowed

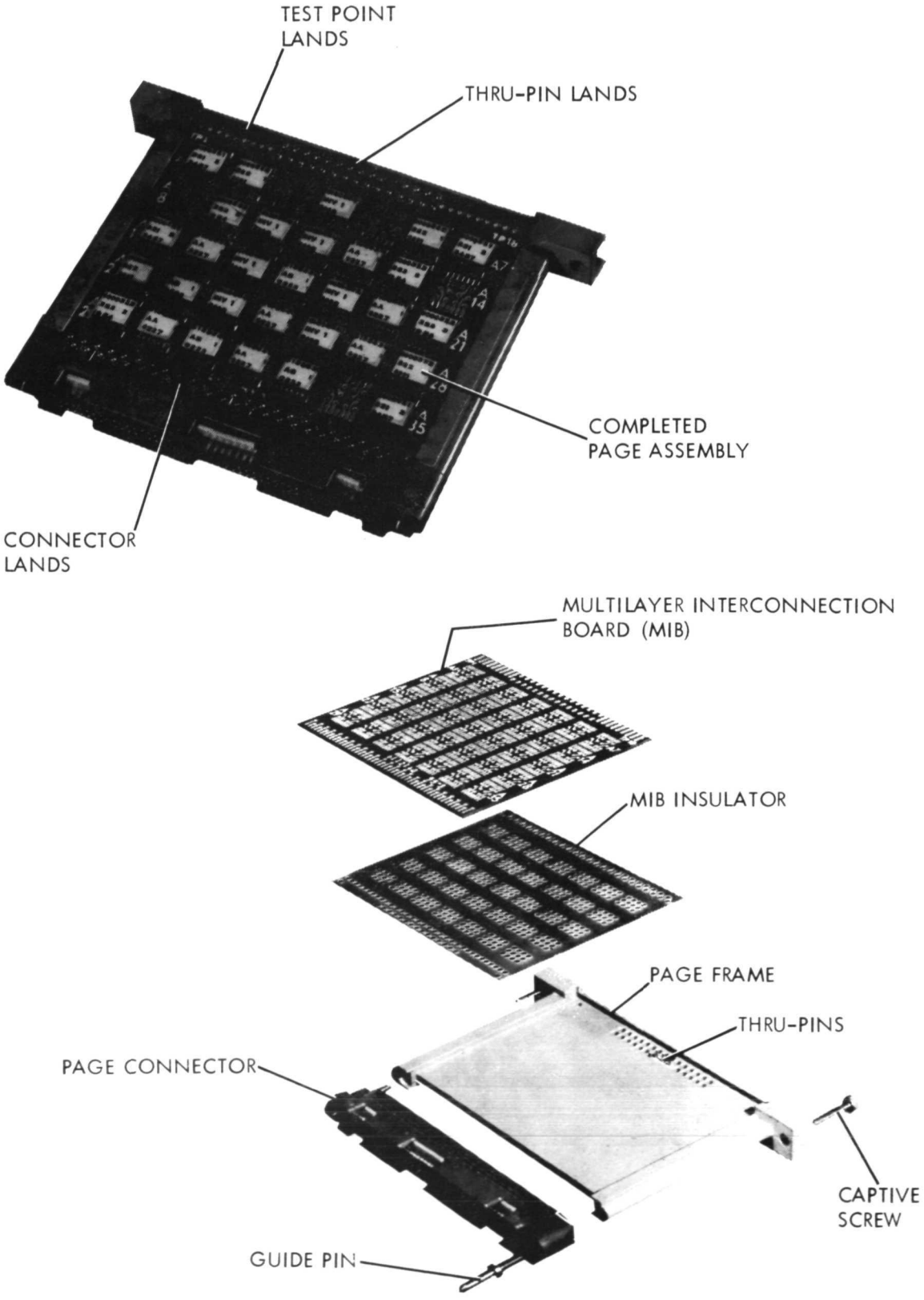


Figure 1-2. Page Assembly

over the pins to connect them to the MIB. In cases where a MIB is installed on each side of the page frame, the thru-pins provide a set of connections from one MIB to the other. Inputs and outputs from the MIBs are supplied through the pluggable page connector.

1-28. Connections between pages are provided by large multilayer printed wiring panels called panel assemblies (figure 1-3) on which are mounted receptacles for the page connectors. The panel assemblies are mounted on the logic frames for rigidity and support. The logic frames also contain grooves which position and support the page assemblies. The combination of panel assemblies, logic frame and page assemblies is called a logic section (previously discussed). Each logic section contains four panel assemblies. The center two assemblies can theoretically accommodate 33 pages each, and the two outside panel assemblies have a theoretical capacity of 27 pages each, making a total capacity of 120 pages for each logic section. In actuality, the page capacity is restricted by circuit modules which extend out over adjacent page connector receptacles, rendering them inaccessible for page use, and also by special terminal blocks (two per panel assembly) which are situated in what would otherwise be page receptacle locations.

1-29. The page assemblies are held in the logic frame by two captive screws. The edges, or shoulders, of each page assembly are different sizes so that the page cannot be inverted and inserted the wrong way, since the grooves in the logic frame allow only one orientation. The page sides are designated "A" and "B". The "A" side is the side toward the viewer with the connector down and the large shoulder to the left.

1-30. A flat metal cover is fitted over the outside of each logic section. The cover is dimpled for rigidity and is held in place by socket head screws around its perimeter. Page assemblies are inserted and removed from the cover side, so it is unnecessary to unfasten the logic sections from the power section to gain access to the page assemblies.

1-31. Connections between panel assemblies are provided by terminal blocks, two in each panel assembly. Each terminal block contains 144 pins. In the breadboard model I, the terminal blocks are wired together from panel assembly to panel assembly. In the breadboard II model, the terminal blocks are interconnected by printed circuit cables (figure 1-4).

1-32. On one end of each of the panel assemblies are three connector receptacles which receive the three plugs of a tape cable from the power section, as previously discussed. The bottom of the logic section is at the same end as the tape cable connectors. From top to bottom, the connectors are designated J1, J2 and J3.

1-33. The logic section which is mounted on the system connector side of the power section is called the front logic section. The remaining logic section is called the back logic section. From left to right, with the top of the logic section facing up, the panel assemblies of the front logic section are designated A5, A6, A7 and A8, respectively. The corresponding panel assemblies on the back logic section are designated A1, A2, A3 and A4, respectively. Page assembly locations are numbered from left to right and top to bottom, A1, A2, A3, etc. A typical page designation would be A3A22, indicating that the page was located in panel assembly A3, position 22. If required, the page assembly MIB side can be added as a suffix, for example, A5A16B, indicating the "B" side of the page in location 16 of panel assembly A5.

1-34. The panel assembly terminal blocks are designated by the letter "E" and for this reason, they are sometimes called E-blocks. In the middle two panel assemblies of each logic section, the E-blocks are located in what would otherwise be page positions

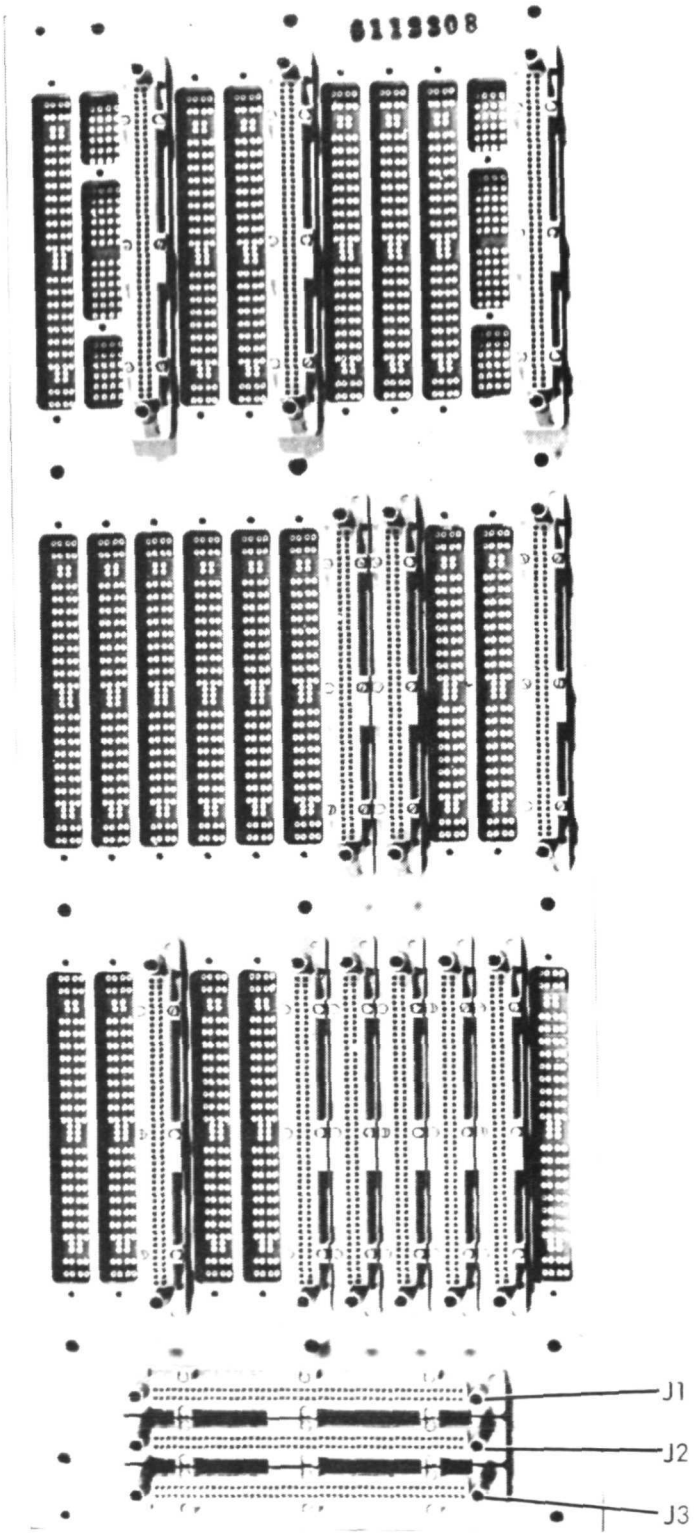
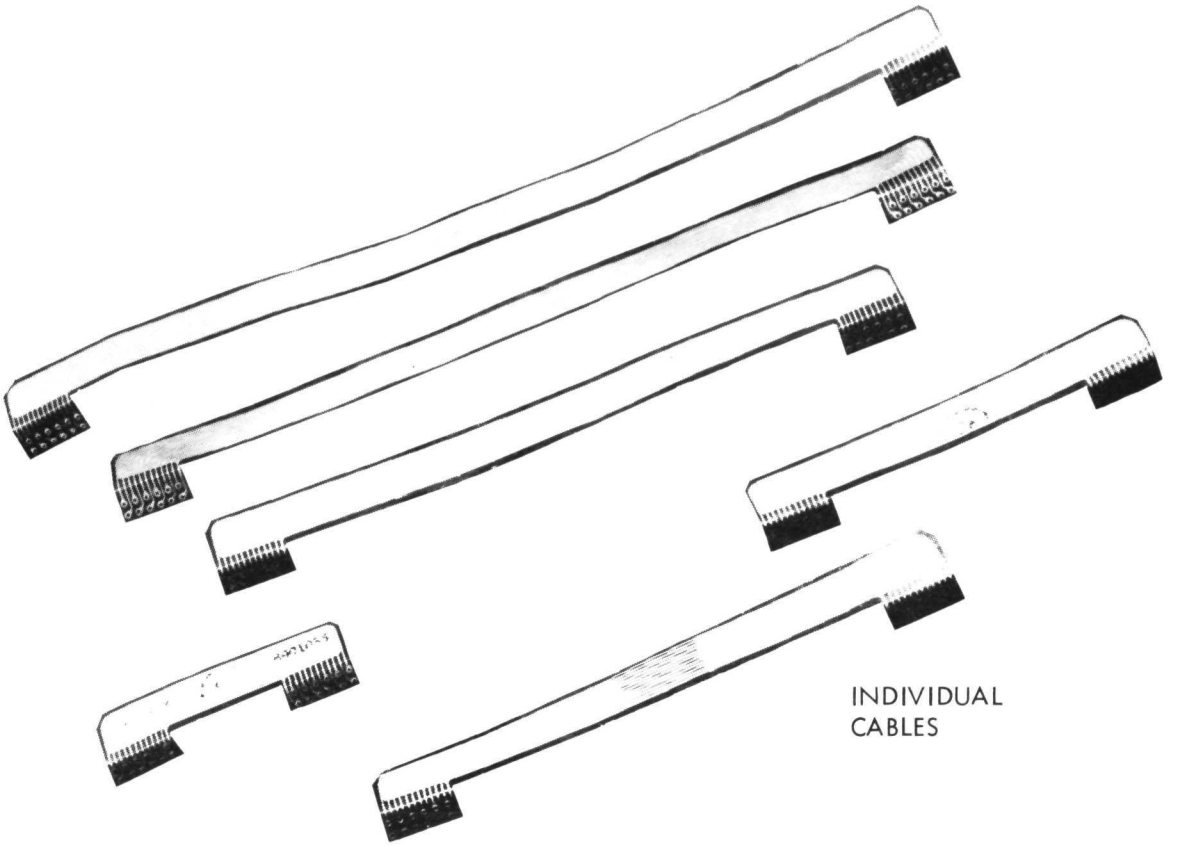


Figure 1-3. Typical Panel Assembly



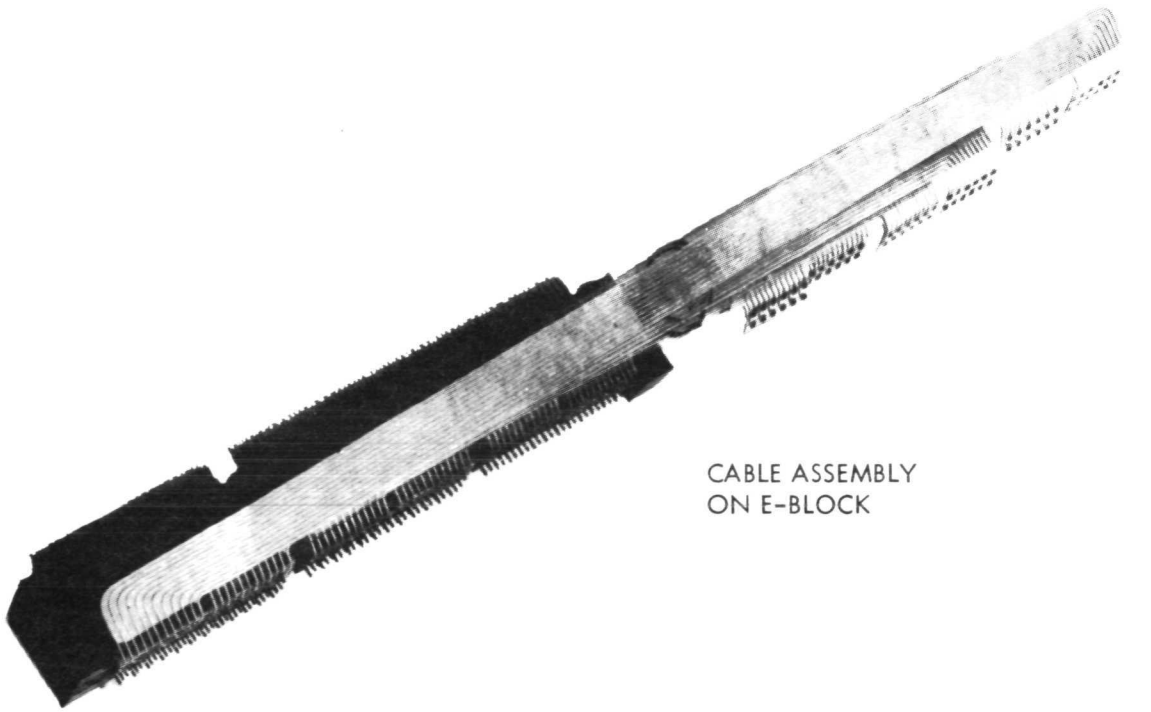


Figure 1-4. Printed Circuit Cables

2 and 10. These blocks are therefore designated E2 and E10. In the remaining two panel assemblies in each logic section, the E-blocks are located in positions 2 and 8, and are designated E2 and E8.

1-35. POWER SECTION. The power section is a boxlike structure with wide flanges at either end. The system connectors, coolant inlet and outlet couplings, and an elapsed time indicator are mounted on the flanges. Reference designations for the system connectors are J1 through J21. The coolant couplings, figure 1-5 (1), are labeled IN and OUT and are designated HP-1 and HP-2 respectively. (No coolant couplings are provided with breadboard model I.) The reference designation for the elapsed time indicator, figure 1-5 (2), is TT-1.

1-36. Across the upper face of the power section is attached a mounting panel (figure 1-6). The mounting panel contains 12 connector receptacles which receive pluggable power supply units called converter-regulators (figure 1-7). (Only eight converter-regulators are provided in the simplex models of the data adapter, although space is provided for 12.) On the back of the mounting panel are 12 power switching relays, two resistors used in computer memory power switching, and two multilayer bus bars. The reference designation for the mounting panel is A10. The connector receptacles for the converter-regulators are numbered left to right and top to bottom, J1, J2, J3, etc. The converter-regulator assemblies have the same designation as the receptacle into which they are plugged. Thus, a typical converter-regulator designation would be A10J11.

LEGEND

1-Adapter (Coolant Coupling)
2-Elapsed Time Indicator

Figure 1-5. Power-Section-Flange Assemblies.

1-37. Across the lower face of the power section is mounted a multilayer interconnection panel called the distribution panel (figure 1-8). The distribution panel contains 14 terminal assemblies called wire guides into which wires are inserted and soldered. The reference designation for the wire guides is "E". Guides E1 through E8 provide connections from the components and connectors on the mounting panel and from the distribution panel to eight tape cable assemblies which, as previously mentioned, interconnect the power section with the logic sections. Guides E9 and E10 provide connections from one side of the distribution panel to the other, as do guides E11 and E12. Guides E13 and E14 provide connections to the system connectors. A capacitor assembly used in conjunction with a digital-to-analog converter circuit is mounted on the distribution panel.

1-38. In most cases, the distribution panel serves as a central point for interconnections between assemblies in the data adapter. In the case of panel assemblies A5 and A6, however, many signals are wired directly from the system connectors to page connector receptacles. This is necessary because the signals so wired would be adversely affected if they were routed through the tape cables.

1-39. Two additional assemblies are mounted on the power section: the resolver frequency source, figure 1-9 (1), and the radio-frequency-interference filter, figure 1-9 (2). Both items are attached to a strut which runs across the frame just below the bottom converter-regulator assemblies. The resolver frequency source, designated FS-1, is wired directly to one of the system connectors. The radio-frequency interference filter output terminals are wired to one of the bus bars on the mounting panel.

(To Be Supplied)

LEGEND

1- Mounting Plate
2- Bus Bar No. 1
3- Bus Bar No. 2
4- Relays
5- Terminal Board
6- Resistors

Figure 1-6. Mounting Panel

Inputs to the radio-frequency-interference filter are provided by system connector J11 which is physically part of the radio-frequency-interference filter assembly.

1-40. The reference designator prefix for all data adapter assemblies is 2. Figure 1-10 lists all data adapter assemblies with part numbers and figure reference numbers. Figure 1-11 lists system connectors and part numbers.

1-41. SUBASSEMBLIES. Subassemblies in the data adapter consist of the page assemblies and converter-regulator assemblies, previously described. A list of data adapter subassemblies is included in section IX, since these subassemblies are the only laboratory replaceable items.

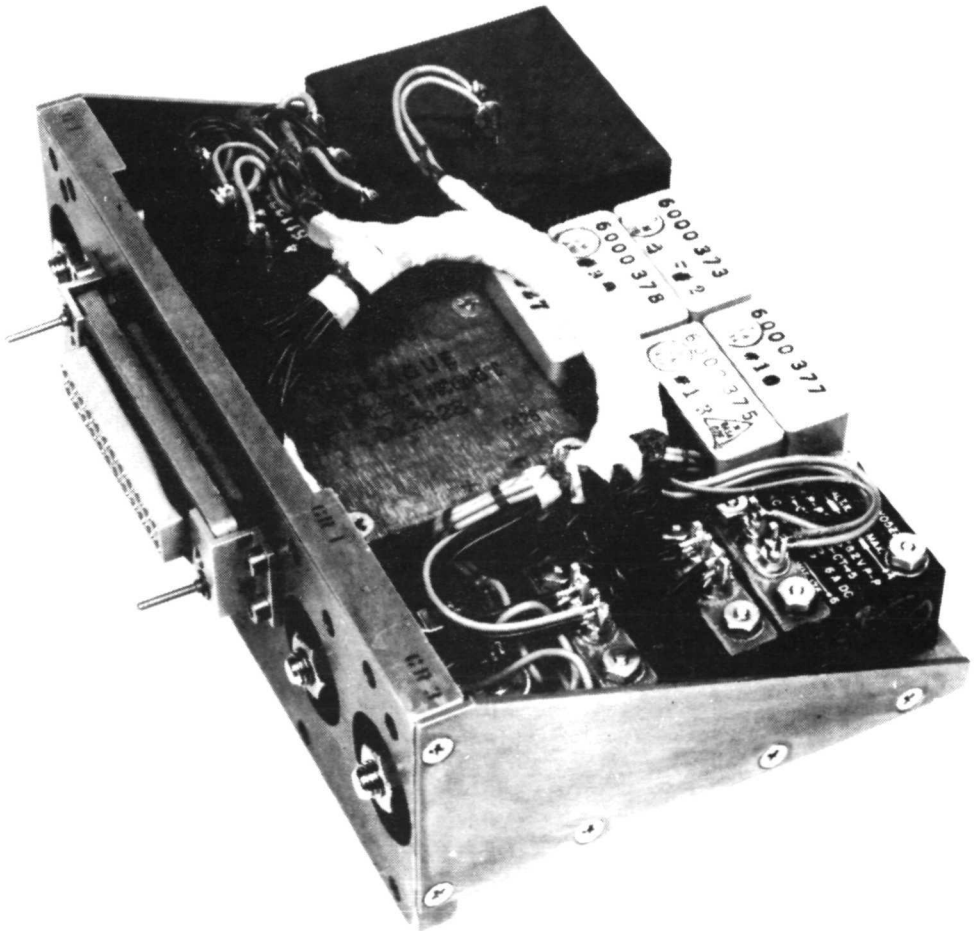


Figure 1-7. Typical Converter-Regulator Assembly

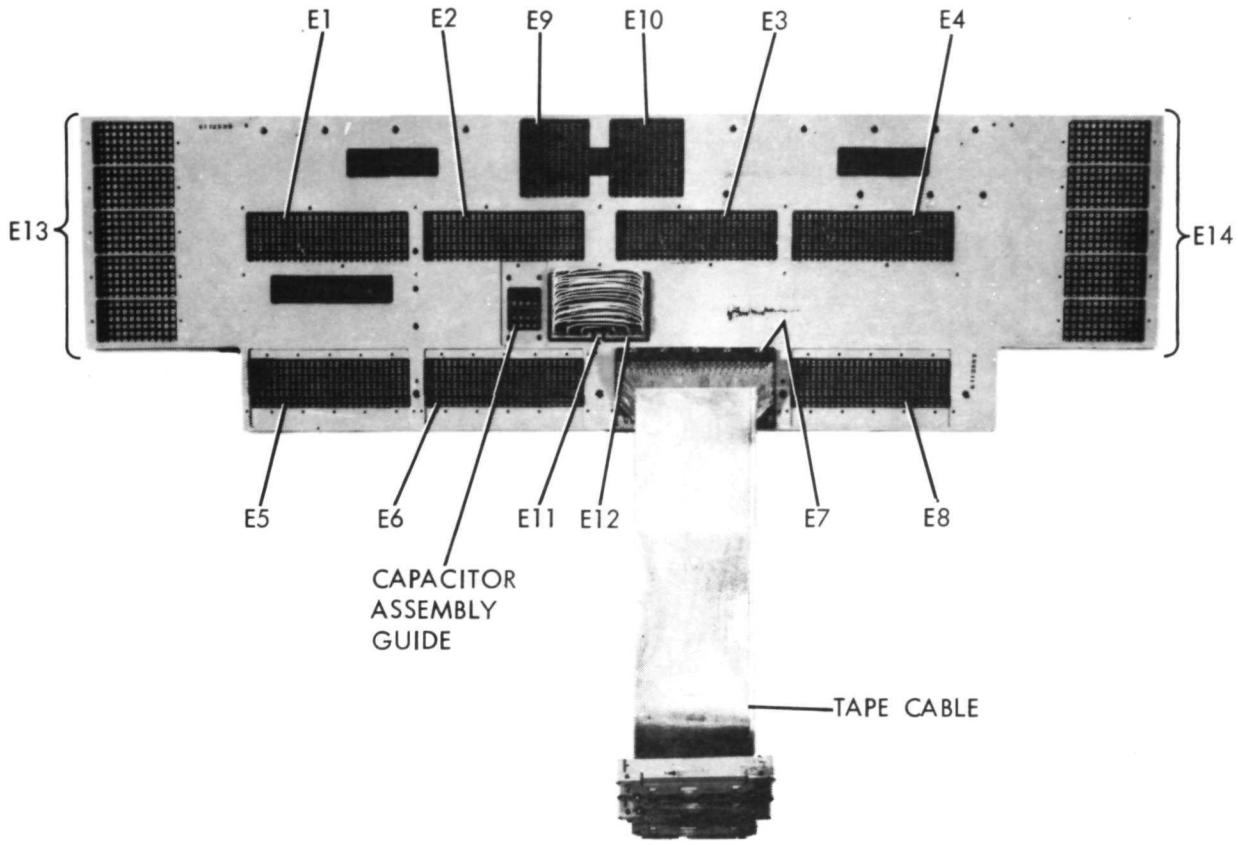
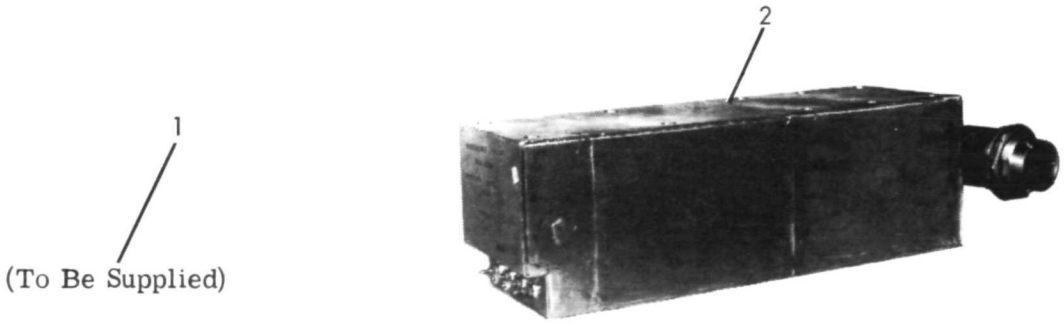


Figure 1-8. Typical Distribution Panel (Shown Partially Assembled)



LEGEND

1- Resolver Frequency Source
2- Radio-Frequency-Interference Filter

Figure 1-9. Power Section Strut-Mounted Assemblies

Reference Designator	Name	Part Number	Figure Reference
2A1	Panel Assembly	6113710	
2A2	Panel Assembly	6113730	
2A3	Panel Assembly	6113740	
2A4	Panel Assembly	6113750	1-3
2A5	Panel Assembly	6113760	
2A6	Panel Assembly	6113770	
2A7	Panel Assembly	6113810	
2A8	Panel Assembly	6113830	
2A9	Distribution Panel	6112726* 6112597**	1-8
2A10	Mounting Panel consisting of:		
	Mounting Plate	6113624	1-6(1)
	Bus Bar No. 1	6112528	1-6(2)
	Bus Bar No. 2	6112798	1-6(3)
	Relays (12)	6080609	1-6(4)
	Terminal Board	6112808	1-6(5)
	Resistors (2)	6071163	1-6(6)
2HP-1	Adapter (Coolant Coupling)	6080654	1-5(1)
2HP-2	Same as 2HP-1		
2FL-1	Radio-Frequency-Interference Filter	6080695	1-9(2)
2FS-1	Resolver Frequency Source	6112627	1-9(1)
2TT-1	Elapsed Time Indicator	6076600	1-5(2)

*breadboard model I only

**breadboard model II only

Figure 1-10. Data Adapter Assemblies

Reference Designator	Part Number	Diameter	Pin Capacity
2J1	6080235	1-3/8"	55
2J2	6080237	1-3/8"	55
2J3	6080243	1-3/8"	55
2J4	6080242	1-3/8"	55
2J5	6080238	1-3/8"	55
2J6	6081187	1-1/4"	41
2J7	6080614	1-1/4"	41
2J8	6080239	1-3/8"	55
2J9	6080240	1-3/8"	55
2J10	6080241	1-3/8"	55
2J11*	6080612	1-3/8"	21
2J12	6080243	1-3/8"	55
2J13	6080238	1-3/8"	55
2J14	6080240	1-3/8"	55
2J15	6080237	1-3/8"	55
2J16	6080235	1-3/8"	55
2J17	6080613	1-1/4"	41
2J18	6081187	1-1/4"	41
2J19	6080614	1-1/4"	41
2J20	6080241	1-3/8"	55
2J21	6080236	1-3/8"	55

*Part of Assembly 2FL-1

Figure 1-11. Data Adapter System Connectors

SECTION II

THEORY OF OPERATION

2-1. SCOPE AND PURPOSE.

2-2. This section contains descriptions of the electrical and logical functions of the data adapter. The detail of description is sufficient to analyze operations as they may be perceived at test point levels. Included in this section are logic and block diagrams typical of every circuit in the data adapter. If required, detailed diagrams (provided in Section X) may be located by referring to the index. Also, the Section X diagrams are provided in the same order as the order in which they are discussed in this section. Items or circuits which cannot be located in Section X will be located in the signal routing lists.

2-3. SYMBOLS.

2-4. LOGIC SYMBOLS.

2-5. Logic symbols used in the section are described in the Logic Symbols appendix.

2-6. ELECTRICAL SYMBOLS.

2-7. Electrical symbols used in this section conform to military standard MIL-STD-15-1. Special symbols are described in the Part Symbols appendix.

2-8. GENERAL CONCEPTS.

2-9. LATCHES AND TRATCHES.

2-10. Latches and tratches are both defined in the Logic Symbols appendix. However, because of their extensive use in the data adapter, and the various ways in which they are modified and depicted, a more detailed description of their construction and function is included here.

2-11. LATCHES. The basic latch form is shown in figure 2-1. It consists of two cross-coupled AND-INVERTERS. In the quiescent condition, latch inputs A and B are "0's" and inputs E and F are "1's". If C is a "1", D will be a "0" and vice versa.

2-12. Inputs A and B are called one-drive inputs, and inputs E and F are called zero-drive inputs. A "1" on input A will ultimately produce a "1" on output C. A "1" on B will ultimately produce a "1" on output D. The inputs need only be momentary; once the latch feedback path has been completed, the latch will maintain the configuration established by its inputs.

2-13. A "0" at input E will produce a "1" on output C; conversely, a "0" at input F will produce a "1" on output D.

2-14. As previously stated, the latch outputs are always complementary. However, this condition is negated if either set of inputs is double-driven. For instance, if both

inputs A and B are "1's" at the same time, outputs C and D will both be "0's". If inputs E and F are both "0's" at the same time, outputs C and D will be "1's". Both double-drive conditions are unstable. As soon as the double-drive is removed, the latch outputs become complementary.

2-15. In general, both outputs of a latch have the same name, except that one output name is suffixed with an "N" (Not). This output is frequently called the "not-side" of a latch. When the not-side of a latch is a "1", the latch is said to be reset. When the not-side is a "0", the latch is set. In cases where the latch outputs are not labeled in this fashion, the set and reset conditions will be specified.

2-16. The basic latch configuration may be modified for certain purposes, such as extending the number of gates that can be used to control the latch. Figures 2-2 and 2-3 show an "OR-extended" and an "AND-extended" latch. In the OR-extended latch, any one of the one-drive set inputs, S1, S2 or S3 is capable of setting the latch. In the AND-extended latch, all three of the set inputs, S1, S2 and S3 must become "1's" simultaneously to set the latch. It should be noted that the three not-sides of the AND-extended latch may be "0's" independently of one another, according to the configuration of "1's" on the three set input lines. The "OR-extended" latch is shown for demonstration purposes only. On the "AND-extended" latch is used in the data adapter.

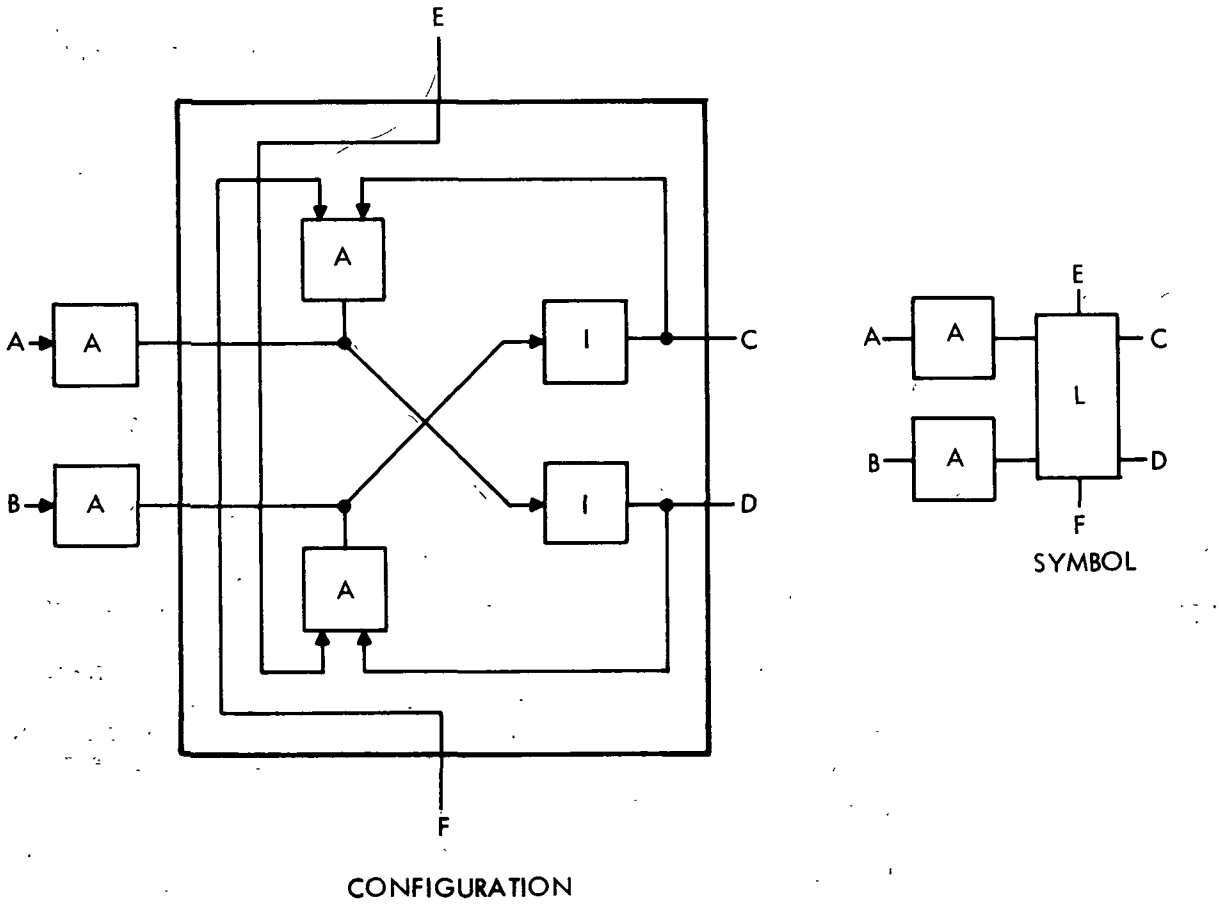


Figure 2-1. Basic Latch

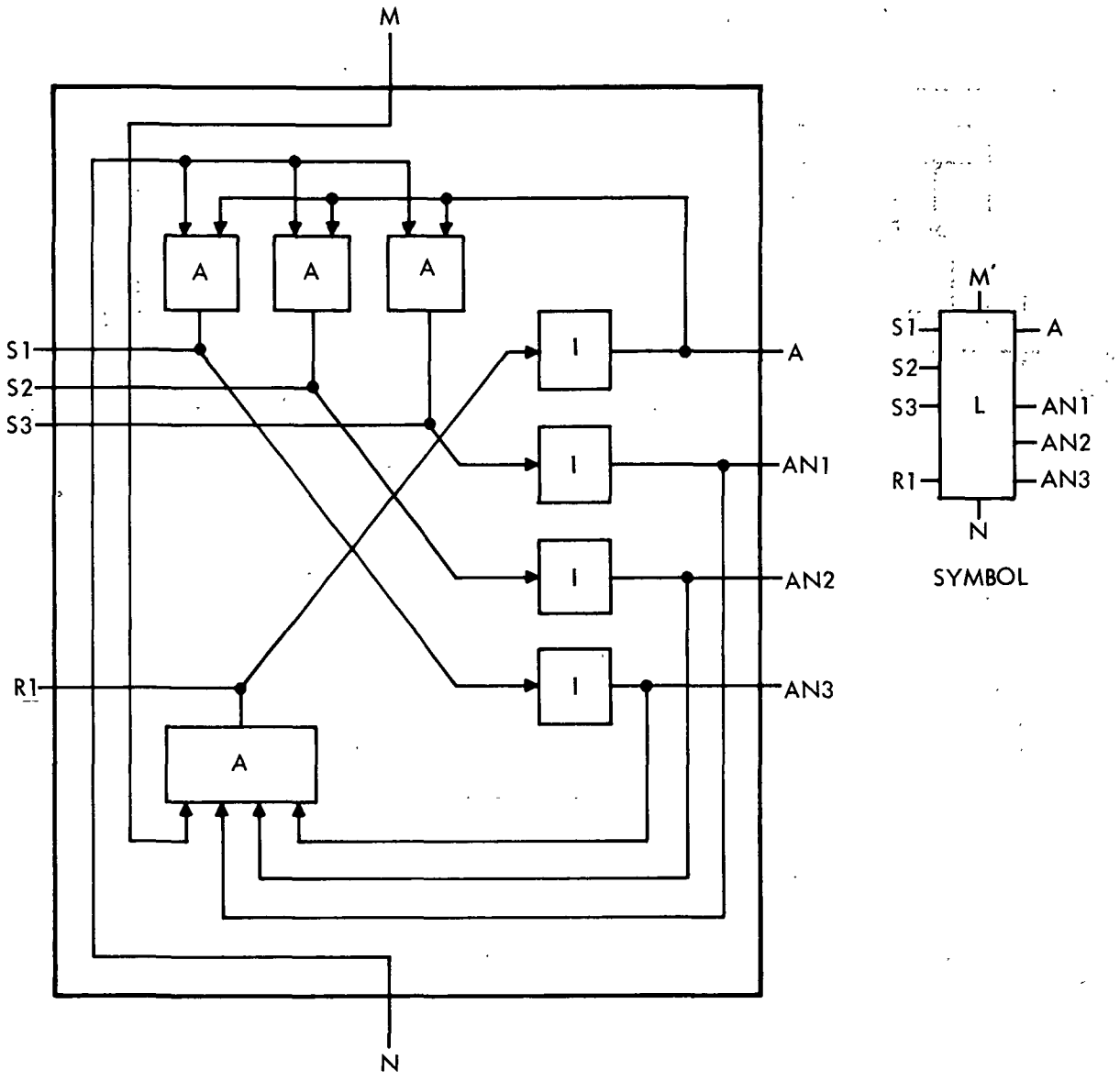


Figure 2-2. OR-Extended Latch

2-17. TRATCHES. Tratches are tristable storage devices which utilize the double-drive feature of an ordinary latch. Figure 2-4 shows a typical tratch. If input C goes to a "1", output F will become a "0". This "0" is applied to both zero-drive inputs simultaneously, driving outputs D and E to "1's". Outputs D and E are both fed to gate A4 which opens and maintains the "1" originally supplied through gate A3. The tratch remains in this condition until either input A or input B goes to a "1". When this occurs, the latch is set or reset accordingly, and since its outputs now become complementary, gate A4 opens to remove the double-drive.

2-18. The type of tratch shown in figure 2-4 is called an exclusive-zero tratch, because only one of its outputs can be a "0" at any given time.

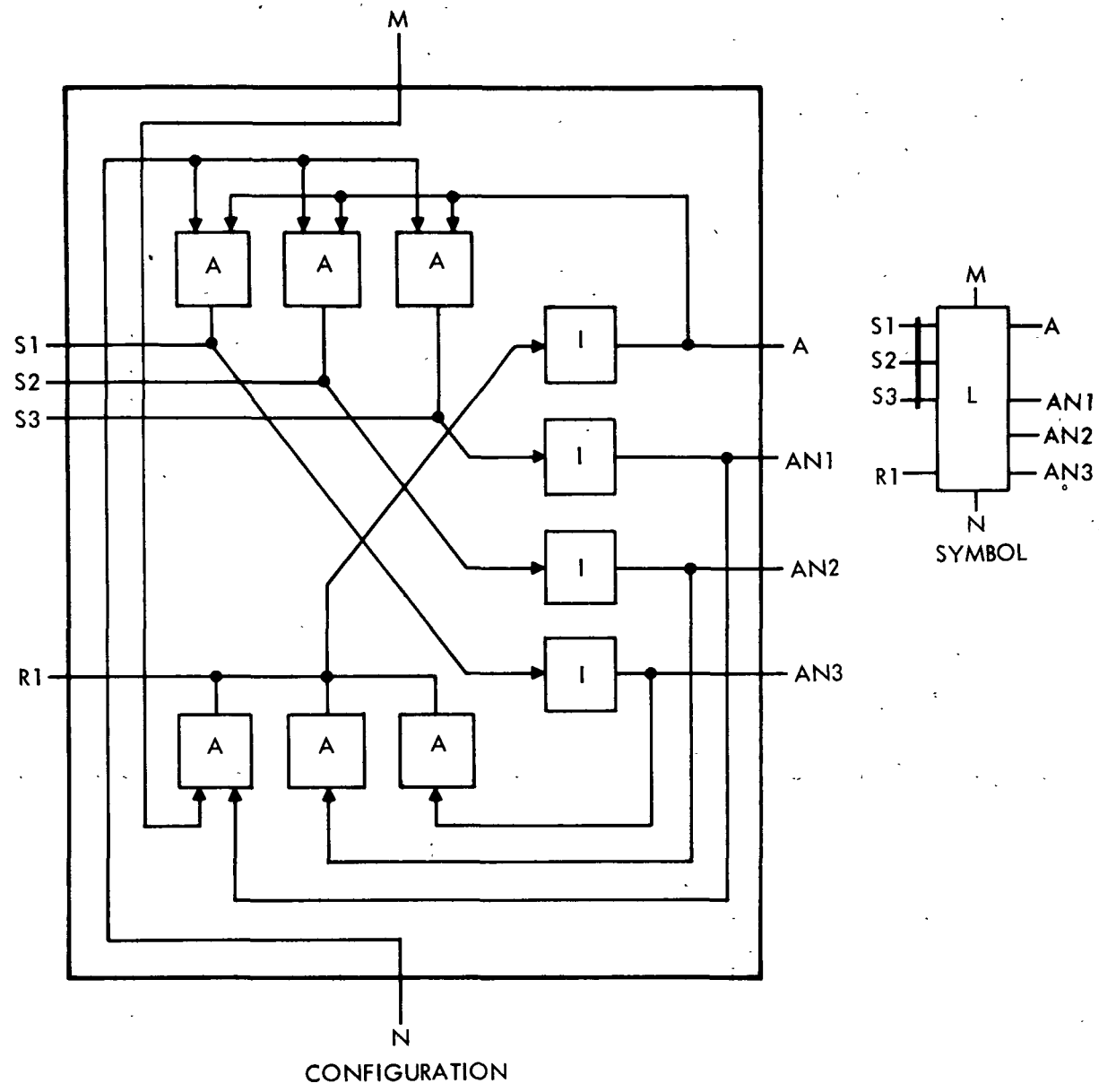


Figure 2-3. AND-Extended Latch

2-19. TRIPLE MODULAR REDUNDANCY.

2-20. A failure of almost any circuit in a flight-model data adapter, even a momentary failure, could conceivably cause intolerable malfunctions of the guidance system. To prevent such errors, flight-model data adapter circuits are redundant in the form of three identical sets, or channels, of logic. (Some circuits are duplexed rather than triplexed. This is feasible only if a failed circuit will be overridden by a good circuit as is done with power supplies, or if a reasonableness check can be made of a circuit output and provisions made to switch to the duplex circuit if the reasonableness check fails.)

2-21. In the triple modular redundancy, TMR, operation, signals from the three channels are fed to "voter" circuits which duplicate the majority input. Any differing circuit is thereby "outvoted" by two unanimous signals (figure 2-5). Since the voter outputs mask errors by providing correct outputs, the voter inputs are also fed to a circuit called a disagreement detector which senses non-unanimous input conditions. This monitoring feature is necessary for trouble-shooting and evaluation.

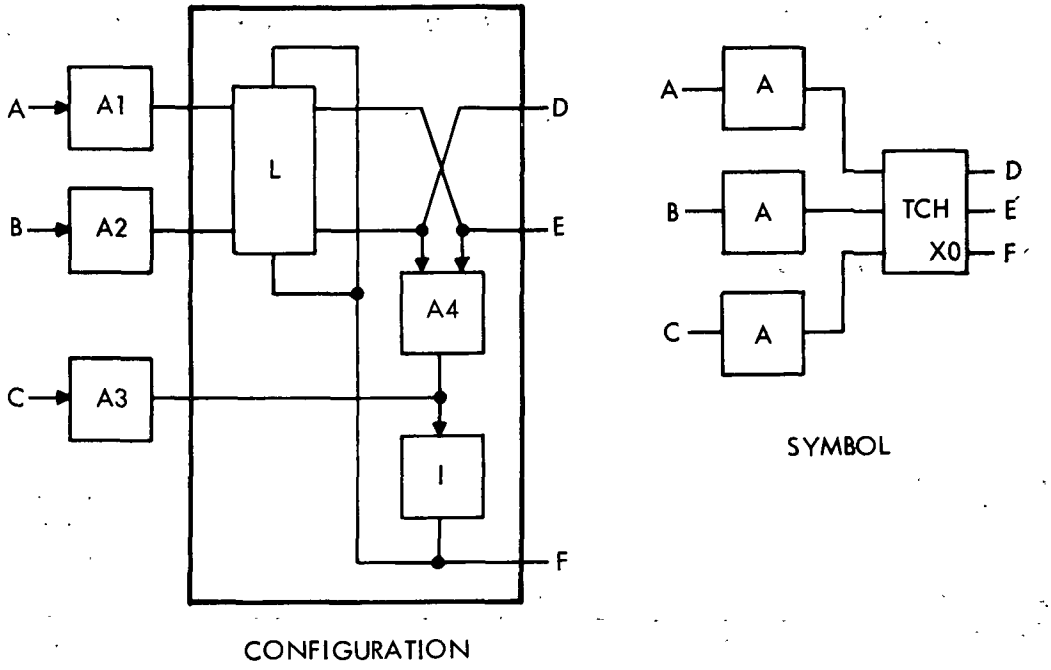


Figure 2-4. Exclusive-Zero Tratch

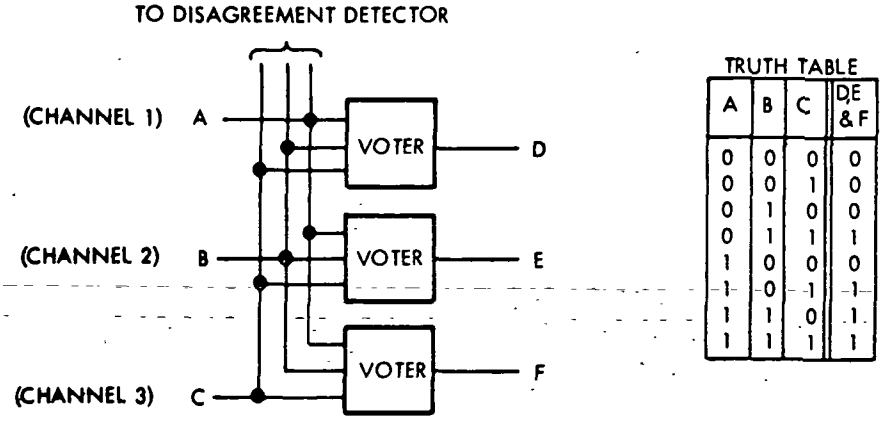


Figure 2-5. Voter Circuits, Block Diagram

2-22. In the simplex data adapter models, only a few circuits are triplexed for evaluation purposes. However, a complete set of voter circuits is provided. Therefore, a number of "dummy" circuits have been added to the simplex models to simulate the voter inputs which are not provided by triplicated circuits. In order to get a voter to work properly from one active input, it is necessary to create a "tie vote" on the remaining two inputs, i. e., a "1" and a "0". The active input then breaks the tie, and the output of the voter follows the active input.

2-23. In order to create the "tie vote", one input to the voter is left disconnected. This is equivalent to a "1" input. The "0" input is provided by connecting an AND-Inverter combination to the voter input. The AND input is left disconnected, which is equivalent to driving the AND with a "1". The inverter output is consequently a "0".

2-24. In a number of other cases, the voters are run duplex with one input left disconnected. In these situations, the duplex inputs provide a majority vote whenever they are "0's" and a unanimous input whenever they are "1's" (since the unconnected input looks like a "1"). This system has the advantage of cycling the voters from a unanimous to a non-unanimous condition for demonstration and evaluation purposes.

2-25. POWER.

2-26. The data adapter develops the voltages required for both itself and the computer from an externally provided 28 volt dc source. The voltages are +20, +12, +6, +6 COMP, -3 and -20 volts. Figure 2-6 shows a typical power supply. The input 28 volts dc is fed through a radio-frequency interference filter to eight converter-regulator assemblies which provide the six voltages and a spare +20 and +6 for duplexing purposes.

2-27. Included in the converter-regulator assemblies are special circuits which adapt the voltage outputs for telemetry circuits and for telemetry ground reference.

2-28. The outputs of some of the converter-regulators are fed to computer and data adapter circuits through power-switching relays which, in turn, are controlled by external signals. The outputs of the remaining converter-regulators are fed directly to computer or data adapter circuits.

2-29. CONVERTER-REGULATOR. The converter-regulators employ dc chopping with transformer step-up or step-down and rectification to generate unregulated dc voltages which are regulated by a process called pulse-width modulation. In pulse-width modulation, a triangular shaped signal is fed to a square wave generator which turns on and off as the triangular shaped signal rises and falls past a given reference level. If the reference level is raised (closer to the apex of the triangle), the on and off points will come closer together and the output pulses from the square wave generator will become narrower. If the reference level is lowered (away from the apex of the triangle), the on and off points will become further apart and the square wave generator output pulses will become wider.

2-30. In the converter-regulators, the triangular waveform is supplied by the same chopper and transformer that supplies the unregulated voltage for use by the converter-regulator circuits. The reference level is represented by the difference between the regulated output voltage and some standard voltage (established by zener diodes). The pulses from the square wave generator are fed to a transformer-rectifier-filter which produces the output voltage. If the output voltage rises, the reference level of the triangular waveform will be driven upward, shortening the pulse width of the square wave generator output and thereby reducing the output voltage. Conversely, a falling output

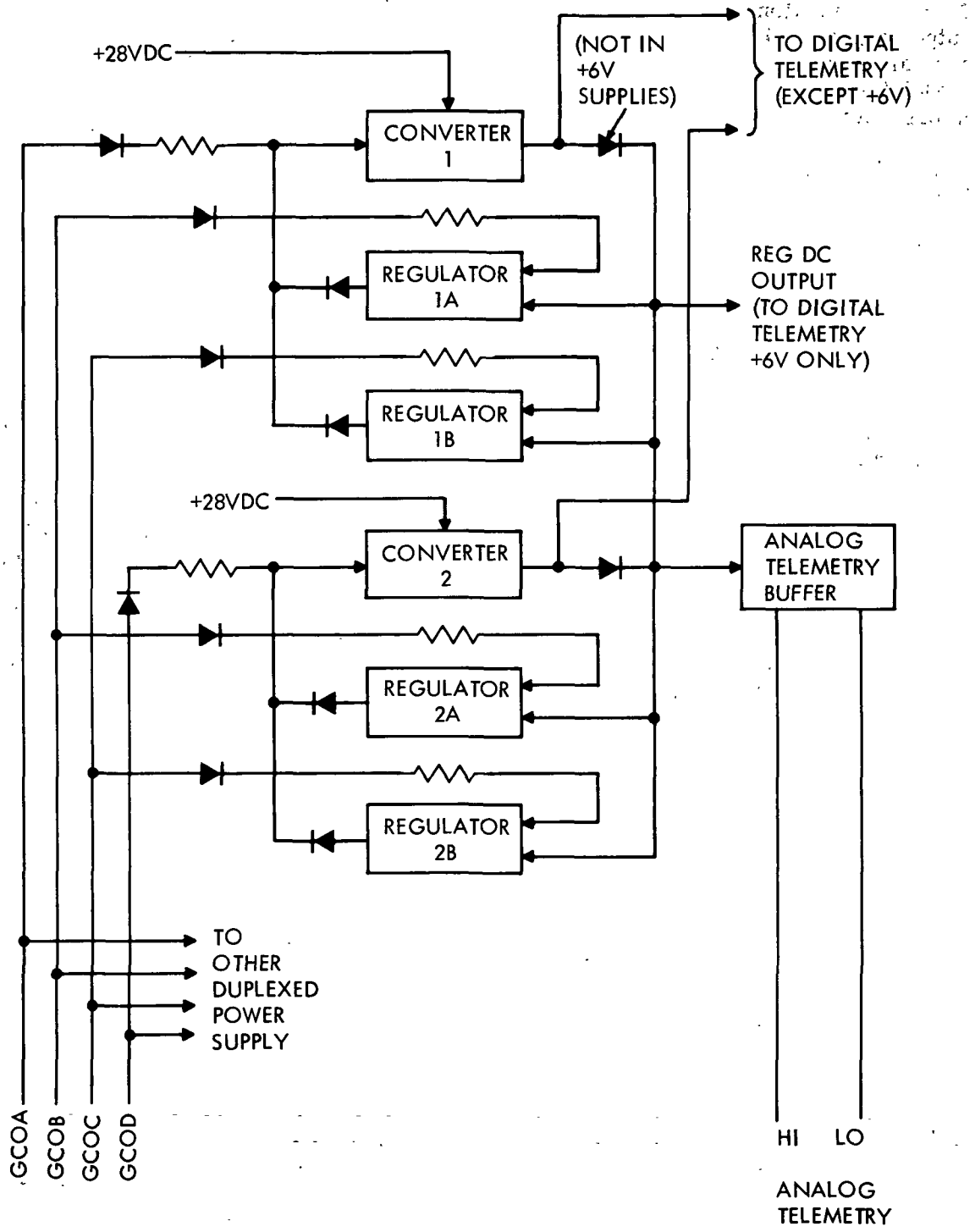


Figure 2-6. Power Supply Switching, Simplified Diagram

voltage will lower the reference level of the triangular waveform, increasing the square wave generator pulse width and thereby raising the output voltage back to normal.

2-31. The portion of the pulse-width modulator which senses the difference between the output voltage and some reference, and which provides the reference level for the triangular waveform is called the regulator. The remaining circuits of the pulse-width modulator are called the converter. Each converter-regulator assembly has two regulators which are provided for duplexing purposes.

2-32. ANALOG TELEMETRY BUFFER. Included in the converter-regulator assemblies are analog telemetry buffer circuits which provide a dc signal proportional to the output level of the converter-regulator. The signal from the analog telemetry buffer is isolated from the data adapter ground return. This prevents inaccurate telemetry readings caused by differences in the gound return potential between the data adapter and the telemetry equipment.

2-33. DIGITAL TELEMETRY CIRCUITS. Also included in the converter-regulator assemblies are digital telemetry circuits which sense whether the converter-regulator output is on or off. For positive supplies, the digital telemetry output is a "1" when the supply is on and a "0" when the supply is off. For negative supplies, the digital telemetry output is a "0" when the supply is on and a "1" when the supply is off.

1/12/66 Note. There is a separate switch for memory.

2-34. POWER CONTROL. Power turn-on and turn-off is controlled simply by turning the external 28 volt dc source on and off. However, in the case of duplexed supplies, arrangements are made to disable each of the supplies to determine if the remaining supply is operable. Simultaneously, one of the two regulators in each converter-regulator assembly may be disabled to check the operability of the remaining regulator. The disabling operation is provided by four signals, GCOA, GCOB, GCOC and GCOD. These signals are generated outside the data adapter. A ground on any one of these signals will disable the circuit to which it is fed. A duplexed supply may be represented as in figure 2-6, where the converters are numbered 1 and 2, and the regulators are numbered 1A, 1B, 2A and 2B. The signals required for various operating conditions are shown as follows:

Operating: Converter	Regulator	Signals Required
1	1A	GCOD, GCOC
1	1B	GCOD, GCOB
2	2A	GCOA, GCOC
2	2B	GCOA, GCOB

2-35. POWER SWITCHING RELAYS. Relays are used to control power to the computer memory drivers, to the discrete output drivers, and to various logic and voters for channel switching.

2-36. Computer Memory Driver Switching. Computer memory driver switching is provided by the memory driver relays, figure 2-7. Under control of externally provided signals MEMC, MEMS and MEMR, these relays disable the memory drivers during channel switching or during power-on and power-off sequences to prevent reading in extraneous data or destruction of data by partially energized circuits. The memory driver relays are bipolar. Prior to power-on, they are all reset as shown in figure 2-7. Resistors Rs1 and Rs2 are connected to dc return via circuitous routing through the relay contacts. When +20 volt dc power comes up, it will be loaded by resistors

Rs1 and Rs2. This loading maintains a trickle current through the power supply filter. At least 50 milliseconds after power comes on, MEMC will set relays K1 and K3, applying +20 volts dc to the memory drivers through resistors Rd1 and Rd2. The minimum 50 millisecond delay allows the logic and power circuits to stabilize. Resistors Rd1 and Rd2 limit the initial driver current which would otherwise be excessive because of a large decoupling capacitance associated with the memory drivers. At least 15 milliseconds after MEMC is enabled, signal MEMS will set relays K2 and K4, shorting resistors Rd1 and Rd2 and completing the memory power-on sequence.

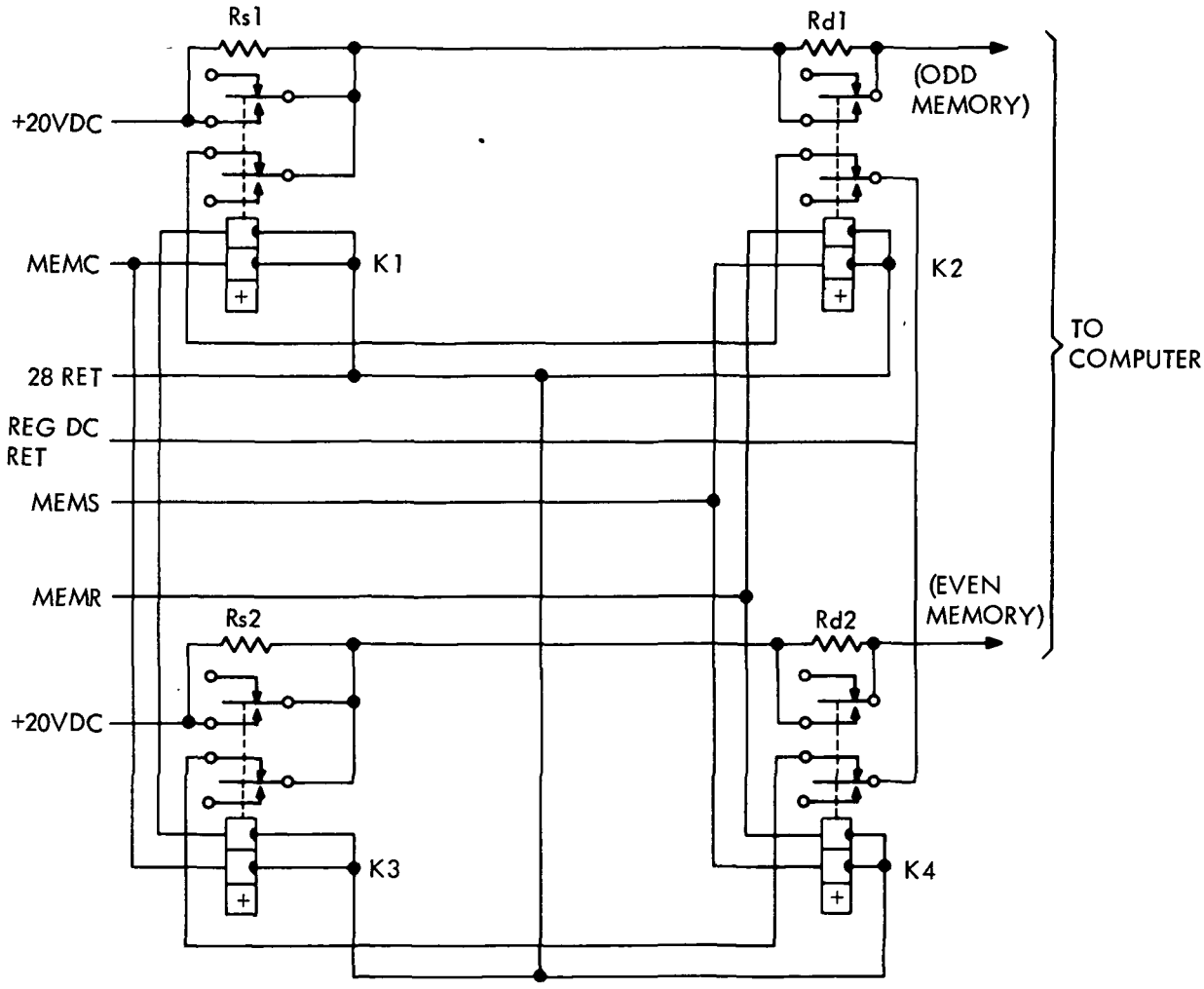


Figure 2-7. Memory Drive Relays, Schematic Diagram

2-37. In the memory power-off sequence, MEMR will reset all relays, grounding the junction between resistors Rs1 and Rd1 and between Rs2 and Rd2. The ground on resistors Rd1 and Rd2 allows the memory driver decoupling capacitors to discharge without excessive surge current. The ground on resistors Rs1 and Rs2 maintains a +20 volt dc trickle current. Power is not removed until at least 8 milliseconds after the MEMR signal, in order to allow the capacitors to discharge first.

2-38. Channel Switching. Channel switching is provided by the channel switching relays, figure 2-8. Under control of signals GCOE, GCOF, GCOG and GCOR, these relays can disable any two of the three TMR channels in order to check the operation of the remaining one. Basically, disablement consists of forcing a tie vote (a "1" and a "0") at two inputs of each voter. The remaining input then breaks the tie and is free to run the voter. The "0" input to the voter is provided directly from the relays. As shown in figure 2-9, the voter inputs consist of three gates which are usually returned to +12 volts dc. To produce a "0", the gate return is grounded through the relays. In order to produce the "1" input, it is necessary to disable the gate of a gate-inverter combination feeding the voter. When the gate is disabled, its output will be a "0", driving the inverter output to a "1". The logic gates are normally returned to +6 volts dc. To disable these gates, the channel switching relays ground the gate return.

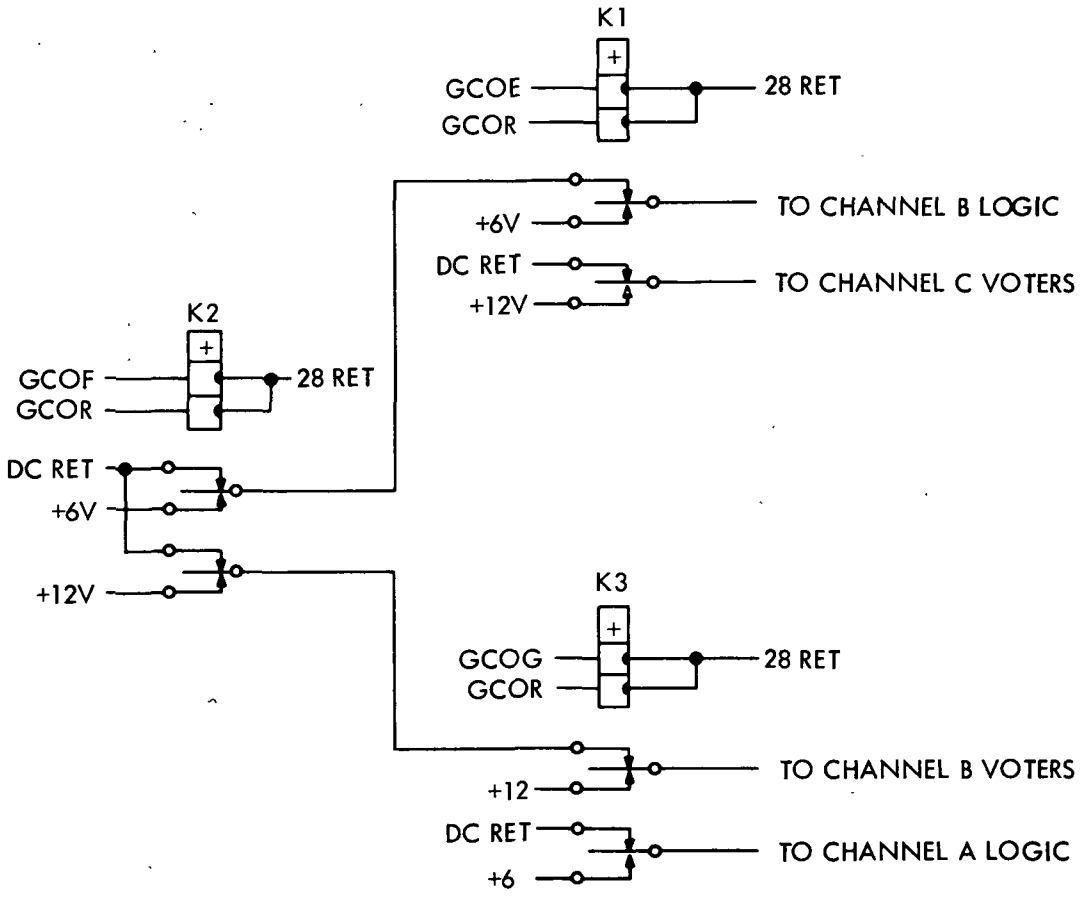


Figure 2-8. Channel Switching Relays

2-39. As shown in figure 2-9, channel C is disabled only by forcing a "0" at the voter. Channel A is disabled only by forcing a "0" at the logic. Channel B may be disabled either way. Briefly, this operation may be summarized as follows:

To Select Active Channel	Disable Logic On Channel	Disable Voter On Channel
A	B	C
B	A	C
C	A	B

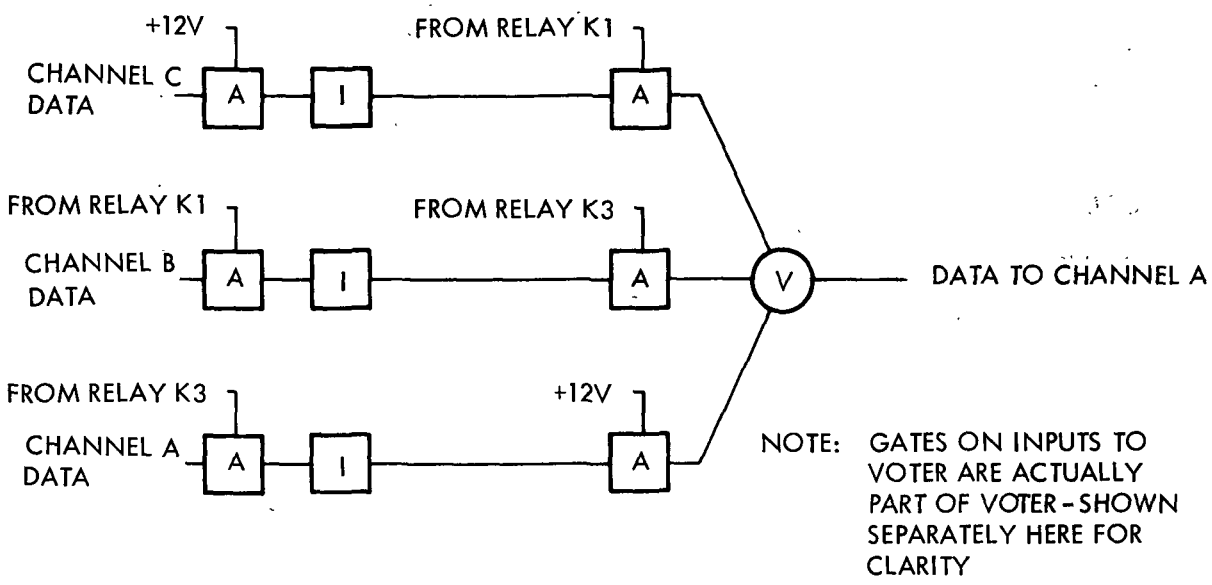


Figure 2-9. Channel Switching Inputs

2-40. As shown in figure 2-8, relay K1 (when set) disables the channel C voters. Relay K3 (when set) disables the channel A logic. Depending on whether relay K1 or relay K3 is set, relay K2 (when set) will disable either the channel B logic or the channel B voters. If none of the relays are set, all channels will operate in TMR. The appropriate relay drive signals for various active channels are shown as follows:

Channel Selected	Relay Drive Signals
A	GCOE and GCOF
B	GCOE and GCOG
C	GCOF and GCOG
A11	GCOR

2-41. Discrete Output Driver Switching. Switching of the discrete output drivers in the data adapter is accomplished by the discrete output driver relays, figure 2-10. Under control of externally provided signals, GCOA, GCOB and GCOC (three of the same signals used for converter-regulator control), these relays can disable any one or any two of the driver inputs (in actuality, disabling one or more of the intermediate output drivers which are considered to be part of the discrete output drivers). The discrete output drivers behave like voters. If one input is grounded, the remaining two will provide a majority input and the driver output will consist of data. If two inputs are

grounded, the driver output will be a "0". The appropriate relay drive signals for various driver outputs are as follows:

Relay Drive Signals	Channel A Input	Channel B Input	Channel C Input	Driver Output
GCOA	"0"	Data	Data	Data
GCOB	Data	"0"	Data	Data
GCOC	Data	Data	"0"	Data
GCOA, GCOB	"0"	"0"	Data	"0"
GCOA, GCOC	"0"	Data	"0"	"0"
GCOB, GCOC	Data	"0"	"0"	"0"

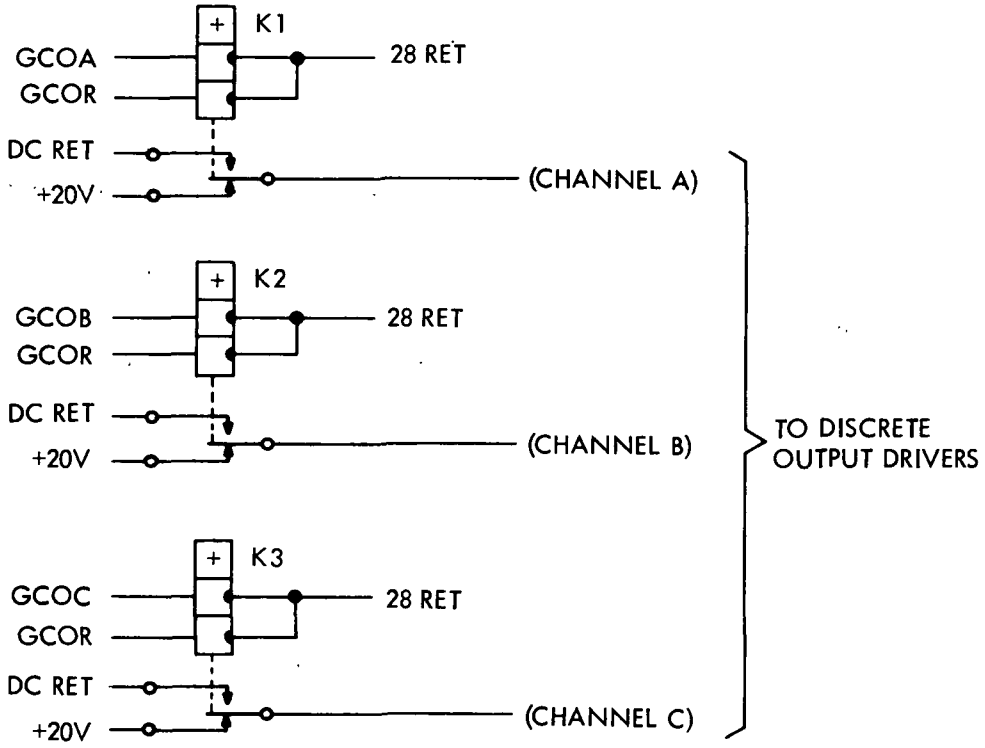


Figure 2-10. Discrete Output Driver Relays

2-42. TIMING.

2-43. GENERAL. Data adapter timing is based upon a unit of time known as the operation cycle, which is approximately 82 microseconds long. The operation cycle is divided into three equal intervals called phases; each phase is subdivided into 14 bit gates

and each bit gate is further divided into four clocks. The nominal values for duration and period of the various timing intervals are as follows:

Interval	Name	Duration (usec)	Period (usec)
Clocks	W, X, Y & Z	0.48828125	1.9531250
Bit Gates	1 thru 14	1.9531250	27.343750
Phases	A, B & C	27.343750	82.03125
Operation Cycle		82.03125	

2-44. Each operation cycle is followed by another as long as the data adapter continues to operate. The preceding values are for the nominal intervals of time indicated and not necessarily for the actual signals used to define these intervals.

2-45. The signals used to define timing intervals are developed from computer clocks which are fed to circuits in the data adapter. Since the timing signals generated in the data adapter are identical to the timing signals generated in the computer, synchronizing signals are provided by the computer.

2-46. Clocks provided by the computer are amplified and distributed in the data adapter by clock driver circuits. The signals used to identify bit gates are developed by the Timing Gate Generator, and the signals used to identify phases are developed by the Phase Generator. A number of additional signals, embodying various combinations of phase, bit gate and clock signals are generated by special timing circuits.

2-47. CLOCK DRIVER CIRCUITS. Each clock coming from the computer is fed to eight clock driver circuits (figure 2-11). These circuits provide level restoration and power gain.

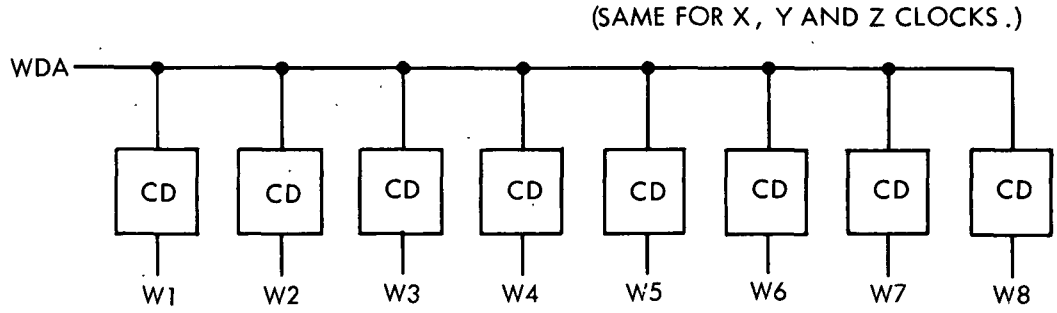


Figure 2-11. Clock Drivers

2-48. *TIMING GATE GENERATOR.* The timing gate generator consists of a control circuit and a seven-bit modified shift register (figure 2-12). The shift register is gated to ultimately force "0's" in positions 2 thru 7 (gating not shown in figure 2-12). The "0's" are complemented to "1's" on subsequent shifts, and when the resulting series of

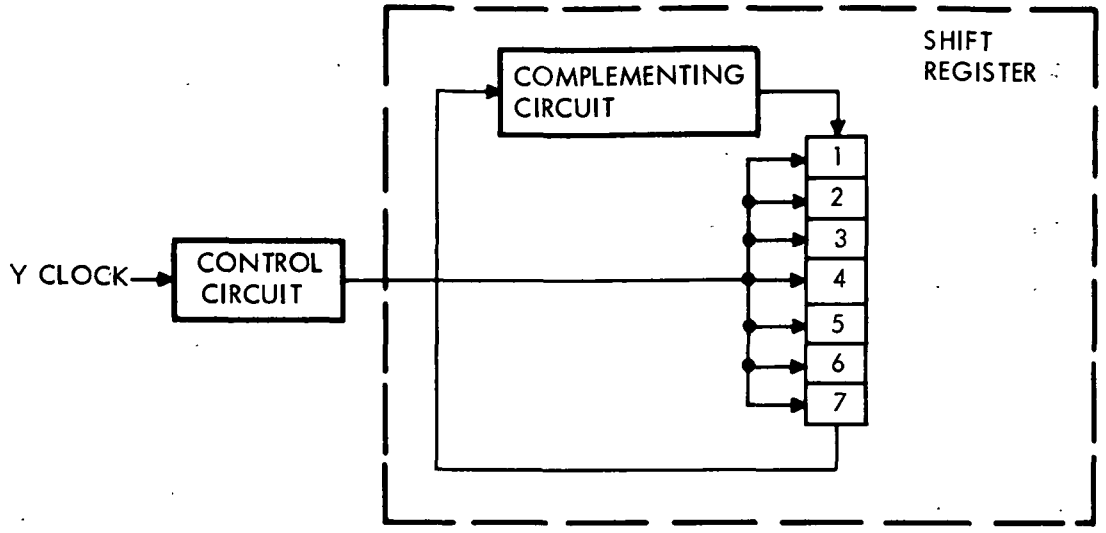


Figure 2-12. Timing Gate Generator, Block Diagram

"1's" emerge from the shift register, they are complemented back to "0's". Therefore, the shift register continuously cycles a series of seven "0's" followed by seven "1's".

2-49. The rate at which the shift register is cycled is determined by the control circuit, which is a binary counter driven by the Y clock from the computer. Each shift of the register occurs at W clock (or every bit gate, since a bit gate is four successive clocks wide).

2-50. Control Circuit. The control circuit consists of a pair of latches interconnected to form a binary counter (figure 2-13). The ABD latch stores the configuration of the AD latch during an X clock and steers the AD latch to its complementary state on each following Y clock. When enabled, an additional gate on the set side of the AD latch opens every Z clock to hold the AD latch set, except during Y clock. This gate is used for synchronizing purposes as will be explained later.

2-51. Shift Register. The shift register consists of seven latches connected in series (figure 2-14). As long as any "1's" exist in latches G2D through G7D, gate A1 cannot open. Ultimately, any "0's" in latches G2D through G7D will be shifted out to open gate A2 and reset latch G1D. Latch G1D will remain reset, effectively cycling "0's" into the shift register until latches G2D through G7D are all reset. Then gate A1 will open, setting latch G1D and effectively cycling "1's" into the register. Latch G1D will remain set as long as "0's" are being cycled out of latch G7D. The complementing circuit previously mentioned is actually latch G1D with its driving gates, A1 and A2.

2-52. In this shift register, "rippling" is prevented by the control circuit, which gates the odd-numbered latches (G1D, G3D, etc.) and the even-numbered latches in alternate modes, i.e., the set sides of the odd-numbered latches are gated at the same time that the reset sides of the even-numbered latches are gated. Consequently, a set condition cannot be propagated through successive latches on any one shift; the same is true for a reset condition.

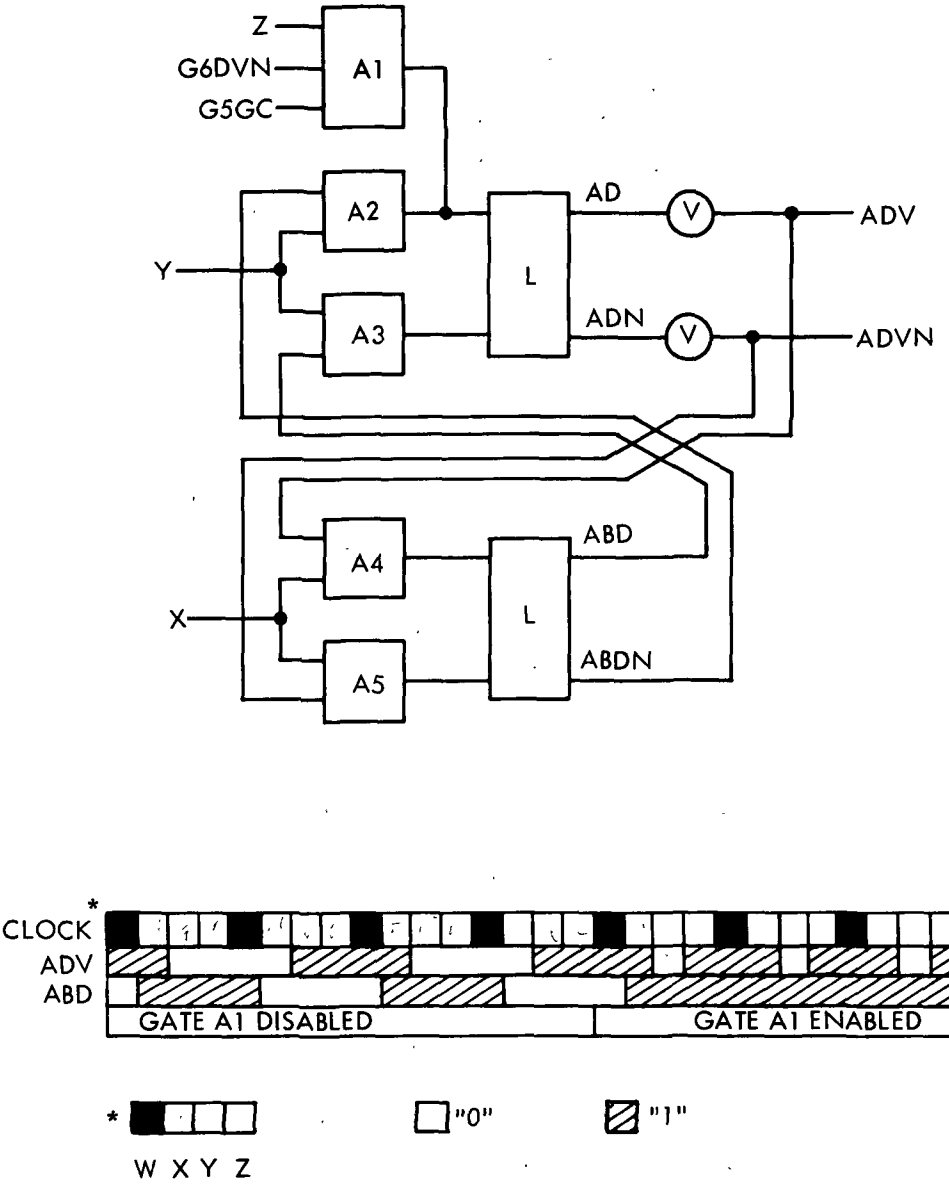


Figure 2-13. Control Circuit

2-53. Identification of Bit Gates. The outputs of the timing gate generator are diagrammed in figure 2-15. This figures shows transition times, i.e., the time that must be allowed for a signal to complete the transition between "0" and "1" or between "1" and "0". Bit gate 1 may be identified as the coincidence of signals G1DV and G2DVN; however, this identification is valid only during the Y and Z clocks, since G1DV is in transition during the W and X clocks. Bit gate 1 may be identified during the W and X clocks by the coincidence of signals G2DVN, G7DVN and ADVN. Therefore, three signals are needed to identify bit gates during W and X clocks, whereas only two signals are needed during Y and Z clocks.

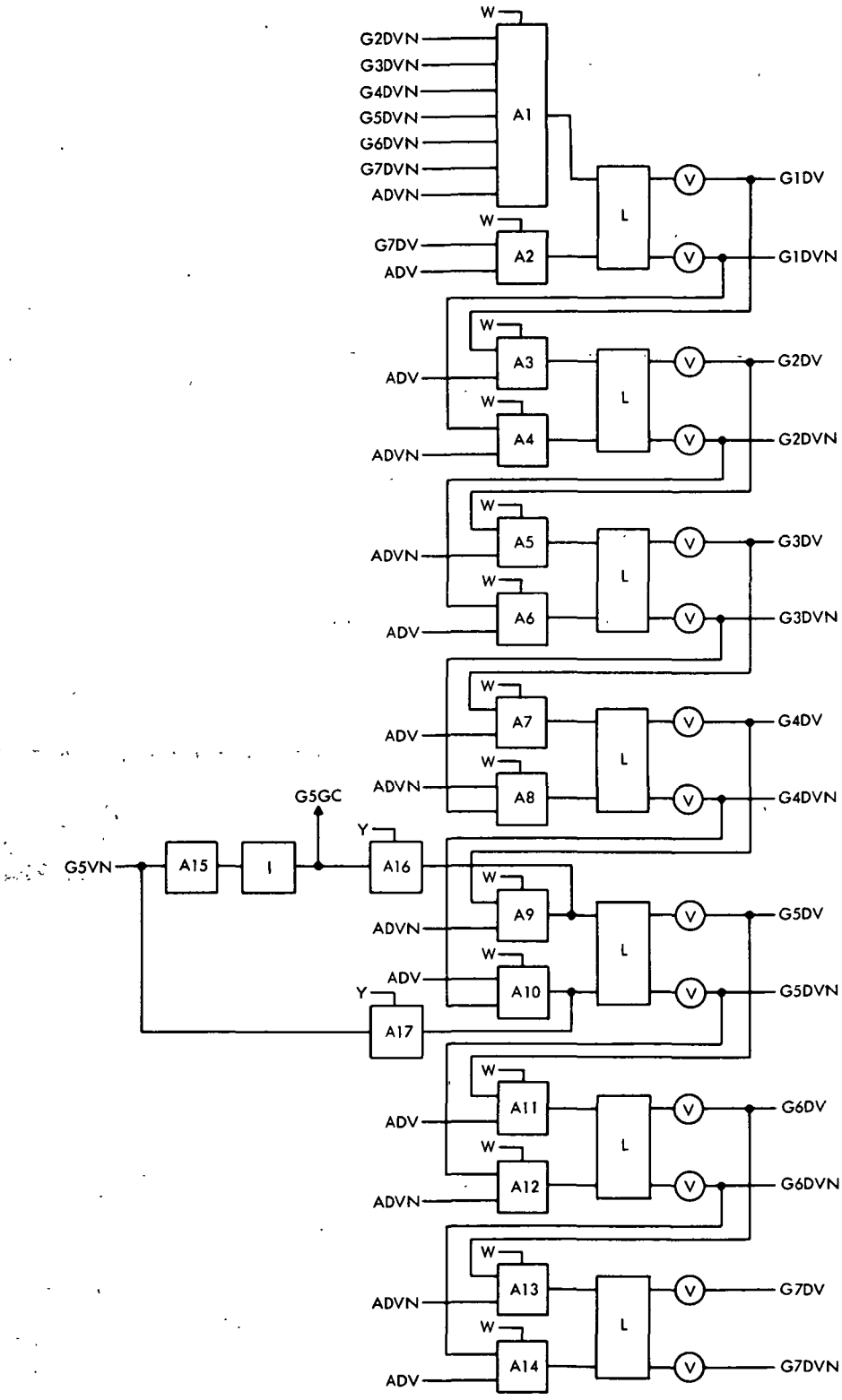


Figure 2-14. Shift Register

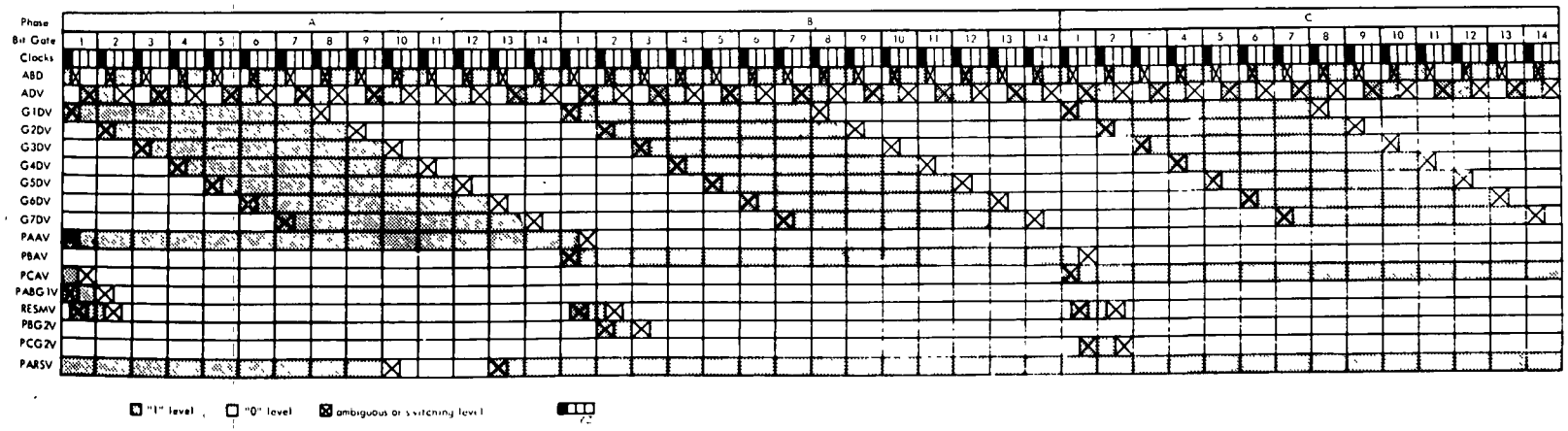


Figure 2-15. Data Adapter Timing Diagram

2-54. Bit gates are decoded at the point where they are used. The combination of signals used to identify bit gates are as follows:

Bit Gate	W or X Clock	Y or Z Clock
1	G7DVN, G2DVN, ADVN	G1DV , G2DVN
2	G1DV , G3DVN, ADV	G2DV , G3DVN
3	G2DV , G4DVN, ADVN	G3DV , G4DVN
4	G3DV , G5DVN, ADV	G4DV , G5DVN
5	G4DV , G6DVN, ADVN	G5DV , G6DVN
6	G5DV , G7DVN, ADV	G6DV , G7DVN
7	G6DV , G1DV , ADVN	G7DV , G1DV
8	G7DV , G2DV , ADV	G1DVN, G2DV
9	G1DVN, G3DV , ADVN	G2DVN, G3DV
10	G2DVN, G4DV , ADV	G3DVN, G4DV
11	G3DVN, G5DV , ADVN	G4DVN, G5DV
12	G4DVN, G6DV , ADV	G5DVN, G6DV
13	G5DVN, G7DV , ADVN	G6DVN, G7DV
14	G6DVN, G1DVN, ADV	G7DVN, G1DVN

2-55. Synchronization. The timing gate generator is required to operate in synchronization with an identical circuit in the computer. For purposes of synchronization, the computer provides signal G5VN, which is the equivalent of G5DVN in the data adapter shift register. Signal G5VN is fed through an isolating AND gate and an inverter to become G5GC which represents the "1" state of the G5 latch in the computer.

2-56. Whenever G5VN becomes a "1", latch G5DV will be reset; conversely, whenever signal G5V in the computer becomes a "1", G5GC will become a "1" and set latch G5DV. If the signal ADVN is a "1" at this time (an in-sync condition between ADVN and its counterpart in the computer), the next ADV signal will transfer the "1" from the G5D latch into the G6D latch in normal fashion. The shift register will continue to operate, with gate A15 cycling a "1" into latch G5D on every shift for the duration of G5GC. The series of "1's" introduced into latch G5D is, of course, complemented to "0's" in the process of being shifted into latch G1D. At the end of signal G5GC, latched G1D through G4D will be reset and the remaining latches will all be set. Figure 2-15 shows this to be the configuration for bit gate 11. The register makes seven more shifts during the absence of G5GC, reaching the configuration for bit gate 4. On the next shift, latch G5D will be set by the normal shift operation at the same time that signal G5GC is generated; thus, the shift register is synchronized with the corresponding register in the computer.

2-57. Basically, the shift register is synchronized by forcing its configuration to bit gate 11 and releasing it at the end of the computer bit gate 11 (i.e., the end of G5GC). A glance at the timing diagram (figure 2-15) will show that the start of bit gate 12 is coincident with the start of the ADV signal. If the ADV signal is out-of-phase (180°) with its corresponding signal in the computer, the first ADV pulse following bit gate 11 would occur at the beginning of what should be bit gate 13, and the data adapter timing would lag the computer timing by one bit gate.

NOTE

The ADV signal can only be either in-sync or 180° out-of sync with its corresponding signal in the computer, since both signals are driven from the same source, i.e., the Y clock.

2-58. In one case, to synchronize an out-of-phase ADV signal, the shift register is forced to its bit gate 11 configuration at what should be bit gate 10 time. The first out-of-sync ADV pulse following bit gate 10 time occurs at bit gate 12, which is the next desired configuration of the shift register and an in-sync condition for the ADV signal.

2-59. If latch G6D is in the set condition at the time latch G5D is set by G5GC, the next pulse will be ADVN (remembering that ADV is out-of-sync), and the G7D latch will be set. Latch G7D is therefore set one shift earlier than it would be if ADV were not out-of-sync. Thus, the forced bit gate 11 configuration is shifted into the register one bit gate early.

2-60. In the other case, the ADV signal is synchronized by forcing the ADV latch to its set condition at the time an even-numbered latch is to be set (figure 2-15). If latch G6D is in its reset condition at the time that G5GC is generated, gate A1 (figure 2-13) of the AD latch will open and set the AD latch. This causes latch G6D to be set, since latch G5D has been set by G5GC. Since latch G6D, an even-numbered latch, has been set during ADV time, the ADV signal is now in-sync.

2-61. PHASE GENERATOR. The phase generator consists of a three-step ring counter formed from three latches (figure 2-16). The ring is stepped at bit gate 1 time. The phase generator is synchronized with its counterpart in the computer by signal PBGC. When signal PBGC is a "1", gates A7, A8 and A9 open (at bit gate 2 time) to set the PBA latch and reset latches PCA and PAA.

2-62. The first bit gate 1 after the ring has been synchronized will set the PCA latch (gate A1), and two clocks later, the PBA latch will be reset (gate A6). At the following bit gate 1 time, latch PAA will be set (gate A3), and two clocks later the PCA latch will be reset (gate A2). The following bit gate 1 will set latch PBA (gate A5), and two clocks later, latch PAA will be reset (gate A4), returning the ring to its synchronized condition. Two clocks after latch PAA is reset, the PBGC signal will attempt to synchronize the ring, but the ring will already be in its synchronized condition.

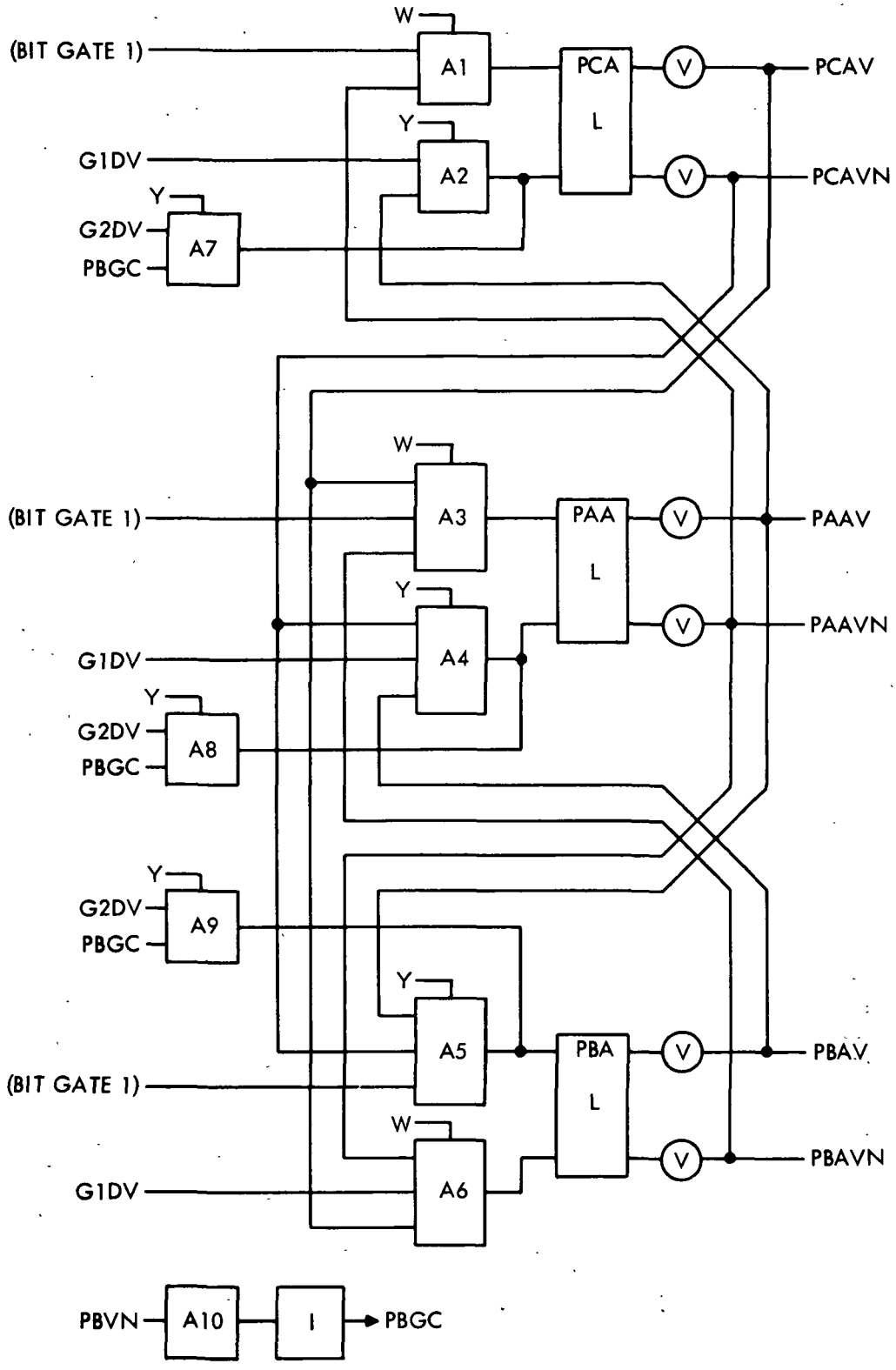


Figure 2-16. Phase Generator

2-63. The outputs of the phase generator are shown in figure 2-15. The outputs of the ring counter correspond to the theoretical phase times except during bit gate 1, where transition time and overlap occur. To properly identify phase time during any bit gate 1, it is necessary to sense the coincidence of timing signals as follows:

	Y or Z Clock		W or X Clock	
Phase A	PAAV, PBAVN	and	PCAV, PBAVN	and G2DVN,
Phase B	PBAV, PCAVN	G1DV,	PAAV, PCAVN	G7DVN,
Phase C	PCAV, PAAVN	G2DVN	PBAV, PAAVN	ADVN

2-64. SPECIAL TIMING. Special timing is provided by four latches (figure 2-17) which sense various combinations of the timing signals previously discussed. (Additional timing signals are developed in the data adapter, but their use is so specific that they are discussed with the particular circuit in which they are used.)

2-65. The RESM latch is set every bit gate 1 time and reset on the following bit gate 2 (figure 2-17). The PBG2 latch ANDs the RESM signal with PBAV to provide a signal during bit gate 2 of phase B. Latch PCG2 is set at the middle of bit gate 1 (phase C) and reset at the middle of the following bit gate. Thus, PCG2 "straddles" bit gates 1 and 2, but is only usable during bit gate 2 because of transition time. Latch PABG1V is set at the beginning of bit gate 1 (phase A) and reset at the beginning of bit gate 2.

2-66. FREQUENCY GENERATOR.

2-67. GENERAL. The frequency generator (actually an extension of the timing circuits) provides pulse intervals in the millisecond range for use as real-time reference.

2-68. The frequency generator consists of a control circuit, a three-bit shift register and a frequency divider (figure 2-18). The shift register is so gated that, irrespective of initial conditions when power is first applied, "0's" will be eventually forced into positions 2 and 3. The "0's" are complemented to "1's" on subsequent shifts, and when the resulting series of "1's" emerge from the shift register, they are complemented back to "0's". The shift register, therefore, continuously generates a series of three "1's" followed by three "0's".

2-69. The rate at which the shift register is cycled is determined by the control circuit which is a binary counter driven by the PCG2V timing pulse. Each shift of the register is made to occur at bit 2 of phase C.

2-70. The frequency divider divides one of the outputs of the shift register by two.

2-71. CONTROL CIRCUIT. The control circuit consists of a pair of latches interconnected to form a binary counter (figure 2-19). The REXCC latch stores the complementary configuration of the REXC latch during X time and steers the REXC latch to this configuration at W time of the next PCG2V pulse.

2-72. SHIFT REGISTER. The shift register consists of three latches connected in series (figure 2-20). As long as any "1's" (set condition) exist in latches RECB and RECC, gate A1 cannot open. Ultimately, any "1's" in latches RECB and RECC will be shifted out to open gate A2 and reset latch RECA. Latch RECA will remain reset and

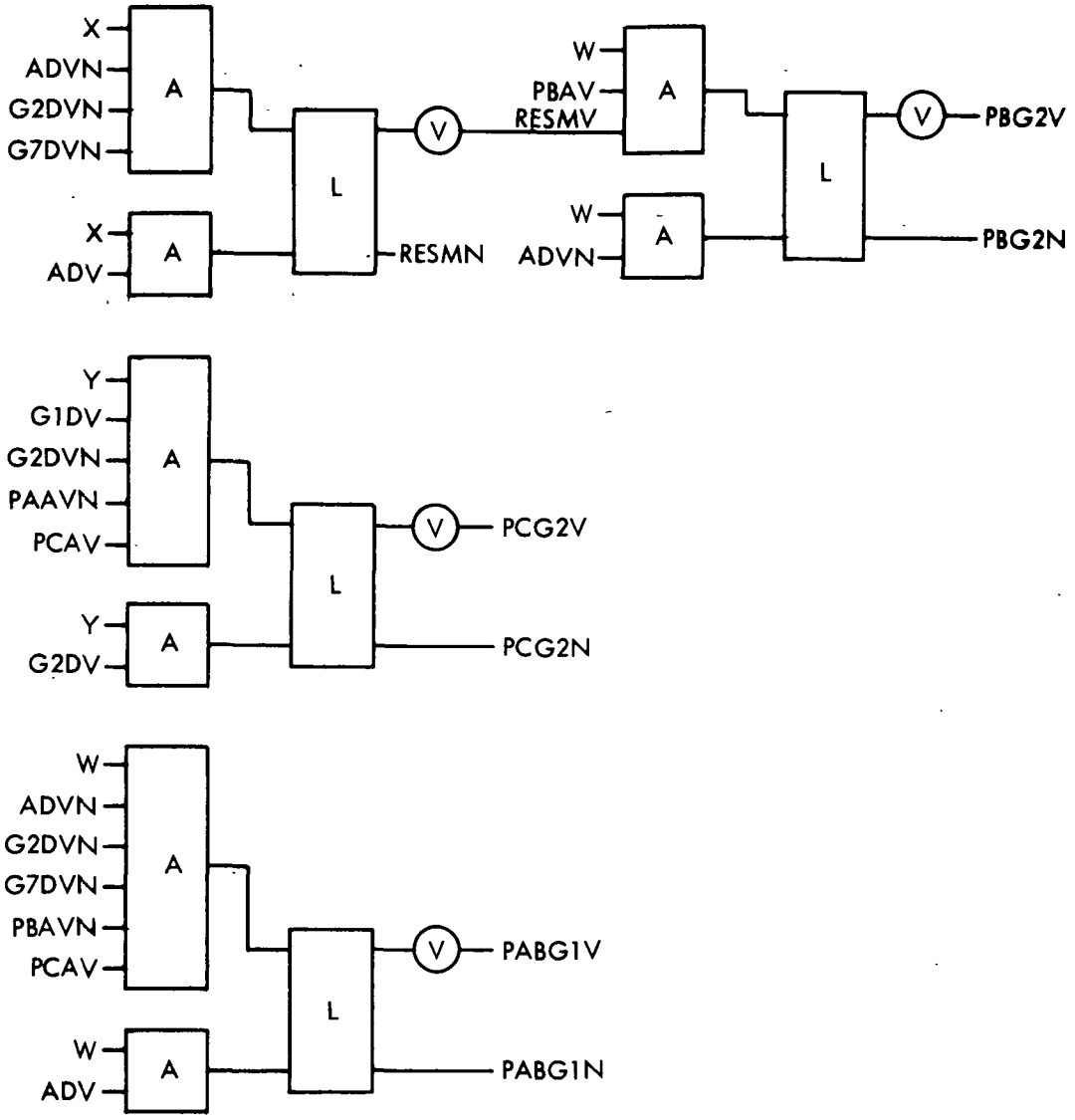


Figure 2-17. Special Timing Circuits

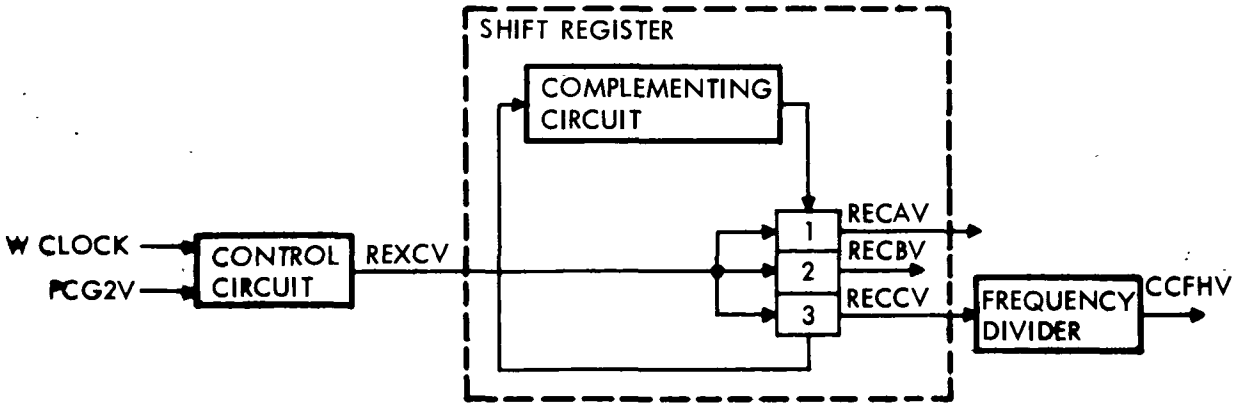


Figure 2-18. Frequency Generator, Block Diagram

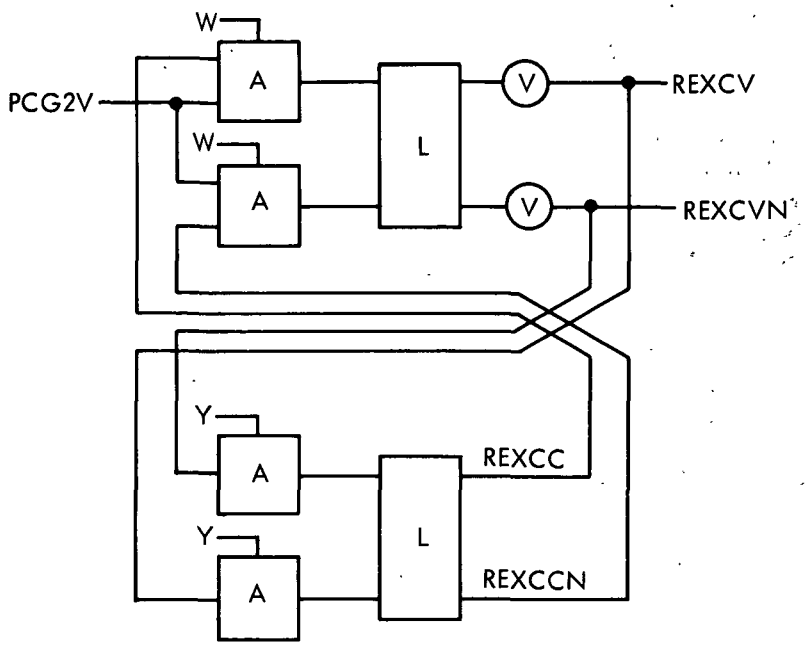


Figure 2-19. Control Circuit

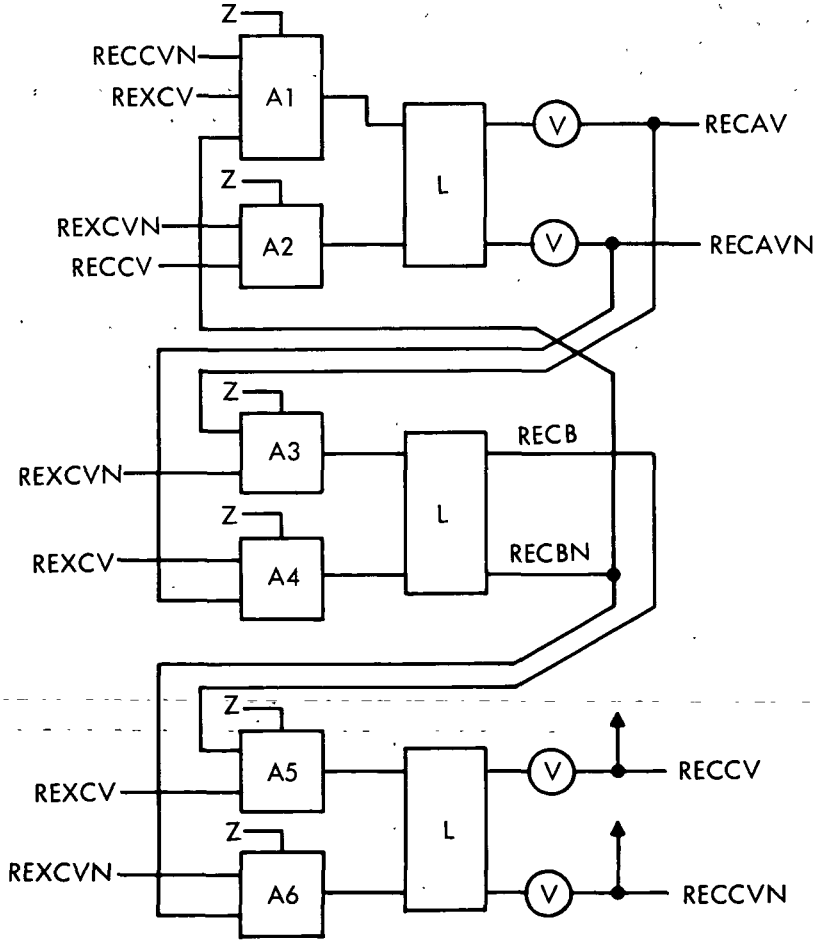


Figure 2-20. Shift Register

cycle "0's" into the shift register until latches RECB and RECC are both reset. Then gate A1 will open, setting latch RECA and effectively cycling "1's" into the register. Latch RECA will remain set as long as "0's" are being cycled out of latch RECC.

2-73. Shift register "rippling" is prevented by the control circuit which gates alternate latches on each shift, e.g., the set side of the RECB latch is gated at the same time that the reset side of the RECA and RECC latches are gated. Consequently, a set condition cannot be propagated through successive latches on any one shift. The same is true for a reset condition.

2-74. The outputs of the control and shift register latches are diagrammed in figure 2-21. The pulse width of each of the shift register latch outputs is nine phase times or 246.09375 milliseconds (nominal). For all practical purposes, this value may be assumed to be 1/4 millisecond.

2-75. FREQUENCY DIVIDER. The frequency divider (figure 2-22), like the control circuit, is a pair of latches interconnected to form a binary counter. Latch CCFH changes state every RECCV time, thereby producing a "1" every two RECCV times. Output pulse width of the CCFH latch is twice that of the RECCV signal, or about 1/2 millisecond.

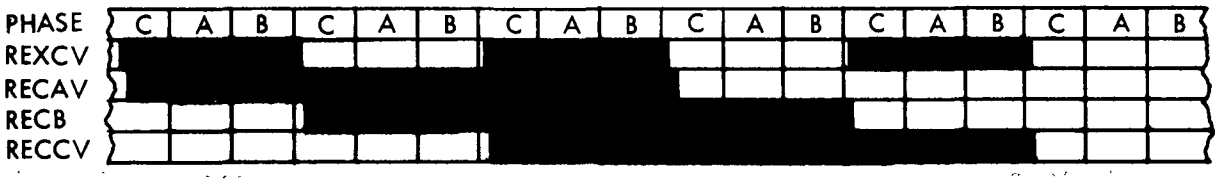


Figure 2-21. Frequency Generator, Timing Diagram

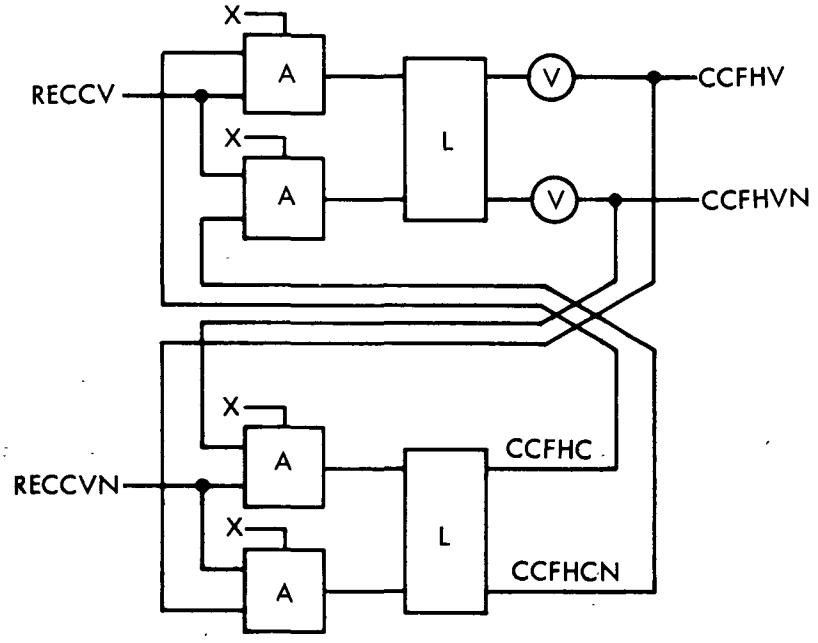


Figure 2-22. Frequency Divider

2-76. DELAY-LINE REGISTERS.

2-77. A delay-line register consists of an ultrasonic delay line and associated logic circuits which feed, modify or recirculate data through the line. The duration of delay is equivalent to an operation cycle (42 bit-gates). The delay line itself provides a delay of 42 bit-gates less three clocks; the remaining delay of three clocks is provided by the logic circuits.

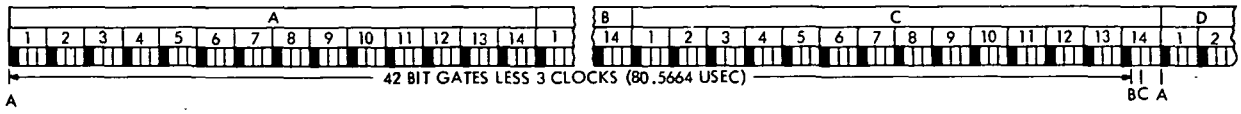
2-78. As soon as 42 bits have been loaded into the delay line, they commence to emerge, i. e., bits clocked in at a given clock time will start to emerge one clock time after the 42nd bit is read in. A bit clocked in at W time, for instance, will emerge at X time, 42 bits later (figure 2-23). Similarly, a bit clocked in at X time will emerge at Y time and bits clocked in at Y and Z times will emerge at Z and W times respectively (all 42 bit-gates later).

NOTE

The delay line driver is clocked by BO1, a timing signal from the computer with a pulse width of about half a clock. This signal provides better separation of pulses within the delay line. This signal is disregarded in figure 2-23.

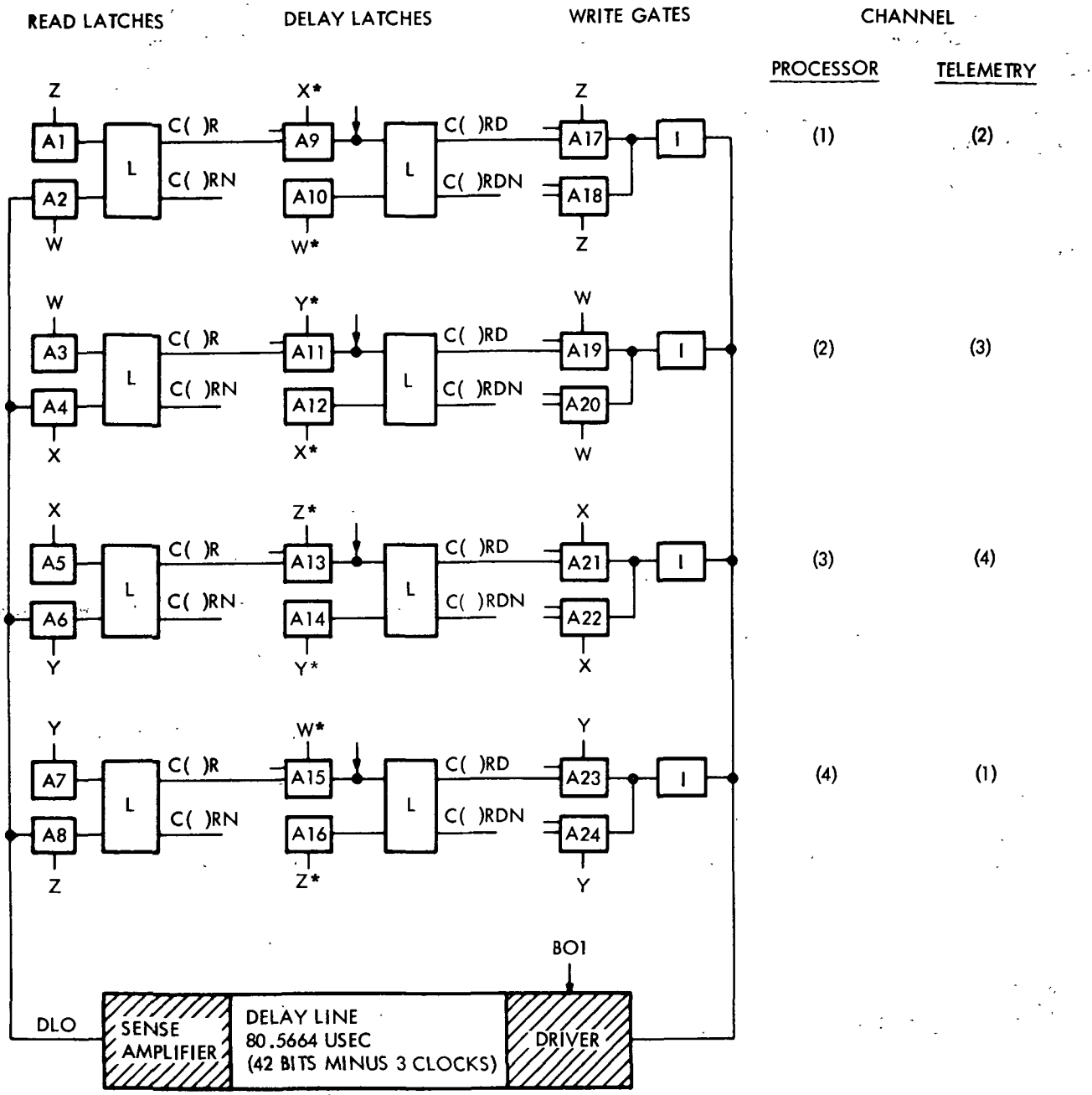
2-79. The output of the delay line is fed to four read latches (figure 2-24). A "1" emerging from the delay line sense amplifier represents a "0" initially fed into the delay line write logic. Consequently, a "1" from the delay line resets its associated read latch. The read latches are set just prior to the emergence of each bit from the delay line and are either reset or not reset according to the nature of the bit from the delay line.

2-80. The outputs of the read latches are fed to delay latches which, if suitably gated, assume the configuration of their respective read latches. The purpose of the delay latches is to allow logical operations to be performed on the outputs of the read latches, e. g., additional gates (not shown in figure 2-24) may be used to drive any delay latch to the configuration (or its complement) of any one of the read latches. (The logical operations which select the various delay latch gates will be covered in the appropriate logic circuit descriptions.)



A - BIT ENTERED INTO DELAY LINE
B - BIT EMERGES FROM DELAY LINE AND IS STORED IN READ LATCH
C - BIT TRANSFERRED INTO DELAY LATCH

Figure 2-23. Delay-Line Register Timing



NOTE: FOR TELEMETRY DELAY LINE REGISTER, PREFIX ALL SIGNAL NAMES (EXCEPT CLOCKS) WITH D

*FOR TELEMETRY DELAY LINES, ADD ONE CLOCK, I.E., X BECOMES Y, ETC.

Figure 2-24. Delay Line Register

2-81. The outputs of the delay latches are fed to write gates which select any desired input for read-in to the delay line, including the output of the delay latches if the object is to circulate the contents of the delay line. The write gates feed the delay line driver through an inverter which provides the logic inversion previously noted in regard to the read latch operation.

2-82. The data adapter has two delay line registers, one triplex and one simplex. The triplex delay line register is used for Processor Storage and the simplex is used for Telemetry Storage.

2-83. There are four delay-line channels corresponding to the four clock times at which data is fed to the delay line. For Processor storage, channel 1 is fed at Z clock, and channels 2, 3 and 4 are fed at W, X and Y clocks, respectively. For Telemetry storage, channel 1 is fed at Y clock and channels 2, 3 and 4 are fed at Z, W and X clocks, respectively.

2-84. GENERAL DESCRIPTION OF FUNCTIONS.

2-85. The data adapter contains five major functional circuits:

1. Computer Output Circuits - convert computer data from serial to parallel and store this data in registers for subsequent use by the guidance system.

2. Internal Data Sampler - converts various digital signals from the computer and from within the data adapter to a serial form for subsequent use by the Telemetry Circuits.

3. System Data Sampler - converts various digital signals either from the system or from system data processors to a serial form for use by the computer and by the Telemetry Circuits.

4. Processors - convert various types of system signals to a digital form for use by the System Data Sampler.

5. Telemetry Circuits - assemble, tag and store data from the computer and both Data Samplers for subsequent telemetering.

2-86. A simplified block diagram of the data adapter circuits is shown in figure 2-25. On this diagram, the Computer Output Circuits include the Error Processor, the Data Select Circuit and the Output Registers. The Telemetry Output Circuits include the Telemetry Storage Circuit and the Telemetry Registers.

2-87. Timing and power circuits are not included in the functional circuit descriptions, since they are considered to be subsidiary to the functional circuit operations. (Although power switching affects system operation, it is included with the power circuit descriptions for convenience.)

2-88. A detailed block diagram of the data adapter functional circuits is shown in figure 2-26. This diagram is provided for reference purposes as the details of the functional circuits are discussed. Timing, power, and address decode circuits are not shown on this diagram.

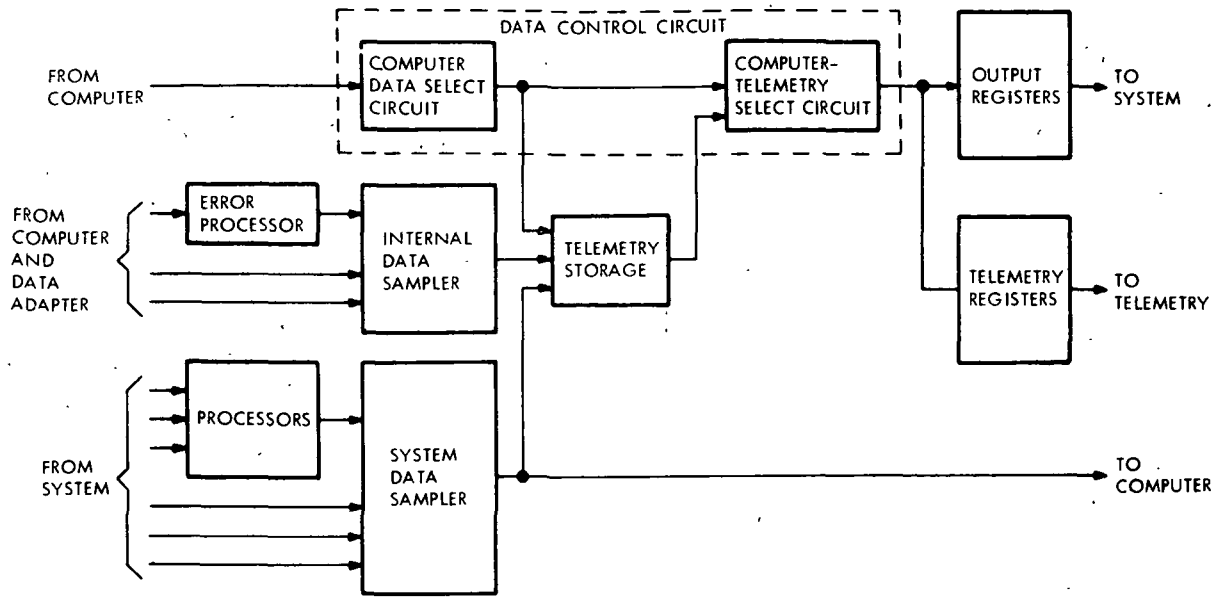


Figure 2-25. Data Adapter, Simplified Block Diagram

2-89. COMPUTER OUTPUT CIRCUITS.

2-90. GENERAL.

2-91. Outputs from the computer are fed to the data adapter either to be telemetered or to be converted to guidance system control signals. Computer outputs consist of error signals, address codes, and serial data. The error signals are fed to an error processor which assembles and stores them for subsequent telemetering. The address codes are decoded and used to control various functions within the data adapter. The serial data is stored for subsequent telemetering and, if required, is fed to storage registers for use as guidance system control signals.

2-92. ERROR PROCESSOR.

2-93. The Error Processor samples 16 externally generated error indications and 9 data adapter generated error indications. Upon receipt of an error indication, which may occur at any time, the error processor stores the error indication until externally commanded to clear it. The error processor also generates a two-bit code which indicates the clock time the error indication was sensed and initiates storage of this code and additional error time indications in the Internal Data Sampler. The error processor conditions the Internal Data Sampler to process the stored error indications and error time indications at the proper time. The error processor consists of: 1) 26-bit storage register with associated control circuits; 2) two clock error latches (ECSA and ECSB); 3) two storage control latches (ETTS and ETSD); 4) two timing latches (ETTC and ETCR).

2-94. The 26-bit storage register stores the error indications until commanded to clear. A typical storage register latch is shown in figure 2-27 together with a table of applicable input conditioning signals and the output nomenclature of the 26 storage latches.

2-95. The ADI signal equals "0" from bit times A-9 through A-11. Signal ADI inhibits invalid TMR disagreements during the time that latches associated with disagreement detector inverters DDI (1A), (1B), (1C), (2A), and (2B) are reset. The EMRS1 reset

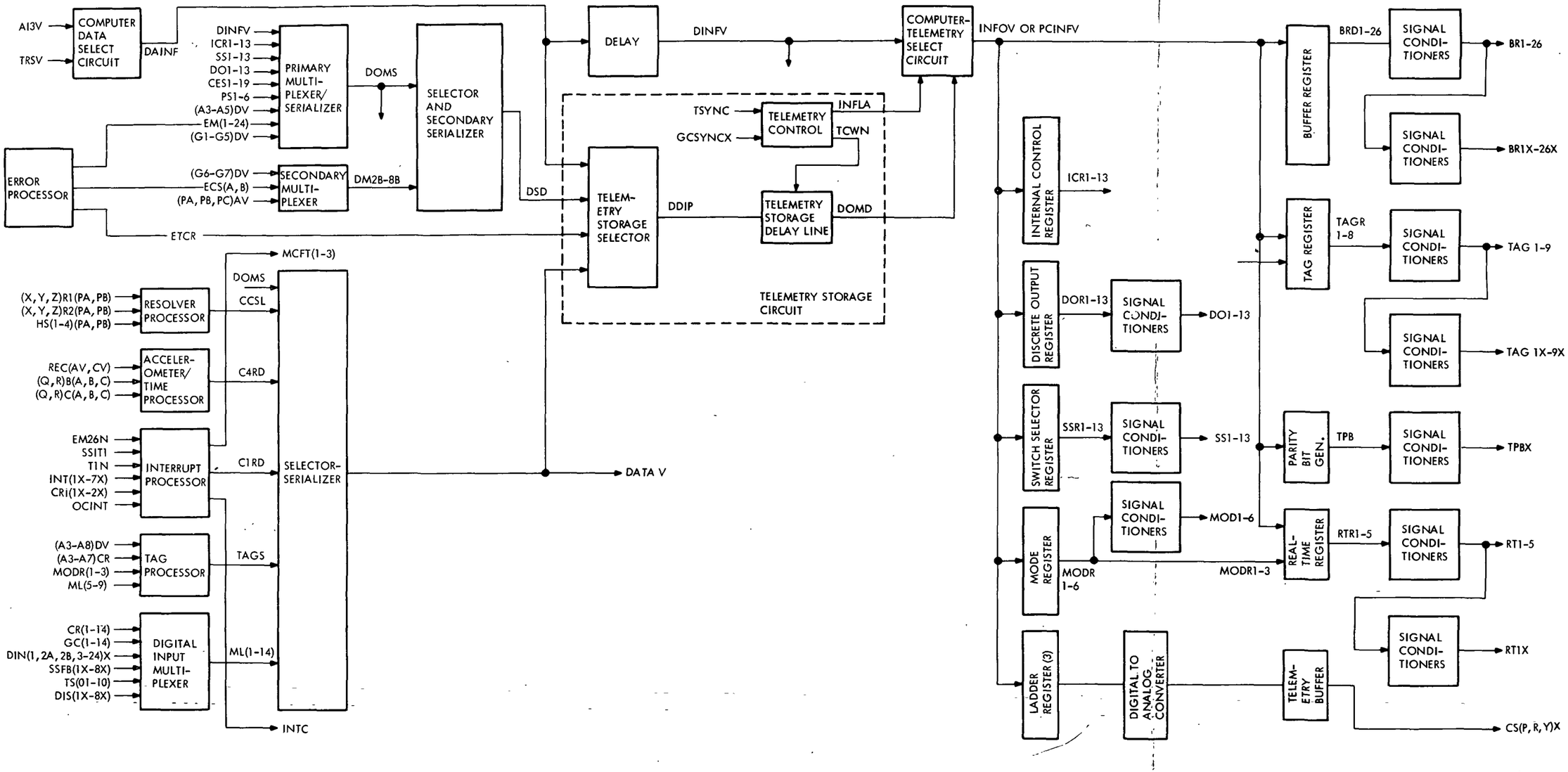
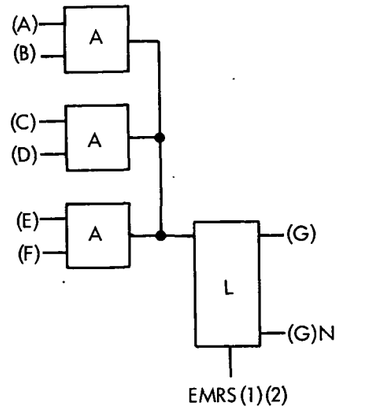


Figure 2-26. Data Adapter, Detailed Block Diagram



(A)	(B)	(C)	(D)	(E)	(F)	(G)
DDI1A	ADI	DDI1B	ADI	DDI1C	ADI	EM1
-	-	DDI2A	ADI	DDI2B	ADI	EM2
-	-	DDI3A	-	DDI3B	-	EM3
-	-	-	-	DDI4	ADI	EM4
-	-	-	-	DDI5	-	EM5
-	-	-	-	DDI6	-	EM6
-	-	-	-	DDI7	-	EM7
-	-	-	-	DDI8	-	EM8
-	-	-	-	SCB	-	EM9
		SPARE				EM10
-	-	-	-	EP1	-	EM11
-	-	-	-	EP2	-	EM12
-	-	-	-	EP3	-	EM13
-	-	-	-	EP4	-	EM14
-	-	-	-	EP5	-	EM15
-	-	-	-	EP6	-	EM16
-	-	-	-	EP7	-	EM17
-	-	-	-	EP8	-	EM18
-	-	-	-	EP9	-	EM19
-	-	-	-	EP10	-	EM20
-	-	-	-	EP11	-	EM21
-	-	-	-	EP12	-	EM22
-	-	-	-	EP13	-	EM23
-	-	-	-	A1EAMV	-	EM24
-	-	-	-	A1EBMV	-	EM25
-	-	-	-	A1TLCV	-	EM26

Figure 2-27. Error Storage Register

signal equals "0" at bit time B-3 when the error monitor address is selected (EMA = "1"); EMSR2 equals "0" at bit time C-3 when EMA equals "1". (The storage latches are cleared at these times, immediately after the associated latches are parallel transferred into the Internal Data Sampler, to insure that additional error indications are not lost.) The storage register outputs are ORed together (figure 2-28) to produce a single error-indicating signal for determining the time the error was sensed.

2-96. The ECSA and ECSB latches (figure 2-29) generate the two-bit code which indicates the clock time that the error was sensed. ECSA and ECSB are alternately complemented as shown in figure 2-29; however, when an error occurs ERRSN becomes a "0" to halt the complementing action. The code stored in the ECSA and ECSB latches, while ERRSN equals "0", indicates the error clock time. The error codes are shown on the chart in figure 2-29.

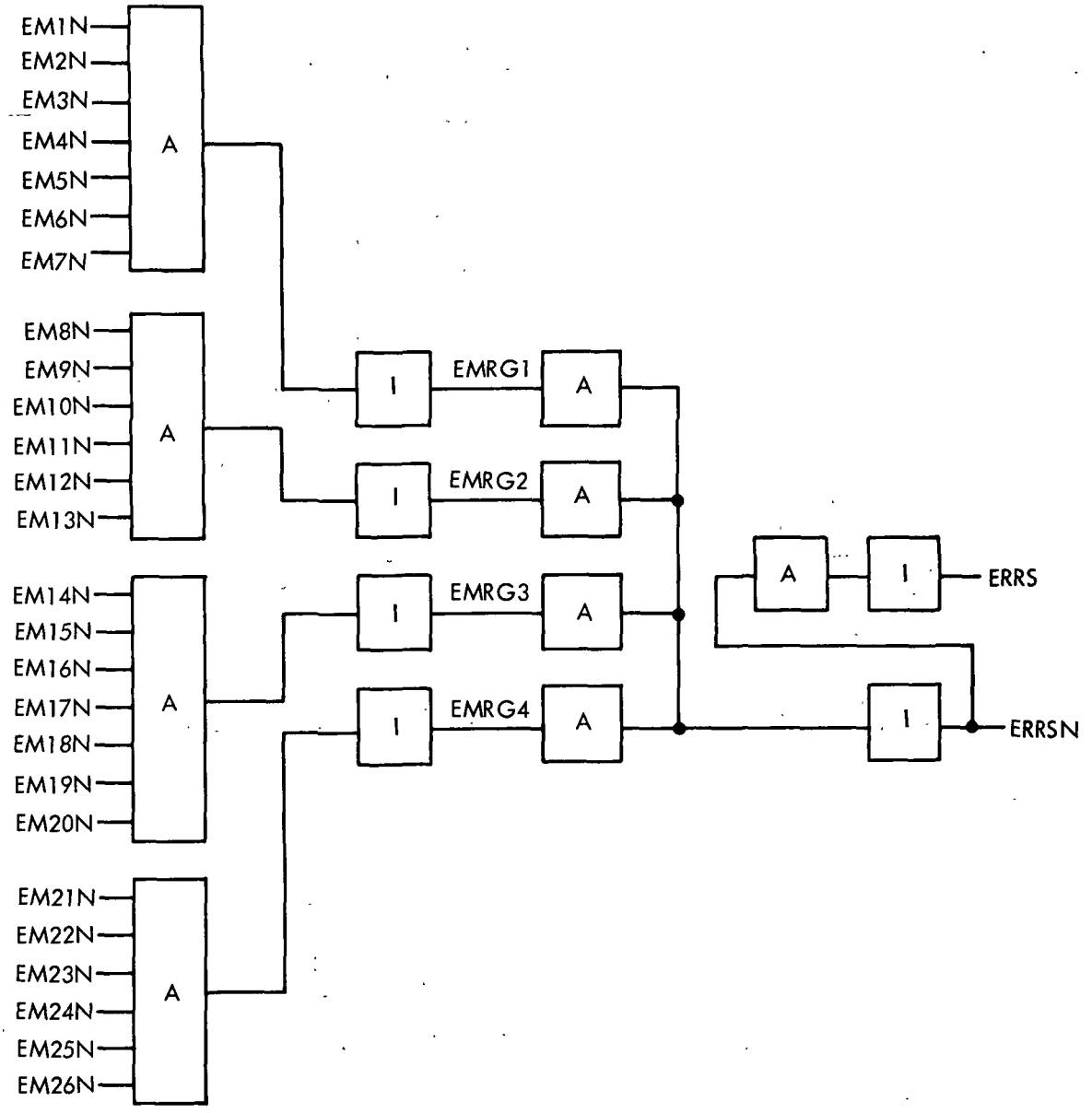
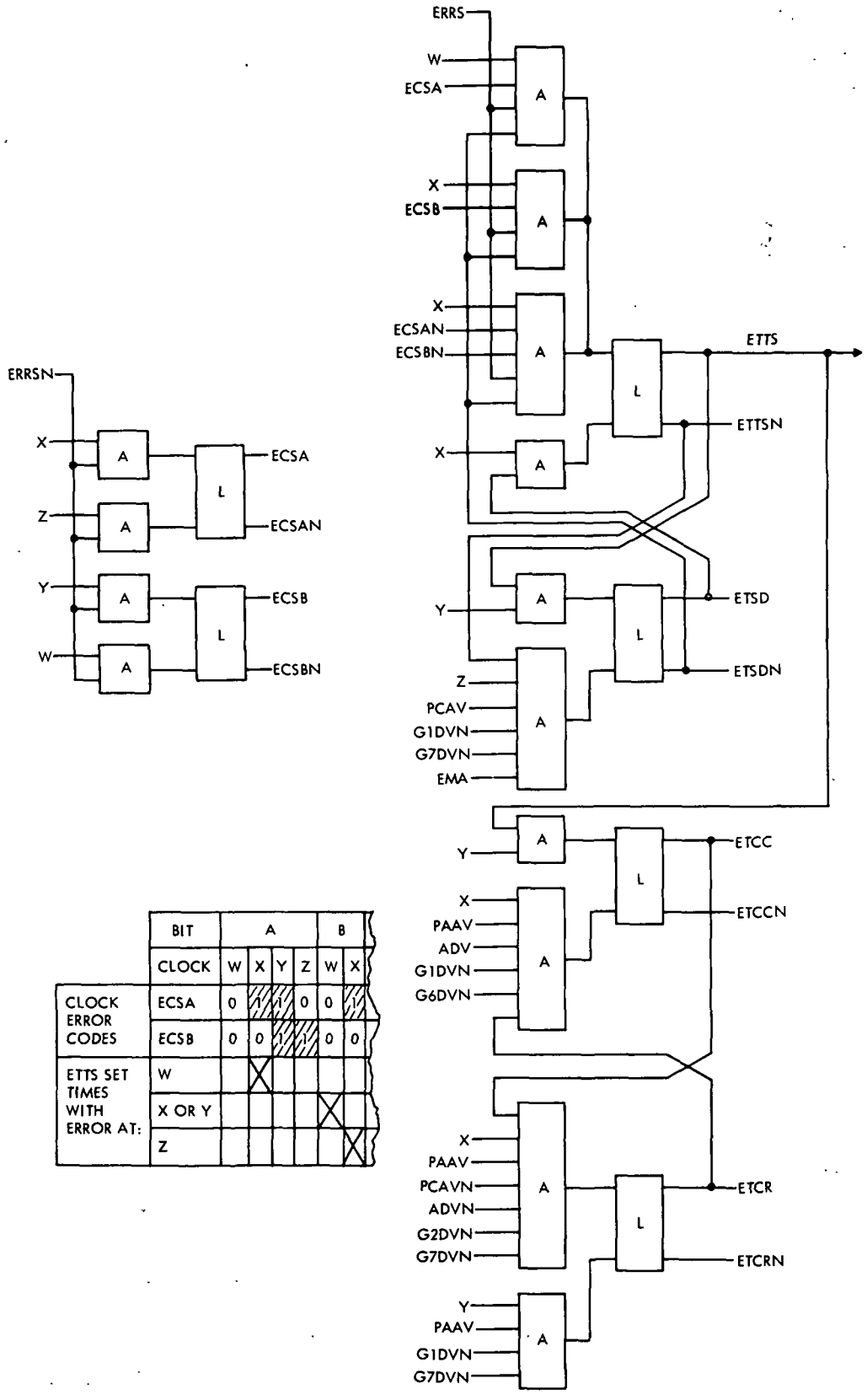


Figure 2-28. Error Or - Circuit

2-97. The ETTS latch initiates processing of the error data in the Internal Data Sampler. ETTS latch set times are shown in figure 2-29. Note that when errors occur at X, Y, or Z clock times, ETTS initiates storage of the bit time following the actual error bit time; a clock error code of 10, 11 or 01 indicates that the stored error time is delayed one bit time. The ETTS latch is conditioned by ECSA, ECSB, ECSAN, and ECSBN to avoid ambiguity in determining error bit time when errors occur at X clock time. Due to circuit delay, ERRS rises slightly after ERRSN drops. Thus, if it were not for the conditioning levels, ETTS could be set during X clock time errors, either at the current bit time or the following bit time. The ETTS conditioning levels insure a one-bit delay during X clock time errors to determine error bit time, reliably. ETTS remains set for approximately one bit time; then when ETSD equals "1", ETTS resets.



	BIT	A				B	
	CLOCK	W	X	Y	Z	W	X
CLOCK ERROR CODES	ECSA	0	1	1	0	0	1
	ECSB	0	0	1	1	0	0
ETTS SET TIMES WITH ERROR AT:	W		X				
	X OR Y					X	
	Z						X

Figure 2-29. Error Control Latches

2-98. The ETSD latch prevents ETTS from initiating storage of error times after storage of the initial error time in the event that multiple errors occur prior to resetting of the error storage register. When the error monitor address is selected (EMA equals "1"), ETSD is reset at C-14-Z time.

2-99. The ETCC and ETCR latches provide conditioning levels at the proper times to enable the Internal Data Sampler to serialize the error indications. When ETTS equals "1", ETCC becomes set to enable ETCR to become set at B-1-X time. ETCR equals "1" from B-1-X through A-14-Y time to condition the Internal Data Sampler to process the error indications. Both ETCC and ETCR are reset during A-14 bit time.

2-100. ADDRESS DECODE.

2-101. Whenever the data adapter receives a PIO signal from the computer, address bits from the computer are decoded and the appropriate function is executed. The incoming address codes are divided into five groups according to the configuration of bits A1, A2, A8 and A9, as shown in figure 2-30. Specific codes within each group are identified by bits A3 through A7 as shown in figure 2-31. Prior to being decoded, the address bits are repowered by latches, figure 2-32. There is one latch for each of the nine address bits. The latches are loaded at A-14-Y time whenever the PIOD latch is set, and they store the address bits until the following A-10 bit time. The PIOD latch is set by the computer PIO command at A-14-W time and is reset at the following B-1-X time.

2-102. ADDRESS GROUPS 1 AND 3. The function of address groups 1 and 3 is to transfer data from the computer to telemetry registers. Bit A2 identifies the group and bit A8 identifies the source of data within the computer (accumulator or memory). Bits A3 through A7 and A9 serve only to identify the computer data. Thus, for groups 1 and 3, these address bits are assembled into a tag code which is telemetered along with the data. Group 1 and group 3 codes are sensed and used by the Computer Data Selector circuit, described later.

2-103. ADDRESS GROUP 2. The function of address group 2 is to transfer data from the computer into output registers or into processors. Basically, the difference between the group 2 data and the groups 1 and 3 data is that group 2 data is used to control certain functions, whereas group 1 and 3 data is simply telemetered as information.

2-104. Group 2 is identified by A1 = "0" and A2 = "1". This combination is sensed by the DARA latch, figure 2-33. Also sensing this combination is a gate-inverter doublet, INFLA-INFLAN which is used to control the Computer Data Selector Circuit, explained later. The DARA latch feeds eight other latches which complete the identification of the codes allotted to group 2. (See figure 2-33.) All of these latches are basically the same except for the CODE latch which is both reset by ETTCN and blocked by ETTS whenever an error occurs in order that system errors may be processed and telemetered in preference to crossover detector errors (CODE).

2-105. The LGA latch senses only bit A7. The remaining bits are picked up by latches L1A through L5A which are enabled by the LGA latch, figure 2-33.

2-106. The final latches in the group 2 category are the TC2A and TC3A latches. These latches are used to control the flow of computer data into two processors called countdown processors which will be explained later. Both of these latches decode the whole group of bits, A1 through A7, directly, rather than in a two or three-step operation as used by the group 2 latches previously described.

Group	A9	A8	A7	A6	A5	A4	A3	A2	A1	Function
1	X	0						0	0	To Data Adapter Telemetry Registers from Computer Accumulator
1A	0	1						0	0	To Data Adapter Telemetry Registers from Computer Main Memory
1B	1	1						0	0	To Data Adapter Telemetry Registers from Computer Residual Memory
2	X	0						1	0	To Data Adapter Output Registers from Computer Accumulator
2A	0	1						1	0	To Data Adapter Output Registers from Computer Main Memory
2B	1	1						1	0	To Data Adapter Output Registers from Computer Residual Memory
3	X	0						0	1	To Data Adapter Telemetry Registers from Computer Accumulator
3A	0	1						0	1	To Data Adapter Telemetry Registers from Computer Main Memory
3B	1	1						0	1	To Data Adapter Telemetry Registers from Computer Residual Memory
4	X	0						1	1	Read Peripheral Data and Errors
5	X	1						1	1	Read Resolver Processors

Note: X indicates either value ("1" or "0")

Figure 2-30. Address Group Codes

A7	A6	A5	A4	A3	(Group 2: A2="1", A1="0") Code = DARA	(Group 4: A8="0", A2="1", A1="1") Code DARO	(Group 5: A8="1", A2="1", A1="1") Code = CODGV
0	0	0	0	0	-	-	Read Backup No. 1
0	0	0	0	1	Mode Register - MODA	-	Read AF No. 3
0	0	0	1	0	Discrete Output Register (Reset) - DOR	-	-
0	0	0	1	1	Discrete Output Register (Set) - DOS	-	-
0	0	1	0	0	Internal Control Register (Set) - ICR	Read Error Monitor Register - EMA	Read FG No. 1
0	0	1	0	1	Internal Control Register (Reset) - ICR	-	-
0	0	1	1	0	Interrupt Register Reset - TC2A	-	Read CG No. 3
0	0	1	1	1	Switch Selector Register - SSR	-	-
0	1	0	0	0	Orbital Checkout - OCR - TLM (Refer to Telemetry Operations)	Read Command Receiver or RCA-110 - CRCA-MLA	Read CG No. 1
0	1	0	0	1	-	-	Read HS No. 1
0	1	0	1	0	Read Sw. Sel. and Dis. Output Regs. - SSDO	Read Discrete Input Spares - DISA-MLA	-
0	1	0	1	1	-	Read Discrete Inputs - DIAD-MLA	Read AF No. 2
0	1	1	0	0	Switch Selector Interrupt Counter - TC2A	-	-
0	1	1	0	1	Read COD Error - CODE	Read Telemetry Scanner - TSA-MLA	-
0	1	1	1	0	Inhibit Interrupt - TC3A	-	Read Backup No. 3
0	1	1	1	1	Minor Loop Timed Interrupt Counter - TC3A	Read Switch Selector - SSR-MLA	Read AC No. 2
1	0	0	0	0	Ladder Address - LGA	Read Real Time - MLA	Read Backup No. 2
1	0	0	0	1	-	Read Accelerometer Processor X - MBYPD	-
1	0	0	1	0	-	-	Read HS No. 3
1	0	0	1	1	-	Read Accelerometer Processor Z - MBYPD	Read AC No. 1
1	0	1	0	0	-	-	Read FG No. 4
1	0	1	0	1	-	Read Accelerometer Processor Y - MBYPD	Read HS No. 2
1	0	1	1	0	-	-	Read CG No. 4
1	0	1	1	1	-	Read Interrupt Storage - MBYPD	Read AC No. 3
1	1	0	0	0	-	-	Read CG No. 2
1	1	0	0	1	Ladder No. 1. - L1A	-	-
1	1	0	1	0	Ladder No. 2. - L2A	-	Read FG No. 3
1	1	0	1	1	Ladder No. 3. - L3A	-	Read AC No. 1
1	1	1	0	0	Ladder No. 4. - L4A	-	Read FG No. 2
1	1	1	0	1	Ladder No. 5. - L5A	-	Read HS No. 4
1	1	1	1	0	-	-	Read Backup No. 4
1	1	1	1	1	-	-	-

Figure 2-31. Address Codes

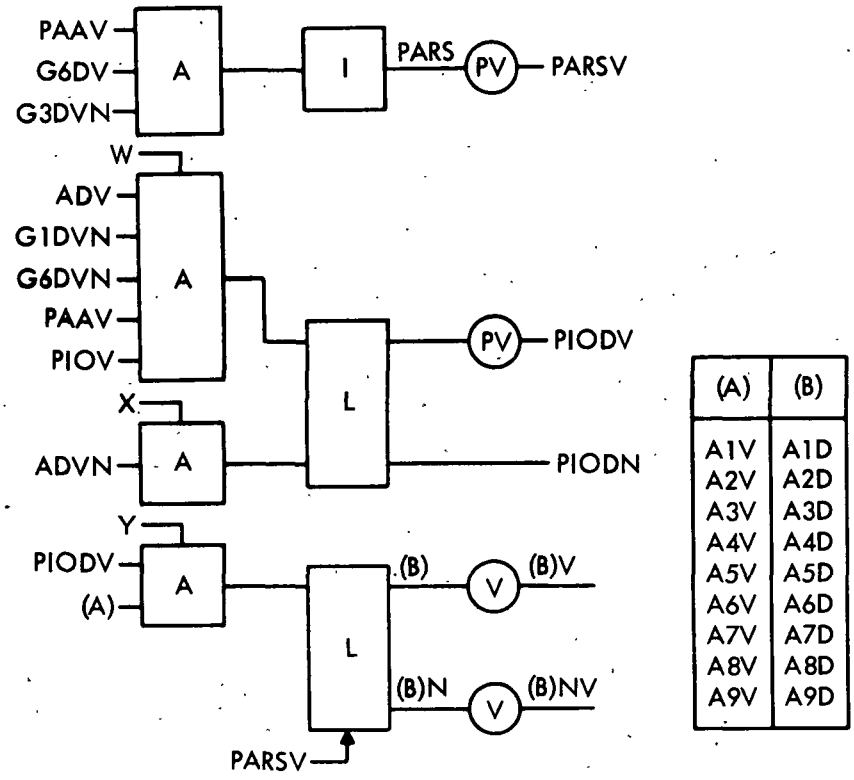
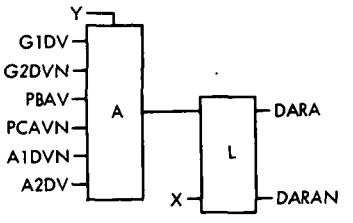


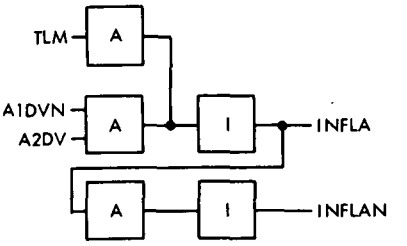
Figure 2-32. Address Latches and Control

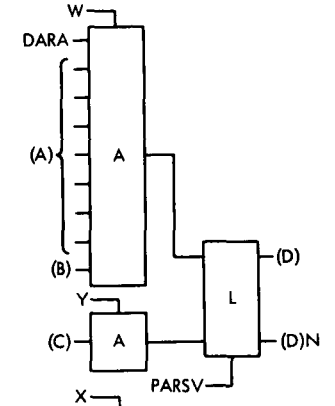
2-107. ADDRESS GROUP 4. The function of address group 4 is to transfer data from the data adapter (via the System Data Sampler, explained later) to the computer. Group 4 is identified by A1 and A2 = "1" and A8 = "0". This combination is sensed by the DARO latch, figure 2-34. The DARO latch feeds seven other latches which complete the identification of the codes allotted to group 4. (See figure 2-34) Since group 4 also commands the readout of certain processors to the computer, a special latch, MBYPD, is included. This latch disables readout of the system data through the System Data Sampler and allows the processor data to be fed to the computer instead. Another latch, EMA, contains some additional inputs over the other six latches. These inputs (from the error processor) keep the EMA latch reset or block it from being set whenever an error occurs. This is necessary so that the error time readout may override the error readout function commanded by EMA. This same override capability is required for the other group 4 functions, but is included in the circuits fed by the decode latches rather than in the latches themselves. These operations are explained in more detail in the portion of theory which discusses the System Data Sampler and the Internal Data Sampler.

2-108. The remaining latch in the group 4 category is the MLA latch. This latch senses the code for group 4 (same as DARO) and in addition, senses the code which commands a readout of the real time processor (discussed later). The MLA latch is used to control the System Data Sampler.

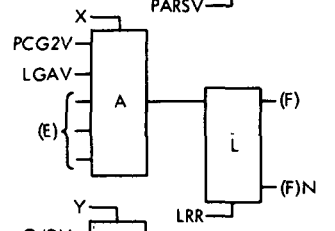
2-109. ADDRESS GROUP 5. Group 5 is identified by A1, A2 and A8 = "1". This combination is sensed by the CODG latch, figure 2-35. The specific codes allotted to group 5 are picked up by a series of decode latches which are discussed in the portion of theory for the Resolver Processor.

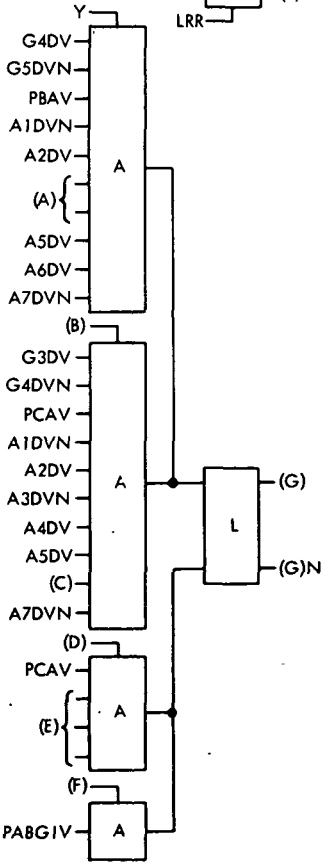






A					B	C	D
A3	A4	A5	A6	A7			
DV	DVN	DV	DV	DVN	ETTS	ETTCN	CODE
DVN	DV	DVN	DVN	DVN	-	-	DOR
DV	DV	DVN	DVN	DVN	-	-	DOS
-	DVN	DV	DVN	DVN	-	-	ICR
-	-	-	-	DV	-	-	LGA
DV	DVN	DVN	DVN	DVN	-	-	MODA
DVN	DV	DVN	DV	DVN	-	-	SSDO
DV	DV	DV	DVN	DVN	-	-	SSA

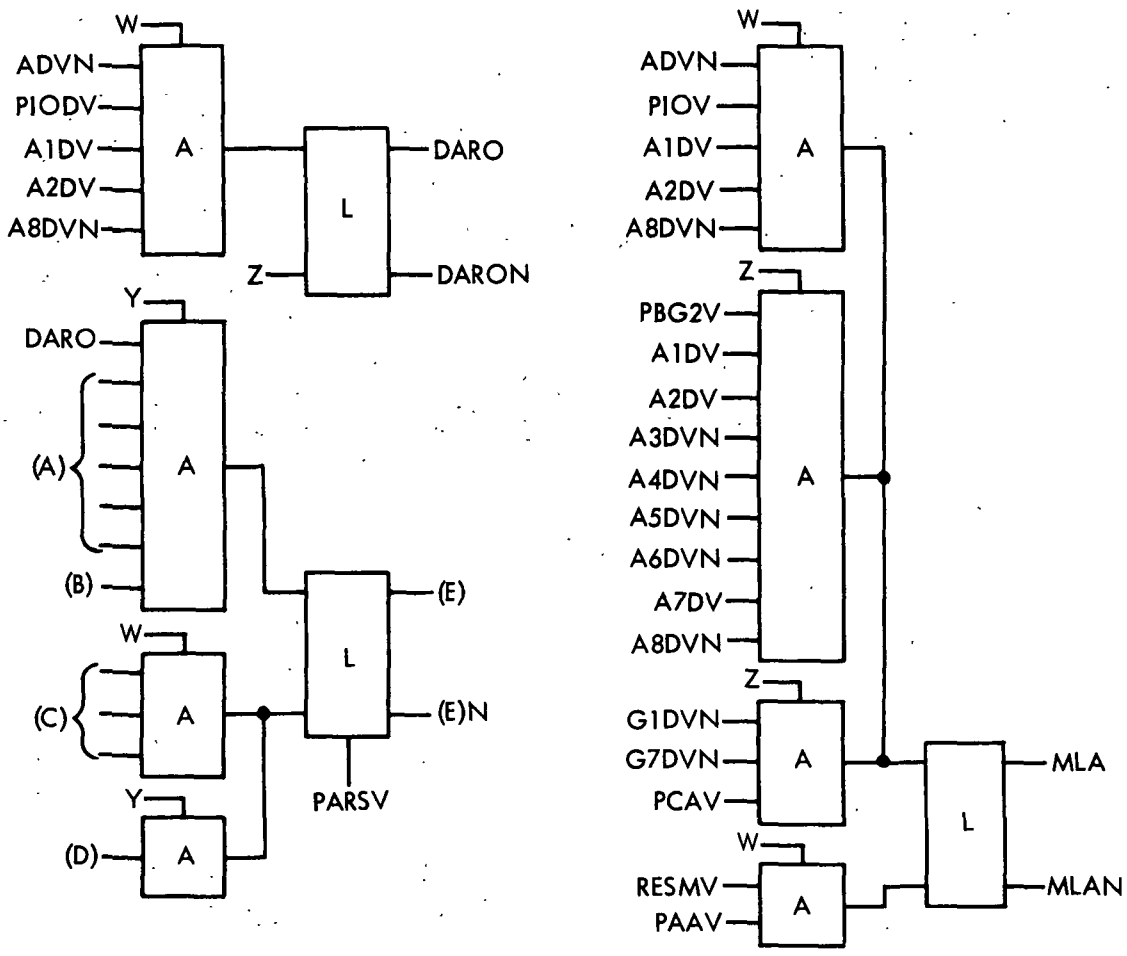




E			F
A3	A4	A5	
DV	DVN	DVN	L1A
DVN	DV	DVN	L2A
DV	DV	DVN	L3A
DVN	DVN	DV	L4A
DV	DVN	DV	L5A

A	B	C	D	E	F	G
A3DVN A4DVN	Y	A6DVN	X	G2DV G4DVN ADVN	Z	TC2A
A3DV A4DV	Z	A6DV	Y	G3DV G4DVN	Y	TC3A

Figure 2-33. Address Group 2 Decoders



A					B	C	D	E
A3	A4	A5	A6	A7				
DVN	DVN	DVN	DV	DVN	-	-	-	CRCA
DV	DV	DVN	DV	DVN	-	-	-	DIAD
DVN	DV	DVN	DV	DVN	-	-	-	DISA
DVN	DVN	DV	DVN	DVN	ETTSN	RESMV PBAV ETCC	ETTS	EMA
DV	-	-	DVN	DV	-	-	-	MBYPD
DV	DV	DV	DV	DVN	-	-	-	SSA
DV	DVN	DV	DV	DVN	-	-	-	TSA

Figure 2-34. Address Group 4 Decoders

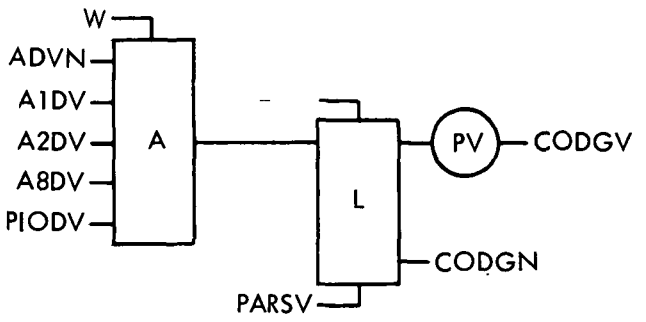


Figure 2-35. Address Group 5 Decoders

2-110. DATA CONTROL CIRCUIT.

2-111. The Data Control Circuit selects data from either the computer memory or the computer accumulator and then routes the data to a telemetry storage circuit and through a delay circuit and a select circuit to a serial line feeding telemetry and output registers. Data may also be routed from the telemetry storage circuit to the serial output. The Data Control Circuit consists of the Computer Data Select Circuit and the Computer-Telemetry Select Circuit, figure 2-36.

2-112. COMPUTER DATA SELECT CIRCUIT. The Computer Data Select Circuit consists of two latches in series, DAINF and DINF. The DAINF latch is fed by two lines from the computer, TRSV, which is essentially the accumulator output, and AI3V, which is the memory output. One of these two lines is selected to drive the DAINF latch according to the configuration of bit A8 which, as demonstrated in the discussion of Address Decode, is the bit which determines the source of data from the computer. The DINF latch produces a two-clock delay so that the computer data is available at the same time the telemetry storage data is, to the circuits following.

2-113. COMPUTER-TELEMETRY SELECT CIRCUIT. The Computer-Telemetry Select Circuit consists of a pair of latches driven in parallel by the outputs of two latches, DOMD and DINFV. The DINFV latch has already been discussed. The DOMD latch (not shown) represents the output of a telemetry storage circuit (discussed later). The latches, INFO and PCINF, are driven either by the DINF latch or the DOMD latch according to the configuration of the signal INFLAN. As previously discussed, INFLAN = "1" when group 2 is selected or when a special signal, TLM (discussed later) is a "1". Therefore, when group 2 is selected, the INFO and PCINF latches will be driven by the Computer Data Select Circuit. At all other times (except TLM), the INFO and PCINF latches will be driven by the telemetry storage latch, DOMD.

2-114. The INFO and PCINF latches are identical except that the PCINF latch is gated to operate only during phase C. This feature is provided because many of the circuits fed by the Data Control Circuit are required to operate at phase C time only. The PCINF latch eliminates the need for separate phase C gating in the circuits which it drives.

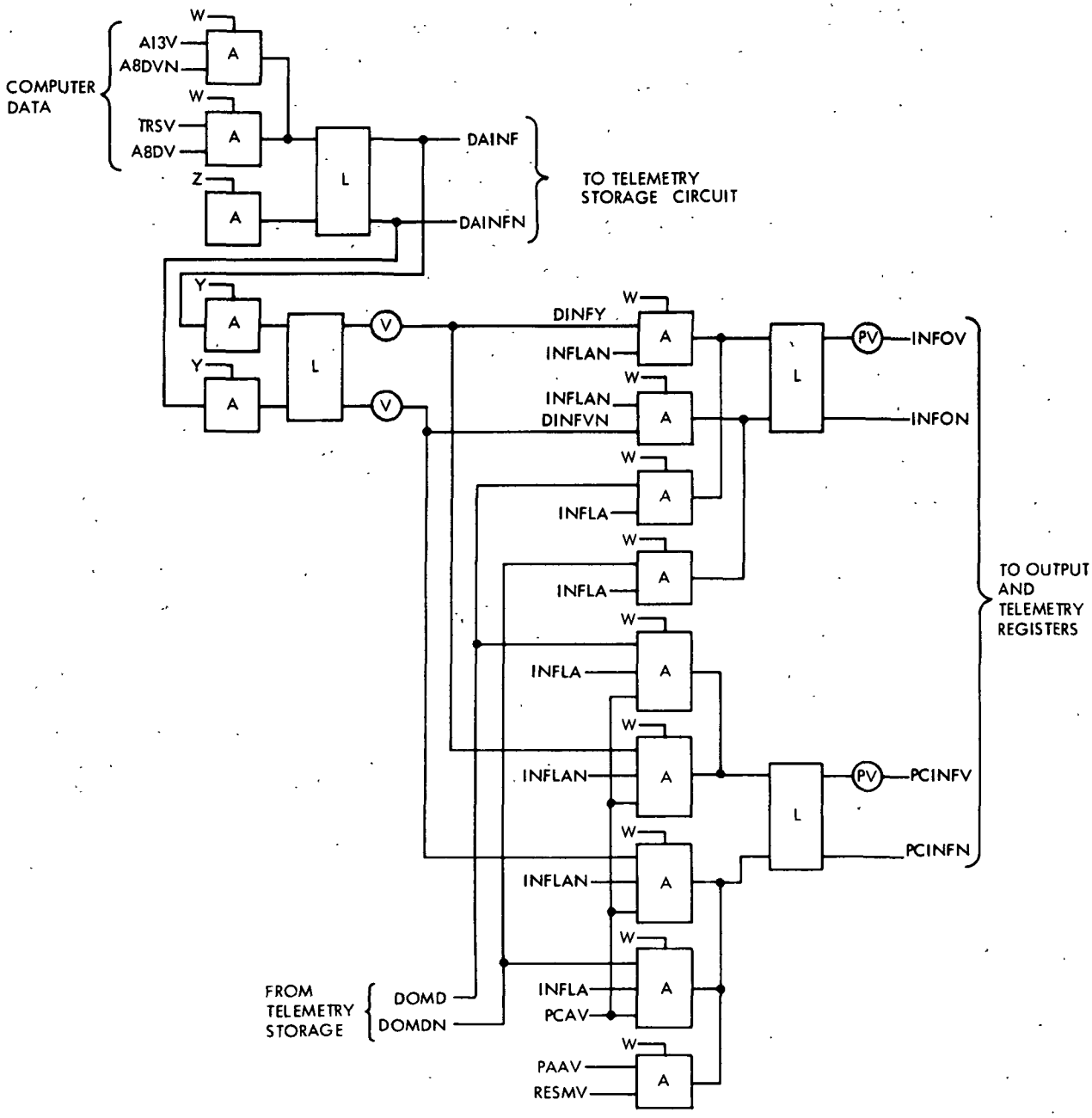


Figure 2-36. Data Control Circuit

2-115 OUTPUT REGISTERS.

2-116. Five output registers store computer data for either internal or external control. When properly conditioned, the output registers are loaded by the Data Control Circuit. The four output registers are: (1) Internal Control Register; (2) Discrete Output Register; (3) Switch Selector Register; (4) Mode Register; and (5) Ladder Register. Except for the Internal Control Register and Ladder Register, the output registers feed Signal Conditioners which adapt the register outputs to the voltage levels and power required for system use.

2-117. INTERNAL CONTROL REGISTER. The Internal Control Register is a 13-bit register with both set and reset functions individually controllable, i. e., any bit or bits may be set or reset separately. The Internal Control Register is enabled by ICRV and address bit A3. Address bit A3 selects either the set or the reset side of the register latches, figure 2-37. The register latches are loaded from bit 5 of phase B to bit 3 of phase C. This time interval is simply phase B of the computer, delayed 1 bit by the Data Control Circuit (bits 1, 2 and 3 not used).

2-118. The Internal Control Register allows the computer a certain degree of control over various data adapter circuits. A typical control would be the selection of a back-up resolver as an input to the Resolver Processor. Each of the Internal Register Control signals will be explained in the discussion of the circuit in which it is used. Bits 1 and 2 of the register are simplex. Bits 3 through 6 are duplex and bits 7 through 13 are triplex.

2-119. DISCRETE OUTPUT REGISTER. The Discrete Output Register is basically the same as the Internal Control Register in that it is a 13-bit register with selective set and reset capabilities. This register is enabled by two separate address codes: DOS, which enables the set side of the register latches, and DOR, which enables the reset side, figure 2-38. The Discrete Output Register is loaded from bit 4 of phase C to bit 2 of phase A. This time interval is phase C of the computer, delayed one bit by the Data Control Circuit (bits 1 and 2 not used).

2-120. The Discrete Output Register provides 13 separate signals for guidance and control system use. A typical signal function might be to command engine cut-off. A detailed description of signal usage is beyond the scope of this discussion. All bits of the Discrete Output Register are simplex.

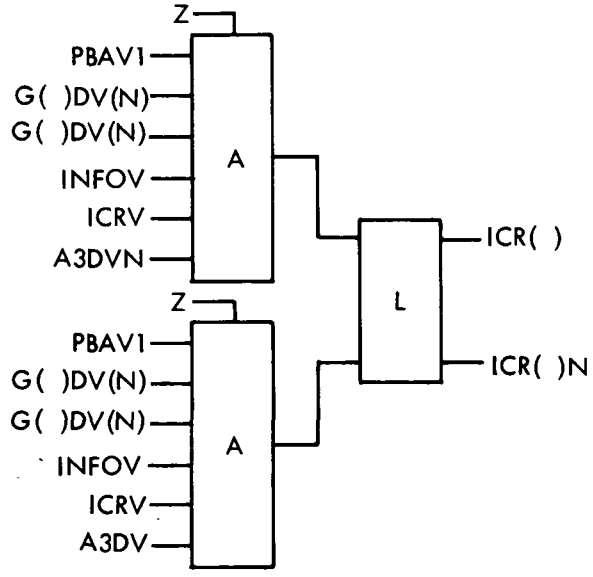


Figure 2-37. Internal Control Register, Typical Latch

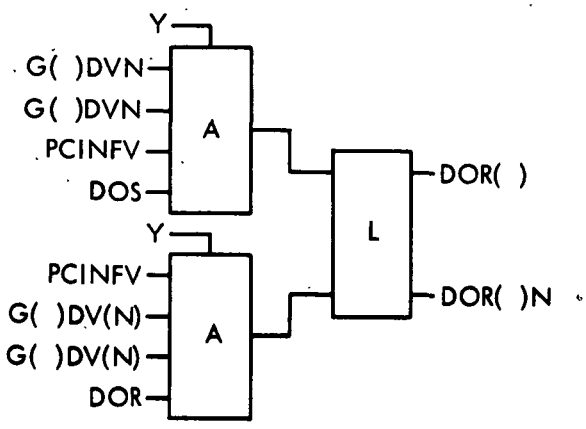


Figure 2-38. Discrete Output Register, Typical Latch

2-121. SWITCH SELECTOR REGISTER. The Switch Selector Register is a 15-bit register which is cleared at the beginning of each phase B time. The Switch Selector Register feeds four relay trees called Switch Selectors (which are external to the data adapter). Bits 1 through 8 control the pick of relays within the Switch Selectors, while bits 9 through 13 select the appropriate Switch Selector to be activated. The Switch Selector relays are bipolar; bit 14 of the register selects the direction in which the relays will be energized. When a path through a given relay tree has been established, bit 15 of the register provides a signal to command the function selected by the Switch Selector.

2-122. Whenever the Switch Selector Register is enabled by SSRV, figure 2-39, bits 1 through 13 only are loaded via the PCINFV line. The register load time extends from bit 2 of phase C to bit 2 of phase A. This time interval is phase C plus the first bit of phase A of the computer, delayed one bit by the Data Control Circuit. Only bits 1 through 13 can be loaded, since bits 14 and 15 will be programmed to be "0's" on the first pass after SSRV has been energized. Register bits 1 through 13 select a particular Switch Selector and a particular relay configuration within the Switch Selector. The Switch Selector sends back a code indicating which relays have been energized. This code is picked up by the System Data Sampler and sent to the computer. If the feedback code matches the code commanded by the computer, the computer will transmit a "1" to bit position 15 of the Switch Selector Register (upon receiving an interrupt signal generated by the Switch Selector Interrupt Processor, explained later). (The Switch Selector Interrupt Processor provides a time delay before bit 15 can be set in order to allow time for the Switch Selector relays to operate and settle down.) Bit 15 ("Read") initiates the function selected by the switch Selector.

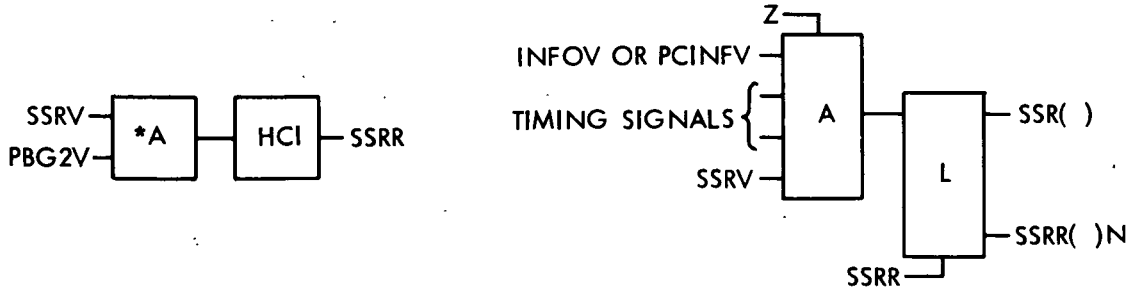


Figure 2-39. Switch Selector Register, Typical Latch

2-123. If the feedback code does not match the code commanded by the computer, the computer will transmit a "1" to bit 14 of the Switch Selector Register. This bit will reset all relays in the Switch Selector. The computer then waits for the interrupt from the Switch Selector Interrupt Processor, then issues the complement of its original code to bits 1 through 13 of the Switch Selector Register. The Switch Selector is designed to select the same function from any code or its complement, although different relays are used in each case. After the usual time delay, the computer will transmit a "1" to bit 15 to energize the function selected by the Switch Selector. The Switch Selector automatically resets its own relays a predetermined time after receiving the "Read" pulse (bit 15).

2-124. Switch Selector codes and their functions are beyond the scope of this discussion. Bits 1 through 8 of the register are simplex; bits 9 through 15 are triplex.

2-125. MODE REGISTER. The Mode Register, figure 2-40, is a 6-bit register which is cleared at the beginning of every phase B time and is loaded from bit 11 of phase C to bit 2 of phase A, a one-bit delay of the computer data (bits 1 through 9 not used).

2-126. The output of the Mode Register is a code representing the computer operational mode, such as Flight Program, Load and Verify, etc. Actual codes and definitions are beyond the scope of this discussion.

2-127. SIGNAL CONDITIONERS. Signal Conditioners are used to switch the logic levels from 0V and +6V to 0V and +28V for driving relays or other circuits returned to the +28V return.

2-128. There are two types of drivers, simplex (SD) and TMR (TD). In the data adapter, the simplex drivers consist of a low-current driver (SDL) and a high-current driver (SDH). The TMR drivers consist of a low-current driver (TDL), a medium-current driver (TDM) and a high-current driver (TDH).

2-129. Both the simplex and TMR drivers must be driven by intermediate drivers (ID). The simplex drivers are driven by low-current intermediate drivers (IDL) and the TMR drivers are driven by high-current intermediate drivers (IDH).

2-130. The TMR drivers are fed by triplicated circuits (actual or simulated) and they act as voters, their outputs being the level-shifted function of the majority input. All of the drivers, simplex, duplex and intermediate, provide logical inversion. The appropriate Signal Conditioners and their output signal names are as follows:

Register Output	Intermediate Driver	Int. Driver Output	Signal Conditioner	Signal Conditioner Output
SSR 1 thru 8	IDL	SSR 1H thru 8H	SDH	SS 1 thru 8
SSR 9 thru 13	IDH	SSR 9H thru 13H	TDM	SS 9 thru 13
SSR 14 thru 15	IDH	SSR 14H thru 15H	TDH	SS 14 thru 15
DOR 1 thru 2	IDL	DOR 1H thru 2H	TDL	DO 1 thru 2
DOR 3 thru 13	IDH	DOR 3H thru 13H	TDM	DO 3 thru 13
MODR 1	IDL	MODR H1	SDL	MOD 1
MODR 2 thru 3	IDL	MODR 2H thru 3H	SDH	MOD 2 thru 3
MODR 4 thru 6	IDL	MODR 4H thru 6H	SDL	MOD 4 thru 6

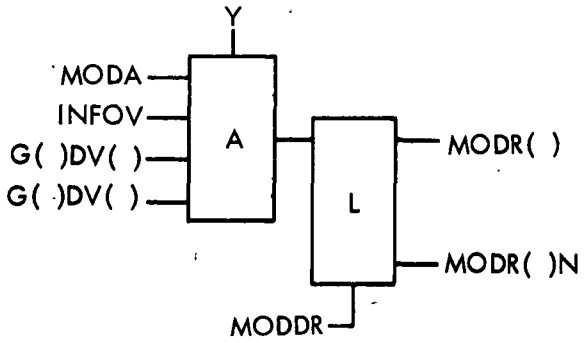


Figure 2-40. Mode Register, Typical Latch

2-131. Since the discrete output register is supplied only in simplex form, special arrangements are provided to make the TDM drivers for bits 3 through 13 operable. The special arrangements consist of a wiring-only page assembly which "straps" "0's" into one of each of the discrete output TDM or TDL circuits. (Note: at the input of the TDM circuits, a +6 v level is interpreted as "0".) One of the two remaining inputs of each TDM or TDL circuit is left open to simulate a "1", thus producing a tie vote. The final input of each TDM or TDL circuit is driven by the discrete output register through an IDL circuit to break the tie.

2-132. The outputs of the two discrete output TDL circuits are fed to special isolating simplex drivers (SDI). The SDI circuit provides no signal inversion.

2-133. LADDER REGISTER. The Ladder Register is a 9-bit register which is cleared at the beginning of each phase B time. The Ladder Register is loaded from bit 5 to bit 13 of phase B, a one-bit delay of the computer data (bits 1 to 3 not used). (See figure 2-41.) The output of the Ladder Register represents attitude control data generated by the computer. This data is converted to analog signals by the Digital-to-Analog Converter for guidance and control system use.

2-134. DIGITAL-TO-ANALOG (D/A) CONVERTER.

2-135. The Digital-to-Analog Converter, figure 2-42, converts digital computer data into analog voltages scaled for use by attitude control devices within the vehicle. The D/A converter produces five analog voltages for external use. Three govern attitude (pitch, roll, yaw) of the vehicle and two are spares. Each analog voltage output is fed to telemetry through a telemetry buffer circuit.

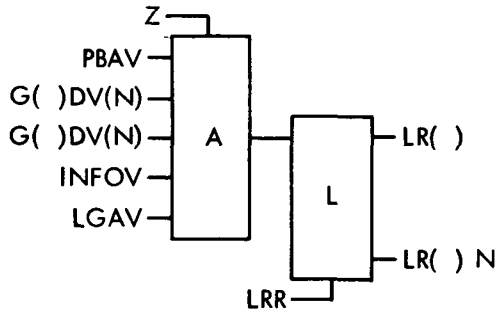


Figure 2-41. Ladder Register, Typical Latch

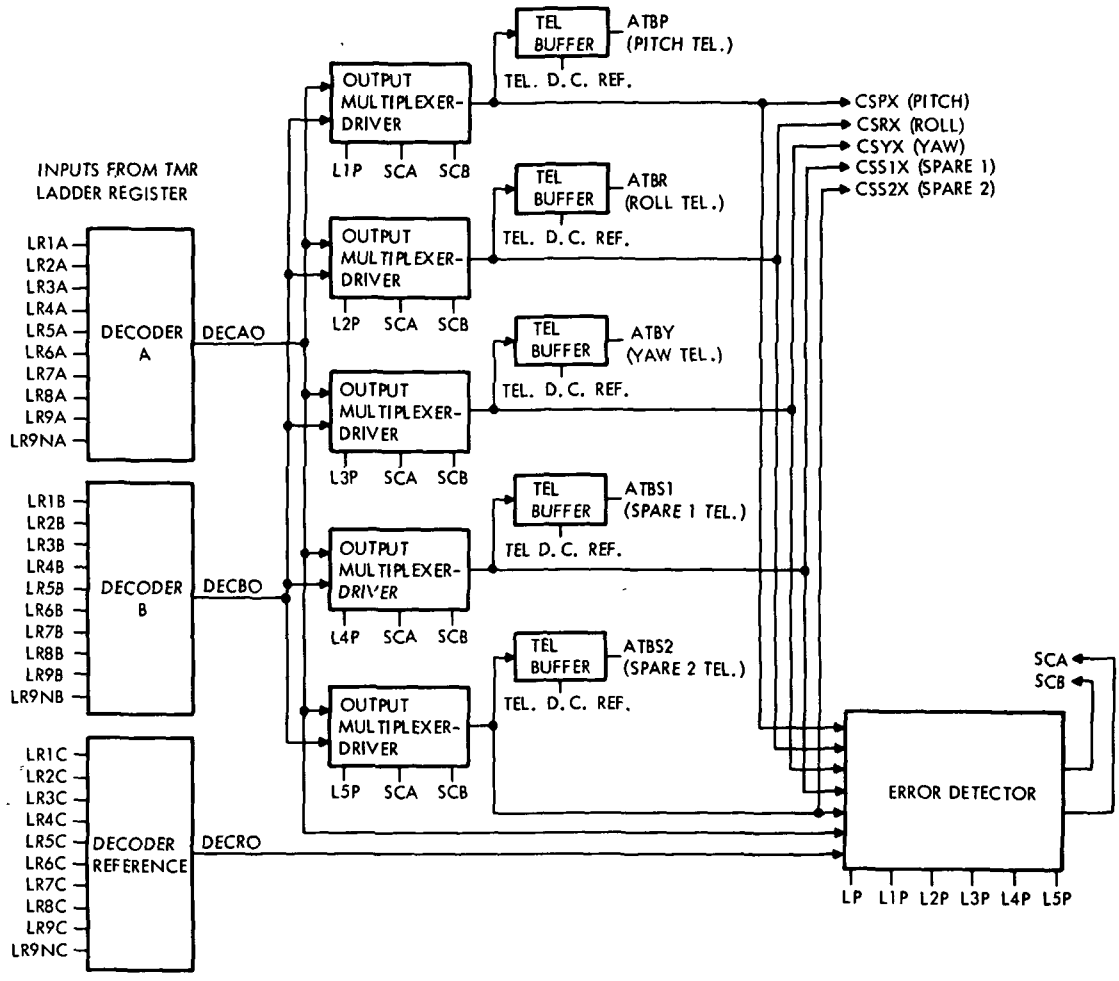


Figure 2-42. Digital-To-Analog Converter

2-136. The D/A converter contains three decoders which convert the computer data stored in the ladder register into analog voltages. Since the one ladder register stores data for each of the five converter outputs, the outputs of the decoders are channeled to appropriate converter outputs by output multiplexer-drivers. Only one of the decoder outputs (DECAO or DECBO) is selected (by the error detector) to be processed by the selected output-multiplexer-driver. The error detector compares the reference decoder output with the A decoder output and also with the output of the selected output-multiplexer-driver. If the comparisons are within proper tolerances, the normally selected A decoder (SCA) remains selected; if invalid comparisons occur, the error detector selects the B decoder (SCB). Once the error detector selects the B decoder it remains selected until the computer commands the selection of the A decoder.

2-137. DECODER. (See figure 2-43.) Each decoder converts 9-bits of incoming digitial data from the ladder register into comparable analog voltages. The polarity of the output voltages is determined by bit 9 (LR9) of the ladder register; when LR9 equals "1", the decoder produces a negative voltage, and vice-versa. The decoder provides a maximum of 256 voltage increments, either positive or negative, as determined by LR1 through LR8. The decoder output is scaled to 24 MV per binary digit and has a range of ±6. 12 volts.

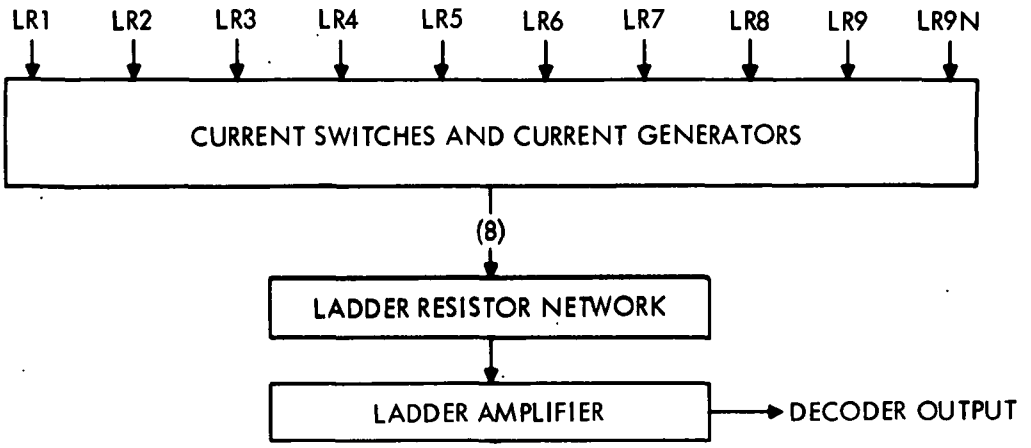


Figure 2-43. Ladder Decoder

2-138. The decoder consists of a matrix of current switching and generating circuits feeding an eight-input ladder resistor network coupled to a ladder amplifier. The current switching circuits consist of eight positive (PCS) and eight negative current (NCS) switches, eight positive (PCG) and eight negative (NCG) current gates, one positive voltage reference (PVR), and one negative voltage reference (NVR). The ladder resistor network produces an analog voltage scaled to 6 MV per binary digit and with a range of ±1.53 volts. The output of the ladder resistor network is amplified four times by the ladder amplifier to provide a maximum decoder output of 6.12 volts. Each digital input to the decoder is decoded in the same manner, consequently the decoding operation for just one bit is defined.

2-139. A typical current switching circuit to decode one digit is shown on figure 2-44. The PCS, NCS, PCG, and NCG circuits shown are unique to bit 5; however, the PVR and NVR circuits are common to all bit positions. Each digital input is ANDed (at a PCS and at an NCS circuit) with bit 9 to determine the polarity of the decoder output voltage. If either or both inputs to a PCS or NCS circuit are "0's", the circuit diverts the output current of the associated PCG or NCG circuit from its load. Two "1" inputs to either a PCS or NCS circuit cause the circuit to act as an open circuit thus permitting current flow through its associated PCG or NCG circuit. The PCG and NCG circuits supply a positive or negative current to one of the L-pads of the ladder resistor network. Each L-pad halves the current from the associated PCG or NCG. The ladder resistor network output is amplified four times by the ladder amplifier prior to being supplied as a decoder output.

2-140. OUTPUT MULTIPLEXER-DRIVER. (See figure 2-45.) Each individual output multiplexer-driver, when enabled by control signals, samples and stores decoder output voltages; then amplifies either decoder A or B voltages as selected by the error detector. The output multiplexer-driver contains hold capacitors which store decoder analog voltages for a maximum of 40 MS to provide a continuous output after the decoder voltages are removed. Consequently the output multiplexer-driver must be conditioned to charge the hold capacitor at intervals not exceeding 40 MS to maintain a correct output voltage.

2-141. The two bipolar electronic switches (BES) of an output multiplexer-driver couple the decoder output voltages to the associated hold capacitors and ladder amplifiers (LDA) when enabled by signals L1 through L5 PA or PB as necessary. Signals L1

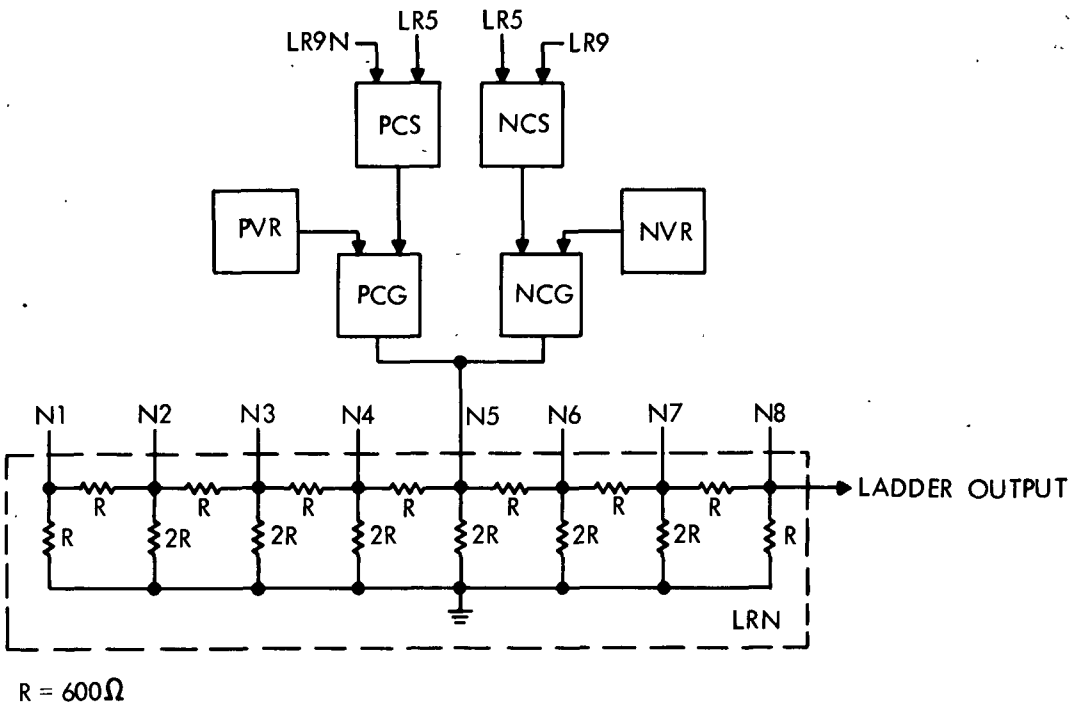


Figure 2-44. Current Switching Circuit

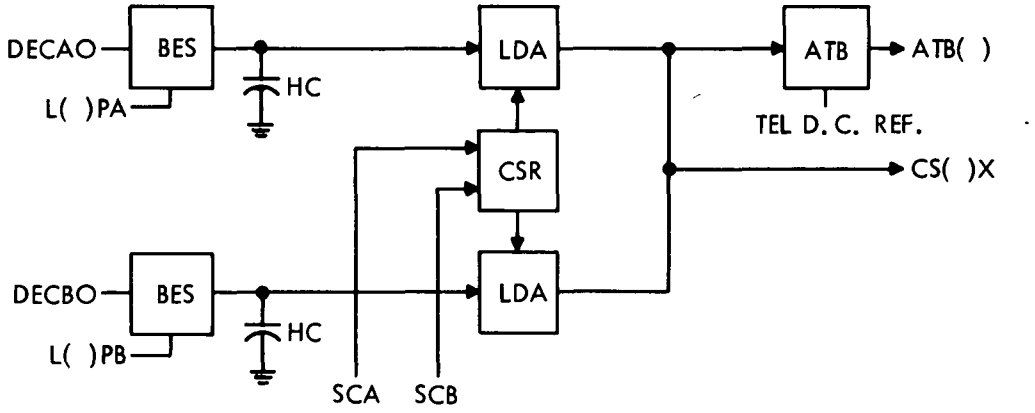


Figure 2-45. Output Multiplexer-Driver

through L5 PA and PB consist of 500 kc pulses which are initiated by the address decoder. During the up half cycles (+ 6V) of the 500 KC pulses, the hold capacitor samples the decoder output voltage. During the down half cycles (0V) of the 500 KC pulses the hold capacitor maintains the sampled voltage. The hold-capacitor voltages are applied to the LDA circuits, one of which is enabled by the converter select (CSR) circuit. The LDA amplifies the hold-capacitor voltage two times prior to supplying the amplified voltage as a D/A converter output. The CSR selects either the outputs of decoder A or B to be amplified when either SCA or SCB, respectively, equals "1". The CSR provides +20 volts to the selected LDA to enable the LDA to function. The analog telemetry buffer converts the output voltage to a level compatible with telemetry equipment.

2-142. ERROR DETECTOR. (See figure 2-46.) The error detector compares the reference decoder output with the A decoder output and also with the output of the selected output multiplexer-driver. The error detector allows the normally provided A decoder select signal (SCA) to remain if comparisons are within ±37 MV; the decoder provides a B decoder select signal (SCB) when one or both comparisons are not within tolerance. Once the error detector selects the B decoder it remains selected until the computer, under program control, commands the selection of the A decoder.

2-143. The error detector consists of a single latch and two comparators (CPR) with associated inverters and bipolar electronic switches (BES). Whenever the two inputs to a comparator are within ±37 MV of each other, the comparator produces a "1" output which is inverted to inhibit the latch from selecting decoder B. A "0" output from a comparator will enable the latch to be set to select decoder B (providing control signal LRPP equals "1"). The reference decoder and A decoder outputs are continuously compared; whereas, the selected output multiplexer-driver and the reference decoder outputs are compared when enabled by 500 KC pulses from the control circuit. Since the output multiplexer-driver signals are twice the amplitude of the reference signals the multiplexer inputs are halved at the BES circuits to enable a comparison at the CPR. The latch is conditioned to select decoder A when the internal control register is selected to be set and PCINFV contains a "1" at C-4 time.

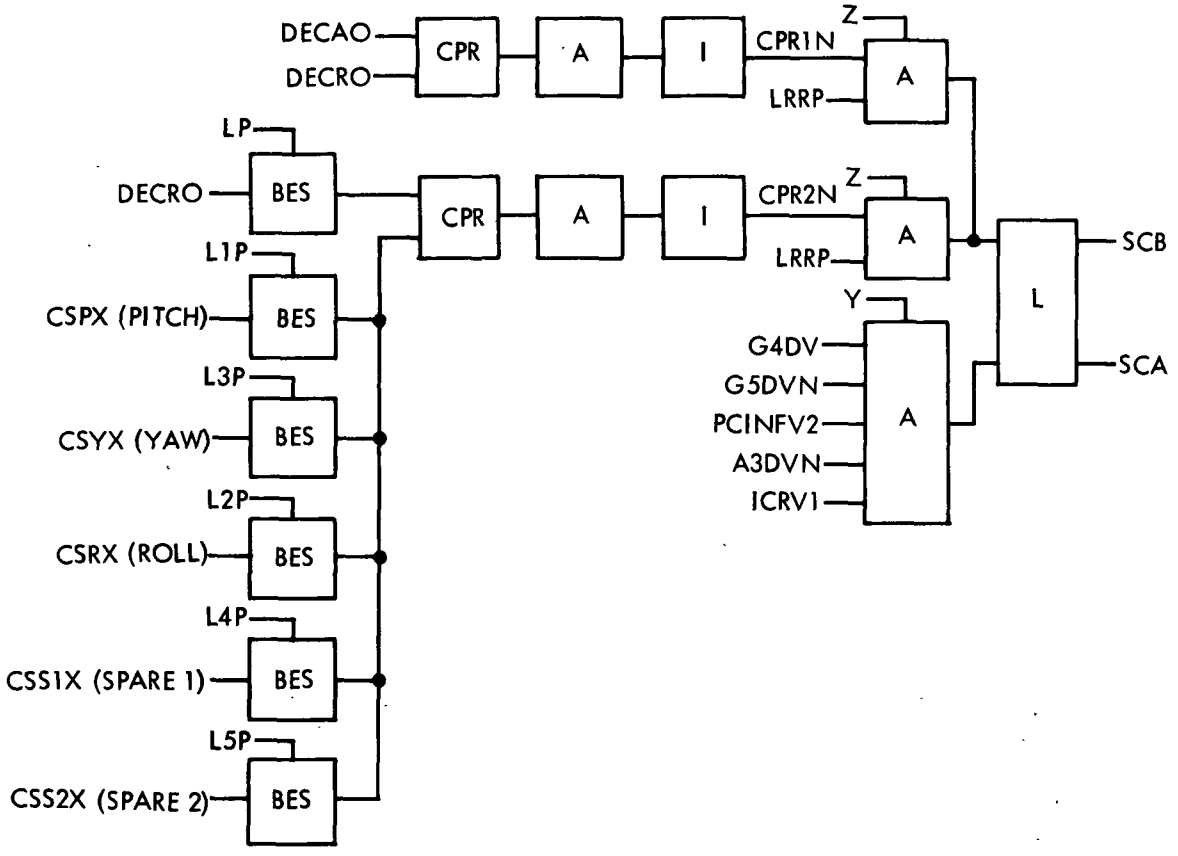


Figure 2-46. Error Detector

2-144. CONTROL CIRCUITS. (See figure 2-47.) The control circuits, under address decoder control, select the appropriate multiplexer and enable the error detector to sample the decoder outputs. The control circuits inhibit the multiplexers and the error detector from sampling the decoder outputs while the ladder register is reloaded and to allow ample time for the ladder amplifiers to settle.

2-145. The control circuits consist of two latches (500 KC and LRRP) and six AND-inverter circuits. The 500 KC latch complements at a 500 KC rate. The LRRP latch is reset by LRR from the address decoder whenever data is loaded into the ladder register. As the ladder register is loaded, a delay count of 10_8 is also loaded into channel 3 of the Telemetry Operation delay line. The delay count while circulating through the delay line is reduced until it reaches zero; then C3RD will equal "1" to enable LRRP to set at A-7-W time. The LRRP latch is utilized by the error detector and conditions the AND-inverter circuits. When LRRP equals "1" the LP and one of the L1-5P signals, selected by the address decoder, equal "1" during the down half cycles of the 500 KC signal.

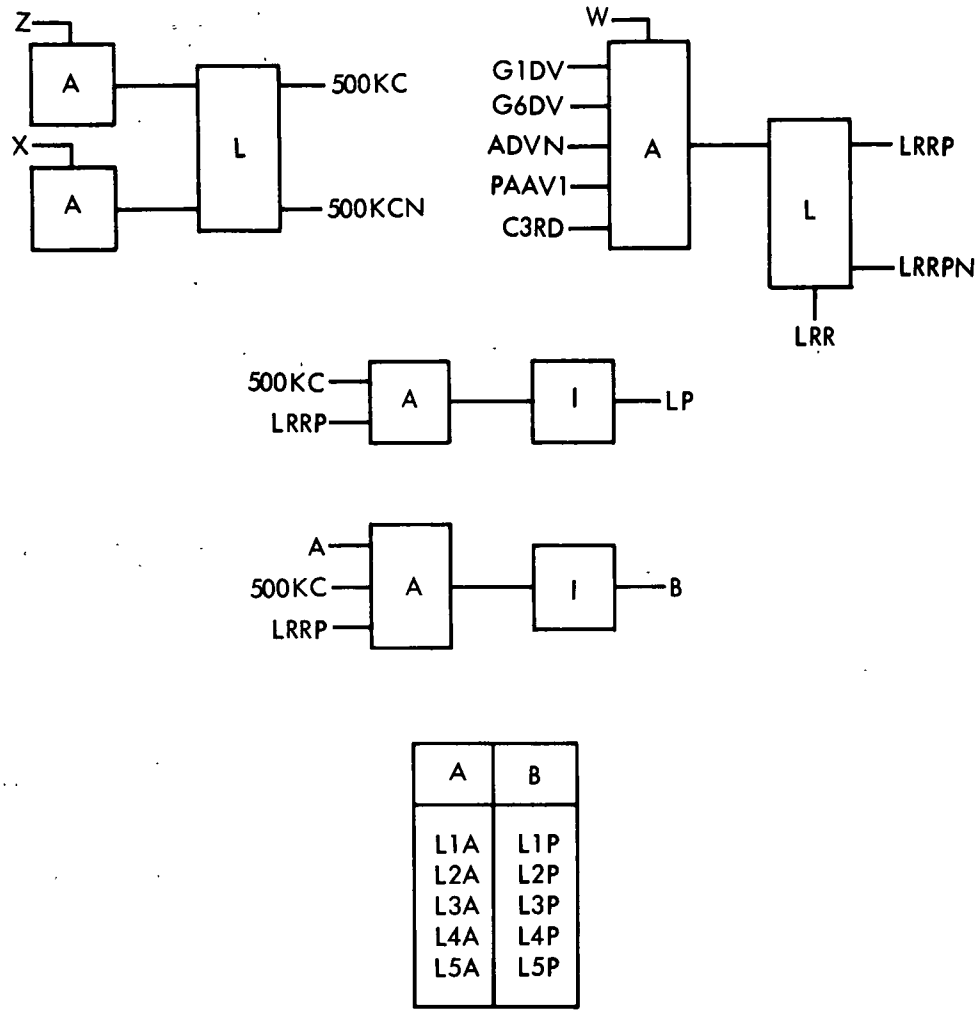
2-146. INTERNAL DATA SAMPLER.

2-147. The Internal Data Sampler (figure 2-48) multiplexes and serializes selected signals generated within the computer and the data adapter for telemetering. Data adapter address decoder output signals select one of five groups of internal signals to be multiplexed, serialized, and fed to Telemetry Storage. The five groups of signals available for selection are (1) crossover detector (CES) error signals, (2) error monitor (EM) signals, (3) internal control register (ICR) signals, (4) ladder register address (LGA) signals, (5) switch selector (SS), and discrete output (DO) signals. In addition, the Internal Data Sampler supplies serialized data (error monitor data) to the System Data Sampler which accepts the data when enabled by the address decoder.

2-148. The Internal Data Sampler consists of a primary multiplexer-serializer, a secondary multiplexer, and a secondary serializer-selector (figure 2-48). The primary multiplexer-serializer merges and serializes data whenever conditioned by the address decoder. The secondary multiplexer merges error time signals when commanded by the error processor. The secondary serializer-selector serializes the secondary multiplexer data if commanded by the error processor; otherwise it duplicates the primary multiplexer serializer output.

2-149. PRIMARY MULTIPLEXER-SERIALIZER. The Primary Multiplexer-Serializer consists of a 13-bit register (multiplexer) and a serializer latch (DOMS). The multiplexer accepts data under three different conditions: data from the computer program instruction counter is accepted via the DINFVN line during phase A time, error time signals are loaded when conditioned by the error processor, and various signals (selected by the address decoder) are loaded during phase B and C times. During non-error periods, the multiplexer stores data for approximately one phase duration. Then, since an error has not occurred (ETCRN = "1"), RESMV will clear the register at 2-W time of each phase time.

2-150. When an error is sensed by the error processor, ETTS equals "1" for approximately one bit time to set latches DM1-2 and DM11A through DM14A prior to loading error time signals. The error processor then prevents further data from being loaded into these latches. Address decoder codes SSDO, EMA, and CODE are inhibited and ETCCN equals "0" to inhibit internal control register signals (ICRIN, 11N, 12N, and 13N) and ladder register address signals (A3DV - A5DV). While ETCCN equals "0", it also prevents latches DM1-2, and DM11A through DM14A from setting thus storing the error time signals until they are sampled by the primary serializer. If an error is sensed during phase A time, ETCRN equals "0" during the following three phase times



A	B
L1A	L1P
L2A	L2P
L3A	L3P
L4A	L4P
L5A	L5P

Figure 2-47. D/A Converter Control

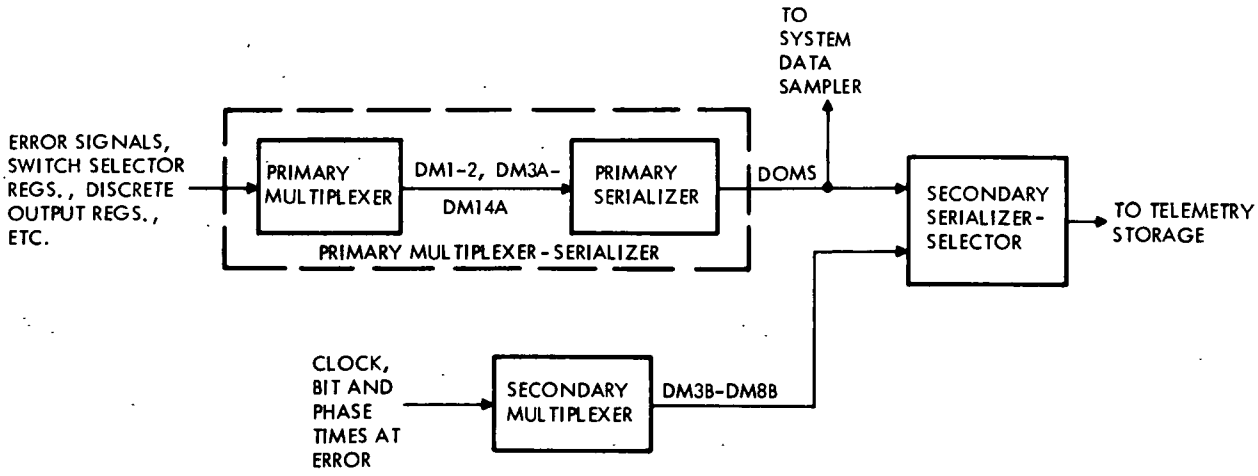


Figure 2-48. Internal Data Sampler

to prevent setting latches DM3A through DM10A. If an error is sensed during non-phase A times, ETCRN will not become a "0" until B-1-X time of the following computer cycle so that the primary multiplexer can be cleared prior to loading instruction counter data during phase A time. After ETCRN equals "0", it remains "0" until the following A-14 bit time preventing latches DM3A through DM10A from being set during this period.

2-151. Figure 2-49 shows a typical multiplexer latch with typical gate-inverter inputs. A table of inputs and associated conditioning signals is shown in figure 2-50. Note that signals CES14, SS13 and EM13 appear out of sequence when stored in latch DM1-2; however, the primary serializer will assemble these bits into their proper sequence.

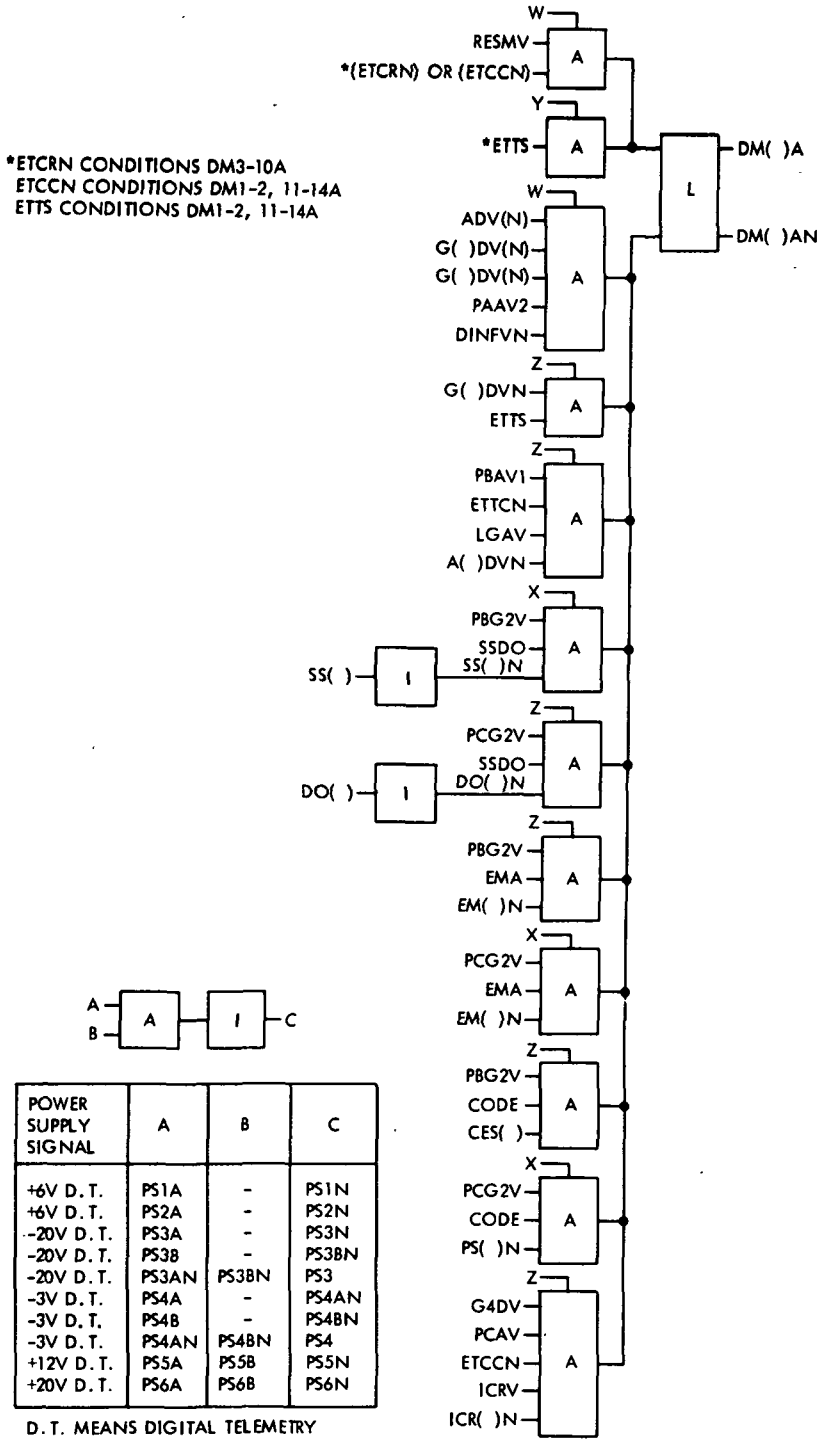
2-152. The primary serializer (DOMS, figure 2-51) serializes the contents of the primary multiplexer each phase time; the output of the DOMS latch is utilized by the secondary serializer-selector only during phase B and C times. The DOMS latch output is also utilized by the System Data Sampler during phase B and C times when enabled by the address decoder.

2-153. Computer instruction-counter data stored in the primary multiplexer is fed to the secondary serializer-selector only if an error occurs. Normally, the instruction-counter data is cleared from the multiplexer at B-2-W time. However, when an error occurs, ETCRN equals "0" to prevent clearing of the instruction counter data at B-2-W time. Consequently, the instruction counter is loaded into the DOMS latch during the following phase B time.

2-154. The DOMS latch sequentially loads the multiplexer outputs as shown in figure 2-52; then resets at each Z clock time. Note that DM1-2 data is loaded into DOMS at bit times C-1 and C-2 since the DM1-2 latch contains data bits 13 and 14 at these times. (Refer to figure 2-50.) During normal operation, the DOMS serialized output, as mentioned previously, is utilized by the secondary serializer-selector during phase B and C times. However, when an error occurs the DOMS output is ignored after C-1 time; the secondary selector-serializer then accepts data from the secondary multiplexer.

2-155. SECONDARY MULTIPLEXER. (Figure 2-53.) The Secondary Multiplexer, a 7-bit register, stores error timing signals until a subsequent error occurs. Whenever an error occurs, ETTS, generated at the error processor, will equal "1" for approximately one bit time to condition the multiplexer to first reset, then to store error timing signals. The error timing signals stored in the secondary multiplexer (figure 2-53) together with the error timing signals stored in the primary multiplexer indicate the time the error was sensed. The secondary multiplexer output is serialized by the secondary serializer-selector.

2-156. SECONDARY SERIALIZER-SELECTOR. (Figure 2-54.) The Secondary Serializer-Selector (DSD latch) normally duplicates the primary serializer (DOMS) at each Y clock time of phase B and C times. When errors occur, DSD continues to accept data from DOMS through bit C-1 time; then ETCR will equal "1" from B-1-X through A-14-Y time to inhibit loading DOMS and enable loading data from the secondary multiplexer. The DSD latch sequentially loads secondary multiplexer data during phase C time as shown in figure 2-54; the DSD latch is reset at every X clock time. The secondary serializer-selector feeds Telemetry Storage.



POWER SUPPLY SIGNAL	A	B	C
+6V D.T.	PS1A	-	PS1N
+6V D.T.	PS2A	-	PS2N
-20V D.T.	PS3A	-	PS3N
-20V D.T.	PS3B	-	PS3BN
-20V D.T.	PS3AN	PS3BN	PS3
-3V D.T.	PS4A	-	PS4AN
-3V D.T.	PS4B	-	PS4BN
-3V D.T.	PS4AN	PS4BN	PS4
+12V D.T.	PS5A	PS5B	PS5N
+20V D.T.	PS6A	PS6B	PS6N

D.T. MEANS DIGITAL TELEMETRY

Figure 2-49. Typical Primary Multiplexer Latch

			LGAV	SSDO		EMA		CODE			ICRV			
LATCH	DINFVN PAAV-W	ETTS-Z	ETCCN PBAV-Z	PBG2V-X	PCG2V-X	PBG2V-Z	PCG2V-X	PBG2V-Z	PCG2V-W	PCG2V-X	PCAV-Z	PCAV-Z ETCCN G4DV	PCG2V-W ETCCN	PCG2V-X ETCCN
DM1-2		G5DVN		SS13	DO1(W)	EM13N	EM14N(W)	CES13	CES14				ICR1N	
DM3A	IC-1			SS1	DO2	EM1N	EM15N	CES1		PS1N				
DM4A	IC-2			SS2	DO3	EM2N	EM16N	CES2		PS2N	ICR2N			
DM5A	IC-3			SS3	DO4	EM3N	EM17N	CES3		CES15	ICR3N			
DM6A	IC-4			SS4	DO5	EM4N	EM18N	CES4		CES16	ICR4N			
DM7A	IC-5			SS5	DO6	EM5N	EM19N	CES5		PS3	ICR5N			
DM8A	IC-6			SS6	DO7	EM6N	EM20N	CES6		PS4	ICR6N			
DM9A	IC-7			SS7	DO8	EM7N	EM21N	CES7		CES17	ICR7N			
DM10A	IC-8			SS8	DO9	EM8N	EM22N	CES8		CES18	ICR8N			
DM11A		G1DVN		SS9	DO10	EM9N	EM23N	CES9		PS5N	ICR9N			ICR10N
DM12A		G2DVN	A3DVN	SS10	DO11	EM10N	EM24N	CES10		CES19		ICR11N		
DM13A		G3DVN	A4DVN	SS11	DO12	EM11N	EM25N	CES11		PS6N		ICR12N		
DM14A		G4DVN	A5DVN	SS12	DO13	EM12N	EM26N	CES12				ICR13N		

CES( ) - Crossover Detector Error
CODE - Crossover Detector Address
DINFV - Computer Accumulator Data Delayed
DO( ) - Discrete Output Register
EM( ) - Error Monitor
EMA - Error Monitor Address
IC( ) - Instruction Counter
ICR( ) - Internal Control Register
ICRV - Internal Control Register Address
SS( ) - Switch Selector
SSDO - Switch Sector-Discrete Output Address
PS( ) - Power Supply

Figure 2-50. Table of Primary Multiplexer Inputs

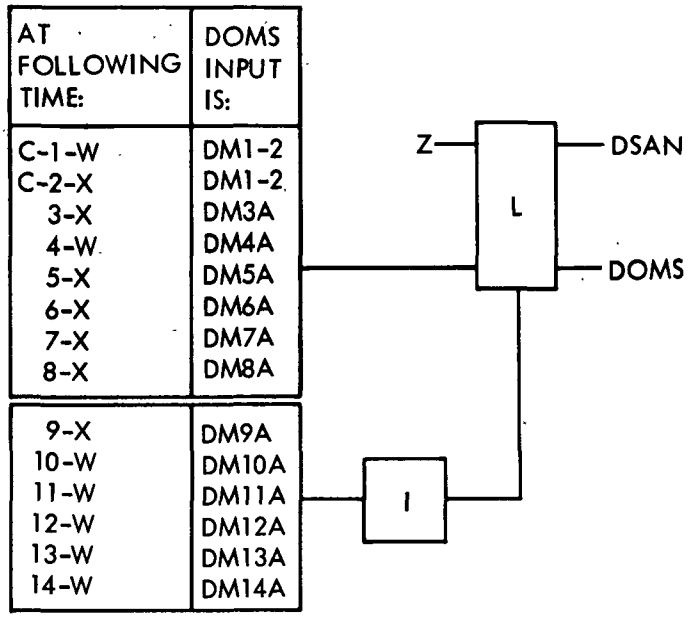


Figure 2-51. Primary Serializer

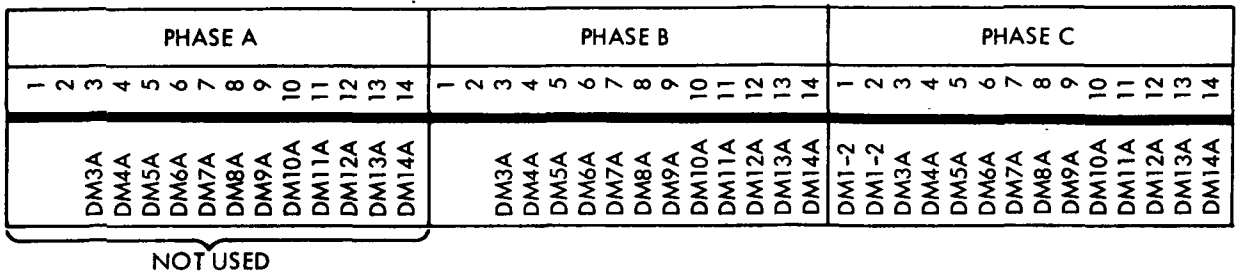
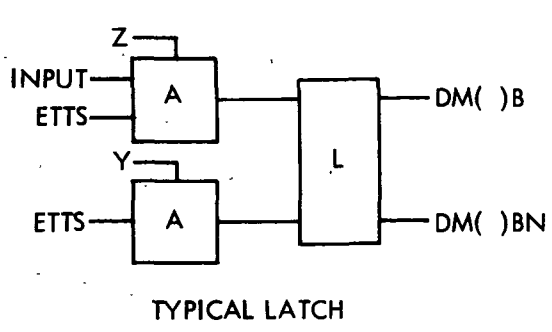


Figure 2-52. Primary Serializer Output Format



LATCH	INPUT
DM2B	G6DV
DM3B	G7DV
DM4B	ECSA
DM5B	ECSB
DM6B	PAAV
DM7B	PBAV
DM8B	PCAV

Figure 2-53. Secondary Multiplexer

AT FOLLOW-ING TIME:	(ETCRN = 1) DSD INPUT IS:	(ETCR = 1) DSD INPUT IS:
PHASE B, EVERY Y CLOCK TIME	DOMS	DOMS
PHASE C, EVERY Y CLOCK TIME	DOMS	-
C-1-Y	-	DOMS
C-2-Y	-	DM2B
C-3-Y	-	DM3B
C-4-Z	-	DM4B
C-5-Z	-	DM5B
C-6-Z	-	DM6B
C-7-Z	-	DM7B
C-8-Z	-	DM8B

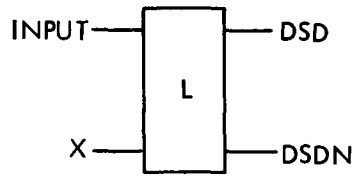


Figure 2-54. Secondary Serializer - Selector

2-157. SYSTEM DATA SAMPLER.

2-158. The System Data Sampler (figure 2-55) selects system signals for telemetry and computer usage. The system signal may be either parallel data (discrete system signals) or serial data derived from processors or from the Internal Data Sampler (error data). The System Data Sampler serialized output (DATAV) is fed to both telemetry storage and the computer. The System Data Sampler consists of a multiplexer and a serializer-selector.

2-159. MULTIPLEXER. (See figure 2-56.) The Multiplexer is a 13-bit register which is completely set at the beginning of phase A. All data is gated into the reset side of the register. All incoming data is complementary data, inverted in the process of coming through level-shifters or power restoring circuits (figure 2-57). (An exception is real-time data, available on C4RDN; this data is not level-shifted, but is provided in complementary form to be compatible with the system signals.) If the system signals are considered as being inputs to the Multiplexer latches prior to being inverted, a "1" level on a system signal will therefore not reset the latch. It is convenient to assume this as being equivalent to having the system signal set the latch, keeping in mind that the latch operation is actually reversed from the normal concept.

2-160. The Multiplexer inputs (prior to level shifting and inversion) are shown in figure 2-58. As demonstrated by this figure, real time data (C4RDN) is loaded into the Multiplexer during phase A, whereas the system signals are loaded during phases B and C. Although the data shown in figure 2-58 appears out of sequence, the serializer-selector will reassemble it into its proper order.

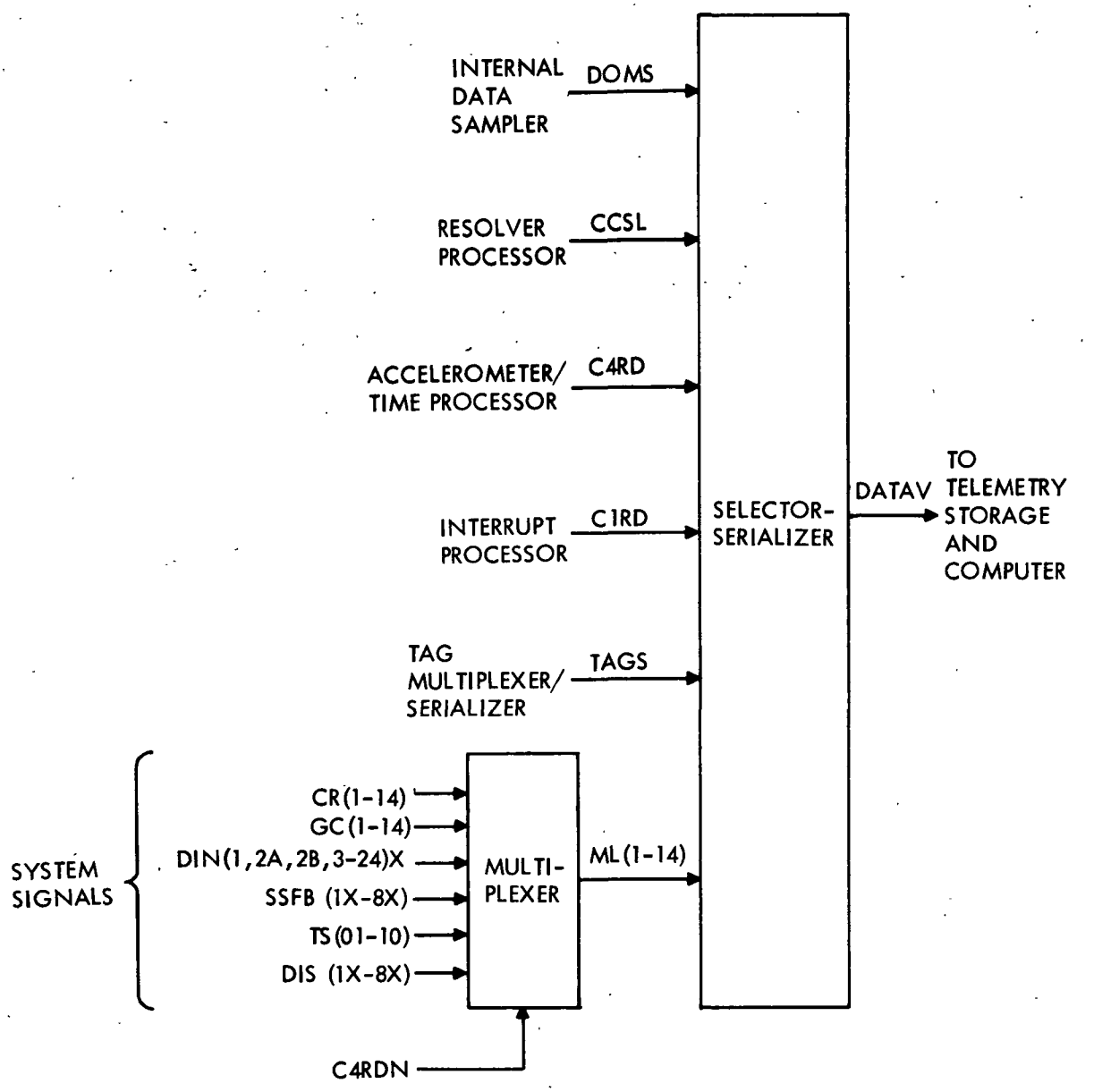


Figure 2-55. System Data Sampler

2-161. SERIALIZER-SELECTOR. The Serializer-Selector serializes or duplicates signals from six sources either automatically or under address decoder control. When enabled by the address decoder, the serializer-selector serializes parallel signals from the multiplexer during phases B and C. The serializer-selector duplicates serial signals from the tag serializer unconditionally during phase A; serial signals from the remaining three sources are duplicated during phases B and C but are selected under address decoder control.

2-162. The serializer-selector, a multiple-input latch, is loaded at Y clock times and reset at X clock times. Figure 2-59 shows serializer-selector inputs and address decoder conditioning signals. Note that when MBYPD equals "1", address decoder bits A4 and A5 enable loading accelerometer data as indicated. Figure 2-60 shows the serializer-selector output format while multiplexer inputs are selected. Note that the ML1-2 latch is loaded into the serializer-selector at bit times B-1, B-2, C-1, and C-2.

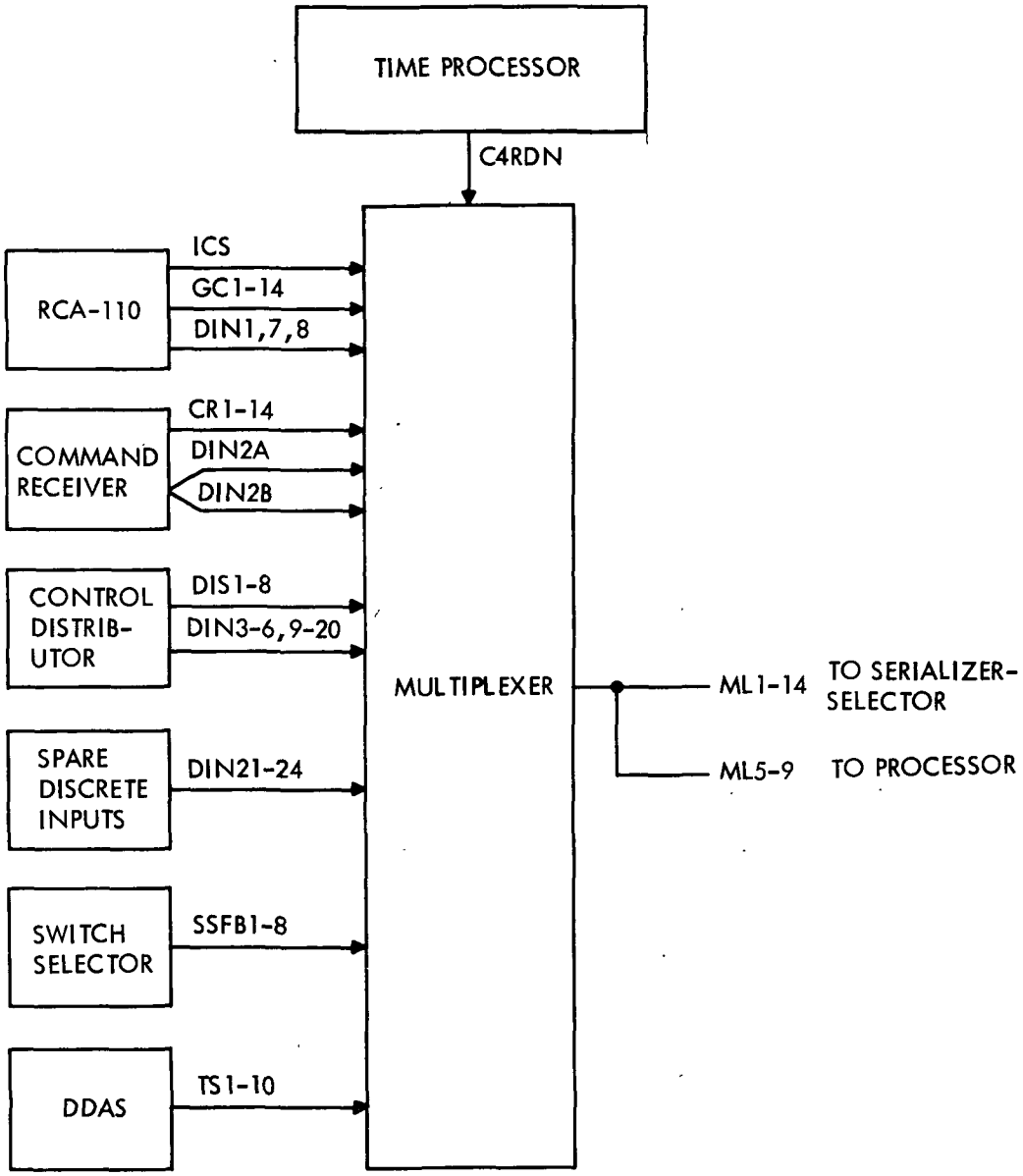


Figure 2-56. Multiplexer

However, the ML1-2 latch is cleared and reloaded between B-1-Y and B-2-Y times and between C-1-Y and C-2-Y times so that consecutive data bits are serialized. (Refer to figure 2-58.)

2-163. PROCESSORS.

2-164. GENERAL.

2-165. Most of the data adapter operations are confined to simple level-shifting of input signals or multiplexing of data. Some input signals, however, must be more drastically modified for use by the computer, other guidance system equipments, or by the data adapter itself. It is the function of the data adapter Processors to modify such signals.

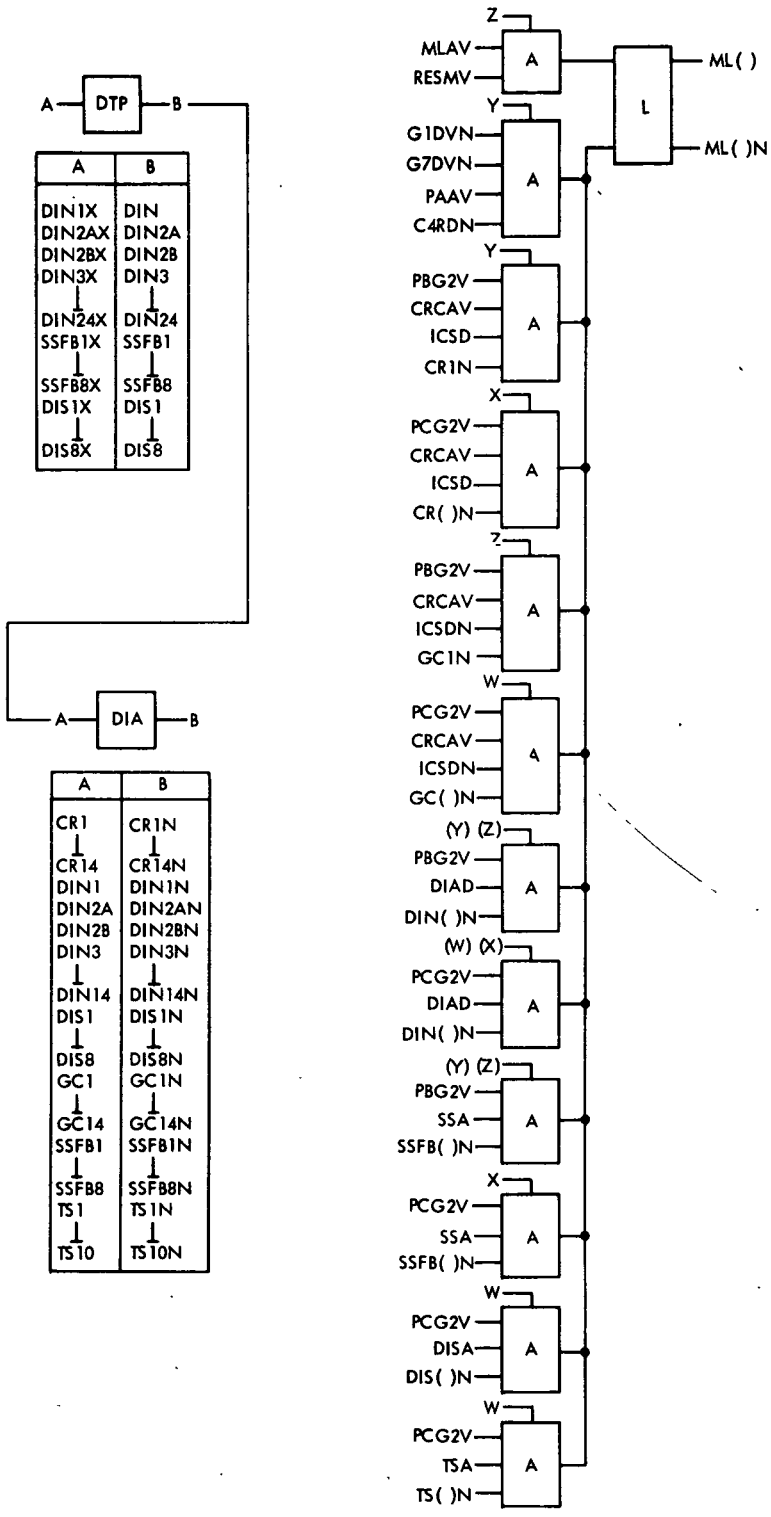


Figure 2-57. Typical Multiplexer Latch

LATCH	C4RDN PAAV-Y	CRCAV					DIAD				SSA			DISA	TSA
		ICSD PBG2V-Y	ICSD PCG2V-X	ICSDN PBG2V-Z	ICSDN PCG2V-W	ICSDN PCG2V-X	PBG2V-Y	PBG2V-Z	PCG2V-W	PCG2V-X	PBG2V-Y	PBG2V-Z	PCG2V-X	PCG2V-W	PCG2V-W
ML1-2	(BG14)	CR1	CR2	GC1	GC2			DIN11	DIN12			SSFB2X	SSFB3X		
ML3	(BG2)		CR3			GC3				DIN13X			SSFB4X		
ML4	(BG3)		CR4			GC4				DIN14X			SSFB5X		
ML5	(BG4)		CR5			GC5	DIN1X			DIN15X			SSFB6X		TS1
ML6	(BG5)		CR6			GC6	(ICSD)			(ICSDN)			SSFB7X		TS2
							DIN2AX			DIN16X					
							DIN2BX								
ML7	(BG6)		CR7			GC7	DIN3X			DIN17X			SSFB8X	DIS1X	TS3
ML8	(BG7)		CR8			GC8	DIN4X			DIN18X				DIS2X	TS4
ML9	(BG8)		CR9			GC9	DIN5X			DIN19X				DIS3X	TS5
ML10	(BG9)		CR10			GC10	DIN6X			DIN20X				DIS4X	TS6
ML11	(BG10)		CR11			GC11	DIN7X			DIN21X				DIS5X	TS7
ML12	(BG11)		CR12			GC12	DIN8X			DIN22X				DIS6X	TS8
ML13	(BG12)		CR13			GC13	DIN9X			DIN23X				DIS7X	TS9
ML14	(BG13)		CR14			GC14	DIN10X			DIN24X	SSFB1X			DIS8X	TS10

BG2 thru BG14 - (Real Time)
CR - Command Receiver
CRCA - Command Receiver and Ground Computer Address
DIAD - Discrete Input Address
DIN - Distributor Input
DIS - Discrete Input Spares
GC - Ground Computer
ICSD - Command Receiver Address
ICSDN - Ground Computer Address
SSA - Switch Selector Address
SSFB - Switch Selector Feedback
TS - Telemetry Scanner
TSA - Telemetry Scanner Address

Figure 2-58. Multiplexer Inputs

CONDITIONING SIGNAL	A4	A5	TIME		SELECTED SIGNAL	TYPE OF DATA
			PAAV		TAGS	TAG CODE
MLAV			PHASES B AND C	BIT TIME 1 2 3 ... 15	ML1-2 ML1-2 ML3 ... ML14	MULTIPLEXER
EMA			PAAVN		DOMS	ERROR
CODGV			PAAVN		CCSL	RESOLVER
MBYPD	0	0	PBAV		C4RDA	ACCEL. X
	0	0	PCAV . PAAVN		C4RDC	
	0	1	PBAV		C4RDB	ACCEL. Y
	0	1	PCAV . PAAVN		C4RDA	
	1	0	PBAV		C4RDC	ACCEL. Z
	1	0	PCAV . PAAVN		C4RDB	
	1	1	ITS		C1RD	INTERRUPT

CODGV - COD OPERATION ADDRESS
EMA - ERROR MONITOR REGISTER ADDRESS
ITS - INTERRUPT TIMING SIGNAL
MBYPD - BY-PASS MULTIPLEXER ADDRESS
MLAV - MULTIPLEXER ADDRESS

Figure 2-59. Serializer-Selector Inputs

PHASE B														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	
ML 1-2	ML 1-2	ML 3	ML 4	ML 5	ML 6	ML 7	ML 8	ML 9	ML 10	ML 11	ML 12	ML 13	ML 14	

PHASE C															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
ML 1-2	ML 1-2	ML 3	ML 4	ML 5	ML 6	ML 7	ML 8	ML 9	ML 10	ML 11	ML 12	ML 13	ML 14	ML 15	

Figure 2-60. Serializer-Selector Output Format

2-166. The data adapter contains five types of Processors: the Resolver Processor, the Accelerometer/Time Processor, the Countdown Processors, the Interrupt Processor and the Tag Processor. All except the Resolver Processor and Tag Processor make use of the Processor Delay Line, explained earlier in this section.

2-167. RESOLVER PROCESSOR.

2-168. In the guidance system for which the data adapter is designed, the inertial platform gimbals and accelerometers drive resolvers whose outputs are fed to the data adapter. Two resolvers are provided for each of the gimbals and accelerometers. One of each pair is called the coarse resolver and the other is called the fine resolver. The coarse resolver is driven directly from the gimbal or accelerometer shaft. The fine resolvers are driven from the same shafts through mechanisms producing a ratio of 1:32 for the gimbal resolvers and 1:8 for the accelerometer resolvers. Thus, a complete rotation of a coarse resolver shaft represents a gimbal or accelerometer shaft rotation of 360°. A complete rotation of a fine accelerometer shaft represents a gimbal shaft rotation of 11°15' or an accelerometer shaft rotation of 45°.

2-169. The outputs from each resolver consist of a pair of 1016 cps a-c signals which are proportional in amplitude to the sine and cosine of the resolver shaft angle. Briefly, the resolver outputs are fed to an R-C network which equalizes the amplitudes of the two outputs and develops a phase shift between them which is dependent upon the angular position of the resolver shaft.

2-170. Basically, the Resolver Processor measures the amount of phase shift between the outputs of each R-C network by starting a binary counter at a certain point on one of the network signals and stopping the counter at the same point on the other network signal. The counter total will be proportional to the amount of phase shift and, consequently, to the amount of rotation of the gimbal or accelerometer shaft which drives the resolver.

2-171. Figure 2-61 shows a pair of sine waves shifted 90° from one another. In this example, the counter is started, then stopped as first sine wave A, then sine wave B rises past its baseline. The counter will therefore run for an interval of time equivalent to 90° of the sine wave. For a 1016 cps sine wave, this interval will be about 246 usec. The counter runs at a rate of 2.048 mc, or one count every 0.488 usec. For the 90° interval of the 1016 cps sine wave in this example, the counter will reach a total of 503 (decimal).

2-172. The counter scaling is determined by the fraction of the 1016 cps sine wave period during which one 2.048 mc count occurs. Multiplied by 3600, this fraction expresses minutes of phase shift per bit. This value turns out to be approximately 10.7 minutes of phase shift per bit.

2-173. The maximum value which the counter can reach on a phase shift count is 2015 (decimal) which represents a phase shift just slightly under 360°. Before the phase shift could expand enough to allow another count, it would have passed through 360° which brings the sine waves back in phase and causes a counter reading of 0. The counter could store a maximum value of 2048 (decimal), an ample excess over the maximum value available from a phase shift count.

2-174. The relation between output phase shift and resolver shaft angle is such that every degree of resolver shaft rotation produces a phase shift of two degrees. Thus, the counter scaling for resolver shaft angle is half the scaling for phase shift angle, or about 5.35 minutes of shaft rotation per bit.

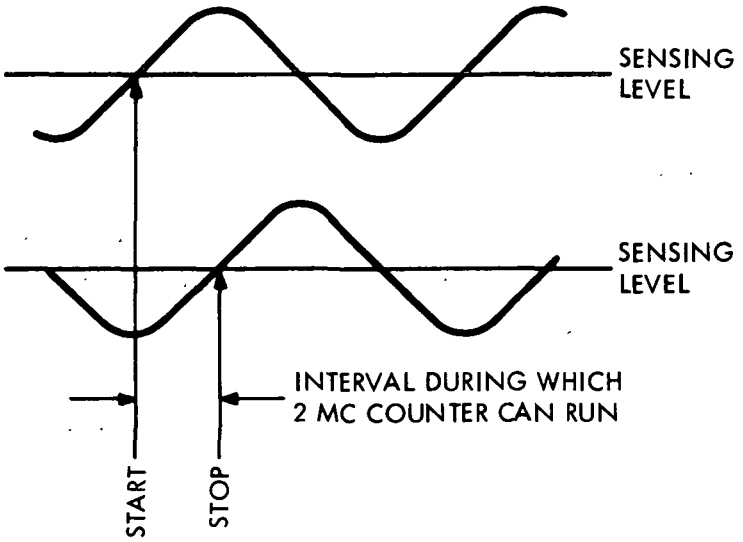


Figure 2-61. Measuring Phase Shift with A Binary Counter

2-175. For the coarse resolvers, the counter measures the phase shift between the resolver excitation signal and one of the R-C network outputs. In this case, the amount of phase shift is identical with the amount of shaft rotation. In other words, one degree of shaft rotation produces one degree of phase shift. It is still possible to run the counter between the two R-C network phases from the coarse gimbal resolvers. This is done whenever it is determined that the usual coarse resolver outputs are not functioning properly. The output taken from the normally not-used junction of the coarse resolver R-C network is therefore called the back-up output. When the back-up output is used, the coarse resolver counter scaling becomes the same as the fine resolver scaling.

2-176. The platform resolver outputs are fed to Crossover Detector (COD) circuits which contain the R-C networks previously mentioned. The COD circuits also sense the baseline crossover of the sine waves from the R-C network (or from the excitation signal in the case of coarse resolvers), producing an up level when the sine wave crosses its baseline in a positive direction and a down level when the sine wave crosses its baseline in a negative direction. It is this square wave output from the COD circuits which is used to start and stop the counter.

2-177. The amplitude of the sine waves from the R-C networks in the COD circuits are supposed to remain constant. After going through an isolating amplifier in the COD circuit, these signals are fed to a monitoring circuit called a Resolver Telemetry Buffer (RTB). Each RTB circuit can monitor two signals. If the rms value of either input signal falls below prescribed limits, the RTB circuit output will become a "0", indicating a malfunction. The RTB circuit outputs, called Crossover Error Signals (CES), are fed to the Internal Data Sampler, previously described.

2-178. There are 38 COD circuits in the data adapter. The input and output signals of each COD and the input from each COD to the RTB circuits are shown as follows:

Source	Input to COD	Output of COD	Input to RTB
X GIMBAL	XR1PA	FG1R	CE1B
	XR1PB	FG1P	CE10B
Y GIMBAL	YR1PA	FG2R	CE2B
	YR1PB	FG2P	CE3A
Z GIMBAL	ZR1PA	FG3R	CE3B
	ZR1PB	FG3P	CE1A
None	RR1PA	FG4R	CE13B
	RR1PB	FG4P	CE11A
X GIMBAL	XR2PA	CG1R	CE6B
	XR2PB	BU1P	CE2A
Y GIMBAL	YR2PA	CG2R	CE12B
	YR2PB	BU2P	CE10A
Z GIMBAL	ZR2PA	CG3R	CE6A
	ZR2PB	BU3P	CE12A
None	RR2PA	CG4R	CE11B
	RR2PB	BU4P	CE13A
Resolver Frequency	RE1EX	CGAP	CE9A
	RE2EX	CGBP	CE9B
None	HS1PA	HS1R	CE5B
	HS1PB	HS1P	CE4A
None	HS2PA	HS2R	CE4B
	HS2PB	HS2P	CE5A
None	HS3PA	HS3R	CE7B
	HS3PB	HS3P	CE8A
None	HS4PA	HS4R	CE8B
	HS4PB	HS4P	CE7A
Accelerometer	AF1PA	AF1R	CE14B
	AF1PB	AF1P	CE19B
Accelerometer	AF2PA	AF2R	CE16B
	AF2PB	AF2P	CE15A
Accelerometer	AF3PA	AF3R	CE16A
	AF3PB	AF3P	CE19A
Accelerometer	AC1PA	AC1R	CE15B
	AC1PB	AC1P	CE17A
Accelerometer	AC2PA	AC2R	CE14A
	AC2PB	AC2P	CE18A
Accelerometer	AC3PA	AC3R	CE17B
	AC3PB	AC3P	CE18B

The PA suffix of the input signals indicates the resolver cosine winding. The PB suffix represents the sine winding. As previously mentioned, each RTB circuit monitors two signals. These signals will have the same designation except that they will be suffixed A and B. Thus, signals CE3A and CE3B will be fed to the same RTB circuit, for example.

2-179. Each of the COD outputs feeds a gate which can be enabled by address codes from the computer. When the CODGV address is issued, the address bits from the repowering latches are transferred to a special address register in the Resolver Processor (figure 2-62). At bit 7 time of phase A, after CODGV has been issued, CODRR (COD Register Reset) is driven to "0" and resets all latches in the special address register. Latch A3CR is double-driven to a double "1" output by CODRR. This output is maintained by signal A3RS. The double "1" output from latch A3CR enables the set gates of the remaining latches in the special address register, and as soon as CODRR returns to a "1" (at the end of bit 8), these latches are set or not set according to the state of signals A4DV through A7DV from the repowering latches. On the following bit 9-Z time, the A3CR latch is either set or reset, breaking the double drive and disabling the set gates of the remaining address latches. This peculiar method of enabling the set gates of the latches was designed to eliminate the need for separate timing signal inputs at each gate.

2-180. The Resolver Processor can operate only during a computer minor loop. Thus, CODGV is issued by the computer only during a minor loop. However, it is possible for the computer to enter the minor loop without issuing CODGV. Therefore, if CODGV is not issued at the time the computer enters the minor loop, one of the resolver addresses is automatically selected. As shown on figure 2-62, CODRR is also driven to "0" (at bit time 11) by MCFT1 and MCFT3. These two signals indicate that the minor loop has been entered. As before, latch A3CR will be double driven to enable the set gates of the remaining latches. At bit time 11, however, the repowering latches will have been reset by PARSV, so nothing will be set into the latches of the special address register. At bit time 13, the minor loop signals will reset the A3CR latch and will simultaneously set latch A5CR, provided signal ICR4N is a "1". The resulting configuration is the address for COD output FG1 (the X gimbal fine resolver). If signal ICR4N (which comes from the Internal Control Register, previously discussed) is a "0", latch A5CR will not be set and the resulting configuration of latches will be the address for BU1, which selects the R-C network output mode from the X gimbal coarse resolver.

2-181. As previously stated, each of the COD outputs feeds a gate which can be selected by the Resolver Processor address register. The "R" signals feed a series of gates on the reset inputs of an AND-extended latch, PCR (figure 2-63). The "P" signals feed a series of gates on the reset inputs of another AND-extended latch, PSTP (figure 2-64). As noted in the discussion of latches, all the inputs to the multiple input side of an AND-extended latch must be "1's" simultaneously in order to set or reset the latch. The top two AND gates on each input to the latches in figures 2-63 and 2-64 are driven from the address register in such a fashion that only one pair of them have "0" inputs simultaneously (one pair, that is, on any one input line). This means that three of the input lines to each latch always have "1's" on them. The remaining input line will be driven to a "1" when the selected COD output goes to a "1".

2-182. Essentially, the PCR latch starts the counter when it is reset and the PSTP latch stops the counter when it is reset. It is a requirement that the counter be started at the beginning of a "1" level from a COD and that it also be stopped at the beginning of a "1" level from a COD circuit. Therefore, both latches must be inhibited from resetting if they sense a "1" input before sensing a "0" input. In other words, if the latches are commanded to start sensing for "1's", and one or the other of them senses a "1" immediately, there is no way of knowing whether the sense point is at the beginning, the middle or the end of the "1". If the latch is forced to wait until the COD output becomes a "0" before it can sense a "1", it will sense the next "1" at its beginning.

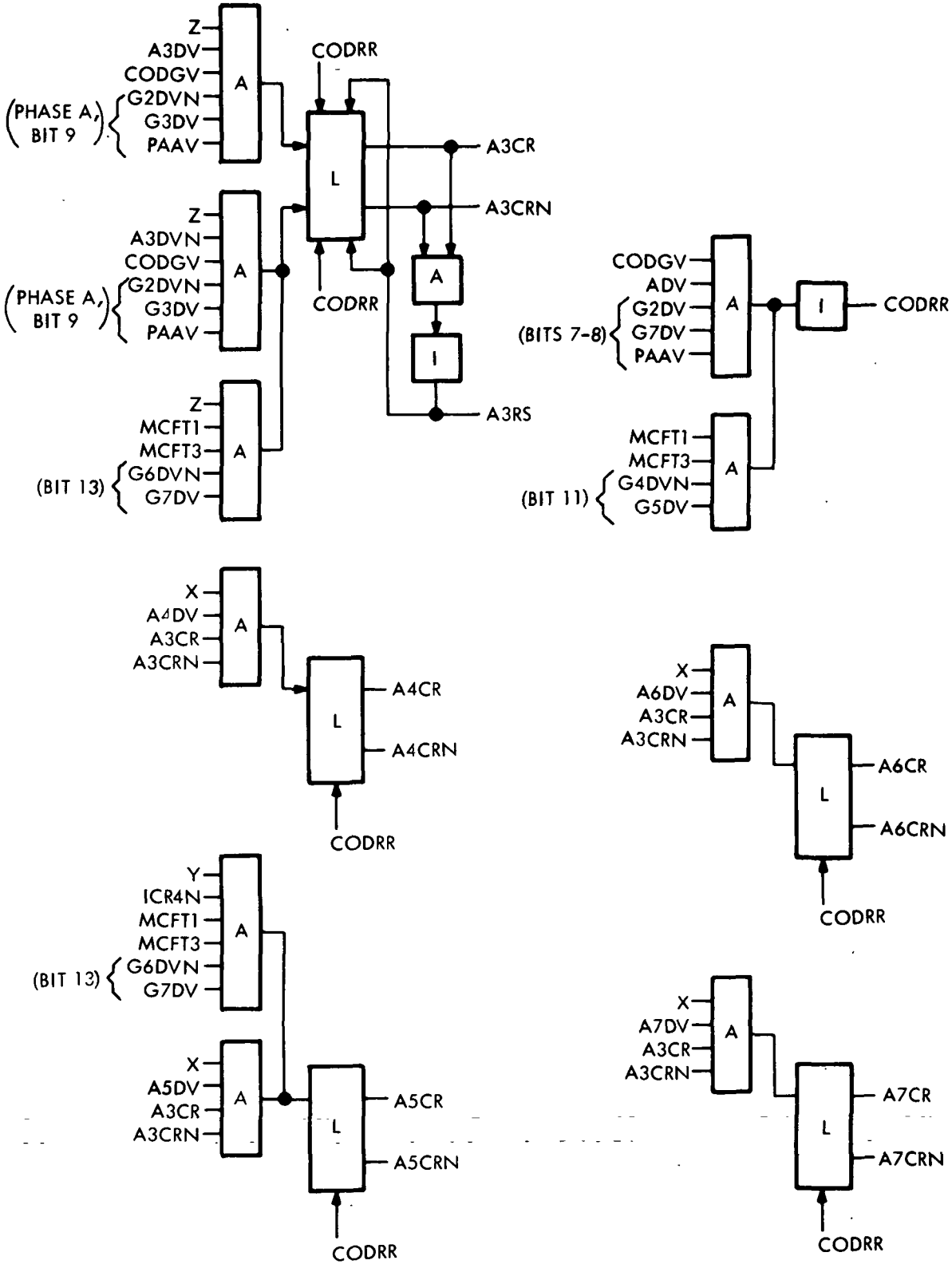


Figure 2-62. Resolver Processor Address Register

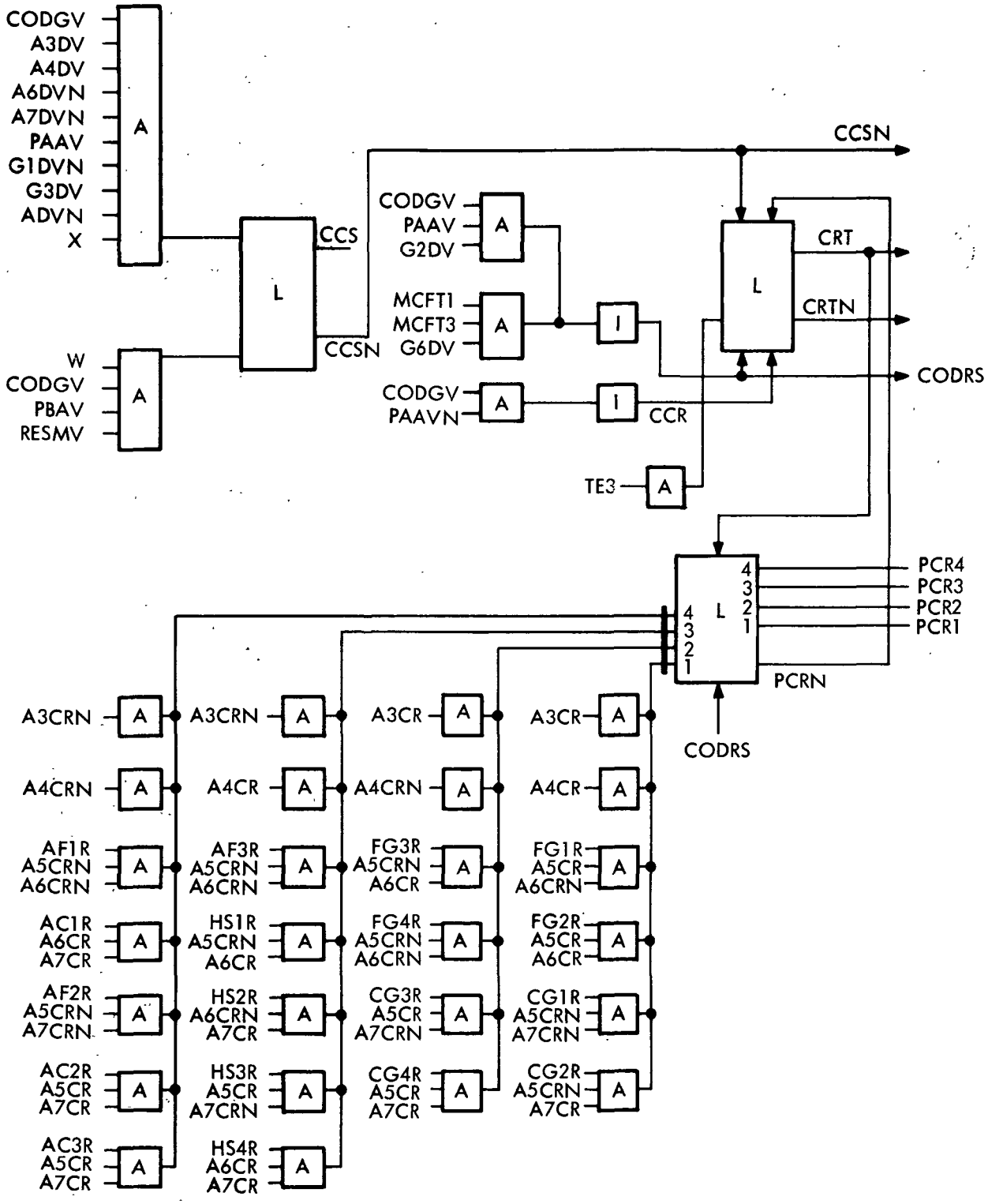


Figure 2-63. Counter Start Latch and Control Circuits

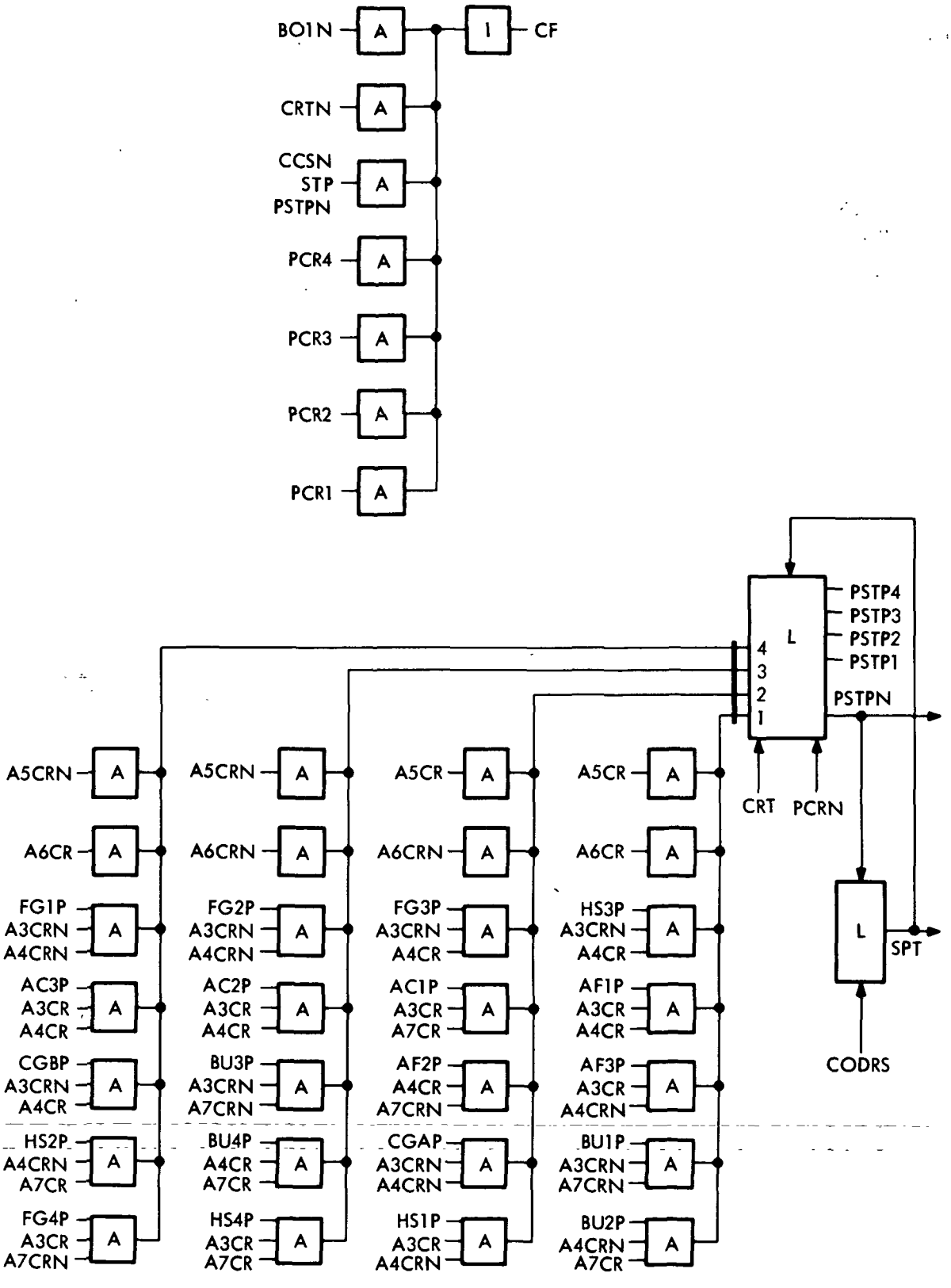


Figure 2-64. Counter Stop Latch and Counter Control Gate.

2-183. The counter is driven by signal CF (figure 2-64) which, in turn, is driven by a 2.048 mc signal from the computer, B01N. In order for signal B01N to be able to drive CF, all inputs to the remaining gates driving the CF inverter must be "0's". A "1" on any one of the gates into the CF latch will lock signal CF to a "0".

2-184. As shown in figure 2-63, either signal CODGV or the minor loop signals MCFT1 and MCFT3 will drive signal CODRS to a "0" whenever it is time to process a COD circuit output. Signal CODRS resets latches CRT, PCR and STP (figures 2-63 and 2-64). Signal CRTN will lock CF to a "0". Latch PSTP will be held to a double "1" output by double zero-drive signals STP and CRT.

2-185. Signal CRT will now attempt to set latch PCR. It will be successful unless all the AND-extended inputs to this latch are "1's", signifying that the selected COD circuit output is a "1". The one-drive inputs override the zero-drive inputs and keep the latch reset. Whenever the selected COD circuit output goes to "0", signal CRT will set the PCR latch. Immediately then, signal PCRN will set the CRT latch and the set outputs of the PCR latch will take over the task of inhibiting CF which was previously accomplished by signal CRTN. Also, signal PCRN will replace CRT to hold the PSTP latch to a double "1" output. Since both the PSTP latch feedback gates have been disabled, the latch cannot be driven to any stable state and therefore, any "1's" at its reset gates will have no effect at this time. Signal STP, still a "0", prevents signals PSTPN and CCSN from locking CF to a "0". Therefore, the only signals holding CF off are the set signals from the start latch, PCR.

2-186. As soon as the selected COD output goes to a "1", latch PCR will be set, releasing CF to be driven by signal B01N. At the same time, the double drive will be removed from latch PSTP and signal STP will set this latch. Signal PSTPN will set the STP latch and simultaneously disable the gate to the CF inverter fed by signals CCSN and STP. Since signal CCSN is normally a "1" and STP has just been driven to a "1", signal PSTPN becomes the controlling signal to turn CF off. This will occur whenever the selected COD output feeding latch PSTPN becomes a "1" and resets the latch.

2-187. Latch CCS (Counter Checkout Set) is normally reset. It is set by a special address from the computer in order to place a known value in the counter. When the CCS latch is set, signal CCSN will set the CRT latch and remove the clamp on CF caused by signal CRTN. Latch PCRN will have been reset by CODRS and will not be able to clamp CF. Signal CCSN will inhibit clamping of CF by STP or PSTPN, so the counter will be allowed to run. At the end of phase A, signal CCR is driven to a "0" and resets the CRT latch, stopping the counter. Input TE3 is an input, from test equipment, which resets latch CRT at any desired time to stop the counter.

2-188. The remaining descriptions of the processors will be included in subsequent revisions to this manual.

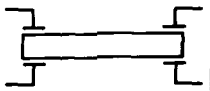
2-189. TELEMETRY CIRCUITS.

2-190. Descriptions of the Telemetry Circuits are not provided for the simplex model data adapters. This portion of the manual will be included in the subsequent revisions to this manual.

MIB SYMBOLS

Symbol	Name	Description
A	AND-Gate	AND-Gate with output OR-diode capability depending on manner of input-output connections. Three types are used: A, figure A-1; AA, figure A-2; and AB, figure A-3.
ATB	Analog Telemetry Buffer	Isolates analog output signals from telemetry circuit reference voltages. Input ranges between plus and minus 12.5 volts dc. Output (referenced to telemetry ground) is 0.204 times the input (referenced to data adapter ground) plus 2.5 volts dc. (See figure A-4.)
BES	Bipolar Electronic Switch	Gates outputs of digital-to-analog converter and reference decoder to converter-selector and comparator, respectively. A 500 kc square wave on logic input closes switch making analog input available at output. Switch is open when logic input is quiescnet. Can be used in either of two modes: Sample and Hold mode or Sample Output mode. (A capacitor from output to ground in MIB logic specifies Sample and Hold mode of operation.) (See figure A-5.)
CD4	Clock Driver, Type 4	An inverter used in conjunction with RDN and FP438 circuits to provide non-inverted power gain for clock pulses. (See figure A-6.)
CLN	Collector Load Network	A package of 1.8k Ω resistors which can be connected in parallel with collector loads in various circuits to provide additional drive capability. (See figure A-7.)

Symbol	Name	Description
COD	Cross Over Detector	Converts sine wave from resolver or frequency source to square wave for controlling COD counter. Output changes states when input sine-wave crosses over its base line. (See figure A-8.)
CPD	Cordwood Page Decoupling Circuit	A capacitor package used to decouple transient signals from the supply voltages used in circuit modules (cordwood modules). (See figure A-9.)
CPR	Comparator	Produces a "O" output whenever its two input signal levels differ by 37 or more millivolts. Otherwise, the output is a "1". The input signals range between plus and minus 6 volts dc with respect to ground. (See figure A-10.)
CS	Converter Select	Connects to two Ladder Decoder Amplifiers and is driven by complementary signals. Feeds +20 volts dc to one amplifier at a time, depending on the input signal condition. Also includes common negative source for amplifiers, since only one amplifier is operative at any given time. (See figure A-11.)
CTN	Collector, Transistor, Network	Used in conjunction with HCI to produce additional drive capability necessary to drive capacitive loads. (See figure A-12.)
C1	Capacitor, Type 1	Capacitor, 0.22 ufd, 35v
C2	Capacitor, Type 2	Capacitor, 2.2 ufd, 20v
C3	Capacitor, Type 3	Capacitor, 5.6 ufd, 10v
C4	Capacitor, Type 4	Capacitor, 8.2 ufd, 6v
DD	Disagreement Detector	Used in conjunction with DDI to sense non-unanimous input conditions. If input signals are all alike, output of DD appears as open circuit. If input signals are non-unanimous, output drives load located in DDI to "O". (See figure A-13.)

<table>
<tr><th>Symbol</th><th>Name</th><th>Description</th></tr>
<tr><td>DDI</td><td>Disagreement Detector Inverter</td><td>Used in conjunction with FP438 to provide power gain and inversion of signal from DD. Contains common load resistor for a number of DD circuits, thus providing OR function for DD's. (See figure A-14.)</td></tr>
<tr><td>DELAY LINE
or
  </td><td>Delay Line</td><td>An electromechanical delay line which consists of two piezoelectric transducers separated by a column of glass. Mechanical pulses generated by the driving transducer are transmitted through the glass to the sensing transducer, the delay between input and output being proportional to the length of the glass column. The delay line must be driven by a DLD circuit through a potentiometer (POT circuit). Its output is amplified by a DSA circuit.</td></tr>
<tr><td>DIA</td><td>Discrete Input Circuit, Type A</td><td>Provides voltage conversion between discrete input logic levels and data adapter logic levels. Specific conversion is as follows:
<table><tr><th>Input</th><th>Output</th></tr><tr><td>+28v</td><td>0v</td></tr><tr><td>0v</td><td>+6v</td></tr></table>Conversion includes logical inversion. Two inputs are provided to accomodate varying drive capabilities of external circuits. (See figure A-15.)</td></tr>
<tr><td>DIB</td><td>Discrete Input Circuit, Type B</td><td>Essentially the same as a DIA circuit, except that +28v input is replaced by open circuit. Specific conversion is as follows:
<table><tr><th>Input</th><th>Output</th></tr><tr><td>OPEN</td><td>0v</td></tr><tr><td>0v</td><td>+6v</td></tr></table>(See figure A-16.)</td></tr>
</table>

Symbol	Name	Description
DLD	Delay Line Driver	Used in conjunction with an FP438 and a potentiometer (POT circuit) to pulse the delay line driving transducer. Drives only when both the clock and the logic inputs are "1s". The potentiometer (POT) is a factory adjustment to match individual delay lines to the driving and sensing circuits. (See figure A-17.)
DLM	Dummy Load Module	A package of resistors used to supply loads to SDI, SDL, TDH, TDL and TDM circuits to discharge line capacitance. (See figure A-18.)
DSA	Delay Line Sense Amplifier	Amplifies the output of the Delay Line. (See figure A-19.)
DTP	Discrete Transient Protector	A package of resistors used in conjunction with diodes and resistors to form transient suppression circuits which, in turn, protect the DIA circuit from a malfunction when: a) the input is a "1" and a 100 usec (max) transient of -150 volts dc (max) is superimposed on the input. b) the input is a "0" and a 4 usec (max) transient of + 150 volts dc (max) is superimposed on the input. (See figure A-20.)
FP355	Flat-Pack, Type 355	A package of two NPN transistors. (See figure A-21.)
FP438	Flat-Pack, Type 438	A package of two PNP transistors. (See figure A-22.)
HCI	High Current Inverter	Inverter; used where extra drive power is required. Must operate in conjunction with CLN circuit which provides output load. (See figure A-23.)

Symbol	Name	Description
I	Inverter	Inverter; output drive capability may be increased by connecting additional load resistor in CLN circuit. (See figure A-24.)
IB	Interface Buffer	Used in conjunction with FP355s and FP438s. Provides ground isolation, power gain and noise rejection for 6v logic signals entering the data adapter from external equipments. Does not introduce logical inversion. (See figure A-25.)
IDH	Intermediate Driver, High Current	Intermediate stage between output register and peripheral equipment. Drives TDM or TDH; provides logical inversion. (See figure A-26.)
IDL	Intermediate Driver, Low Current	Intermediate stage between output register and peripheral equipment. Drives TDL, SDL or SDH; provides logical inversion. (See figure A-27.)
LDA	Ladder Decoder Amplifier	Amplifies and isolates output of ladder network. A gain of 1, 2 or 4 is available depending on connection of input and feedback common (FB COMM). (See figure A-28.)
LRN	Ladder Resistive Network	Part of digital-to-analog converter. Output is analog voltage proportional to magnitude of binary inputs. Polarity follows sign input and amplitude is scaled at 6 millivolts per low order bit. (See figure A-29.)
M3B	Minus 3 Volt Telemetry Buffer	Provides + 3 volt dc output to telemetry which is proportional to output of -3 volt supply. (See figure A-30.)
NCG	Negative Current Generator	Negative constant current source for LRN. Four generators per CM, each turned on by a separate NCS. (See figure A-31.)

Symbol	Name	Description
NCS	Negative Current Switch	Provides logic control for switching NCGs on and off. If both inputs are "1's", output will turn NCG on. (See figure A-32.)
NVR	Negative Voltage Reference	Provides regulated bias voltage to NCGs. (See figure A-33.)
PCG	Positive Current Generator	Positive constant current source for LRN. Four generators per CM, each is turned on by a separate PCS. (See figure A-34.)
PCS	Positive Current Switch	Provides logic control for switching PCGs on and off. If both inputs are "1's", output will turn PCG on. (See figure A-35.)
POT	Potentiometer	See DLD.
PVR		Provides regulated bias voltage to PCGs. (See figure A-33.)
P6B	Plus 6 Volt Telemetry Buffer	Provides + 3 volt dc output to telemetry which is proportional to output of + 6 volt supply. (See figure A-36.)
P12B	Plus 12 Volt Telemetry Buffer	Provides + 3 volt dc output to telemetry which is proportional to output of + 12 volt supply. (See figure A-36.)
RDN	Resistor Diode Network	A package of resistors and diodes used in clock driver circuits. (See figure A-37.)
RTB	Resolver Telemetry Buffer	Monitors output 1 of CODs and provides a "go or no-go" indication of COD and resolver operation to LVDC on request. Output switches to a "0" if either input exceeds 5 volts rms. (See figure A-38.)
SDH	Simplex Driver, High Current	An inverter circuit, driven by an IDL, which drives relays returned to 28 V RET. (See figure A-39.)

Symbol	Name	Description
SDI	Simplex Driver, Isolation	Drives resistive loads equal to or greater than 1125 Ω. Driven by either an SDL or TDL. Produces no signal inversion. (See figure A-40.)
SDL	Simplex Driver, Low Current	An inverter circuit, driven by an IDL, which drives resistive loads returned to 28 V RET. (See figure A-41.)
TDH	TMR Driver, High Current	An inverter circuit, driven by an IDH, which drives 75 Ω relay loads. Has three inputs and acts as a voter. (See figure A-42.)
TDL	TMR Driver, Low Current	An inverter, driven by an IDL, which drives resistive loads equal to or greater than 1080 Ω. Has three inputs and functions as a voter. (See figure A-43.)
TDM	TMR Driver, Medium Current	An inverter, driven by an IDH, which drives 122 Ω relay loads. Has three inputs and functions as a voter. (See figure A-44.)
TMV	TMR Voter	Produces a logic output equivalent to the inverse of the majority logic of its three inputs. Thus, two or more "0's" at its inputs produce a "1" output. Two or more "1's" produce a "0" output. Must be loaded by a VI or HCI circuit. (See figure A-45.)
VI	Voter Inverter	Inverts output of TMV circuit. (See figure A-46.)
20 B	Plus or Minus 20 Volt Telemetry Buffer	Provides + 3 volt dc output to telemetry which is proportional to output of either the + 20 volt or -20 volt supply. (See figure A-30 for hookup to -20 volt supply or figure A-36 for hookup to + 20 volt supply.)

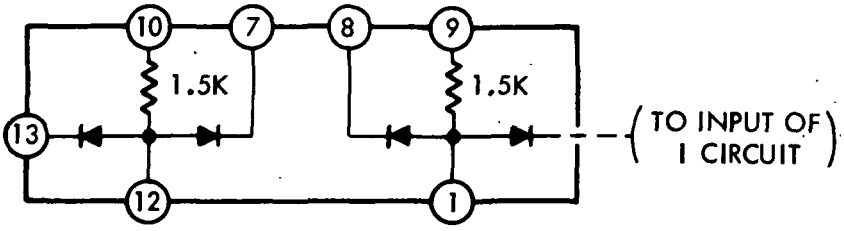


Figure A-1. AND-Gate, Type A

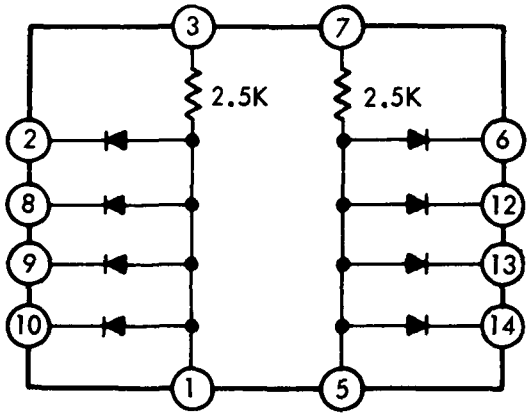


Figure A-2. AND-Gate, Type AA

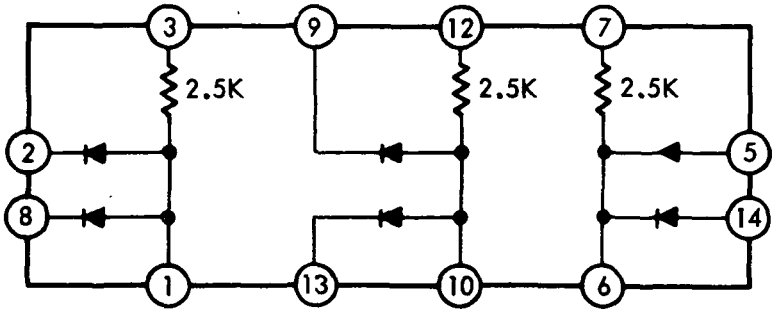


Figure A-3. AND-Gate, Type AB

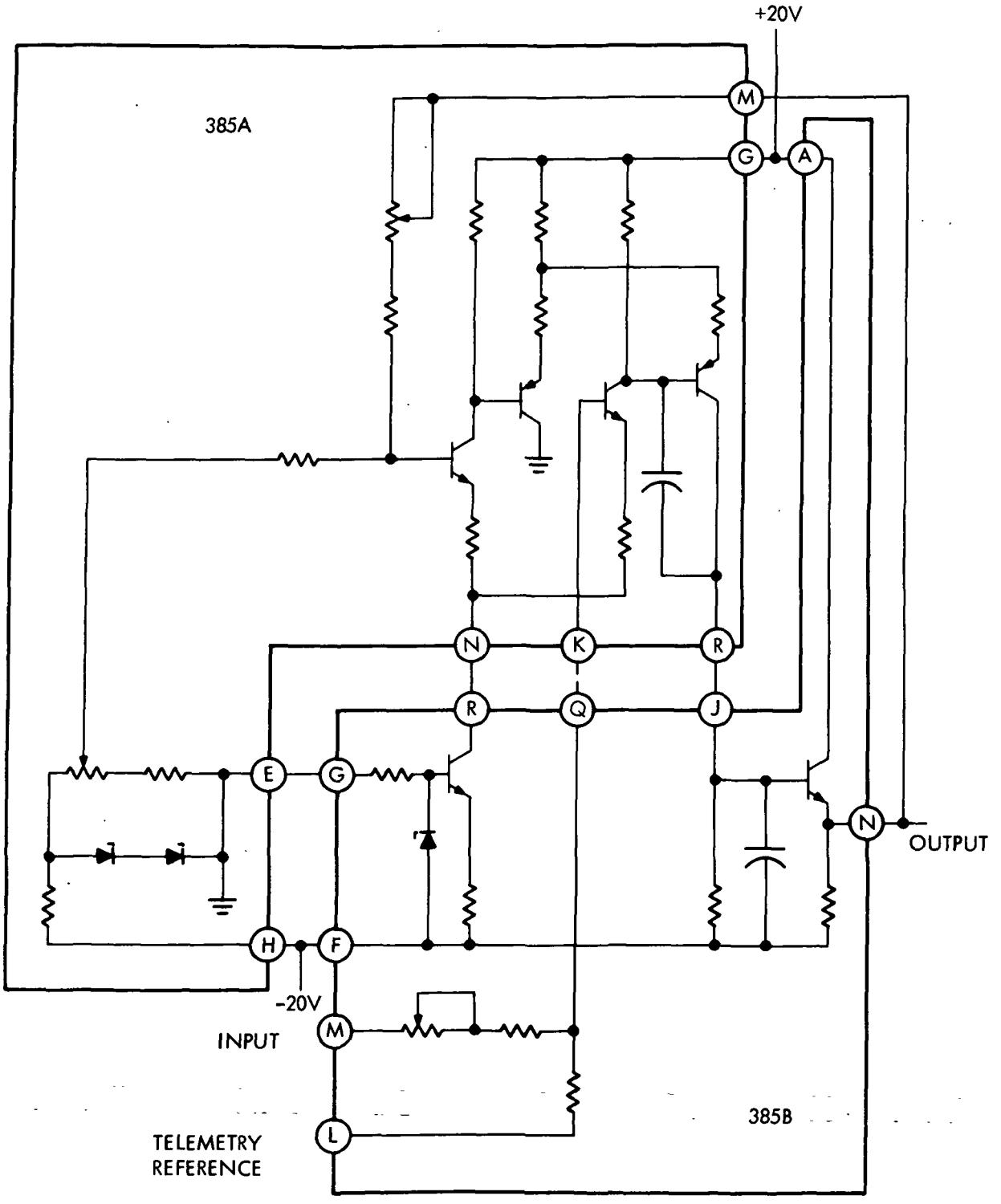


Figure A-4. Analog Telemetry Buffer, ATB

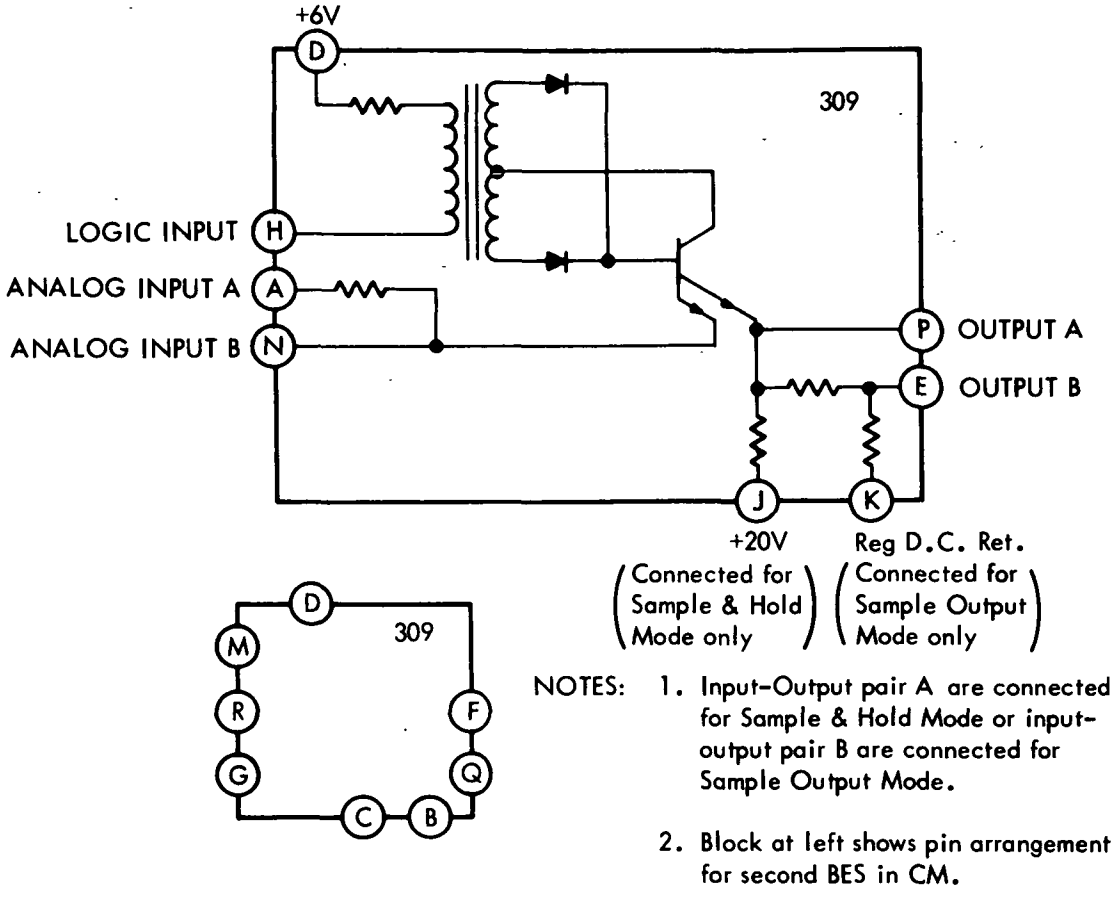


Figure A-5. Bipolar Electronic Switch, BES

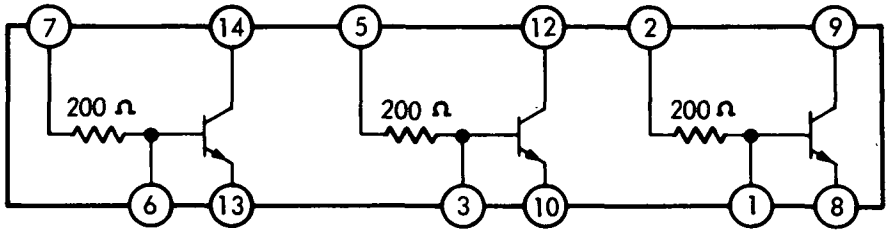


Figure A-6. Clock Driver, Type 4, CD4

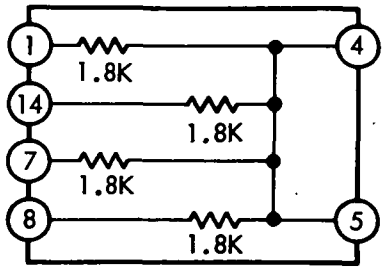


Figure A-7. Collector Load Network, CLN

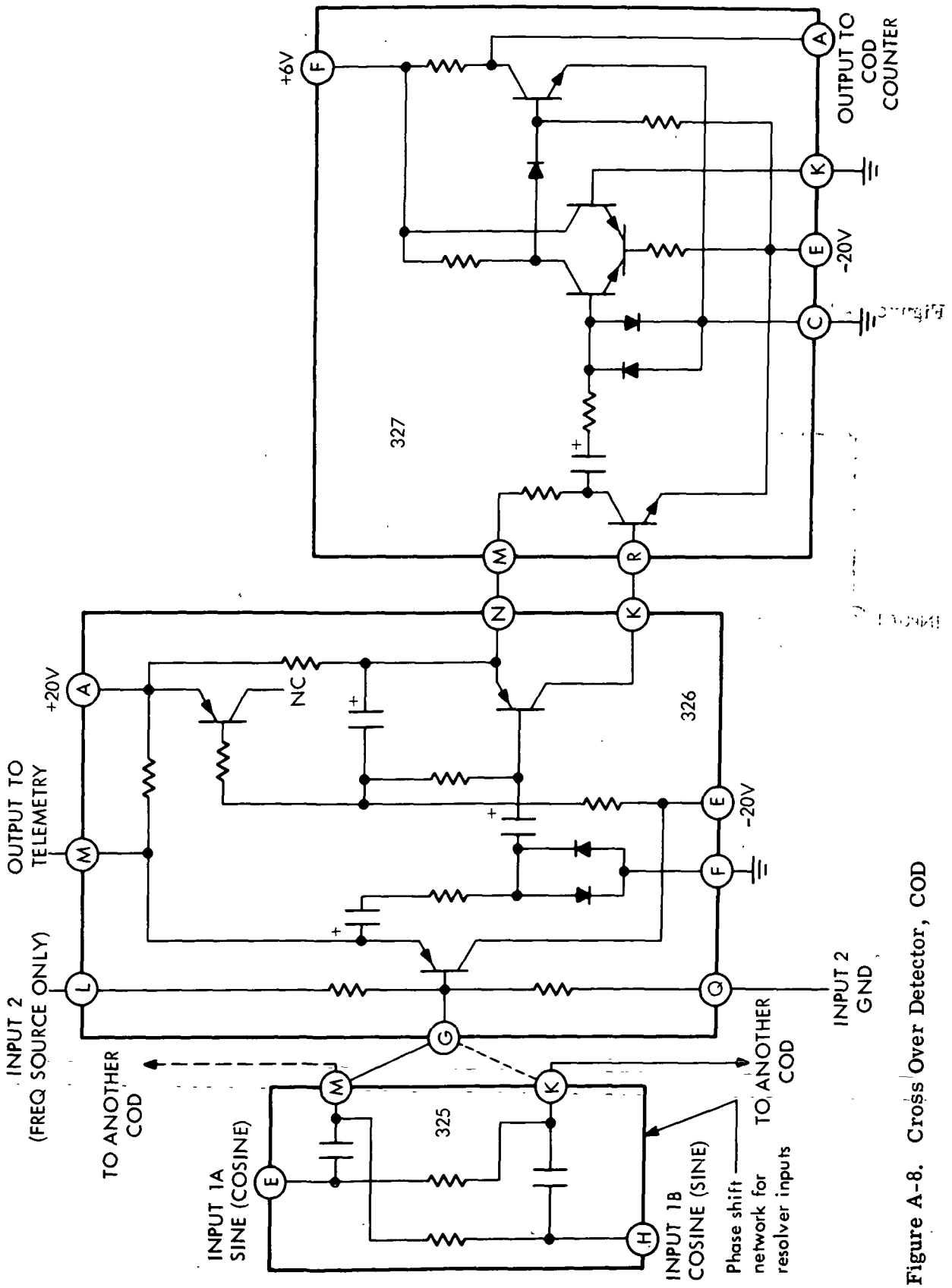


Figure A-8. Cross Over Detector, COD

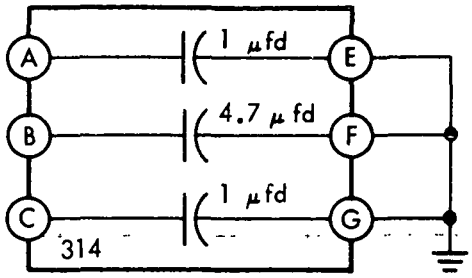


Figure A-9. Cordwood Page Decoupling Circuit, CPD

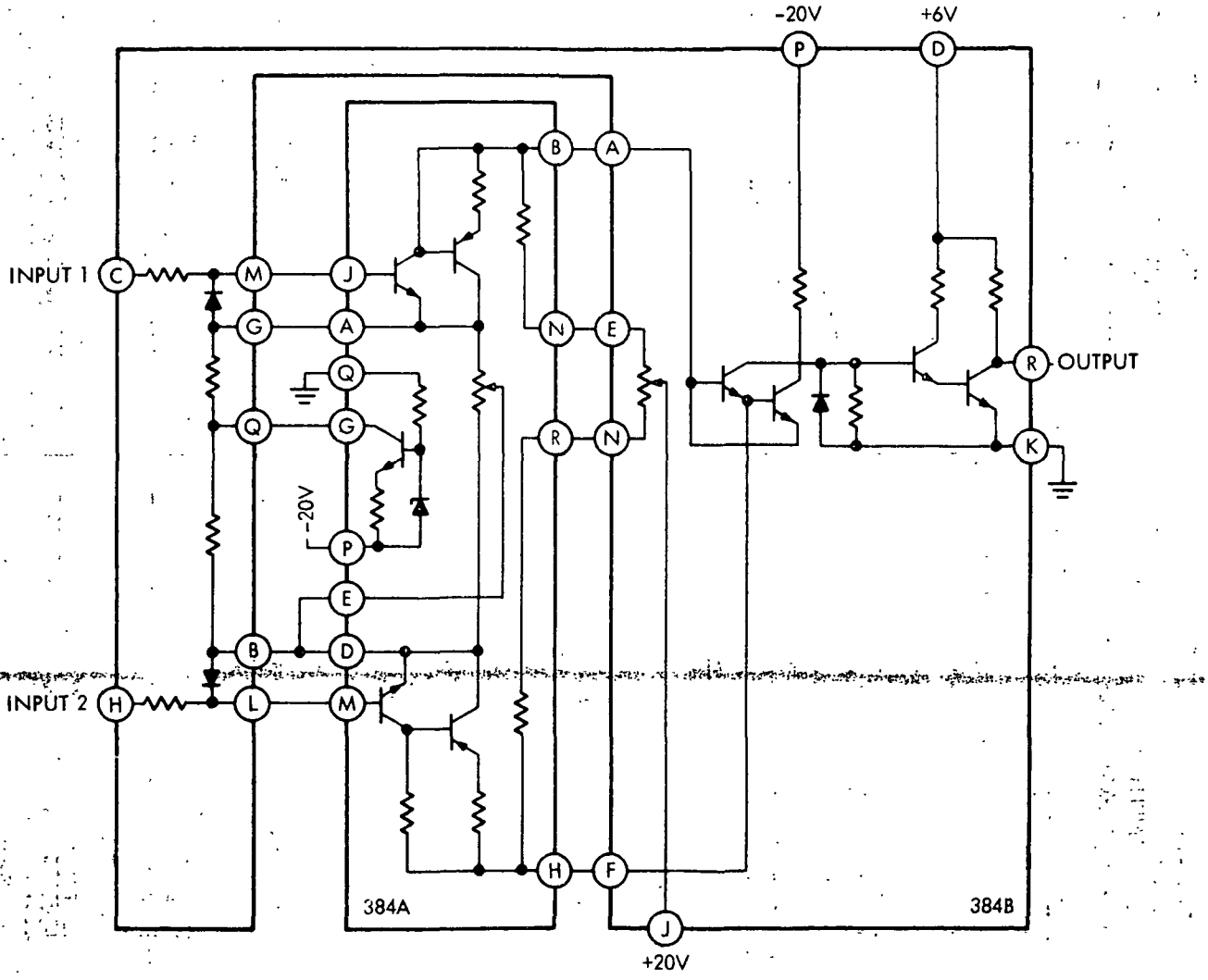


Figure A-10. Comparator, CPR

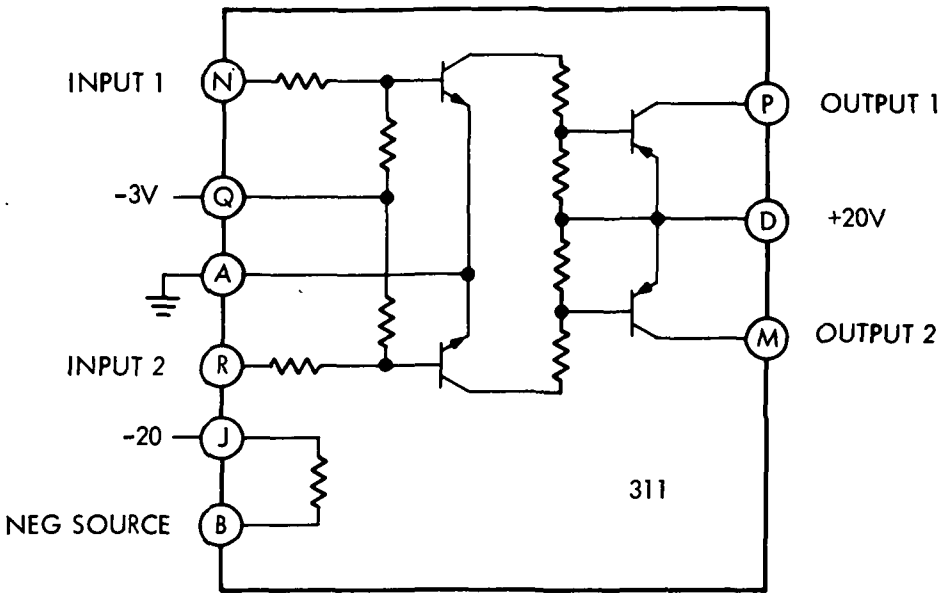


Figure A-11. Converter Select, CS

(To Be Supplied)

Figure A-12. Collector, Transistor, Network, CTW

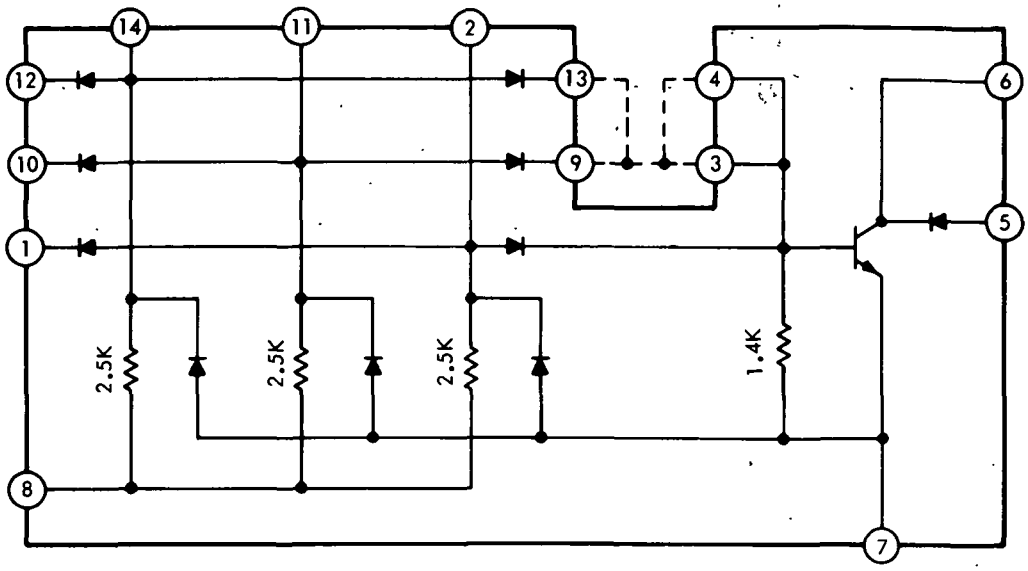


Figure A-13. Disagreement Detector, DD

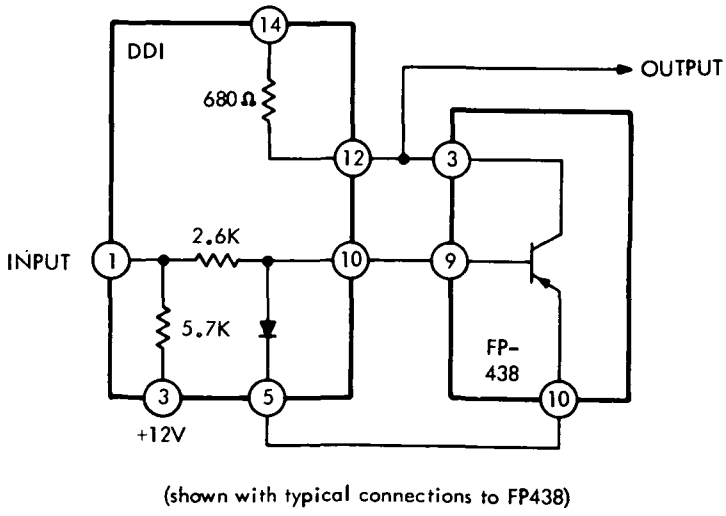


Figure A-14. Disagreement Detector Inverter, DDI

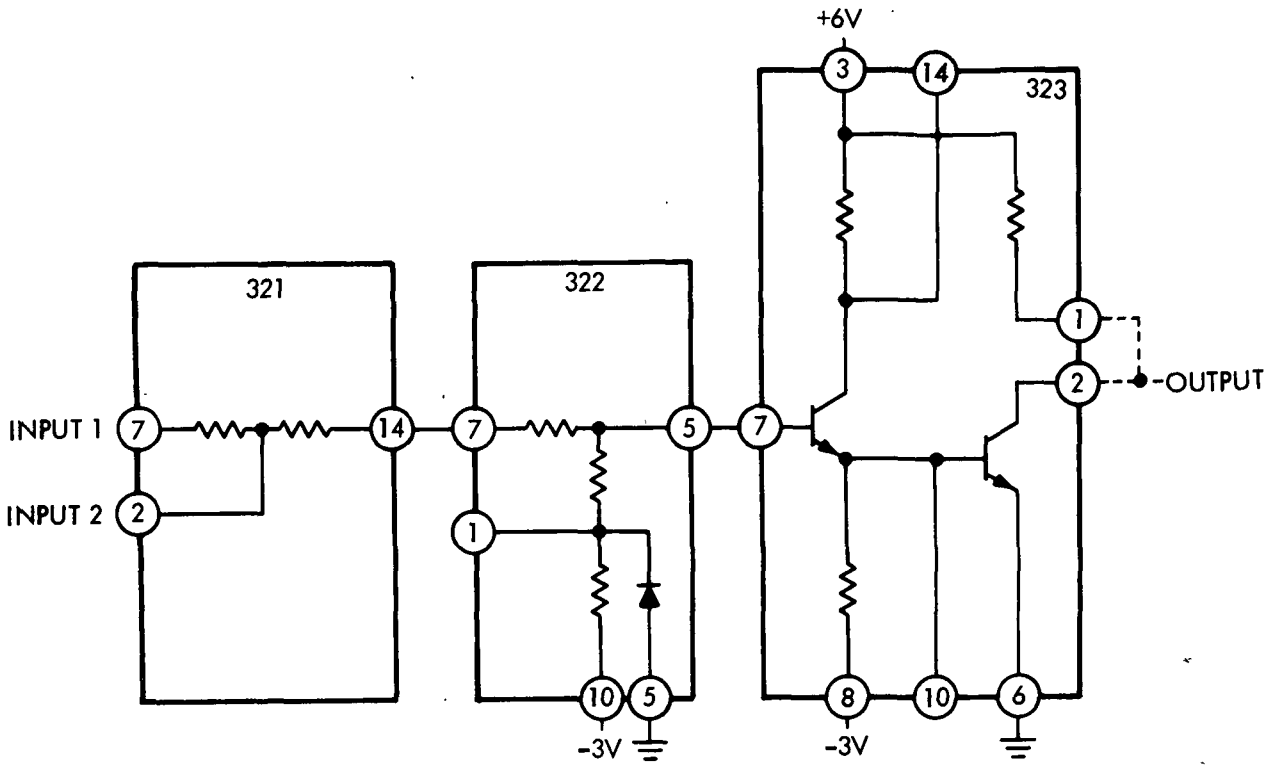


Figure A-15. Discrete Input Circuit, Type A, DIA

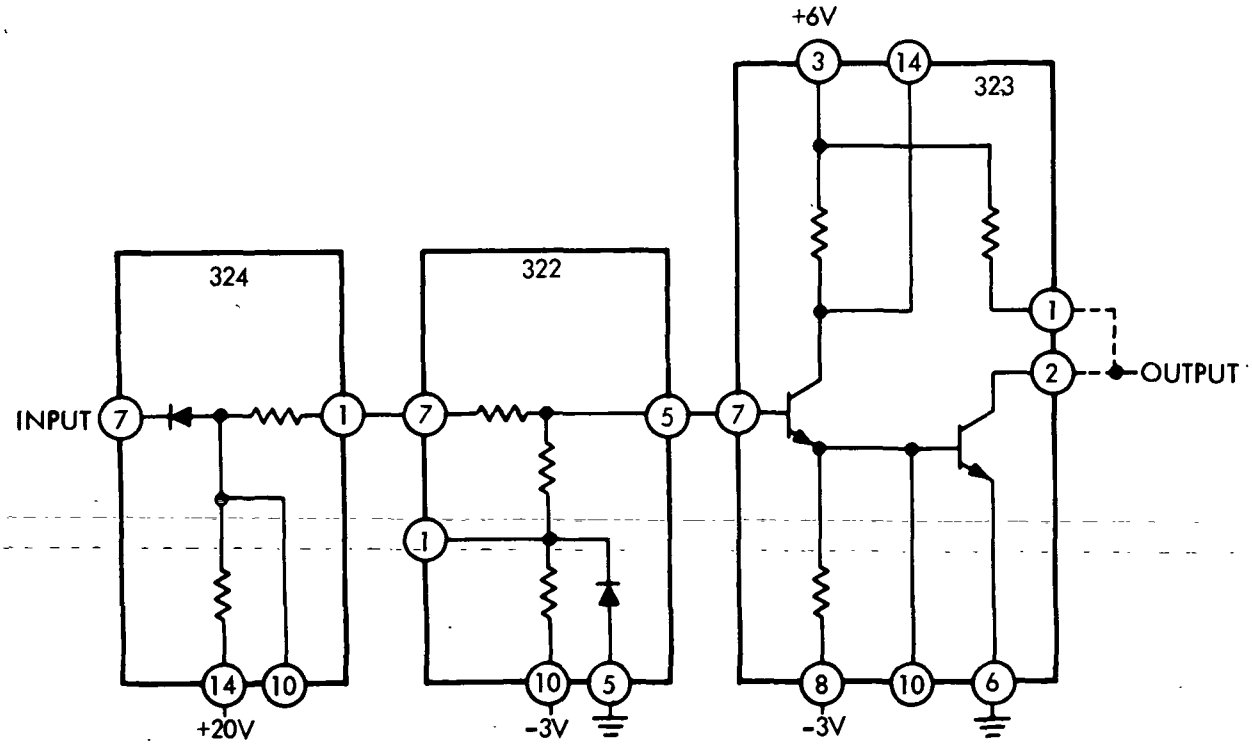


Figure A-16. Discrete Input Circuit, Type B, DIB

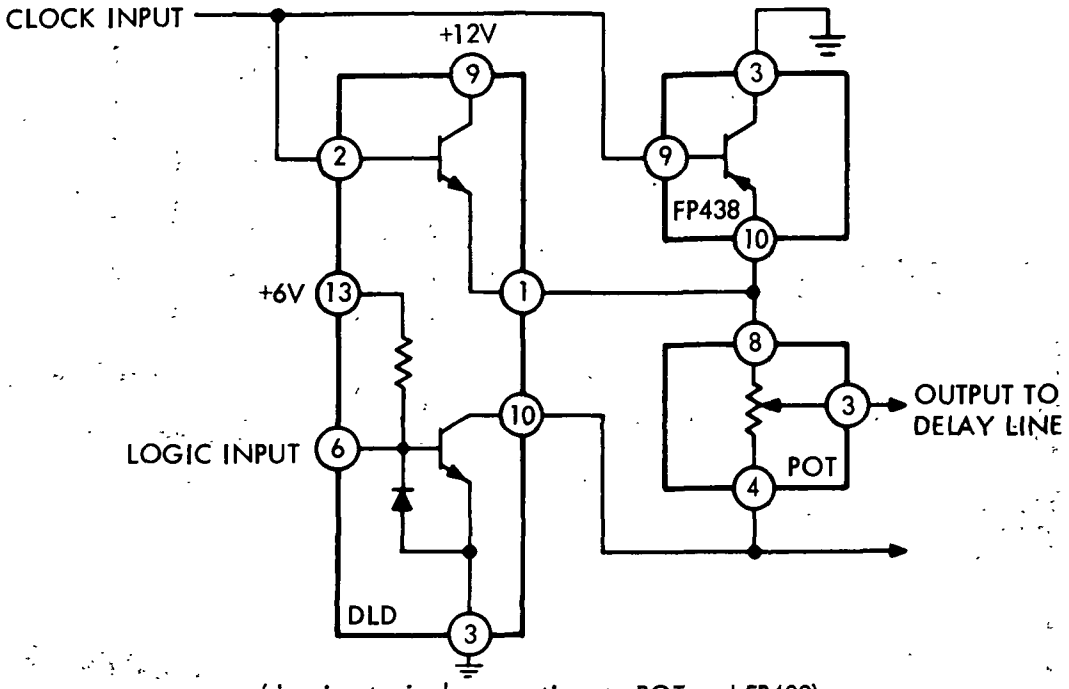


Figure A-17. Delay Line Driver, DLD

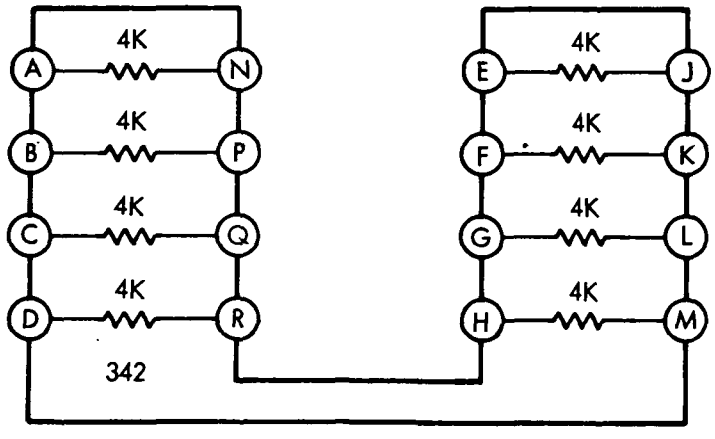


Figure A-18. Dummy Load Module, DLM

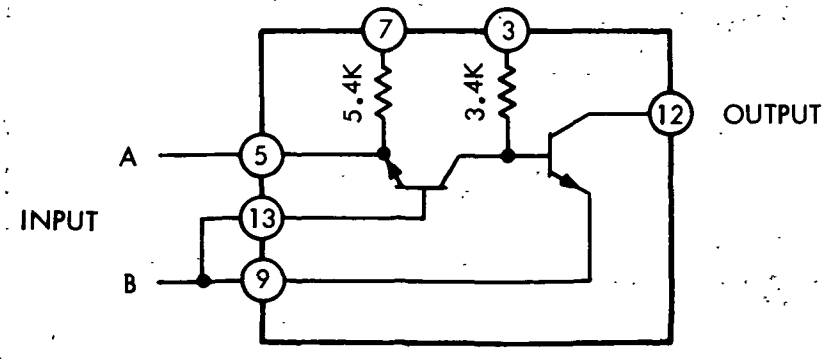


Figure A-19. Delay Line Sense Amplifier, DSA

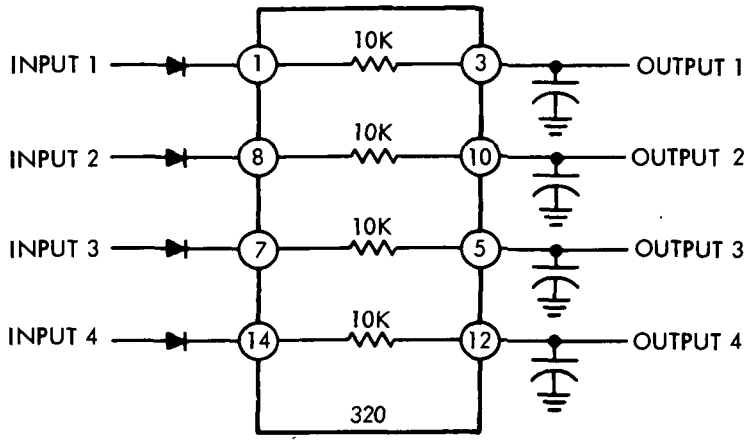


Figure A-20. Discrete Transient Protector, DTP

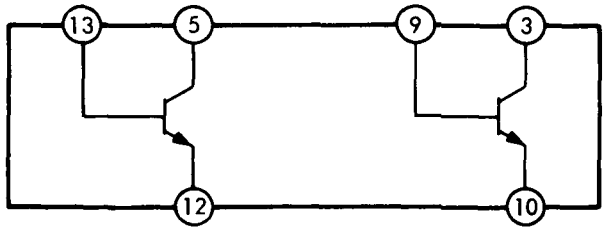


Figure A-21. Flat-Pack, Type 355, FP355

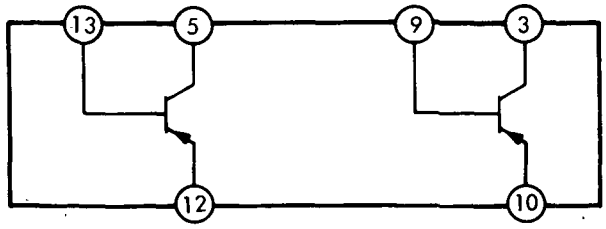


Figure A-22. Flat-Pack, Type 438, FP438

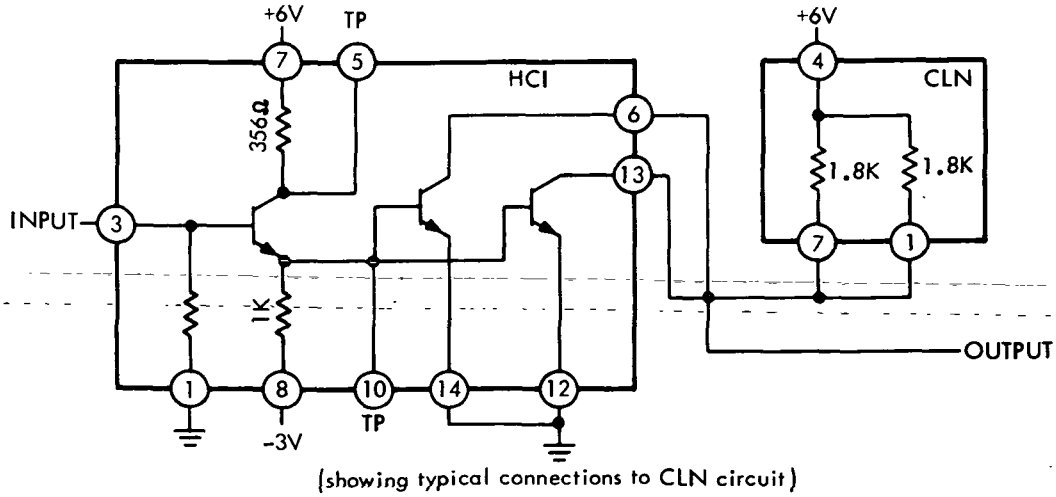


Figure A-23. High-Current-Inverter, HCI

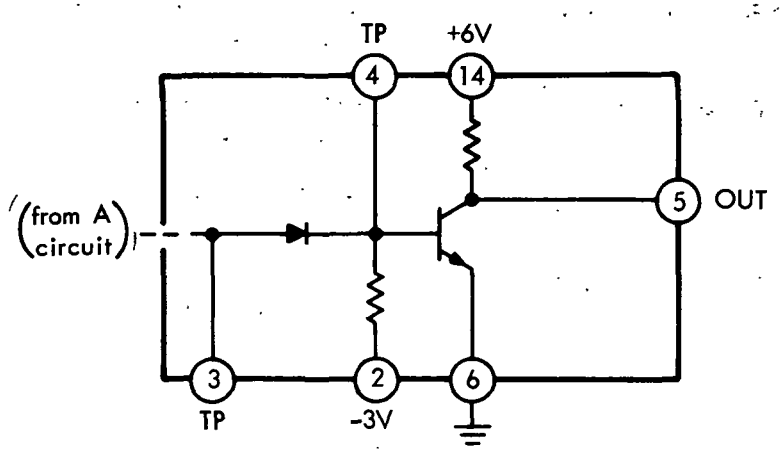


Figure A-24. Inverter Circuit, I

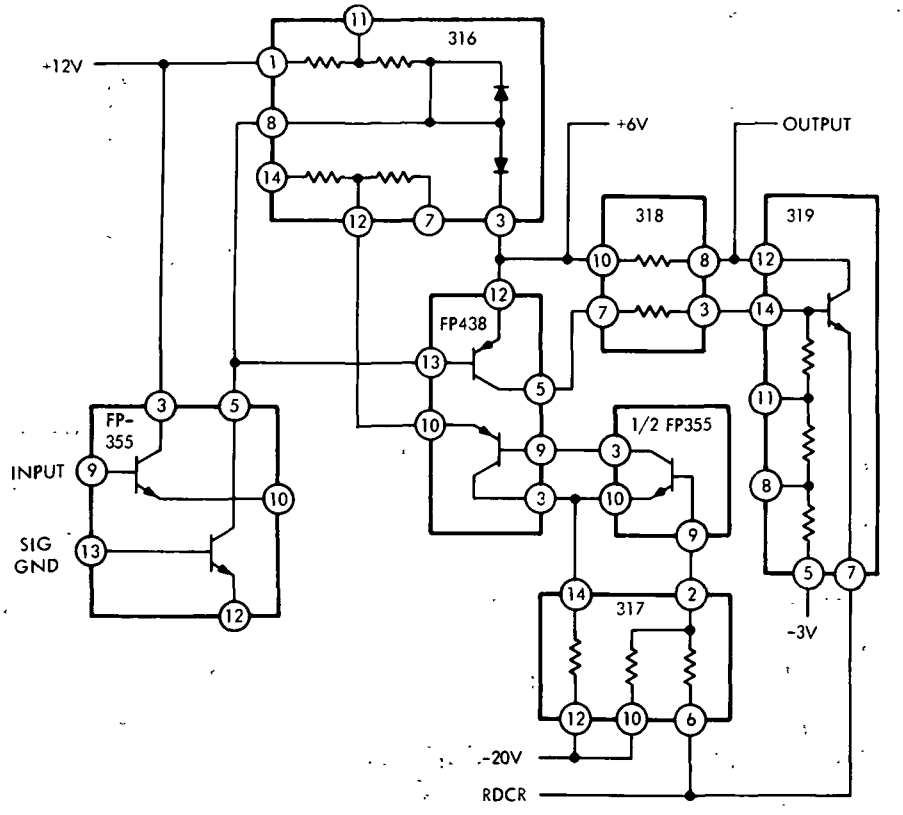


Figure A-25. Interface Buffer, IB

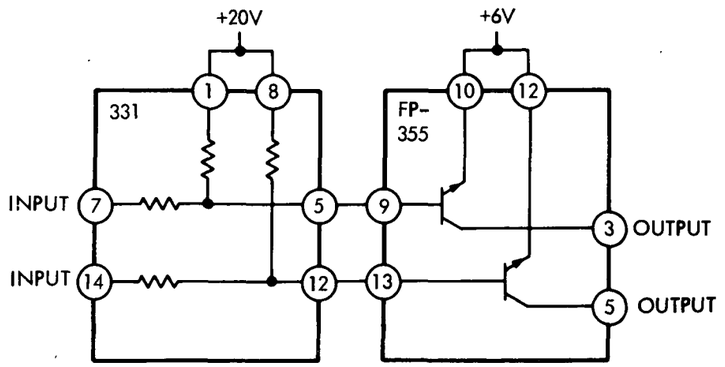


Figure A-26. Intermediate Driver, High Current, IDH

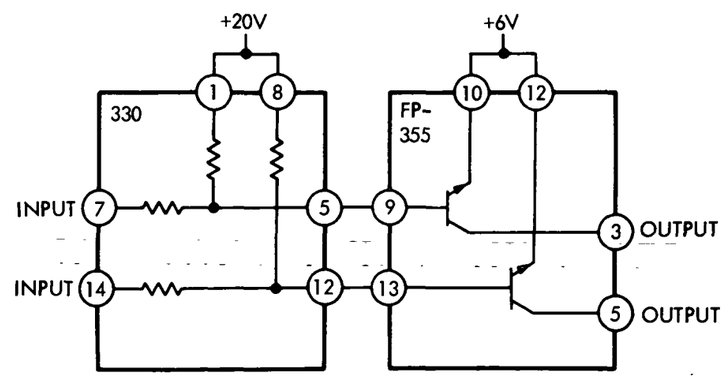


Figure A-27. Intermediate Driver, Low Current, IDL

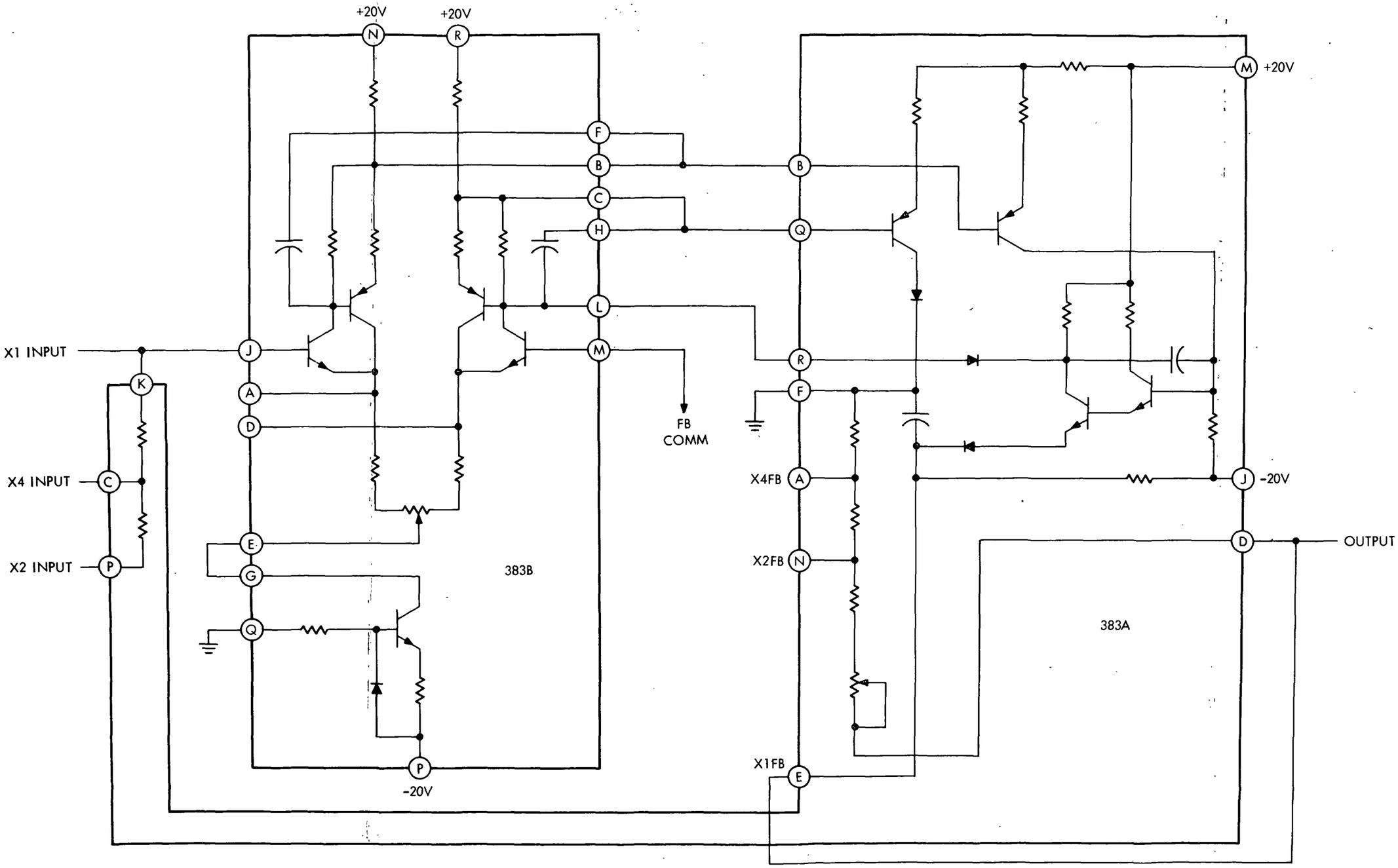


Figure A-28. Ladder Decoder Amplifier, LDA

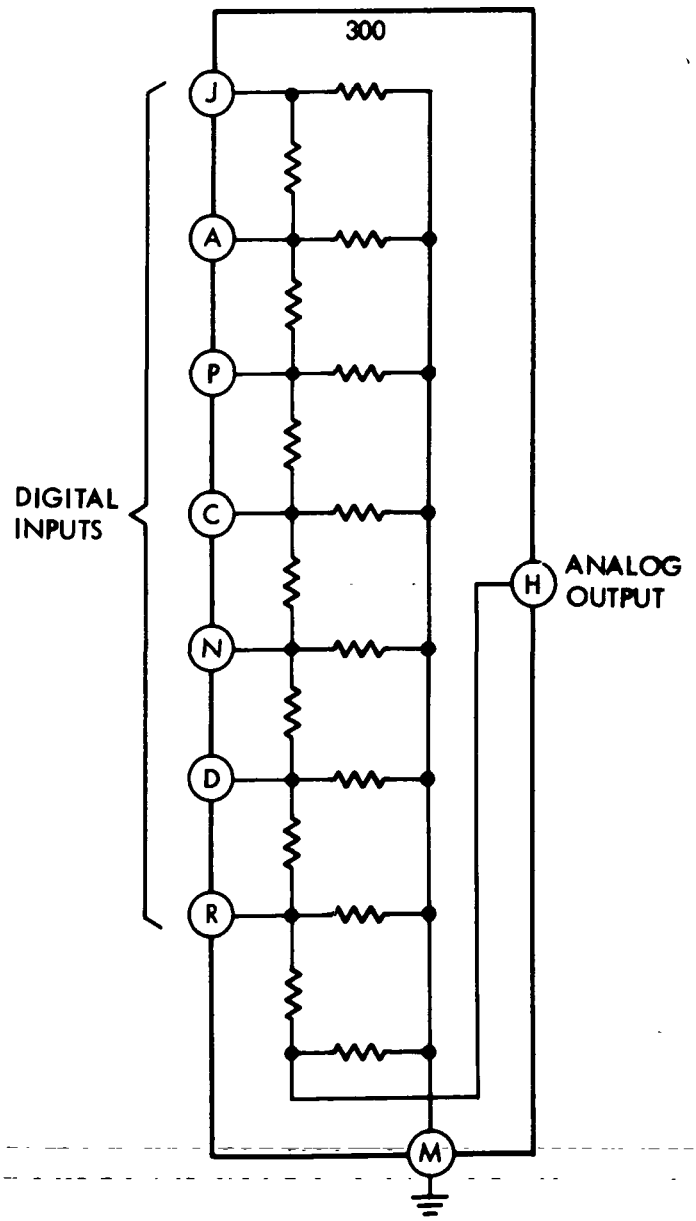


Figure A-29. Ladder Resistor Network, LRN

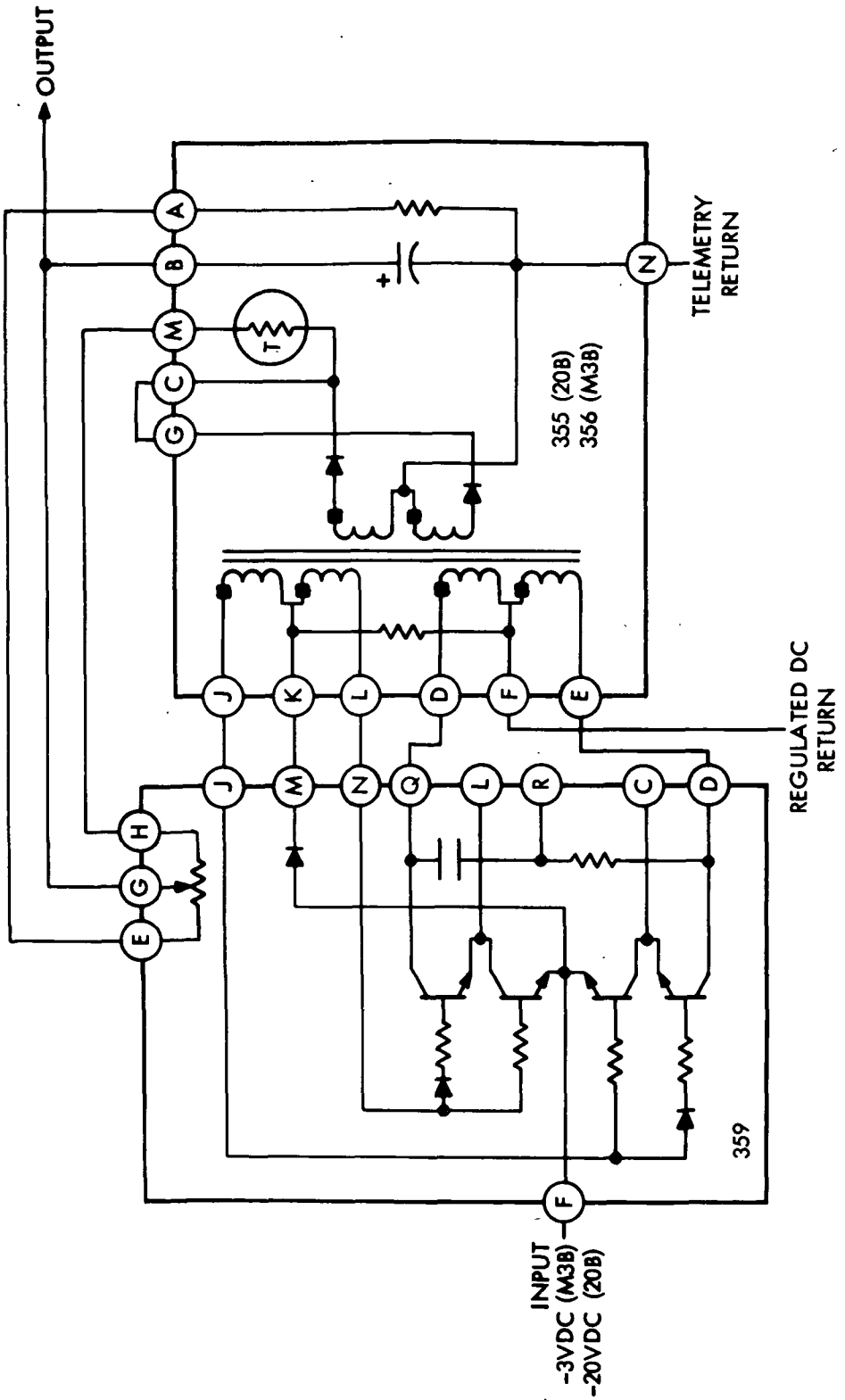


Figure A-30. Minus 3V or 20B Telemetry Buffer, M3B or 20B

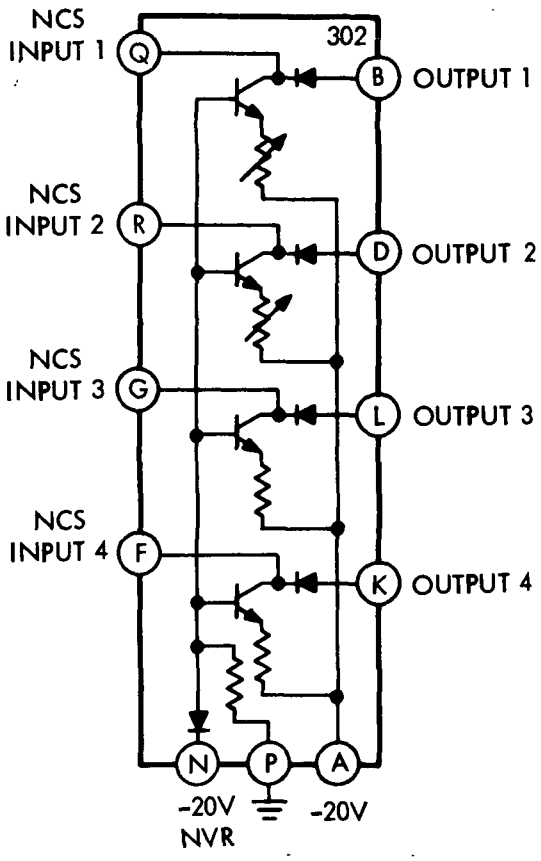


Figure A-31. Negative Current Generator, NCG

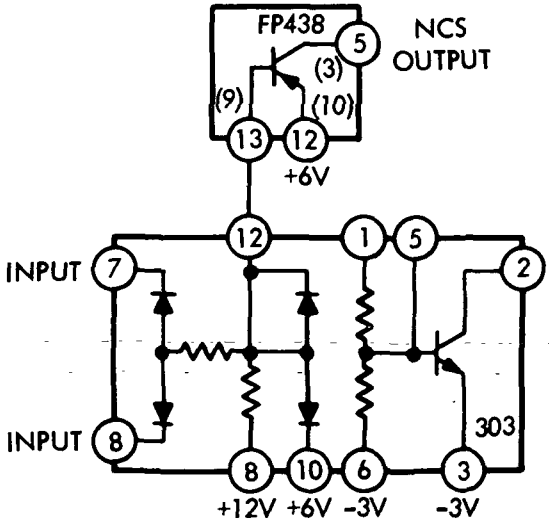


Figure A-32. Negative Current Switch, NCS

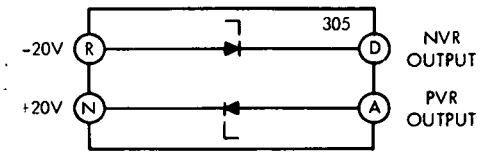


Figure A-33. Negative or Positive Voltage Reference, NVR or PVR

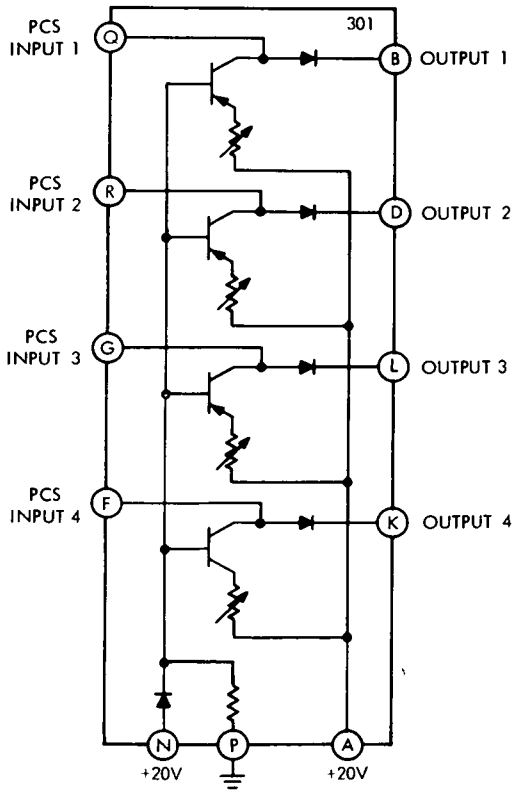


Figure A-34. Positive Current Generator, PCG

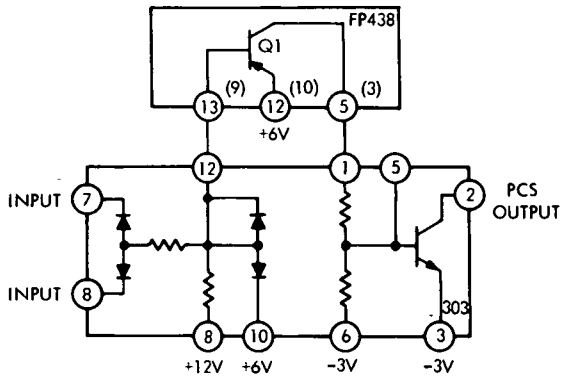


Figure A-35. Positive Current Switch, PCS

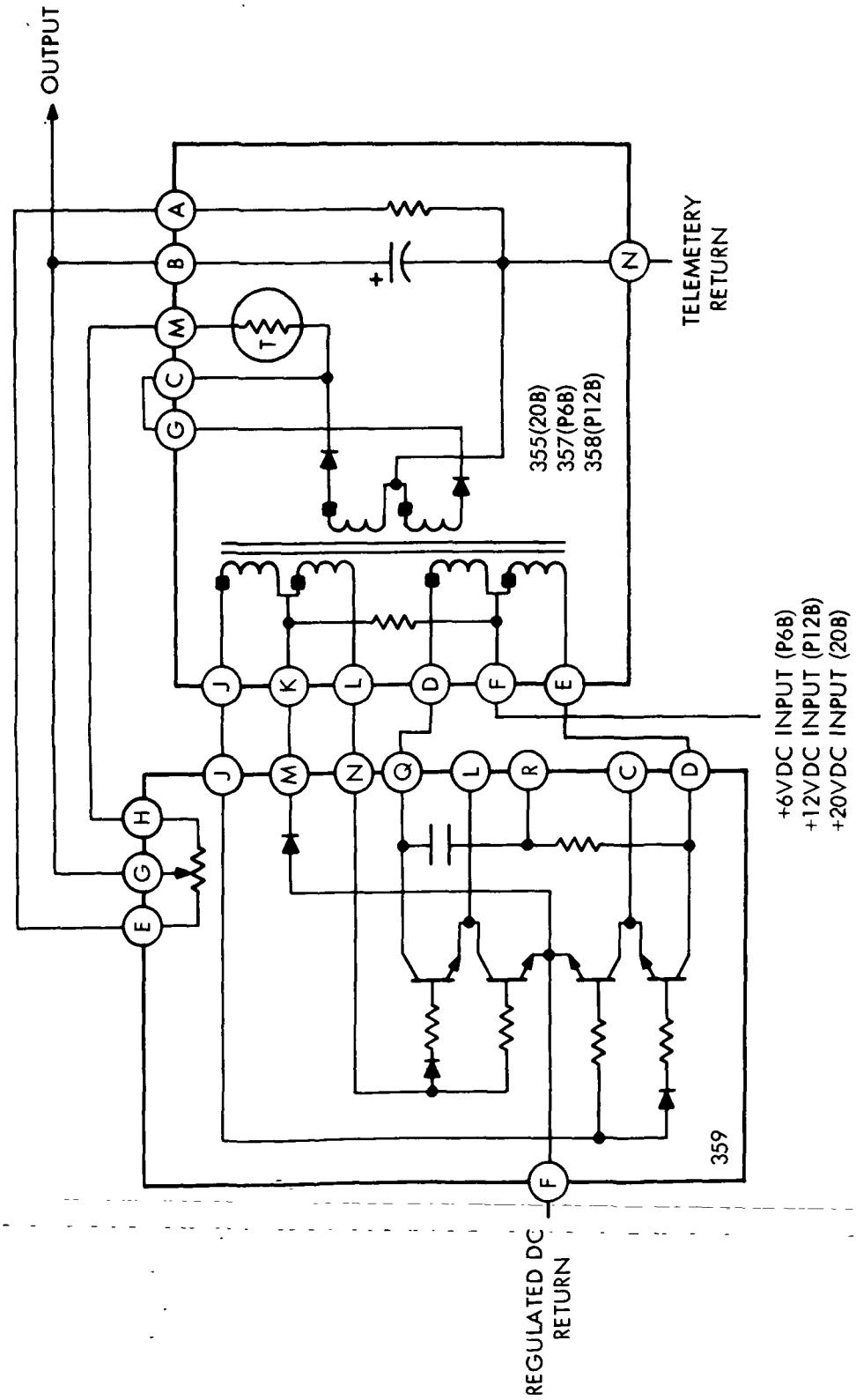


Figure A-36. Plus 6V, 12 and 20V Telemetry Buffers, P6B and P12B

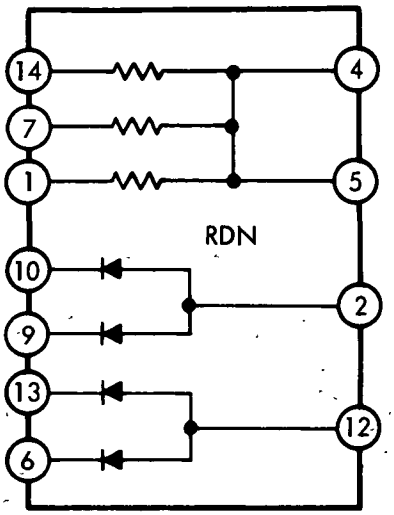


Figure A-37. Resistor Diode Network, RDN

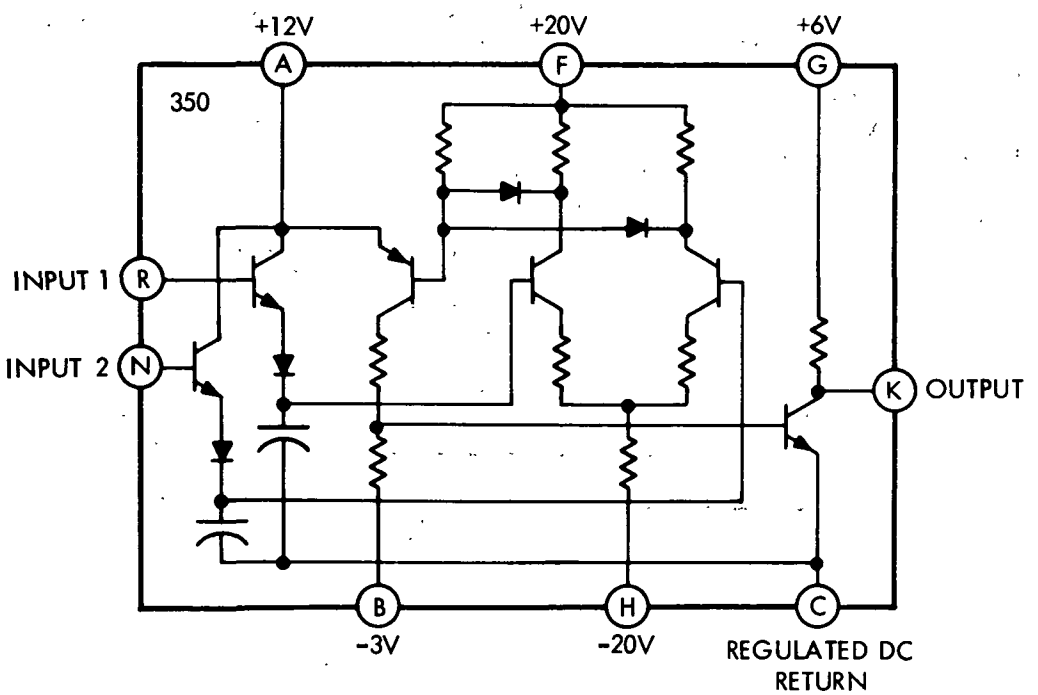


Figure A-38. Resolver Telemetry Buffer, RTB

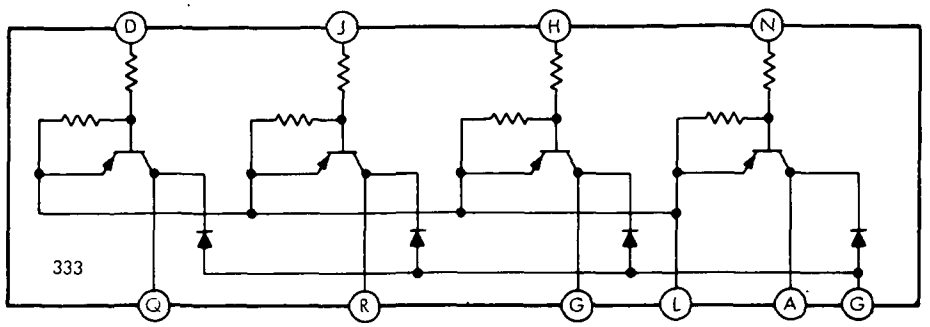


Figure A-39. Simplex Driver, High Current, SDH

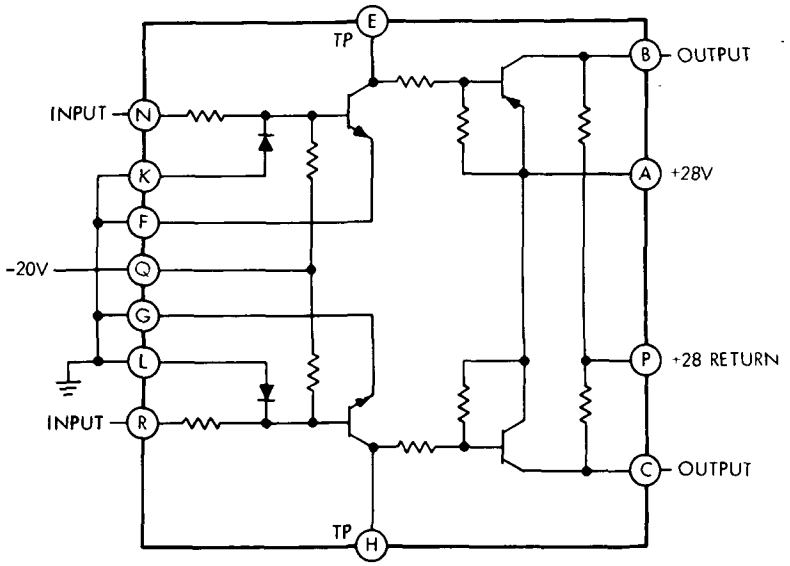


Figure A-40. Simplex Driver, Isolation, SDI

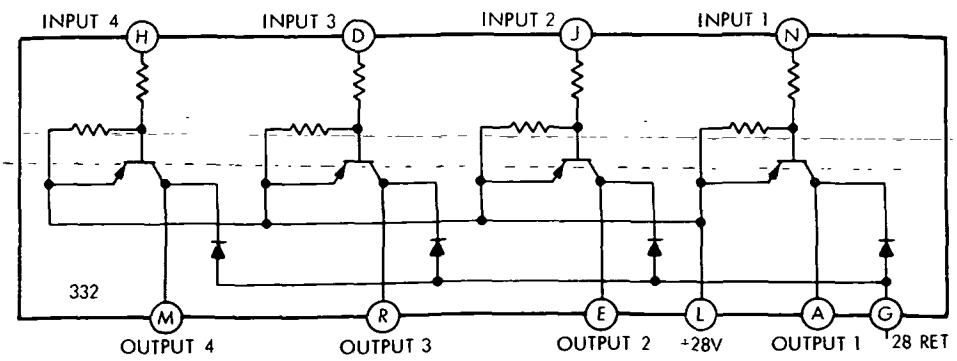


Figure A-41. Simplex Driver, Low Current, SDL

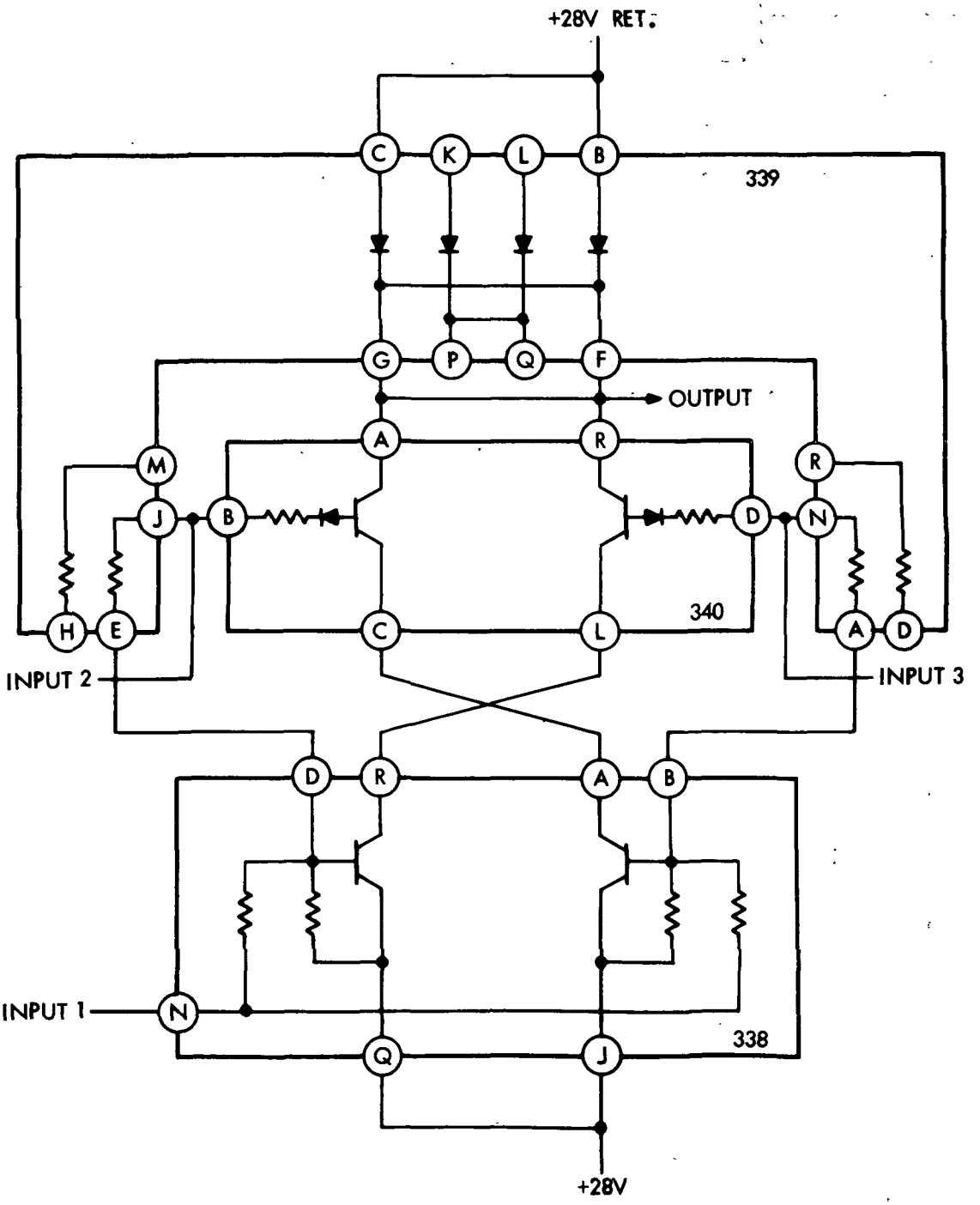


Figure A-42. TMR Driver, High Current, TDH

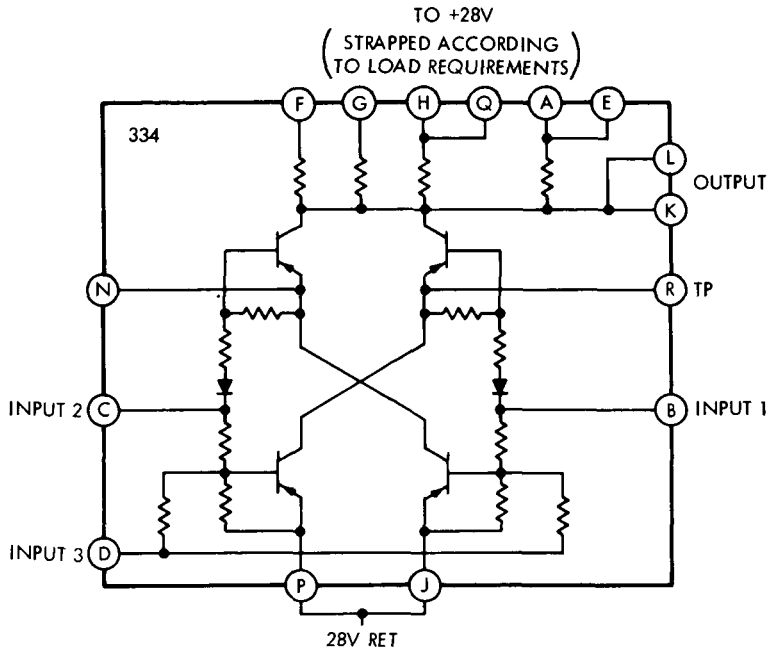


Figure A-43. TMR Driver, Low Current, TDL

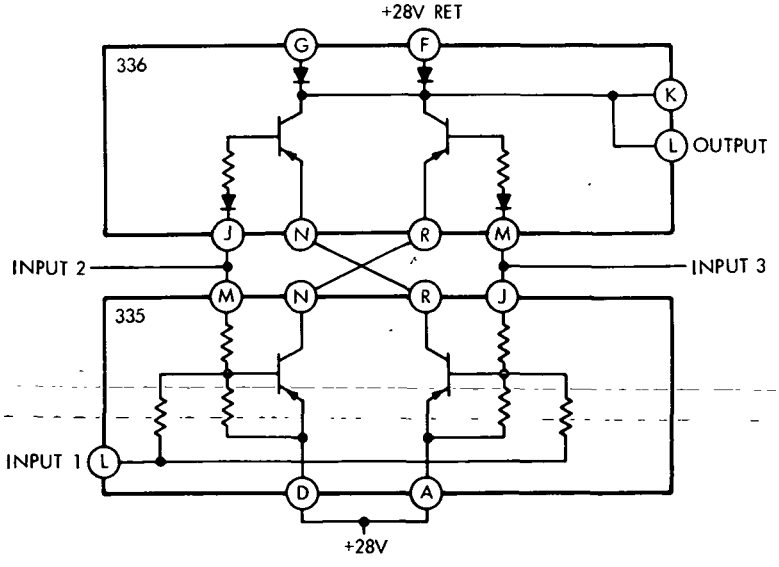


Figure A-44. TMR Driver, Medium Current, TDM

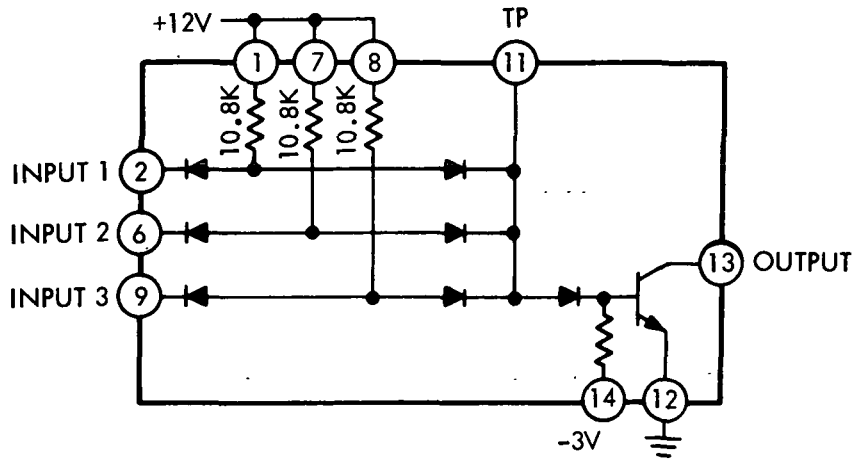


Figure A-45. TMR Voter, TMV

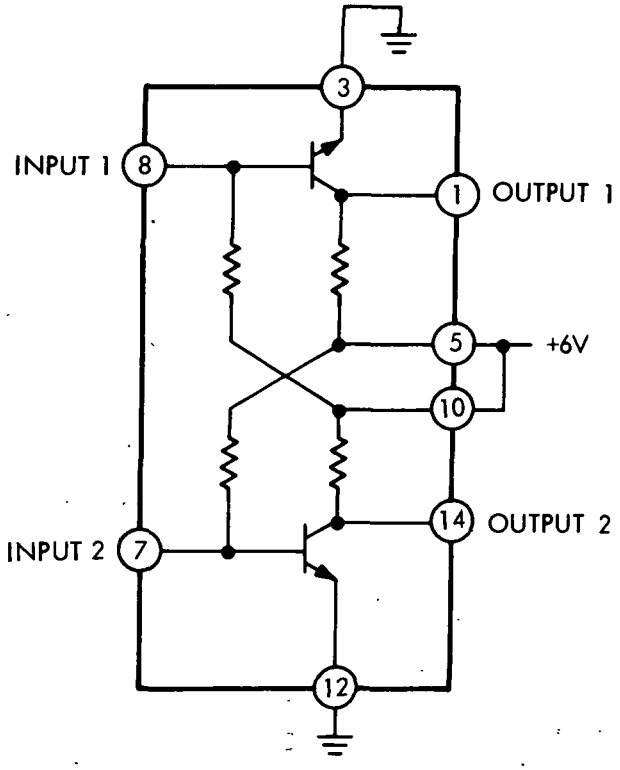


Figure A-46. Voter Inverter, VI

SYMBOL	DEFINITION
ABD	LATCH IN BIT GATE GENERATOR USED TO CONTROL LATCH AD
ACS	A CONVERTER SELECT
AD	LATCH IN BIT GATE GENERATOR USED TO DECODE BIT GATES DURING W AND X CLOCK TIMES
ADI	INVERTER USED TO INHIBIT INVALID TMR DISAGREEMENTS OCCURING DURING PHASE A
AI3	INTERFACE SIGNAL BETWEEN LVDC AND LVDA, GENERATED IN LVDC USED TO INPUT DATA TO LVDA.
ALR	ALTERNATE LADDER REGISTER
AQ	LATCH IN ACCELEROMETER PROCESSOR WHICH STORES THE Q INPUTS FROM THE OPTISYNS
AR	LATCH IN THE ACCELEROMETER PROCESSOR WHICH STORES THE R INPUTS FROM THE OPTISYNS AND CONTROLS ACCELEROMETER PROCESSOR OPERATION
ATBP	ANALOG TELEMETRY BUFFER PITCH
ATBR	ANALOG TELEMETRY BUFFER ROLL
ATBS	ANALOG TELEMETRY BUFFER SPARE
ATBY	ANALOG TELEMETRY BUFFER YAW
A1-9	INTERFACE SIGNAL BETWEEN LVDC AND LVDA ORIGINATING IN LVDC, ADDRESS REGISTER LATCH 1-9
A10-9D	LATCH WHICH REPOWERS INTERFACE ADDRESS REGISTER LATCH 1-9 OUTPUT FROM THE LVDC
A1EAM	LATCH LOCATED IN LVDC WHICH INDICATES ERROR IN EVEN MEMORIES
A1EBM	LATCH LOCATED IN LVDC WHICH INDICATES ERROR IN ODD MEMORIES
A1TLC	LATCH IN LVDC INDICATING TWO SIMULTANEOUS MEMORY ERRORS
A3CR-7CR	ADDRESS BIT 3-7 FROM A3D-A7D LATCH SET INTO COD REGISTER TRATCH FOR COD ADDRESSING AND CONTROL
A3RS	RESET STATE OF A3CR TRATCH IN COD REGISTER
BCS	B CONVERTER SELECT
BDI	INVERTER USED TO INHIBIT INVALID TMR DISAGREEMENTS OCCURING DURING PHASE B

SYMBOL	DEFINITION
BESO	BIPOLAR ELECTRONIC SWITCH OUTPUTS
BGTF1	BIT GATE THREE AND FOUR TIMING LATCH
BORL	BORROW LATCH USED FOR COD SUBTRACT OPERATION
BOR2-3	BORROW LATCH USED FOR TMR DELAY LINE CHANNEL 2-3 SUBTRACTION OPERATION
B01N-3N	TWO MEGACYCLE SQUARE WAVE ORIGINATING IN LVDC, CHANNEL 1-3
BRD01-26	BUFFER REGISTER LATCH 01-26
BRD01H	OUTPUT OF THE INTERMEDIATE LOW CURRENT DRIVER WHICH IS FED BY BRD01-26 LATCH
BRR1	INVERTER USED TO RESET BUFFER REGISTER LATCH BRD1 THROUGH BUFFER REGISTER LATCH BRD11
BRR2	INVERTER USED TO RESET BUFFER REGISTER LATCH BRD12 THROUGH BUFFER REGISTER LATCH BRD26
BR01-26	OUTPUT TO THE TELEMETRY TRANSMITTER FROM THE SIMPLEX LOW CURRENT DRIVER WHICH IS FED BY INTERMEDIATE DRIVER BRD01H-26H
BR01X-26X	INTERFACE OUTPUT TO THE RCA 110 FROM THE SIMPLEX DRIVER ISOLATION CIRCUIT WHICH IS FED BY SIMPLEX DRIVER BR01-26
BU1P-4P	COD OUTPUT USED TO STOP THE COD COUNTER WHEN COARSE GIMBAL ANGLE 1-4 IS ADDRESSED AS A BACK UP, IN CASE FINE GIMBAL ANGLE 1-4 FAILS
CA4	LATCH USED IN CROSS-OVER DETECTOR COUNTER A TO ASSURE PROPER OPERATION OF TT TRATCH
CB4	LATCH USED IN CROSS-OVER DETECTOR COUNTER B TO ASSURE PROPER OPERATION OF TT TRATCH
CCAS	COD COUNTER A SERIALIZER
CCA01-11	CROSS-OVER DETECTOR COUNTER A LATCH, POSITION 1-11
CCBS	COD COUNTER B SERIALIZER LATCH
CCB01-11	CROSS-OVER DETECTOR COUNTER B LATCH, POSITION 1-11
CCFH	LATCH WHICH EXCITES THE RESOLVER FREQUENCY SOURCES
CCFHC	RESOLVER FREQUENCY SOURCE CONTROL LATCH
CCR	INVERTER USED TO STOP COD COUNTER WHEN COD GROUP IS ADDRESSED

SYMBOL	DEFINITION
CCS	LATCH WHICH WILL START THE COD COUNTER BY A DECODED ADDRESS
CCSL	COD COUNTER SEQUENCE LATCH, WILL SEQUENCE SERIAL OUTPUTS OF COD COUNTERS IN A-B ORDER OR B-A ORDER
CDIF	COD COUNTER DIFFERENCE LATCH, WHOSE OUTPUT IS COD COUNTER A MINUS COD COUNTER B
CES01-19	COD ERROR SIGNAL 01-19 OUTPUT FROM RESOLVER TELEMETRY BUFFER CIRCUIT
CE01A-19A	OUTPUT FROM COD TO RESOLVER TELEMETRY BUFFER USED TO GENERATE COD ERROR SIGNAL
CE01B-19B	OUTPUT FROM COD TO RESOLVER TELEMETRY BUFFER USED TO GENERATE COD ERROR SIGNAL
CF	COD COUNTER CONTROL INVERTER, 2 MEGACYCLE PULSE TO STEP COD COUNTER
CGAP	COD OUTPUT USED TO STOP THE COD COUNTER WHEN COARSE GIMBAL ANGLE 1 OR 2 IS ADDRESSED
CGBP	COD OUTPUT USED TO STOP THE COD COUNTER WHEN COARSE GIMBAL ANGLE 3 OR 4 IS ADDRESSED
CG1-8	POSITIVE AND NEGATIVE CURRENT GENERATOR GROUP 1-8
CG1R-4R	COD OUTPUT USED TO START THE COD COUNTER WHEN COARSE GIMBAL ANGLE 1-4 IS ADDRESSED
CODE	ADDRESS LATCH USED TO SEND COD ERROR WORD TO THE TELEMETRY SYSTEM
CODG	ADDRESS LATCH DEFINING A COD OPERATION
CODRR	COD REGISTER RESET INVERTER
CODRS	COD MULTIPLEXER RESET INVERTER
COS	COSINE OUTPUT OF CROSS-OVER DETECTOR
CPR1	LADDER DECODER COMPARATOR OUTPUT
CPR2	DIGITAL TO ANALOG CONVERTER COMPARATOR OUTPUT
CRCA	ADDRESS LATCH FOR COMMAND RECEIVER AND RCA-110 INPUTS
CR11-2	COMMAND RECEIVER INTERRUPT LINE 1-2, OUTPUT OF A DISCRETE TRANSIENT PROTECTOR AND INPUT TO LOGIC

SYMBOL	DEFINITION
CR11X-2X	COMMAND RECEIVER INTERRUPT INTERFACE LINE 1-2 INPUT TO DISCRETE TRANSIENT PROTECTOR
CRT	LATCH USED TO CONTROL OPERATION OF COD MULTIPLEXER
CR01-14	INTERFACE INPUT LINE 01-14 FROM COMMAND RECEIVER
CSPX	PITCH ATTITUDE ERROR OUTPUT
CSRX	ROLL ATTITUDE ERROR OUTPUT
CSS1X-2X	SPARE 1-2 ATTITUDE ERROR OUTPUT
CST	SIGNAL EXTERNALLY GENERATED WHICH PERMITS SINGLE STEP OPERATION
CSYX	YAW ATTITUDE ERROR OUTPUT
C1GT-4GT	TRATCH WHICH DEFINES WHETHER THE INFORMATION IN DOM DELAY LINE CHANNEL 1-4 HAS BEEN TRANSMITTED BY TELEMETRY
C1R-4R	READ LATCH FOR CHANNEL 1-4 OF TMR DELAY LINE
C1RD-4RD	LATCH WHICH DELAYS INFORMATION INPUT FROM C1R-4R LATCH
DAINF	LATCH WHICH RECEIVES INPUT INFORMATION FROM THE ACCUMULATOR OR MEMORY OF THE LVDC
DARA	ADDRESS LATCH USED TO DEFINE AN INPUT OPERATION FROM THE LVDC TO AN LVDA REGISTER
DARO	ADDRESS LATCH USED TO DEFINE AN OUTPUT OPERATION TO THE LVDC
DATA	TMR SERIALIZER LATCH WHICH SENDS DATA TO THE LVDC
DCAL	DOM COUNTER ADVANCE LATCH
DCCA1-4	LATCH USED TO CONTROL CROSS-OVER DETECTOR COUNTER A LATCH 1-4
DCCB1-4	LATCH USED TO CONTROL CROSS-OVER DETECTOR COUNTER B LATCH 1-4
DC1R-4R	READ LATCH FOR DOM DELAY LINE CHANNEL 1-4
DC1S-4S	LATCH WHICH SELECTS DOM DELAY LINE CHANNEL 1-4 TO RECEIVE INPUT DATA
DDC1-2	CONTROL LATCH FOR DOM COUNTER LATCH 1-2
DDC1R-4R	LATCH WHICH DELAYS INFORMATION COMING FROM DC1R-4R LATCH
DDIHLT	OUTPUT OF DISAGREEMENT DETECTOR INVERTER ASSOCIATED WITH HALT INVERTER

SYMBOL	DEFINITION
DDIN	LATCH WHICH DELAYS INFORMATION COMING FROM DIN LATCH
DDIP	INVERTER INPUT TO DOM DELAY LINE
DDI01-10	OUTPUT OF DISAGREEMENT DETECTOR INVERTER 1-10
DDI01-10N	*INPUT TO DISAGREEMENT DETECTOR INVERTER 1-10*
DDLO	DOM DELAY LINE OUTPUT
DD11TP	DISAGREEMENT DETECTOR 11 TEST POINT
DD38TP	DISAGREEMENT DETECTOR 3B TEST POINT
DECAO	LADDER DECODER A OUTPUT
DECBO	LADDER DECODER B OUTPUT
DECO	LADDER DECODER OUTPUT
DECRET	LADDER DECODER RETURN
DECRO	LADDER REFERENCE DECODER OUTPUT
DIAD	ADDRESS LATCH WHICH SENDS DISCRETE INPUT INFORMATION TO LVDC
DIN	LATCH USED TO SELECT AND TRANSMIT INPUT DATA TO DOM DELAY LINE
DINF	LATCH WHICH DELAYS INFORMATION COMING FROM THE DAINF LATCH
DINP	INVERTER INPUT TO TMR DELAY LINE
DIN01-24	DISCRETE INPUT INTERFACE LINE 01-24, OUTPUT OF A DISCRETE TRANSIENT PROTECTOR AND INPUT TO LEVEL SHIFTING INVERTER
DIN01X-24X	DISCRETE INPUT INTERFACE LINE 01-24, INPUT TO DISCRETE TRANSIENT PROTECTOR
DISA	ADDRESS LATCH WHICH SENDS SPARE DISCRETE INPUT INFORMATION TO LVDC
DISD	DISAGREEMENT DETECTOR OUTPUT
DIST	DISAGREEMENT DETECTOR TEST POINT
DIS1-8	SPARE DISCRETE INPUT LINE 1-8, OUTPUT OF A DISCRETE TRANSIENT PROTECTOR AND INPUT TO LEVEL SHIFTING INVERTER
DIS1X-8X	SPARE DISCRETE INPUT INTERFACE LINE 1-8 INPUT TO DISCRETE TRANSIENT PROTECTOR
DLO	OUTPUT FROM TMR DELAY LINE TO LOGIC

SYMBOL	DEFINITION
DLS	ADDRESS LATCH WHICH SELECTS THE DOM DELAY LINE TO RECEIVE INFORMATION
DM01-2	DOM MULTIPLEXER LATCH USED DURING BIT GATES 01 AND 02
DM03A-14A	DOM MULTIPLEXER LATCH A USED DURING BIT GATE 03-14 FOR NORMAL OPERATION
DM2B-8B	DOM MULTIPLEXER LATCH 2B-8B USED ONLY DURING ERROR TIME READOUT OPERATION
DOM	DATA OUTPUT MULTIPLEXER
DOMC1-2	DOM CONTROL COUNTER LATCH POSITION 1-2
DOMD	DOM LATCH SELECTS DATA FROM 1 OF 4 DELAY LINE CHANNELS AND OUTPUTS IT TO TELEMETRY
DOMS	DOM SERIALIZER LATCH WHICH SERIALIZES THE DOM MULTIPLEXER
DOR	DISCRETE OUTPUT REGISTER ADDRESS LATCH USED TO RESET POSITIONS OF THE REGISTER INDIVIDUALLY
DOR01-13	DISCRETE OUTPUT REGISTER LATCH 01-13
DOR01H-13H	OUTPUT FROM THE INTERMEDIATE LOW CURRENT DRIVER FED BY DISCRETE OUTPUT REGISTER LATCH 01-13
DOS	DISCRETE OUTPUT REGISTER ADDRESS LATCH USED TO SET POSITIONS OF THE REGISTER INDIVIDUALLY
DO01-13	INPUT TO COMMAND RECEIVER FROM THE TMR LOW CURRENT DRIVER ASSOCIATED WITH DISCRETE OUTPUT REGISTER LATCH 1-13
DO2RCA	INPUT TO THE RCA-110 FROM THE SIMPLEX DRIVER ISOLATION CIRCUIT ASSOCIATED WITH DISCRETE OUTPUT REGISTER LATCH 2
DPBR	CONTROL LATCH FOR BUFFER REGISTER PARITY LATCH
DSAN	ZERO OUTPUT OF DOM SERIALIZER LATCH
DSBN	ZERO OUTPUT OF DOM SERIALIZER LATCH
DSD	LATCH WHICH DELAYS INFORMATION COMING FROM THE DOM SERIALIZER
DT	DOM DELAY LINE INPUT CONTROL TRATCH
DTPB	CONTROL LATCH FOR TELEMETRY PARITY BIT LATCH
ECSA	ERROR CLOCK SIGNAL LATCH A

SYMBOL	DEFINITION
ECSB	ERROR CLOCK SIGNAL LATCH B
EMA	ADDRESS LATCH WHICH SENDS ERROR MONITOR REGISTER TO LVDC
EMRG1-4	INVERTER GROUP 1-4 OF ERROR MONITOR REGISTER LATCH OUTPUTS
EMRS1-2	ERROR MONITOR RESET INVERTER 1-2
EM01-26	ERROR MONITOR REGISTER LATCH 1-26
EP01-13	OUTPUT OF DISAGREEMENT DETECTOR INVERTER 01-13 LOCATED IN LVDC
ERRS	INVERTER OUTPUT INDICATING ERROR
ETCC	ERROR TIME READOUT CONTROL LATCH
ETCR	ERROR TIME READOUT ADDRESS LATCH
ETSD	ERROR TIME READOUT CONTROL LATCH
ETTS	ERROR TIME READOUT STORAGE INITIATION LATCH
FG1P-4P	COD OUTPUT USED TO STOP THE COD COUNTER WHEN FINE GIMBAL ANGLE 1-4 IS ADDRESSED
FG1R-4R	COD OUTPUT USED TO START THE COD COUNTER WHEN FINE GIMBAL ANGLE 1-4 IS ADDRESSED
FPA	DISAGREEMENT DETECTOR INVERTER FLAT PACK INPUT A
GCSYN	INTERFACE INPUT LINE FROM RCA-110 LEVEL SHIFTED AND INPUT TO LOGIC, USED TO SYNCHRONIZE OR STEP THE DOM
GCSYNC	OUTPUT OF DISCRETE TRANSIENT PROTECTOR AND INPUT TO LEVEL SHIFTING INVERTER, SYNCHRONIZING SIGNAL FOR DOM
GCSYNCX	INTERFACE LINE FROM RCA-110 TO DISCRETE TRANSIENT PROTECTOR USED TO SYNCHRONIZE OR STEP THE DOM
GC01-14	INTERFACE INPUT LINE 01-14 FROM RCA-110
G1D-7D	BIT GATE GENERATOR LATCH 1-7
G5	INTERFACE LINE, LVDC BIT GATE GENERATOR LATCH 5 USED TO SYNCHRONIZE LVDA BIT GATE GENERATOR
G5GC	INVERTER OUTPUT WHICH COMPLEMENTS INTERFACE LINE FROM LVDC
HALT	INTERFACE OUTPUT LINE USED TO HALT LVDC
HCA1-5	INPUT 1-5 TO ALTITUDE ERROR HOLD CAPACITOR ASSOCIATED WITH DECODER A

SYMBOL	DEFINITION
HCA1A-5A	INPUT 1A-5A TO ALTITUDE ERROR HOLD CAPACITOR ASSOCIATED WITH DECODER A
MCB1-5	INPUT 1-5 TO ALTITUDE ERROR HOLD CAPACITOR ASSOCIATED WITH DECODER B
HCB1A-5A	INPUT 1A-5A TO ALTITUDE ERROR HOLD CAPACITOR ASSOCIATED WITH DECODER B
HLT	INTERFACE LINE FROM TEST EQUIPMENT AND RCA-110, INPUT TO LEVEL SHIFTER AND INVERTER, USED TO HALT LVDC
HLTX	INTERFACE LINE FROM TEST EQUIPMENT AND RCA-110, INPUT TO DISCRETE TRANSIENT PROTECTOR USED TO HALT LVDC
HS1P-4P	COD OUTPUT USED TO STOP THE COD COUNTER WHEN THE HORIZON SEEKER 1-4 IS ADDRESSED
HS1PA-4PA	HORIZON SEEKER 1-4 RESOLVER OUTPUT, PHASE A
HS1PB-4PB	HORIZON SEEKER 1-4 RESOLVER OUTPUT, PHASE B
HS1R-4R	COD OUTPUT USED TO START THE COD COUNTER WHEN THE HORIZON SEEKER 1-4 IS ADDRESSED
HS1RTN-4RTN	HORIZON SEEKER 1-4 RETURN
HS1SHD-4SHD	SHIELD FOR HORIZON SEEKER 1-4 COD INPUT LINES
ICR	LATCH WHICH ADDRESSES INTERNAL CONTROL REGISTER TO RECEIVE INFORMATION
ICR01-13	INTERNAL CONTROL REGISTER LATCH 01-13
ICS	INTERFACE INPUT LINE FROM RCA-110 LEVEL SHIFTED AND INVERTED, USED TO BLOCK COMMAND RECEIVER INPUTS
ICSD	INVERTER, ONE OUTPUT ADDRESSES THE COMMAND RECEIVER INPUT DATA LINES DURING CRCA ADDRESS
INFLA	INVERTER, ONE OUTPUT SIGNIFIES INFO LATCH IS AVAILABLE TO TRANSFER DOM OUTPUTS
INFO	LATCH WHICH DELAYS INFORMATION ORIGINATING IN LVDC ACCUMULATOR OR MEMORY, INPUT TO LVDA REGISTERS
INTC	INTERFACE OUTPUT LATCH WHICH INTERRUPTS LVDC
INTR1-7	INTERRUPT 1-7 INTERFACE LINE OUTPUT OF DISCRETE TRANSIENT PROTECTOR AND INPUT TO LOGIC

SYMBOL	DEFINITION
INTR1X-7X	INTERRUPT 1-7 INTERFACE LINE INPUT TO DISCRETE TRANSIENT PROTECTOR
ITS	INTERRUPT TIMING SIGNAL LATCH
LCB1-2	LIMIT CHECK LATCH 1-2 FOR COD COUNTER SUBTRACT OPERATION
LGA	ADDRESS LATCH USED TO DEFINE INPUT OPERATIONS TO LADDER REGISTER
LP	INTERTER, 500KC SIGNAL INPUT TO ATTITUDE ERROR CIRCUITRY WHEN ANY LADDER IS ADDRESSED
LPAG2N	INVERTER USED TO CONTROL INPUT TO LADDER PULSE COUNTER
LRR	LADDER REGISTER RESET INVERTER
LRRP	CONTROL LATCH FOR 500KC PULSE GENERATION TO ATTITUDE ERROR CIRCUITRY
LR1-9	LADDER REGISTER LATCH 1-9
LTR	ADDRESS LATCH USED TO LOAD TELEMETRY REGISTERS
LTRD	LATCH WHICH CONTROLS LTR LATCH DURING DOM OPERATION
L1A	PITCH LADDER ADDRESS LATCH
L1P	INVERTER, 500KC SIGNAL INPUT TO ATTITUDE ERROR CIRCUITRY WHEN PITCH LADDER IS ADDRESSED
L2A	ROLL LADDER ADDRESS LATCH
L2P	INVERTER, 500KC SIGNAL INPUT TO ATTITUDE ERROR CIRCUITRY WHEN ROLL LADDER IS ADDRESSED
L3A	YAW LADDER ADDRESS LATCH
L3P	INVERTER, 500KC SIGNAL INPUT TO ATTITUDE ERROR CIRCUITRY WHEN YAW LADDER IS ADDRESSED
L4A-5A	SPARE 1-2 LADDER ADDRESS LATCH
L4P-5P	INVERTER, 500KC SIGNAL INPUT TO ATTITUDE ERROR CIRCUITRY WHEN SPARE 1-2 LADDER IS ADDRESSED
MBYPD	ADDRESS LATCH USED FOR SERIAL OUTPUTS TO LVDC WHICH BY-PASS THE TMR MULTIPLEXER
MCFT	TRATCH USED TO DEFINE MINOR LOOP OF LVDC PROGRAM AND TO FORCE FINE GIMBAL ANGLE 1 ADDRESS INTO THE COD REGISTER AT BEGINNING OF MINOR LOOP.

SYMBOL	DEFINITION
MLA	GENERAL ADDRESS LATCH FOR CONTROL OF TMR MULTIPLEXER
ML03-14	TMR MULTIPLEXER LATCH USED AT BIT GATE 03-14
ML1-2	TMR MULTIPLEXER LATCH USED AT BIT GATES 1 AND 2
MODA	LATCH WHICH ADDRESSES MODE REGISTER TO RECEIVE INFORMATION FROM LVDC
MODRR	MODE REGISTER RESET INVERTER
MODR1-6	MODE REGISTER LATCH 1-6
MODR1H-6H	OUTPUT OF INTERMEDIATE LOW CURRENT DRIVER WHICH IS FED BY MODR1-6
MOD1-6	INPUT TO RCA-110 FROM SIMPLEX LOW CURRENT DRIVER ASSOCIATED WITH MODE REGISTER LATCH 1-6
NCS1-8	NEGATIVE CURRENT SOURCE 1-8 OF LADDER DECODER
NVRO	LADDER NEGATIVE VOLTAGE REFERENCE OUTPUT
N03TLM	NEGATIVE 3 VOLT POWER SUPPLY ANALOG TELEMETRY SIGNAL
N20TLM	NEGATIVE 20 VOLT POWER SUPPLY ANALOG TELEMETRY SIGNAL
OCINT	ORBITAL CHECKOUT INTERRUPT INTERFACE LINE ORIGINATING IN DDAS
OCR	ORBITAL CHECKOUT ADDRESS DECODE LATCH
OCRH	OUTPUT OF INTERMEDIATE LOW CURRENT DRIVER ASSOCIATED WITH ORBITAL CHECKOUT ADDRESS LATCH
OCRX	OUTPUT OF TMR LOW CURRENT DRIVER ASSOCIATED WITH ORBITAL CHECKOUT ADDRESS LATCH
PAA	PHASE GENERATOR LATCH A
PABG1	PHASE A BIT GATE 1 TIMING LATCH
PARS	INVERTER, RESET SIGNAL OCCURING DURING PHASE A
PB	PHASE GENERATOR LATCH B IN LVDC USED TO SYNCHRONIZE PHASE GENERATOR
PBA	PHASE GENERATOR LATCH B
PBGC	INVERTER OUTPUT WHICH COMPLEMENTS INTERFACE LINE FROM LVDC
PBG2	PHASE B BIT GATE 2 TIMING LATCH

SYMBOL	DEFINITION
PBR	PARITY OF BUFFER REGISTER LATCH
PCA	PHASE GENERATOR LATCH C
PCAO	PITCH LADDER CONVERTER A OPERATING
PCBO	PITCH LADDER CONVERTER B OPERATING
PCG2	PHASE C BIT GATE 2 TIMING LATCH
PCINF	LATCH USED TO TRANSFER INFORMATION FROM LVDC TO LVDA REGISTERS DURING PHASE C
PCRN	ZERO OUTPUT OF START PRECONDITION LATCH USED IN COD MULTIPLEXER
PCR1-4	ONE OUTPUT OF START PRECONDITION LATCH USED IN COD MULTIPLEXER
PCS1-8	POSITIVE CURRENT SOURCE 1-8 OF LADDER DECODER
PIO	DECODED PROCESS INPUT-OUTPUT OPERATION ORIGINATING IN LVDC
PIOD	LATCH USED TO REPOWER PIO INTERFACE LINE FROM LVDC
PSTPN	ZERO OUTPUT OF STOP PRECONDITION LATCH USED IN COD MULTIPLEXER
PSTP1-4	ONE OUTPUT OF STOP PRECONDITION LATCH USED IN COD MULTIPLEXER
PS1A-6A	POWER SUPPLY DIGITAL TELEMETRY INPUT SIGNAL 1A-6A
PS1B-6B	POWER SUPPLY DIGITAL TELEMETRY INPUT SIGNAL 1B-6B
PVRO	LADDER POSITIVE VOLTAGE REFERENCE OUTPUT
P06TLM	LVDA +6 VOLT ANALOG TELEMETRY SIGNAL
P12TLM	LVDA +12 VOLT ANALOG TELEMETRY SIGNAL
P20TLM	LVDA +20 VOLT ANALOG TELEMETRY SIGNAL
P6STLM	LVDC +6 VOLT ANALOG TELEMETRY SIGNAL
QB	OUTPUT OF INTERFACE BUFFER CIRCUIT TO THE ACCELEROMETER PROCESSOR, LEVEL SHIFTED ACCELEROMETER Q PHASE B INPUT
QBP	Q OUTPUT FROM OPTISYNS TO INTERFACE BUFFER CIRCUIT, USED IN ACCELEROMETER PROCESSOR AT PHASE B TIME
QC	OUTPUT OF INTERFACE BUFFER CIRCUIT TO THE ACCELEROMETER PROCESSOR, LEVEL SHIFTED ACCELEROMETER Q PHASE C INPUT

SYMBOL	DEFINITION
QCP	Q OUTPUT FROM OPTISYNS TO INTERFACE BUFFER CIRCUIT, USED IN ACCELEROMETER PROCESSOR AT PHASE C TIME
QRARTN	ACCELEROMETER RETURN FOR TMR CHANNEL A
QRBRTN	ACCELEROMETER RETURN FOR TMR CHANNEL B
QRCRTN	ACCELEROMETER RETURN FOR TMR CHANNEL C
RB	OUTPUT OF INTERFACE BUFFER CIRCUIT TO THE ACCELEROMETER PROCESSOR, LEVEL SHIFTED ACCELEROMETER R PHASE B INPUT
RBP	R OUTPUT FROM OPTISYNS TO INTERFACE BUFFER CIRCUIT, USED IN ACCELEROMETER PROCESSOR AT PHASE B TIME
RC	OUTPUT OF INTERFACE BUFFER CIRCUIT TO THE ACCELEROMETER PROCESSOR, LEVEL SHIFTED ACCELEROMETER R PHASE C INPUT
RCAO	ROLL LADDER CONVERTER A OPERATING
RCBO	ROLL LADDER CONVERTER B OPERATING
RCP	R OUTPUT FROM OPTISYNS TO INTERFACE BUFFER CIRCUIT, USED IN ACCELEROMETER PROCESSOR AT PHASE C TIME
RECA-C	ONE-HALF MILLISECOND FREQUENCY GENERATOR LATCH A-C
RESM	BIT GATE 1 AND 2 TIMING LATCH USED PRIMARILY TO RESET MULTIPLEXER LATCHES
REXC	ONE-HALF MILLISECOND FREQUENCY GENERATOR CONTROL LATCH
REXCC	ONE-HALF MILLISECOND FREQUENCY GENERATOR CONTROL LATCH
RE1EX-2EX	OUTPUT OF RESOLVER FREQUENCY SOURCE 1-2
RE1RTN-2RTN	RESOLVER FREQUENCY SOURCE 1-2 RETURN SIGNAL
RFSRTN	COD RETURN SIGNAL
RFSRTN1-8	RESOLVER FREQUENCY SOURCE RETURN
RR1PA	R RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 4.PHASE A
RR1PB	R RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 4 PHASE B
RR2PA	R RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 4 PHASE A
RR2PB	R RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 4 PHASE B
RTRR	REAL TIME REGISTER RESET

SYMBOL	DEFINITION
RTR1-5	REAL TIME REGISTER LATCH 1-5
RTR1H-5H	OUTPUT OF INTERMEDIATE LOW CURRENT DRIVER ASSOCIATED WITH REAL TIME REGISTER LATCH 1-5
RT1-5	OUTPUT OF SIMPLEX LOW CURRENT DRIVER ASSOCIATED WITH REAL TIME REGISTER LATCH 1-5 TO TELEMETRY TRANSMITTER
RT1X	OUTPUT OF SIMPLEX DRIVER ISOLATION CIRCUIT ASSOCIATED WITH REAL TIME REGISTER LATCH 1 TO RCA-110
SCA-B	SELECT CONVERTER A-B LATCH ASSOCIATED WITH ATTITUDE ERROR CIRCUITRY
SIG-RET	SIGNAL RETURN
SIGRET	SIGNAL RETURN
SIN	SINE OUTPUT OF CROSS-OVER DETECTOR
SINTA-C	ONE OUTPUT OF INTERRUPT SERIALIZER LATCH
SINTN	ZERO OUTPUT OF INTERRUPT SERIALIZER LATCH
SP1P-6P	COD OUTPUT USED TO STOP THE COD COUNTER WHEN SPARE 1-6 IS ADDRESSED
SP1R-6R	COD OUTPUT USED TO START THE COD COUNTER WHEN SPARE 1-6 IS ADDRESSED
SSA	ADDRESS LATCH USED TO SEND 8 SWITCH SELECTOR FEEDBACK LINES TO LVDA
SSDO	SWITCH SELECTOR REGISTER AND DISCRETE OUTPUT REGISTER ADDRESS LATCH USED FOR DOM TELEMETRY
SSEP	LATCH USED TO INHIBIT INTERRUPT REGISTER READ WORD FROM BEING SENT VIA DOM TELEMETRY WHEN CAUSED BY SWITCH SELECTOR INTERRUPT
SSFB1-8	SWITCH SELECTOR FEEDBACK LINE 1-8 INPUT TO LEVEL SHIFTER AND INVERTER
SSFB1X-8X	SWITCH SELECTOR FEEDBACK LINE 1-8 INPUT TO DISCRETE TRANSIENT PROTECTOR
SSIT	SWITCH SELECTOR INTERRUPT TRATCH
SSR	SWITCH SELECTOR REGISTER ADDRESS LATCH
SSRR	SWITCH SELECTOR REGISTER RESET INVERTER
SSR01-15	SWITCH SELECTOR REGISTER LATCH 1-15

SYMBOL	DEFINITION
SSR01H-15H	OUTPUT OF INTERMEDIATE LOW CURRENT DRIVER ASSOCIATED WITH SWITCH SELECTOR REGISTER LATCH 1-15
SS01-15	OUTPUT OF CURRENT DRIVER ASSOCIATED WITH SWITCH SELECTOR REGISTER LATCH 1-15
STP	LATCH USED TO CONTROL OPERATION OF COD MULTIPLEXER
SYNCP	INVERTER, SYNCHRONIZING OR STEPPING SIGNAL TO DOM
SYNCPN	INVERTER, COMPLEMENT OF SYNCP
S1CAO	SPARE 1 LADDER CONVERTER A OPERATING
S1CBO	SPARE 1 LADDER CONVERTER B OPERATING
S2CAO	SPARE 2 LADDER CONVERTER A OPERATING
S2CBO	SPARE 2 LADDER CONVERTER B OPERATING
TAGRR	TAG REGISTER RESET INVERTER
TAGR1-8	TAG REGISTER LATCH 1-8
TAGR1H-8H	OUTPUT OF INTERMEDIATE LOW CURRENT DRIVER ASSOCIATED WITH TAG REGISTER LATCH 1-8
TAGS	TAG SERIALIZER LATCH
TAG1-8	OUTPUT OF SIMPLEX LOW CURRENT DRIVER ASSOCIATED WITH TAG REGISTER LATCH 1-8 TO TELEMETRY TRANSMITTER
TAG1X-8X	OUTPUT OF SIMPLEX DRIVER ISOLATION CIRCUIT ASSOCIATED WITH TAG REGISTER LATCH 1-8 TO RCA-110
TCW	DOM LATCH USED TO SIGNIFY TELEMETRY OF WORD ORIGINATING IN LVDC
TC2A-3A	TMR DELAY LINE CHANNEL 2-3 ADDRESS LATCH
TELREF	TELEMETRY REFERENCE SIGNAL
TE1-3	LABORATORY TEST EQUIPMENT INPUT LINE 1-3
TG1N-2N	ZERO OUTPUT OF TAG SERIALIZER LATCH
TI	TIMED INTERRUPT INITIATION LATCH
TLM	ADDRESS LATCH INDICATING A COMPUTER TELEMETRY OPERATION
TLMGRD	TELEMETRY RETURN SIGNAL

SYMBOL	DEFINITION
TPB	TELEMETRY PARITY BIT GENERATOR LATCH
TPBH	OUTPUT OF INTERMEDIATE LOW CURRENT DRIVER ASSOCIATED WITH TELEMETRY PARITY BIT LATCH
TPBX	OUTPUT OF SIMPLEX LOW CURRENT DRIVER ASSOCIATED WITH TELEMETRY PARITY BIT LATCH TO TELEMETRY TRANSMITTER
TP01-18	TEST POINT 01-18
TRP	DOM LATCH INDICATING VALID TRANSMISSION OF A WORD FROM BUFFER REGISTER TO TELEMETRY TRANSMITTER
TRPC	CONTROL LATCH ASSOCIATED WITH TRP LATCH
TRSV	TRANSFER REGISTER SERIAL OUTPUT LATCH LOCATED IN LVDC
TSA	DIGITAL DATA ACQUISITION SYSTEM ADDRESS LATCH USED TO INPUT INFORMATION TO LVDC
TSYN	INVERSION OF SYNCHRONIZING OR STEPPING SIGNAL INPUT TO DOM FROM TELEMETRY TRANSMITTER
TSYNC	SYNCHRONIZING OR STEPPING SIGNAL INPUT TO DOM INTERFACE BUFFER CIRCUIT FROM TELEMETRY TRANSMITTER
TSYNS	SYNCHRONIZING OR STEPPING SIGNAL OUTPUT FROM INTERFACE BUFFER AND INPUT TO DOM LOGIC
TS01-10	DIGITAL DATA ACQUISITION SYSTEM INTERFACE INPUT LINE 01-10
TT	TRANSITION TRATCH BETWEEN DOUBLE LATCH AND TRATCH STAGES OF THE COD COUNTER
VC	LVDA STATIC RETURN LINE
VEE	+28 VOLT DC
V1	+06 VOLT DC
V1COMP	+6 VOLT DC ORIGINATING IN LVDC
V20	+20 VOLTS DC
V3	-3 VOLTS DC
V4	CHANNEL SWITCHING +6 VOLTS DC
V5	CHANNEL SWITCHING +12 VOLTS DC
V7	-20 VOLTS DC

SYMBOL	DEFINITION
WDA	W CLOCK PULSE DRIVER GENERATED IN LVDC AND INPUT TO LVDA
W1-8	W CLOCK PULSE DRIVER OUTPUT 1-8
XDA	X CLOCK PULSE DRIVER GENERATED IN LVDC AND INPUT TO LVDA
XR1PA	X RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 1 PHASE A
XR1PB	X RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 1 PHASE B
XR2PA	X RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 1 PHASE A
XR2PB	X RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 1 PHASE B
X1-8	X CLOCK PULSE DRIVER OUTPUT 1-8
YCAO	YAW LADDER CONVERTER A OPERATING
YCBO	YAW LADDER CONVERTER B OPERATING
YDA	Y CLOCK PULSE DRIVER GENERATED IN LVDC AND INPUT TO LVDA
YR1PA	Y RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 2 PHASE A
YR1PB	Y RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 2 PHASE B
YR2PA	Y RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 2 PHASE A
YR2PB	Y RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 2 PHASE B
Y1-8	Y CLOCK PULSE DRIVER OUTPUT 1-8
ZDA	Z CLOCK PULSE DRIVER GENERATED IN LVDC AND INPUT TO LVDA
ZERW	INVERTER, USED TO WRITE ZEROES INTO DOM DELAY LINE AT PREDEFINED TIMES
ZR1PA	Z RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 3 PHASE A
ZR1PB	Z RESOLVER OUTPUT FOR FINE GIMBAL ANGLE 3 PHASE B
ZR2PA	Z RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 3 PHASE A
ZR2PB	Z RESOLVER OUTPUT FOR COARSE GIMBAL ANGLE 3 PHASE B
Z1-8	Z CLOCK PULSE DRIVER OUTPUT 1-8
500KC	LATCH USED TO GENERATE 500KC PULSE

INDEX

INDEX (Cont)

P (cont)

R

S

T

U

V

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