HT8 MCU 24-bit Delta Sigma A/D Converter Application Note

D/N: AN0437E

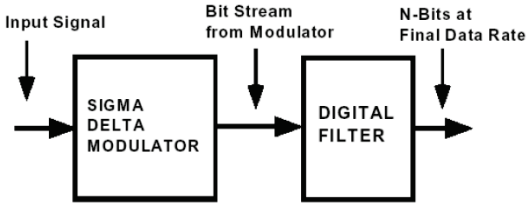
Introduction

The Delta Sigma A/D converter forms a basic and necessary component of the signal sampling and processing system designer's toolkit. The purpose of this article is to give readers a background into the fundamental principles of the Delta Sigma A/D converter topology structure. With this basis the article takes the Holtek BH66F5233 MCU as an example device to introduce the usage and special considerations when using the HT8 MCU internal Delta Sigma A/D converter.

Functional Description

Delta Sigma A/D Converter Principle

Delta Sigma A/D conversion is a technique used for high resolution analog to digital conversion applications. The two most important components in the Delta Sigma A/D converter are the Delta Sigma Modulator and the Digital Filter, as shown below.



Delta Sigma A/D Converter Structure

The Delta Sigma A/D converter has the characteristics of extremely high resolution and low noise. In using an over-sampling technology, it greatly reduces the front end anti-aliasing filter requirements and in general requires only a simple RC low-pass filter. This type of A/D converter also has very good linearity characteristics but at the cost of reducing the sampling rate. This results in the A/D converter sampling rate being relatively low. In addition, the internal filter requires a considerable amount of settling time for sudden changes in the input analog signal or for channel switching. This means that there will be a certain delay time between the analog input and the digital data output. Generally, this type of A/D converter is suitable for applications whose analog signals are not subject to rapid changes such as temperature measurements, pressure measurements, etc.

Delta Sigma A/D Converter Advantages and Disadvantages

- Disadvantages

  A hysteresis exists between high-resolution conversion results and A/D sampling for the Delta Sigma A/D converter, which will affect the valid data output rate. The Delta Sigma A/D converter also requires multiple clock cycles to allow the digital filter to settle after each after channel switching. Therefore it is recommended that the first three A/D sampled data results should be discarded for the HT8 MCUs integrated Delta Sigma A/D converter. Additionally the Delta Sigma A/D converter is best used only for low frequency signals or analog inputs not subject to rapid changes.

- Advantages

  By using an oversampling technology the Delta Sigma A/D converter greatly simplifies the anti-aliasing filter design.

Delta Sigma A/D Converter Main Indicators ENOB and NFB

The Effective Number of Bits and Noise Free Bits, known as ENOB and NFB respectively, are the important indicators for the Delta Sigma A/D converter noise performance evaluation.

The term NFB stands for noise free bits. The ENOB stands for effective number of bits, this parameter can be looked upon as a figure for accuracy after filtering and for other processing operations. The relationship between these two parameters is:

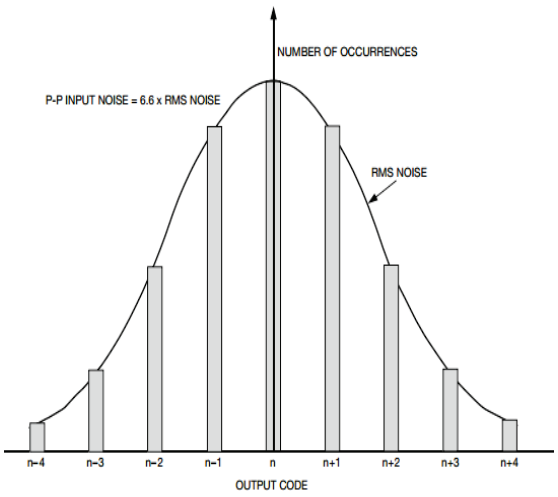
$$NFB \approx ENOB - 2.7 \text{ bits}$$

Theoretical basis: set the A/D converter input to a fixed voltage level and then sketch a diagram with the sampled A/D data. The resulting diagram will provide a Gaussian distribution curve as shown below.

According to the Gaussian distribution curve regulation: the peak-to-peak input noise value (99% of bits) will appear with a range of 6.6 times the RMS noise, as follows:

Peak-to-peak input noise = RMS noise × 6.6

From the ENOB and NFB definitions, the desired NFB ≈ ENOB – 2.7 bits



Peak-to-peak Input Noise and RMS Noise Curve

Corresponding to A/D conversion results, the NFB resolution, which is noise free bits, stands for the number of stable bits, as shown below.

NFB	Noise Free Bits	—	PGA gain=128, Data rate=10Hz	—	15.4	—	Bit
ENOB	Effective Number of Bits	—	PGA gain=128, Data rate=10Hz	—	18.1	—	Bit

BH66F5233 NFB and ENOB

There are certain factors which influence influencing ENOB and NFB. The ENOB value depends on the data rate, the PGA gain and the A/D conversion rate, etc.

1. The higher the data rate is, the lower the ENOB will be.
2. The greater the PGA gain is, the lower the ENOB will be.

In real applications, the A/D converter operating transition can be determined by roughly estimating the ENOB value.

In actual usage, setup two input ports of the A/D converter to be in a short-circuit mode in the MCU. Then connect the A/D converter input ports to the external VCM pin to prevent the input ports from floating. Now the number of stable bits in the obtained A/D conversion value will be approximately equal to NFB, which plus 2.7 bits will be the ENOB value. In general, there is little difference between this ENOB value and the value from the datasheet, however if the ENOB difference is too big, it will be required to check whether there are any hardware and software errors.

In the MCU setup the A/D converter input ports as follows:

- Software
  - Check whether the A/D conversion clock setting is correct
  - Check the A/D converter data rate, which is usually set to 10Hz~100Hz
  - Check the PGA gain, A/D converter gain and reference voltage, etc. It is usual to use a PGA Gain value of x128 and an A/D converter Gain of x1
- Hardware
  - Check whether the A/D converter reference voltage is within the specification range and also check whether the reference voltage is stable.
  - Check whether the A/D converter input voltage is within the specification range.
- Others

  Finally if there are no errors in the hardware and software, but the ENOB value is still low, the reason may be attributed to the PCB layout or the electrical environment.

BH66F5233 24-Bit Delta Sigma A/D Converter Considerations

Hardware Considerations

- Reference input voltage range
  - ◆ 0.96V < V_{REFP} < 2.2V and 0 < V_{REFN} < 1V
  - ◆ 0.96V < V_{REF} = V_{REFP} – V_{REFN} < 1.44V
- Common mode voltage range
  - ◆ 0.4V < V_{CM_PGA} < V_{OREG} – 1.1V
- A/D converter differential input voltage range ΔD_I
  - ◆ (-V_{REF}) / Gain < ΔD_I < (+V_{REF}) / Gain

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
f_{ADCK}	ADC clock frequency	–	–	40	409.6	440	kHz
f_{ADO}	ADC output data rate	–	f_{MCLK} = 4MHz, FLMS[2:0] = 000B	4	–	521	Hz
		–	f_{MCLK} = 4MHz, FLMS[2:0] = 010B	10	–	1302	Hz
V_{REFP}	Reference input voltage	–	VGS[1:0] = 00B,VREFS = 1,VRBUFP = 0,RBUFN = 0VGS[1:0] = 00B,	0.96	1.25	2.2	V
V_{REFN}		–		0	0	1	V
V_{REF}		–	V_{REF} = V_{REFP} – V_{REFN}	0.96	1.25	1.44	V
PGA							
V_{CM_PGA}	Common mode voltage range	–	–	0.4	–	VOREG-1.1	V
Ga	Gain accuracy (Design Spec. not for datasheet)	–	–	-10	–	10	%
ΔD_I	Differential input voltage range	–	Gain = PGS * AGS	-V_{REF} /Gain	–	+V_{REF} /Gain	V
TC_{TS}	Temperature sensor temperature coefficient	–	Ta = -40℃ ~ 85℃, V_{REF} = 1.25V, VGS[1:0]=00B (Gain = 1), VRBUFP = 0, VRBUFN = 0	–	175	–	μV/℃

BH66F5233 Delta Sigma A/D Converter Specification

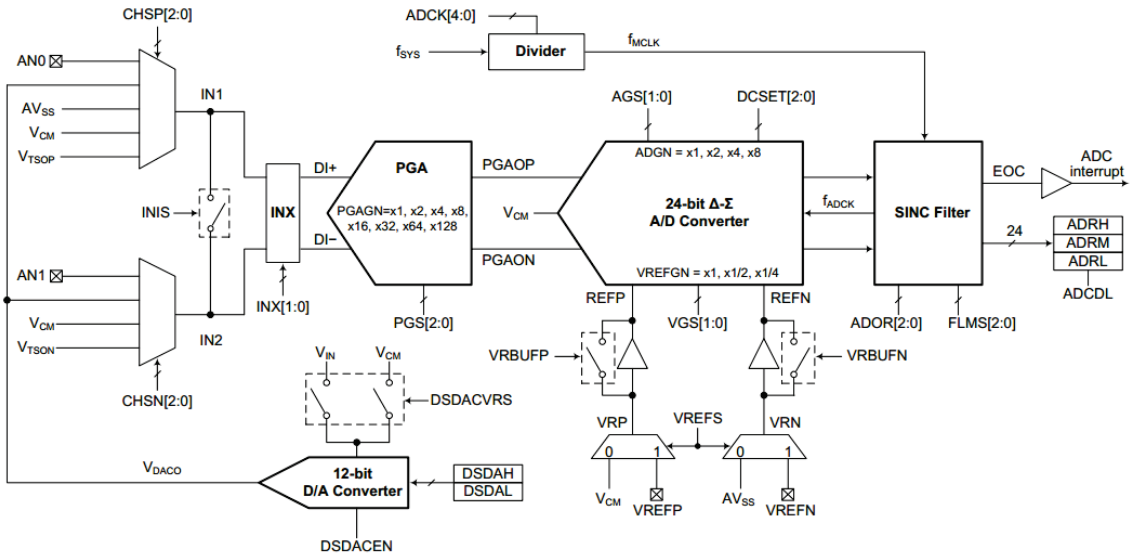
Programming Considerations

1. During the program design, when the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption. This is implemented by setting the ADOFF bit in the ADCR0 register to a high value. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines.
2. When the LDO is switched off, the VCM will also be disabled.
3. The A/D converted data should be latched before reading the A/D conversion results to prevent the possibility of obtaining undesired data. After the converted data has been read out, the latched A/D converter data can be released.

BH66F5233 24-Bit Delta Sigma A/D Converter F/W Configuration

BH66F5233 Delta Sigma A/D Converter Introduction

The BH66F5233 contains a high accuracy multi-channel 24-bit Delta Sigma analog-to-digital converter which can directly interface to external analog signals such as those from sensors or other control signals and convert these signals directly into a 24-bit digital value. In addition, the PGA gain control, A/D converter gain control and A/D converter reference gain control determine the amplification gain for the A/D converter input signal. Designers can select the best gain combination for the optimal input signal amplification. The following block diagram illustrates the A/D converter basic operational function. The A/D converter input channel can be arranged as two differential input channels. The input signal can be amplified by the PGA before entering the 24-bit Delta Sigma A/D converter. The Delta Sigma A/D converter modulator will output a single bit converted data stream to the SINC filter which will transform the converted one-bit data stream to a 24-bit digital number which will then be stored into specific data registers. Additionally, this device also provides a temperature sensor to compensate for any A/D converter deviations due to temperature effects. With high accuracy and good performance, this device is very suitable for weight scales and similarly related products. The BH66F5233 Delta Sigma A/D converter structure is shown below.



BH66F5233 A/D Converter Structure

BH66F5233 Delta Sigma A/D Converter Related Registers

There are a series of registers related to the following A/D converter settings in the BH66F5233. Refer to the BH66F5233 datasheet in the Reference Annexes for a more detailed register description.

Register Name	BITS							
	7	6	5	4	3	2	1	0
PWRC	LDOEN	VCMEN	—	—	—	LDOBPS	LDOVS1	LDOS0
PGAC0	—	VGS1	VGS0	AGS1	AGS0	PGS2	PGS1	PGS0
PGAC1	VCMS	INIS	INX1	INX0	DCSET2	DCSET1	DCSET0	—
PGACS	—	—	CHSN2	CHSN1	CHSN0	CHSP2	CHSP1	CHSP0
ADRL	D7	D6	D5	D4	D3	D2	D1	D0
ADRM	D15	D14	D13	D12	D11	D10	D9	D8
ADRH	D23	D22	D21	D20	D19	D18	D17	D16
ADCR0	ADRST	ADSLP	ADOFF	ADOR2	ADOR1	ADOR0	—	VREFS
ADCR1	FLMS2	FLMS1	FLMS0	VRBUFN	VRBUFP	ADCDL	EOC	—
ADCS	—	—	—	ADCK4	ADCK3	ADCK2	ADCK1	ADCK0
DSDAH	D11	D10	D9	D8	D7	D6	D5	D4
DSDAL	-	-	-	-	D3	D2	D1	D0
DSDACC	DSDACEN	DSDACVRS	-		-	-	-	-

BH66F5233 A/D Converter Related Register List

BH66F5233 Delta Sigma A/D Converter Setup Steps

Step	Operation	Registers	Setup Bits	Functional Description
1	LDO output voltage selection, LDO enable control, VCM voltage selection	PWRC PGAC1	LDOBPS, LDOVS1, LDOVS0, LDOEN, VCMS	Enable LDO output and VCM output
2	A/D converter reference voltage selection	ADCR0	VREFS	0: Internal reference voltage 1: External reference voltage
3	A/D converter reference voltage gain, A/D converter gain and PGA gain selection	PGAC0	VGS1, VGS0, AGS1, AGS0, PGS2, PGS1, PGS0	Select an appropriate gain according to the actual application
4	A/D converter reference voltage gain, A/D converter gain and PGA gain selection, A/D converter register enable control	PGAC0 ADCR1	VGS1, VGS0, AGS1, AGS0, PGS2, PGS1, PGS0, VRBUFN, VRBUFP	Select an appropriate gain according to the actual application and enable the A/D converter
5	A/D converter channel selection	PGACS	CHSN2, CHSN1, CHSN0, CHSP2, CHSP1, CHSP0	Set an analog signal input pin
6	A/D conversion clock selection	ADCS	ADCK4~ADCK0	Set A/D conversion clock
7	A/D converter output data rate selection	ADCR0	ADOR2~ADOR0	Set output data rate, usual to use a range of 10Hz~100Hz
8	A/D converter power down mode and sleep mode on/off control	ADCR0	ADOFF, ADSLP	Disable the A/D converter sleep mode, ensure the A/D converter is ready for operation
9	A/D converter reset control	ADCR0	ADRST	Set this bit high and then reset low to initiate an A/D conversion process
10	A/D converter interrupt enable control	INTC0	ADE, EMI	Initiate an A/D converter interrupt

Hardware Description

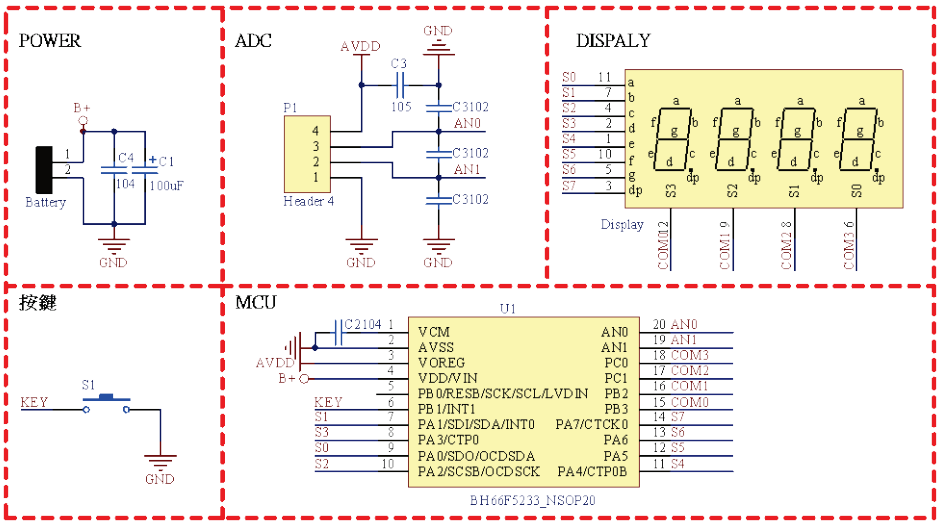
PCB Design Notes

1. The power lines should be as wide as possible to reduce their impedance. In addition the power lines and ground wires should follow the same direction as the signal lines, to improve their anti-interference characteristics.
2. Ground line design: The digital ground and analog ground should be kept apart. If there are both analog circuits and digital circuits on the circuit board, they should be kept apart as much as possible.

   The low-frequency circuit ground should use a single point parallel grounded technique. The high-frequency circuit ground should use a multipoint series grounded technique and the ground wires should be as short and thick as possible.

   On circuit boards which are composed only of digital circuits, most closed loops which are formed by corresponding ground circuits can provide anti-noise capabilities.
3. For the location of capacitors, the power line capacitors should be located as close to the device as possible.

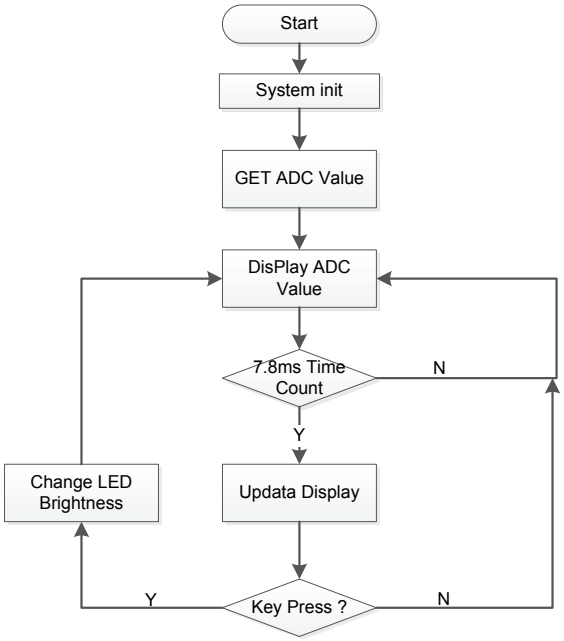
This example illustrates how to show the A/D converted values on an LED display using the BH66F5233 application circuit.



BH66F5233 Application Circuit

Software Description

S/W Flowchart



1. In this example, when the program starts running, the obtained A/D conversion value will be displayed on the LED display. Additionally the LED illumination level can be adjusted using a key.
2. When the program starts running, first initialise the RAM and then setup the LED brightness to the lowest value in the A/D converter sampling process.
3. When the key is pressed, the LED brightness will change. The brightness changes once for every key press recycling every 4 times.
4. The LED display shows the A/D conversion results.

Conclusion

This application note has introduced the principles and how to evaluate the performance of the Sigma Delta A/D converter using the BH66F5233 MCU. Users can setup the A/D converter to obtain appropriate parameters according to their actual application requirements.

Versions and Modification Information

Date	Author	Issue Release and Modification
2016.11.07	林琛洋	First Version

References

Reference document: BH66F5233 Data Sheet.

For more information, refer to the Holtek's official website: http://www.holtek.com.

Reference Annexes

Related Document

原理圖.rar

Related Firmware Archives

BH66F5233_AD_Digital_LED.zip

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