10-bit, 125 MS/s, 40 mW Pipelined ADC in 0.18 μm CMOS

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This paper presents a 10-bit, 125 MS/s CMOS pipelined analog-to-digital converter (ADC). The power consumption of this ADC is just 40 mW at a supply voltage of 1.8 V, which is less than half that of other ADCs with an equivalent sampling rate. Low power consumption is achieved by using a flip-around digital-to-analog converter (FADAC) that reduces the power consumption of the front-end circuit by 50% compared to that of a conventional one. The ADC was fabricated using 0.18 μm CMOS technology, and the active area is 1.1 × 0.6 mm². The measured peak signal-to-noise and distortion ratio (SNDR) is 54.2 dB with an 80 MHz input operating at a 125 MS/s sampling rate. The ADC will help reduce the power consumption of system-on-a-chips (SoCs) for digital consumer products and wireless communication equipment.

1. Introduction

Ten-bit analog-to-digital converters (ADCs) are in high demand for applications such as digital consumer products and wireless communication equipment. For these applications, because of the increase in the transferred data volume and resolution of video data, there have been demands for higher sampling rates in the ADCs that convert analog signals to digital signals. Also, system-on-a-chips (SoCs) that contain analog circuits and digital signal processing circuits in a single chip are required to achieve higher performance and lower costs. ADCs occupy the principal part of analog circuits in SoCs; therefore, reducing the ADC power consumption helps reduce the power consumption of an entire SoC.

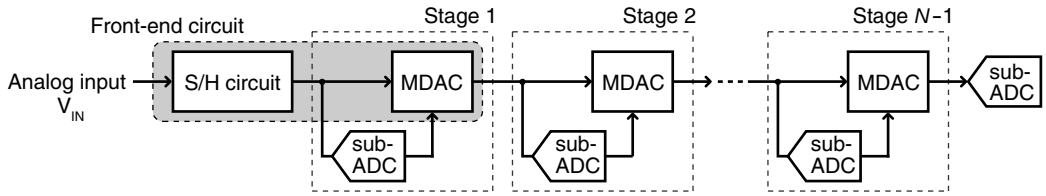
The speed and power consumption of 10-bit ADCs have been improved by using the pipelined architecture.[1)-6)] In the conventional pipelined ADC shown in **Figure 1**, the front-end circuit, which consists of a sample-and-hold (S/H) circuit and a multiplying digital-to-analog converter (MDAC),[7)] requires the highest accuracy and consumes the most power. For example, in our conventional pipelined ADC, the power consumption of the front-end circuit is half the total. In order to reduce the power consumption of pipelined ADCs, we need to reduce the power consumption of the front-end circuit. Therefore, we developed a new front-end circuit that we call a flip-around digital-to-analog converter (FADAC). The FADAC reduces the power consumption of the front-end circuit by 50% compared to that of a conventional S/H and MDAC. Moreover, we developed a 10-bit, 125 MS/s, pipelined ADC using the FADAC. This ADC achieved the low power consumption of just 40 mW from a 1.8 V supply.

Section 2 explains the configuration and operation of the FADAC in detail. The design and experimental results of the prototype ADC are described in Sections 3 and 4.

2. FADAC design

2.1 Conventional front-end circuit

Figure 2 shows the conventional switched-capacitor implementation of a front-end circuit.



ADC: Analog-to-digital converter
S/H circuit: Sample-and-hold circuit
MDAC: Multiplying digital-to-analog converter

Figure 1
Conventional pipeline architecture.

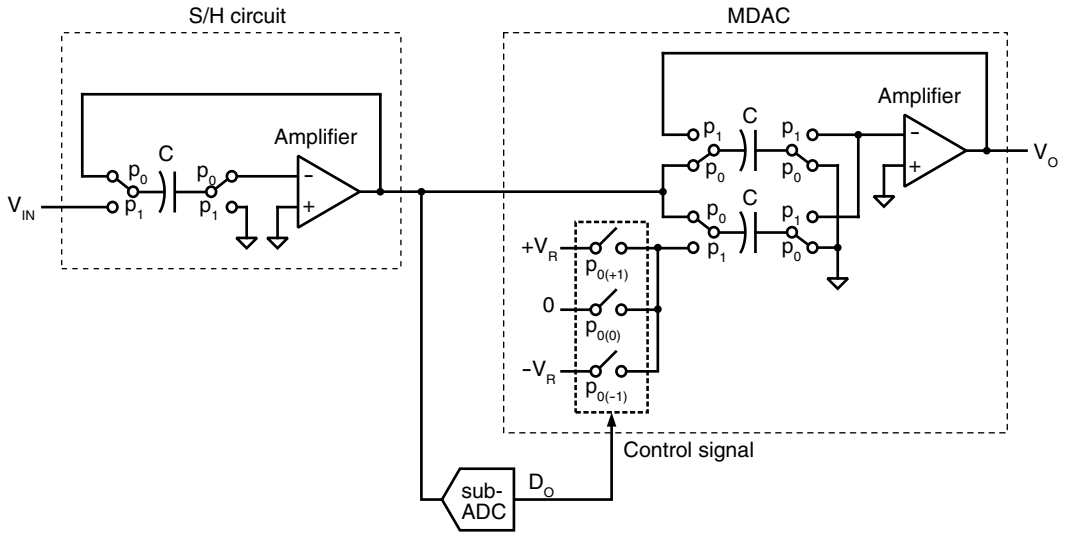


Figure 2
Conventional front-end circuit.

The S/H circuit samples the analog input signal V_{IN} during clock phase p_1. The analog input signal ranges from $-V_R$ to $+V_R$. During the next clock phase p_0, the S/H circuit holds the sampled signal. The output of the S/H circuit is digitized by the sub-ADC and applied to the MDAC. During the next clock phase p_1, the MDAC generates the stage residue at V_O. The outputs of the sub-ADC are used to select the reference voltages of $+V_R$, 0, and $-V_R$.

The S/H and MDAC each have an amplifier, and these amplifiers are the major power consumers in these circuits. To achieve highly accurate, low-noise signal processing, large capacitors are required. This means the amplifiers have to drive large capacitors at high speed, which means the amplifiers need more power. Furthermore, the charge-redistribution architecture applied to the MDACs also increases the power consumption of the amplifiers. This is described in detail in Section 2.3.

To reduce the power consumption of the amplifiers, we established two goals. The first was to reduce the number of amplifiers by realizing the functions of the S/H and MDAC with a single amplifier. The second was to apply a flip-around architecture that reduces the power consumption compared to a charge-redistribution architecture. As a result, we developed the FADAC.

2.2 Operation of FADAC

Figure 3 shows the schematic and operation of the FADAC. Although a single-ended configuration is shown for simplicity, the actual implementation is fully differential. The upper half of this diagram shows the FADAC, and the lower half shows the two comparators that correspond to the sub-ADC shown in Figure 2. The FADAC has three operating phases: sample, comparison, and hold. First, during the sample phase, the analog input signal V_{IN} is applied to capacitors $C_{S(IN)}$, C_{C1}, and C_{C2}. The analog input signal ranges from $-4V_R$ to $+4V_R$. Simultaneously, reference voltages of $+2V_R$, 0, and $-2V_R$ are applied to capacitors $C_{S(-1)}$, $C_{S(0)}$, and $C_{S(+1)}$, respectively. To prevent sample clock skew between the converter and comparators from degrading the conversion accuracy at higher input frequencies, the switched-capacitor networks have the same topology, values, and layout pattern. $C_{S(IN)}$, C_{C1}, C_{C2}, $C_{S(-1)}$, $C_{S(0)}$, and $C_{S(+1)}$ are all 0.5 pF. Next, during the comparison phase, the top plates of C_{C1} and C_{C2} are connected to the comparators, and the reference voltages ($+V_R$, $-V_R$) are applied to the bottom plates. The sampled analog input is compared to the reference voltages, and the outputs of the comparators are latched. In the FADAC, all the switches at both ends of the capacitors are opened. Then, during the hold phase, either $C_{S(-1)}$, $C_{S(0)}$, or $C_{S(+1)}$ is selected based on the outputs of the comparators, and a negative feedback loop forms around the amplifier in parallel with $C_{S(IN)}$. This is the flip-around architecture. The output of the FADAC during the hold phase is equivalent to the output of an MDAC. Therefore, the FADAC provides the S/H and MDAC functions using a single amplifier. Therefore, the power consumption of the front-end circuit is reduced by the amount needed for one amplifier.

2.3 Advantages of flip-around architecture

The flip-around architecture consumes less power than the charge-redistribution architecture used in conventional MDACs because of two features. Firstly, the amplifier does not have to charge the capacitors during the hold phase. As shown in **Figure 4**, in the flip-around architecture, the sampled charge is only shared between the two capacitors during the hold phase. However, in the charge-redistribution architecture, the amplifier charges the capacitors because the sampled charge is redistributed to the two capacitors during the hold phase. Therefore, the amplifier of the flip-around architecture consumes less

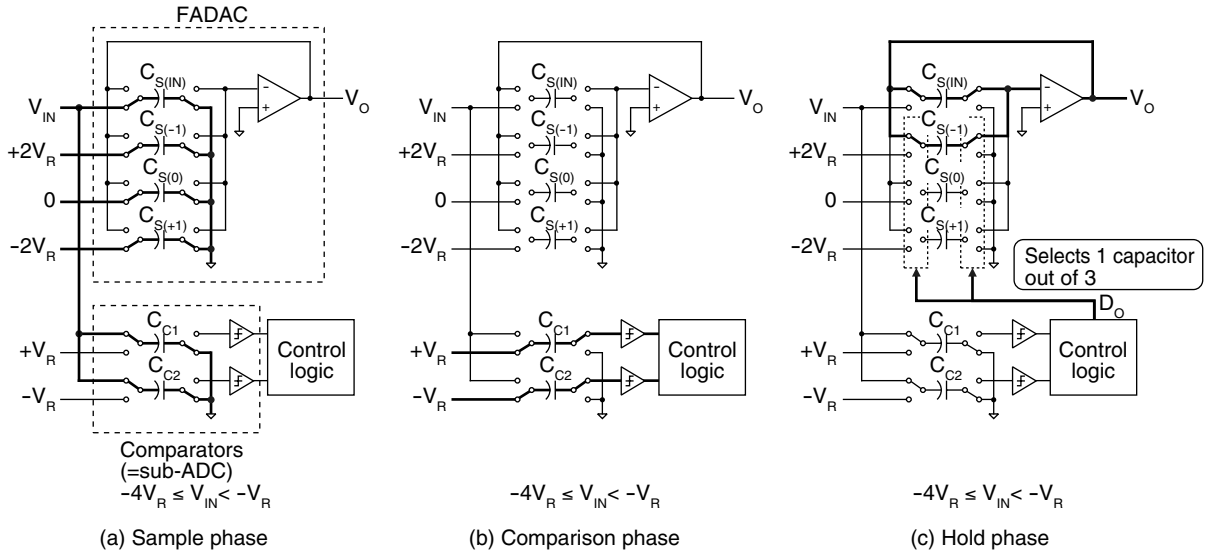
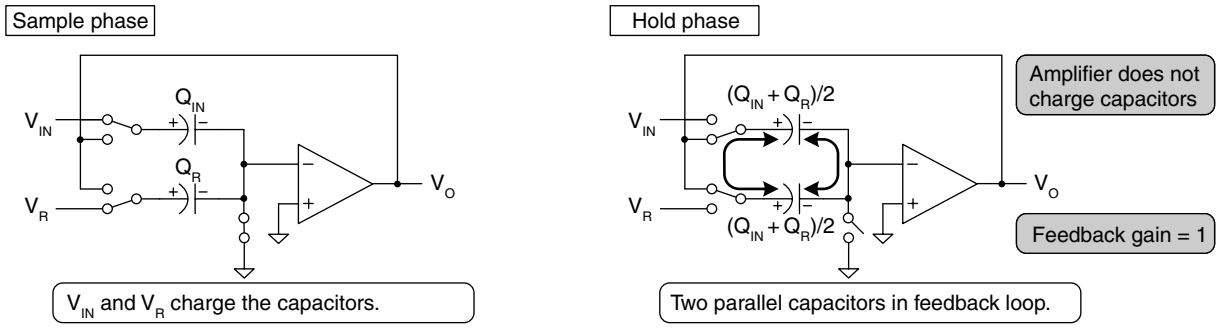
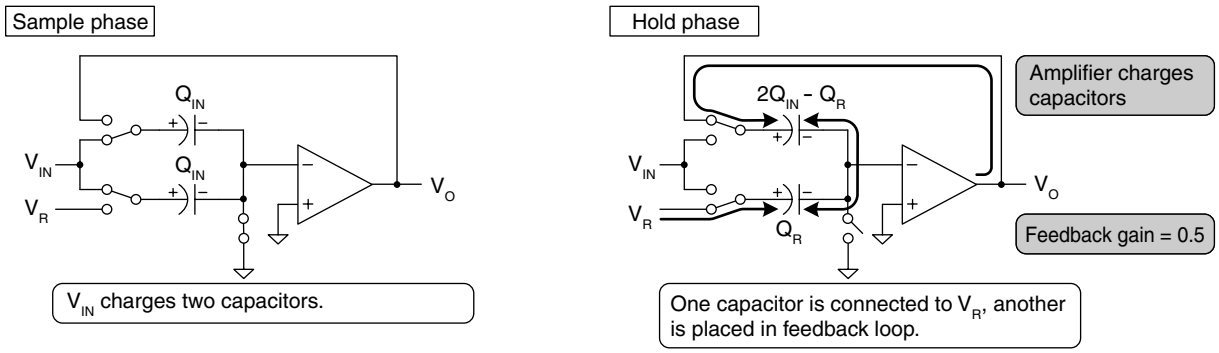


Figure 3
Schematic and operation of flip-around digital-to-analog converter (FADAC).



(a) Flip-around architecture



(b) Charge-redistribution architecture

Figure 4
Comparison of flip-around and charge-redistribution architectures.

power than the amplifier of the charge-redistribution architecture. Secondly, the capacitor is connected to the input and output nodes of the amplifier only during the hold phase. Therefore, the feedback gain from the output node to the input node of the amplifier is 1. In contrast, with the charge-redistribution architecture, the input of the amplifier is the middle node of two serial capacitors, so the feedback gain is 0.5. The feedback gain affects the operation speed during the hold phase: the lower the feedback gain, the longer the settling time. When the gain bandwidth product of the amplifier is fixed, the settling time during the hold phase with the flip-around architecture is shorter than that with the charge-redistribution architecture because the feedback gain is twice as large. In other words, to achieve a target settling time during the hold phase, the gain-bandwidth product requirement of the amplifier is relaxed, which means that less power is needed.

Figure 5 shows the power reduction that is achieved over a conventional ADC when a FADAC is used as the front-end circuit of a 10-bit A/D converter consisting of eight pipelined stages. With the FADAC, the power consumption of the front-end circuit is reduced by 50%, and the total power consumption of the ADC is reduced by 25%.

2.4 Transfer function of FADAC

Figure 6 compares the transfer functions of the conventional front-end circuit and the FADAC. The transfer function of the conventional front-end circuit is $V_O = 2V_{IN} - D_O V_R$, where V_{IN} is the analog input and D_O is –1, 0, or 1 as determined by the outputs of the comparators. The output range of the conventional front-end circuit is between $-V_R$ and $+V_R$. On the other hand, because

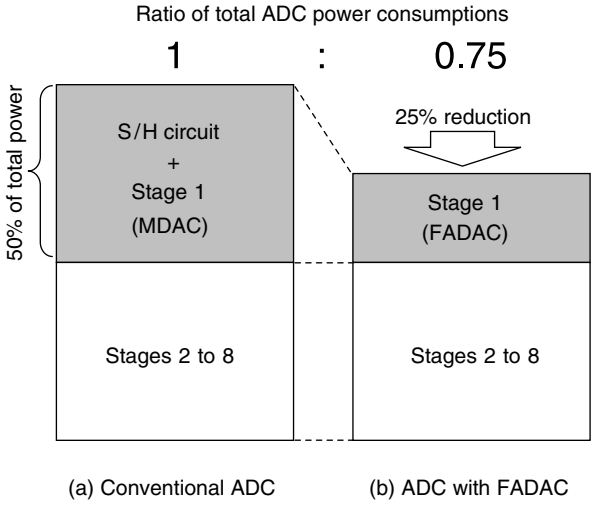


Figure 5
Power reduction achieved using FADAC.

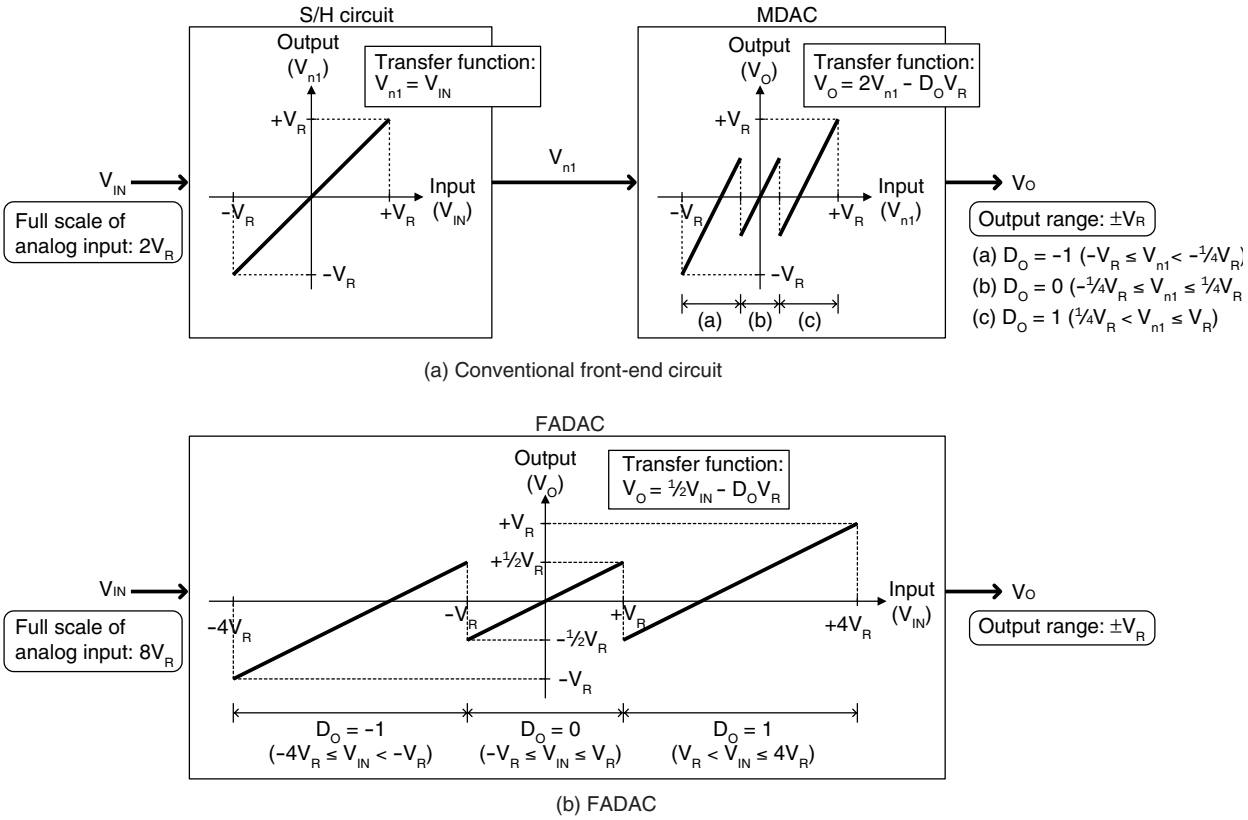


Figure 6
Comparison of transfer functions.

the output of the FADAC is the average voltage of the two capacitors that are charged by the analog input and the reference voltage, respectively, the transfer function is $V_O = \frac{1}{2}V_{IN} - D_O V_R$. Therefore, to make the output range of the FADAC the same as that of the conventional front-end circuit, the analog input range is expanded by 4 times and reference voltages of $-2V_R$ and $+2V_R$ are provided. As a result, the output of the FADAC ranges from $-V_R$ to $+V_R$.

3. Prototype implementation

3.1 ADC architecture

Figure 7 shows the block diagram of the prototype ADC. The first stage consists of the FADAC, and the following seven stages consist of conventional MDACs. The back-end is a 2-bit flash. Both the FADAC and MDACs have fully differential configurations to minimize the effects of common-mode noise and to suppress even-order distortions. Each stage has a 1.5-bit sub-ADC consisting of two comparators. The sub-ADC of the first stage has thresholds at $\pm V_R$, and the sub-ADCs of the following seven stages have thresholds at $\pm\frac{1}{4}V_R$. In our design, the differential full-scale range of the analog input is $4.0\,V_{pp}$, and the differential full-scale range of the output of each pipeline stage is $1.0\,V_{pp}$. V_R is 0.25 V, and its common-mode voltage is 0.9 V. Therefore, the thresholds of the sub-ADC of the first stage are 0.65 V and 1.15 V, and the thresholds of the other sub-ADCs are 0.8375 V and 0.9625 V.

3.2 Double-sampling technique

A double-sampling technique[8] is used for the FADAC and MDACs. The double-sampling configuration consists of a single amplifier and two time-interleaved switched-capacitor networks. This configuration relaxes the bandwidth requirement of the amplifiers without increasing their number, which further reduces the amplifier power consumption. **Figure 8** shows the configuration and timing chart of the double-sampling FADAC. The sample phase and comparison phase of one network occur during the two halves of the other network's hold phase to ensure the settling time is as long as possible during the hold phase. At any time, one switched-capacitor network is in the sample or comparison state and the other is in the hold state.

While the double-sampling technique has the advantage of reducing power consumption, it also has the drawback of additional distortion caused by offset, gain, and clock-skew mismatches between the two switched-capacitor networks. In this ADC, to minimize the spurious tones caused by the channel mismatches, we took care with the layout of the amplifiers, capacitors, switches, clock-generation circuits, and all the wiring to maintain symmetry between the two switched-capacitor networks.

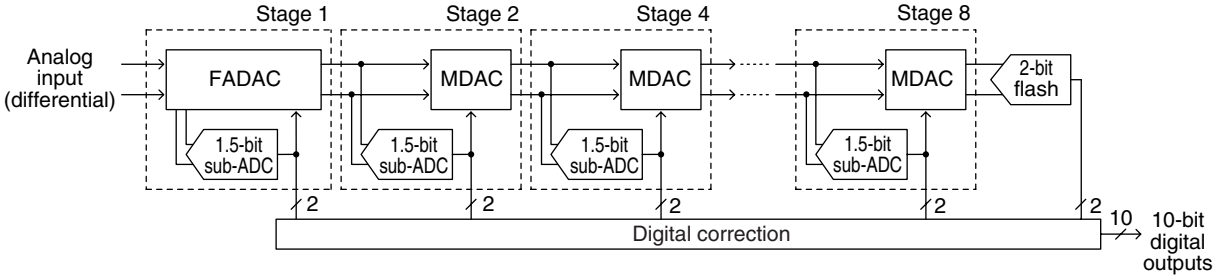


Figure 7
Block diagram of prototype ADC.

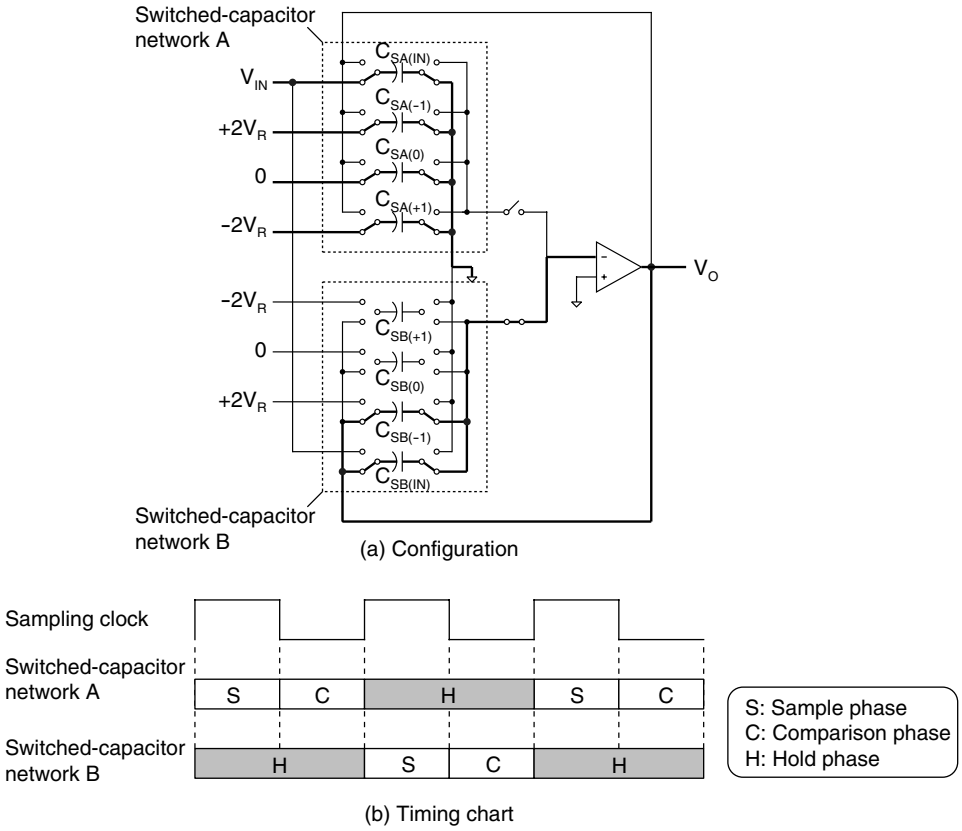


Figure 8
Configuration and timing chart of double-sampling FADAC.

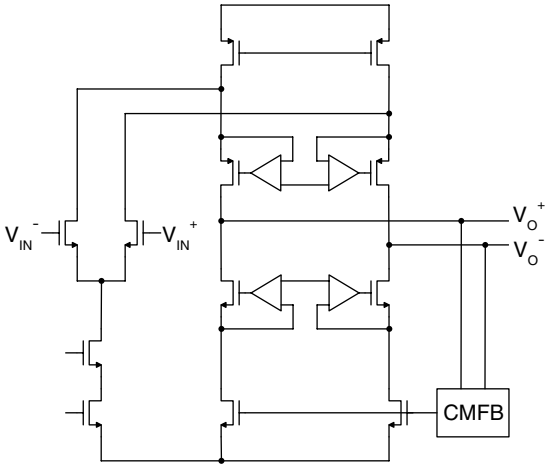
3.3 Operational amplifier

Figure 9 shows the schematic of the amplifier used in the FADAC and MDAC. To obtain a high bandwidth and high DC gain with a low supply voltage, we use a folded-cascode topology with a gain-boost technique. A simulation showed the DC gain of the amplifier is 79 dB when the supply voltage is 1.8 V.

4. Measurement results

The prototype ADC was fabricated using 0.18 μm CMOS technology with 1-poly and 4-metal layers. **Figure 10** shows a photomicrograph of the ADC chip, which has an active area of 0.66 mm^2. The FADAC is 0.058 mm^2 and occupies 8.8% of the ADC's area. Because the FADAC places the reference voltages on the capacitors in advance, extra switches and capacitors are required. However, the values and number of switches and capacitors in the FADAC are comparable to those of the conventional front-end circuit. Therefore, compared to the conventional pipelined ADC, the area of the ADC is not increased by using the FADAC.

Table 1 summarizes the performance of the ADC measured at a sampling rate of f_s = 125 MS/s. **Figure 11** shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) curves of the ADC measured at a sampling rate of f_s =125 MS/s. The DNL is within ±0.5 of the least significant bit (LSB), and the INL is within ±0.7 LSB. **Figure 12** shows the measured spectrum at 125 MS/s and an input frequency of f_{in} = 80 MHz. The spurious tone caused by offset mismatch appears at $f_s/2$ = 62.5 MHz and is –68.7 dB. The spurious tone caused by gain and clock-skew mismatches appears at $f_{in} - f_s/2$ = 17.5 MHz and is –73.1 dB. These characteristics



CMFB: Common-mode feedback circuit

Figure 9
Schematic of fully differential amplifier.

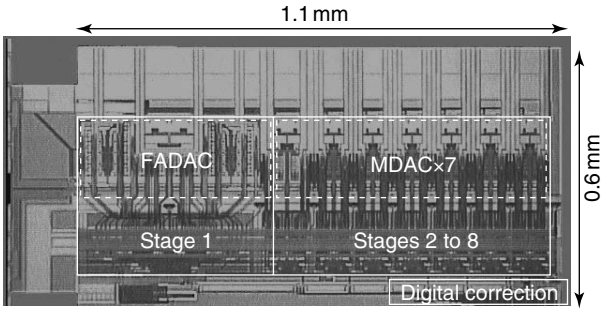
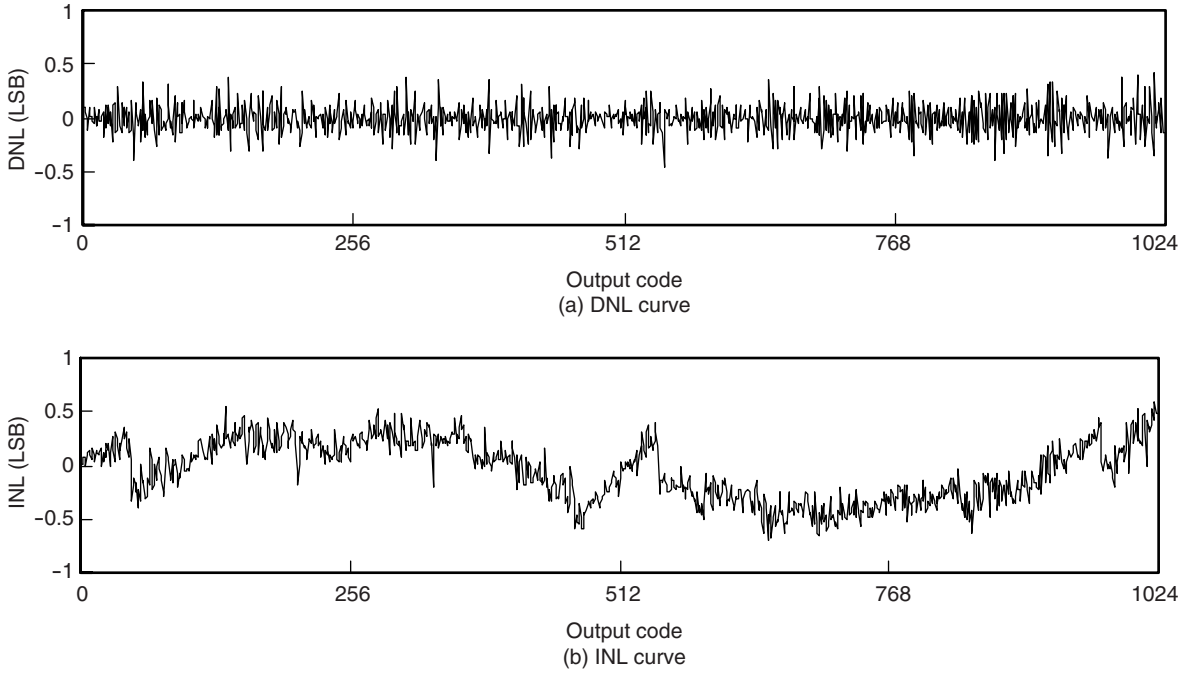


Figure 10
ADC chip photomicrograph.

Table 1
Performance summary of ADC.

Technology	0.18 μm CMOS process
Resolution	10 bit
Sampling rate	125 MS/s
Supply voltage	1.8 V
Differential nonlinearity (DNL)	< 0.5 LSB
Integral nonlinearity (INL)	< 0.7 LSB
Signal-to-noise and distortion ratio (SNDR)	56.4 dB @ 2 MHz input 54.2 dB @ 80 MHz input
Total power consumption	40 mW
Active area	1.1 × 0.6 mm^2

LSB: Least significant bit



DNL: Differential nonlinearity INL: Integral nonlinearity

Figure 11
Measured DNL and INL.

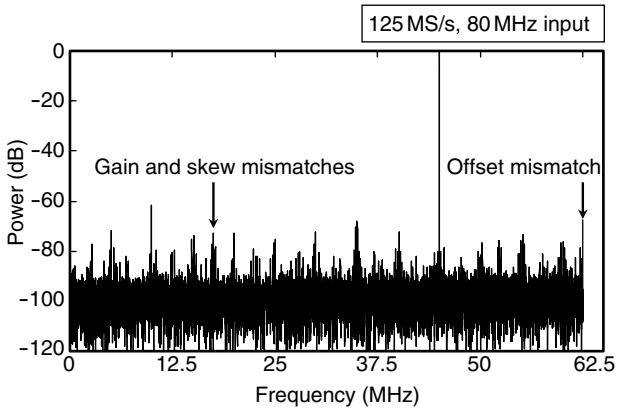


Figure 12
Measured spectrum.

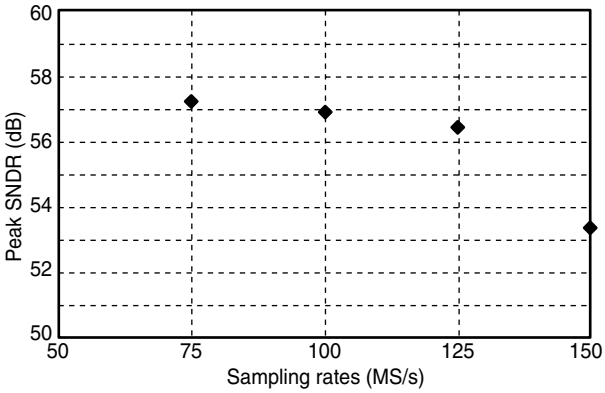
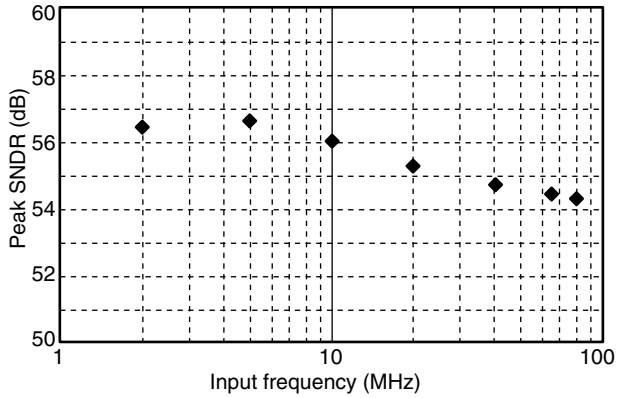


Figure 14
Measured Peak SNDR versus sampling rates at 2 MHz sinusoidal input.



SNDR: Signal-to-noise and distortion ratio

Figure 13
Measured peak SNDR versus input frequency at 125 MS/s.

Table 2
Performance comparison.

Reference	Sampling rates (MS/s)	Power consumption (mW)	FoM (pJ/conversion)
[1]	12	3.3	0.79
[2]	30	16	1.03
[3]	50	29	0.98
[4]	80	69	1.22
[5]	150	123	2.00
[6]	220	135	1.59
This work	**125**	**40**	**0.59**

are sufficient for a 10-bit ADC. **Figure 13** shows the peak signal-to-noise and distortion ratio (SNDR) for sinusoidal input frequencies up to 80 MHz at 125 MS/s. The peak SNDR is 56.4 dB with a 2 MHz input and 54.2 dB with an 80 MHz input, which is a difference of just 2.2 dB. The ADC maintains good performance up to an 80 MHz input. **Figure 14** shows the peak SNDR for sampling rates up to 150 MS/s with a 2 MHz sinusoidal input. The peak SNDR is approximately constant up to 125 MS/s and then slowly starts to roll off at about 150 MS/s.

The ADC dissipates only 40 mW at 125 MS/s with a 1.8 V supply. We quote an ADC figure of merit (FoM) in order to show that the power of the ADC is very low. The FoM expresses the energy per conversion and is defined as FoM = P/[2^{ENOB}·min(f_s,2ERBW)], where ENOB is the effective number of bits and ERBW is the effective resolution bandwidth. The FoM of our ADC is 0.59 pJ/conversion. **Table 2** lists the sampling rates, power consumption, and FoM of our ADC and some recently reported 10-bit CMOS ADCs. As the table shows, our ADC has the best FoM.

5. Conclusion

We have developed a FADAC as a new low-power front-end circuit for pipelined ADCs. The FADAC reduces the power consumption of the front-end circuit by reducing the number of amplifiers and by using the flip-around architecture. In our design, the FADAC reduces the power consumption of the front-end circuit by 50% compared to that of a conventional S/H circuit and MDAC and reduces the total ADC power consumption by 25%. This demonstrates that the FADAC is a very effective means of reducing power in pipelined ADCs.

Using a FADAC, we fabricated a 10-bit, 125 MS/s pipelined ADC with an active area of 0.66 mm^2 using 0.18 μm CMOS technology. At 125 MS/s, the measured DNL and INL of this ADC are 0.5 LSB and 0.7 LSB, respectively, and the measured peak SNDR is 54.2 dB with an 80 MHz input. Particularly, the power consumption is just 40 mW at a 1.8 V supply. To our knowledge, this value is less than half that of reported 10-bit ADCs running at a comparable sampling rate. We intend to apply this ADC to the SoCs of digital consumer products and wireless communication equipment.

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