AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

PROBLEM ADVISORY

CAES

1. TITLE MIL-STD-1553 RESIDUAL VOLTAGE DEPENDENCIES ON TRANSFORMER SELECTION WHEN INTERFACING TO CAES TRANSCEIVERS	**2. DOCUMENT NUMBER** SPO-2015-PA-0001
	3. DATE *(Year, Month, Date)* 2015, February, 25
4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	**5. MANUFACTURER POINT OF CONTACT NAME** Tim Meade
	6. MANUFACTURER POINT OF CONTACT TELEPHONE 719-594-8048
	7. MANUFACTURER POINT OF CONTACT EMAIL Tim.meade@cobhamaes.com

8. CAGE CODE	9. LDC START	10. LDC END	11. PRODUCT IDENTIFICATION CODE	12. BASE PART
65342	ALL	ALL	JB01-05; BA02; MM016-27	UT63Mxxx; UT69151xxxx

13. BLANK	**14. SMD NUMBER** (See Sheet 2)	**15. DEVICE TYPE DESIGNATOR** See Sheet 2
	16. RHA LEVELS ALL	**17. QML LEVEL** ALL
	18. NON QML LEVEL ALL	**19. BLANK**

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

CAES recently worked with a customer who observed unexpectedly high residual voltage amplitude and a high degree of residual voltage variance across a small sample of MIL-STD-1553 terminals during system level testing. A bus monitor flagged the anomaly while the Terminal-Under-Test maintained error free communication with the test side bus controller.

MIL-STD-1553B requires that all MIL-STD-1553 terminals meet the output symmetry requirements as defined in section 4.5.2.1.1.4 for transformer-coupled (4.5.2.2.1.4 for direct-coupled) terminals. This requirement ensures that a terminal completing a transmission does not leave a residual voltage on the bus that interferes with the sync pulse of a subsequent message. If a residual voltage with a high enough amplitude is present on the bus while another terminal begins transmission, the residual voltage can affect the incoming message such that the intended target fails to properly decode the message.

Output symmetry is strongly dependent upon electrical imbalances in the closed-loop system created by the digital MIL-STD-1553 protocol device, the differential transceiver, and a center-tapped isolation transformer. The problem investigation determined root cause of the elevated residual voltage was imbalanced transfer of energy from Aeroflex's transceivers through isolation transformers due to parasitic elements within the transformer. There are several relevant transformer parameters that affect the transformer/transceiver performance. Transformer datasheets generally exclude these parameters.

21. ACTION TAKEN / PLANNED

Presently, there are an increasing number of MIL-STD-1553 Transformer vendors in the market. Based on interoperability history and parametric performance, CAES recommends selecting transformers from Pulse Electronics (http://www.pulseelectronics.com) and North Hills Signal Processing Corp. (http://www.nhsignal.com).

CAES also recommends that users perform additional parametric screening for transformers with a sorting preference toward balanced primary side leakage inductances and reflected impedances. The detailed Product Advisory appended to this notification includes a worksheet for additional parametric screening.

Finally, CAES recommends an evaluation of primary side signal integrity and half-bit time balance vs. residual voltage during brass board and engineering model checkout. If the circuit board uses a transformer vendor other than Pulse or North Hills, CAES strongly encourages the system designer to perform a compatibility analysis.

22. DISPOSITIONARY RECOMMENDATION:	CHECK & USE AS IS ☒	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CORRECT & USE AS SPECIFIED ☐

23. ADEPT REPRESENTATIVE	24. SIGNATURE	25. DATE
Lin-Chi Huang		

List of Applicable Products

Applicable MIL-STD-1553 Transceivers as of February 2015		
SMD #s	SMD #s	Generic Part #s
5962-0724201QXA	5962-9322603QXA	UT63M105C-PCA
5962-0724201QXC	5962-9322603QXC	UT63M105C-PCC
5962-0724201QYA	5962-9322603QZA	UT63M105C-PPC
5962-0724201QYC	5962-9322603QZC	UT63M125C-BCA
5962-0724201VXA	5962-9322603VXA	UT63M125C-BCC
5962-0724201VXC	5962-9322603VXC	UT63M125C-BPC
5962-0724201VYA	5962-9322603VZA	UT63M125C-CCA
5962-0724201VYC	5962-9322603VZC	UT63M125C-CCC
5962D0724201VYC	5962R9322603Q9A	UT63M125C-CPC
5962R0724201QXA	5962R9322603QXA	UT63M125C-DCA
5962R0724201QXC	5962R9322603QXC	UT63M125C-DCC
5962R0724201QYA	5962R9322603QZA	UT63M125C-DPC
5962R0724201QYC	5962R9322603QZC	UT63M143-BCA
5962R0724201VXA	5962R9322603VXA	UT63M143-BCC
5962R0724201VXC	5962R9322603VXC	UT63M143-BPC
5962R0724201VYA	5962R9322603VZA	UT63M143-CCA
5962R0724201VYC	5962R9322603VZC	UT63M143-CCC
5962F0724201QXA	5962F9322603QXA	UT63M143-CPC
5962F0724201QXC	5962F9322603QXC	UT63M145-BCA
5962F0724201QYA	5962F9322603QZA	UT63M145-BCC
5962F0724201QYC	5962F9322603QZC	UT63M145-CPC
5962F0724201VXA	5962F9322603V9A	UT63M147-BCA
5962F0724201VXC	5962F9322603VXA	UT63M147-BCC
5962F0724201VYA	5962F9322603VXC	UT63M147-BPC
5962F0724201VYC	5962F9322603VZA	UT63M147-CCA
5962G0724201QXA	5962F9322603VZC	UT63M147-CCC
5962G0724201QXC	5962G9322603QXA	UT63M147-CPC
5962G0724201QYA	5962G9322603QXC	UT63M147-DIE
5962G0724201QYC	5962G9322603QZA	
5962G0724201VXA	5962G9322603QZC	
5962G0724201VXC	5962G9322603VXA	
5962G0724201VYA	5962G9322603VXC	
5962G0724201VYC	5962G9322603VZA	
5962H0724201QXA	5962G9322603VZC	
5962H0724201QXC	5962H9322603Q9A	
5962H0724201QYA	5962H9322603QXA	
5962H0724201QYC	5962H9322603QXC	
5962H0724201VXA	5962H9322603QZA	
5962H0724201VXC	5962H9322603QZC	
5962H0724201VYA	5962H9322603VXA	
5962H0724201VYC	5962H9322603VXC	
	5962H9322603VZA	
	5962H9322603VZC	
	5962P9322603QZA	

Applicable MIL-STD-1553 Protocol Devices with Integrated Transceivers as of February 2015	
SMD #s	Generic Part #s
5962-9466308QXA	UT69151CDXE-WCA
5962-9466308QXC	UT69151CDXE-WCC
5962-9466308QYA	UT69151CDXE-WPC
5962-9466308QYC	UT69151CLXE15-W
5962-9466309QXA	UT69151CLXE15-WPC
5962-9466311QYA	UT69151CLXE-WCA
5962-9466311QYC	UT69151DXE-GCA
5962R9466311QYA	UT69151DXE-GCC
5962R9466311QYC	UT69151DXE-GPC
5962R9466311VYA	UT69151DXE-WCA
5962R9466311VYC	UT69151DXE-WCC
5962F9466311QYA	UT69151DXE-WPC
5962F9466311QYC	UT69151LXE15-GC
5962F9466311VYA	UT69151LXE15-GP
5962F9466311VYC	UT69151LXE15-WC
5962-9475808QXA	UT69151LXE15-WP
5962-9475808QXC	UT69151RTE-FCC
5962-9475808QYA	UT69151RTE-FPC
5962-9475808QYC	UT69151RTE-GCA
5962-9475808QZA	UT69151RTE-GCC
5962-9475808QZC	UT69151RTE-GPC
5962-9475809QXA	UT69151RTE-WCA
5962-9475809QXC	UT69151RTE-WCC
5962-9475809QYA	UT69151RTE-WPC
5962-9475809QYC	UT69151XTE12-GC
5962-9858701QXA	UT69151XTE12-GP
5962-9858701QXC	UT69151XTE12-WC
5962-9858701QYC	UT69151XTE12-WP
5962-9858701QZC	UT69151XTE15-GC
	UT69151XTE15-GP
	UT69151XTE15-WC
	UT69151XTE15-WP
	UT69151XTE5-GCA
	UT69151XTE5-GCC
	UT69151XTE5-GPC
	UT69151XTE5-WCA
	UT69151XTE5-WCC
	UT69151XTE5-WPC
	UT69151XTE5-ZCA
	UT69151XTE5-ZCC
	UT69151XTE5-ZPC

Appended Full Product Advisory
CAES Transformer Recommendation for Optimal MIL-STD-1553 Residual Voltage when Interfacing to CAES Transceivers

Table 1: List of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC* Number
UT63M147 Bus Transceiver	UT63M147	5962-93226	03, 04	JB01 JB03
UT63M143 Bus Transceiver	UT63M143	5962-07242	01, 02	JB04 JB05
UT63M1X5C Bus Transceiver	UT63M1X5C	N/A	N/A	BA02
SμMMIT DXE	UT69151 DXE	5962-94663	08, 11	MM016 MM023 MM025 MM027
SμMMIT XTE	UT69151 XTE	5962-94758	08	MM019
SμMMIT RTE	UT69151 RTE	5962-98587	01	MM022

* PIC = CAES Internal Product Identification Code

1.0 Overview

The objective of this product advisory is to inform MIL-STD-1553 circuit designers of lessons learned during a residual voltage investigation and to offer some transformer selection recommendations to minimize residual voltage.

2.0 Background

CAES recently worked with a customer who observed unexpectedly high residual voltage amplitude and a high degree of residual voltage variance across a small sample of MIL-STD-1553 terminals during system level testing. A bus monitor flagged the anomaly while the Terminal-Under-Test maintained error free communication with the test side bus controller. CAES worked extensively with its customer to evaluate all aspects of their circuit and system design and test network, which included evaluating a test-side bus controller and MIL-STD-1553 bus monitor, to understand the cause of the variance.

The investigation method was to isolate, swap, compare, and contrast every aspect of the system, circuit design, manufacturing and component handling/accountability systems. Disqualifying one variable at a time, the investigation team reduced the anomalistic problem area to the interaction between Aeroflex's transceiver and the transformer.

MIL-STD-1553B requires that all MIL-STD-1553 terminals meet the output symmetry requirements as defined in section 4.5.2.1.1.4 for transformer-coupled (4.5.2.2.1.4 for direct-coupled) terminals. This requirement ensures that a terminal completing a transmission does not leave a residual voltage on the bus that interferes with the sync pulse of a subsequent message. If a residual voltage with a high enough amplitude is present on the bus while another terminal begins transmission, the residual voltage can affect the incoming message such that the intended target fails to properly decode the message.

Output symmetry is strongly dependent upon electrical imbalances in the closed-loop system created by the digital MIL-STD-1553 protocol device, the differential transceiver, and a center-tapped isolation transformer. All three devices work cooperatively to drive Manchester-II bi-phase encoded signals onto the MIL-STD-1553 bus. Manchester-II bi-phase signaling encodes clock and data onto a single wire pair while maintaining a zero DC bias on the physical interconnect. In an ideal MIL-STD-1553 bus, the zero DC voltage bias occurs because positive energy in the system exactly matches the negative energy.

However, the reality is that non-idealities in the components and their connection to one another create an imbalance in the system. Some of this imbalance is inherent to the MIL-STD-1553 terminal components themselves, while others are dependent upon the terminal designer's decoupling, layout, and assembly decisions. This product advisory focuses on the former. Although the circuit designer cannot substantively affect the actual interaction between the specific transformer and transceiver combination, having awareness of the device characteristics related to output symmetry and using these insights to select and screen components is an effective strategy to maximize energy transfer in the system and assuring minimal residual voltage on the MIL-STD-1553 serial bus.

2.1 Definition of Residual Voltage

To determine output symmetry, measure the waveform tail-off time (T_T) after the end of each valid transmitted message as shown in Figure 1. The residual voltage (V_R) on the bus is the resulting measure of output symmetry. The pass criteria for residual voltage is ±250mV peak, line-to-line, for transformer-coupled terminals and ±90mV peak, line-to-line, for direct-coupled terminals. Measure V_R at Point A (see Figure 2) in a MIL-STD-1553 system 2.5µs after the mid-bit zero crossing of the parity bit.

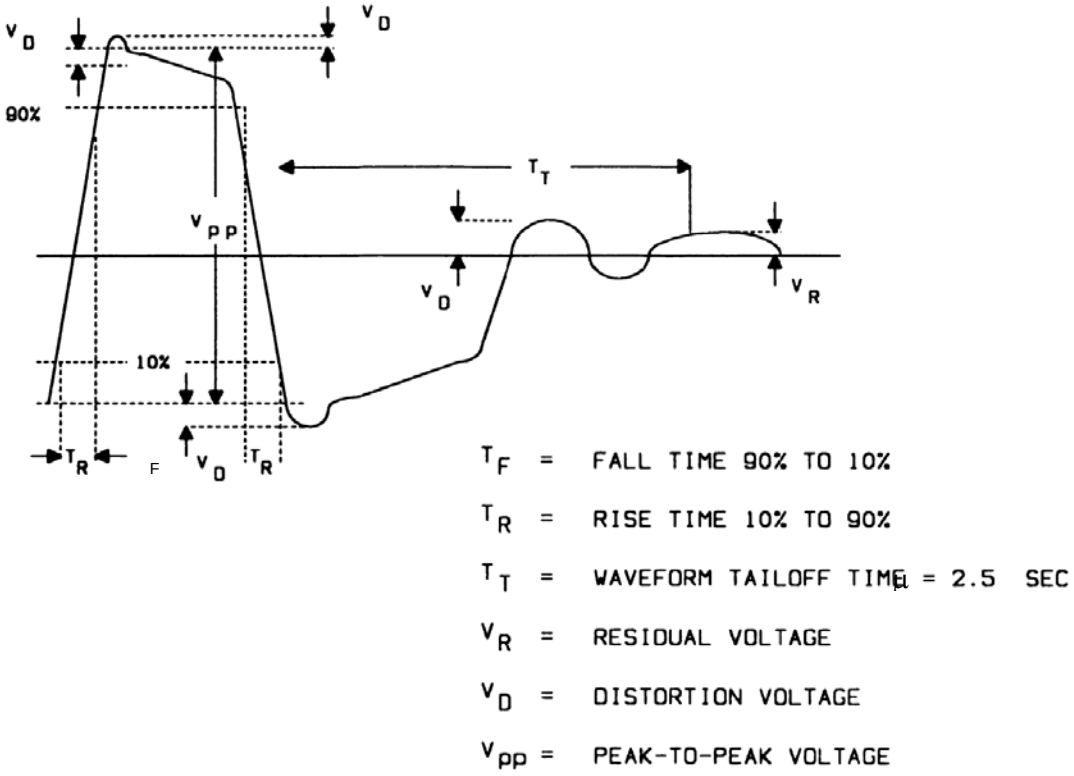


Figure 1. MIL-STD-1553 Waveform Measurements

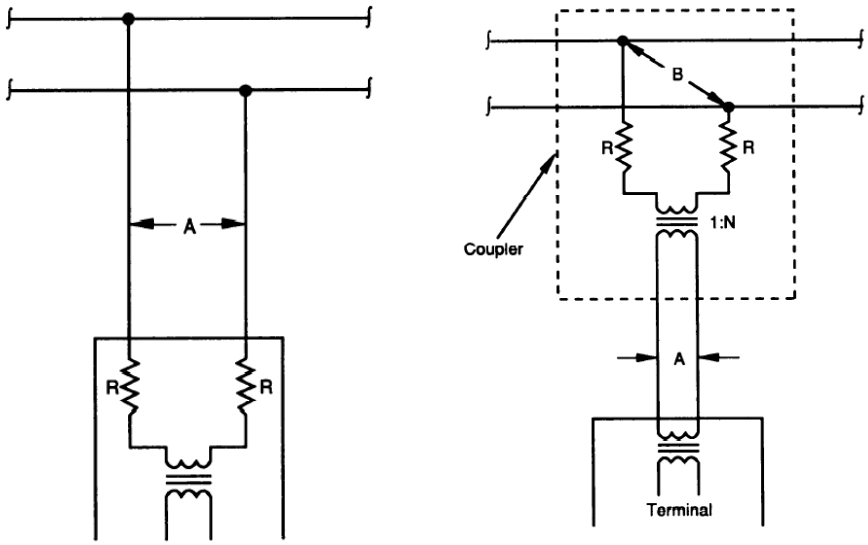
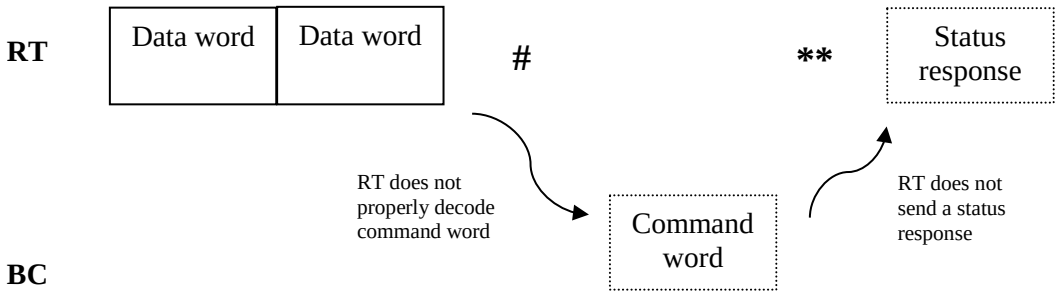


Figure 2. (Left) Direct-Coupled Bus / (Right) Transformer-Coupled Bus

2.2 How residual voltage affects the system

The residual voltage that a terminal produces at Point A of its transformer-coupled stub (Figure 2 right-hand side) is not likely to cause errors in other terminals because the voltage is transformed and voltage-divided by at least 75% by the time it reaches the stubs on all other terminals. However, if the terminal produces a residual voltage higher than the specification limit and a subsequent transmission targeted to that terminal immediately follows, this can result in message errors. The message errors will manifest themselves in several ways. Figure 3 illustrates a case in which a remote terminal produces a high residual voltage at the end of the last transmitted data word. In this case, the residual voltage interferes with the subsequent command word, and the remote terminal improperly decodes the command word, which forces the bus controller to record a no-response condition.

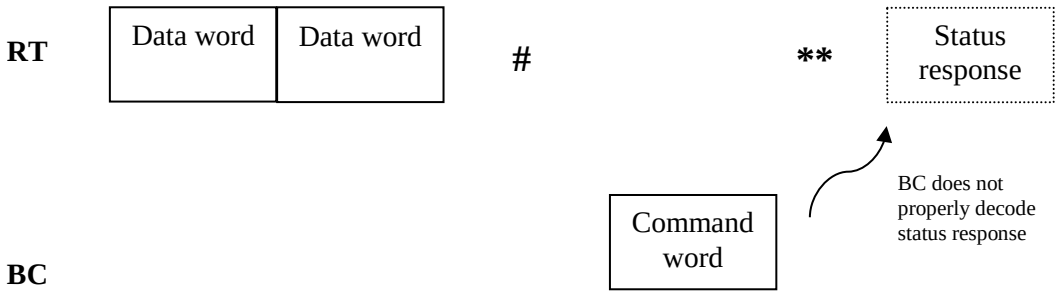


** Response time delay or gap

End-of-message delay or gap

Figure 3. Remote Terminal Residual Voltage Producing a Bus Error

Figure 4 illustrates a condition where a bus controller produces a high residual voltage. In this case, the remote terminal sends a valid status response but the bus controller does not properly decode the status word due to the residual voltage present. This also forces the bus controller to record a no-response condition.



** Response time delay or gap

End-of-message delay or gap

Figure 4. Bus Controller Residual Voltage Producing a Bus Error

2.3 Causes of Residual Voltage

This section describes MIL-STD-1553 waveforms that produce a residual voltage. Recall that residual voltage results from stored energy in the transformer, which accumulates when the transmitting waveform is not symmetrical about the system's neutral point. For reference, Figure 5 illustrates a perfectly balanced MIL-STD-1553 waveform.

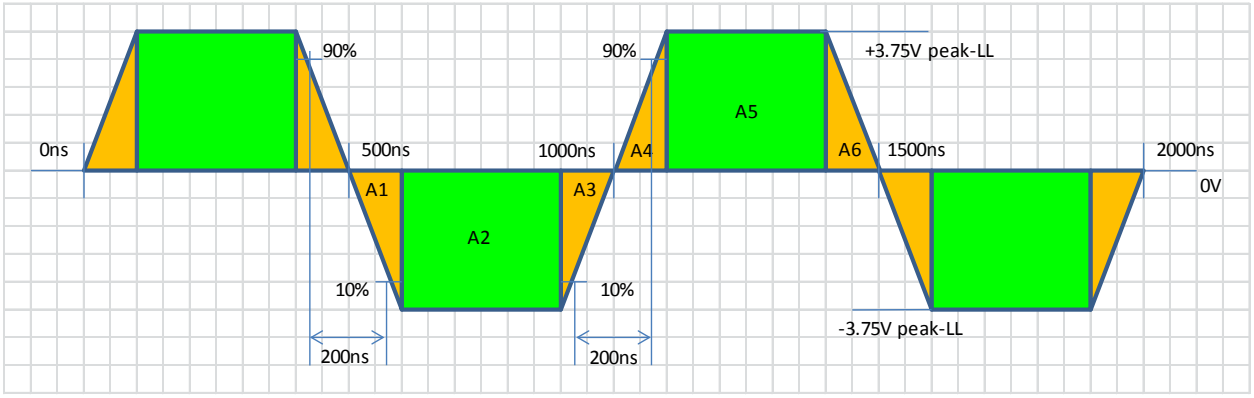


Figure 5. Example of a Perfectly Balanced MIL-STD-1553 Waveform

Characteristics of a perfectly symmetrical waveform include the following:

- Equal voltage amplitudes above and below ground
- Matching rise and fall times
- Zero crossings at intervals that are exact multiples of 500ns
- No signal distortion from overshoots/undershoots
- Half bit areas below the ground are equal to their half bit counterparts above ground (i.e. A1+A2+A3 = A4+A5+A6 in figure 5)

Several asymmetrical waveforms are common to the MIL-STD-1553 data bus, and the following sub-sections illustrate the most prevalent asymmetries.

2.3.1 Output Voltage Overshoot and Undershoot or Ringing

Output overshoots and undershoots result from leakage inductance in the transformer or by inconsistent current/voltage transients from the bus driver can result in residual voltage if the overshooting waveform is not equivalent to the undershooting waveform. Figure 6 illustrates an imbalanced overshoot/undershoot scenario.

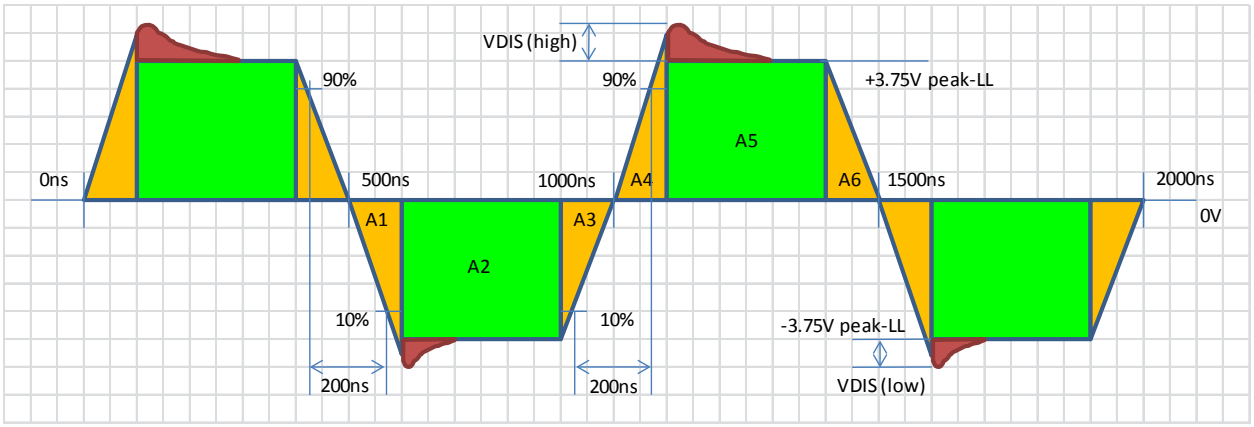


Figure 6. Under-damped waveform with output distortion evidenced by over/undershoot

In this case, the overshoot area is greater than the area within the undershooting waveform. The unequal areas accumulate with each bit of the transmitted message. Assuming all other waveform characteristics are matched, the total difference in overshoot and undershoot areas proportionally appear as residual voltage when the driver stops transmitting.

2.3.2 Over-damped or Slow Peaking Output Voltage

Over-damped output voltage occurs when the driver satisfies the MIL-STD-1553 rise and fall time requirements by covering 80% of the output amplitude within 100-300ns, but it enters a slower ramp in reaching the peak amplitudes. If the positive and negative drivers have well matched peak amplitude characteristics, output symmetry will remain balanced and negligible residual voltages will occur. However, if one of the differential drivers has a different peaking slope than the other, as shown in Figure 7, an energy storage imbalance occurs in the transformer and a proportional residual voltage resides on the bus after transmissions stop.

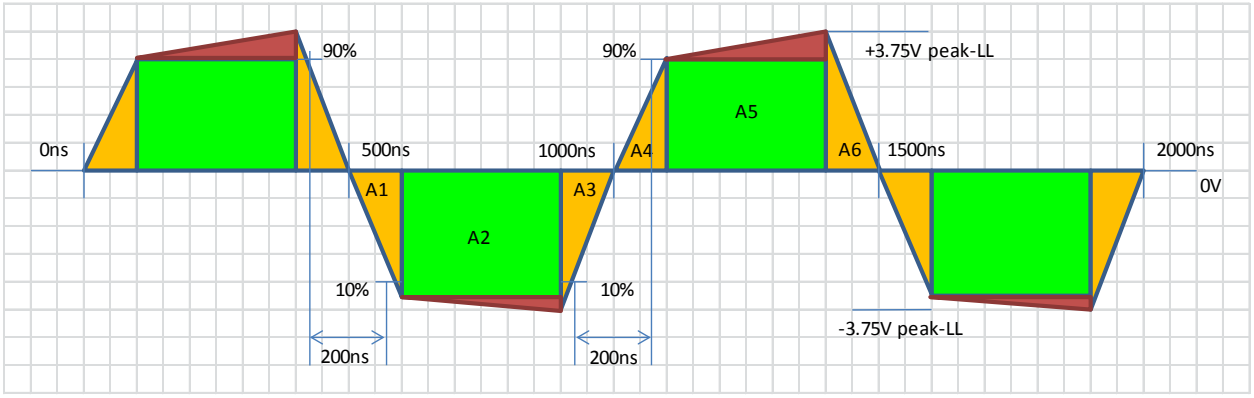


Figure 7. Over-damped waveform with output distortion evidenced by slow charging to the peak amplitude

2.3.3 Unequal Peak Amplitude Output Voltages

Similar to the over-damped waveform, differential drivers that produce positive peak voltages that are different from the negative peaks also create an energy imbalance. Figure 8 depicts the case where the positive driver attains a peak line-to-line, amplitude of 3V while the negative driver reaches a -3.75V peak, line-to-line, amplitude. Approximate the final residual voltage with the formula {[(A1+A2+A3) – (A4+A5+A6)] * # bits] * transformer's open circuit field collapse rate}.

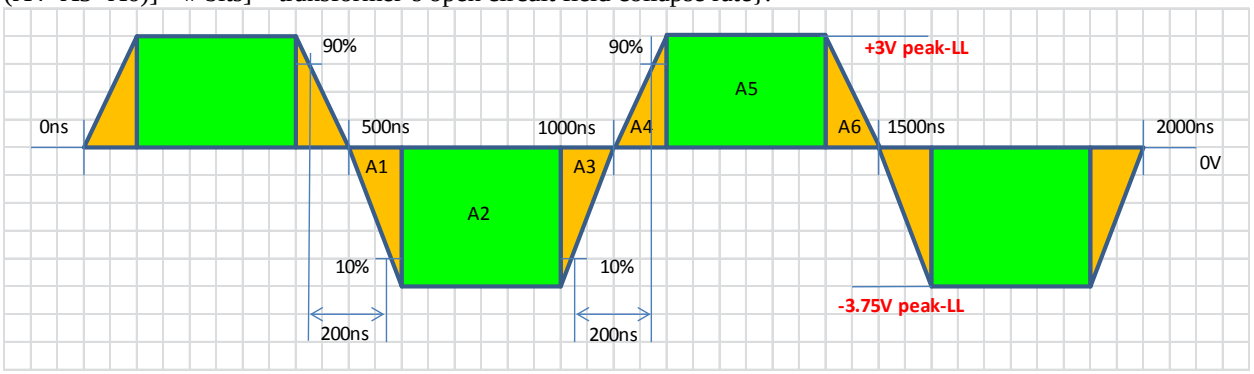


Figure 8. Unequal positive and negative amplitudes

2.3.4 Differences in Rise and Fall Times

A misconception exist that asymmetrical rise and fall times are a source of residual voltage. Differences in rise and fall time results in a balanced waveform unless the rise and fall asymmetry varies from bit-to-bit. Figure 9 demonstrates how unequal rise and fall times create a distorted trapezoid while the waveform maintains symmetry.

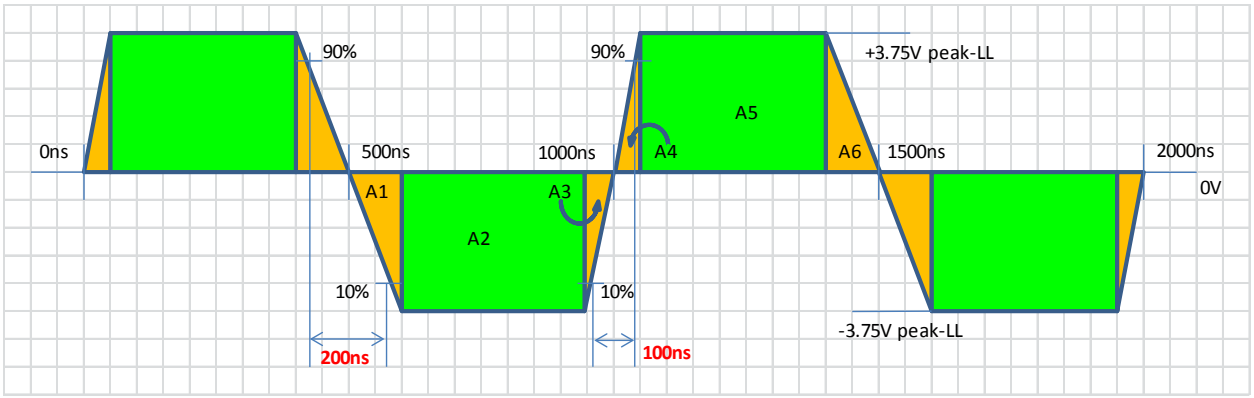


Figure 9. Rise and Fall time differences

Specifically, the area below 0V (e.g. A1+A2+A3) is equal to the positive area (e.g. A4+A5+A6). In other words, one could rotate the negative waveform about the 1000ns zero-crossing point and the waveforms would exactly overlap.

To break the symmetry a rise and fall time difference must vary between bits (as opposed to half-bit times) in the message. This scenario is extremely unlikely because it requires the transceiver to have a periodic bi-modal drive characteristic and/or a dependency on the message itself. For this purpose, rise and fall times are not a realistic source of residual voltage.

2.3.5 Zero Crossing Stability

MIL-STD-1553 specifies that a transmitting terminal with nominal zero-crossings every 500ns on two consecutive data bits must cross the zero-voltage reference point within ±25ns of each 500ns interval. If the zero-crossings modulate (e.g. because of jitter) around each 500ns nominal crossover point, a negligible residual voltage will accumulate. If, however, the zero crossings are consistently to one side of the nominal crossover point, then an energy imbalance accumulates.

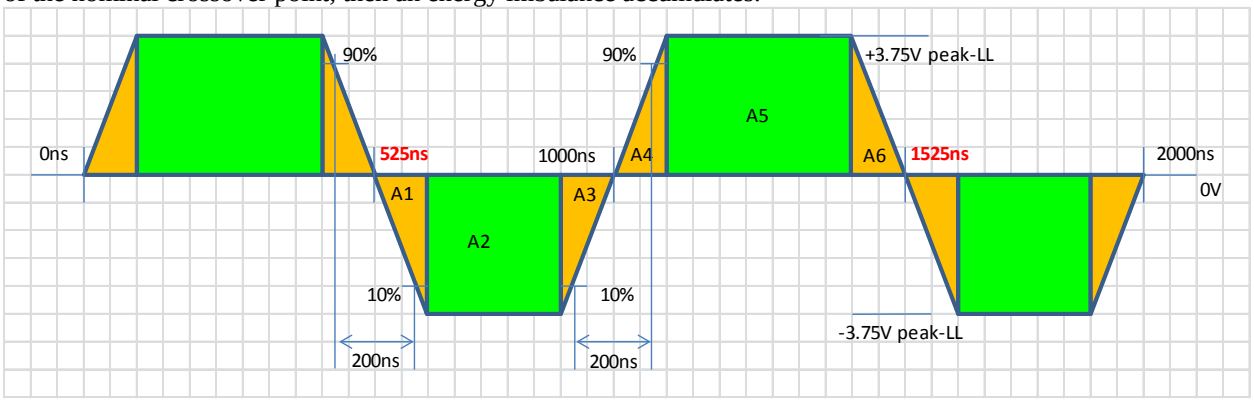


Figure 10. Zero-Crossing Stability (or Instability)

Figure 10 illustrates a MIL-STD-1553 waveform with nominal 500ns bit transitions where each positive pulse is 25ns longer than the ideal 500ns pulse width. Consequently, the negative pulse is 25ns shorter than ideal. The total positive pulse width minus the negative pulse width is 50ns. The area associated with this 50ns difference results in a proportional residual voltage.

2.4 Summary on Background Residual Voltage Discussion

The exaggerated asymmetries depicted in Figures 6-10 are often much more subtle on a bit-by-bit basis. Furthermore, the isolated, well-balanced, closed-loop nature of the MIL-STD-1553 bus results in a natural self-zeroing behavior on the bus, making it difficult to notice asymmetries. That said, non-idealities in the real world inevitably create a non-zero residual voltage on the MIL-STD-1553 bus following any transmission.

The remainder of this product advisory focuses on the findings from a residual voltage problem investigation, which focuses on transceiver-transformer interaction that appears to correlate well with residual voltage.

3.0 Major Investigation Findings

The investigation team isolated the anomalistic residual voltage to an interaction between the transceiver and transformer. All other likely factors such as power supply decoupling, board layout, clock integrity, assembly defects (e.g. cold solder joints), and bus side connector and cable harnessing were disqualified as significant residual voltage contributors in the application and board design.

The investigation team reduced the MIL-STD-1553 network to a minimal set of components – protocol, transceiver, transformer, and load resistor. A pair of oscilloscope probes were attached in a single-ended fashion to the primary terminals of the transformer while a second set of probes were connected differentially across the load resistor. The protocol device transmitted a 32-word message using a valid V_{OS} test pattern described in MIL-STD-1553 section 4.5.2.2.1.4. The investigation team captured the signal characteristics on the primary side during the transmission and recorded the associated residual voltage across the resistor. Figure 11 depicts the single-ended measurement configuration for this portion of the investigation and Figure 12 shows the associated waveforms and measurements.

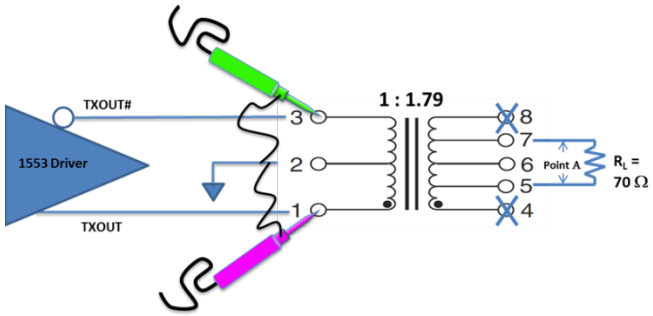


Figure 11. Test Configuration Used to Evaluate Transceiver-Transformer Interactions

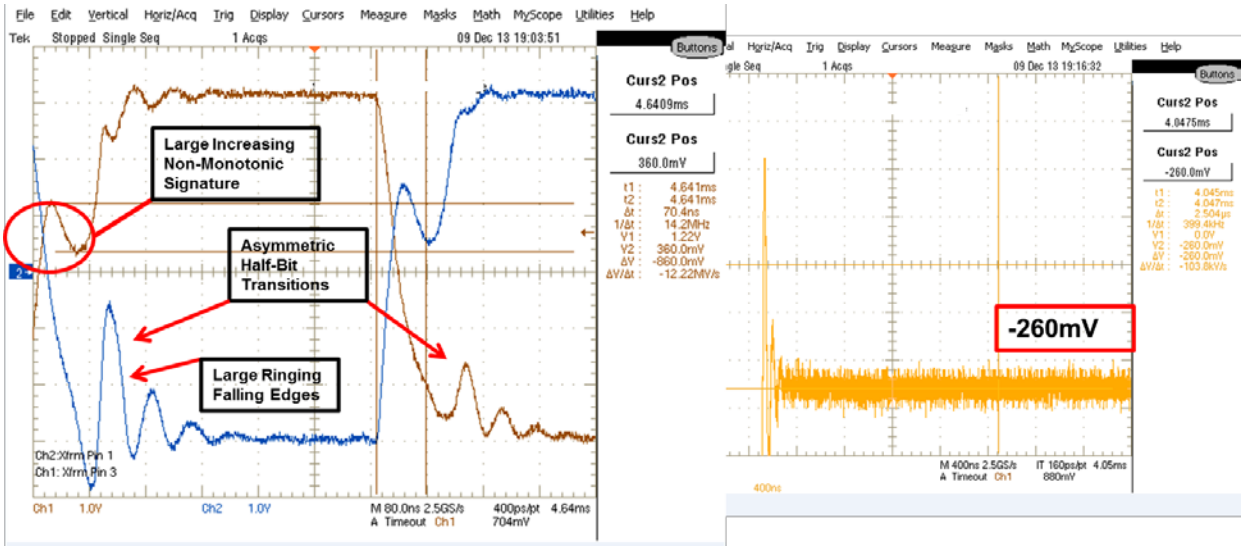


Figure 12. (Left) Waveforms on Primary Side of Isolation Transformer (Right) Final Residual Voltage on Secondary Side of Isolation Transformer (10mV below MIL-STD-1553 Specification Limit)

The waveforms on the isolation transformer primary terminals had a large amount of ringing. The blue waveform shows the TXOUT signal from the transceiver while the brown trace represents the TXOUT# signal. Therefore, the half-bit depicted on the left side of Figure 12 is a differential LOW pulse followed by the differentially positive half bit which occurs when the blue waveform rises. The distinctly different wave-shapes for each half bit are demonstrable evidence of asymmetric leakage inductances in the transformer's positive and negative windings. The transformer's bandwidth blocks the high frequency oscillations from reaching the secondary side of the transformer. Consequently, the blocked energy is lost – dissipated as heat in the system. Since the amount of energy blocking is different for each half-bit, a corresponding residual voltage arises reflecting the unequal energy transfer to the secondary side of the transformer. Proof of this asymmetry is shown by the right side of Figure 12, where the secondary side of the isolation transformer exhibits -260mV (-10mV below spec) of residual voltage at conclusion of the transmission.

Armed with the observations from Figure12, the investigation team proceeded to evaluate a variety of transformers from several vendors to validate its hypothesis that primary side leakage inductance imbalances are the leading factor to half-bit asymmetries and are the main source of residual voltages. Table 2 lists five transformers used in the analysis along with the leakage inductance for each transformer and the resulting residual voltage when each transformer interfaced to a single CAES UT69151-DXE protocol+transceiver module.

Table 2. Sample Transformers from Evaluation with Primary Leakage Inductance and Residual Voltage Measurements

Manufacturer	Transformer SN	Vr	Leakage Inductance $L_{1\text{-}2}$ µH's pin 5-pin 7 shorted all other pins open	Leakage Inductance $L_{2\text{-}3}$ µH's pin 5-pin 7 shorted all other pins open	Leakage Inductive Imbalance ($L_{1\text{-}2}$ - $L_{2\text{-}3}$) µH's	% of Leakage Inductance Imbalance
Vendor X	005	-41mV	0.469	0.314	0.155	20%
Vendor X	069	+39mV	0.295	0.436	-0.141	19%
Vendor X	207	+7mV	0.251	0.247	0.004	1%
North Hills	A	+12mV	0.411	0.385	0.026	3%
Pulse	586	+12mV	0.187	0.197	0.010	3%

Table 2 includes 3 transformers from the customer's selected vendor along with one transformer each from Aeroflex's recommended vendors – Pulse Electronics and North Hills Signal Processing Corp. CAES has generally recommended Pulse and North Hills transformers because these are the two suppliers whose transformers CAES used in the development of the transceivers listed in Table 1. Furthermore, it is the Pulse Electronics transformer that CAES uses in the production testing of its transceiver. Due to the long proven history of Pulse and North Hill transformers in successful MIL-STD-1553 network implementations, CAES strongly recommends the use of these two transformer vendors.

Notice the column indicating the residual voltage measured with each transformer when interfaced to a single UT69151-DXE in Table 2. In addition to the residual voltages, the last column lists the percentage of differential inductance mismatch for each transceiver. Comparing the two columns, one can see a relationship between the amount of inductive mismatch and the associated residual voltage. Figures 13 through 17 present the oscilloscope plots for each of the transformers in Table 2 interfacing to channel A on the same UT69151-DXE module.

The scope probes were connected to pins 1 and 3 on the transformer as depicted in Figure 11. Referencing the plots in Figures 13 through 17, the PINK trace is TXOUT and the GREEN trace is TXOUT#. The PURPLE trace is the mathematical addition of the TXOUT and TXOUT# signals. This is <u>not</u> differential addition, which would result in the conventional looking MIL-STD-1553 pp-ll waveforms. Instead, the addition of the two signals is intended to illustrate the amount of differential imbalance in the waveforms. If the waveforms were exactly balanced, the PURPLE trace would be exactly 0V throughout the measurement. More importantly, a difference in the total area beneath the PUPLE curve for each half-bit is indicative of the meaningful asymmetry that creates a residual voltage.

Since the PURPLE waveform during subsequent half-bit times is not identical, an imbalance is present. As a word of caution, the oscilloscope statistics shown in the following plots <u>do not</u> show the Delta-volts/Delta-time measurements for each half pulse. Therefore, you cannot quantitatively extrapolate the half-bit differences from these plots. However, the half-bit imbalances are sufficiently obvious to illustrate the relationship between these waveforms and their associated residual voltages.

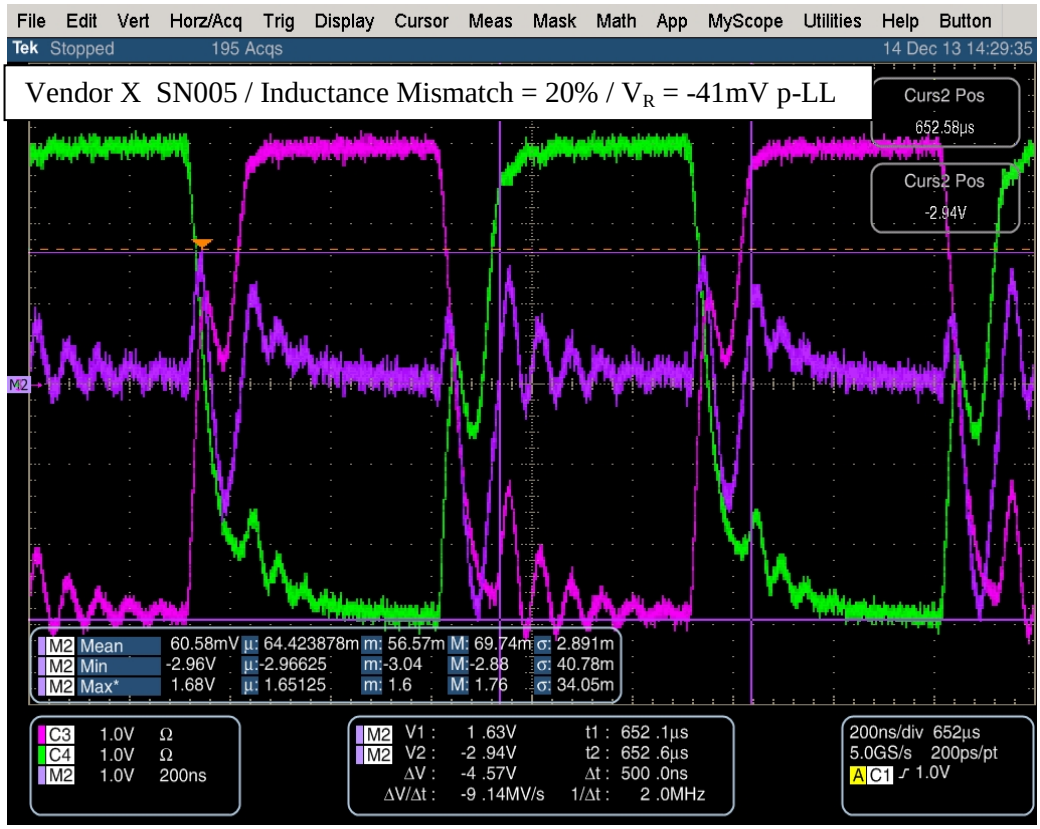


Figure 13. TXOUT & TXOUT# symmetry between UT69151-DXE CHA and Vendor X SN005

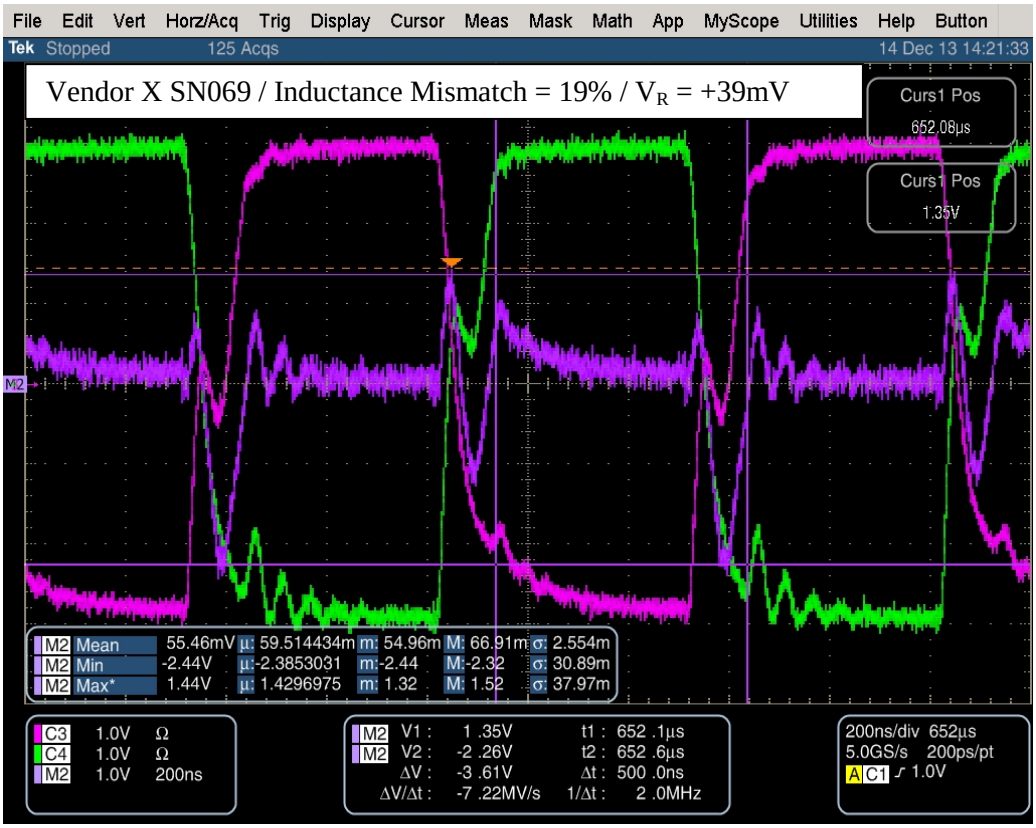


Figure 14. TXOUT & TXOUT# symmetry between UT69151-DXE CHA and Vendor X SN069

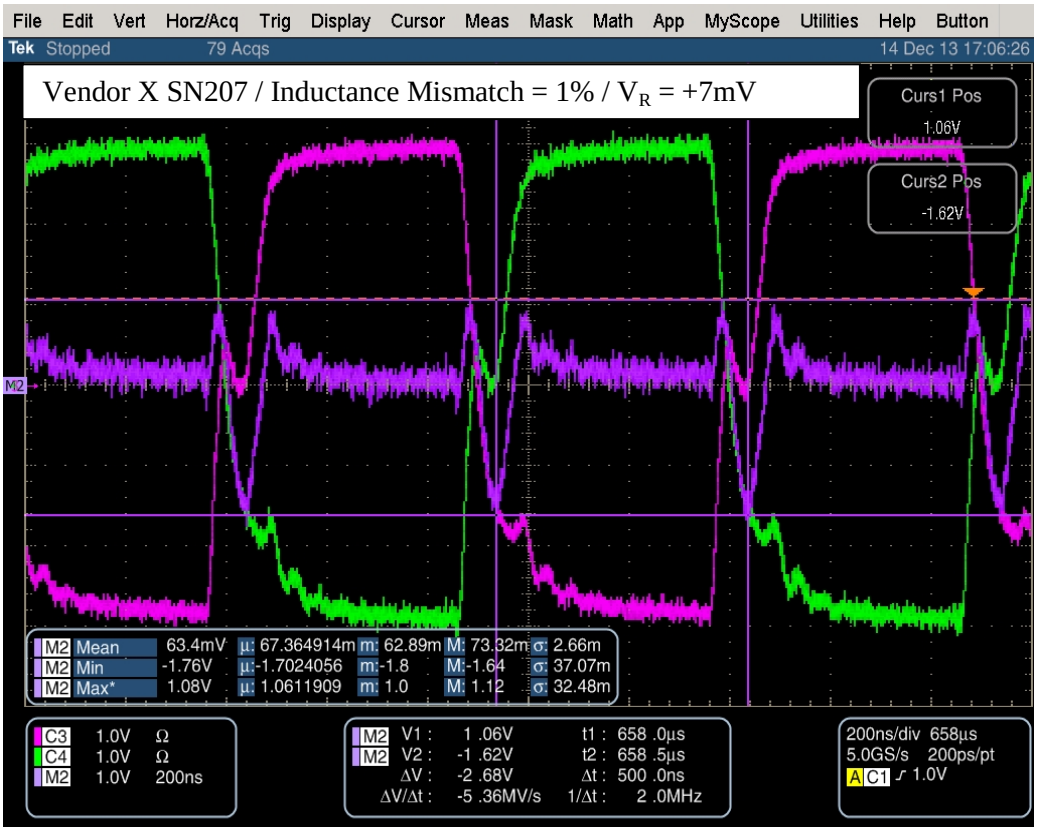


Figure 15. TXOUT & TXOUT# symmetry between UT69151-DXE CHA and Vendor X SN207

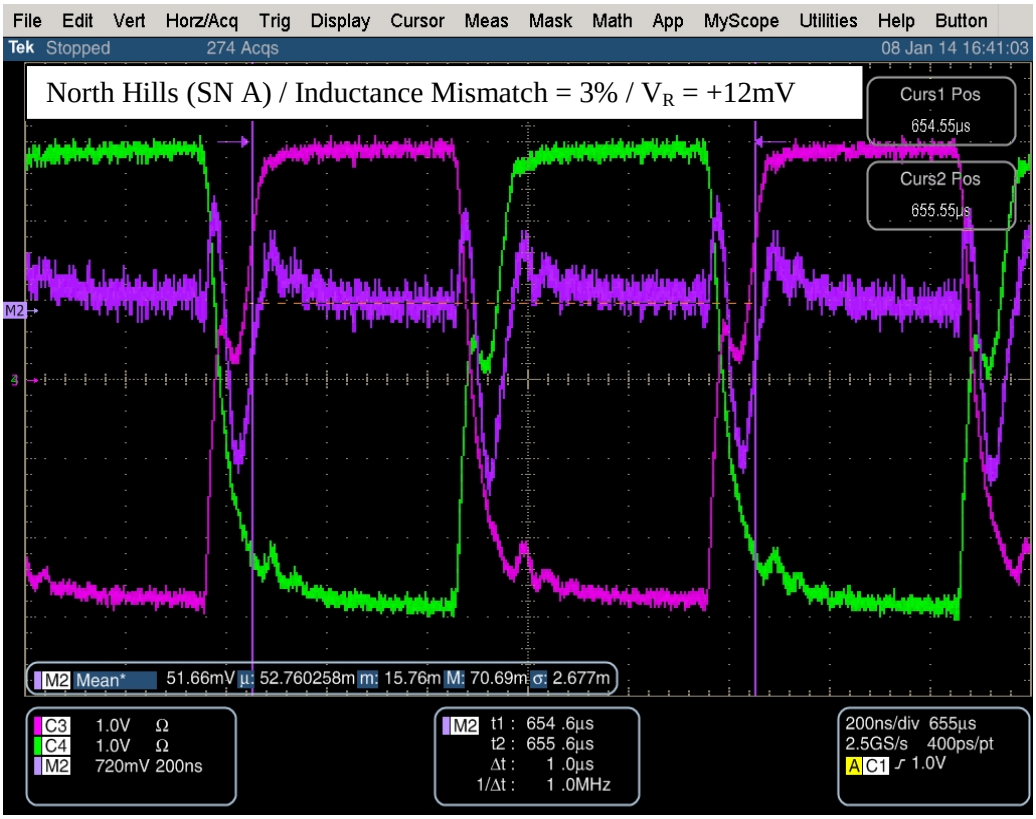


Figure 16. TXOUT & TXOUT# symmetry between UT69151-DXE CHA and North Hills SN A

** Note: The oscilloscope setup for the North Hills transformer experiment in Figure 16 represents the initial configuration. The remaining transformer experiments are subsequent to Figure 16 and reflect a higher sample rate and better display organization.

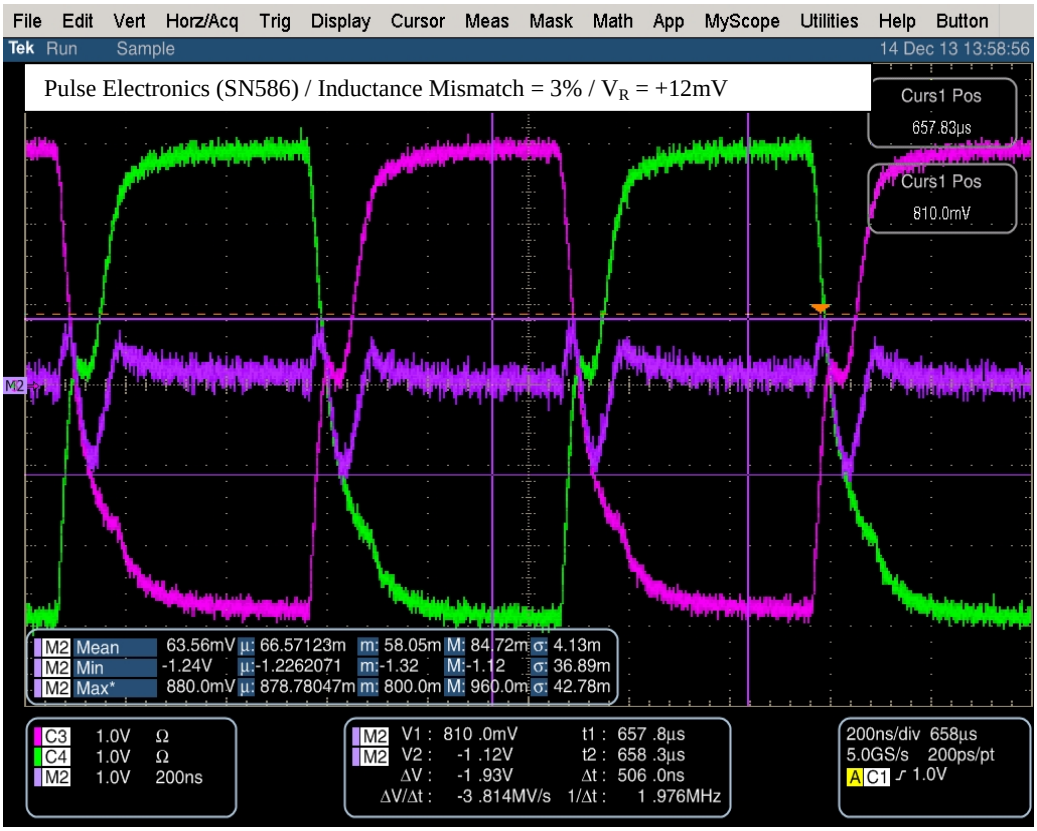


Figure 17. TXOUT & TXOUT# symmetry between UT69151-DXE CHA and Pulse SN586

Qualitatively, the Pulse brand transformer has the least distorted response to the UT69151-DXE transceiver interface. The North Hills transformer also has a good response to Aeroflex's transceiver. Vendor X's transformers, on the other hand, have a very inconsistent response. SN207 for example resulted in the lowest residual voltage of the five samples and exhibited a small amount of primary side signal distortion on par with the North Hills. However, the other two transformers from Vendor X exhibit a poor interaction with the UT69151-DXE transceiver and result in the highest degree of residual voltage. Note that the waveform and residual voltage seen in Figure 12 was produced by a fourth transformer from Vendor X.

Leakage inductance mismatch between the positive and negative legs on the primary side of the transformer is a major contributor to residual voltage. However, the correlation factor is still unclear. Transformers have additional characteristics that are not listed in the product specifications and are not readily extracted from parametric measurements of the transformers (i.e. permeability of the core material, reflected impedance mismatches, manufacturing techniques, etc.). Each of these plays a role in the compatibility between transceiver and transformer and their ability to efficiently transfer energy in a balanced way. Ultimately, the degree of "ringing" and asymmetry in successive half-bit times, as measured by signal distortion and voltage area analysis, is the best method to determine if a terminal is going to leave an unnecessarily high residual voltage on the MIL-STD-1553 data bus.

4.0 Recommendations

CAES recommends that system designers continue to use Pulse or North Hills transformers for interfacing with CAES transceivers. We also recommend additional parametric screening for transformers with a sorting preference toward balanced primary side leakage inductances and reflected impedances. Transformer datasheets exclude many relevant parameters as shown in the Pulse Electronics specification for the 1553-45 transformer in Appendix A of this advisory. Appendix B presents parametric screening gathered by CAES engineers when characterizing transformers beyond what is gleaned from the manufacturer's specification. The data contained in Appendix B is data measured on the Pulse 1553-45 transformer.

CAES also recommends an evaluation of primary side signal integrity and half-bit time balance vs. residual voltage during brass board and engineering model checkout. If the circuit board uses a transformer vendor other than Pulse or North Hills, CAES strongly encourages the system designer to perform a compatibility analysis.

5.0 Conclusion

The system designer must consider many important factors when implementing a MIL-STD-1553 terminal. Achieving optimal performance and compliance to MIL-STD-1553 is a function of the components employed (e.g. clocking, protocol handler, transceiver, transformer, and connectors) as-well-as circuit implementation decisions such as board layout, ground planes, signal routing and decoupling. This product advisory focuses the component-driven contribution to residual voltage in a MIL-STD-1553 network and discusses how to minimize it through wise component selection.

CAES made efforts to correlate residual voltage with leakage inductance, primary and secondary side inductance, and winding resistance of various transformers. Within the closed-loop system of the MIL-STD-1553 protocol device, all of the parameters interact with each other, often times cancelling the unbalancing effects of each other. For this reason, no single parametric characteristic precisely predicts residual voltage. Apart from the parametric characteristics that are readily measurable, manufacturing techniques and materials employed by the various manufacturers also affect transformer performance.

Although it is difficult to ascertain the exact parameter that will eliminate residual voltage for a given MIL-STD-1553 terminal, the investigation team found leakage inductance to be the most predictive parametric indicator of residual voltage. The presence of leakage inductance is most evident when evaluating signal integrity of the waveforms on the primary side of the isolation transformers. Measuring signal quality on the primary side of the isolation transformer is a high fidelity indicator of inefficient and/or imbalanced energy transfer onto point A of the MIL-STD-1553 bus..

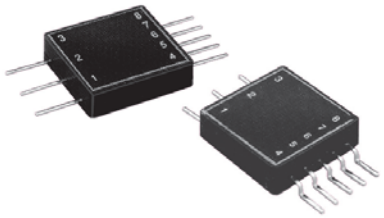
Using proven transformer vendors who have a demonstrated history of reliable, problem free, interoperation with the selected transceivers affords the system designer the highest probability of success. For the purpose of matching transformers to the CAES components listed in Table 1, Pulse Electronics (http://www.pulseelectronics.com) and North Hills Signal Processing Corp. (http://www.nhsignal.com) are proven MIL-STD-1553 transformer suppliers.

Appendix A

MIL-STD-1553 Transformers

Low Profile SMT non-QPL InterfaceTransformers

Pulse Electronics



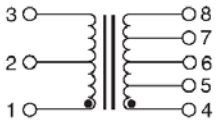
These non-QPL interface transformers are built and tested in ISO 9001 approved facilities. They conform to all electrical and physical parameters of MIL-PRF-21038/27. Choose one of three operating temperature ranges including 0° to +70°C, -40° to +85°C, or -55° to +125°C.

- Dual ratio, single interface (see schematic)
- Surface Mount, flat pack or gull wing package
- For use in MIL-STD-1553 applications
- Low profile, 0.155 inches height
- Performance to MIL-PRF-21038 requirements
- Built in ISO 9001 facility
- Applicable specifications:
  - MIL-STD-1553B
  - MIL-PRF-21038
  - MIL-STD-202
  - ISO 9001

Operating Temperature	Flat Pack Prefix	Gull Wing Prefix
0° to 70°C	FLC	GLC
-40° to +85°C	FLN	GLN
-55° to +125°C	FL	GL

Summary Performance Specifications	
Impedance	(see table below)
Droop	20%
Overshoot	±1V MAX
Common Mode Rejection (CMR)	45dB
Frequency Range (no load)	75kHz to 1MHz
Operating Temperature Range	(see table above)
Weight	5 grams
Insualtion Resistance (MIN)	10K MΩ @ 250Vdc
Dielectric Withstanding Voltage	100Vrms

Schematic



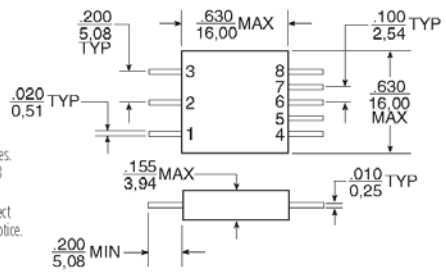
Characteristics				
Part Number [1]	Terminals	Ratio (±3%)	RDC (Ω MAX)	Impedance (Ω MIN)
(XXX)1553-1	1-3 : 4-8 1-3 : 5-7	1CT:1CT 1CT:.707CT	1-3 = 3.0 4-8 = 3.0	(1-3) 4,000
(XXX)1553-2	1-3 : 4-8 1-3 : 5-7	1.4CT:1CT 2CT:1CT	1-3 = 3.5 4-8 = 3.0	(1-3) 7,200
(XXX)1553-3	1-3 : 4-8 1-3 : 5-7	1.25CT:1CT 1.66CT:1CT	1-3 = 3.2 4-8 = 3.0	(1-3) 4,000
(XXX)1553-5 [2]	1-3 : 4-8 1-3 : 5-7	1CT:2.12CT 1CT:1.5CT	1-3 = 1.0 4-8 = 3.5	(4-8) 4,000
(XXX)1553-45 [2]	1-3 : 4-8 1-3 : 5-7	1CT:2.5CT 1CT:1.79CT	1-3 = 1.0 4-8 = 3.5	(4-8) 4,000

NOTE: 1. Refer to prefix table (above) to select temperature range. **2.** Designed for transceivers utilizing a single supply voltage (+5V).

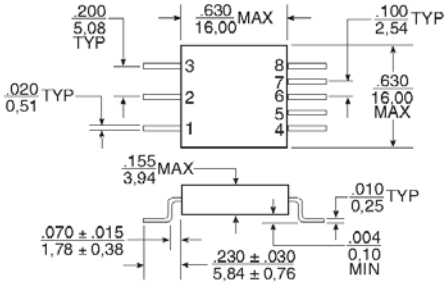
Mechanicals

Notes:
1. All dimensions: in inches.
2. Tolerances: .xx = +.008
3. All specifications and dimensions are subject to change without notice.

Flat Pack



Gull Wing



MIL-PRF-21038/27 Inspection, Sampling, Testing

Table 1 — Group A Inspection

Level "C"**		Level "M"		Level "T"	
Tests	**Sampling Plan**	**Tests**	**Sampling Plan**	**Tests**	**Sampling Plan**
N/A	N/A	Electrical Characteristics per MIL-PRF-21038/27	Sample per Table 3	Thermal Shock	100%
N/A	N/A	Visual and Mechanical Inspection	Sample per Table 3	Winding Continuity	100%
N/A	N/A	N/A	N/A	Electrical Characteristics per MIL-PRF-21038/27	100%
N/A	N/A	N/A	N/A	Impedance	Sample per Table 3
N/A	N/A	N/A	N/A	Visual and Mechanical Inspection	Sample per Table 3

Table 2 — Group B Inspection

Level "C"**		Level "M"		Level "T"	
Tests	**Sampling Plan**	**Tests**	**Sampling Plan**	**Tests**	**Sampling Plan**
N/A	N/A	Dielectric Withstanding Voltage	Sample per Table 3	Dielectric Withstanding Voltage	Sample per Table 3
N/A	N/A	Insulation Resistance	Sample per Table 3	Insulation Resistance	Sample per Table 3

Table 3 — Sampling Plans for Group A and Group B Inspections

Lot Size	Group A, Group II Inspections	Group B
1 to 5	All	All
6 to 13	All	5
14 to 50	13	5
51 to 90	13	7
91 to 150	13	11
151 to 280	20	13
281 to 500	29	16
501 to 1200	34	19
1,201 to 3,200	42	23
3,201 to 10,000	50	29

****NOTE:** Parts ordered to Level C are certified to comply with MIL-PRF-21038 Level C, however testing is performed per manufacturer's internal requirements and sampling rates.

For More Information

Pulse North America Headquarters
Two Pearl Buck Court
Bristol, PA 19007
U.S.A.
Tel: 215 781 6400
Fax: 215 781 6403

Pulse Europe
Zeppelinstrasse 15
71083 Herrenberg
Germany
Tel: 49 7032 7806 0
Fax: 49 7032 7806 12

Pulse China Headquarters
B402, Shenzhen Academy of Aerospace Technology Bldg.
10th Kejinan Road
High-Tech Zone
Nanshan District
Shenzen, PR China 518057
Tel: 86 755 33966678
Fax: 86 755 33966700

Pulse North China
Room 2704/2705
Super Ocean Finance Ctr.
2067 Yan An Road West
Shanghai 200336
China
Tel: 86 21 62787060
Fax: 86 2162786973

Pulse South Asia
135 Joo Seng Road
#03-02
PM Industrial Bldg.
Singapore 368363
Tel: 65 6287 8998
Fax: 65 6287 8998

Pulse North Asia
3F No. 198, Zhongyuan Road
Zhongli City
Taoyuan County (32068)
Taiwan
Tel: 886 3 4356768
Fax: 886 3 4356823

Appendix B

1553-45 TRANSFORMER

	IMPEDANCE	
Z1-3	4-8 OPEN	
FREQ, KHZ	MAG Z, KΩ	ANGLE Z, DEGREES
75	1.857	55
100	2.562	46
200	7.936	2.4
269	13.000	0
300	11.660	-34
400	6.420	-53
500	4.337	-64
600	3.312	-70
700	2.700	-74
800	2.288	-77
900	1.992	-79
1000	1.767	-80

5-7 70 OHM TERM	Z 1-2	Z 2-3
FREQ, KHZ	MAG Z, OHMS	MAG Z, OHMS
75	5.828	5.827
500	5.873	5.879
1000	5.992	6.013

4-8 140 OHM TERM	Z 1-2	Z 2-3
FREQ, KHZ	MAG Z, OHMS	MAG Z, OHMS
75	5.941	5.938
500	5.967	5.963
1000	6.038	6.032

INDUCTANCE		UNITS
L1-3	4.22	mH
L4-8	23.69	mH
L1-2	1.14	mH
L2-3	1.14	mH
L7-5	12.37	mH
4-8 SHORTED		
LL1-2	0.105	uH
LL2-3	0.108	uH
LL1-3	0.358	uH
7-5 SHORTED uH		
LL1-2	0.171	uH
LL2-3	0.181	uH
TURNS RATIO		
L1-3/4-8	2.369	
L1-2/4-8	4.559	
L2-3/4-8	4.559	
L1-3/7-5	1.712	
L1-2/7-5	3.294	
L2-3/7-5	3.294	
DC RESISTANCE		
L1-3	0.466	Ohms
L1-2	0.228	Ohms
L2-3	0.243	Ohms
L4-8	2.61	Ohms
L7-5	1.68	Ohms