Part Number: QSFP-100G-CWDM4-S

QSFP-100G-CWDM4-S OVERVIEW

The QSFP-100G-CWDM4-S Optical Transceiver is a full duplex, photonic-integrated optic transceiver that provides a high-speed link at aggregated data rate of 103.13 Gbps over 2 km of single mode fiber with a maximum link budget of 8 dB when maximum transmitter and dispersion penalty (TDP) of 3 dB is presented. The transceiver four lasers with center wavelengths of 1271 nm, 1291 nm, 1311 nm and 1331 nm. The optical signals are then multiplexed into a single-mode fiber through an industry standard LC connector. On the receive side, four lanes of optical data streams are optically de-multiplexed by an integrated optical demultiplexer and transformed to an electrical CAUI-4 compliant output driver. This module features a hot-pluggable electrical interface, low power consumption and 2-wire I2C management interface.

PRODUCT FEATURES

- Optical line rate of 103.125 Gbps (4 x 25.78125 Gbps)
- Requires host system to enable RS-FEC RS (528,514) in accordance with IEEE802.3 clause 91
- Supports up to 5 dB channel insertion loss including up to 2 km of single mode fiber
- Operating case temperature range of 0ºC to 70ºC
- Tx and Rx re-timers
- External reference clock is not required
- Power dissipation < 3.5 W
- Single 3.3 V power supply
- Integrated CWDM TOSA/ROSA
- Duplex single mode LC optical receptacle
- 100G CWDM4 MSA Technical Specification Rev 1.0 compliant
- CAUI-4 chip-to-module 100G four-lane electrical interface per IEEE 802.3 Annex 83E compliant
- Supports digital diagnostic monitoring
- Hot pluggable 38-pin electrical interface
- 2-wire I2C management interface
- Green handle

APPLICATIONS

- Local area network (LAN)
- Wide area network (WAN)
- Ethernet switches and router applications

FUNCTIONAL DESCRIPTION

The QSFP-100G-CWDM4-S Optical Transceiver is a full duplex device with both transmit and receive functions contained in a single module. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector. The module provides a high speed link at an aggregated signaling rate of 103.125 Gbps. It is compliant with: 100G CWDM4 MSA Technical Specification Rev 1.0 and the IEEE 802.3bm CAUI-4 chip-to-module electrical specifications at 103.125 Gbps. The two-wire management interface complies with SFF-8636. The transceiver mechanical design complies with SFF-8661 and the base electrical design complies with SFF-8679. A block diagram is shown in Figure 1.

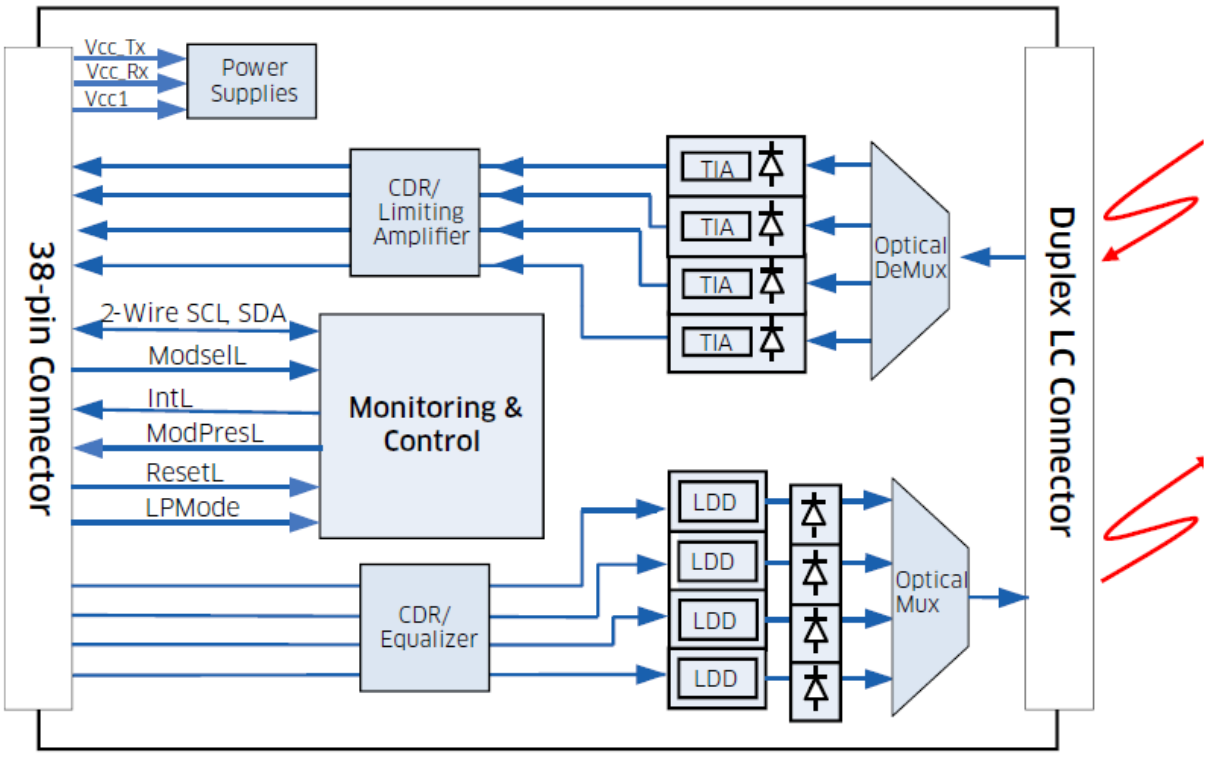

Figure 1: Functional block diagram

TRANSMITTER

The transmitter path converts four lanes of serial NRZ electrical data from line rate of 25.78 Gbps to a standard compliant optical signal. Each signal path, accepts a 100 Ω differential 100 mV peak-to-peak to 900 mV peak-to-peak electrical signal on TDxn and TDxp pins. Inside the module, each differential pair of electric signals is input to an equalizer and then to a CDR (clock-data recovery) chip. The recovered and retimed signals are then passed to a laser driver which transforms the small swing voltage to an output modulation that drives an un-cooled EML laser. The laser drivers control four EMLs with center wavelengths of 1271 nm, 1291 nm, 1311 nm and 1331 nm, respectively. The optical signals from the four lasers are optically multiplexed and coupled to single-mode optical fiber through an industry standard LC optical connector. The optical signals are engineered to meet the CWDM4 MSA specifications.

RECEIVER

The receiver takes incoming combined four lanes of DC balanced CWDM NRZ optical data from line rate of 25.78 Gbps through an industry standard LC optical connector. The four incoming wavelengths are separated by an optical demultiplexer into four separated channels. Each output is coupled to a PIN photodetector. The electrical currents from each PIN photodetector are converted to a voltage in a high-gain transimpedance amplifier. The electrical output is recovered and retimed by the CDR chip. The four lanes of reshaped electrical signals are output on the RDxp and RDxn pins as a 100 Ω differential CAUI-4 chip-to-module signals.

LOW-SPEED SIGNALING

QSFP-100G-CWDM4-S Optical Transceiver has several low-speed interface connections including a 2-wire serial interface (SCL and SDA). These connections include; Low Power Mode (LPMode), Module Select (ModSelL), Interrupt (IntL), Module Present (ModPrsL) and Reset (ResetL) as shown in Figure 1.

MODSELL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is “High”, the module does not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP28 modules are deselected. Similarly the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-assertion periods of different modules may overlap as long as the above timing requirements are met.

RESETL

The ResetL pin is pulled up to Vcc inside the QSFP28 module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts upon the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal

with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMODE

The LPMode pin is pulled up to Vcc inside the QSFP28 module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93, bits 0,1). The module has two modes: a low power mode and a high power mode. The high power mode operates in one of the four power classes. When the module is in a low power mode it has a maximum power consumption of 1.5 W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

The module's 2-wire serial interface and all laser safety functions are fully operational in this low power mode. The module still supports the completion of reset interrupt in this low power mode.

The Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that our module has power consumption greater than 1.5 W. When the module is in low power mode, the module will reduce its power consumption to less than 1.5 W while still maintaining the functionality above. However, the Tx or Rx may not be operational in this state.

The module will be in low power mode if the LPMode pin is in the high state, or if the Power_over-ride bit is in the high state and the Power_set bit is also high. The module will be in high power mode if the LPMode pin is in the low state, or the Power_over-ride bit is high and the Power_Set bit is low. Note that the default state for the Power_over-ride bit is low. A truth table for the relevant configurations of the LPMode and the Power_over-ride and Power_set is shown below. At power up, the Power_over-ride and Power_set bits are set to 0.

POWER MODE TRUTH TABLE

LPMode	Power Over-ride bit	Power_set Bit	Module Power Allowed
1	0	X	Low Power
0	0	X	High Power
X	1	1	Low Power
X	1	0	High Power

MODPRSL

ModPrsL is pulled up to V_{cc}_Host on the host board and grounded in the module. The ModPrsL is "Low" when the module is inserted and "High" when the module is physically absent from the host connector.

INTL

IntL is an output pin. “Low” indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to host supply voltage on the host board.

APPLICATION SCHEMATICS

An example application schematic (reference SFF 8679) showing connections from a host IC and host power supply to the SO-QSFP28-CWDM4 Optical Transceiver is shown in Figure 2.

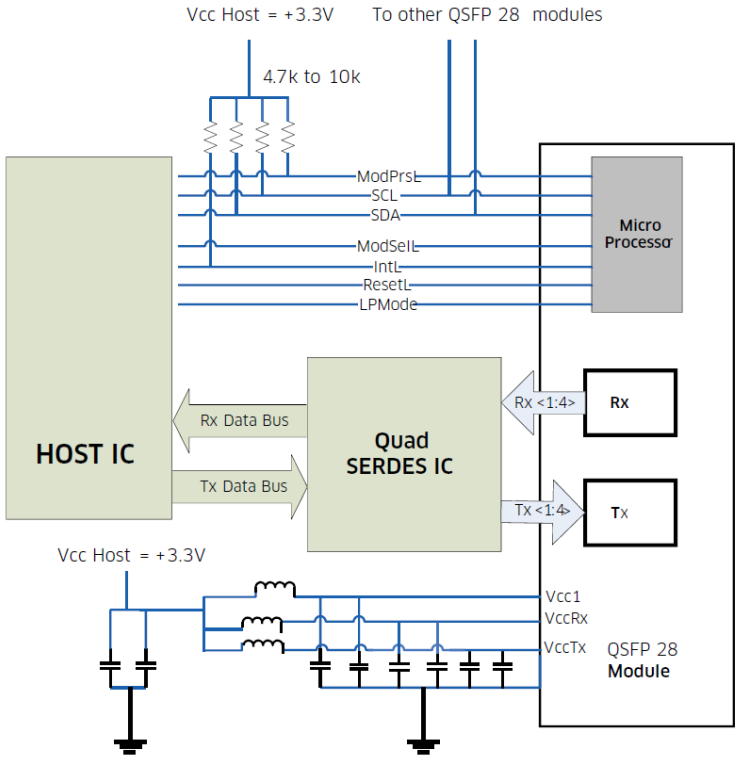

Figure 2: Typical application schematics.

QSFP28 CWDM4 modules are hot pluggable and active connections are powered by individual power connection at 3.3 V nominal voltage. Multiple modules can share a single 3.3 V power supply with individual filtering. To limit wide band noise power, the host system and module shall each meet a maximum of 2% peak-to-peak noise when measured with a 1 MHz low pass filter. In addition, the host system and the module shall each meet a maximum of 3% peak-to-peak noise when measured with a filter from 1 MHz - 10 MHz. A module will meet all electrical requirements and remain fully operational in the presence of noise on the 3.3V power supply. Power supply filtering components should be placed as close to the V_{cc} pins of the host connector as possible for optimal performance.

Note: Decoupling Capacitor values vary depending on the application.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{ST}	-40	+85	°C
Relative humidity (noncondensing)	RH	5	85	%
Static electrical discharge (human body model). 1 kV for high speed lines. 2 kV for others	ESD		1000	V
Power supply voltages	$V_{CC}3$, max	-0.3	3.6	V
Receive damage threshold	P_{DMG}		3.5	dBm (per lane)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	3.135	3.3	3.465	V
Operating case temperature	T_{OP}	0		+70	°C
Signal rate (per channel) 1	fD		25.78125		Gbps
Operating range	m	2		2000	m

LOW SPEED ELECTRICAL CHARACTERSTICS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Currents and Voltages						
Voltage	V_{CC}	3.135	3.3	3.465	V	With respect to GND
Supply current	I_{cc}			1118	mA	
Power dissipation						
Power dissipation (low power mode)	P_{lp}			1.5	W	
Low speed control and sense signals (detailed specification in SFF-8679 Rev 1.6)						
Outputs (Interrupt, ModPrsL)	V_{OL}	0		0.4	V	R_{pullup} pulled to host _V_{CC} measured at host side of connector. I_{OL} (max)=2mA
Outputs (Interrupt, ModPrsL)	V_{OL}	host_V_{CC} − 0.5		host_V_{CC} + 0.3	V	R_{pullup} pulled to host _V_{CC} measured at host side of connector.
Inputs (ModSelL, ResetL, LPMode)	VIL	−0.3		0.8	V	Pulled up in module to $V_{CC}3$
Inputs (ModSelL, ResetL, LPMode)	V_{IH}	2		V_{CC} 3 + 0.3	V	Pulled up in module to $V_{CC}3$
SCL and SDA inputs	V_{IL}	−0.3		$V_{CC}3$ * 0.3	V	R_{pullup} pulled to host _V_{CC} measured at QSFP+ side of connector

SCL and SDA inputs	V_{IH}	$V_{CC}3$ * 0.7	$V_{CC}3$ + 0.5	V	R_{pullup} pulled to host _V_{CC} measured at QSFP+ side of connector

ELECTRICAL INPUT AND OUTPUT SQUELCH BEHAVIOR

QSFP-100G-CWDM4-S is compliant to the Tx and Rx squelch behavior described in SFF-8636 section 6.6.2 and will be indicated in Page 00h, Byte 194, bit 0:3. Rx(n)(p/n) are QSFP28 module receiver data outputs. Output squelch for loss of optical input signal, hereafter Rx Squelch, is supported by the SO-QSFP28-CWDM4. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. For the SO-QSFP28-CWDM4, squelch and output disable is controlled for each channel using bytes 240 and 241 of page 03h. Writing a '1' in the Squelch Disable register (byte 240, page 03h) disables the squelch for the associated channel. Writing a '1' in the Output Disable register (byte 241, page 03h) squelches the output of the associated channel. When a '1' is written in both registers for a channel, the associated output is disabled.

QSFP-100G-CWDM4-S will disable Tx Squelch Function as default. Tx(n)(p/n) are QSFP28 module transmitter data inputs and Tx Squelch is implemented to reduce OMA only (Page 00h, Byte 195, bit 2=0b). For details regarding Tx Squelch behaviors, please contact FluxLight to learn more.

MODULE CTLE BEHAVIOR

The QSFP-100G-CWDM4-S supports continuously automatic (adaptive) equalization with non-readable CTLE gain. Please contact FluxLight for details if manual (programmable) equalization is preferred.

REGULATORY COMPLIANCE

The QSFP-100G-CWDM4-S is RoHS 6/6 compliant and complies with international EMC (Electromagnetic Compatibility) and product safety requirements and standards.

TIMING REQUIREMENT OF CONTROL AND STATUS I/O

Parameter	Symbol	Max	Unit	Notes
Initialization time	t_init	2000	ms	Time from power on, hot plug or rising edge of reset until the module is fully functional. This time does not apply to non-power level 0 modules in low-power state
Reset Init assert time	t_reset_init	2	µs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Serial bus hardware ready time	t_serial	2000	ms	Time from power on until the module responds to data transmission over the 2-wire serial bus
Monitor data ready time	t_data	2000	ms	Time from power on to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset assert time	t_reset_init	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional
LPMode assert time	ton_ LPMode	100	µs	Time for assertion of LPMode (Vin: LPMode=Vin) until module power consumption reaches power level 1
LPMode deassert time	Toff_ LPMode	300	ms	Time for deassertion of LPMode (Vin:LPMode=Vil) until module is fully functional
IntL assert time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL deassert time	toff_IntL	500	µs	Time from clear on read operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx Los, Tx Fault and other flag bits
Rx LOS assert time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set (Value = 1b) and IntL asserted.
Tx Fault assert time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted
Flag assert time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted
Mask assert time	ton_mask	100	ms	Time from mask bit set (Value = 1b) until associated IntL assertion is inhibited
Mask deassert time	toff_mask	100	ms	Time from mask bit set (Value = 0b) until associated IntL operation resumes
Application or rate select change time	t_ratesel	100	ms	Time from change of state of Application or Rate Select bit until transmitter or receiver bandwidth is in conformance with appropriate specification, Not applicable
Power_over-ride or power-set assert time	ton_Pdown	100	ms	Time from P_Down bit set (Value = 1b) until module power consumption reaches Power Level 1
Power_over-ride or power-set deassert time	toff_Pdown	300	ms	Time from P_Down bit set (Value = 0b) until module is fully

				functional	

OPTICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Typ	Max	Unit	Notes
Signaling rate, each lane		25.78125 ± 100 ppm		GBd	
The following specifications are applicable within the operating case temperature range					
Optical modulation amplitude, each lane	OMA	-4	2.5	dBm	
Transmitter and dispersion penalty, each lane	TDP		3	dB	
OMA minus TDP, each lane	OMA-TDP	-5		dBm	
Average launch power, each lane	Pavg	-6.5	2.5	dBm	
Total launch power	Pavg-total		8.5	dBm	
Extinction ratio	ER	3.5		dB	
Side-mode suppression ratio	SMSR	30		dB	
Difference in launch power between any two lanes (OMA)			5	dB	
Average launch power of OFF transmitter, each lane	Toff		-30	dBm	
Optical return loss tolerance	ORL		20	dB	
Transmitter reflectance			-12	dB	
Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			
T_x DD reporting accuracy	TxDD Error	-2	2	dB	

OPTICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Typ	Max	Unit	Notes
Signaling rate, each lane		25.78125 ± 100 ppm		GBd	
The following specifications are applicable within the operating case temperature range					
Damage threshold		3.5		dBm	
Average receive power, each lane	P_{avg}	-11.5	2.5	dBm	
Receiver reflectance			-26	dB	
Receiver Sensitivity (OMA), each lane	Rx Sens		-10	dBm	5E-5 BER, pre-FEC, PRBS31, using typical FluxLight transmitter
Stressed receiver sensitivity (OMA), each lane	SRS		-7.3	dBm	Measured with conformance test signal at TP3 for BER = $5x10^{-5}$.
Stressed receiver sensitivity test conditions [Note: test conditions for measuring stress receiver sensitivity, not characteristic of the receiver]					
Vertical eye closure penalty, each lane	VECP	1.9		dB	
Stressed sys J2 jitter, each lane	J2	0.33		UI	
Stressed sys J4 jitter, each lane	J4	0.48		UI	
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}			
LOS assert	LOS_A		-15	dBm	
LOS hysteresis	LOS_Hys	0.5		dB	
R_X DD reporting accuracy	R_XDD Error	-2	2	dB	

PIN LAYOUT AND FUNCTION DEFINITIONS

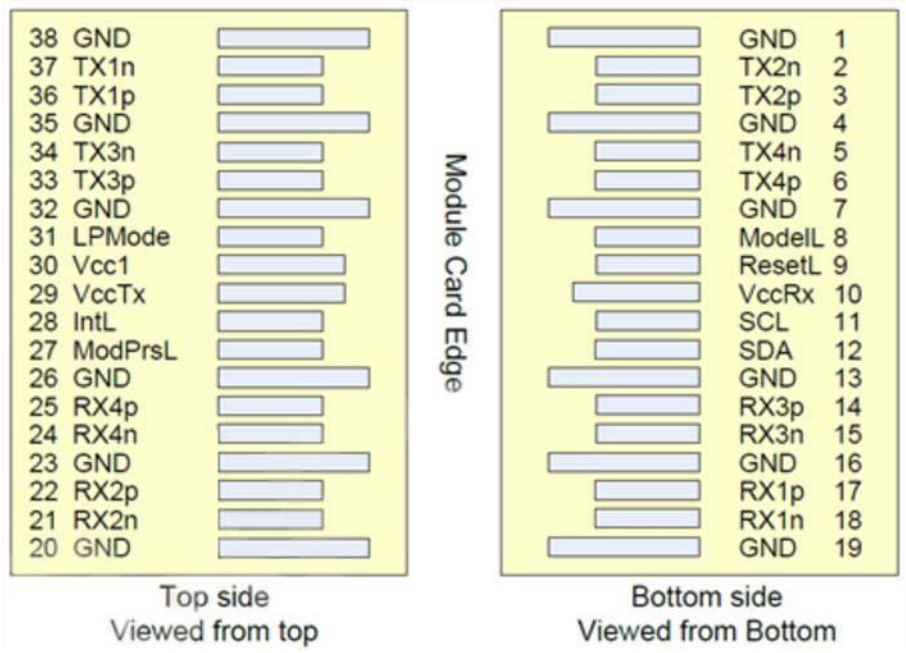

Figure 3: Transceiver pin-out.

PIN DEFINITIONS / DESCRIPTIONS

PIN Number	Type	Name	Description
1		GND	Module ground
2	CML-I	Tx2n	Transmitter inverted data input
3	CML-I	Tx2p	Transmitter non-inverted data input
4		GND	Module ground
5	CML-I	Tx4n	Transmitter inverted data input
6	CML-I	Tx4p	Transmitter non-inverted data input
7		GND	Module ground
8	LVTTL-I	ModSelL	Module select
9	LVTTL-I	ResetL	Module reset
10		Vcc Rx	+3.3V power supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13		GND	Module ground
14	CML-O	Rx3p	Receiver non-inverted data output
15	CML-O	Rx3n	Receiver inverted data output

16		GND	Module ground
17	CML-O	Rx1p	Receiver non-inverted data output
18	CML-O	Rx1n	Receiver inverted data output
19		GND	Module ground
20		GND	Module ground
21	CML-O	Rx2n	Receiver non-inverted data output
22	CML-O	Rx2p	Receiver inverted data output
23		GND	Module ground
24	CML-O	Rx4n	Receiver non-inverted data output
25	CML-O	Rx4p	Receiver inverted data output
26		GND	Module ground
27	LVTTL-O	ModPrsL	Module present
28	LVTTL-O	IntL	Interrupt
29		Vcc Tx	+3.3V power supply
30		Vcc1	+3.3V power supply
31	LVTTL-I	LPMode	Low power mode
32		GND	Module ground
33	CML-I	Tx3p	Transmitter non-inverted data input
34	CML-I	Tx3n	Transmitter inverted data input
35		GND	Module ground
36	CML-I	Tx1p	Transmitter non-inverted data input
37	CML-I	Tx1n	Transmitter inverted data input
38		GND	Module ground

QSFP28 CWDM LANE ASSIGNMENT

Lane	Center Wavelength	Wavelentgth Range	Module electrical lane per SFF8679
L1	1271 nm	1264.5 nm to 1277.5 nm	Tx1, Rx1
L2	1291 nm	1284.5 nm to 1297.5 nm	Tx2, Rx2
L3	1311 nm	1304.5 nm to 1317.5 nm	Tx3, Rx3
L4	1331 nm	1324.5 nm to 1337.5 nm	Tx4, Rx4

MECHANICAL DRAWING

FIBER

The module has duplex single mode LC receptacle connector.

ELECTRICAL

The electrical connector is the 38-pin row PCB edge connector.

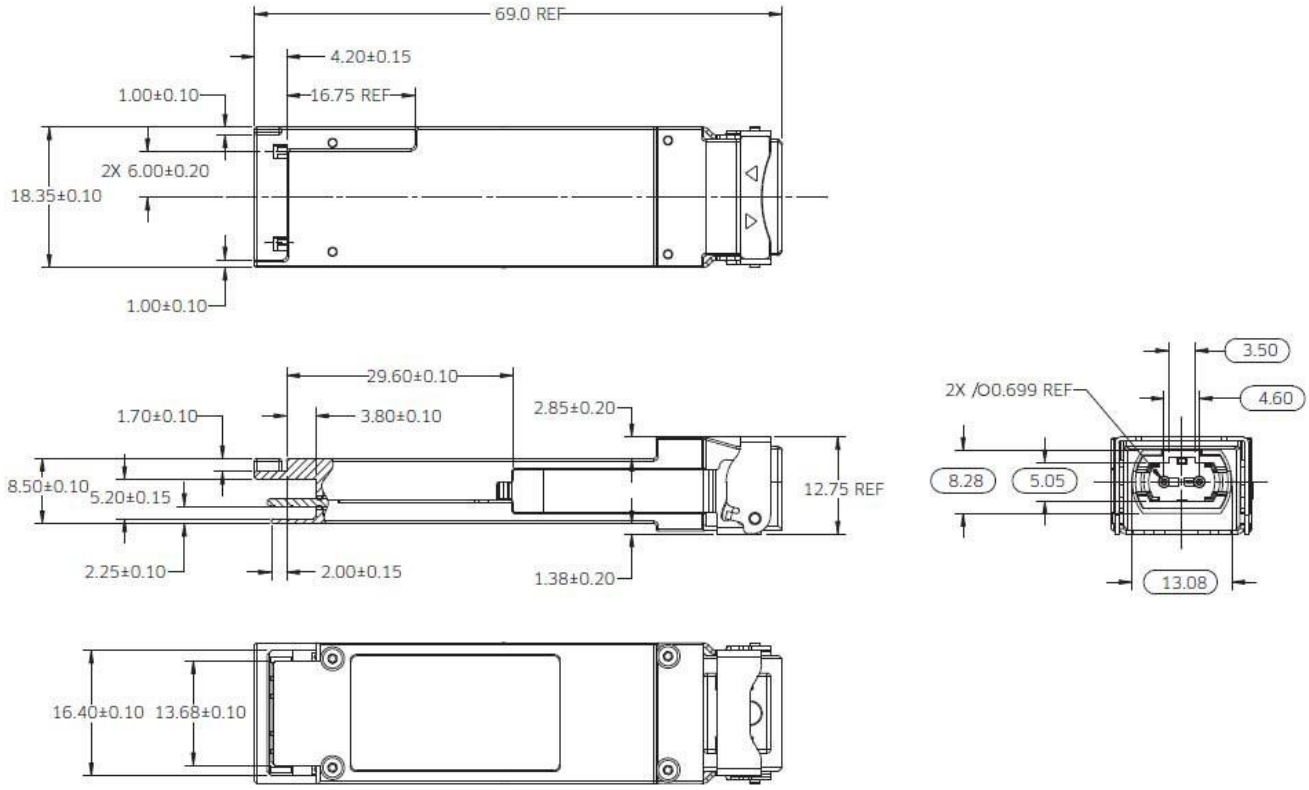

Figure 4: Mechanical drawing.

COMPLIANCE

- 100G CWDM4 MSA Technical Specification Rev 1.0
- • IEEE 802.3bm CAUI-4 chip to module electrical standard
- • SFF-8661 Rev 2.3 QSFP28 Module Mechanical
- • SFF-8679 Rev 1.7 QSFP28 Base Electrical
- • SFF-8636 Rev 2.6 Common Management Interface
- • Class 1 laser safety
- • Tested in accordance with Telcordia GR-468

Feature	Test Merhod	Performance
SAFETY		
Product safety	UL 60950-1	UL recognized component for US and CAN
	CSA C22.2 No. 60950-1	
	EN 60950-1	TUV certificate
	IEC 60950-1	CB certificate
	Flame class V-0	Passes Needle Flame Test for component flammability verification
	Low Voltage Directive 2006/95/EC	Certified to harmonized standards listed; Declaration of Conformity issued
Laser safety	EN 60825-1, EN 60825-2	TUV certificate
	IEC 60825-1	CB certificate
	U.S. 21 CFR 1040.10	FDA/CDRH certified with accession number
ELECTROMAGNETIC COMPATIBILITY		
Radiated emissions	EMC Directive 2004/108/EC	Class B digital device with a minimum -6dB margin to the limit. Final margin may vary depending on system implementation. Tested frequency range: 30 MHz to 40 GHz or 5th harmonic (5 times the highest frequency), whichever is less. Good system EMI design practice is required to achieve Class B margins at the system level.
	FCC rules 47 CFR Part 15	
	CISPR 22	
	AS/NZS	
	CISPR22	
	EN 55022	
	ICES-003, Issue 5	
	VCCI regulations	
Immunity	EMC Directive 2004/108/EC	Certified to harmonized standards listed; Declaration of Conformity issued
	CISPR 24	
	EN 55024	
ESD	IEC/EN 61000-4-2	Exceeds Requirements. Withstands discharges of ±8kV contact, ±15kV air
Radiated immunity	IEC/EN 61000-4-3	Exceeds Requirements. Field strength of 10V/m from 80 MHz to 6 GHz. No effect on transmitter / receiver performance is detectable between these limits.

RESTRICTION OF HAZARDOUS SUBSTANCES (ROHS)

RoHS 2011/65/EU	EU Directive	Compliant per the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast).