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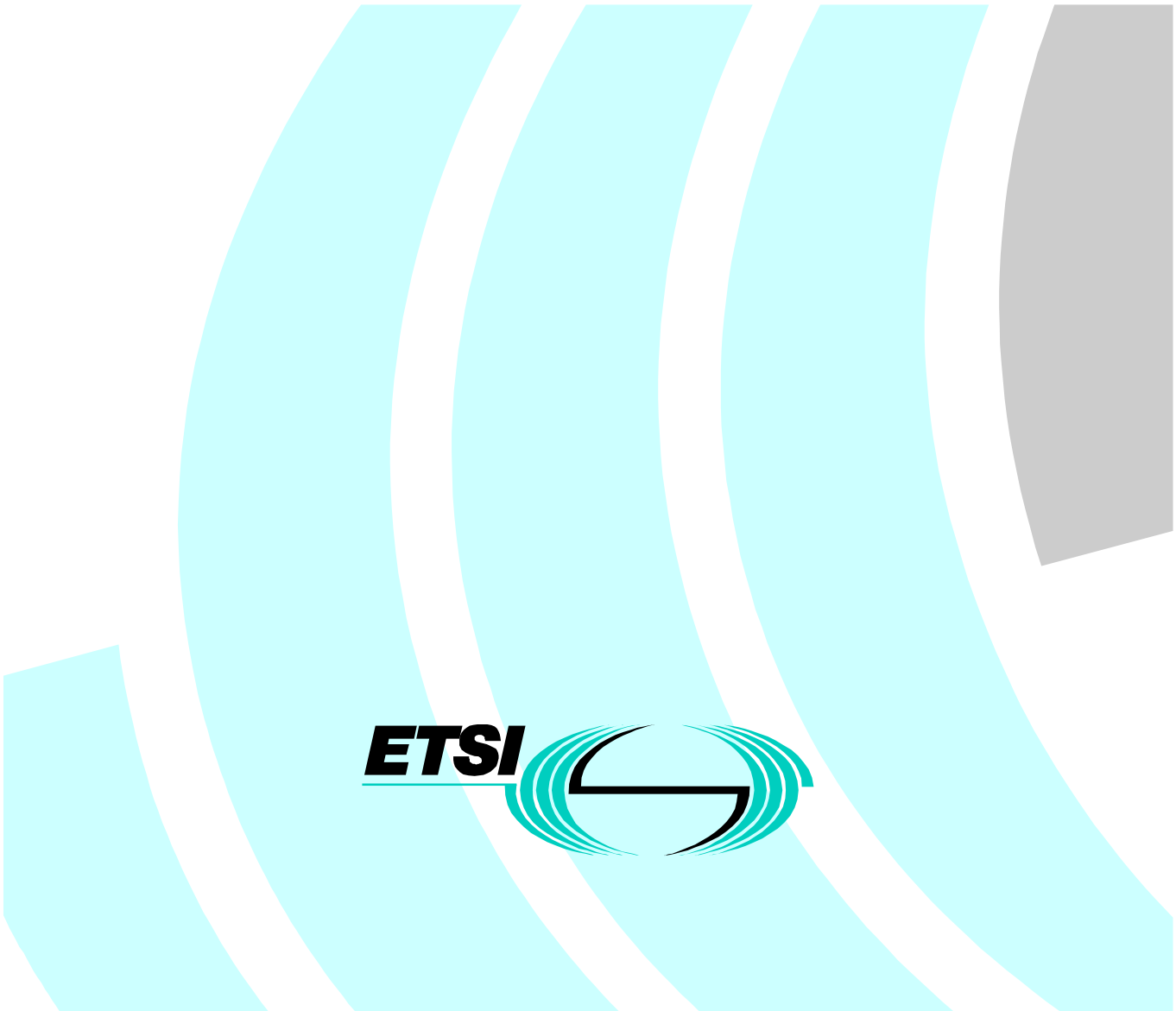
European Standard (Telecommunications series)

Transmission and Multiplexing (TM); The control of jitter and wander in transport networks



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Foreword

This European Standard (Telecommunications series) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM), and is now submitted for the Voting phase of the ETSI standards Two-step Approval Procedure.

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Date of latest announcement of this EN (doa):	3 months after ETSI publication
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Introduction

In a transport network, jitter and wander accumulate on data paths according to the jitter and wander generation and transfer characteristics of each equipment interconnected. These equipments may be different types of multiplexers/demultiplexers, cross-connects and line systems, for example.

An excessive amount of jitter and wander can adversely affect both digital signals (e.g. by generation of bit errors, uncontrolled slips and other abnormalities) and analogue signals (e.g. by unwanted phase modulation of the transmitted signal). The consequences of such impairment will, in general, depend on the particular service that is being carried and the terminating or adaptation equipment involved.

It is therefore necessary to set limits on the magnitude of jitter and wander at network interfaces, in order to guarantee a proper quality of the transmitted signals and a proper design of the equipment.

The jitter and wander control philosophy of the present document is based on the need:

- to specify a maximum network limit of jitter and wander that should not be exceeded at any relevant interface;
- to specify a minimum equipment tolerance to jitter and wander that should be provided at any relevant interface;
- to establish a consistent framework for the specification of individual digital equipment types; and
- to provide sufficient information and guidelines for organizations to measure and study jitter and wander characteristics in any network configuration.

1 Scope

The present document specifies the relevant parameters and their limiting values that are able to satisfactorily control the amount of jitter and wander present at synchronous digital hierarchy (SDH) and plesiochronous digital hierarchy (PDH) network-network interfaces (NNI).

The present document also provides the minimum jitter and wander requirements at SDH and PDH user-network interfaces (UNI). However, particular terminals or services may have additional jitter and wander requirements and in those cases the relevant standards apply.

The jitter and wander requirements specified in the present document are applicable to the interfaces irrespective of the transport mechanism (PDH, SDH or ATM networks, for example).

The jitter and wander requirements for an interface will be different, depending on whether the signal at the interface is used to transport data only, or synchronization as well. The requirements for synchronization interfaces are specified in EN 300 462-3-1 [7] and reference is made to that document where appropriate.

The present document also specifies the jitter and wander requirements for interfaces using the generic frame structures at PDH rates as described in ETS 300 337 [3].

The electrical characteristics of the relevant network interfaces for SDH and PDH interfaces are described in specification ETS 300 166 [1] and the characteristics of SDH optical interfaces are described in specification ETS 300 232 [2].

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, subsequent revisions do apply.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1] ETS 300 166: "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2 048 kbit/s-based Plesiochronous or Synchronous Digital Hierarchies".

[2] ETS 300 232: "Transmission and Multiplexing (TM); Optical interfaces for equipments and systems relating to the Synchronous Digital Hierarchy [ITU-T Recommendation G.957 (1993), modified]".

[3] ETS 300 337: "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s".

[4] EN 300 417-1-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 1-1: Generic processes and performance".

[5] EN 300 462-1-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1-1: Definitions and terminology for synchronization networks".

[6] EN 300 462-2-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2-1: Synchronization network architecture".

[7] EN 300 462-3-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks".

[8] EN 300 462-4-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4-1: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

[9] EN 300 462-5-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[10] EN 300 462-6-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6-1: Timing characteristics of primary reference clocks".

[11] ITU-T Recommendation G.803: "Architecture of transport networks based on the synchronous digital hierarchy (SDH)".

[12] ITU-T Recommendation O.150: "General requirements for instrumentation for performance measurements on digital transmission equipment".

[13] ITU-T Recommendation O.171: "Timing jitter and wander measuring equipment for digital systems which are based on the plesiochronous digital hierarchy (PDH)".

[14] ITU-T Recommendation O.172: "Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)".

[15] ITU-T Recommendation G.703: "Physical/electrical characteristics of hierarchical digital interfaces".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply. Additional definitions relating to synchronization networks are provided in EN 300 462-1-1 [5], whilst the architectural principles of synchronization networks are described in EN 300 462-2-1 [6].

traffic interface: these interfaces may be synchronous (i.e. normally PRC-traceable) or asynchronous (e.g. meeting the frequency offset requirements of ETS 300 166 [1]). Network jitter and wander limits are specified in the present document and wander is specified using the MRTIE (Maximum Relative Time Interval Error) parameter. Input jitter and wander tolerance is also specified in the present document. This interface category can be further sub-divided as follows:

- interface is not able to provide synchronization, and is not required to. An example is an interface supporting only 34 368 kbit/s or 139 264 kbit/s PDH signals according to ETS 300 166 [1];
- interface is not able to provide synchronization at the defined performance level, but nevertheless is used to provide timing to other network elements such as terminal equipment, remote concentrators, etc. Examples include 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s PDH signals and leased lines transported on SDH, which may be subject to pointer justifications. ITU-T Recommendation G.803 [11] recommends that these interfaces are not used for synchronization, but in some network applications there is little alternative;
- interface is able to provide synchronization at the defined performance level, in which case it is defined to be a synchronization interface. An example is STM-N interfaces. This sub-category may also include interfaces using the generic frame structures at PDH rates as described in ETS 300 337 [3].

synchronization interface: these interfaces are synchronous (i.e. normally PRC-traceable) and their requirements are not specified in the present document. The network limits for synchronization interfaces are specified using MTIE (Maximum Time Interval Error) and TDEV (Time Deviation) parameters with values given in EN 300 462-3-1 [7]. The input jitter and wander tolerance of clock equipment ports is specified in EN 300 462-4-1 [8] (for equipment containing an SSU function) and EN 300 462-5-1 [9] (for equipment containing an SEC function).

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply. Additional abbreviations relating to synchronization networks are provided in EN 300 462-1-1 [5].

ATM	Asynchronous Transfer Mode
CMI	Coded Mark Inversion
MRTIE	Maximum Relative Time Interval Error
MS-AIS	Multiplex Section Alarm Indication Signal
MTIE	Maximum Time Interval Error
NE	Network Element
NNI	Network-Network Interface
PDH	Plesiochronous Digital Hierarchy
pk-pk	peak-to-peak
PLL	Phase Locked Loop
ppm	parts per million
PRBS	Pseudo-Random Binary Sequence
PRC	Primary Reference Clock
RTIE	Relative Time Interval Error
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SSU	Synchronization Supply Unit
STM-1e	Synchronous Transport Module, level 1 (electrical format CMI-encoded signal)
STM-N	Synchronous Transport Module, level N
TDEV	Time Deviation
TIE	Time Interval Error
UI	Unit Interval
UIpp	Unit Interval, peak-to-peak
UNI	User-Network Interface
VC-n	Virtual Container, level n

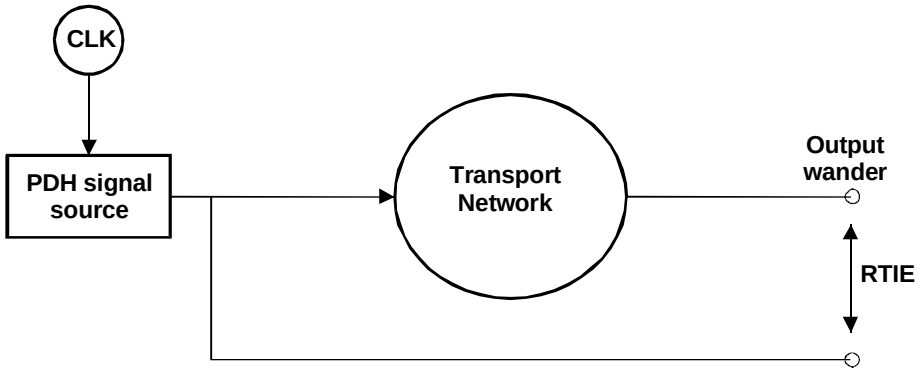
4 Network wander specification

4.1 Wander reference model

Wander is always specified and measured as a Relative Time Interval Error (RTIE) between the signal of interest and some reference clock. However, the reference clock against which the RTIE is specified or measured depends on the type of signal of interest. For the purposes of the present document, two cases can be distinguished.

1) Asynchronous PDH connection

The appropriate reference for specifying the output wander of asynchronous PDH signals is the signal source itself. For measurement purposes, since that source is not normally available for use as the reference clock, it can be substituted by a suitably-filtered version of the output signal. Annex B has further information regarding this. The reference model is illustrated in figure 1.

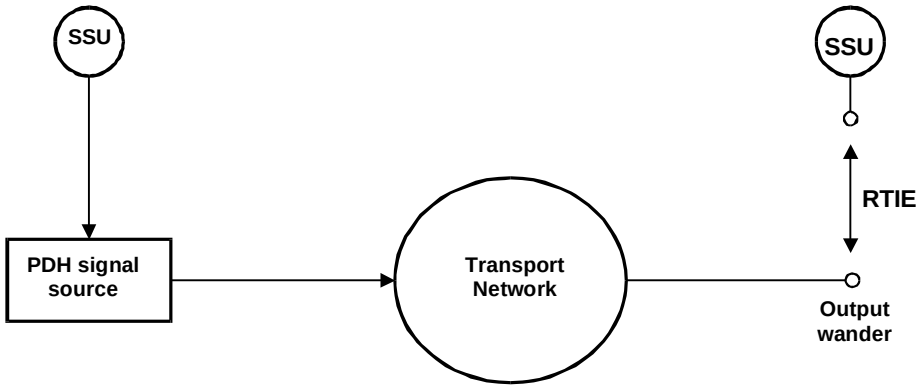


NOTE: CLK frequency offset conforms to bit-rate specifications of ITU-T Recommendation G.703 [15].

Figure 1: Wander reference model for asynchronous PDH connection

2) Synchronous PDH connection

The appropriate reference for specifying the output wander of synchronous PDH signals (i.e. most 2 048 kbit/s signals as well as signals framed according to ETS 300 337 [3]) is the network clock reference used at the PDH signal termination. This means that the wander of two reference clock distribution networks is added to the output wander generated by the transport network. The reference model is illustrated in figure 2.



NOTE 1: SSU outputs conform to EN 300 462-3-1 [7] network wander limit.
NOTE 2: Both SSUs are traceable to a PRC (but not necessarily the same PRC).

Figure 2: Wander reference model for synchronous PDH connection

Although for cases 1 and 2, different wander sources contribute to the total output wander, the resulting measured RTIE will not be very different. This is due to a lack of correlating effects and because statistically-speaking the transport network wander is the dominant source compared with the synchronization network wander. Consequently the same network limits have been set for both cases in the following output wander specifications.

The wander specifications of the present document are consistent with the derivation of limits outlined for the case of SDH network transport in annex A.

4.2 Specification of wander by MRTIE parameter

There are several parameters in use for specifying wander in standard specifications, such as MTIE and TDEV. For the purposes of the present document, MRTIE (Maximum Relative Time Interval Error) has been selected because it is most suitable to allow derivation of consequent equipment performance specifications.

For asynchronous payloads (refer to figure 1) the MRTIE specifies the wander accumulated by the network relative to the input signal phase. This is reasonable because it provides information for designing the filter required for any filtering of the transported signal clock in order to achieve the required phase stability of the payload.

For synchronous payloads (refer to figure 2) the MRTIE specifies the wander of the payload output relative to the clock phase of an input buffer (e.g. located in an exchange). This is reasonable because it provides information for designing the buffer size.

Measurement methodologies used to measure the MRTIE parameter are described in annex B.

5 Network limits for output jitter and wander

5.1 Network limits for output jitter

The limits given in table 1 represent the maximum permissible levels of jitter at interfaces within a digital network. Jitter as measured over a 60 second interval shall not exceed the limits given in table 1, when using the specified measurement bandwidths. The limits shall be met for all operating conditions and regardless of the amount of equipment preceding the interface. In general, these network limits are compatible with the minimum tolerance to jitter that all equipment input ports are required to provide.

There is a close relationship between network limits and input tolerance such that in terms of specification, the frequency bandwidth used for measurement and the frequency breakpoints used for tolerance, are defined using the same frequencies. In other words, the jitter measurement filter cut-off frequencies used in table 1 have the same values as the jitter tolerance mask corner frequencies used in clause 6. Annex D provides further information about this relationship.

The functional description for measuring output jitter at a digital interface can be found in ITU-T Recommendation O.172 [14].

The high-pass measurement filters of table 1 have a single-order characteristic and a roll-off of 20 dB/decade. The low-pass measurement filters have a maximally-flat, Butterworth characteristic and a roll-off of 60 dB/decade. Further specifications for the frequency response of the jitter measurement function such as measurement filter accuracy and additional allowed filter poles are given in ITU-T Recommendation O.172 [14].

Instrumentation in accordance with ITU-T Recommendations O.172 [14] and O.171 [13] is appropriate for measurement of jitter in SDH and PDH systems, respectively.

ITU-T Recommendation O.172 [14] includes test set specifications for the measurement of SDH tributaries operating at PDH bit-rates, where the test set requirements are more stringent than those relating only to PDH systems. Therefore, instrumentation in accordance with ITU-T Recommendation O.172 [14] shall be used at PDH interfaces in SDH systems.

Table 1: Maximum permissible jitter at interfaces

Interface	Measurement bandwidth, -3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp)
64 kbit/s (note 1)	20 to 20 k	0,25
	3 k to 20 k	0,05
2 048 kbit/s	20 to 100 k	1,5
	18 k to 100 k (note 2)	0,2
8 448 kbit/s	20 to 400 k	1,5
	3 k to 400 k (note 2)	0,2
34 368 kbit/s	100 to 800 k	1,5
	10 k to 800 k	0,15
139 264 kbit/s	200 to 3,5 M	1,5
	10 k to 3,5 M	0,075
STM-1e (note 3)	500 to 1,3 M	1,5
	65 k to 1,3 M	0,075
STM-1	500 to 1,3 M	1,5
	65 k to 1,3 M	0,15
STM-4	1 k to 5 M	1,5
	250 k to 5 M	0,15
STM-16	5 k to 20 M	1,5
	1 M to 20 M	0,15
STM-64	20 k to 80 M	1,5
	4 M to 80 M	(note 4)

NOTE 1: For the co-directional interface only.
NOTE 2: For 2 048 kbit/s and 8 448 kbit/s interfaces within the network of an operator, the high-pass cut-off frequency may be specified to be 700 Hz (instead of 18 kHz) and 80 kHz (instead of 3 kHz) respectively. However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise.
NOTE 3: Electrical format CMI-encoded, according to ETS 300 166 [1].
NOTE 4: A value of 0,15 UIpp has been proposed. The effect of dispersion and non-linearities on the eye opening and on the choice of this value is for further study.
NOTE 5: UI Unit Interval:

64 kbit/s	1 UI = 15,6 µs
2 048 kbit/s	1 UI = 488 ns
8 448 kbit/s	1 UI = 118 ns
34 368 kbit/s	1 UI = 29,1 ns
139 264 kbit/s	1 UI = 7,18 ns
STM-1	1 UI = 6,43 ns
STM-4	1 UI = 1,61 ns
STM-16	1 UI = 0,402 ns
STM-64	1 UI = 0,100 ns

5.2 Network limits for output wander

The MRTIE specifications given in this clause are intended for application to both synchronous (i.e. normally PRC-traceable) and asynchronous (e.g. liable to a frequency offset) PDH interfaces of ETS 300 166 [1], refer to figure 1 and figure 2, respectively, for the reference network configurations.

It is required that, within a synchronized network, digital equipment provided at nodes shall accommodate permitted phase deviations on the incoming signal, i.e. under normal synchronized conditions, impairments will not occur.

However, it should be recognized that, as a result of some performance degradations, failure conditions, maintenance actions and other events, the RTIE between the incoming signal and the internal timing signal of the terminating equipment may exceed the jitter and wander tolerance of the equipment which may result in an abnormal event such as a controlled slip or bit-error burst.

In addition, at a node which connects to an independently-synchronized network (or where plesiochronous operation is used in national networks), the RTIE between the incoming signal and the internal timing signal of the terminating equipment may eventually exceed the jitter and wander tolerance of the equipment in which case an abnormal event such as a controlled slip may occur. The maximum permissible long-term mean controlled slip rate resulting from this mechanism is derived from the clock performance defined in EN 300 462-6-1 [10], i.e. no more than one slip in 70 days.

The wander measurement requirements (e.g. sampling time and measurement interval) for MTIE, MRTIE and TDEV parameters, the 10 Hz wander measurement filter characteristic and the functional description for measuring output wander are described in ITU-T Recommendation O.172 [14].

Instrumentation in accordance with ITU-T Recommendation O.172 [14] is appropriate for measurement of wander parameters at both SDH and PDH interfaces.

Measurement methodologies used to measure the MRTIE parameter are described in annex B.

5.2.1 2 048 kbit/s interface output wander limit

The maximum level of wander that may exist at a 2 048 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in table 2. The resultant overall specification is illustrated in figure 3.

Table 2: 2 048 kbit/s interface output wander limit

Observation Interval τ (sec)	MRTIE requirement
$0,05 < \tau \leq 0,2$	46τ µs
$0,2 < \tau \leq 32$	9 µs
$32 < \tau \leq 64$	$0,28\tau$ µs
$64 < \tau \leq 1\,000$ (note)	18 µs
NOTE: For the asynchronous configuration (refer to figure 1), the maximum observation interval to be considered is 80 seconds.	

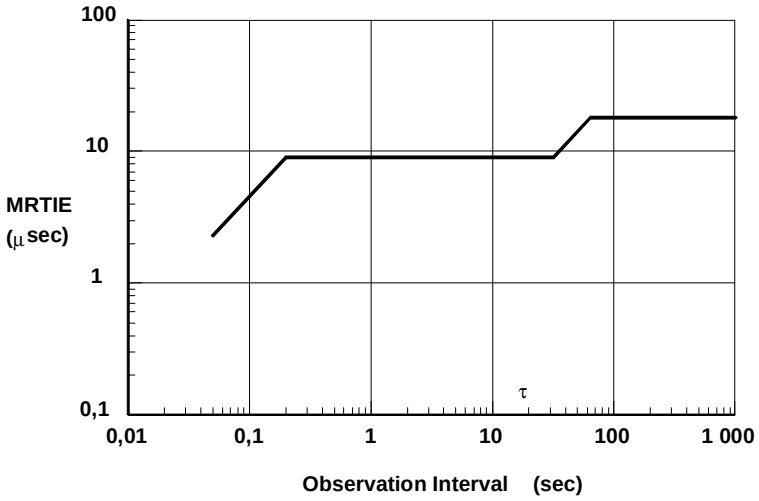


Figure 3: 2 048 kbit/s interface output wander limit

5.2.2 34 368 kbit/s interface output wander limit

The maximum level of wander that may exist at a 34 368 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in table 3. The resultant overall specification is illustrated in figure 4. 34 368 kbit/s signals can be framed in accordance with ETS 300 337 [3]; in the case when these are used as a synchronization interface, the output wander limit is for further study.

Table 3: 34 368 kbit/s interface output wander limit

Observation Interval τ (sec)	MRTIE requirement
0,05 < τ ≤ 0,073	14τ µs
0,073 < τ ≤ 2,5	1 µs
2,5 < τ ≤ 10	0,4τ µs
10 < τ ≤ 80	4 µs

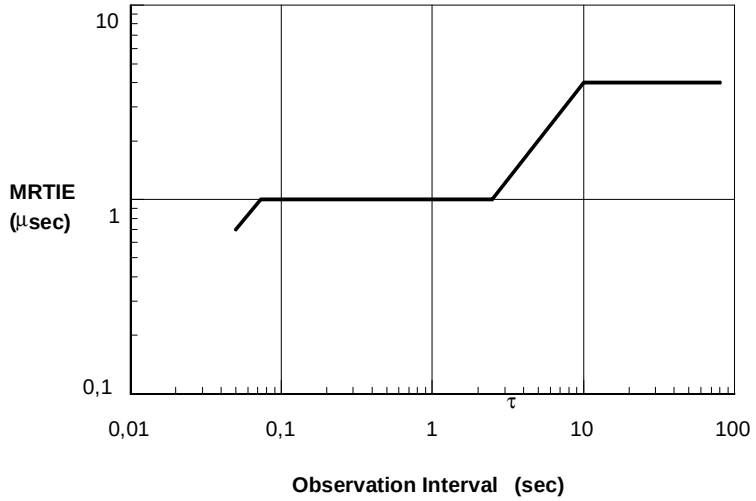


Figure 4: 34 368 kbit/s interface output wander limit

5.2.3 139 264 kbit/s interface output wander limit

The maximum level of wander that may exist at a 139 264 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in table 4. The resultant overall specification is illustrated in figure 5. 139 264 kbit/s signals can be framed in accordance with ETS 300 337 [3]; in the case when these are used as a synchronization interface, the output wander limit is for further study.

Table 4: 139 264 kbit/s interface output wander limit

Observation Interval τ (sec)	MRTIE requirement
0,05 < τ ≤ 0,15	6,8τ µs
0,15 < τ ≤ 2,5	1 µs
2,5 < τ ≤ 10	0,4τ µs
10 < τ ≤ 80	4 µs

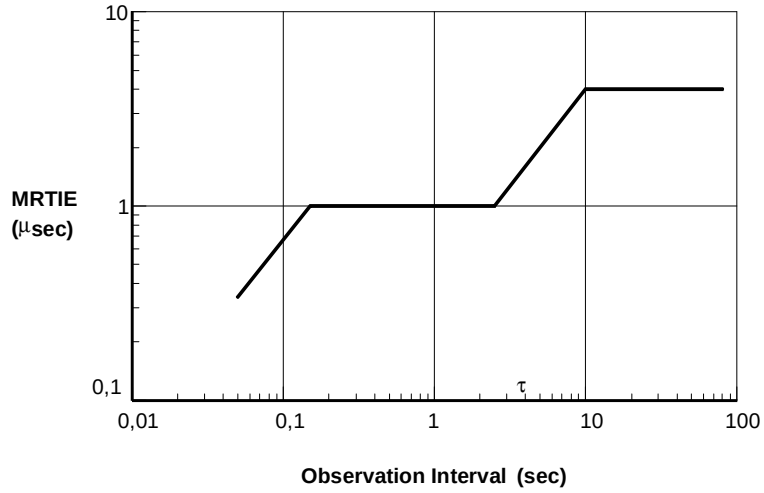


Figure 5: 139 264 kbit/s interface output wander limit

5.2.4 STM-N interface output wander limit

STM-N interfaces are defined as synchronization interfaces, and the network limits for wander at synchronization interfaces are specified in EN 300 462-3-1 [7].

6 Jitter and wander tolerance of equipment interfaces

In order to ensure that, in general, any equipment can be connected to any appropriate interface within a network, it is necessary to arrange that the input ports of all equipment are capable of accommodating levels of jitter and wander up to at least the minimum limits defined in the following clauses.

The jitter and wander tolerance of an SDH or PDH interface indicates the minimum level of phase noise that the input port shall accommodate whilst:

- not causing any alarms;
- not causing any slips; and
- not causing any bit errors; except for optical STM-N interfaces at jitter frequencies above f_P, (refer to table 12, table 13 and table 14) where an equivalent 1 dB optical power penalty shall not be exceeded.

All digital input ports of equipment shall be able to tolerate a digital signal that has:

- electrical characteristics in accordance with the requirements of ETS 300 166 [1] or the optical characteristics of ETS 300 232 [2];
- a constant frequency offset (relative to the nominal value) in the range defined in table 5;
- a rate of change in frequency up to at least 0,5 ppm/minute for all STM-N interfaces; and
- a sinusoidal phase deviation having an amplitude-frequency relationship defined in the following clauses which indicates the appropriate limits for the different interfaces.

In principle, these requirements shall be met regardless of the information content of the digital signal. However, for test purposes, the content of the signal with jitter and wander modulation should be a structured test sequence as defined in the following clauses.

When specifying or assessing interface tolerance, two equipment operating conditions can be distinguished:

- non-synchronized operation, where the receiving equipment is not being timed from a source that is synchronous with the interface under consideration. In this case, it is the equipment capability to accommodate phase variation on the incoming signal (in terms of clock recovery circuitry and synchronizer/desynchronizer buffers) that is of interest;

- synchronized operation, where the receiving equipment is being timed from a source that is synchronous with the interface under consideration. In this case, slip buffer dimension and operation is also of interest.

Unless otherwise stated, the tolerance specifications in the following clauses apply to both asynchronous and synchronous operating conditions.

The jitter and wander limit above 10 Hz reflects the maximum permissible jitter magnitude in a digital network. However the limit below 10 Hz does not aim to represent the maximum permissible wander that might occur in practice. Below 10 Hz the limits are derived such that where necessary, the provision of this level of buffer storage at the input of an equipment facilitates the accommodation of wander generated in a large proportion of real connections.

For convenience of testing, the required tolerance is defined in terms of the peak-to-peak amplitude and frequency of sinusoidal jitter which modulates a digital test pattern. It is important to recognize that this test condition is not, in itself, intended to be representative of the type of jitter found in practice in a network.

Guidance on the measurement set-up for input jitter and wander tolerance is provided in annex C.

Instrumentation in accordance with ITU-T Recommendations O.172 [14] and O.171 [13] is appropriate for generation of jitter and wander in SDH and PDH systems, respectively.

Table 5: Maximum frequency offset at interfaces

Interface	Maximum frequency offset (± ppm)	Example Application
64 kbit/s	0	Switch input channel
2 048 kbit/s	0	Switch, 1/0 cross-connect
2 048 kbit/s	4,6	Byte-synchronous mapping into SDH
2 048 kbit/s	50	PDH, asynchronous mapping into SDH
8 448 kbit/s	30	PDH
34 368 kbit/s	20	PDH, asynchronous mapping into SDH
34 368 kbit/s	4,6	Signal defined in ETS 300 337 [3]
139 264 kbit/s	15	PDH, asynchronous mapping into SDH
139 264 kbit/s	4,6	Signal defined in ETS 300 337 [3]
STM-N	4,6	SDH
STM-N	20	MS-AIS in SDH regenerator sections
NOTE: Frequency offset values are aligned with ETS 300 166 [1], EN 300 462-5-1 [9] and EN 300 417-1-1 [4].		

6.1 64 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 64 kbit/s co-directional network interface, expressed in peak-to-peak sinusoidal phase deviation, shall exceed the limit given in table 6. The resultant overall specification is illustrated in figure 6. The test sequence to be used is a PRBS of length 2^{11} - 1, defined in ITU-T Recommendation O.150 [12].

Table 6: 64 kbit/s input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
12 μ < f ≤ 4,3	18 μs	1,2 UI
4,3 < f ≤ 20	77 f^{-1} μs	5 f^{-1} UI
20 < f ≤ 600	3,9 μs	0,25 UI
600 < f ≤ 3 k	2,3 x 10^3 f^{-1} μs	150 f^{-1} UI
3 k < f ≤ 20 k	0,78 μs	0,05 UI

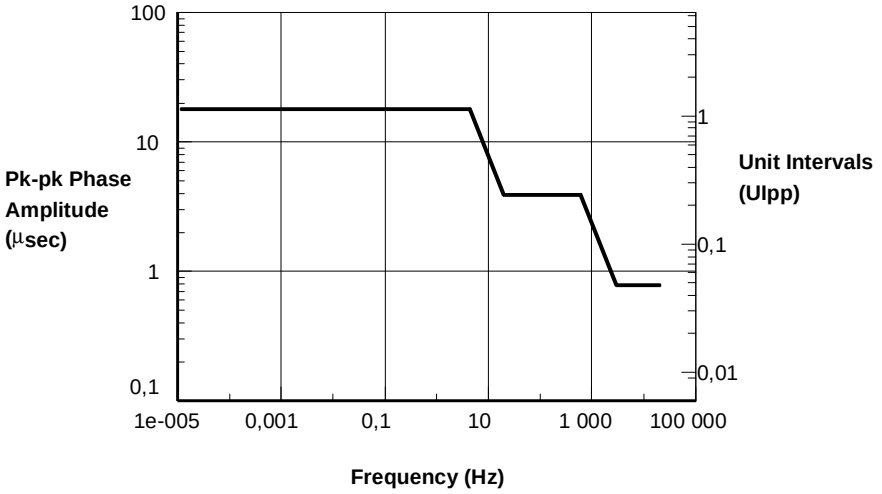


Figure 6: 64 kbit/s input jitter and wander tolerance limit

6.2 2 048 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 2 048 kbit/s network interface, expressed in peak-to-peak sinusoidal phase deviation, shall exceed the limits given in table 7. The resultant overall specification is illustrated in figure 7. The test sequence to be used is a PRBS of length 2^{15} - 1, defined in ITU-T Recommendation O.150 [12].

Table 7: 2 048 kbit/s input jitter and wander tolerance limits

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
12 μ < f ≤ 4,88 m	18 μs	37 UI
4,88 m < f ≤ 10 m	0,088 f^{-1} μs	0,18 f^{-1} UI
10 m < f ≤ 1,67	8,8 μs	18 UI
1,67 < f ≤ 20	15 f^{-1} μs	30 f^{-1} UI
20 < f ≤ 2,4 k (note)	0,73 μs	1,5 UI
2,4 k < f ≤ 18 k (note)	1,8 x 10^3 μs	3,6 x 10^3 f^{-1} UI
18 k < f ≤ 100 k (note)	0,098 μs	0,2 UI
NOTE: For 2 048 kbit/s interfaces within the network of an operator, the frequencies may be specified as 93 Hz (instead of 2,4 kHz) and 700 Hz (instead of 18 kHz). However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise.		

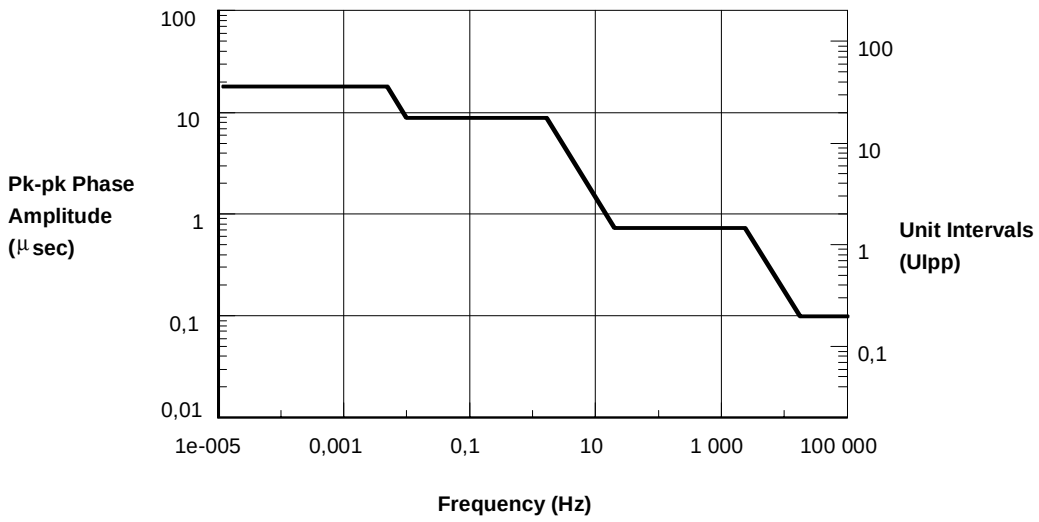


Figure 7: 2 048 kbit/s input jitter and wander tolerance limits

6.3 8 448 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 8 448 kbit/s network interface, expressed in peak-to-peak sinusoidal phase deviation, shall exceed the limit given in table 8. The resultant overall specification is illustrated in figure 8. The test sequence to be used is a PRBS of length 2^{15} - 1, defined in ITU-T Recommendation O.150 [12].

Table 8: 8 448 kbit/s input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
20 < f ≤ 400 (note)	0,18 µs	1,5 UI
400 < f ≤ 3 k (note)	72 f^{-1} µs	600 f^{-1} UI
3 k < f ≤ 400 k (note)	0,024 µs	0,2 UI
NOTE: For 8 448 kbit/s interfaces within the network of an operator, the frequencies may be specified as 10,7 kHz (instead of 400 Hz) and 80 kHz (instead of 3 kHz). However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise.		

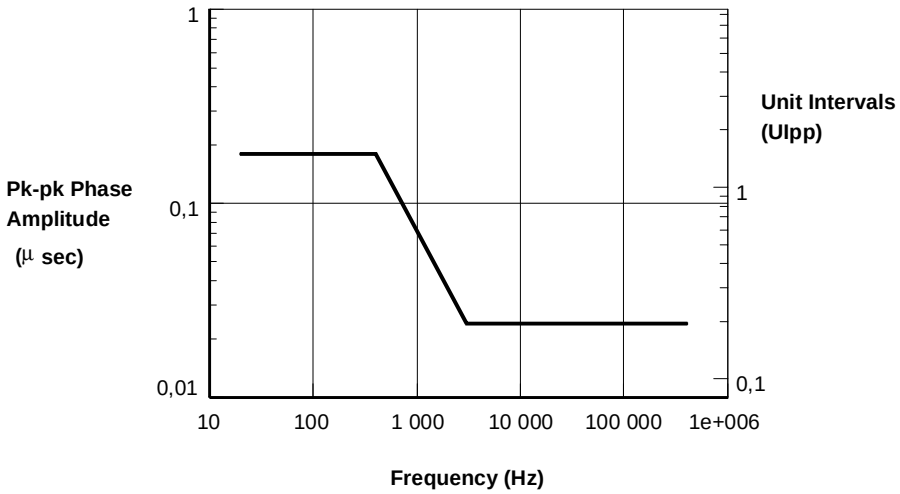


Figure 8: 8 448 kbit/s input jitter and wander tolerance limit

6.4 34 368 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 34 368 kbit/s network interface, expressed in peak-to-peak sinusoidal phase deviation, shall exceed the limit given in table 9. The resultant overall specification is illustrated in figure 9. The test sequence to be used is a PRBS of length 2^{23} - 1, defined in ITU-T Recommendation O.150 [12]; for signals in accordance with ETS 300 337 [3], the test sequence to be used is for further study.

Table 9: 34 368 kbit/s input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
10 m < f ≤ 32 m	4 µs	140 UI
32 m < f ≤ 130 m	0,13 f^{-1} µs	4,5 f^{-1} UI
130 m < f ≤ 4,4	1 µs	34 UI
4,4 < f ≤ 100	4,4 f^{-1} µs	150 f^{-1} UI
100 < f ≤ 1 k	44 ns	1,5 UI
1 k < f ≤ 10 k	4,4 x 10^{4} f^{-1} ns	1,5 x 10^{3} f^{-1} UI
10 k < f ≤ 800 k	4,4 ns	0,15 UI

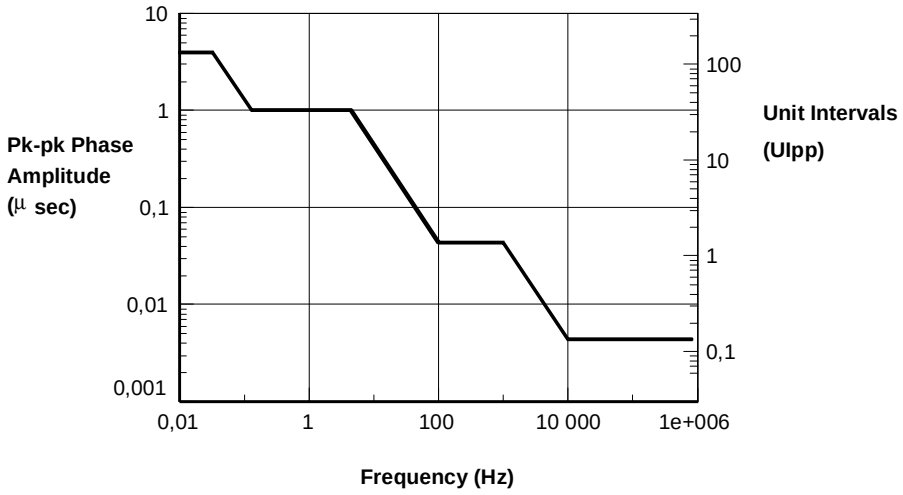


Figure 9: 34 368 kbit/s input jitter and wander tolerance limit

6.5 139 264 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 139 264 kbit/s network interface, expressed in peak-to-peak sinusoidal phase deviation, shall exceed the limit given in table 10. The resultant overall specification is illustrated in figure 10. The test sequence to be used is a PRBS of length 2^{23} - 1, defined in ITU-T Recommendation O.150 [12]; for signals in accordance with ETS 300 337 [3], the test sequence to be used is for further study.

Table 10: 139 264 kbit/s input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
10 m < f ≤ 32 m	4 µs	560 UI
32 m < f ≤ 130 m	0,13 f^{-1} µs	18 f^{-1} UI
130 m < f ≤ 2,2	1 µs	140 UI
2,2 < f ≤ 200	2,2 f^{-1} µs	300 f^{-1} UI
200 < f ≤ 500	11 ns	1,5 UI
500 < f ≤ 10 k	5,5 x 10^{3} f^{-1} ns	750 f^{-1} UI
10 k < f ≤ 3,5 m	0,54 ns	0,075 UI

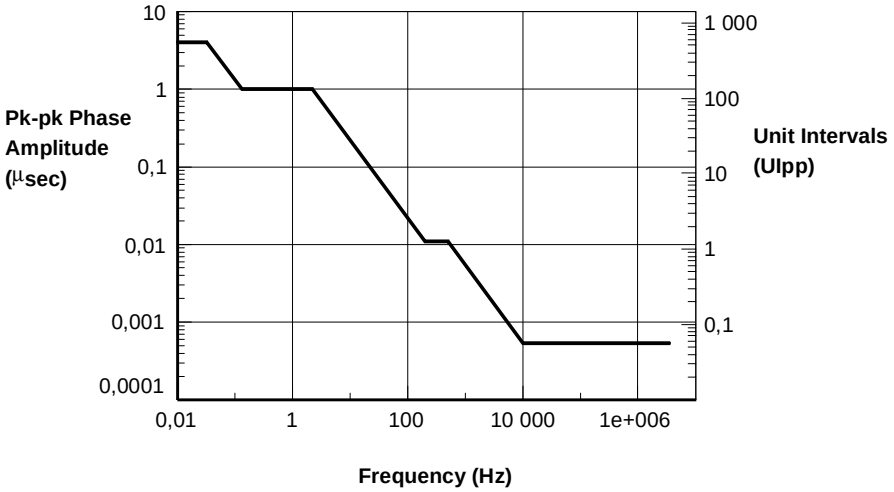


Figure 10: 139 264 kbit/s input jitter and wander tolerance limit

6.6 STM-N input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a STM-N network interface, expressed in peak-to-peak sinusoidal phase deviation, shall exceed the limits given in tables 11, 12, 13, 14 and 15 for STM-1e, STM-1, STM-4, STM-16 and STM-64, respectively. The resultant overall specification is illustrated in figure 11, figure 12, figure 13 and figure 14 for STM-1e/-1, STM-4, STM-16 and STM-64, respectively. Guidance on the test sequences suitable for SDH systems is provided in ITU-T Recommendation O.172 [14].

Table 11: STM-1e input jitter and wander tolerance limits

Frequency f (Hz)	Requirement, STM-1e interface (pk-pk phase amplitude)	
10 m < f ≤ 130 m	0,033 f^{-1} µs	5,1 f^{-1} UI
130 m < f ≤ 19,3	0,25 µs	39 UI
19,3 < f ≤ 500	4,8 f^{-1} µs	750 f^{-1} UI
500 < f ≤ 3,3 k	9,7 ns	1,5 UI
3,3 k < f ≤ 65 k	3,2 x 10^{4} f^{-1} ns	4,9 x 10^{3} f^{-1} UI
65 k < f ≤ 1,3 M	0,48 ns	0,075 UI
NOTE: STM-1e interface is electrical format CMI-encoded, according to ETS 300 166 [1].		

Table 12: STM-1 input jitter and wander tolerance limits

Frequency f (Hz)	Requirement, STM-1 interface (pk-pk phase amplitude)	
10 m < f ≤ 130 m	0,033 f^{-1} µs	5,1 f^{-1} UI
130 m < f ≤ 19,3	0,25 µs	39 UI
19,3 < f ≤ 500	4,8 f^{-1} µs	750 f^{-1} UI
500 < f ≤ 6,5 k (note)	9,7 ns	1,5 UI
6,5 k < f ≤ 65 k	6,3 x 10^4 f^{-1} ns	9,8 x 10^3 f^{-1} UI
65 k < f ≤ 1,3 M	0,97 ns	0,15 UI
NOTE: f_P (refer to clause 6) is 6,5 kHz for STM-1 interface.		

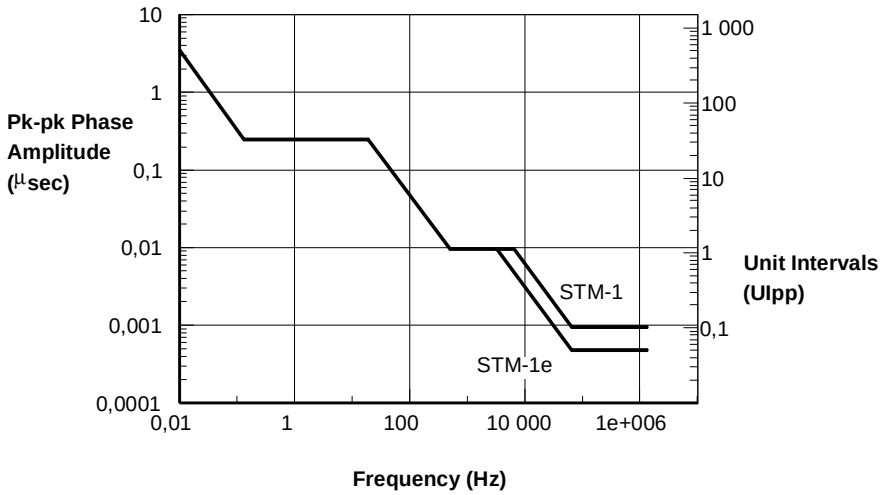


Figure 11: STM-1e and STM-1 input jitter and wander tolerance limits

Table 13: STM-4 input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
10 m < f ≤ 130 m	0,033 f^{-1} µs	21 f^{-1} UI
130 m < f ≤ 9,65	0,25 µs	160 UI
9,65 < f ≤ 1 k	2,4 f^{-1} µs	1,5 x 10^3 f^{-1} UI
1 k < f ≤ 25 k (note)	2,4 ns	1,5 UI
25 k < f ≤ 250 k	6 x 10^4 f^{-1} ns	3,8 x 10^4 f^{-1} UI
250 k < f ≤ 5 M	0,24 ns	0,15 UI
NOTE: f_P (refer to clause 6) is 25 kHz for STM-4 interface.		

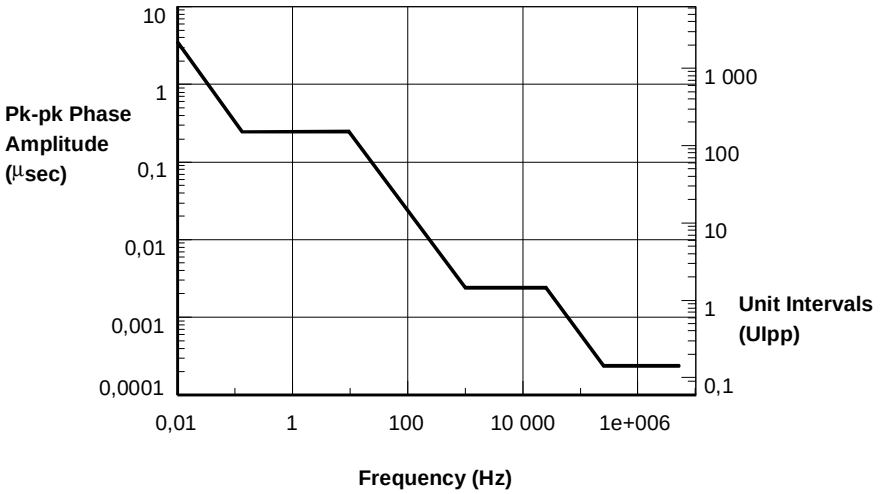


Figure 12: STM-4 input jitter and wander tolerance limit

Table 14: STM-16 input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
10 m < f ≤ 130 m	0,033 f^{-1} µs	82 f^{-1} UI
130 m < f ≤ 12,1	0,25 µs	620 UI
12,1 < f ≤ 5 k	3 f^{-1} µs	7,5 x 10^{3} f^{-1} UI
5 k < f ≤ 100 k (note)	0,6 ns	1,5 UI
100 k < f ≤ 1 M	6 x 10^{4} f^{-1} ns	1,5 x 10^{5} f^{-1} UI
1 M < f ≤ 20 M	0,06 ns	0,15 UI
NOTE: f_P (refer to clause 6) is 100 kHz for STM-16 interface.		

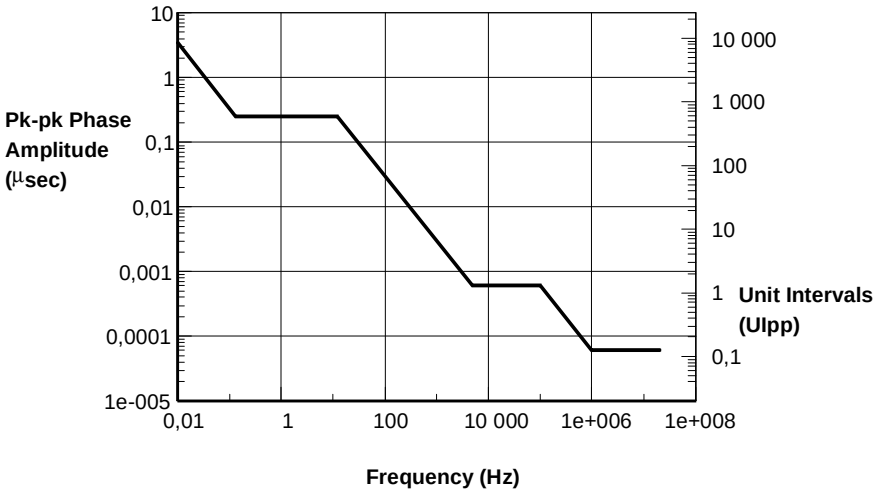


Figure 13: STM-16 input jitter and wander tolerance limit

Table 15: STM-64 input jitter and wander tolerance limit

Frequency f (Hz)	Requirement (pk-pk phase amplitude)	
10 m < f ≤ 130 m	0,033 f^{-1} µs	330 f^{-1} UI
130 m < f ≤ 12,1	0,25 µs	2,5 x 10^{3} UI
12,1 < f ≤ 20 k	3 f^{-1} µs	3 x 10^{4} f^{-1} UI
20 k < f ≤ 400 k (note 1, 2)	0,15 ns	1,5 UI
400 k < f ≤ 4 M	6 x 10^{4} f^{-1} ns	6 x 10^{5} f^{-1} UI
4 M < f ≤ 80 M	0,015 ns	0,15 UI (note 1)
NOTE 1: Values of 0,15 UI and 400 kHz are provisional and are for further study. NOTE 2: f_P (refer to clause 6) is 400 kHz (note 1) for STM-64 interface.		

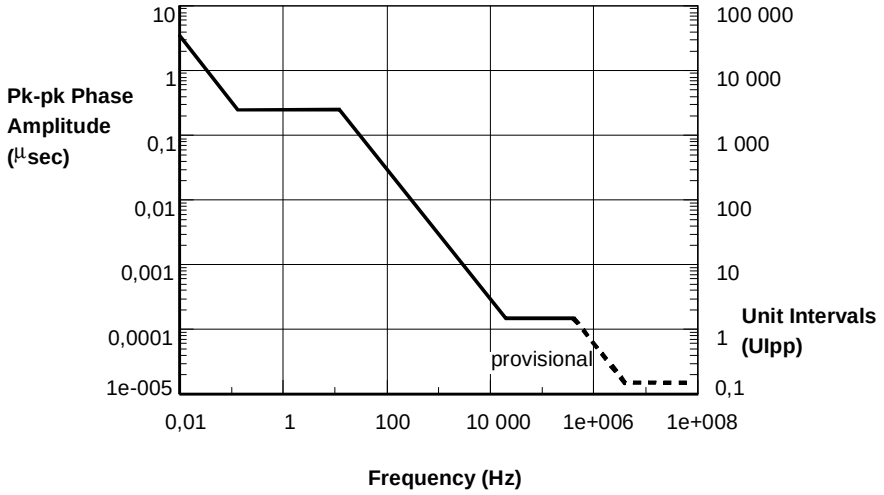


Figure 14: STM-64 input jitter and wander tolerance limit

Annex A (informative): Wander limit considerations for SDH transport networks

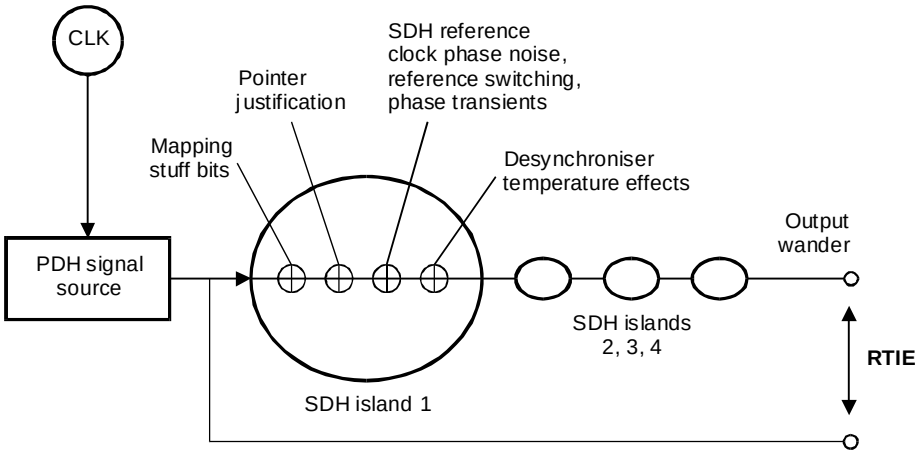
A.1 Introduction

The information in annex A is provided to assist an understanding of the derivation of the network wander limits and input wander tolerances that are specified in the present document.

A.1.1 Wander reference model for SDH

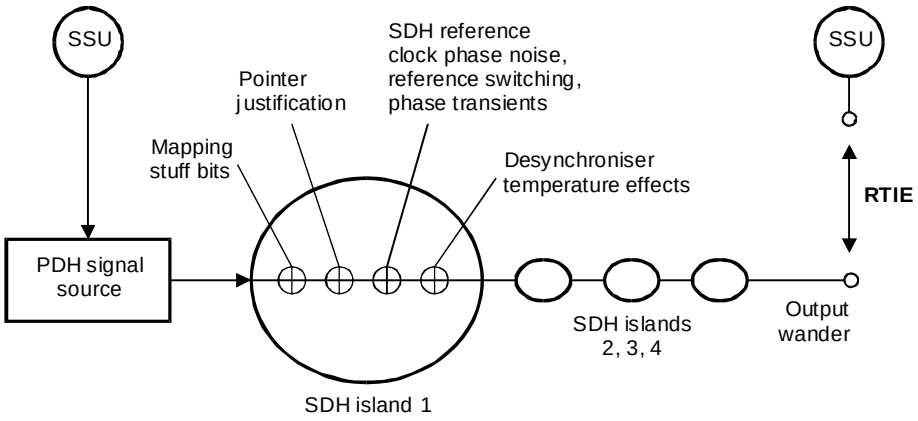
The wander reference models as shown in figure A.1 and figure A.2 are simplified representations of the wander reference model described in annex B of EN 300 462-3-1 [7]. They also illustrate how the generic reference models of figure 1 and figure 2 can accommodate network-specific sources of wander using the example of an SDH transport network.

Four cascaded SDH islands have been considered to be a reasonable modelling approach in previous jitter and wander accumulation computer simulation calculations. This approach is adopted in annex A. Figure A.1 and figure A.2 illustrate the principal sources of wander on network connections that have been considered when deriving the network limits and interface tolerances.



NOTE: CLK frequency offset conforms to bit-rate specifications of ITU-T Recommendation G.703 [15].

Figure A.1: Wander reference model for asynchronous PDH signals



NOTE 1: SSU outputs conform to EN 300 462-3-1 [7] network wander limit.
NOTE 2: Both SSUs are traceable to a PRC (but not necessarily the same PRC).

Figure A.2: Wander reference model for synchronous PDH signals

A.1.2 Sources of wander

The wander accumulated on payload signals when they are transported over a network connection employing SDH network elements depends on the total dynamic fill of all intermediate signal processing buffers in those network elements. The buffer fill of a single Network Element (NE) depends on the relative wander between the incoming data and the read clock. The read clock may be provided from an external source (e.g. in a pointer processor) or may be provided from a recovered clock (e.g. in a desynchronizer).

The buffer fill may be changed by reference clock phase noise and transient effects (e.g. bit-stuffing, pointer processing) and by temperature effects in phase-locked loops (e.g. desynchronizer clock recovery).

A.1.3 Wander accumulation limiting effects

At least when considering 2 048 kbit/s connections, the total amount of these buffers in a single connection may exceed the 18 µs limit requested as a limit for the daily wander in the present document. But under normal operating conditions, these buffer fills remain almost constant due to a stable network synchronization performance. Furthermore the fluctuating part of the buffer fills contributes only randomly to the accumulation because of a lack of correlating effects between different buffers.

A.1.4 Network configuration and performance

The SDH islands (refer to figure A.1 and figure A.2) are normally internally-synchronized so that pointer justifications (at least at TU-12 level) are rare events. An exceptional case is when one or more of the NEs is operated using a clock source that is in holdover mode, so generating an approximately regular sequence of pointer justifications.

Under normal conditions, it is unlikely that two or more of these SDH islands are not internally-synchronized. It is also unlikely that a double pointer justification is generated in a single NE. Therefore it is improbable that the cumulative wander effect of more than two simultaneous pointer justifications will occur. Such rare cases may cause wander that will exceed the network limits specified in the present document.

In general, the performance of the SDH islands should be good enough that the error and slip performance of the transported signal are not more than marginally affected by excessive phase noise effects that would cause buffer overflow in some NE.

A.1.5 Correlation of wander sources

The normal operating mode of the SDH network is the synchronous mode, which means that the rate of pointer justification is low and therefore the occurrence of simultaneous, but independent, pointer justifications in cascaded SDH islands is unlikely. The following accumulation model accounts for this by using a statistical accumulation approach (i.e. a power-law accumulation).

In the case of wander generated by a single SDH island, a worst-case accumulation is assumed which simply totals all wander generating effects within that island.

Correlation of bit-stuffing wander effects depends on the frequency offset of the PDH payload against that of the network clocks of the islands. This is an issue for synchronous 2 048 kbit/s connections, as follows:

- for frequency offsets below approximative 10^{-10} to 10^{-9} the network clock phase noise will randomize the bit-stuffing;
- for higher frequency offsets of the payload signal and with all SDH islands synchronized to nominal frequency, the bit-stuffing effects are correlated.

This is further considered in annex B of EN 300 462-3-1 [7].

A.1.6 Network conditions for the output wander limits

The network conditions for the output wander limits specified in the present document are described in annex B of EN 300 462-3-1 [7]. It is intended that such networks will meet the specified limits when using any equipment conforming to EN 300 417-1-1 [4] specifications.

For more complex network connection configurations, the application of some method of wander reduction may be necessary in order to obtain the desired level of performance. For synchronous 2 048 kbit/s connections, this may be performed by a re-timing function, for example. For other PDH connections an appropriate low-pass filtering function may be required.

A.2 Derivation of wander specification limits

For services which are provided by higher-order PDH connections, a short-term phase stability is required because these services normally use an adaptive synchronization to the received bit stream.

Short-term phase distortion is generated by the bit-stuffing techniques employed in asynchronous multiplex systems. This effect has first been studied for the PDH multiplex systems which use optimized stuff ratio values in order to minimize the effect. In SDH multiplex systems, the worst-case stuff ratio of zero-one is used, which generates short-term wander of an entire unit interval.

At the time of creation of the present document, SDH systems are widely deployed in the networks. This means that the network wander limit should be met by the existing SDH networks.

Referring to figure A.1 and figure A.2, PDH connections may pass through several SDH islands which are interconnected using PDH interfaces. In each of these SDH islands, phase distortion according to the bit- and byte-stuffing is created. For example, bit-stuffing is used when mapping the PDH payload to a VC-n payload and byte-stuffing (that is to say, pointer justification) is used when accommodation of the phase of the VC-n to the SDH frame is required.

In addition to the wander generated by the bit- and byte- stuffing techniques, the pointer processor hysteresis causes wander of the reference clock to be transferred to the PDH signal at the mapping or at the demapping node. The worst-case reference clock wander is caused by the reaction of the SDH Equipment Clock (SEC) function to a reference input switch event. The related phase transient has a maximum amplitude of 240 ns (refer to subclause 9.1 of EN 300 462-5-1 [9]).

This leads to the following two scenarios using a 34 368 kbit/s signal as the example.

1) Wander budget for 1 SDH island with phase transient at the demapping node (34 368 kbit/s signal)

The desynchronizer may use a digital PDH clock filtering circuit using the SEC output as a reference. This would cause the SEC output wander to be transferred to the recovered PDH clock.

Furthermore there may be a single pointer justification added to the phase offset just before the appearance of the SEC output transient.

The resulting wander budget is the following (values are rounded):

± stuffing:	60 ns
SEC phase transient:	240 ns
TU-3 pointer justification:	160 ns
Total:	460 ns

NOTE: The stuffing effect at the mapping node takes into account the reference clock noise at that point and the phase transient represents the reference clock effect at the demapping node. The effect of the intermediate network is taken into account by one pointer justification.

2) Wander budget for 1 SDH island with phase transient at the mapping node (34 368 kbit/s signal)

Any phase transient (i.e. transient frequency offset) of the reference clock (SEC output) at the mapping node causes a modification of the stuff bit sequence which ultimately is compensated by the pointer justifications. Provided that not all the intermediate pointer processor buffers are at their threshold, no compensating pointer justifications are received at the desynchronizer node. Consequently, the PDH signal is recovered at an equivalent frequency offset of opposite polarity (this is known as the "phase ramp effect"). The 240 ns reference input switching phase transient at the mapping node consequently leads to a similar phase transient of the recovered PDH output.

The resulting wander budget is the following (values are rounded):

Mapping phase transient:	240 ns
Double pointer justification:	320 ns
Total:	560 ns

NOTE: The effect of the reference clock wander at the mapping node is taken into account by the phase transient and the effects of the intermediate network together with the effect of the reference clock wander at the demapping node is accounted for by the double pointer.

3) Wander specification limits

The values in the above wander budgets for the mapping and demapping nodes are worst-case values. However, the impact of a phase transient on the output wander cannot be calculated by simply adding the values of both wander budgets because reference clock switching is a rare event and should be considered at only one end of the connection. It is therefore considered reasonable to use a value for output wander of a single SDH network island of the order of 500 ns.

When four SDH network islands of such intrinsic wander are cascaded using a statistical wander accumulation approach, the intrinsic wander is multiplied by a factor of the square root of the number of cascaded islands (in this case, a factor of two). The result is a total network output wander of 1 000 ns.

This applies similarly to the 139 264 kbit/s connections with the only difference that the stuffing effect is almost zero.

From this follows that for practical specification purposes, the maximum short-term output wander at higher-order PDH interfaces would be of the order of 1 000 ns which is consequently defined as the first plateau of the output wander specifications defined in subclause 5.2 of the present document.

In order to derive the longer-term output wander specification, the effect of the reference clock phase noise has to be considered. This wander is bounded by a limit of 2 000 ns according to the synchronization network wander limit specification at long observation intervals. When the above analysis is done using the increased reference clock effect, the result is of the order of 4 000 ns which is the second plateau of the output wander specifications defined in subclause 5.2 of the present document.

Annex B (informative): Measurement methodologies for output wander

Instrumentation in accordance with ITU-T Recommendation O.172 [14] is appropriate for measurement of wander parameters at both SDH and PDH interfaces.

B.1 Synchronization interfaces

B.1.1 Synchronous signals (SDH and PDH bit-rates)

When the signal is synchronous (i.e. normally PRC-traceable), and is used to carry synchronization, its wander is measured by comparing its phase with that of another PRC. The test procedure for measuring MTIE of a synchronous signal is shown in figure B.1 (the standard estimator formula for calculating MTIE is given in annex B of EN 300 462-1-1 [5]).

The PRC used for the wander measurement need not be the same as that used to originate the synchronous signal, for most measurement applications. However, it should be noted that the worst-case frequency difference between two PRCs could give rise to a phase difference of the order of 2 μs per day.

NOTE: The relevant limits for synchronization interfaces are defined in EN 300 462-1-1 [5], EN 300 462-2-1 [6], EN 300 462-3-1 [7], EN 300 462-4-1 [8], EN 300 462-5-1 [9] and EN 300 462-6-1 [10].

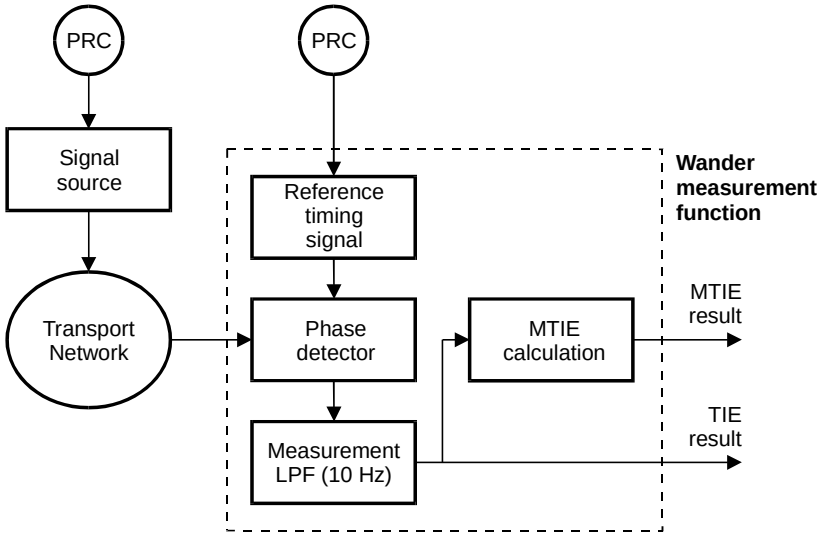


Figure B.1: MTIE measurement of synchronous signals

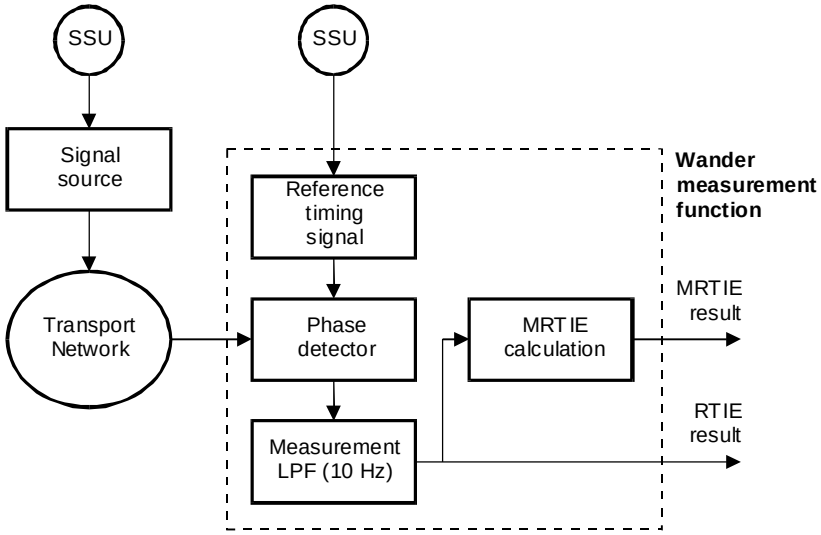
B.2 Traffic interfaces

PDH signals, such as 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s, can be either synchronous (i.e. normally PRC-traceable) or asynchronous (e.g. engineered to operate in a free-run mode with bounded frequency accuracy in accordance with ETS 300 166 [1] but no traceability to a PRC). For both cases, MRTIE is used as the wander specification parameter at network interfaces.

B.2.1 Synchronous signals (PDH bit-rates)

The wander limit for the synchronous PDH bit rate signals is defined as the relative wander of the PDH signal output at the transport network interface against the local network clock reference. This reference is represented by the SSU reference input to the wander measurement function in figure B.2.

While the output wander of a synchronization reference signal is to be tested against UTC which may be realized by a PRC (see figure B.1) the wander of synchronous payload traffic signals is to be measured against the local network clock reference as described above.



NOTE 1: SSU outputs conform to EN 300 462-3-1 [7] network wander limit.
NOTE 2: Both SSUs are traceable to a PRC (but not necessarily the same PRC).

Figure B.2: MRTIE measurement of synchronous signals

B.2.2 Asynchronous signals (PDH bit-rates)

In this case, a frequency difference can exist between the measurement reference frequency and the clock frequency originating the PDH signal, e.g. 50 ppm difference is allowed by ETS 300 166 [1] at 2 048 kbit/s. This difference causes a phase ramp in the measured wander, resulting in a distortion of the desired MRTIE phase parameter.

In order to support the wander reference model for PDH signals transported on SDH networks and the corresponding output wander specifications of subclause 5.2, two situations are described further:

- asynchronous signals, source reference clock available;
- asynchronous signals, source reference clock unavailable.

B.2.2.1 Asynchronous signals, source reference clock available

When the source reference clock is available at the measurement point, the MRTIE of an asynchronous signal may be measured as shown in figure B.3.

NOTE: The measurement point and the source reference should normally be co-located, in order to ensure that wander is not introduced into the measurement reference signals during transmission of the source reference clock.

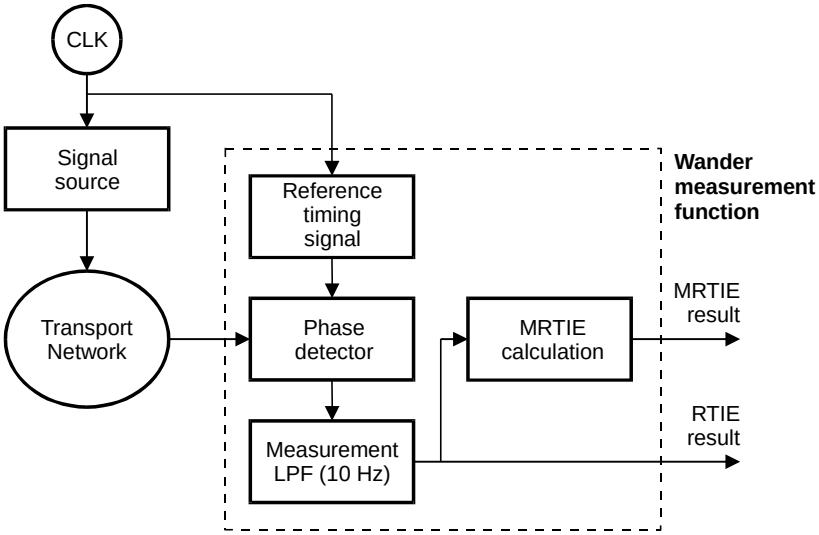


Figure B.3: MRTIE measurement of asynchronous signals, source reference clock available

B.2.2.2 Asynchronous signals, source reference clock unavailable

When the source reference is not available at the measurement point, there will be a frequency difference between the source reference and the measurement reference, resulting in a ramp of phase in the wander measurement. This phase ramp should be removed before MRTIE is calculated, otherwise the phase ramp would obscure MRTIE information of interest at longer observation intervals.

One method of removing the phase ramp is shown in figure B.4. This represents a "stop-start" method of measurement, where TIE phase samples are acquired, stored and post-processed to obtain the MRTIE parameter.

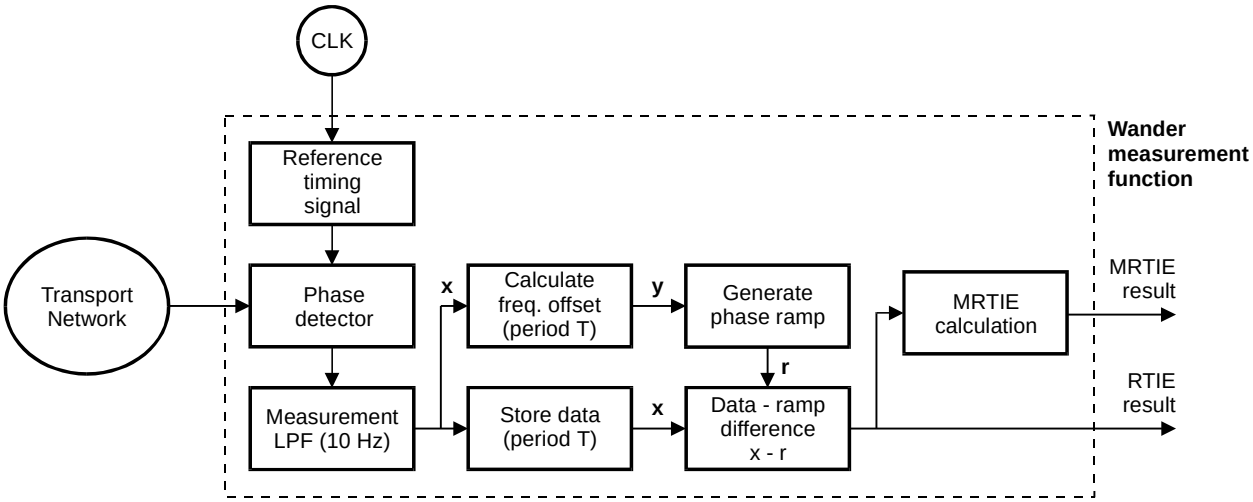


Figure B.4: MRTIE measurement of asynchronous signals, source reference unavailable

In this method, the frequency difference y (in ppm) is estimated by the algorithm:

$$y = \frac{0{,}006}{N\tau_0}\sum_{i=1}^{N} x_i\left[\frac{2i}{N^2-1} - \frac{1}{N-1}\right]$$

where τ_0 is the sample period in seconds, N is the number of phase samples in the measurement period and x_i is the TIE in ns. The results of the measurement will depend on the measurement period $T = N\tau_0$ over which the frequency offset and MRTIE are calculated.

The net result of applying this measurement method is to remove any frequency offset and wander frequency components below $f_c = 0{,}3 / T$, so that frequencies above $f_c = 0{,}3 / T$ contribute to the calculated MRTIE result.

NOTE: The signal source clock and the measurement reference clock should both have sufficient phase stability that the measurement result is only marginally affected by frequency drift effects, for example.

Annex C (informative): Measurement guidelines for input jitter and wander tolerance of equipment interfaces

A generic measurement set-up for jitter and wander tolerance measurements is shown in figure C.1.

NOTE: Not all elements are necessarily needed for every measurement of tolerance.

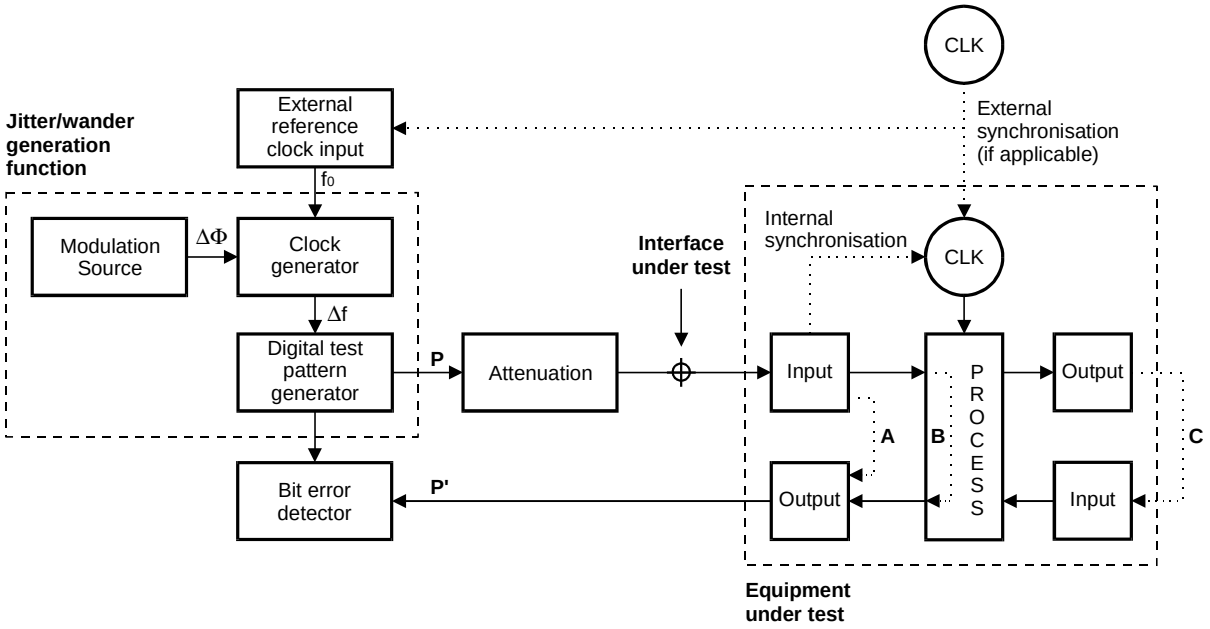


Figure C.1: Generic measurement set-up for input jitter and wander tolerance testing

The actual measurement set-up is determined by the following considerations:

Clock of equipment under test

The equipment under test clock can be externally synchronized (if a reference input is available) or it can be synchronized from the interface under test.

Constraints on Δf

The clock generator can be used to generate a fixed frequency offset Δf upon which the jitter and wander is modulated. The frequency offset should be limited to the values applicable to the interface or equipment under test. The frequency offset should be held constant during a stabilization period and the subsequent measurement. The allowed frequency offset can be dependent on the path that the measurement signal takes through the system and the way that the equipment under test clock is synchronized.

Constraints on ΔΦ

The modulation source is used to superpose a jitter or wander effect ΔΦ on top of the clock signal, which can also have a fixed frequency offset Δf. These jitter and wander phase perturbations usually have a sinusoidal, triangular or noisy (PRBS-generated) characteristic. The exact perturbations are defined in the applicable jitter and wander tolerance requirements.

Choice of test-pattern (P and P')

The test-pattern P should match the bit-rate of the particular interface that is being subjected to the jitter and wander tolerance test. Pattern P' is not necessarily the same as pattern P. It is of importance that a part of pattern P is present in P'. This part, Q, is passed transparently through the equipment under test. The bit error detector can only search for errors in this common part Q.

Routing the signal through the equipment under test

Depending on which parts of the system are actually to be tested and the capabilities of the equipment under test, the signal can be looped back in different configurations:

- directly behind the input (path A), to test the tolerance of the receiving circuitry;
- in the routing functionality (path B), which could test in addition, buffer hysteresis, stuffing mechanisms, etc.; or
- externally through some other inputs and outputs of the system (path C).

The choice of the actual path can influence the selection of test-pattern P' and the part Q, over which errors can be monitored.

Attenuation

The attenuation function is needed for optical interfaces in order to determine the 1 dB sensitivity penalty (in terms of optical power) at a certain bit-error ratio. For electrical interfaces the (frequency-dependent) attenuation should represent the worst-case cable length.

Annex D (informative): Relation between parameters for input jitter tolerance and output jitter limits

Annex D provides outline information regarding the relationship between output jitter specification and measurement bandwidths and input jitter tolerance mask specification corner frequencies.

The weighting filters for measuring output jitter at a network interface are given in table 1 of the present document; they are reproduced here in figure D.1 using the STM-1 interface as an example.

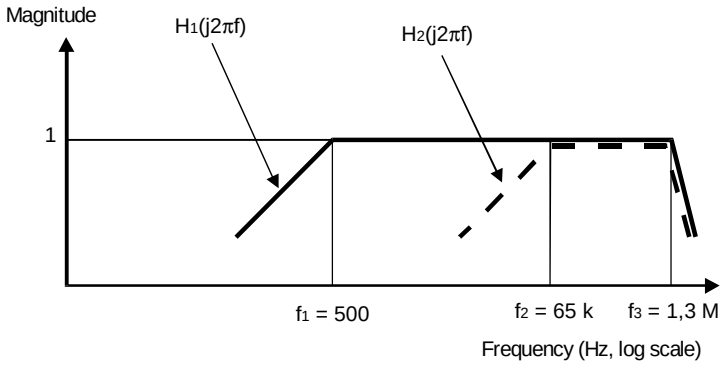


Figure D.1: Weighting filters for measuring STM-1 output jitter

$$H_1(s) = \frac{s}{s+\omega_1} \cdot \frac{\omega_3^3}{s^3 + 2\omega_3 s^2 + 2\omega_3^2 s + \omega_3^3}$$

$$H_2(s) = \frac{s}{s+\omega_2} \cdot \frac{\omega_3^3}{s^3 + 2\omega_3 s^2 + 2\omega_3^2 s + \omega_3^3}$$

$$\omega_1 = 2\pi f_1 \qquad \omega_2 = 2\pi f_2 \qquad \omega_3 = 2\pi f_3$$

The first term of the function $H_1(s)$ represents the phase error transfer function $H_e(s)$ of some PLL (phase-locked loop), and its amplitude of A_1 = 1,5 UIpp represents its phase error tolerance.

Then the corresponding input phase tolerance of the PLL is given by:

$$A_{tol1}(f) = \frac{A_1}{|H_1(j2\pi f)|}$$

Similarly, the input phase tolerance corresponding to $H_2(s)$ and its amplitude of A_2 = 0,15 UIpp is given by:

$$A_{tol2}(f) = \frac{A_2}{|H_2(j2\pi f)|}$$

These sinusoidal jitter tolerance masks are illustrated in figure D.2. If unweighted sinusoidal jitter at a network interface satisfies *both* of these masks, it also satisfies (i.e. lies below) a single mask that is the lower of the two masks for each frequency. Such a combined mask is shown as a dashed curve in figure D.3.

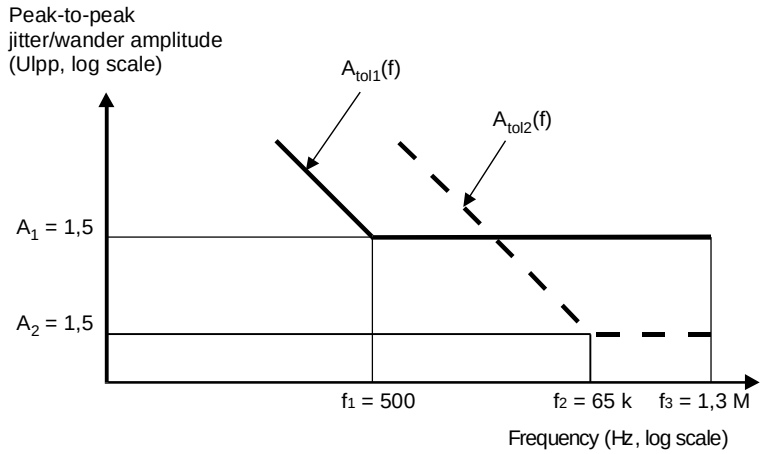


Figure D.2: Upper bounds on sinusoidal jitter amplitude at an STM-1 interface

Figure D.3 compares this combined mask with the STM-1 input jitter and wander sinusoidal tolerance mask (the solid line). They are the same in the range $19,3 < f < 1,3$ MHz. In the wander region of phase ($f < 19,3$ Hz), there are no interface specifications that use weighting filters to control the peak-to-peak phase.

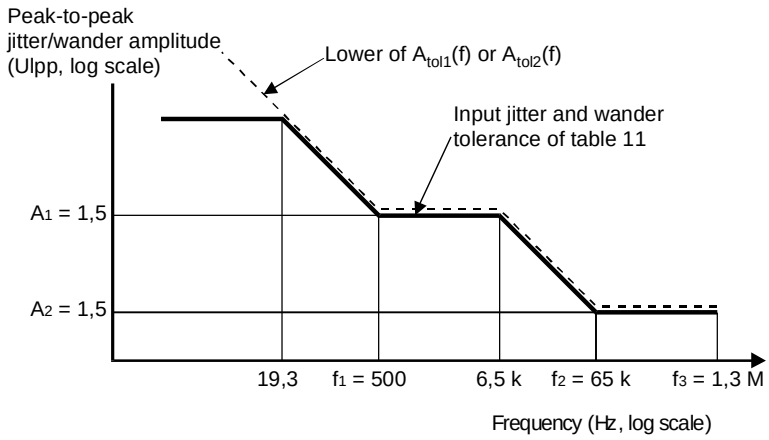


Figure D.3: Upper bound on sinusoidal output jitter at an STM-1 interface [lower of $A_{tol1}(f)$ or $A_{tol2}(f)$] compared with input jitter and wander tolerance mask

History

Document history				
V1.1.1	January 1999	Public Enquiry	PE 9918:	1999-01-01 to 1999-04-30
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