analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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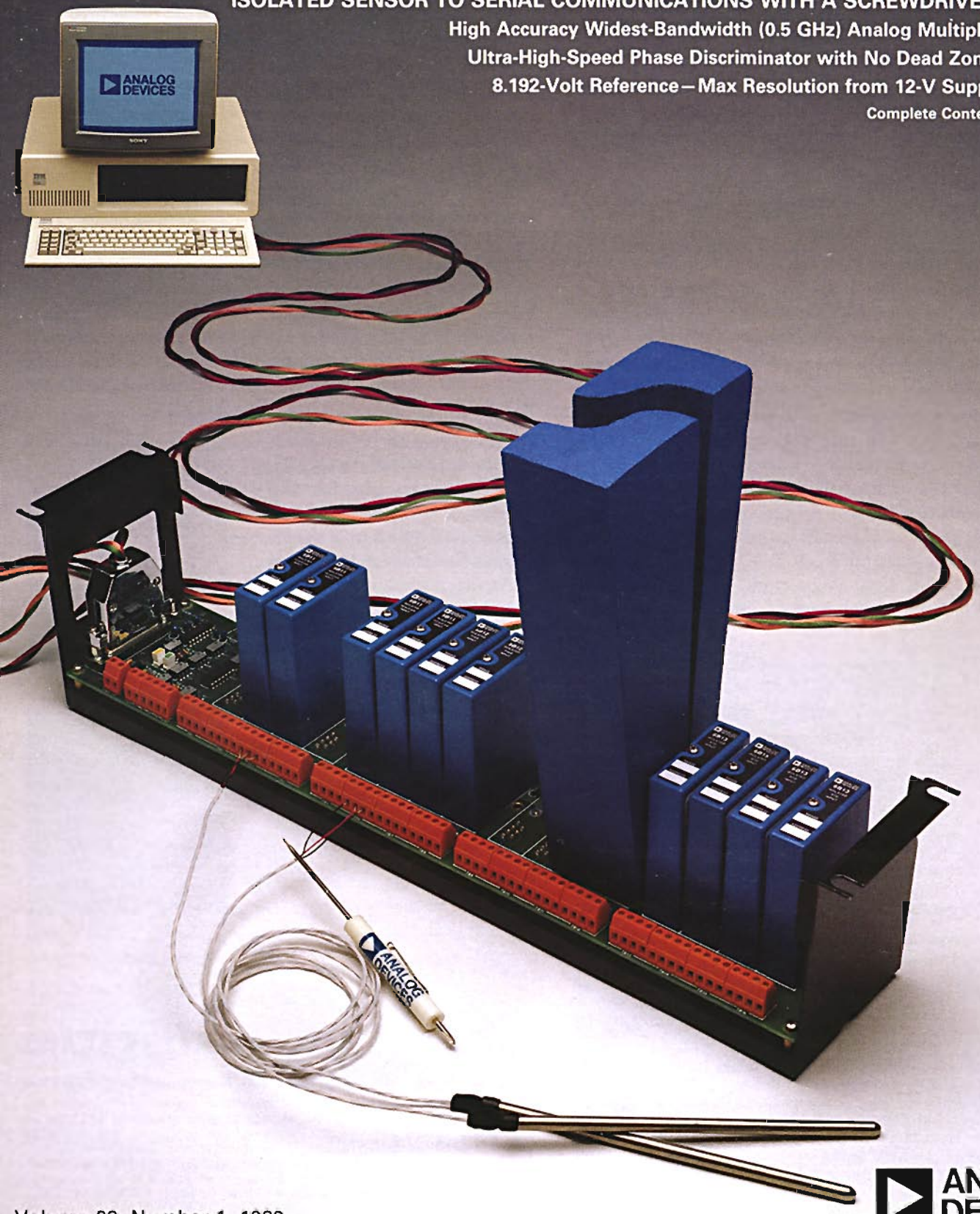


Volume 23, Number 1, 1989

ANALOG DEVICES

Editor's Notes

MULTIPLIER MEANDERINGS—REVISITED

Eighteen years ago we celebrated the arrival of the monolithic multiplier age with the AD530, the first commercially available *complete* analog multiplier on a chip.[1] In that issue, we used this column to wax historical about the multiplier scene in analog computing during the decades prior to this momentous debut.

We mentioned many of the approaches that had been used or considered, ranging from quarter-square (employing vacuum tube characteristics or piecewise-linear diode networks as a square-law approximation) to servos, crossed fields, masks, triangular-wave modulation, piecewise-planar functions of two variables, and Hall effect.

The method that ultimately made fast analog multiplication with precision readily achievable at low cost (one form was used in Dick Burwen's AD530) employs the *translinear* property of semiconductor junctions[2]—the *linear* dependence of *trans*conductance on collector current in bipolar transistors. It surfaced in a seminal paper by Barrie Gilbert.[3]

Since publication of the Burwen article, fortune has smiled on our multiplier efforts. Not only have advanced translinear architectures, together with laser-trimming of chips at the wafer stage, led to improved *multiplier accuracy* (the AD534—*Analog Dialogue* 11-1, 1977) and *speed* (the AD539—*A-D* 16-3,1982); they have also made possible low-cost monolithic devices for *root-mean-square* measurement (the AD536—*A-D* 11-2, 1977—through the AD736/37—*A-D* 22-1, 1988), *trigonometric approximations*[4] (the AD639—*A-D* 18-3, 1984), and *wideband logarithmic amplification* (watch this space in coming issues).

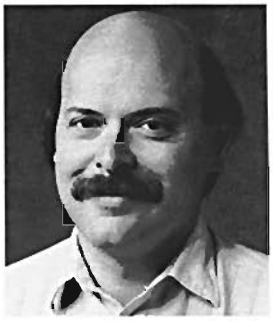
Publications to support the understanding and application of these products are available in impressive numbers. Besides data sheets brimming with information, currently available publications include the FREE *RMS-to-DC Conversion Application Guide*, 2nd edition (1986), and the classic: *Nonlinear Circuits Handbook* (1974), available from Analog Devices and still priced at only $5.95.

In this issue, we are pleased to mark the arrival on the market of the AD834, the all-time speed champion among monolithic analog multipliers, with response approaching the gigahertz region (yet excellent d-c behavior, too); it comes close to fulfilling, in a complete integrated-circuit device, the challenge inherent in the title of Gilbert's 1968 paper. Together with the devices mentioned above, it's a tough act to follow. Will the next 18 years be as prolific?

Dan Sheingold

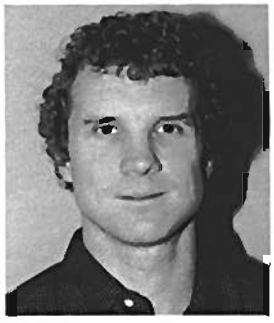
[1] "A Complete Multiplier/Divider on a Single Chip," by Richard S. Burwen. *Analog Dialogue* 5-1 (1971).
[2] "Translinear Circuits: A Proposed Classification," by Barrie Gilbert. *Electron. Lett.* 11, 1975 (14-16).
[3] "A Precise Four Quadrant Multiplier with Subnanosecond Response," by Barrie Gilbert. *IEEE Journal of Solid-State Circuits*, December, 1968.
[4] "A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and Their Inverses," by Barrie Gilbert. *IEEE Journal of Solid-State Circuits*, Vol. SC-17, No. 6, Dec. 1982 (1179-91).

THE AUTHORS

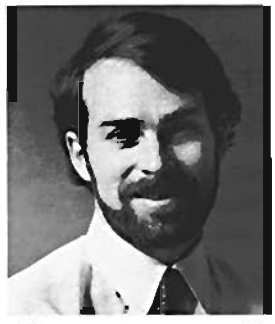


Norm Bernstein (page 3) is a Staff Engineer for the Industrial Products Division in Norwood, MA. Besides designing the 6B series, he designed the AD1170 and was a co-originator of the μMAC® series; he also designed the popular RTI-815 PC-compatible I/O board. Norm joined Analog Devices after graduating from Northeastern University with a BSEE in 1974. His leisure activities include sailing and boat-building.

Barrie Gilbert (page 8), a Division Fellow at Analog Devices Semiconductor, is a prolific designer, writer, teacher, and inventor, with numerous patents, publications, and awards. He is also a Fellow of the IEEE. A native of England, with a Higher National Certificate in Applied Physics (with honours), from Bournemouth Municipal College, he has worked at Mullard and Plessey. Joining ADI from Tektronix, his most visible linear-IC designs include the AD534, AD539, and AD834 multipliers, the AD536 rms IC, the AD537 VFC, and the AD639 trig-function IC.



Perry Jordan (page 10) is a Senior Project Engineer at Analog Devices' Computer Labs Division. He received his BEE from Georgia Tech and his MSEE from Florida Atlantic University. Before joining CLD, he worked at Motorola's Communications Division in South Florida. Perry's leisure-time activities include golf, softball, and other outdoor activities.



John Sylvan (page 12) is a Senior Technical Publicity Specialist at Analog Devices, in Norwood, Massachusetts. He has written numerous articles for a variety of publications. He has a BS in Administrative Science from Colby College, Waterville, Maine. In his spare time he enjoys sailing, skiing, and swimming.

(More authors on page 22)

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SENSOR-TO-SERIAL COMMUNICATIONS WITH A SCREWDRIVER

6B-Series I/O Modules Accept Variety of Inputs, Drive Current Loops Provide Conditioning, Scaling, Linearizing, and Digitized Output

by Norman Bernstein

The 6B series* of configurable digitizing signal-conditioning modules, an evolutionary step beyond the Analog Devices 3B and 5B analog signal-conditioner families, includes an a/d converter, microcontroller, memory, and serial communications within each module. The key to making it practical is surface-mount technology (Figure 1). The 1,500-V-isolated 6B module can be connected between a transducer and a serial port with a screwdriver and a +5-V power supply. A wide selection of sensor types, ranges, and digital numerical formats are available.

Each module provides signal conditioning, isolation, scaling, and a/d conversion; in addition, its embedded microcontroller provides many other benefits, such as ranging, autocalibration, linearization, and compensation for internal sources of error—including ambient temperature changes. For example, the 6B11, one of the series, handles all standard thermocouple types, as well as other voltage and current input sources, eliminating inventories of different modules. There are no manual trims or adjustments; all factory and user calibrations and settings, made via the communications port, are stored in non-volatile memory.

A 6B module is designed to interface to an RS-232 or RS-485 serial port operating at speeds up to to 19,200 baud; it is mounted on a 1-, 4-, or 16-channel backplane—a manifold—for physical support, power & field-wiring connections, and communications interface. As many as sixteen backplanes can be interconnected on a single multidrop link, providing up to 256 channels of transducer I/O. Each 6B module draws only 225 mW from the single +5-V dc supply required for operation.

At present, there are 4 modules in the series:

- the **6B11**, for thermocouples, ±15-mV to ±5-V voltage ranges, and 0- or 4-to-20 mA current inputs, is very similar in design and firmware to

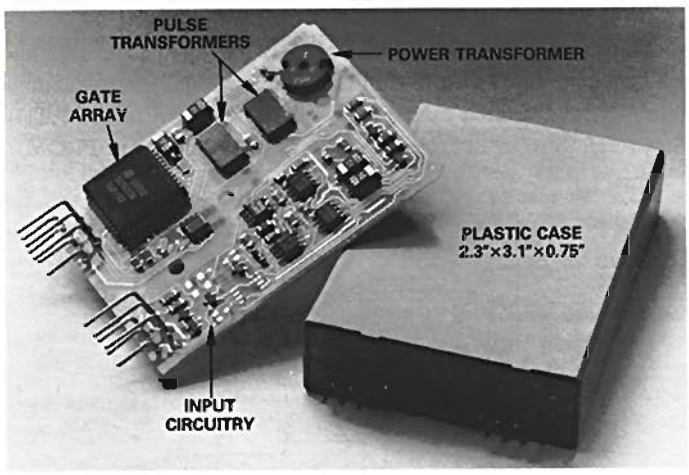
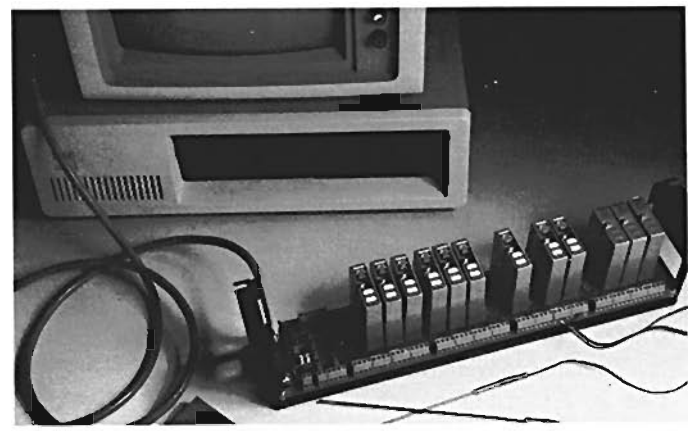


Figure 1. Module circuit board. The microcontroller and nonvolatile memory, plus other components, are on the other side of the surface-mount pc-board.

*Use the reply card for technical data.



- the **6B12**, which handles voltages (±150-mV to ±50-V ranges) or currents (to 20 mA).
- The **6B13** is specifically for RTD temperature measurement.
- For analog *outputs*, a 6B module to be introduced soon provides digitally controlled, isolated analog current-loop output of 0- or 4-to-20 mA.

Price (not including user-furnished +5-V supply) is $140 for each input module (100s), and $290 (1s) per 16-channel backplane.

INPUT MODULE DESIGN

Figure 2 shows the signal flow from input stage through the signal-conditioning and the charge-balancing a/d converter, which produces a train of synchronized pulses that cross an isolation

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barrier into a custom CMOS clock/counter chip. A microcontroller manages overall operation and interfaces directly to RS-485 line drivers and receivers. Isolated power, generated from the +5-V supply, is provided to the input side by the clock oscillator.

The input stage of the 6B module multiplexes several signals: Besides the analog input, V_{in} (with fault protection to 240 V rms), an internal reference voltage, V_{ref}, and an internal zero (ground), the mux accepts inputs from a local-temperature sensor and a cold-junction sensor, which are used in compensating for the internal temperature coefficient and the thermocouple termination temperature, respectively. Ten of the 20 conversions that the 6B module performs each second are for the analog input. The other mux inputs are sampled during the remaining conversion cycles.

The 6B module uses a synchronous voltage-to-frequency a/d converter (similar to the AD651, *Analog Dialogue* 20-2) to measure the input against the difference between V_{ref} and zero, two significant points of a straight line relating an analog input to corresponding converter output. This method relies on the ratio of the input signal to the difference between the endpoint values, rather than just the absolute value of the reference voltage. Key to module accuracy is the linearity of the v/f converter transfer function; but its stability with time is not critical, because the zero and full-scale end-point values are re-established frequently (nearly as often as the analog signal conversion itself).

Reference Calibration: Determining the actual value of the analog input requires a stable reference that can be calibrated. As long as V_{ref} (nominally 6.4 V) is stable, its absolute value is not critical. In calibrating it at the factory, both a precisely known analog input and V_{ref} are converted. Their ratio is stored in EEPROM and used as a correction factor in subsequent calculations.

Gain and Ranging: A programmable-gain amplifier (PGA) between the mux and a/d converter is set digitally by the user so as to make maximum use of the converter's full-scale range. Because they can be calibrated, the absolute accuracy and ratios of the gain values are not critical (if within a few percent), but the temperature coefficients of the ratios between gain ranges are important to consider.

Digital Temperature Compensation: The temperature coefficient of the reference is a major factor in overall accuracy; but instead of using a costly reference with the lowest possible tempco, the 6B11 and 6B12 modules use an internal temperature sensor to measure the module temperature; they then apply reference-correction factors based on the reading.

The local-temperature sensor within the module is uncalibrated but linear over the operating temperature range. At the factory, conversions are performed with the module at 25°C and 85°C, to obtain a measure of the uncompensated tempco of the module. This ratio is used by the microcontroller to compensate for the drift at temperatures within the span, reducing net drift by factors of 10 or 20 and resulting in overall tempcos of 2-3 ppm/°C in the 6B11. Over its operating temperature range of –25 to +85°C, accuracies to within ±0.5°, ±0.005% of FS, and ±0.008% are typical for thermocouple, voltage, and current measurements, respectively.

Isolation: The pulse output of the v/f converter passes to the non-isolated side of the 6B module through a transformer, which need not be designed for analog, modulated signals; its windings are etched tracks on the circuit board. A U-I core set, clamped and glued into a cutout hole in the board, completes the transformer; its rms isolation rating (including tracks) is 1,500 V.

Gate Array: The pulse-transformer signal goes directly into a custom gate array, which provides counting and frequency-to-binary number conversion. The gate array has a crystal-controlled clock oscillator and two counters, which produce counts of the v/f signal and the period of the reference clock. The count values undergo final processing in the microcontroller. The gate array also provides a driver for the isolated front-end power.

Microcontrol: An 8052 microcontroller is the computational and communications heart of a 6B module. It contains the entire executable program memory and performs scaling & ranging, calibration, internal temperature correction, and linearization (if needed). Count values from the gate array are converted from fixed-point binary to single-precision floating point—a 23-bit mantissa and 8-bit exponent—for all calculations.

Output data, represented with ASCII characters, is available to the user in three formats:

- scaled engineering units, including sign, a 5-digit number, and an appropriately located decimal point
- percentage of full scale (±100%) with fixed decimal point and 0.01% resolution, preferred in some control-loop applications
- twos-complement hexadecimal binary (the most compact form), from positive full scale (7FFF) to negative full scale (8000).

Both factory-set calibration factors and user-defined calibration and module data (such as desired input type and range, module number, and desired numerical format) are stored in the 1,024-bit, serial in/serial out, electrically-eraseable PROM (EEPROM).

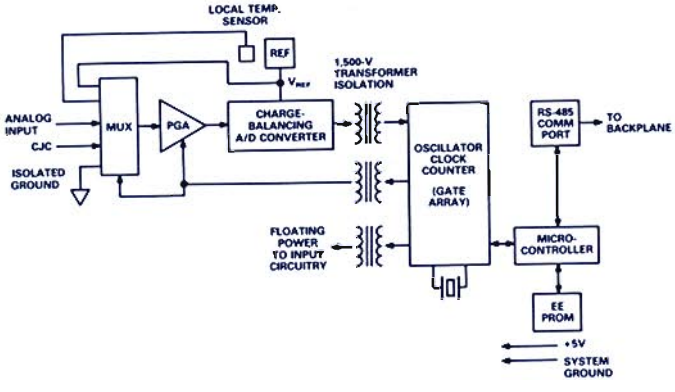


Figure 2. Input Module (6B11) block diagram.

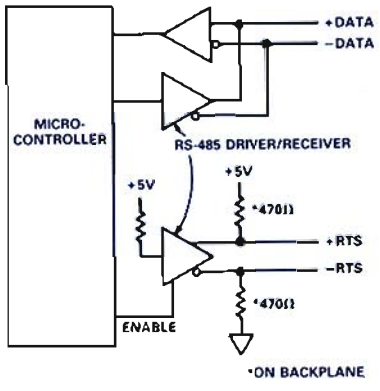


Figure 3. Serial communications circuitry.

Each module continuously takes readings of its analog input and other inputs (even if there is no user request), performs the conversions and calculations, and places the result in a buffer (in the microcontroller) for the serial port. A result is transmitted only when the host actually requests it; the last conversion result is always ready, and no reading is older than 100 milliseconds.

Serial Communications: The microcontroller interfaces to communications lines using a pair of RS-485 line driver and receiver ICs. Figure 3 shows how the bidirectional half-duplex scheme is wired. One wire pair represents incoming/outgoing differential data and the other pair is a differential handshake line for request to send (RTS). The RTS driver input is wired high, and the driver Enable is controlled by the microcontroller; the differential outputs of the driver have 470-Ω pullup (and pulldown) resistors, located on the backplane.

To avoid conflicts that would occur if several modules tried to send data at the same time, a simple command/response protocol is used: all modules normally listen to the data line. When the received message is addressed to a particular module, and the module must answer, it first asserts the RTS line by enabling the line driver. Then it turns the transceiver around and transmits, after which the module relinquishes the RTS line, allowing other modules to be accessed.

The use of an RTS signal means that the host-to-module link has two wire pairs rather than one, but this neatly solves two problems. First, RTS functions as a transceiver control line when connecting multidropped RS-485 units to a host using RS-232—a point-to-point standard that does not directly support multidrop operation. RTS also controls the direction (transmit/receive) of in-line repeaters; this can increase the transmission range to 4,000 feet for each inter-backplane segment. Because nothing happens until the RTS control signal is received, line and repeater propagation delays are not critical factors.

The 6B-Series Output Module: Many industrial control applications require a 0-to-20 mA or 4-to-20 mA digitally controlled current as the output to drive a recorder, actuator, or indicator. This module responds to digital inputs and provides currents up to 20 mA with 12-bit resolution into a load of up to 750 Ω. Since loop power is transmitted across the isolation barrier, no loop supply is needed.

The user can set the zero point of the range (0 or 4 mA), as well as the power-up default output current, a convenience in applications where the traditional "power-up at zero" is not flexible enough. In addition, the output-current setpoint can be read back to the host.

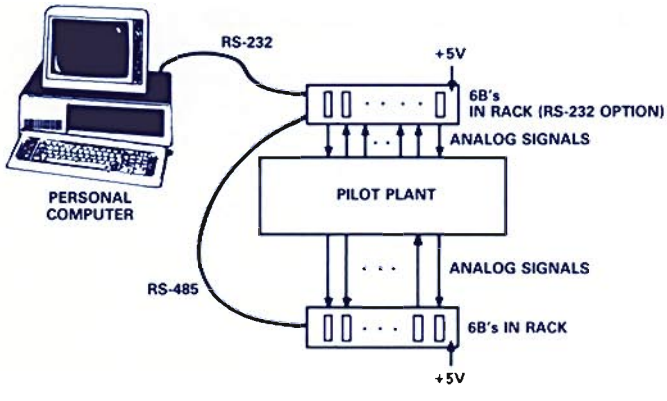


Figure 4. Pilot-plant application.

Backplanes: Backplanes for the 6B modules provide physical support, terminations for field transducer wiring, and connections for communications interfaces. A screwdriver is the only tool needed for all connections. All backplane models have the RS-485 interface, for use with compatible hosts and for daisy-chaining to additional backplanes. The 4-wire RS-485 interface can drive a twisted-pair cable of up to 4,000 feet in length.

HANDLING ANALOG INPUTS

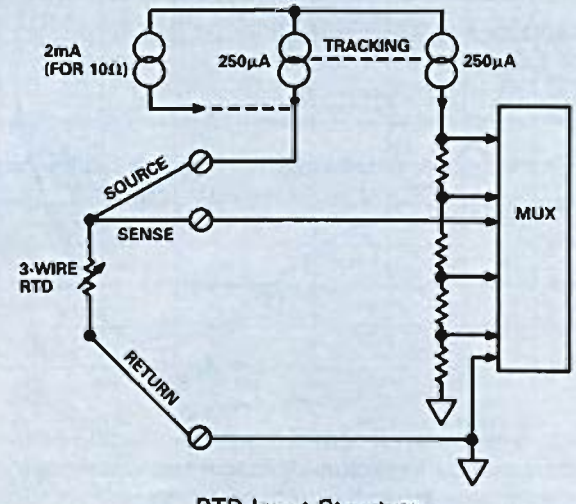
There are numerous similarities and some key differences among the three input modules. The low-level-input 6B11 has an input impedance of >100 MΩ; the 6B12, for higher signal levels, uses an input attenuator and provides a 1-MΩ input impedance. These two modules are otherwise identical, and the microcontroller code is essentially the same as well. Thermocouple linearization is accomplished using straight-line segments (see Box: *Linearizing* on page 6).

The RTD-input 6B13 uses a unique input design made possible by the nature of the sensor. The three-wire RTD interface (see figure) compares the ratio of the RTD resistance to that of an internal resistor, as measured by voltage drops. An internal resistor string provides ranging for different types and ranges of RTDs: platinum (100 Ω at 0°C), nickel (also 100 Ω), and copper (10 Ω). Excitation for the RTD and the internal resistors is furnished by a tracking pair of 250-μA current sources.

The input reading must provide lead-wire compensation, since any voltage drop in the wires to the RTD itself would otherwise be interpreted as resistance (and temperature changes) in the RTD. In the 6B13 this compensation is performed digitally. Since no current flows into the Sense lead input, the voltage difference between the Source and Sense inputs is entirely due to IR drop in the source lead. The software subtracts twice the measured value to compensate for source- plus (similar) return lead resistance.

For the 10-Ω copper RTD, the 250-μA source current is too low to provide adequate drop across the RTD. Rather than change both current sources—or the mux range resistors—a tracking 2-mA source is paralleled with the 250-μA RTD source; the known ratio between the RTD current source and the mux'd resistor current source is used in the calculations.

RTD linearization is performed with a 5th-order polynomial (unlike the straight-line segments of thermocouple linearization). This provides excellent conformance when done with the single-precision floating-point arithmetic.



RTD Input Structure.

An RS-232-interface option is available for connecting the first of 4, 8, or 16-channel backplanes to the commonly available RS-232 port of a computer. Also available, a single-channel RS-232 backplane is useful for test and evaluation.

Each 6B position is electrically identical to all others on the backplane and is equipped with a laser-trimmed cold-junction sensor in close thermal proximity to the field-wiring termination screws. When a 6B module is configured for thermocouple input, it automatically reads this sensor to determine the ambient temperature at the screws and uses the value for the cold-junction compensation calculation.

Software: All communications between the host computer port and the 6B modules use command/response protocol and ASCII characters. Communicating with the 6B modules requires simply assembling and sending character strings and parsing received strings. An optional checksum, which can be appended to verify data integrity, adds two characters to each command and reply.

An evaluation program disk is available for testing module functionality and setting all parameters (address, input type, range, output format, error checksum). The program also lets the user request readings from a module and displays the results. A driver program for tying in with TURBO Pascal™ (Borland) and a single-channel QuickBasic® (Microsoft) demonstration program, both with listings, are also available.

Drivers for industry-standard applications programs are also available for the 6B series. These drivers provide the user with easy and transparent access to the modules from Control EG™ (Quinn-Curtis), Labtech Notebook® (Laboratory Technologies), and The Fix™ (Intellution) packages, with their ease-of-use, user prompts, and graphics displays.

Figure 4 shows how a pilot-plant operation might be implemented with a personal computer running a standard application program (with 6B drivers) using several 6B racks, connected to the PC serial port. Each rack provides the needed combination of input and output modules, a mix that can changed as application needs change, often without changing a 6B module, since a single module handles such a wide variety of inputs. Communications protocols for the modules are transparent to the user, who initially configures the application program by simply telling it what sensor (type and range) is connected to each 6B module, by its logical channel number.

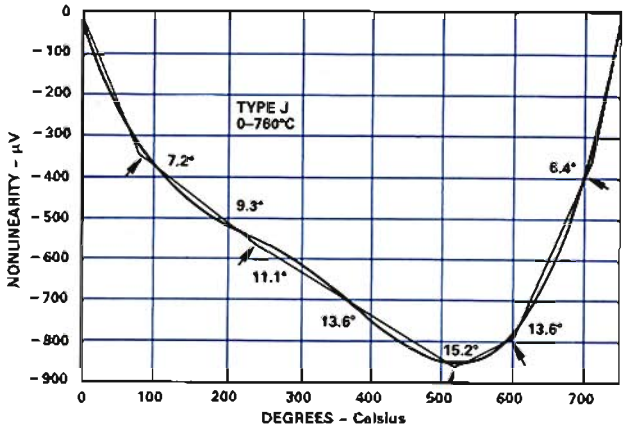


Figure 5. 6-segment piecewise linearization using patented algorithm, comparing actual deviation from linearity in µV with correction—as a function of temperature reading. Arrows indicate breakpoints.

LINEARIZING

The temperature-to-voltage output transfer function of a transducer, such as a thermocouple, is precise and repeatable, but nonlinear. Linearization, needed for accurate temperature readings, has traditionally been achieved with carefully designed analog circuitry in the conditioner or software calculations in the host.

The 3B and 5B Series of analog signal conditioning modules (*Analog Dialogue* 16-3 and 20-2) use piecewise-linearization circuitry with breakpoints between segments, and segment slopes established by resistor and diode combinations around op amps.[1] For the 6B modules, the digitized analog input value points to a specific entry in a look-up table, where linearization slope (m) and intercept (b) values are stored. These values are combined with the raw value in a standard $y = mx + b$ calculation to produce a linearized value.

Regardless of the implementation means, determining the best choice of breakpoints and slopes to minimize the error for a given number of straight-line segments is not easy. The simplistic approach is to divide the overall range evenly by the number of allowed segments, and select the straight line over that segment that produces the smallest error from the correct value while ensuring that endpoints are contiguous. But equally spaced breakpoints produce segments with trivially low and others with unacceptably large errors; and adding more segments is costly. Unequally spaced breakpoints provide better results, but determining the best breakpoint spacing is difficult and involves considerable trial-and-error.

A patented algorithm[2] provides a better solution to producing a piecewise approximation to a curve described by a closed-form expression, such as a polynomial. For any predetermined number of segments, both the locations of the breakpoints and their slopes are optimized. For temperature, error is measured for a given increment by dividing the approximation error (µV) by the slope of the increment (µV/°), yielding error in degrees (Figure 5 shows 6-segment piecewise linearization).

The algorithm begins with a guess at a reasonable error band and divides the curve into 1% increments. It then draws the longest chord from the starting point of the curve such that the error at each of these increments is less than the error band. This gives a unipolar error with maximum less than the error band. The end of the chord is extended beyond its intersection with the curve, increment by increment, until it is as long as possible without exceeding the error band on the other side. This yields the longest segment possible within the specification. Each successive segment starts at the end of the preceding one and uses the same method.

When the approximation is complete, if not all of the available segments are used, the error band can be reduced; if all segments have been used and the maximum error in the last segment is too great, then the error band is too tight. Further analysis of the error function yields improved approximations, leading to an optimum. The numbers in Figure 5 indicate pre-linearization errors at the ordinates; the linearized error is $<\pm 0.45$°C, for a 30:1 improvement.

[1] Sheingold, D. H., ed., *Nonlinear Circuits Handbook* (1974), available from Analog Devices ($5.95).

[2] Howard R. Samuels (Analog Devices, Inc.), U. S. Patent 4,774,685, *Approximation System.*

REFERENCE MAXIMIZES RESOLUTION FROM 12-V SUPPLIES

AD689 Has 8.192-V Output, Stability to within <5 ppm/°C Provides Round-Number Scaling: 2 mV/LSB For 12-Bit Systems

by Bill Schweber

The AD689 monolithic voltage reference[1] provides a fixed 8.192-volt output, operating with a range of excitation voltages from 10.8 to 36 V. This reference is principally intended for systems with a nominal 12-V ± 10% supply; at the lower limit (12 V – 10% = 10.8 V), there is insufficient headroom for a 10-V reference to function. Many computer peripherals, such as disk drives, lack the 15-V supply that a 10-V reference would require.

The 8.192-V reference output corresponds to 2 mV/LSB in a 12-bit system (8.192 V/4,096). In contrast to a 5-V reference, often used with 12-V systems (1.2207 mV/LSB), the AD689 provides 64% greater effective range and analog resolution. Signals digitized within this increased range are less affected by noise, and reference error constitutes a smaller percentage of the measured value. The "round-number" 2 mV/LSB factor eases software scaling between digital and analog I/O values.

As in the 5- and 10-V AD586 and AD587 references (*Analog Dialogue* 21-2), the heart of the AD689 is a proprietary ion-implanted buried-Zener diode reference cell and amplifier (Figure 1). The design of the AD689 relies on high-stability thin-film resistors that are laser-trimmed for high accuracy and low drift. For the highest-grade device (L), initial accuracy is within ±4 mV (±16 mV for the J grade), while drift is less than 5 ppm/°C (25 ppm/°C for J). Long-term stability of the reference value is 15 ppm/1,000 hr. A fine-trim connection is available for applications which require even higher initial accuracy (or 8.000 V full-scale). The trim range is at least +8%, –3% of the nominal output.

A reference's noise output critically affects the overall results that can be realized in a system. For the AD689, low-frequency noise (0.1 to 10 Hz) is typically <2 μV peak-to-peak (p-p). Wideband noise, to 1 MHz, is below 400 μV p-p. The buried-Zener cell is the dominant noise source; it contributes about 100 nV/$\sqrt{\text{Hz}}$. A noise-reduction pin permits the broadband noise to be reduced to 200 μV p-p by the use of a 1-μF capacitor, which combines with the bias-compensation resistor, R_s (40 kΩ), and the Zener resistance to form a 12-Hz (–3 dB) low-pass filter.

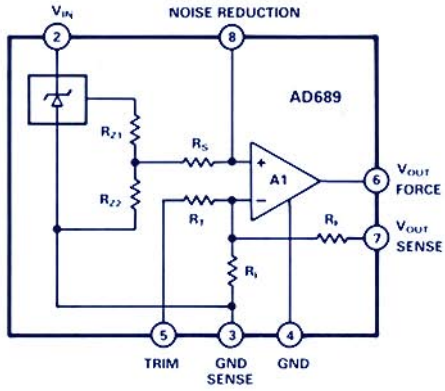
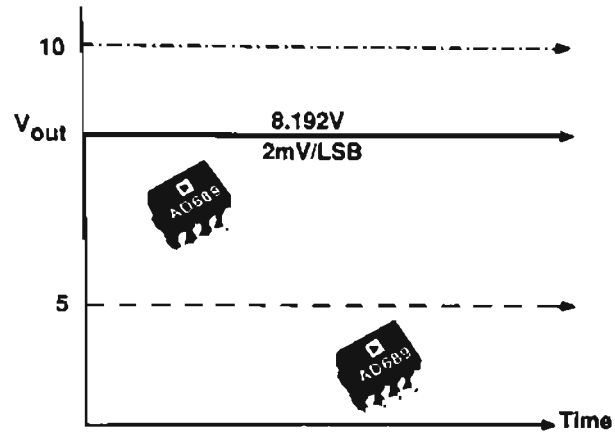


Figure 1. Functional block diagram of the AD689

[1]Use the reply card for technical data.



Force and Sense Connections: Amplifier A1 amplifies the Zener voltage to the required 8.192-V value. It also is configured to allow Kelvin connections from its output terminal to feedback resistor, R_F, as well as from its ground reference to the ground of the buried Zener and input-resistor (R_1).

Force and sense connections allow the user to realize the accuracy of the reference at the load terminals by eliminating the effects of voltage drops in the leads between the reference and the load. Load current, I_L, flowing through lead resistance, R_W, produces an error equal to the product, $R_W I_L$ (Figure 2a). The force and sense connections available in the AD689 overcome this problem by including this voltage drop within the forcing loop of the amplifier and sensing the voltage at the load (b). This causes the amplifier to correct for errors at the load.

The error caused by line drops can be significant. A 1-kΩ load, sinking 8.192 mA from the reference through 2 feet (1+1) of No. 28 AWG wire (0.066 Ω/ft), or the circuit-board track equivalent, would have an error of 2 × 0.066 × 8.192 = 1.08 mV. This is greater than one-half LSB of error in a 12-bit system. Using the force and sense connections, the error is moved inside the loop, with increased reference output voltage for compensation.

The AD689 can sink or source currents up to 8.192 mA. It is available for temperature ranges of 0 to +70°C and –55 to +125°C. All performance- and temperature grades are packaged in 8-pin hermetic cerdip. Prices begin at $2.95 (100s).

The AD689 was designed by Robert Libert at Analog Devices Semiconductor, Wilmington, Massachusetts.

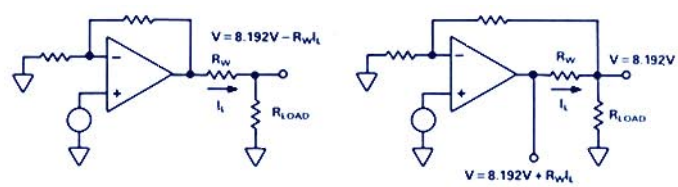


Figure 2. Force and sense connections. a. Error at load caused by line drop. b. Line drop included within the feedback loop; output is forced to the correct voltage.

HIGH-ACCURACY WIDEST-BANDWIDTH IC ANALOG MULTIPLIER

4-Quadrant AD834 Multiplies with Excellence from DC to 500 MHz

Use It for Power Measurement, Wideband Modulation & Gain Control

by Barrie Gilbert

The AD834[1] is a monolithic laser-trimmed four-quadrant analog multiplier designed for use in high-frequency applications. A descendant of the AD534[1] general-purpose multiplier (*Analog Dialogue* 11-1, 1977) and a cousin of the AD539[1] 2-channel wideband (60 MHz) multiplier (16-3, 1982), it combines 500-MHz minimum bandwidth (*both inputs*) and total low-frequency error less than ±2% of full scale to provide operation in all four quadrants, with low distortion, drift, and noise. Its uses include basic multiplication-related functions with typical applications in power measurement, modulation, and frequency doubling (through squaring).[2]

The relationship between its differential, high-impedance voltage inputs, X and Y, and its differential current output, W, is accurately given as

$$W = \frac{XY}{1\ volt} \cdot \frac{1}{250\Omega}$$

where $X = X_1 - X_2$ and $Y = Y_1 - Y_2$, for the range ±1V.

For 1 volt dc applied to one of the differential inputs, the relationship between the output and the other input corresponds to a transconductance of 4 mA/V. The output appears at a pair of open collectors, each drawing about 8.5 mA of standing current, which must be furnished from a voltage somewhat higher than $+V_S$ (e.g., at the high end of the $+V_S$ decoupling resistor).

With suitable external circuitry, the AD834 can perform all of the operations supported by the industry-standard AD534 and, if necessary, provide loadable, ground-referenced outputs. In most cases the upper usable frequency will not be limited by the AD834 chip, which has an intrinsic response extending beyond 1 GHz, but by the packaging and layout limitations and by the much lower bandwidth of the external active components.

The AD834 operates on supply voltages from ±4 V to ±9 V and consumes only 290 mW with the recommended 5-volt supplies. It

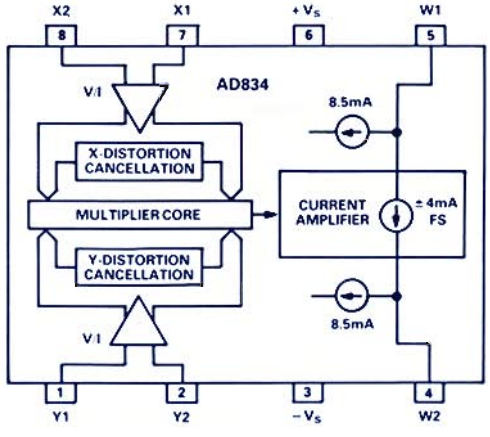
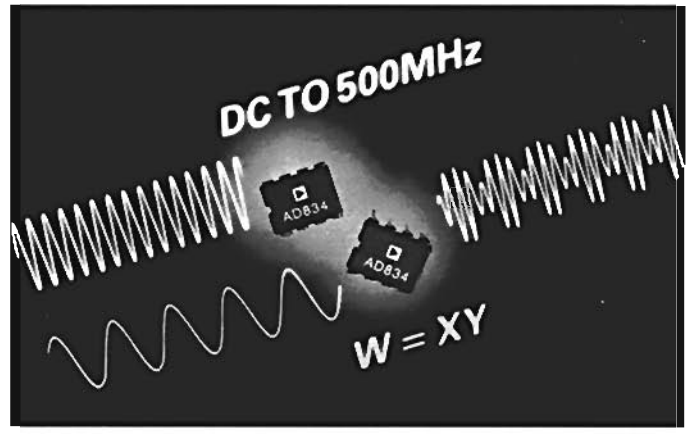


Figure 1. Block diagram of the AD834

[1]Use the reply card for technical data.

[2]For considerable information on analog multiplier design, specifications, testing, and applications, see *Nonlinear Circuits Handbook*, published by Analog Devices ($5.95). Use the book reply card.



is available in 8-pin cerdip (JQ) and small-outline plastic (JR) for the 0° to +70°C temperature range, and in cerdip (SQ/883B) for the −55° to +125°C range. Prices (100s) start at $19.20.

Figure 1 shows a block diagram of the AD834. Like all *translinear* multipliers, it exploits the *linear* relationship between *trans*conductance and collector current in bipolar transistors in a fast, accurate, current-in-current-out multiplier core. The wideband V/I converters at the input maintain almost the full bandwidth of the translinear core. Distortion due to nonlinearity in the input stages is almost eliminated by the subtraction of compensating currents derived through Kelvin sensing, in the core, of voltages which have the same error form. The raw current output from the core is buffered by a current amplifier, which also provides the correct laser-trimmed scale factor.

For a device with a current output, conversion to voltage—if needed—is provided externally by the user. The absence of on-chip voltage-to-current conversion has major advantages: first, the power dissipation of a wideband current-to-voltage output stage capable of driving 50-Ω loads and stray capacitance increases the power requirement—and the chip temperature in its vicinity, which affects core performance and dc stability. Second, many applications require wide bandwidth only for computing the product, but call for an averaged output that is relatively slowly

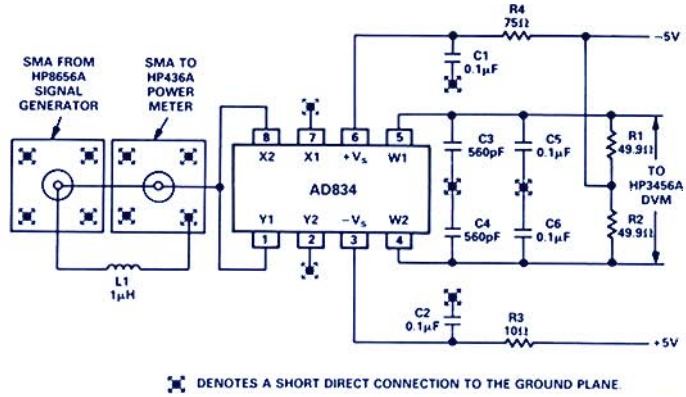


Figure 2. Connections for wideband mean-square measurements.

varying and can be handled with more-routine output amplifiers (an example is computation of r-f power). Third, for applications involving sums of products, the currents can be summed by simple paralleling of outputs. Finally, reduced chip size means improved yield and lower cost.

Figure 2 shows an example of a circuit in which the current is averaged and passively converted to voltage. It is a mean-square circuit, measuring the power content of a waveform by multiplying the input by itself, a simplified version of the general $A \times B$ power-measurement case. When driven from a constant-amplitude high-frequency sinusoidal source, the wideband output would be a fluctuating current at twice the input frequency with a mean (dc) value proportional to the square of the input amplitude. By placing capacitors directly across the load resistors, making a simple low-pass filter, the mean-square value is extracted. (For a frequency doubler, the filter capacitors would be omitted and the output would be ac-coupled.)

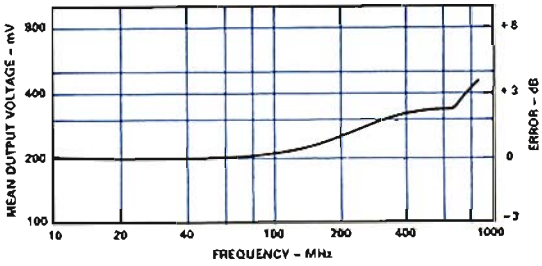


Figure 3. Mean-square output (represented by voltage) vs. frequency. Decibel scale represents error in the *power* measurement.

This measurement is a demanding test of a multiplier from the viewpoints of both amplitude and phase; both the wideband and the mean-square output will fall off faster at high frequencies than the response of either input channel measured independently. Small differential time delay (phase lag) between the inputs will affect the output at high frequencies, an effect absent when examining the response of each channel excited independently; and if the phase angle were 90°, the mean-square output would be zero; this corresponds to only 500 ps for an input frequency of 500 MHz. The measurement also has the advantage of not requiring a wideband measuring device at the output; a simple DVM connected across the load resistors will do.

Of course, extreme care must be taken to decouple the power supplies and use very short connections and low-inductance components to reduce response resonances. Figure 3 is a typical plot of mean-square output (represented by voltage) vs. frequency. The rising response is due to package resonances. Note that the output voltage indicates an error less than +1.5 dB of low-frequency mean-square value to beyond 250 MHz—and within +3 dB to almost 800 MHz.

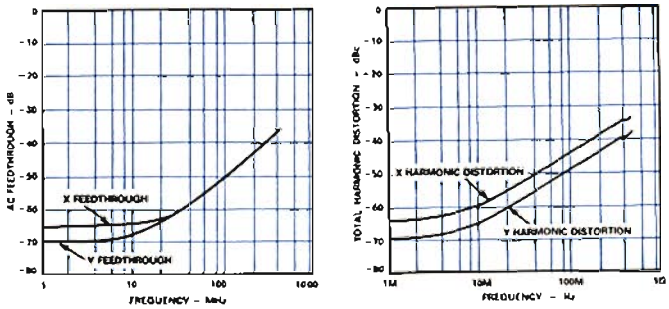


Figure 4. Feedthrough and total harmonic distoration vs. frequency.

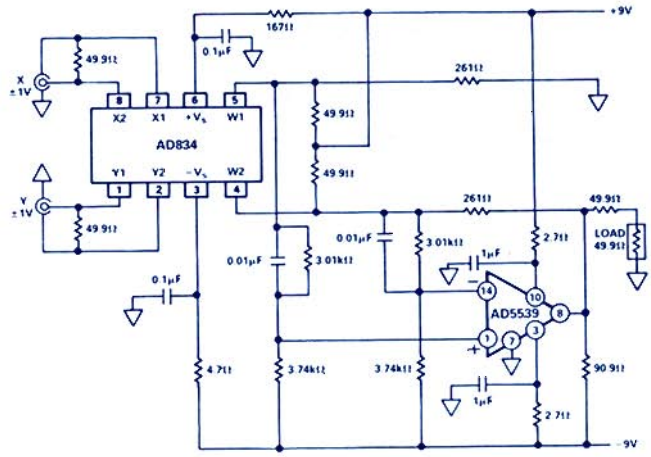


Figure 5. Direct-coupled voltage-output wideband multiplier.

AC feedthrough and total harmonic distortion are also quite low, as Figure 4 shows; well below –60 dB for 10 MHz-input(s), they increase to about –35 dB (<2%) at 500 MHz.

TYPICAL CONNECTIONS

The output can be either ac- or dc-coupled, depending on the needs of the application. Figure 5 shows connections for a wideband dc-coupled multiplier with *voltage* output into a 50-Ω load. Output voltage, $W = X\,Y$ (with a scale factor of 1.0 V^{-1}), where $X = X_1 - X_2$ and $Y = Y_1 - Y_2$; all variables are voltage. Instant-by-instant output polarity is correct for any combination of input polarities; it can be reversed by reversing connections to one of the inputs. Note the supply-voltage decoupling filters, the 49.9-Ω collector loads, and the subtractor connection of the op amp to bring the output to ground.

The op amp is chosen to support the desired output bandwidth. The AD5539, shown here, provides an overall system bandwidth of 100 MHz. The level-shifting network holds the input nodes of the op amp to within a few hundred mV of ground, using the recommended balanced supplies. Pulse output transition time is about 4 nanoseconds for a 0 to +1-volt pulse times +1 volt dc.

For ac-only applications, transformers are an effective means of coupling. Widest bandwidth is obtained with a *balun* (*bal*ance-to-*un*balance transformer), typically a length of coaxial cable or twisted pair threaded through several small toroidal ferrite beads, or wound onto a larger toroidal core. Figure 6 shows how a balun is used to couple the balanced output of the AD834 to a grounded output. For a very high-quality balun, bandwidth will be limited by the multiplier itself.

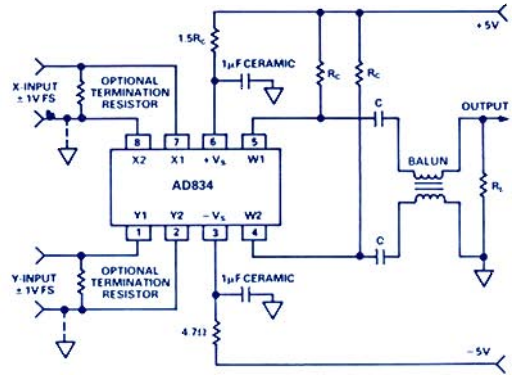


Figure 6. AC coupling with balun.

ULTRA-HIGH-SPEED PHASE DISCRIMINATOR HAS NO DEAD ZONE

AD9901 Digital Detector Has Low Noise, Linear Transfer Function ECL/TTL/CMOS-Compatible for Telecommunications, Synthesis

by Perry Jordan

The AD9901[1] Digital Phase/Frequency Discriminator (detector) is a monolithic IC that directly compares two inputs, then produces a train of output pulses with duty cycle proportional to the phase difference. It will handle signals of any frequency—to well beyond 100 MHz. Unlike many other detectors, the AD9901 has a linear transfer function through most of its range, without a "dead zone" around the zero point—which can introduce phase noise and lead to sluggish system performance and errors.

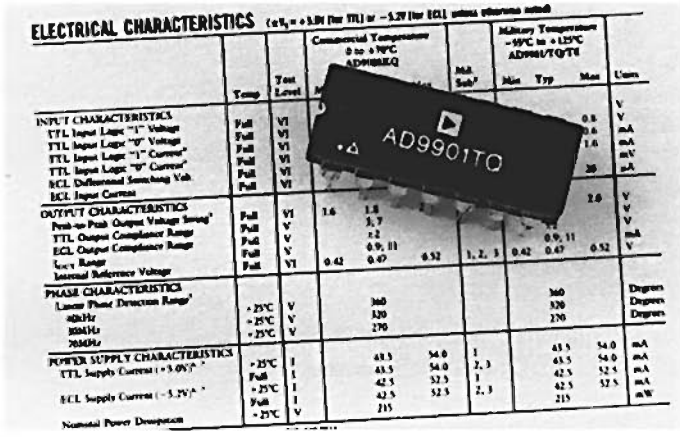
Fabricated in a trench-oxide-isolated process, the device requires a single supply and can be operated compatibly with TTL, ECL, or CMOS logic. The primary application of the AD9901 is at the heart of a phase-locked loop (PLL), as shown in Figure 1, for use in telecommunications, signal tracking and demodulation, and in establishing low-phase-noise references; when used in frequency synthesis, it can act as the local-oscillator tuning element of an IF stage. It requires a +5-V supply (TTL/CMOS) or –5.2 V (ECL); typical dissipation is 215 mW.

PHASE DETECTOR DESIGN AND PERFORMANCE

The simplest form of digital phase detector is the exclusive-OR gate (XOR): when the frequency-scaled oscillator output and the reference input are in the same state, the output is "0", and when they are in opposing states, the output is "1." If they are square waves (50% duty cycle) of the same frequency and exactly in phase, the output will be a steady 0; when they are exactly out of phase, the output will be a steady 1.When they are exactly 90° out of phase (the set- or "lock" point of the system), the average value of the XOR's output pulse train is 1/2 of full-scale; at other angles between 0° and 180°, the average value is in proportion.

Low-pass filtering produces a dc value, proportional to the phase difference, which drives the PLL's voltage controlled oscillator (VCO) to increase or decrease its output frequency so as to approach the correct phase/frequency to produce an average detector output of 1/2-scale, and so lock onto the input's phase. PLL operation has been extensively analyzed for many types of input signals, noise, and realizable circuit performance.[2]

This simple XOR scheme cannot discriminate effectively between a fundamental frequency and its harmonics; it can produce a "no error" output when in fact the input frequency is off by a factor of two. Also, it has restricted ability to adapt to sudden input-frequency changes.



The more-sophisticated scheme of the AD9901 (Figure 2), uses sequential logic (four D-type flip-flops, an XOR gate, and combinational logic) to form a phase comparator and a frequency discriminator. When the reference input signal and the oscillator input signal are very close in frequency, only the phase-detection circuitry is active. However, when the two input signals differ greatly in frequency (which is the rate-of-change of phase) the frequency-discrimination circuit overrides the phase comparator, producing a larger error signal, which drives the VCO more rapidly towards the reference-frequency value.

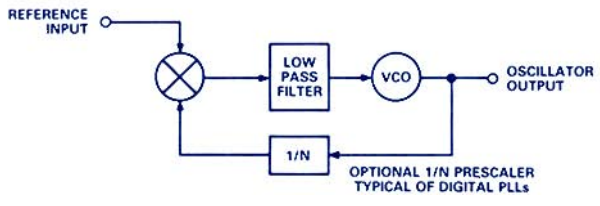
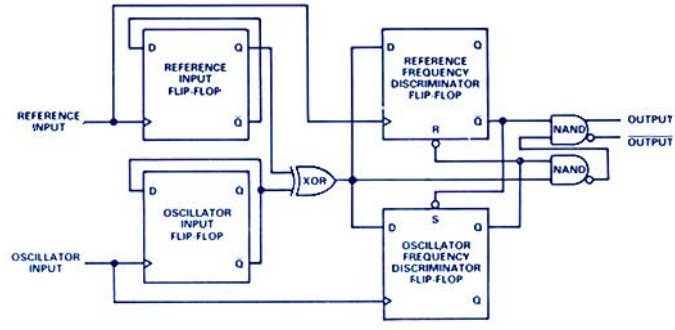
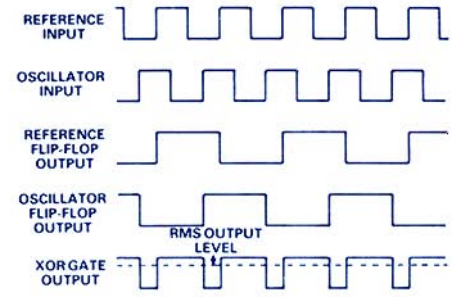


Figure 1. Basic phase-locked loop.



a. AD9901 functional diagram.



b. Waveforms with the oscillator's phase leading the input.

Figure 2.

[1]Use the reply card for technical data.

[2]References:

Best, R.G., *Phase-Locked Loops: Theory, Design & Applications*. New York: McGraw-Hill, 1984.

Gardner, F.M., *Phase-lock Techniques*, 2nd ed. New York: Wiley, 1979.

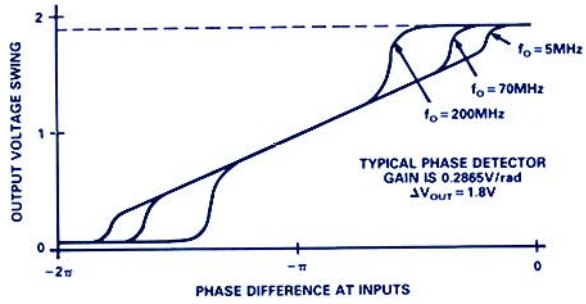


Figure 3. Linearity performance at 5, 70, and 200 MHz.

The AD9901 is designed for lock when the two signals are 180° out of phase. The duty cycle of the inputs does not affect accuracy, since the internal ÷2 circuit produces half-frequency symmetrical square waves. Figure 3 shows that the average output is linear throughout the specified range, without any dead zone at the lock point. The nonlinearities at the ends of the range are not as critical, since fine-scale PLL performance (stability and jitter) is determined primarily by response in the lock region.

The output of the AD9901 is a current (rather than a voltage), determined by a single current-setting resistor, and referenced to a temperature-compensated bandgap voltage reference. Thus the single-ended outputs, which can use simple passive filters, are temperature stable. A substantial output current of 10 mA is preferred in high-speed applications, because it produces large voltage swings with minimal load resistance, thus minimizing the parasitic pole associated with larger-value load resistors. The AD9901's output of 1.8 V p-p into 180 Ω is available even when configured for ECL operation. The linear phase-detection range is ±177° at 5 MHz, ±135° at 70 MHz, and ±50° at 200 MHz.

APPLICATIONS

Figure 4 shows a frequency-doubling PLL circuit for evaluating the AD9901 performance. In this design, the divide-by-two forces the VCO output to be between 95 and 125 MHz, at double the reference-signal frequency, with good phase stability. The oscillator's frequency is adjusted by a pair of varactor diodes. Single-ended VCO and reference signals are converted to complementary ECL (for improved power-supply rejection) by the AD96685 comparator and the ECL divide-by-2 flip-flop.

A PLL in the lock-in region is analyzed using traditional servo analysis techniques and has many selectable loop parameters. These include the nominal center frequency (110 MHz in this case), locking range (±15 MHz), the natural frequency of the control-voltage response, and the damping factor—which encompasses settling time and overshoot. Higher natural frequencies and less damping provide faster loop response to input changes, but with increased phase noise. For the filter component values shown, at the phase gain of the VCO and AD9901, the PLL will be able to lock onto any signal from 47.5 to 62.5 MHz, regardless of its initial state, and settle to ±5% within 1ms with an overshoot of approximately 25%.

Frequency Synthesis (Figure 5): These characteristics are significant in frequency-synthesis applications, where a multitude of local oscillator (LO) frequencies are generated by the VCO for the mixing stage of a superheterodyne receiver, but must have the stability and accuracy of a single reference. Since the divided-down output of the VCO must be equal to the reference frequency

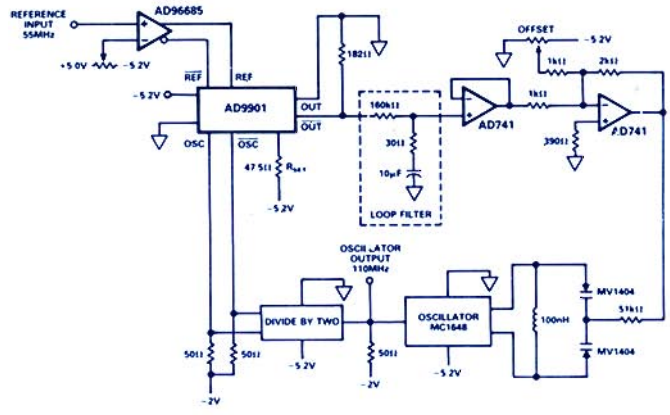


Figure 4. AD9901 evaluation circuit configured for ECL

at lock, the VCO's output frequency must be equal to the reference frequency times the divider ratio, N.

The result is ideal for digitally controlled tuning of the receiver's LO (and consequently the received signal), by adjusting N. The specified VCO output is mixed with the incoming r-f signal, and the result is tuned to the fixed intermediate frequency (IF). As an illustrative example, a VCO at 0.2 MHz and N from 387 to 486 produces LOs from 77.4 to 97.2 MHz. These LOs are then mixed with the received signal—from 88.1 to 107.9 MHz, with 200-kHz channel spacing, for the standard FM broadcast band; the difference, at a given N, is the common 10.7-MHz IF used in most FM broadcast-band receivers. The same concept applies to other bands, channel spacings, and IFs.

This application requires fast slewing by the PLL to the new frequency so that a selected channel is quickly reached, while minimizing overshoot and instability that cause mistuning. The system designer must consider circuit parameters and user requirements in closed-loop analysis of PLLs. The AD9901's wide input range and "no dead zone" make this much easier.

The AD9901 is available in ceramic DIP and LCC, for 0 to +70°C and −55 to +125°C operation. Prices begin at $8.00 (100s).

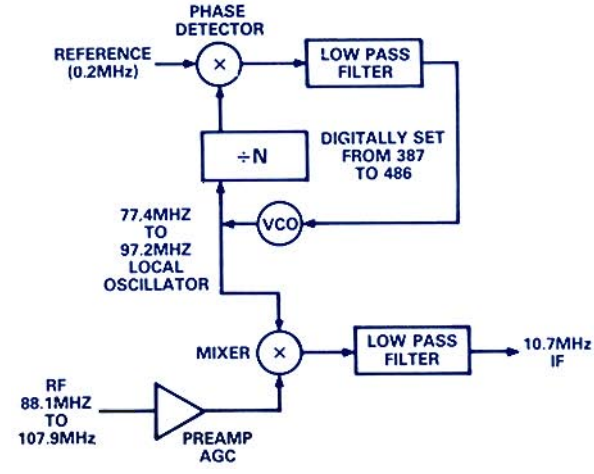


Figure 5. Digitally-controlled frequency synthesizer in mixer application.

NEW 12-BIT SAMPLING ADCs DIGITIZE FAST AC WAVEFORMS

Monolithic AD7870 and AD1678 Sample and Convert Analog Signals at up to 100 KSPS and 200 KSPS

by John Sylvan

The AD7870[1] and AD1678[1] use high-density linear-compatible bipolar/CMOS processes (LC²MOS and BiMOS) to combine an a/d converter (ADC), sample/hold amplifier, reference, and interface logic on a single chip. The ICs function as *sampling systems*, not just a/d converters. The devices' high conversion rates—up to 200 ksps for the AD1678—and dynamic specifications are useful in spectrum analysis, speech processing, and telecommunication systems. Some grades of the AD7870 have sufficient dc accuracy for traditional measurement-and-control applications that now require a separate SHA and ADC.

Besides the twofold difference in maximum sampling rates, they also differ in input signal range, input impedance, power-supply requirements, and interface logic. The AD7870 utilizes a standard successive-approximation architecture, while the AD1678 employs recursive subranging using "flash" conversion.[2]

RECURSIVE SUBRANGING

Recursive subranging improves an ADC's conversion rate by reducing the number of decision points. Figure 1 details the AD1678's architecture. Instead of the 12 trials needed for a 12-bit successive-approximation converter, the AD1678 requires only four passes on the input signal and delivers a maximum sample rate of 200 ksps. On each pass, a four-bit flash ADC digitizes the signal. The gain and offset of the flash are then adjusted so that the full scale of the flash operates within the range of the previous cycle's scale. A 12-bit DAC supplies the offset, and a programmable-gain residue amplifier sets the gain. The process is repeated four times at successively higher levels of gain, and the four digital values are combined to form the 12-bit output word.

Four 4-bit conversions could produce a 16-bit output, but the circuitry deliberately overlaps the MSB with the LSB of the previous cycle for error correction. In return for giving up one bit on each cycle (adding one cycle to the conversion process), the resulting overlapping ranges produce additional error correction of ±1/2 LSB beyond the ±1/2 LSB flash quantization error.

CYCLE	AMPLIFIER GAIN	FLASH RESOLUTION	OVERALL SIGNAL GAIN
1	1	1×	1
2	1	8×	8
3	64	1×	64
4	64	8×	512

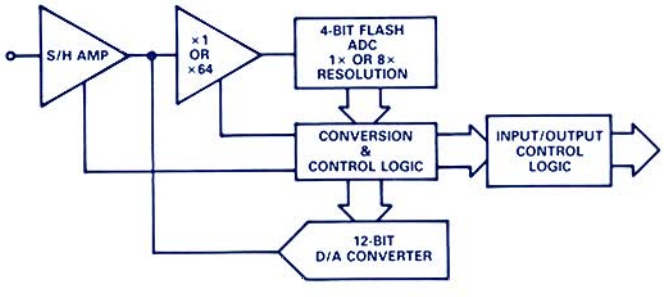
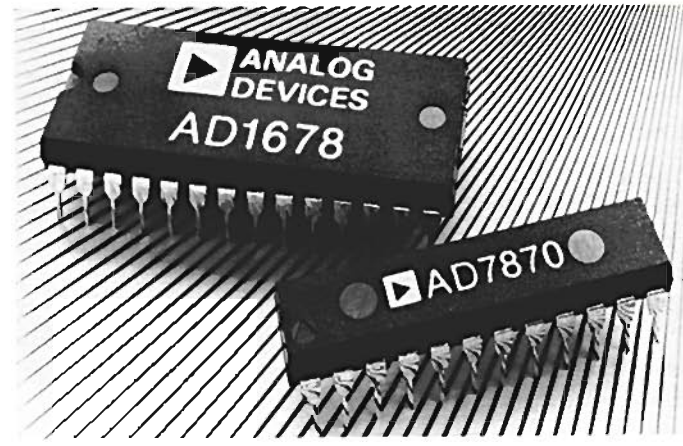


Figure 1. AD1678 functional block diagram.

[1]Use the reply card for technical data.

[2]See "A 14b 10 µs Subranging A/D Converter with S/H," by Fernandes, Lewis, Mallinson, and Miller, *1988 IEEE International Solid-State Circuits Conference Digest of Technical Papers*—Volume XXXI.



DYNAMIC VERSUS DC PERFORMANCE

Sampling ADCs can be used in traditional measurements, such as monitoring absolute voltage levels. In fact, several grades of the AD7870 have standard dc specifications: accuracy, linearity, offset, and gain. However, applications in dynamic or "ac" signal analysis are rapidly growing. In dynamic signal analysis, "spectral binning" issues predominate; and the ac performance of a circuit depends on the interplay of the s/h amplifier and ADC.

Spectral binning refers to extracting the frequency content of an analog signal at many discrete frequencies with digital-signal-processing techniques. Harmonics and noise added by the sampling ADC can corrupt the signal's spectral content. Thus, dynamic specs are needed to characterize system performance.

One of the key dynamic specifications applied to sampling ADCs is *signal-to-noise* ratio (sometimes called signal-to-noise-plus-distortion). SNR or (S/N+D) is the log-ratio (in decibels) of the rms magnitudes of the fundamental frequency and all non-fundamental signals (up to 1/2 the sampling rate and excluding dc). For an ideal 12-bit ADC, the SNR is about 74dB. All grades of the AD1678 and AD7870 guarantee 70 dB minimum over temperature. Figure 2 shows an FFT plot of the AD1678's output at 200 ksps with a 49.902-kHz input signal. As the graph makes clear, all harmonics are at least 80 dB below the fundamental.

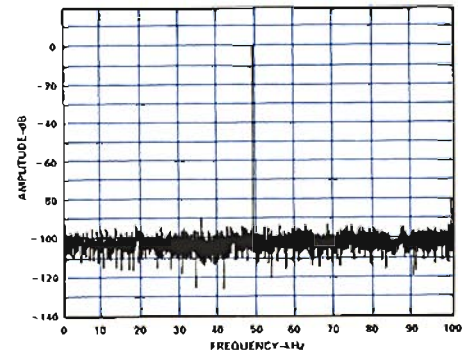


Figure 2. Non-averaged 2,048-point FFT of AD1678 response with 49.902-kHz sinusoidal input, 200-ksps sampling.

Distortion specifications include *total harmonic distortion* (THD), *peak spurious*, or peak harmonic distortion, and *intermodulation distortion* (IMD). THD is the log-ratio of the rms sum of the first six harmonics to the rms value of the measured input signal. Peak spurious is the log-ratio of the next largest component in the converter's output spectrum (excluding dc) to the fundamental. And IMD accounts for the sum and difference frequencies that can appear when the input signal contains sine waves of different frequencies. IMD performance is important in (for example) modem and other communication applications, where the modulated carrier signal contains multiple frequencies. Distortion specifications (THD, IMD, and peak spurious) for the AD1678 and AD7870 are –80dB, *maximum*.

Input bandwidth is another sampling-ADC dynamic performance specification; it is limited by the s/h amplifier. The input bandwidth should equal one-half the maximum sampling rate in order to pass all signals that satisfy the Nyquist criterion. It is desirable for this bandwidth to be "*full-linear*" bandwidth, implying that the input signal is attenuated by 0.1dB or less. At *full-power* –3dB-bandwidth, a full-scale input signal will be attenuated to 70% of its original amplitude.

Some applications require an input bandwidth in excess of the sampling rate (see *Analog Dialogue* 22-2, p.6). In undersampling applications, for example, a low-frequency baseband signal is recovered from a high-frequency carrier. The wide input-signal bandwidth also minimizes signal distortion, especially on high-slew-rate signals, such as square pulses. And it simplifies external filter design, since it reduces concern about the filter properties of the ADC itself at higher frequencies approaching and beyond Nyquist. The AD1678 guarantees 500-kHz full-linear and 1-MHz typical full-power bandwidth. The AD7870 has a typical 500-kHz —0.1-dB bandwidth.

PROCESSOR INTERFACE:

As microprocessors and DSPs attain higher clock rates, they demand faster access to memory chips and peripheral ICs, including ADCs. The AD7870 has a fast 57-ns maximum bus-access time, reducing the number of WAIT states required to read data; the AD1678's slower 100-ns access time is still faster than for most non-sampling converters. Both devices support 12-bit parallel and 8+4 dual-byte data transfer; the AD7870 adds serial.

When a high-speed signal processor has a serial data port (the Analog Devices ADSP-2101 has two), the processor can access memory over its high-speed parallel data bus while reading data from the converter simultaneously via the serial bus. After all the data bits are received in the processor's serial register, it can steal a single clock cycle to transfer the data to a memory location. Figure 3 shows the simple interface between the AD7870 and the ADSP-2101.The external timer's precisely timed Conversion-Start command, $\overline{\text{CONVST}}$, ensures uniform sampling.

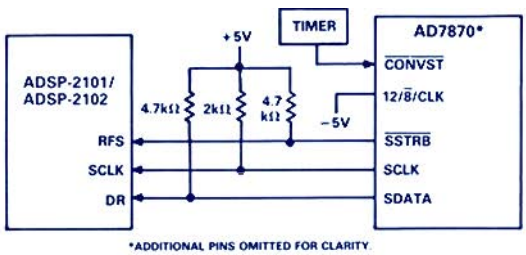


Figure 3. AD7870 interfaced serially to the ADSP-2101/2102 digital signal processor.

ASYNCHRONOUS vs. SYNCHRONOUS

Most signal-processing algorithms demand tightly controlled sampling intervals; variations appear as excessive s/h uncertainty, resulting in severely degraded SNR. For this reason, a sampling ADC should work in both "synchronous" and "asynchronous" modes. The former can be used where the processor has ample overhead to coordinate conversion starts and read the results. Where this is unfeasible, asynchronous operation uses a precise system timer for tight control of sampling intervals. Both the AD1678 and AD7870 have provisions to work in either mode.

Figure 4 illustrates maximum AD1678 throughput, programmed for asynchronous operation (SYNC tied Low). A precise timer initiates a conversion by bringing $\overline{\text{SC}}$ low, regardless of the state of the chip-select pin. The end-of-conversion signal, EOC, controls the state of the device's output Enable. On the falling edge of $\overline{\text{OE}}$, data from the previous conversion is latched into the output register and is available 100 ns later.

OTHER FEATURES

The AD1678 operates from ±12-V and +5-V supplies; it accepts a 10-V input signal span: ±5-V bipolar or 0-to-10-V unipolar. On the other band, the AD7870's ±5-V supply limits input signals to ±3V.

The internal s/h amplifier of the AD1678 has the added benefit of a 10-MΩ input impedance; an external buffer amplifier is not needed when driving the converter from ordinary sources. The AD7870's input impedance, not quite so high, is 15 kΩ.

The AD1678's pinout will be used on a family of sampling ADCs, including versions with both ac and dc performance specs, higher sampling rates, and 14-bit resolution. Thus system performance can be upgraded without board layout changes.

The AD1678 is offered in two grades, J and K, with respective minimum SNR of 70 dB and 71 dB. Available DIP packages are 28-pin plastic or ceramic. Prices start at $38.00 (100s).

The AD7870 is available in 9 different grades specified over three operating temperature ranges: 0 to +70°C (J/K/L), –25 to +85°C (A/B), and –55 to +125°C (S/T). The J/A grades are ac-tested but not specified for maximum integral or differential nonlinearity (INL or DNL). The K/B/T grades guarantee ±1-LSB INL and DNL and 70-dB SNR. The L/C grades guarantee ±1/2-LSB INL, ±1-LSB DNL, and 71dB SNR. Packages include 24-pin plastic DIP and cerdip, and 28-pin PLCC. Prices start at $20 (100s).

The AD1678 was designed by John Fernandes, Stephen R. Lewis, Martin Mallinson, and Gerald A. Miller at Analog Devices Semiconductor, Wilmington, Mass., and the AD7870 was designed by Roy Speer at Analog Devices BV, Limerick, Ireland.

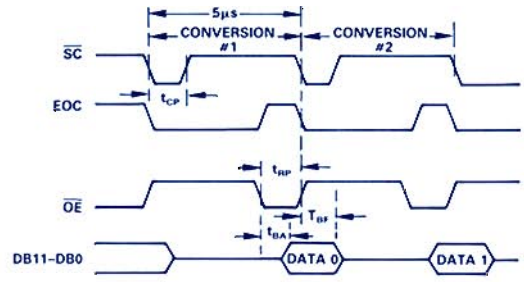


Figure 4. Reading out the AD1678 at 200-ksps—timing.

DUAL BIPOLAR OP AMP PROVIDES SUPERIOR MATCHING OF SPECS

AD708 Offset and Drift Matched to 25 μV and 0.3 μV/°C Max

Performance of Two Matched AD707s on a Single Chip

by Bill Schweber

The AD708 dual op amp[1] offers superior matching of dc specifications, while each op amp individually provides excellent dc precision and stability. This combination of dc performance with tight matching characteristics offers designers new opportunities for high-accuracy circuit performance. The AD708 design is based on the AD707 (*Analog Dialogue* 22-1), the first bipolar op amp with offset voltage drift below 0.1 μV/°C.[1]

Some obvious advantages of any dual device are savings in board space, along with reduced inventory and assembly operations. But often more importantly, a properly designed dual device can provide a near-isothermal environment and inherent matching of characteristics that inevitably drift with temperature and operating-condition changes. The designer has an opportunity to develop circuits (such as ratiometric ones) which take advantage of tracking to cancel out a large part of these drifts.

Minimum open-loop gain of 5 V/μV (10 μV/V typ), and CMR of 130 dB make this device ideal for high-gain, precision instrumentation amplifiers; they will also benefit from the matched characteristics. Open-loop gain is maintained over the full 10-V output range when driving a 2,000-Ω load. Maximum input offset voltage and drift (AD708S) are 25 μV and 0.3 μV/°C. Input bias current is 1.0 nA maximum, with drift below 25 pA/°C (AD708B), and offset current drift is typically 1 pA/°C.

Noise can also set limits to overall system performance. From 0.1 to 10 Hz, the guaranteed maximum input voltage noise is 350 nV peak-to-peak (AD708S). The 1/*f* noise corner is at 0.7 Hz; input noise spectral density is less than 11 nV/$\sqrt{\text{Hz}}$ at 100 Hz.

Matching Characteristics: "Matching" is the difference between parameters of the two amplifiers; the matching of three parameters of this dual op amp are important for many designs. *Offset voltages* of the two devices in the AD708S are matched to 25 μV (maximum), and offset voltage *drifts* (which, unlike offset voltage, cannnot be trimmed out) track to better than 0.3 μV/°C. Input *bias currents* are within 2 nA of one another.

Crosstalk: A dual op amp can have a signficant disadvantage compared to a pair of discrete devices if crosstalk from one corrupts the signal in the other. Crosstalk is minimized by careful electrical and thermal design of the IC. Figure 1 plots crosstalk for the case where the output of unit A is slowly varying between −10 V and +10 V with a 2-kΩ load. The crossplot shows unit A's output as the horizontal axis; the vertical axis is the change in the input offset voltage of unit B. The crosstalk-induced change (due to heating of the die) is less than 4 μV; for loads >2 kΩ, the change is even less. Channel separation is typically 135 dB.

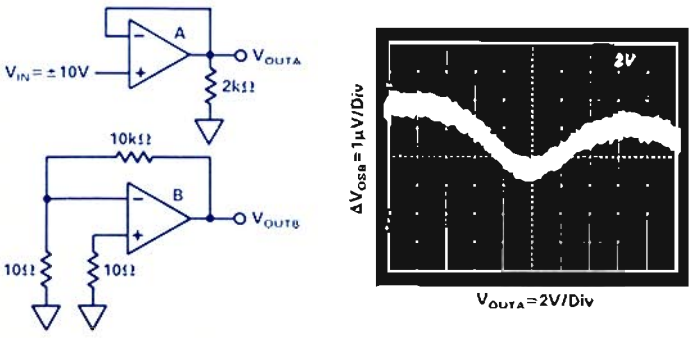
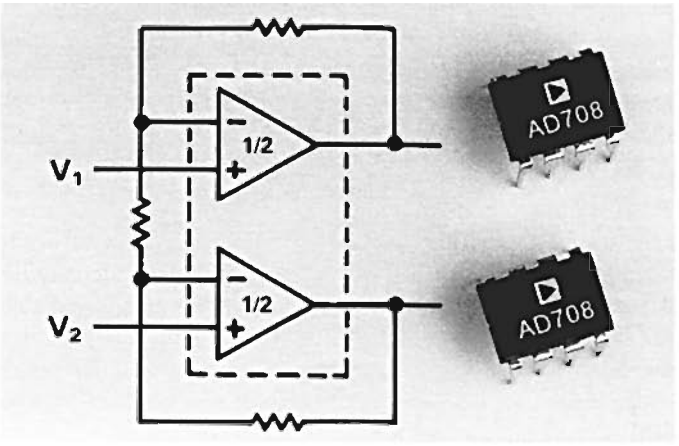


Figure 1. Crosstalk crossplot for 2-kΩ load. Unit A output voltage (horizontal—2 V/div) vs. unit B offset change (vertical—1 μV/div).

[1] Use the reply card for technical data.



Bridge Signal-Conditioning Circuit: Figure 2 shows a circuit for accurately and inexpensively implementing a bridge configuration. One half of the AD708 establishes a reference voltage for the bottom of the bridge, while the other half conditions and scales the bridge output. The transfer function of this circuit is $V_{OUT}/V_{REF} = [R_G/R][\Delta R/(R + \Delta R)]$. Any offset or drift in the first device would ordinarily pass through directly to the output, amplified by R_G/R. However, the close matching means that the output conditioning op amp's offset and drift are nearly identical to those of the reference-setting op amp, so most of the error is cancelled.

The AD708 is available in plastic mini-DIP, hermetic Cerdip, and TO-99 metal-can packages, and for commercial (0° to +70° C), industrial (−40° to +85° C), and military (−55° to + 125° C) temperature ranges; MIL-STD-883B processing is also available. Premium (SQ) prices begin at $11.50 (100s). Somewhat lower-performance versions are available at prices down to $2.95 (JN).

The AD708 was designed by Moshe Gerstenhaber at Analog Devices Semiconductor, Wilmington, MA.

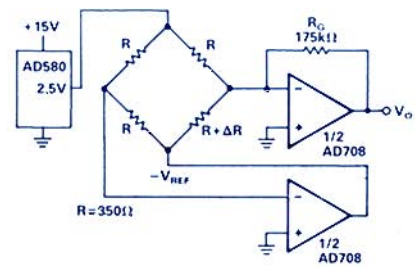


Figure 2. Bridge signal-conditioning circuit.

LOW POWER 16-BIT DAC FOR HIGH ACCURACY AT LOW COST

AD1145: +5V Supply (2.5 mW), 8/16-Bit Bus, Data Readback Features 6-μs Settling, ±0.001% DNL, Accuracy to ±0.003%

In the AD1145 Digital-to-Analog Converter,[1] proprietary two-chip construction provides 16-bit performance in an IC package size (44-pin grid array or PLCC). The double-buffered digital input is designed for easy interfacing to 8- and 16-bit buses, as well as serial data; internal application resistors, used with an external amplifier, supply outputs of 0 to +5 V, 0 to +10 V, 0 to −5 V, 0 to −10 V, and bipolar ±5- & ±10-V ranges. Serial data readback capability, a necessity in critical applications, such as machine tools, robotics, and ATE, is inherent.

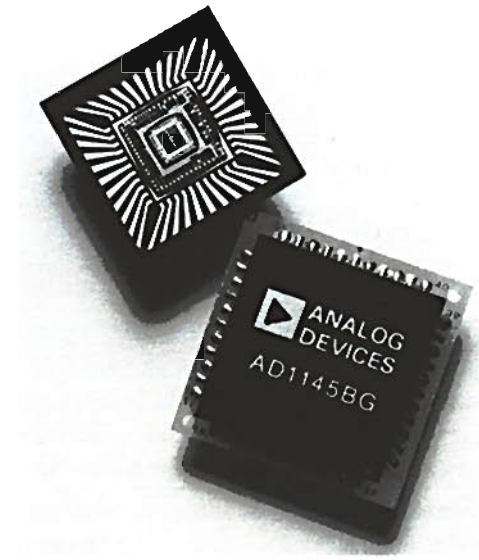
Performance: The AD1145B's differential nonlinearity (DNL) is ±3/4 LSB max (±0.001%), with integral nonlinearity (INL) of ±1 LSB (±0.0015%). Relative-accuracy error is less than ±0.003%, with initial offset below ±1/4 LSB. Stability with temperature and time are excellent: offset and gain tempcos are ±0.1 ppm/°C, with ±0.1 ppm/1,000 hr long-term stability.

Analog output appears as an 18-pF, 5-kΩ voltage source, which settles to 1/2 LSB in 6 μs for a 5-V step output. THD is less than −98 dB, and noise is also low: 5 μV peak-to-peak (p-p) from 0.1 to 10 Hz, and 50 μV p-p to 100 kHz.

Operation: Data is loaded into the AD1145 as a single 16-bit word, two 8-bit bytes, or a serial bit stream. The serial mode is especially useful where data lines are costly or unavailable, or where the AD1145 must be isolated from the rest of the circuitry. Optoisolators for control lines and the serial-data input and read-back lines, plus a DC/DC converter, isolate the analog output.

The digital coding is straight binary for unipolar output ranges, and either offset binary or twos complement for bipolar output. Internal double-buffered latches allow several AD1145s to be updated simultaneously. The latches can also be made transparent if necessary. The serial readback can be transformed to parallel with two octal D-type latch ICs (Figure 1). The DAC output is automatically reset to zero on power up (00 . . . 000 in unipolar mode, 10 . . . 000 in bipolar mode), or by the hardware Clear line.

The nominal output range of the DAC is 0 to +5 V. To avoid attenuation due to loading, the high-impedance output should be buffered (Figure 2). Considerations for the buffer op amp include offset voltage and drift, bias current and drift, slew rate, and settling time. A high-quality BiFET amplifier, like the AD711, is recommended. Similarly, the voltage reference output impedance



and recovery time are critical; the AD586 is a good 5-volt choice.

The internal application resistors facilitate setting the other standard ranges, and custom ranges can be set with only two external resistors. The reference need not be fixed, either; as a two-quadrant multiplying DAC, the AD1145 can handle V_{REF} between 3 and 6 V, as long as V_{REF} is within +0.6/-0.3 V of V_{DD}. They may be tied together if V_{REF} is well buffered.

Packaging: The AD1145 is housed in a compact, 44-pad leadless chip carrier made of glass epoxy (the same as circuit boards). Besides providing excellent dimensional tolerance and planarity, the temperature coefficient of this package inherently matches circuit boards'. This minimizes stress, maximizes reliablity, and makes this package especially suitable for surface mounting. A pin-grid array package is also available for conventional boards.

The AD1145 is specified for −40 to +100°C operation, with +5-V power consumption of 2.5 mW (CMOS-driven inputs) or 17.5 mW (TTL-driven inputs). A/B grades have ±1 LSB/±3/4-LSB differential nonlinearity. Prices (100s) start at $29.50/$39 (A/B).

The AD1145 was designed by Scott Wayne, of the Industrial Products Division of Analog Devices, Norwood, Massachusetts.

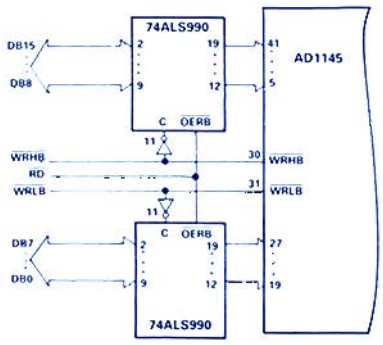


Figure 1. Serial to parallel readback.

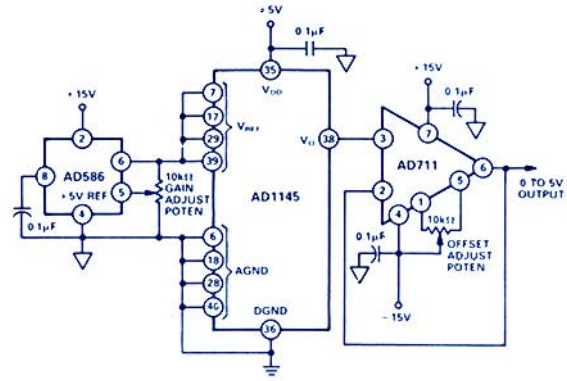


Figure 2. Configuration for buffered 0 to +5 V output.

[1]Use the reply card for technical data.

ISOLATED mV/TC CONDITIONER HAS HIGH GAIN, LOW DRIFT

1B51 Has Gains from 2 to 1,000, Input Offset Tempco of ±0.1 μV/°C
1,500-V RMS Isolation, 240-V RMS Input Protection in a Small DIP

The 1B51 Isolated Signal Conditioner[1] provides the analog interface for low-level signals from thermocouples and millivolt-level sources, featuring high accuracy and low input offset temperature coefficient (±0.1 μV/°C). Housed in a small circuit-board-mountable DIP (1.0" × 2.1" × 0.35"), it is a functionally complete solution for introducing such signals into an analog control system, or a digitizing front end, at standard voltage levels. Requiring a ±15 V supply, it provides up to 2 mA of isolated power, at ±6.2 V, for auxiliary front-end functions, such as zero suppression and open-input detection.

The 1B51 provides a low cost front-end solution for electrically harsh enviroments with high common-mode noise, systems with multiple-channel thermocouple (or similar low-level) inputs, and any application that needs input-to-output *and* channel-to-channel isolation. The 1,500-V rms isolation and 240-V rms input protection, combined with 3-Hz low-pass filtering are well suited for industrial measurement needs. Common-mode rejection is 160 dB at 60 Hz, at a gain of 1,000 V/V; gain tempco is ±50 ppm/°C, and nonlinearity is ±0.035%.

The circuitry has three sections (Figure 1): a chopper-stabilized input amplifier, isolation transformers, and an output demodulator/filter. Power applied to the output side supplies both that side and the isolated side. A 25-kHz power oscillator provides both the timing signal for the demodulator and ac power for the input side. Transformer T2's secondary voltage is rectified and filtered to develop the input-side supply voltages.

A pair of external resistors (R_G and R_{FB} in Figure 2) set the gain of the input stage. The absolute accuracy and ratiometric temperature coefficients must be taken into account when calculating the initial gain accuracy. A trimming potentiometer can be used to correct for initial errors.

The input signal is amplitude modulated onto a 25-kHz carrier and passed through transformer T1, where a synchronous demodulator recreates the baseband input signal on the output side. Passive input filtering on the front end provides normal-mode rejection, and an active two-pole filter on the output is used to filter out the carrier and provide additional normal-mode rejection—for a total of 60 dB at 60 Hz.

Zero Suppression: The 1B51 is a differential-input device, and true input-referred zero suppression is readily achieved. This is useful for eliminating tare weights or large temperature offsets while maintaining high gain and effective resolution for the region of interest; this compares very favorably with keeping the offsets and being restricted to low gain to prevent overranging. A voltage reference, powered by the input-side power supply, is applied to the LO input terminal. The input voltage for which the desired output is zero is set by resistors R1 and R2, acting as a voltage divider. A temperature-stable reference is required, since any drift in this suppression voltage looks like offset drift.

Open Input Detection: Adding a single 220-MΩ resistor between the input HI pin and either supply rail causes the input to go to full scale positive (or negative, depending on which rail is connected to the resistor). This feature is useful for any input which may fail by opening, but it is especially necessary for identifying critical thermocouples (or their long lead wires) which can fail or be accidentally cut in use. The small (<0.1-μA) leakage associated with the resistor is usually tolerable.

The 1B51 is potted in a plastic package. Though specified for –25° to +85°C, it operates to –40°C. Pricing is $52 (100s).

The 1B51 was designed by Howard Samuels, of the Industrial Products Division of Analog Devices, Norwood, Massachusetts.

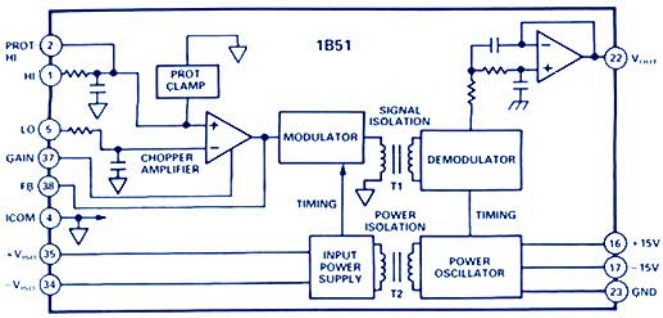


Figure 1. Functional Block Diagram.

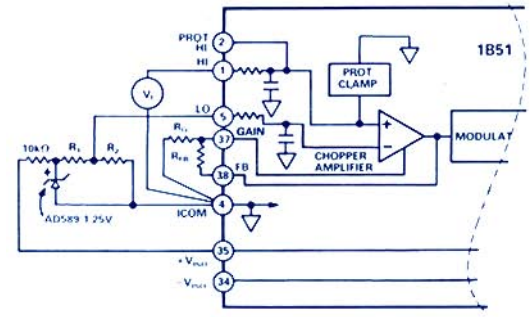


Figure 2. Setting input gain and zero supression.

[1]Use the reply card for technical data.

4 SAMPLE/HOLDS ON A CHIP WITH 1-μs MAX ACQUISITION TIME

AD684 Is Complete, Includes Hold Capacitors, Independent Control Lines

Specs Include 500-ns Hold Settling, 200-ps max Aperture Jitter

by Brad Fluke and Peter Predella

The AD684* is a monolithic quad sample-and-hold (s/h) amplifier designed for use with high-speed a/d converters in multichannel data-acquisition systems. Working at rates approaching 100 ksps with true 12-bit performance, each channel of the AD684 samples with the speed and accuracy that high-performance systems require. All grades of the device have guaranteed maximum acquisition time of 0.6 μs to within 0.1% of full-scale and 1 μs to 0.01% for a 10-V step. The AD684's maximum nonlinearity of ±0.003% offers considerable improvements over earlier quad sample/holds.

Manufactured on a BiMOS process, the AD684 has four sampling channels, each with an on-chip Hold capacitor. Each channel is controlled by independent Hold commands and is capable of sourcing 5 mA with a 10-V p-p input voltage swing (±5V)—well-suited for either sequential, random, or simultaneous sampling. Inputs and outputs are treated as single-ended signals referred to common. A proprietary error-correcting architecture quickly compensates for hold-mode errors and ensures accuracy and repeatability over temperature.

Advantages Over Single SHAs: Besides the obvious savings of space and power, the AD684 offers up to 3 times the speed, with less total harmonic distortion and higher signal-to-noise ratio than are found in many single s/h amplifiers. Equally important is an improvement in channel-to-channel matching characteristics. Here's an example of where it's useful: When single s/h amplifiers are used in a multi-channel simultaneous sampling design, one must first determine the aperture-delay mismatch from manufacturers' data sheets and, depending upon the desired accuracy, compensate for each by adding digital delays to the sampling clock—not easily done in a production environment.

Simplify with a Quad: Because close interchannel matching of timing and accuracy specifications is inherent in the monolithic AD684's construction, it represents a simpler and more accurate

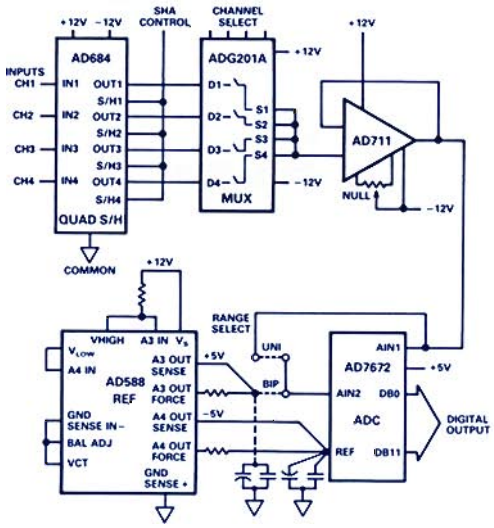
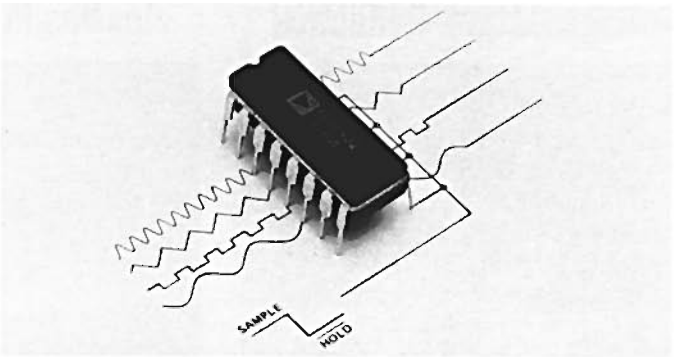


Figure 1. Four-channel data-acquisition system, using the AD684 and the 12-bit AD7672 a/d converter.

*Use the reply card for technical data.



solution without external compensation between channels; the entire aperture error budget is included in the "interchannel aperture offset" specification: 300ps, maximum, *guaranteed*.

Aperture jitter, often refered to as "aperture uncertainty", is the result of unwanted noise, often emanating from power-line frequency, or poor grounding techniques. In either case, the result is a phase-modulated Hold command. Keeping the aperture jitter low will, in effect, increase the maximum frequency that can be handled by the s/h amplifier. The formula for calculating maximum frequency is:

$$f_{MAX} = \frac{1}{\pi t_a 2^{N+1}}$$

where t_a is the rms aperture jitter, and N is the number of bits of desired resolution (to 1/2 LSB). For t_a = 200 ps and N = 12, the maximum operating frequency of the s/h amplifier (per channel) is 194 kHz.

Figure 1 shows a high-speed simultaneous data-acquisition circuit where a single command puts all four channels of the AD684 into the hold mode. In less than 500 ns, the s/h amplifiers settle. The channel-select logic then connects each of the four input channels in turn to the AD7672 12-bit, 3-μs analog-to-digital converter (See *Analog Dialogue* 22-1). Using a 300-ns switch and an input buffer amplifier (AD711), requiring just 1 μs to settle to within 0.01%, the rate at which each channel can be updated is calculated as 55 ksps. Since the s/h amplifier's maximum interchannel aperture offset is 300ps, true 12-bit performance is possible at input frequencies up to 129 kHz, well beyond the 55-kHz maximum per-channel throughput rate.

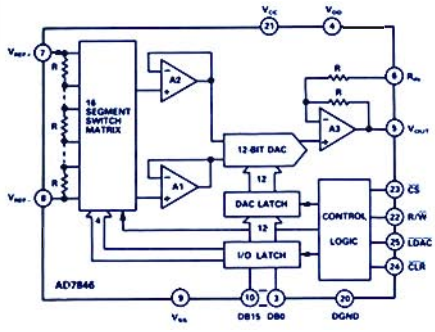
For the best performance, it is important to drive the inputs from a low-impedance signal source; this will enhance the sampling accuracy by minimizing analog and digital crosstalk. A buffer amplifier is recommended for applications having a high signal source impedance. A low output impedance of 0.5 Ω makes the AD684 well-suited for direct interface to ADCs.

The AD684 operates from ±12-V supplies, with 530 mW of power consumption. Housed in a 16-pin skinny (0.3") DIP, it is offered in three temperature ranges: 0 to 70°C (J), –40 to +85°C (A), and –55 to +125°C (S). Prices begin at $23.50 (100s).

The AD684 was designed by Christopher O'Connor and Gerald A. Miller, of Analog Devices Semiconductor, Wilmington, MA.

TRUE 16-BIT IC DAC

AD7846: Fully Monotonic Voltage Output, Readback



The AD7846[1], a true-16-bit voltage-output digital-to-analog converter, is complete on a single monolithic chip with: double-buffered digital inputs, a 16-bit segment-switching 2-quadrant multiplying DAC, and an output buffer amplifier.

Its guaranteed 16-bit monotonicity over temperature for all grades makes the AD7846 ideal for closed-loop applications, such as industrial control and robotics. Constructed in Analog Devices' LC^{2}MOS process, the device dissipates only 100 mW. The ability to read back the DAC register contents (which represent the actual analog output) minimizes software routines when the AD7846 is used in ATE systems.

The AD7846 has a pair of differential reference inputs, V_{REF+} and V_{REF-}, and an on-chip output amplifier with 7 µs max settling time to 0.006% FSR (9 µs max to 0.003%); they can be configured for unipolar—(0 to +5 V or +10 V)—or bipolar output ranges (±5 V or ±10 V). The output amplifier is configured as a track-hold "deglitcher" to greatly reduce glitch amplitude and width (0.4 mV-µs typical major-carry glitch impulse).

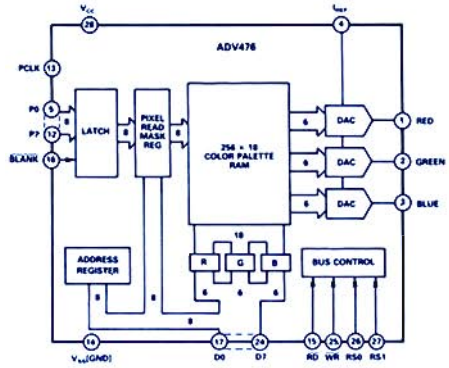
Two accuracy grades are available for industrial and commercial applications (J,K for 0 to +70°C and A,B for −25 to +85°C), with an S (/883B) grade for the −55 to +125°C military temperature range. The K and B versions guarantee relative accuracy error <±2 LSB max for bipolar output at +25°C (±4 LSB over temperature), while J/A/S offer ±8 LSB max over temperature. Packaging is in plastic and ceramic DIPs and LCCCs. Prices (100s) start at $19.

[1]Use the reply card for technical data.

PS/2-COMPATIBLE COLOR PALETTE RAM-DAC

ADV476: Pin- and Function-Compatible with IMSG171 Has Pixel Read Mask Register for Rapid MPU Access

The ADV476[1] is a complete analog-output RAM-DAC on a single monolithic chip. Besides a triplet of 6-bit video d/a converters, it contains a 256 × 18 lookup table and a pixel mask register. The ADV476 is capable of displaying simultaneously up to 256 colors—from a total color palette of 262,144 addressable colors. It is well suited for high-resolution color graphics, image processing, and CAE/CAD applications.



By writing to the pixel read-mask register, the system CPU can access different sections of the ADV476's lookup table and alter the displayed colors without updating the lookup table. Video outputs are directly compatible with RS-343 and RS-170 communications without external buffering.

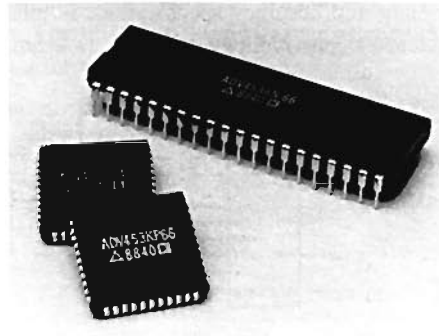
Features include: full compatibility with VGA and Personal System/2 color graphics; guaranteed monotonic behavior, with guaranteed ±1-LSB maximum integral and differential nonlinearity; low glitch impulse, 75 pV-s; blanking on all three channels; and asynchronous access to all internal registers.

The CMOS device, housed in a 0.6"-wide, 28-pin plastic DIP, operates from 0 to +70°C. Using a +5-V supply, it dissipates a low 800 mW maximum. The ADV476 is available for 35, 50, and 66-MHz clock rates. Pricing (100s) is $16, $17, and $20, respectively.

256 × 24 COLOR PALETTE IC RAM-DAC

8-Bit ADV453 Is Fully Compatible with Bt453 3 × 24 Overlay Palette for Cursors, Pulldown Menus, Grids

The ADV453[1] is a complete analog video-output RAM-DAC on a single monolithic CMOS chip; it is specifically designed for high-resolution color graphics systems. It contains triple 8-bit video d/a converters, a user-programmable 256 × 24 RAM color lookup table, a 3 × 24 color overlay palette, and CRT drive circuitry.



Compatible with a wide variety of high-resolution color-graphics systems—including IBM's VGA and Apple's Macintosh II—it provides video-formatted signals for computer, instrumentation, and image-processing applications.

The triplet of DACs give the user access to 16.8 million colors, while the RAM color lookup table and the overlay palette reduce processing requirements by respectively storing 256- and 3-member subsets of the color universe, encoded as 8- and 2-bit words (instead of the raw 24 bits that drive the DACs). The stored colors can be updated during the beam retrace. The 2-bit overlay color, for grids, cursors, and menus, takes priority over the 8-bit data.

It is guaranteed monotonic, with integral and differential nonlinearities less than ±1 LSB and glitch impulse <50 pV-s. Its outputs are compatible with RS-343A and RS-170. Packaged in a 40-pin DIP or 44-pin PLCC, it dissipates 1 W. It is available for 66-MHz and 40-MHz clock rates. Prices (100s) are $45 and $35, respectively.

ANALOG & DIGITAL I/O BOARDS FOR STD BUS

RTI-1265/66/67: Compatible with Both IBM PC Application Software and ADI Signal-Conditioning Panels

The RTI®-1265/66/67[1] cards are a series of modular analog and digital I/O subsystems for the STD bus. The 12-bit RTI-1265 analog input card handles up to 64 analog inputs; the RTI-1266 I/O card adds 16 analog outputs; the RTI-1267 handles 24 digital I/O points with three 8-bit ports.

They make possible economical low-card-count multi-channel STD bus systems with electrical isolation, signal conditioning and sophisticated processing, because of at least four beneficial characteristics:

- They are compatible with Analog Devices STB signal-conditioning panels (below).
- They are software-compatible with IBM PC applications software written for the RTI-820 PC plug-in card[1] (see *Analog Dialogue* 21-1); this facilitates use of such packages as The FIX,[1] LT/Control,[1] and ASYST[1] in STD-bus systems containing PC-compatible processors.

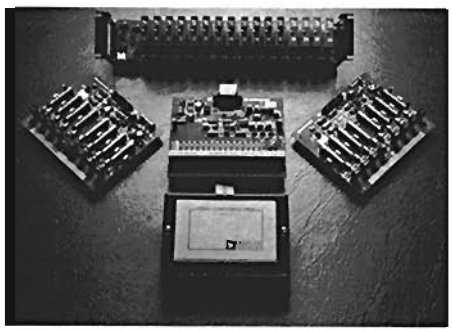
- They have high channel density; for example, the RTI-1265 handles a maximum of 64 analog inputs with acquisition rates to 19 kHz.
- They are low in cost. The RTI-1265/66/77 are priced at $425/$550/$225.

CONDITIONING FOR DATA ACQUISITION

Isolated STB-TCI and STB-HLI Panels Work with RTI-820 (PCs), RTI-1265/66/67 (STD bus), and μMAC-6000

The STB-TCI and STB-HLI[1] are rack-mountable analog expansion panels for use with the RTI®-820[1] (data-acquisition card for PCs), the RTI-1265/66/67 (data-acquisition cards for PC-compatible STD-bus processors), and the μMAC-6000[1] modular I/O processor board. These panels are the newest members of an existing series of expansion panels.

Both panels provide eight channels of isolated signal conditioning: the STB-TCI is designed for thermocouples and millivolt-level inputs, and the STB-HLI is for high-level (±5V to ±10-V full-scale) inputs. Up to four panels can be connected, and the panels (including the earlier 5B02, STB-TC, and STB-HL02)[1] may be used interchangeably. Signals from the field are connected to the panels via quick-disconnect screw terminals, making installation and



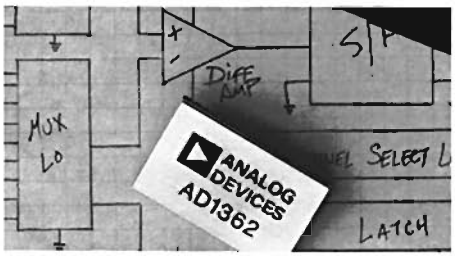
field replacement easy.

Each input has 750 V rms (±1,000 V peak) of channel-to-channel and input-to-output isolation. Gain for each channel is individually selectable, and the factory-configured gains are trimmed to ±0.05%. Gain-trim potentiometers are available for improving accuracy for any gain value. The only power required is at computer-compatible +5 V. Prices for STB-TCI/HLI are $795/$695.

[1]Use the reply card for technical data.

DAS FRONT END

AD1362: Complete Hybrid: MUX, Diff-Amp, S/H, Buffer



The AD1362[1] provides a complete, calibrated solution to data-acquisition system design. It combines a fully protected input multiplexer, high-input-impedance differential amplifier, sample/hold amplifier, output buffer amplifier, and control logic in a 32-pin ceramic dual in-line package.

Users can take advantage of a mode control to select either 16 single-ended or 8 differential input channels—or a mixture of both modes—and need only supply power and channel-select instructions to have a complete front end for analog signal acquisition. The DAS connects directly to popular 10- and 12-bit a/d converters, such as the Analog Devices AD578, AD574, and AD7572.[1]

Accurate 12-bit performance (over temperature) is ensured by the AD1362's low error specifications (all maximum): ±0.01% nonlinearity, ±0.02% gain error, and ±4-mV offset error. Common-mode rejection for differential inputs is typically 80 dB; acquisition time for a ±10-V input signal to within ±0.01% is 10 μs. The s/h amplifier's respective maximum aperture delay and uncertainty are 200 ns and 500 ps.

The AD1362 is pin- and function-compatible with the Analog Devices AD362 (*Analog Dialogue* 14-2), with 20% less power consumption, less than half the noise and offset error, and lower cost. Its self-contained Hold capacitor results in improved performance and further cost savings.

Two temperature ranges are available: the AD1362KD is specified for the 0 to +70°C range and the AD1362SD for the −55 to +125°C range; an /883B version of the latter is also available. Power supply requirements are ±15 V and +5 V, with 800-mW maximum power consumption. Prices in 100s are $144.25, $265.75, and $372.

Ask the Applications Engineer—2

by James Bryant

WHEN IT COMES TO TRIMMING . . .

Q: *I need some advice about trimming offsets and gains.*

A. Don't!—unless you must. Good alternatives include (a) using headache-free devices, components, and circuits that meet the specs without trimming; (b) taking advantage of digital technology in system applications to make trim corrections in software. Savings provided on occasion by trim potentiometers, in conjunction with loosely spec'd devices, can turn out to be illusory when you consider the effects of circuit design, temperature, vibration, and life on performance and stability—as well as additional paperwork and complexity trimming entails.

Q: *Nevertheless, how do I trim the offset and gain errors in analog circuitry?*

A: In the correct order and with the correct inputs. If you consider the transfer characteristic of the circuit being trimmed the method to use is generally straightforward.

The simplified ideal transfer characteristic of a linear analog circuit (such as an amplifier, ADC or DAC) is given by the equation:

$$OP = K \times IP \qquad (1)$$

where OP is output, IP is input, and K is a scale factor (Note that this simplification hides an enormous number of issues: quantization error in an ADC; dimensionality of K if the input and output are in different forms [e.g. voltage in / current out]; intentional offsets; and many others.)

In a real (non-ideal) circuit, offset and gain errors, OS (referred to the input) and ΔK, respectively, also appear in the equation, which becomes:

$$OP = (K + \Delta K) \times (IP + OS) \qquad (2)$$

$$OP = (K \times IP) + [(K \times OS) + (\Delta K \times IP) + (\Delta K \times OS)] \qquad (3)$$

Equations (2) and (3) are incomplete in that they assume only one offset—at the input—but this is the most-common case. Systems with separate input and output offsets will be considered later.

From (3) we see that it not possible to trim gain directly when an unknown offset is present. Offset must be trimmed first. With IP set at 0, the offset trim is adjusted until OP is also 0. Gain may then be trimmed: with an input near to full scale (FS), the gain trim is adjusted to make the output obey equation (1).

Q: *But what about bipolar ADCs and DACs?*

A: Many ADCs and DACs may be switched between unipolar and bipolar operation; such devices, wherever possible, should have their offset and gain trimmed in the unipolar mode. Where it is not possible, or where the converter is to operate only in the bipolar mode, other considerations apply.

A bipolar converter may be considered as a unipolar converter with a large offset (to be precise, an offset of 1 MSB—one-half of full-scale range). Depending on the architecture used, this bipolar offset (BOS) may or may not be affected by the gain trim. If it is so affected, equation (1) becomes:

$$OP = K \times (IP - BOS) \qquad (4)$$

In this case offset is trimmed at analog zero, after which gain is trimmed near FS—positive or negative, but usually positive. This is normally the method used for DACs where the bipolar offset is within the DAC.

If the bipolar offset is not affected by the gain trim:

$$OP = K \times IP - BOS \qquad (5)$$

Here offset is trimmed at FS negative and gain is trimmed at (or very near to—see below) FS positive. This method is used for most ADCs and for DACs where bipolar offset is obtained by the use of op amps and resistors external to the DAC.

Naturally, the method suggested on the data sheet should always be followed, but where a data sheet is unobtainable, in general, offset should be trimmed at analog zero for DACs and FS negative for ADCs—and near FS positive for both.

Q: *Why do you keep saying "near" to full scale?*

A: Amplifiers and DACs may be trimmed at zero and full scale. In the case of a DAC, all-1's—the largest digital input possible—should produce an output 1 LSB below "full scale," where "full scale" is considered as some constant times the reference; this follows since the output of a DAC is the normalized product of the reference and the digital input.

ADCs are not trimmed at zero and FS. The output of an ideal ADC is quantized, and the first output transition (from 00 . . . 00 to 00 . . . 01) takes place 1/2 LSB above the nominal value of all 0's. Thereafter transitions take place every 1-LSB increase in analog input until the final transition takes place 1 1/2 LSB below FS. A non-ideal ADC is trimmed by setting its input to the nominal value of a desired transition and then adjusting until the ADC output flickers between the two values equally.

The offset of an ADC is therefore trimmed with an input corresponding to the first transition (i.e., 1/2 LSB above zero or above FS negative—which is "near" zero or "near" FS negative); and the gain is then trimmed at the last transition (i.e. 1 1/2 LSB below FS positive—which is "near" FS positive). This procedure results in an interaction between the gain and offset errors during offset trim but it should be too slight to be significant.

Q: *Are there any other anomalies resulting in a need to trim "near", rather than at full scale?*

A: Synchronous voltage-to-frequency converters (SVFCs) are liable to injection locking phenomena when their output frequency is harmonically related to their clock frequency, i.e., when their output is very close to 1/2, 1/3 or 1/4 of clock frequency. FS for an SVFC is 1/2 clock frequency. The presence of a trim tool can exacerbate the problem. It is therefore advisable to trim the gain of an SVFC at around 95% of FS.

Q: *What about circuits requiring both "input" and "output" offset trim?*

A: Circuits such as instrumentation and isolation amplifiers often have two stages of dc gain, and the gain of the input stages can be variable. Thus a two stage amplifier, with an input offset, *IOS*, an output offset, *OOS*, a first stage gain of *K*, and a unity-gain output stage, has (for zero input) an output, *OP*, of:

$$OP = OOS + K \times IOS \qquad (6)$$

From (6) it is evident that if the gain is constant we need only adjust either *IOS* or *OOS* to null the total offset (although if the input uses a long-tailed pair of bipolar transistors we will get a better offset temperature coefficient if we trim both—for FET long-tailed pairs this is not necessarily the case). If the first stage gain is to be varied, both offsets must be trimmed.

This is done by an iterative procedure. With zero input, and gain set to maximum, the input offset is adjusted until the output is also zero. The gain is then reduced to its minimum value and the output offset adjusted until the output is zero again. The two steps are repeated until no further adjustment is necessary. Gain trimming should not be done until both *IOS* and *OOS* are nulled; the actual values of the high and low gains used in offset trim are unimportant.

Q: *What circuitry should I use for gain and offset trims?*

A: Many amplifiers (and a few converters) have terminals for trimming gain and offset. Many more do not.

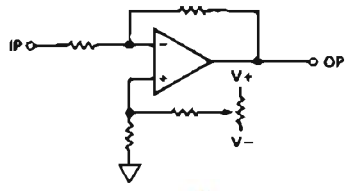
Offset trim is normally performed with a potentiometer connected between two assigned terminals, and its wiper is connected (sometimes via a resistor) to one of the supplies. The correct connections and component values will be given on the device data sheet. One of the commonest differences between op-amps is the value of offset correction potentiometer and which supply it should be connected to.

Where separate terminals are not provided for offset trim, an offset-adjusting constant can usually be added to the input signal. Two basic possibilities are shown in Figures 1a and 1b. Where the correction is being made to a system where a differential input op amp is used as an inverter (the commonest case) the method of 1a is best to correct for device offsets—but not system offsets. In the single-ended connection, method 1b will work for system offsets but should be avoided where possible for small device offsets, because it often requires a very large value of summing resistance, compared to the signal-input resistances, in order to (i) avoid loading the summing point excessively, (ii) scale the correction voltage properly and produce enough attenuation to minimize the effects of differential supply-voltage drifts. It is often helpful to use resistances between the supplies and the potentiometer to increase trim resolution and reduce dissipation.

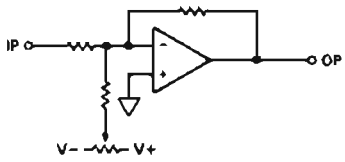
Where gain trim is provided for in a circuit, it will generally consist of a variable resistor. Details of its value and connection will appear on the data sheet of the device. Where gain trim is not required, this resistor may be replaced by a fixed resistor having half the resistance of the maximum value of the recommended trim potentiometer.

Where gain trim is not provided it is not always achievable externally without an additional variable-gain stage. For example, consider a DAC using a ladder network. If the ladder network is used in the current mode (Figure 2a), the input impedance at the reference terminal does not vary with digital code, and the gain of the DAC may be trimmed with a small variable resistor in series with either the reference input or the feedback resistor. However, if the DAC is used in the voltage mode (Fig 2b), then the reference input impedance is code dependent, and gain may only be trimmed by varying the reference voltage—which is not always possible—or the gain of the buffer amplifier.

The possibility of trimming gain in circuits not furnished with gain-trim circuitry, therefore, will depend on individual cases; each must be assessed on its own merits. ◘

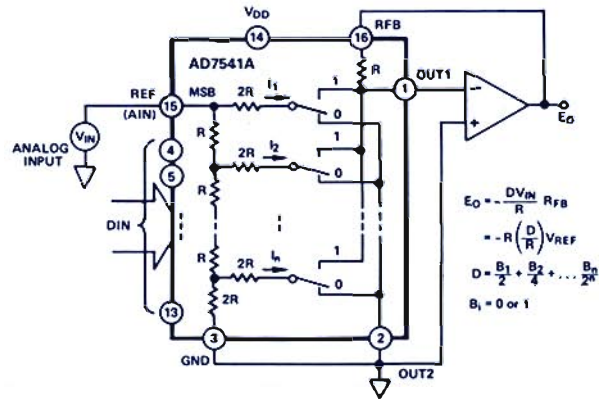


a. Voltage applied to non-inverting input.

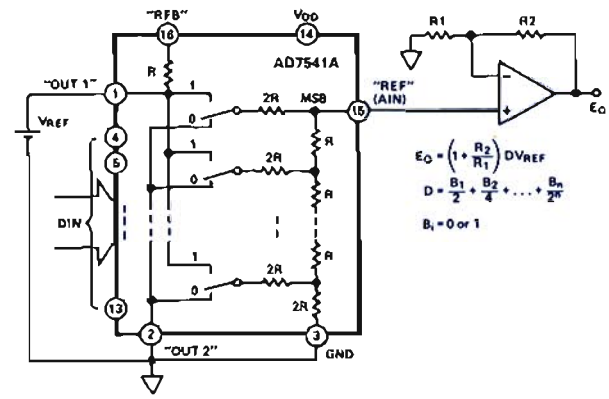


b. Current summed at inverting input.

Figure 1. Two connections for offset adjustment.



a. CMOS DAC connected for current steering. Input impedance is constant.



b. The same DAC connected for voltage output.

Figure 2. Comparing basic DAC circuits.

Worth Reading

NEW DSP HANDBOOK

ADSP-2100 Family Applications Handbook, Volume 2, is now in print, and available free upon letterhead request. It has 240 pages of new information on applications of the ADSP-2100A DSP microprocessor and the ADSP-2101 and ADSP-2102 single-chip microcomputers. Building on the foundation provided by *Volume 1*, which presents information on fixed-point arithmetic, floating-point arithmetic, function approximation, fixed-coefficient digital filters, fast Fourier transforms, adaptive filters, image processing, linear predictive speech coding, and high-speed modem algorithms, *Volume 2* presents a compilation of routines for a variety of advanced digital signal-processing applications; it covers the following topics:

Graphics: Presents a graphics subsystem based on the ADSP-2100, complete with support circuitry and all software routines for rotation, translation, scaling, and clipping.

Multirate Digital Filters: Describes filters which change the sampling rate of digitally represented signals.

Pulse Code Modulation: Presents an ADSP-2100 implementation of the CCITT standard PCM algorithm. Encoding and decoding are shown, and both μ-law and A-law companding methods are used.

Adaptive Differential Pulse-Code Modulation: Presents an ADSP-2100 implementation of the CCITT standard ADPCM algorithm. A non-standard program that is suitable for some applications is also described.

Dual Tone Multifrequency: Describes the generation and detection of the CCITT standard DTMF signals.

APPLICATION NOTES[1]

Simple DAC-Based Circuit Implements Constant Linear Velocity (CLV) Motor Speed Control, by John Wynne. This 5-page Application Note introduces an idea for a novel motor-control circuit to effect constant linear-velocity control of a motor. CLV is not a new idea; it is widely used in numerically controlled lathes to achieve a constant cutting speed of the work. Another application for CLV has been in IC production equipment where laser annealing of a wafer is achieved by a slow-speed spiral scan of the wafer by a laser beam. Potential applications are for speeding up data access in optical disc drives and backup tape drives.

Microstepping Drive Circuits for Single Supply Systems, by John Wynne (Analog Devices) and Mark Heisig (Sprague Electric Co.). This 8-page Application Note presents a short tutorial on microstepping two-phase stepper motors. Among the topics discussed are the advantages of using 8-bit (instead of 6-bit) DACs and the benefits of closed-loop control vs. open-loop (with data densities of all types of drives increasing, closed-loop operation is becoming a *must*). Two practical circuits are shown, one using a dual DAC and an ADC, the other using an AD7669 8-bit dual-DAC-plus-ADC-on-a-chip (*Analog Dialogue* 22-2, p. 26) for very economical closed-loop microstepping.

[1]Use the reply card to request your copy.

Overvoltage Protection for the ADG5XXA Multiplexer Series, by Dan Sheehan (Analog Devices BV). Overvoltage protection of multiplexers is a hoary topic, but one which continues to be lively. Protection against voltages exceeding the device supplies can be easily achieved with external resistors, keeping their dissipation off-chip. The 2-page Application Note discusses the issues involved and the protection required in two typical applications.

SERIAL PUBLICATION

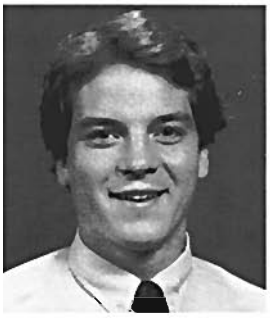
DSPatch—The Digital Signal Processing Applications Newsletter Number Ten is now available.[1] It announces the debut of the ADSP-1402 Program Sequencer for microcode [see also *Analog Dialogue 22-2*, page 28]. Also in the issue: A description of the Sigmet + Lassen Research SP20 Signal/Array Processor; "Why a CD Player is Like a Satellite Modem;" Disk Drive Head Positioning with the ADSP-2101; and the usual departments: "Q & A," "How to Talk Analog;" "Up To Date" briefs; and a listing of Available DSP literature.

ORDERING GUIDE[1]

A 12-page updated Ordering Guide for the μMAC-6000 Universal Controller family of products is now available, organized in sections covering each component of the system, such as CPU modules, system backplanes, analog signal-conditioning modules, analog expansion backplanes, solid-state relays, digital backplanes, software support packages, documentation, and cables & accessories. The final section includes an example, illustrating how the Guide is used to configure a system.

MORE AUTHORS *(continued from page 2)*

Bill Schweber (pages 7 and 14) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue*. Besides having his BSEE and MSEE degrees, he has designed microprocessor-based machine controls, been a product marketing engineer, authored numerous technical articles, and written two textbooks. He enjoys bicycling and reading in his spare time.



Brad Fluke (page 17) is a Product Marketing Specialist with the Converter Operating Group at Analog Devices Semiconductor in Wilmington, MA. He joined Analog Devices upon graduation from Rochester Institute of Technology with a BSEE in 1984. He is currently working on his MBA at Boston University. He enjoys skiing, golf and photography.

Peter Predella (page 17) is a Technical Publicity Associate in Marketing Communications at Analog Devices, in Norwood MA. His photo and a biographical sketch appear in *Analog Dialogue*, Volume 22, Number 2, 1988.

James Bryant (page 20) is European Applications Manager for Analog Devices, based in Newbury, England. A biographical sketch and his photo appear in *Analog Dialoque*, Volume 22, Number 2, 1988.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

NEW-PRODUCT CLIPS . . . Use the reply card for technical data . . . An economical 0 to 70°C "J" version of the AD293 isolator is available with initial offset voltage of $(\pm 5 \pm 25/G_{IN})$ mV max and drift of $(\pm 10 \pm 500/G_{IN})$ µV/°C max. Until now, only -25 to +85°C A & B versions were available . . . Laboratory Technologies LT/CONTROL industrial monitoring and process control software is now available from Analog Devices for the RTI®-800, RTI-200, and RTI-1265 series of analog and digital input/output boards for IBM PC and Micro Channel architecture systems. It features acquisition rates up to 2,000 Hz in the normal mode. An upwardly compatible superset of LABTECH NOTEBOOK, it reduces development time when applications migrate from laboratory to pilot plant to plant floor.Both a development system (ask for SW-LTC) and a run-time system (SW-LTC-RTL) are available. Prices: AD293J in 100s: $68; LT/CONTROL (1's) SW-LTC $2,995, SW-LTC-RTL: $1,495.

PRODUCT NEWS . . . The 1740 series of hybrid synchro/resolver-to-digital converters has been redesigned with faster step response and a greatly reduced number of internal components, more than doubling MIL-HDBK-217 reliability, at the sole cost of somewhat higher power dissipation. They are housed in 32-pin solid-sidewall packages (formerly 32-pin platform) and are otherwise identical in function and pinout to the earler version . . . A number of additional products are now available in small-outline integrated circuit (SOIC) packages. The "R"-packaged versions of ADG201A/201HS/202A/211A/212A/221/222/508A/509A switches and MUXes, and of the AD7224/AD7226/7524/7528/7628/7820 converters, have the same specs as the N-packaged J-, K-, or L-grade versions . . . .The AD573 and AD673 ADCs are now available in PLCCs.

CHANGES . . . The DSP Bulletin Board has a new phone number, (617) 461-4258 . . . AD9615 data sheet (C1216-10-7/88): The Life Test/Burn-In Circuit (page 4) has pins 1 and 3 reversed . . . AD652 data sheet: reference output current specification: 10 mA minimum at 25°C and over temperature.

NEWS FROM THE MILITARY FRONT . . . The AD574A is the first (and at present the only) monolithic 12-bit a/d converter to make the QPL. Two grades are available under QPL part numbers: JM38510/14001BXA (a/k/a JAN AD574AUD) and /14002BXA (a/k/a JAN AD574ATD) . . . Three more Analog Devices DAC families have members on Standard Military Drawings: the 8-bit DACPORT AD558SD(&TD)/883B; SMD 5962-8778901(&02)EA, the µP-compatible 12-bit AD567SD/883B (5962-8780101XA) and AD667SD/883B (5962-8865901JA) . . . Four /883B versions of the AD9002 150-MSPS 8-bit monolithic a/d converter are now available: SD & TD in ceramic DIPs and SE & TE in LCCs.

PATENTS RECEIVED . . . 4,717,883 to Carl Browning for Method and Apparatus for Reducing Errors in a Sampling System Untilizing an Error-Sampled Feedback Loop . . . 4,722,910 to John Yasaitis for Partially Self-Aligned Metal Contact Process and Semiconductor Device Fabricated Therewith . . . 4,742,331 to Jeff Barrow and A. Paul Brokaw for Digital-to-Time Converter . . . 4,751,455 to Chuck Ayres for Low-Frequency Noise Measurement System Using Sliding Pole for Fast Settling . . . 4,752,900 to John Wynne for Four-Quadrant Multiplier Using a CMOS D/A Converter.

IN THE LAST ISSUE

Volume 22, Number 2, 1988—32 Pages

ANALOG DEVICES

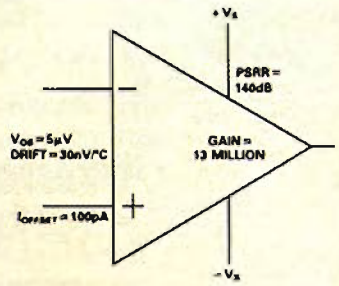
15μV max Offset Voltage Ultralow Drift Op Amp

AD707

FEATURES

Very High dc Precision
- 15μV max Offset Voltage
- 0.1μV/°C max Offset Voltage Drift
- 0.35μV p-p max Voltage Noise (0.1Hz to 10Hz)
- 8V/μV min Open-Loop Gain
- 0.32μV/V max CMRR
- 1μV/V max PSRR
- 1nA max Input Bias Current
- 1nA max Input Offset Current

Dual Version Available: AD708



PRODUCT DESCRIPTION

The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15μV is outstanding for a bipolar op amp, as is the 1.0nA maximum input offset current. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1μV/°C, and offset current drift and input bias current drift are both specified at 25pA/°C maximum.

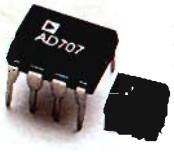
The AD707's open-loop gain is 8V/μV minimum over the full ±10V output range when driving a 1kΩ load. Maximum input voltage noise is 350nV p-p (0.1Hz to 10Hz). CMRR and PSRR are 130dB and 120dB minimum respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline, hermetic cerdip and hermetic TO-99 metal can packages. Chips and Mil Standard/883 parts are also available.

APPLICATION HIGHLIGHTS

1. The AD707's 13V/μV typical open-loop gain and 0.1μV/V typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the OP-07, OP-77 and the LT1001.

HERE'S THE MOST ACCURATE SOURCE OF INFORMATION ON THE WORLD'S MOST ACCURATE BIPOLAR OP AMP.



If your analog applications demand precision performance, then you should demand our new AD707 – the world's best dc precision op amp.

The AD707 is the first bipolar monolithic to offer a maximum offset voltage drift of only 0.1μV/°C, and 15μV maximum offset voltage. These features, combined with its ultralow 0.35μV p-p voltage noise, allow the AD707 to amplify extremely small signals without sacrificing system performance.

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