Conference Program and Exhibitor Listings

Don't miss out on electronic packaging's premier conference!

ECTC

The 2018 IEEE 68th Electronic Components and Technology Conference

May 29 - June 1, 2018

Sheraton San Diego Hotel & Marina
San Diego, California, USA

For more information, visit: www.ectc.net

Program Supported by:

Sponsored by:

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE

WELCOME FROM THE MAYOR OF SAN DIEGO, CALIFORNIA

KEVIN L. FAULCONER

MAYOR

WELCOME TO THE

2018 Electronic Components and Technology Conference

May 29-June 1, 2018

On behalf of the citizens of San Diego, it is my pleasure to welcome you to the 2018 Electronic Components and Technology Conference. We are delighted that you chose to host the Electronic Components and Technology Conference in our beautiful city. This conference is a wonderful opportunity for the best in packaging, components and microelectronic systems science, technology and education to come together and help one another exchange ideas and develop professionally. I am certain you will find San Diego to be a perfect location for your conference and I invite you to explore America's Finest City during your stay here.

Please accept my warmest wishes for an enjoyable event in San Diego.

Best personal regards,

Kevin L. Faulconer
Mayor

WELCOME TO SAN DIEGO FROM THE 68th ECTC GENERAL CHAIR AND PROGRAM CHAIR

On behalf of the Program Committee and Executive Committee, it is our pleasure to welcome you to IEEE's 68th Electronic Components and Technology Conference (ECTC), held at the beautiful Sheraton San Diego Hotel & Marina, San Diego, Calif., USA from May 29 - June 1, 2018. This premier international annual conference, sponsored by the IEEE Electronics Packaging Society (EPS), brings together key stakeholders of the global microelectronic packaging industry, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, material suppliers, research institutions and universities, all under one roof. More than 1,400 people have attended ECTC in each of the last three years.

At the 68th ECTC, more than 370 technical papers are scheduled to be presented in 36 oral sessions and five interactive presentation sessions, including one interactive presentation session featuring papers exclusively by student authors. The oral sessions will feature selected papers on key topics such as fan-out packaging, wafer-level packaging, flip-chip packaging, 3D/TSV technologies, design for RF performance and signal/power integrity, thermal and mechanical modeling, optoelectronics packaging, materials, and reliability. Interactive presentation sessions will showcase papers in a format that encourages more in-depth discussion and interaction with authors about their work. Authors from over 20 countries are expected to present their work at the 68th ECTC, covering ongoing technology development within established disciplines or emerging topics of interest for our industry such as additive manufacturing, heterogeneous integration, and flexible and wearable electronics.

ECTC will also feature eight special sessions with invited industry experts covering several important and emerging topic areas. On Tuesday, May 29 at 10 a.m., W. Hong Yeo and C. S. Premachandran will chair an Emerging Technologies special session covering recent advancements and applications using soft materials. On that same day at 2 p.m., Florian Herrault will chair a session focused on emerging device assembly methods and applications. Tuesday evening sessions start at 7:00 p.m. with a Young Professionals networking panel chaired by Yan Liu. This year's ECTC Panel Session begins at 7:45 p.m. and will be chaired by IEEE EPS President Avi Bar-Cohen and Chris Bailey, where the topic will be IC/Package Co-Design for Heterogeneous Systems.

Boon Chye Ooi, Senior Vice President of Global Operations at Broadcom Inc., will be giving the invited keynote talk on "Packaging Advancement to Enable Artificial Intelligence, Autonomous Cars and Wearables in the Near Future: Cost and Implications to Supply Chains" at the ECTC Luncheon on Wednesday, May 30. This conference also features a Women's Panel and Reception jointly organized by ECTC and ITherm on Wednesday, May 30 at 6:30 p.m. This year, panelists from around the globe will share their perspectives on efforts to enhance the participation of women in engineering, and the panel will be chaired by Cristina Amon and Tanja Braun. On that same day at 7:30 p.m., Kemal Aygun will chair the ECTC Plenary Session titled "Artificial Intelligence and Its Impact on System Design." In this plenary session, experts will address the requirements and challenges for future AI hardware and share their views on how AI will impact system design and manufacturing. On Thursday, May 31 at 8 p.m., the IEEE EPS Seminar "High-Density Packaging Technologies in the Era of Big Data" will be moderated by Yasumitsu Orii and Sheigenori Aoki from the High-Density Substrates & Boards Technical Committee of the IEEE EPS Society.

Supplementing the technical program, ECTC also offers Professional Development Courses (PDCs) and Technology Corner exhibits. Co-located with the IEEE ITherm Conference this year, the 68th ECTC will offer 18 PDCs, organized by the PDC Committee chaired by Kitty Pearsall and Jeffrey Suhling. The PDCs will take place on Tuesday, May 29, and are taught by distinguished experts in their respective fields. The Technology Corner will showcase the latest technologies and products offered by leading companies in the electronic components, materials, packaging and services fields. More than 100 Technology Corner exhibits will be open Wednesday and Thursday starting at 9 a.m. ECTC also offers attendees numerous opportunities for networking and discussion with colleagues during coffee breaks, daily luncheons, and nightly receptions.

Whether you are an engineer, a scientist, a manager, a student, or an executive, ECTC offers something unique for everyone in the microelectronics packaging and components industry. We would like to take this opportunity to thank all our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, and program committee members, as well as all the volunteers who have helped make the 68th ECTC another resounding success. Once again, thank you for being a part of the 68th ECTC.

Sam Karikalan
General Chair
Broadcom Inc.

Chris Bower
Program Chair
X-Celeprint, Inc.

WELCOME FROM ECTC SPONSORING ORGANIZATION

On behalf of the IEEE Electronics Packaging Society, it is my great pleasure and privilege to welcome you to the 68th ECTC.

This conference and the electronic packaging community we serve have grown enormously in size and in impact since the inaugural ECTC held 67 years ago. We expect this year's attendance to reach 1,400 at ECTC, with another 2,500 participating in our other sponsored and co-sponsored conferences and workshops.

I would like to take this opportunity to thank all of you for attending ECTC and our volunteers on the ECTC Executive and Program Committees, members of the Board of Governors, volunteers from the EPS Society, and the ECTC and EPS staff for their commitment and dedication to making the 68th ECTC and its associated activities the premier annual event of the electronic packaging community. We are fortunate to have so many of you actively engaged in this conference, and we are indebted to the large, skilled and enthusiastic team that keeps finding new ways to enhance this flagship conference.

In this first year of my presidency, I am excited about the impact of these technical events and networking activities on the EPS Society, our industry, and our members. It is profoundly gratifying to know that together we are developing the packaging technology for future product generations and driving innovation in the microelectronic industry!

Avram Bar-Cohen
EPS President 2018-2019

CONFERENCE POLICIES AND GUIDELINES

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel "house" phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel's safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
Smoking is NOT permitted in the hotel. Please follow hotel policies and signs regarding this. Smoking is also NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, and / or seminars. Thank you for your consideration and cooperation.

Recording presentations via photos or video is prohibited.

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Conference organizers reserve the right to cancel or change this program without prior notice.

ECTC Luncheon Keynote Speaker

Wednesday, May 30, 2018
12:00 Noon
Grande Ballroom

Packaging Advancement to Enable Artificial Intelligence, Autonomous Cars and Wearables in the Near Future: Cost and Implications to Supply Chains

Boon Chye Ooi
Senior Vice President, Global Operations – Broadcom Inc.

Recent advancements in IC Packaging have played a vital role in enabling semiconductor devices to scale new performance heights and penetrate into new application frontiers. Technologies such as 2.5D/3D packaging and fan-out packaging are in the forefront, leading us into the world of artificial intelligence, autonomous cars and wearables. The packaging industry still has to make these technologies cost competitive and multi-sourced for their ubiquitous deployment, while also keeping up with performance challenges on signal integrity, thermal performance and mechanical reliability. Will IDMs, foundries or OSATs keep up with the design challenges and drive down the cost of supply chain? Boon Chye Ooi, Senior Vice President of Global Operations at Broadcom Inc., will discuss such challenges in the immediate future and issue a call to action by the industry stakeholders.

As a Senior Vice President at Broadcom, Boon Chye Ooi leads the Global Operations organization that is responsible for worldwide manufacturing, including foundry and package engineering, outsourcing, procurement and logistics, planning and quality programs. He has held this position since January 2009. From November 2003 until 2008, Mr. Ooi was the Senior Vice President of Worldwide Operations at Xilinx, where he was responsible for all worldwide plant operations, supply chain processes, and inventory controls, as well as contract electronic component manufacturers. Prior to Xilinx, Mr. Ooi had a long career at Intel, where he served in a variety of management positions.

Heterogeneous Integration Roadmap Workshop

Tuesday, May 29, 2018 • 8:00 a.m. - 5:00 p.m.
Executive Center 1 & 4

Our Industry has reinvented itself through multiple disruptive changes in technologies, products, and markets. With migration of logic, memory and applications to the cloud, AI at the edge, the Internet of Things (IoT) to internet of everything (IOE), smart devices everywhere, and autonomous automotives, the pace of innovation is increasing to meet these challenges.

The Heterogeneous Integration Technology Roadmap (HIR) is sponsored by the IEEE EPS Society, the Electron Devices Society (EDS), and Photonics Society together with SEMI and ASME EPPD. It will address the future directions of heterogeneous integration technologies serving system integration for future markets and products, which are so very crucial to our societies' fields of interest and our industries and academic and research communities. Fresh from the highly successful Heterogeneous Integration Roadmap Symposium on February 22nd hosted by the IEEE EPS Santa Clara Valley Chapter at Santa Clara California, the first Heterogeneous Integration Roadmap will be unveiled at the 2018 ECTC Conference.

The 2018 ECTC Conference is pleased to host the upcoming Heterogeneous Integration Roadmap workshop on Tuesday, May 29, in San Diego, Calif. We invite all the ECTC participants to attend this important working session for our profession and for our industry. The workshop is open to all. Registration is not necessary. There is no fee for attendance.

REGISTRATION, RECEPTIONS AND GENERAL INFORMATION

Registration

ECTC registration will be open at the ECTC Registration Desk located in the Sheraton San Diego Hotel & Marina, Marina Tower, Lobby Level, in the Bayview Foyer.

Monday, May 28, 2018 • 3:00 p.m. – 5:00 p.m.

Tuesday, May 29, 2018 • 6:45 a.m. – 8:15 a.m.*

(AM PD Courses & Special Session Only)*

Tuesday, May 29, 2018 • 8:15 a.m. – 5:00 p.m.

(All conference attendees)

Wednesday, May 30, 2018 • 6:45 a.m. – 4:00 p.m.

Thursday, May 31, 2018 • 7:30 a.m. – 4:00 p.m.

Friday, June 1, 2018 • 7:30 a.m. – 12:00 Noon

New for 2018 – On Tuesday morning from 6:45 a.m. – 7:15 a.m., ECTC will be providing morning refreshments for those registering early! If you get there after 7:15 a.m., you run the risk that they'll be gone.

**The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time on Tuesday, May 29 as registration becomes very congested prior to the start of morning Professional Development Courses.*

Door Registration Fees

Door Registration with Proceedings on USB drive

IEEE Member JOINT Registration (full ECTC + ITHERM conference)	$1125
IEEE Member Full Registration	$835
IEEE Member Speaker / Session Chair	$730
IEEE Member One Day	$550
IEEE Member Speaker One Day	$415
Exhibit Booth Attendant	$0
Non-Member JOINT Registration (full ECTC + ITHERM conference)	$1335
Non-Member Full Registration	$1025
Non-Member Speaker / Session Chair	$730
Non-Member One Day	$550
Non-Member Speaker One Day	$415
Exhibit Booth Attendant	$0
Student	$315
Student Speaker	$315
Exhibits Only	$25

Tuesday Professional Development Courses

IEEE Members and Non-Members

Tuesday AM or PM Course with luncheon	$500
Tuesday All-Day Courses with luncheon	$710
Tuesday Student All-Day Courses with luncheon	$130
Extra Luncheon Tickets for Each Day	$65
Extra Proceedings with Registration	$100

Each student registrant will be offered FREE memberships to the IEEE & EPS for the rest of 2018.

PROFESSIONAL DEVELOPMENT COURSE INSTRUCTORS BREAKFAST
Tuesday, May 29, 2018 • 7:00 a.m. - 8:00 a.m.
Grande Ballroom B

PDC Instructors and Proctors are required to attend a briefing breakfast.

SESSION CHAIRS AND SPEAKERS BREAKFAST
Wednesday, May 30 - Friday, June1, 2018
7:00 a.m. - 8:00 a.m.
Grande Ballroom A

Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows XP and MS Office 2003.

SPEAKER PREP ROOM
Tuesday, May 29 - Friday, June1, 2018
7:00 a.m. - 5:00 p.m.
Marina 3

Speakers should prepare and review their digital presentations within the allotted times above:

(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

MISCELLANEOUS INFORMATION

Hotel Concierge

The Hotel Concierge, located in the hotel lobby, can direct you to various types of entertainment or restaurants, or give suggestions for that special night out. The Concierge can help to make your visit and conference experience a memorable one!

Message Center

Please use the hotel switchboard or the ECTC Registration Desk, located in the Marina Tower, Lobby Level, Bayview Foyer to leave and pickup messages.

The hotel phone number is +1 (619) 291-2900.

Press Room

Press Interviews will be scheduled on an as-requested basis. To coordinate an interview with conference leadership or presenting technical experts, please contact ECTC Publicity Chair:

Eric Perfecto
eric.perfecto@globalfoundries.com
+1 (845) 475-1290

LUNCHEONS

Tuesday, May 29, 2018
12:00 Noon
(Grande Ballroom)

The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, proctors and PDC committee members.

Wednesday, May 30, 2018
12:00 Noon
(Grande Ballroom)

The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Boon Chye Ooi, Senior Vice President - Global Operations for Broadcom Inc.

Thursday, May 31, 2018
12:00 Noon
(Grande Ballroom)

The IEEE Electronics Packaging Society (EPS) will sponsor a luncheon for conference attendees. The EPS awards will be presented.

Friday, June 1, 2018
12:00 Noon
(Grande Ballroom)

The ECTC Program Chair will sponsor a luncheon for conference attendees. You don't want to miss it!

There will be a raffle for attendees.

ECTC Mobile App

ECTC is pleased to announce that a free mobile app is available this year. The app provides schedules for the technical program and PDCs, as well as details on exhibitors, sponsors, and general conference information and venue maps. The app also enables you to set your personal conference schedule so you don't miss important presentations and social functions. Plus, you can rate presentations that ECTC uses to select candidates for best paper awards.

The app is available for iOS and Android devices from the respective app stores by searching "2018 ECTC". Look for additional information in the separate handout included in your ECTC registration packet received at the conference.

2018 ECTC SESSIONS & SEMINARS – Open to all conference attendees

2018 EMERGING TECHNOLOGIES SPECIAL SESSION

Soft Material-Enabled Electronics for Medicine, Healthcare, and Human-Machine Interfaces

Tuesday, May 29, 2018
10:00 a.m. – 11:30 a.m.
Grande Ballroom C

Chairs: W. Hong Yeo - Georgia Institute of Technology and C. S. Premachandran - GLOBALFOUNDRIES

Speakers:
1. Michael McAlpine, University of Minnesota
2. Todd Coleman , University of California, San Diego
3. Aadeel Akhtar, Psyonic
4. Rooz Ghaffari, Epicore Biosystems

2018 ECTC SPECIAL SESSION

Assembly Frontiers – New Methods and Applications

Tuesday, May 29, 2018
2:00 p.m. – 3:30 p.m.
Grande Ballroom C

Chair: Florian Herrault – HRL Laboratories, LLC

Speakers:
1. Jeffrey Demmin, DARPA
2. Hugo Pristauz, Besi Switzerland AG
3. Matthew Meitl, X-Celeprint
4. Doris Tang, PlayNitride
5. Val Marinov, Uniqarta

2018 ECTC PANEL SESSION

I/C Package Co-Design for Heterogeneous Integrated Systems

Tuesday, May 29, 2018
7:45 p.m. – 9:15 p.m.
Harbor Island 1 & 2

Chairs: Avi Bar-Cohen, IEEE EPS President - Raytheon and Chris Bailey – University of Greenwich

Speakers:
1. Harrison Chang, Advanced Semiconductor Engineering, Inc.
2. John Parry, Mentor Graphics
3. Yong Liu, ON Semiconductor
4. Xuejun Fan, Lamar University
5. Madhavan Swaminathan, Georgia Institute of Technology
6. Andrew Kahng, University of California, San Diego

2018 ECTC/ITHERM WOMEN'S PANEL AND RECEPTION

How to Enhance Women's Participation in Engineering Around the Globe

Wednesday, May 30, 2018
6:30 p.m. – 7:30 p.m.
Harbor Island 3

Chairs: Cristina Amon – University of Toronto and Tanja Braun - Fraunhofer Institute for Reliability and Microintegration (IZM)

Speakers:
1. Kawthar (Kat) Kasim, Boeing Research and Technology, USA
2. Jayathi Murthy, UCLA Dean of Engineering, USA
3. Li Ming, R&D Director, Enabling Technologies at ASM Pacific Technology, Hong Kong

2018 PLENARY SESSION

Artificial Intelligence and Its Impact on System Design

Wednesday, May 30, 2018
7:30 p.m. – 9:00 p.m.
Harbor Island 1 & 2

Chair: Kemal Aygun – Intel Corporation

Speakers:
1. Igor Arsovski, GLOBALFOUNDRIES
2. Kailash Gopalakrishnan, IBM Corporation
3. Andrew Putnam, Microsoft Corporation
4. Madhavan Swaminathan, Georgia Institute of Technology
5. Dan Oh, Samsung

2018 IEEE EPS SEMINAR

High Density Packaging Technologies in the Era of Big Data

Thurday, May 31, 2018
8:00 p.m. – 9:30 p.m.
Harbor Island 1 & 2

Chairs: Yasumitsu Orii - Nagase, Japan and Sheigenori Aoki – Fujitsu

Speakers:
1. Shunichi Kikuchi, Fujitsu
2. Spike Narayan, IBM Research
3. Urmi Ray, JCET StatsChipPac
4. Masato Tanaka, Shinko
5. Toshihisa Nonaka, Hitachi Chemical

PROFESSIONAL DEVELOPMENT COURSES
TUESDAY, MAY 29, 2018

Morning Courses 8:00 a.m. – 12:00 Noon	Afternoon Courses 1:15 p.m. – 5:15 p.m.
Seabreeze **1. Achieving High Reliability of Lead-Free Solder Joints – Materials Considerations** *Course Leader: Ning-Cheng Lee – Indium Corporation*	**Seabreeze** **10. Flip Chip Fabrication and Interconnection** *Course Leaders: Eric Perfecto – GLOBALFOUNDRIES; Shengmin Wen – Synaptics Inc.*
Harbor Island 1 **2. Introduction to Fan-Out Wafer-Level Packaging** *Course Leader: Beth Keser – Intel Corporation*	**Harbor Island 1** **11. Wafer-Level Chip-Scale Packaging** *Course Leader: Luu Nguyen - Texas Instruments, Inc.*
Harbor Island 2 **3. Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging** *Course Leaders: Aric Shorey and Jingshi Wu – Corning Inc.*	**Harbor Island 2** **12. Flexible Hybrid Electronics – Manufacturing and Reliability** *Course Leader: Pradeep Lall – Auburn University*
Harbor Island 3 **4. Future of Device and Systems Packaging in Post Moore's Law** *Course Leader: Rao Tummala – Georgia Institute of Technology*	**Harbor Island 3** **13. Fan-Out Wafer-Level Packaging and 3D Packaging** *Course Leader: John Lau – ASM Pacific Technology Ltd.*
Spinnaker **5. Introduction to Mechanics-Based Quality and Reliability Assessment Methodology** *Course Leaders: Shubhada Sahasrabudhe and Sandeep Sane – Intel Corporation*	**Spinnaker** **14. Polymers for Electronic Packaging** *Course Leader: Jeffrey Gotro – InnoCentrix, LLC*
Grande Ballroom A **6. Polymers and Nanocomposites for Electronic and Photonic Packaging** *Course Leaders: C. P. Wong – Georgia Institute of Technology; Daniel Lu – Henkel Corporation*	**Grande Ballroom A** **15. Corrosion in Microelectronic Packages** *Course Leader: Varughese Mathew – NXP Semiconductors*
Nautilus 1 & 2 **7. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Panel-Level Packages and Interposers** *Course Leaders: Ivan Ndip and Markus Wöhrmann – Fraunhofer IZM*	**Nautilus 1 & 2** **16. Ageing of Polymers and the Influence on Microelectronic Package Reliability** *Course Leaders: Tanja Braun and Ole Hölck – Fraunhofer IZM*
Nautilus 3 & 4 **8. Reliability Mechanics and Modeling for IC Packaging - Theory, Implementation and Practices** *Course Leaders: Ricky Lee – HKUST and Xuejun Fan – Lamar University*	**Nautilus 3 & 4** **17. Solving Package Failure Mechanisms for Improved Reliability** *Course Leader: Darvin Edwards – Edwards Enterprises*
Nautilus 5 **9. Integrated Thermal Packaging and Reliability of Power Electronics** *Course Leader: Patrick McCluskey – University of Maryland*	**Nautilus 5** **18. Design and Optimization of Heat Sinks** *Course Leaders: Marc Hodes – Tufts University; Georgios Karamanis – Transport Phenomena Technologies, LLC.*

Refreshment Breaks – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.
Harbor Island Foyer, Grande Ballroom A Foyer, and Nautilus Foyer

2018 ECTC/ITHERM YOUNG PROFESSIONALS PANEL AND RECEPTION

Tuesday, May 29, 2018
7:00 p.m. – 7:45 p.m.
Harbor Island 3

Chair: Yan Liu – Medtronic, Inc.

ECTC and ITherm cordially invite young professionals (including current graduate students) to attend this networking event. The two panelists will talk about career development for young professionals based on their experiences and achievements in the industry and academia. A reception for panelists and attendees will follow.

Speakers:
1. Steve Bezuk, Qualcomm Technologies, Inc.
2. Kathleen Kramer, University of San Diego

ECTC STUDENT RECEPTION
Tuesday, May 29, 2018 • 5:00 p.m. - 6:00 p.m.
Host: Texas Instruments, Inc.
Executive Center 3

ECTC welcomes our student attendees and student presenters who bring their research results to our audience. The Student Reception is an event where students can get guidance for their job search from industry leaders. In addition to the Student Reception, in the Student Interactive Presentation Session, we provide our audience one-on-one access to students and their research. We encourage you to attend the Student Interactive Presentation Session on Friday in the Nautilus Foyer. This reception is sponsored by Texas Instruments, Inc.

GENERAL CHAIR'S SPEAKERS RECEPTION
Tuesday, May 29, 2018 • 6:00 p.m. - 7:00 p.m.
Grande Ballroom B

Invited session chairs and speakers are requested to attend the reception.

TECHNOLOGY CORNER RECEPTION
Wednesday, May 30, 2018 • 5:30 p.m. - 6:30 p.m.
Bayview Pavilion

An Exhibitor Sponsored Reception will be held in the Bayview Pavilion. All attendees and guests are invited.

68th ECTC GALA RECEPTION
Thursday, May 31, 2018 • 6:30 p.m.
Outisde at the Bayview Lawn;
(Rain Back Up – Grande Ballroom)

All badged attendees and guests are invited to attend our Gala Reception outside at the Bayview Lawn.

CONTINUING EDUCATION UNITS

The IEEE Electronics Packaging Society (EPS) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 68th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops. Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Course CEUs will be underwritten by the conference, i.e., there are no additional costs for Professional Development Course attendees to obtain CEU credit.

2017 ECTC BEST PAPER AWARDS

BEST OF CONFERENCE PAPERS – 2017

The Electronic Components and Technology Conference is proud to announce the "Best of Conference" papers selected from the 67th ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500, and the authors of the Best Interactive Presentation share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

Best Session Paper

Session 28, Paper 3

High Thermal Conductivity Mold Compounds for Advanced Packaging Applications

Makoto Shibuya & Luu Nguyen – Texas Instruments, Inc.

Best Interactive Presentation Paper

Session 39, Paper 6

Development of Die Attachment Technology for Power IC Module by Introducing Indium into Sintered Nano-silver Joint

C. A. Yang, C. Robert Kao – National Taiwan University; and H. Nishikawa – Osaka University

INTEL BEST STUDENT PAPER – 2017

The winning student receives a personalized plaque and a check for US $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 67th ECTC:

Session 2, Paper 7

Latency, Bandwidth and Power Benefits of the Super CHIPS Integration Scheme

Siva Chandra Jangam, Saptadeep Pal, Adeel Bajwa, Sudhakar Pamarti, Puneet Gupta, and Subramanian Iyer – University of California, Los Angeles

OUTSTANDING PAPERS – 2017

The winning authors for the Conference Outstanding Session Paper and Interactive Presentation selected from the 67th ECTC proceedings receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

Outstanding Session Paper

Session 18, Paper 4

Warpage Modeling and Characterization of the Viscoelastic Relaxation for Cured Molding Process in Fan-Out Packages

Shu-Shen Yeh, Po-Yao Lin, Kuang-Chun Lee, Jin-Hua Wang, Wen-Yi Lin, Ming-Chih Yew, Po-Chen Lai, Shyue-Ter Leu, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company, Ltd.

Outstanding Interactive Presentation

Session 40, Paper 8

Via-in-Trench: A Revolutionary Panel-based Package RDL Configuration capable of 200-450 IO/mm/layer, an Innovation for More-Than-Moore System Integration

Fuhan Liu, Chandrasekharan Nair, Hao Lu, Rui Zhang, Hang Chen, Venky Sundaram, and Rao R. Tummala – Georgia Institute of Technology; Atsushi Kubo and Tomoyuki Ando – Tokyo Ohka Kogyi; Kwon Sang Lee – Disco Corporation

TEXAS INSTRUMENTS OUTSTANDING STUDENT INTERACTIVE PRESENTATION – 2017

The winning student receives a personalized plaque and a check for US $500. The following paper was selected based on the Texas Instruments Outstanding Student Interactive Presentation competition conducted at the 67th ECTC:

Session 39, Paper 6

Development of Die Attachment Technology for Power IC Module by Introducing Indium into Sintered Nano-Silver Joint

Chun An Yang and C. Robert Kao – National Taiwan University; Hiroshi Nishikawa – Osaka University

COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

Tuesday, May 29, 2018

8:00 a.m. – 5:00 p.m.
Heterogeneous Integration Roadmap Workshop
Executive Center 1 & 4

9:00 p.m. – 10:30 p.m.
ECTC Optoelectronics Committee
518, 5th Floor

9:00 p.m. – 10:30 p.m.
ECTC Interconnections Committee
411, 4th Floor

Wednesday, May 30, 2018

7:00 a.m. – 8:00 a.m.
EPS Power & Energy TC
514, 5th Floor

4:30 p.m. – 5:30 p.m.
EPS Technical Committee Chairs
511, 5th Floor

6:00 p.m. – 7:00 p.m.
Program Subcommittee Chairs & Assistant Chairs Reception
General Chair's Suite
(by invitation only)

Thursday, May 31, 2018

7:00 a.m. – 8:00 a.m.
EPS Region 8 Meeting
Seabreeze

7:00 a.m. – 8:00 a.m.
EPS Nanotechnology TC
511, 5th Floor

7:00 a.m. – 8:00 a.m.
EPS High Density Substrates & Boards TC
514, 5th Floor

7:00 a.m. – 8:00 a.m.
EPS Region 10 Meeting
Spinnaker 1

7:00 a.m. – 8:00 a.m.
EPS Reliability TC
Spinnaker 2

9:00 a.m. – 10:00 a.m.
ECTC High-Speed, Wireless & Components Committee
Marina 2

5:30 p.m. – 6:30 p.m.
ECTC 2019 Program Committee Meeting
Harbor Island 3

8:00 p.m.
68th ECTC Steering/Executive Committee Reception
General Chair's Suite

Friday, June 1, 2018

7:00 a.m. – 8:00 a.m.
EPS Transaction Editors TC / AEs
511, 5th Floor

7:00 a.m. – 8:00 a.m.
EPS RF & THz Techn. TC/ECTC Components Committee
514, 5th Floor

7:00 a.m. – 8:00 a.m.
EPS Emerging Technologies TC
Spinnaker 1

7:00 a.m. – 8:00 a.m.
EPS Electrical Design, Modeling & Simulation TC
Spinnaker 2

1:30 p.m. – 4:30 p.m.
ECTC Executive Committee
Executive Center 3

4:45 p.m. – 5:45 p.m.
ECTC Steering Committee
Executive Center 3

Program Sessions: Wednesday, May 30, 8:00 a.m. - 11:40 a.m.

Session 1: Flexible Electronics, Substrate for High Frequency Applications	Session 2: Advances in Wafer and Panel-Level Fan-Out Packaging	Session 3: 3D Design, Assembly and Additive Manufacturing
Committee: Materials & Processing	**Committee: Advanced Packaging**	**Committee: Emerging Technologies joint with Advanced Packaging**
Room: Harbor Island 1	**Room: Harbor Island 2**	**Room: Harbor Island 3**
Session Co-Chairs: **Yan Liu – Medtronic Inc. USA** **Email: yan.x.liu@medtronic.com** **Lejun Wang – Qualcomm Technologies, Inc.** **Email: lejunw@qti.qualcomm.com**	**Session Co-Chairs:** **Beth Keser – Intel Corporation** **Email: beth.keser@intel.com** **Mike Ma – Amkor Technology Taiwan (ATT)** **Email: mike.ma@amkor.com**	**Session Co-Chairs:** **Benson Chan – Binghamton University** **Email: chanb@binghamton.edu** **John Knickerbocker – IBM Corporation** **Email: knickerj@us.ibm.com**
1. 8:00 AM - In-Situ Stress Determination of Electroless Cu on PCB-relevant Substrates Tobias Bernhard, L. Gregoriades, E. Steinhäuser, S. Kempa, and F. Brüning – Atotech Deutschland GmbH; Ralf Bruening, T. Sharma, D. Brown, and E. A. Luy – Mount Allison University	***1. 8:00 AM - A Novel Submicron Polymer Redistribution Layer Technology for Advanced InFO Packaging*** Han-Ping Pu, H.J. Kuo, C.S. Liu, and Douglas C.H. Yu – Taiwan Semiconductor Manufacturing Company, Ltd.	***1. 8:00 AM - Novel Failure Analysis Techniques for 1.8 µm Pitch Wafer-to-Wafer Bonding*** Christian Schmidt and Lorenz Lechner - ZEISS; Ingrid De Wolf, Soon-Wook Kim and Eric Beyne - IMEC
2. 8:25 AM - Stretchable, Printable and Electrically Conductive Composites for Wearable RF Antennas Bo Song, Ryan Bahr, Fan Wu, Kyoung-sik Moon, Manos Tentzeris, and C.P. Wong – Georgia Institute of Technology	***2. 8:25 AM - Fan-Out Panel Level Package With Fine-Pitch Pattern*** Jinyoung Kim, Ikjun Choi, JunHyeong Park, Jae-Ean Lee, TaeSung Jeong, Jungsoo Byun, Young Gwan Ko, and Kangheon Hur – Samsung Electro-Mechanics Co., Ltd.; Dae-Woo Kim and Kyung Suk Oh - Samsung Electronics	***2. 8:25 AM - Column Interconnects: A Path Forward for Embedded Cooling of High-Power 3D Chip Stacks*** Mark Schultz, Cyril Cabral, Joana Maria, Paul Andry, Qianwen Chen, and Timothy Chainer – IBM Corporation; Cornelia Tsang Yang – Raytheon
3. 8:50 AM - A Study on the Anchoring Polymer Layer (APL) Solder Anisotropic Conductive Films (ACFs) for Ultra Fine Pitch Flex-On-Flex (FOF) Assembly Using an Ultrasonic Bonding Method Dal-Jin Yoon, Sang Hoon Lee, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology	***3. 8:50 AM - Ultra Fine RDL Structure Fabrication Using Alternative Patterning and Bottom-Up Plating Processes*** Richard Hollman – TEL Advanced Packaging.; Ognian Dimov and Sanjay Malik – Fujifilm Electronic Materials U.S.A., Inc.; Markus Arendt and Habib Hichri – SUSS Microtec Photonic Systems, Inc.	***3. 8:50 AM - Assembly Process Development of Ultra Large Scale 3D Stacking with Transmission Circuits Via TSVs*** Shunichi Kikuchi, Hidehiko Kira, Makoto Suwada, and Tatsumi Nakada – Fujitsu Limited; Naoaki Nakamura, Norio Kainuma, Kazuhiro Kanai, and Takumi Masuyama – Fujitsu Advanced Technologies Limited
Refreshment Break: 9:15 a.m. - 10:00 a.m. Bayview Pavilion		
4. 10:00 AM - Development of Novel BT Laminate Material for Low-Loss and High-Speed Transmission Masahiko Shigaki, Mika Suzuki, Takashi Kobayashi, Kentarou Takano, Takaki Tsuchida, Sotaro Hiramatsu, Yoshitaka Ueno, Tsuyoshi Kida, Shu Yoshida, and Toyoji Oshima – Mitsubishi Gas Chemical Company, Inc.	***4. 10:00 AM - Low-Cost Si-Less RDL Interposer Package for High-Performance Computing Applications*** Kyoung-Lim Suk, Seok Hyun Lee, Jong Youn Kim, Seok Won Lee, Hak Jin Kim, Su Chang Lee, Pyung Wan Kim, Dae-Woo Kim, and Dan (Kyung Suk) Oh – Samsung Electronics Co., Ltd.; Jung Soo Byun – Samsung Electro-Mechanics Company, Ltd.	***4. 10:00 AM - The Principles of "Smart" Encapsulation: Using Additive Printing Technology for the Realization of Intelligent Application-Specific Packages for IoT, 5G, and Automotive Radar Applications*** Bijan Tehrani, Ryan Bahr, and Manos Tentzeris – Georgia Institute of Technology; Daniel Revier and Benjamin Cook – Texas Instruments, Inc.
5. 10:25 AM - Organic Substrate Material With Low Transmission Loss and Effective in Suppressing Package Warpage for 5G Application Shunsuke Tonouchi, Etsuo Mizushima, Tomio Fukuda, Tomokazu Shimada, Yukio Nakamura, and Toshiyuki Iijima – Hitachi Chemical Company, Ltd.	***5. 10:25 AM - Panel Level Packaging - A View Along the Process Chain*** T. Braun, K. F. Becker, O. Hoelck, R. Kahle, M. Wöhrmann, L. Boettcher, M. Topper, L. Stobbe, H. Zedel and R. Aschenbrenner – Fraunhofer IZM; S. Voges, M. Schneider-Ramelow, K. D. Lang - Technical University Berlin	***5. 10:25 AM - A New Microsystem Packaging Approach Using 3D Printing Encapsulation Process*** Gabrielle Aspar, Baptiste Goubault de Brugiere, Jean-Charles Souriau, Laetitia Castagne, Gilles Simon, and Lea Di Cioccio – CEA-LETI; Yves Brechet – CEA
6. 10:50 AM - Porous Epoxy Film for Low Dielectric Constant Chip Substrates and Boards Jisu Jiang, Oluwadamilola Phillips, Landon Keller and Paul Kohl – Georgia Institute of Technology	***6. 10:50 AM - Patterning High-Resolution Features Through the Integration of an Advanced Lithography System With a Novel Nozzleless Spray Coating Technology*** Jack Mach and Corey Shay – Rudolph Technologies, Inc.; Stuart Erickson – Ultrasonic Systems Inc.; Gary Smith - Sumitomo Chemical Advanced Technologies	***6. 10:50 AM - A Design Study of 3D Printed Reduced Height Waveguide Structures*** Vincens Gjokaj and Premjeet Chahal – Michigan State University
7. 11:15 AM - Development of Multi-Layered Build-Up Insulation Dry-Film Material for Ultra-Low Transmission Loss Wirings for High-Speed Semi-Conductor Packaging Zhong Guan and Arata Endo – Taiyo Ink Mfg. Co. Ltd.; Tadahiko Hanada – Taiyo America, Inc.	***7. 11:15 AM - Extreme Thinned-Wafer Bonding Using Low-Temperature Curable Polyimide for Advanced Wafer Level Integrations*** Julien Bertheau, Fumihiro Inoue, Alain Phommahaxay, Serena Iacovo, Ian Peng, Erik Sleeckx, Kenneth Rebibis, Andy Miller, Gerald Beyer, Eric Beyne, and Nouredine Rassoul – IMEC; Atsushi Nakamura – Fujifilm	***7. 11:15 AM - Self-Powered, Inkjet Printed Electrochromic Films on Flexible and Stretchable Substrate for Wearable Electronics Applications*** Ebraheem Azhar, Hongbin Yu, and Terry Alford – Arizona State University

Program Sessions: Wednesday, May 30, 8:00 a.m. - 11:40 a.m.

Session 4: Automotive and Harsh Environment Reliability	Session 5: Antenna-in-Package for RF and mm-Wave Systems	Session 6: Warpage and Moisture Characterization
Committee: Applied Reliability	**Committee: High-Speed, Wireless & Components**	**Committee: Thermal/Mechanical Simulation & Characterization**
Room: Nautilus 1 & 2	**Room: Nautilus 3 & 4**	**Room: Nautilus 5**
Session Co-Chairs: **Varughese Mathew – NXP Semiconductors** **Email: varughese.mathew@nxp.com** **Vikas Gupta – Texas Instruments, Inc.** **Email: gvikas@ti.com**	**Session Co-Chairs:** **Maciej Wojnowski – Infineon Technologies AG** **Email: maciej.wojnowski@infineon.com** **Prem Chahal – Michigan State University** **Email: chahal@msu.edu**	**Session Co-Chairs:** **Przemyslaw Gromala – Robert Bosch GmbH** **Email: Przemyslawjakub.gromala@de.bosch.com** **Jiantao Zheng – Qualcomm Technologies, Inc.** **Email: jiantaoz@qti.qualcomm.com**
1. 8:00 AM - Novel Corrosion Prevention Treatments for Cu Wire Bonded Device to Improve Bonding Reliability Muthappan Asokan, Oliver Chyan, Joshua Caperton, and Zachary Thompson – University of North Texas; Mahmud Chowdhury, Shawn O' Connor, and Luu Nguyen – Texas Instruments, Inc.	***1. 8:00 AM - Small Shielded Bluetooth Module Equipped with Slot Antenna on the Surface*** Keiju Yamada, Makoto Sano, Makoto Higaki, and Akihiko Happoya – Toshiba Corporation	***1. 8:00 AM - A Novel Finite Element Technique for Moisture Diffusion Modeling using ANSYS*** Cagan Diyaroglu – University of Arizona; Selda Oterkus and Erkan Oterkus – University of Strathclyde
2. 8:25 AM - A Monte Carlo Approach to Predicting Failure Across Multiple Temperature and Humidity Field Environments Jonathon Tucker, Ramji Dhakal, George Thiel, and Virendra Jadhav – Microsoft Corporation	***2. 8:25 AM - A 77 GHz Antenna-in-Package with Low-Cost Solution for Automotive Radar Applications*** Cheng Yu Ho, Sheng-Chi Hsieh, Ming-Fong Jhong, Chen-Chao Wang, and Chun-Yen Ting – Advanced Semiconductor Engineering, Inc.	***2. 8:25 AM - Adaptive Curvature Flexure Test to Assess Flexible Electronic Systems*** Rui Chen, Justin Chow, Christine Taylor, and Suresh Sitaraman – Georgia Institute of Technology; Jeffrey Meth - DuPont Electronics & Imaging
3. 8:50 AM - Improve Interconnect Reliability of BGA Substrate with Stacked Vias by Reducing Carbon Inclusion in the Interface between Via and Land Pad Kejun Zeng and Jaimal Williamson – Texas Instruments, Inc.	***3. 8:50 AM - An Enhanced 64-Element Dual-Polarization Antenna Array Package for W-band Communication and Imaging Applications*** Xiaoxiong Gu, Duixian Liu, Christian Baks, Jean-Oliver Plouchart, Wooram Lee, and Alberto Valdes-Garcia – IBM Corporation	***3. 8:50 AM - Parametric Optimization and Yield Probability Prediction of Package Warpage*** Shenghua Huang, Zhongli Ji, Ning Ye, Yangming Liu, and Hem Takiar – Western Digital Corporation
Refreshment Break: 9:15 a.m. - 10:00 a.m. Bayview Pavilion		
4. 10:00 AM - Understanding Underfill Degradation in Reliability Testing Conditions for ADAS Packages Development Ziyin Lin, Vijay Subramanian, Pramod Malatkar, and Nisha Anathakrishnan - Intel Corporation	***4. 10:00 AM - InFO_AiP Technology for High-Performance and Compact 5G Wave System Integration*** Chuei-Tang Wang, Tzu-Chun Tang, Chun-Wen Lin, Che-Wei Hsu, Jeng-Shien Hsieh, Chung-Hao Tsai, Kai-Chiang Wu, Han-Ping Pu, and Douglas Yu – Taiwan Semiconductor Manufacturing Company	***4. 10:00 AM - An Integrated Warpage Prediction Model Based on Chemical Shrinkage and Viscoelasticity for Molded Underfill*** Shu-Shen Yeh, Po-Yao Lin, Kuang-Chun Lee, Jin-Hua Wang, Wen-Yi Lin, Ming-Chih Yew, Po-Chen Lai, Chia-Kuei Hsu, Che-Chia Yang, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company
5. 10:25 AM - Quantification and Modeling of Microstructural Evolution in Lead-Free Solders During Long Term Isothermal Aging Sudan Ahmed, Jing Wu, Nianjun Fu, Jeffrey Suhling, and Pradeep Lall – Auburn University	***5. 10:25 AM - Mm-Wave Antenna in Package (AiP) Design Applied to 5th Generation (5G) Cellular User Equipment Using Unbalanced Substrate*** Ying-Wei Lu, Bo-Siang Fang, Hsuan-Hao Mi, and Kuan-Ta Chen – Siliconware Precision Industries Co., Ltd.	***5. 10:25 AM - Trend Plots for Different Mold-thick Selection on Warpage Design of MUF FCCSP with 4L ETS*** Chih-Sung Chen, Nicholas Kao, and Don Son Jiang – Siliconware Precision Industries Co. Ltd.
6. 10:50 AM - Reliability Enhancement of Automotive Electronic Modules Using Various Glues Dongji Xie, Zhongming Wu, Joe Hai, and Manthos Economou – Nvidia Corp.	***6. 10:50 AM - Novel 3D-/Inkjet-Printed Flexible On-Package Antennas, Packaging Structures, and Modules for Broadband 5G Applications*** Tong-Hong Lin, Ryan A. Bahr, Manos M. Tentzeris, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology	***6. 10:50 AM - Numerical/Experimental Hybrid Approach to Predict Warpage of Thin Advanced Substrates*** Byung Kim and Bongtae Han – University of Maryland
7. 11:15 AM - High-Temperature and Moisture Ageing Reliability of High-Density Power Packages for Electric Vehicles Shreya Dwarakanath, P. Markondeya Raj, Vanessa Smet, Venky Sundaram, Mark Losego, and Rao Tummala – Georgia Institute of Technology	***7. 11:15 AM - A Compact 27 GHz Antenna-in-Package (AiP) With RF Transmitter and Passive Phased Antenna Array*** Mei Xue and Delong Qiu -- Institute of Microelectronics of Chinese Academy of Sciences; Liqiang Cao -- University of Chinese Academy of Sciences; Qidong Wang and Jun Li -- National Center for Advanced Packaging	***7. 11:15 AM - Warpage and Thermal Stress Under Thermal Cycling Test in SiC and Si Power Device Structures Using Direct Chip-Bonding with Ag Sintered Layer on Cu Plate*** Masaki Kanemoto, Masaaki Aoki, and Nobuhiko Nakano – Keio University; Akihiro Mochizuki, Yoshio Murakami, and Mutsuharu Tsunoda – MacDermid Performance Solutions

Program Sessions: Wednesday, May 30, 1:30 p.m. - 5:10 p.m.

Session 7: Low-Temperature Metallic Interconnection Technologies	Session 8: Fan-Out Packaging-Applications and Architectures	Session 9: Flip-Chip Manufacturing Challenges
Committee: Interconnections	**Committee: Advanced Packaging**	**Committee: Assembly & Manufacturing Technology**
Room: Harbor Island 1	**Room: Harbor Island 2**	**Room: Harbor Island 3**
Session Co-Chairs: **David Danovitch – University of Sherbrooke** **Email: David.Danovitch@USherbrooke.ca** **Matthew Yao – GE Energy Management** **Email: matthew.yao@ge.com**	**Session Co-Chairs:** **Bora Baloglu – Amkor Technology** **Email: bora.baloglu@amkor.com** **Kuo-Chung Yee-TSMC** **Email: kcyee@tsmc.com**	**Session Co-Chairs:** **Jae-Woong Nah – IBM Corporation** **Email: jnah@us.ibm.com** **Garry Cunningham – NGC** **Email: Garry.Cunningham@ngc.com**
1. 1:30 PM - Laser Sintering of Dip-Based All-Copper Interconnects Luca Del Carro, Thomas Brunschwiler – IBM Corporation; Martin Kossatz, Lucas Schnackenberg, Matthias Fettke – Pac Tech - Packaging Technologies GmbH; Ian Clark – Intrinsiq Materials Ltd.	***1. 1:30 PM - Millimeter-Wave Antenna in Fan-Out Wafer Level Packaging for 60 GHz WLAN Application*** Zihao Chen, Lim Tech Guan, David Soon We Ho, and Surya Bhattacharya – Institute of Microelectronics, A*STAR, Singapore	***1. 1:30 PM - Low-Temperature Assembly of Surface-Mount Device on Flexible Substrate using Additive Printing Process*** Christine Taylor, Vanessa Smet, Xuanke He, Manos Tentzeris, and Suresh Sitaraman – Georgia Institute of Technology
2. 1:55 PM - Low-Temperature Fine-pitch Wafer-level Cu-Cu Bonding Using Nanoparticles Fabricated by PVD Zijian Wu, Qian Wang, Changming Song, and Jian Cai – Institute of Microelectronics, Tsinghua University	***2. 1:55 PM - 3D Heterogeneous Integration with Multiple Stacking Fan-Out Package*** Feng-Chen Hsu, Jackson Li, Shuo-Mao Chen, Po-Yao Lin, Jerry Fang, Jin-Hua Wang and Shin-Puu Jeng - TSMC	***2. 1:55 PM - Evaluation of Chip-last Fan-out Panel Level Packaging with G2.5 LCD Facility Using FlexUP(TM) and Mechanical De-bonding Technologies*** Wei-Yuan Cheng, Yuh-Zheng Lee, Chen-Tsai Yang, Jie-Mo Lin, Tai-Jui Wang, and Wei-Han Chen – Industrial Technology Research Institute
3. 2:20 PM - Transient Liquid Phase Bonding Using AgSn-Alloys for Stress Reduced Sensor Mounting Markus Feisst, Jun Yu, and Juergen Wilde – University of Freiburg, IMTEK	***3. 2:20 PM - Study of Advanced Fan-Out Packages for Mobile Applications*** Taejoo Hwang, Dan (Kyung Suk) Oh, Eunseok Song, Kilsoo Kim, Seokwon Lee, and Jaechoon Kim – Samsung Electronics Company, Ltd.	***3. 2:20 PM - Design and Application of Innovative Multi-Table and Bond Head Drive System on Thermal Compression Bonder with UPH over 2000*** Kohei Seyama, Shoji Wada, Yuji Eguchi, and Tomonori Nakamura – Shinkawa Ltd.; Shigetoshi Sugawa – Tohoku University; Doug Day - Shinkawa USA, Inc.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Bayview Pavilion		
4. 3:30 PM - Demonstration of Patternable All-Cu Compliant Interconnections with Enhanced Manufacturability in Chip-to-Substrate Applications Kashyap Mohan, Ninad Shahane, Ramon Sosa, Raj Pulugurtha, Antonia Antoniou, Vanessa Smet, and Rao Tummala – Georgia Institute of Technology; Sadia Khan - Texas Instruments, Inc	***4. 3:30 PM - An RDL-First Fan-out Wafer Level Package for Heterogeneous Integration Applications*** Y. M. Lin, S. T. Wu, W. W. Shen, S. Y. Huang, T. Y. Kuo, A. Y. Lin, T. C. Chang, H. H. Chang, and S. M. Lee – Industrial Technology Research Institute (ITRI); C. H. Lee, J. Su, X. Liu, and Q. Wu – Brewer Science Taiwan; K. N. Chen – National Chiao Tung University .	***4. 3:30 PM - Adhesion Property of Polyimide and Passivation Layer for Polymer/Metal Wafer-level Hybrid Bonding in 3D Integration*** Cheng-Hsien Lu, Yi-Tung Kho, Yu-Tao Yang, and Kuan-Neng Chen – National Chiao Tung University; Chiao-Pei Chen,Yu-Pei Chen, Chiu-Feng Chen, and Tsuang-Tai Hung - Taiflex Scientific Corporation
5. 3:55 PM - Development of Low-Temperature, Presssureless Copper-to-Copper Bonding by Microfluidic Electroless Interconnection Process Sean Yang, H. T. Hung, and C. Robert Kao – National Taiwan University; H. Nisikawa – Joining and Welding Institute Osaka University	***5. 3:55 PM - Chip-First Fan-Out Panel-Level Packaging for Heterogeneous Integration*** C. T. Ko, H. Lang, C. Lin, J. W. Lin, Y. H. Chen - Unimicron Technology Corp.; J. Lau, M. Li, M. Li, N. Fan, Y. M. Cheung, E. Ng, W. Kai, J. Hao, M. Li - ASM Pacific Technology Ltd.; T. Chen, I. Xu, Z. Li, K. H. Tan - Jiangyin Changdian Advanced Packaging Co. Ltd.; C. L. Chang, J. Y. Pan, H. H. Wu, R. Beica, M. Lin - The Dow Chemical Company; Q. X. Wong, Z. Cheng, K. S. Wee, J. Ran, C. Xi - Huawei Technologies Co., Ltd.; S.P. Lim, N.C. Lee - Indium Corporation; M. Tao, J. Lo, R. Lee - Hong Kong University of Science and Technology	***5. 3:55 PM - Advances in Memory Die Stacking*** Oranna Yauw, Daniel Buergi, Jie Wu, Andreas Marte, Horst Clauberg, and Bob Chylak – Kulicke and Soffa, Inc.; Urban Ernst - Kulicke & Soffa Switzerland; Ulrich Barthold and Ulf Friederichs - CADFEM GmbH
6. 4:20 PM - Scaling Packaging Interconnect Below 20 µm With Hybrid Bonding Guilian Gao, Laura Mirkarimi, Gill Fountain, Liang Wang, Cyprian Uzoh, Thomas Workman, Gabe Guevara, Chandrasekhar Mandalapu, Bongsub Lee, and Rajesh Katkar – Xperi	***6. 4:20 PM - Design and Fabrication of Feasible 3D Optoelectronics Integration Based on Embedded IC Fanout Technology*** Fengman Liu – Institute of Microelectronics, Chinese Academy of Science; Xueping Guo, Fengze Hou, Haiyun Xue, Yu Sun, Huimin He, Zhaoyao Y, Wenqi Zhang and Liqiang Cao - System Packaging and Integration Center/ Institute of Microelectronics, Chinese Academy; Qian She - National Center for Advanced Packaging	***6. 4:20 PM - Plasma Treatment for Fluxless Flip-Chip Chip-Joining Process*** Maxime Godard, Dominique Drouin, and Maxime Darnon – Université de Sherbrooke; Serge Martel and Clément Fortin – IBM Corporation
7. 4:45 PM - Micro-Silver Sinter Paste Developed for Pressure Sintering on Bare Cu Surfaces Under Air or Inert Atmosphere Ly May Chew, Wolfgang Schmitt, Christian Schwarzer and Jens Nachreiner – Heraeus Deutschland GmbH & Co. KG	***7. 4:45 PM - A Novel Fan-Out Concept for Ultra-High Chip-to-Chip Interconnect Density with 20 µm Pitch*** Arnita Podpod, John Slabbekoorn, Alain Phommahaxay, Fabrice Duval, Abdellah Salahouelhadj, Mario Gonzalez, Kenneth Rebibis, Andy Miller, Gerald Beyer, and Eric Beyne – IMEC	***7. 4:45 PM - Effects of Laser Selective Reflow on Solder Joint Microstructure and Reliability*** Luke Wentlent – Universal Instruments Corp.; Mohammed Genanu, Thaer Alghoul, and Peter Borgesen – Binghamton University; Jim Wilcox – Universal Instruments Corp; Francis Mutuku – Indium Corporation

Program Sessions: Wednesday, May 30, 1:30 p.m. - 5:10 p.m.

Session 10: Innovative Design, Modeling and Predictions for Reliability	Session 11: Emerging Packaging Technologies for 5G and Advanced Computing	Session 12: Sintering Pastes, Transient Liquid Phase and Direct Bonding
Committee: **Applied Reliability**	**Committee:** **Emerging Technologies**	**Committee:** **Materials & Processing**
Room: Nautilus 1 & 2	**Room: Nautilus 3 & 4**	**Room: Nautilus 5**
Session Co-Chairs: **Tim Chaudhry – Amkor Technology, Inc.** **Email: timchaudhry@gmail.com** **Lakshmi N. Ramanathan – Microsoft Corporation** **Email: laramana@microsoft.com**	**Session Co-Chairs:** **Vaidyanathan Chelakara – Acacia Communications** **Email: cvaidyanathan@acacia-inc.com** **Ramakrishna Kotlanka – Analog Devices** **Email: rama.krishna@analog.com**	**Session Co-Chairs:** **Dwayne Shirley – Inphi** **Email: shirley@ieee.org** **Mikel Miller – EMD Performance Materials** **Email: mikel.miller@emdgroup.com**
1. 1:30 PM - Die Attach Delamination Analysis and Modeling Between Temperature Cycling and Thermal Shock for Exposed Pad Lead Frame Devices Madison Koziol, Yutaka Suzuki, Siva Gurrum, and Muhammad Khan – Texas Instruments, Inc.	***1. 1:30 PM - Modeling and Design of a 3D Interconnect Based Circuit Cell Formed with 3D SiP Techniques Mimicking Brain Neurons for Neuromorphic Computing Applications*** M. Miao, L. Wang, T. Chen, X. Duan, J. Zhang, and N. Li – Beijing Information Science and Technology University; L. Sun, R. Fang , X. Sun, H. Liu and Y. Jin – Peking University	***1. 1:30 PM – Pressure-less Sintering of Large Dies Using Infrared Radiation and Optimized Silver Sinter Paste*** Wolfgang Schmitt and Ly May Chew – Heraeus Deutschland GmbH & Co. KG; Robert Miller – Hochschule Aschaffenburg, University of Applied Sciences
2. 1:55 PM - A Comparison Study of Cu Dissolution Kinetics in Solder Joints Under Electromigration and Extended Reflow Pilin Liu, Alan Overson, and Deepak Goyal – Intel Corporation	***2. 1:55 PM - Surface Mount Electroosmotic Pump for Integrated Microfluidic Printed Circuit Boards*** Sarkis Babikian and G. P. Li – University of California, Irvine; Makoto Jinsenji – OM Sangyo Co. Ltd; Mark Bachman – Integra Devices	***2. 1:55 PM - Direct Bonding Silver to Aluminum Using Eutectic Reaction in Air*** Shao-Wei Fu and Chin C. Lee – University of California, Irvine
3. 2:20 PM - Anand Parameters for Modeling Prolonged Storage on High Strain Rate Mechanical Properties of SAC-Q Leadfree Solder at High Operating Temperature Pradeep Lall, Vikas Yadav, and Jeff Suhling – Auburn University; David Locker – US Army AMRDEC	***3. 2:20 PM - Cryogenic Qubit Integration for Quantum Computing*** Rabindra Das, Danna Rosenberg, David Kim, Jonilyn Yoder, Donna-Ruth Yost, David Hover, Andrew Kerman, Justin Mallek, Vladimir Bolkhovsky, and William Oliver – MIT Lincoln Laboratory	***3. 2:20 PM - Effects of the Interlayer Thickness and Alloying on the Reliability of Transient Liquid Phase (TLP) Bonding*** Junghyun Cho and Fei Dong – Binghamton University; Liang Yin and David Shaddock – GE Global Research
Refreshment Break: 2:45 p.m. - 3:30 p.m. Bayview Pavilion		
4. 3:30 PM - Innovative Design of Crackstop Wall for 14nm Technology Node and Beyond Mohamed Rabie, Nicholas Polomoff, Md Khaled Hassan, Victoria Calero-DdelC, Danielle Degraw, Michael Hecker, Michael Thiele, and El Mehdi Bazizi – GLOBALFOUNDRIES	***4. 3:30 PM - A Novel Structure for Backside Protection Against Physical Attacks on Secure Chips or SiP*** Stephan Borel, Edouard Deschaseaux, Jean Charbonnier, L. Duperrex, Jessy Clediere, Romain Wacquez, Jacques Fournier, Jean-Charles Souriau, Gilles Simon, and Alain Merle – CEA-LETI	***4. 3:30 PM - Nano-Cu Sintering Paste for High-Power Devices Die Attach Applications*** Jinjin Zhao, Ning-Cheng Lee, Hiroshi Yamaguchi, and Min Yao – Indium Corporation
5. 3:55 PM - Back-end-of-line (BEOL) Mechanical Integrity Evaluation: A Mixed-Mode Double Cantilever Beam Test for Crackstop Strength Assessment Max Cioban, Tuhin Sinha, and Thomas Shaw – IBM Corporation	***5. 3:55 PM - Supply-Chain Security Enhancement by Chaotic Wireless Chip-Package-Board Interactive PUF*** Masanori Takahashi, Makoto Nagata, and Noriyuki Miura – Kobe University	***5. 3:55 PM - Transient Liquid Phase Sintering Using Copper-Solder-Resin Composite for High-Temperature Power Modules*** Hiroaki Tatsumi and Takeshi Monodane – Mitsubishi Electric Corporation; Adrian Lis, Yoshihiro Kashiba, and Akio Hirose – Osaka University
6. 4:20 PM - Study of the Long-Term Reliability of 3D IC under Near-Application Conditions Omar Ahmed, Golareh Jalilvand, Jessica Dieguez, and Tengfei Jiang – University of Central Florida; Peng Su – Juniper Networks	***6. 4:20 PM - Interconnect Technology Development for 180 GHz Wireless mm-Wave System-in-Foil Transceivers*** Krzysztof Nieweglowski, David Fritsche, Patrick Seiler, Sebastian Lüngen, Corrado Carta, Frank Ellinger, Dirk Plettemeier, and Karlheinz Bock – Technical University Dresden	***6. 4:20 PM - Detection of Liquefaction by DSC for Cu-Sn TLP bonding*** Sylvain Lemettre, Nathalie Isac, Sana Hammami, Seonho Seok, Johan Moulin, and Alain Bosseboeuf – C2N; Pierre Alphonse – CIRIMAT
7. 4:45 PM - The Experimental and Numerical Study of Electromigration in 2.5D Packages Jiefeng Xu, Yuling Niu, Stephen R. Cain, and S.B. Park – Binghamton University; Scott McCann, Hohyung Lee, and Gamal Refai-Ahmed – Xilinx, Inc.	***7. 4:45 PM - Long Range LiDAR Characterisation for Obstacle Detection for Use by the Visually Impaired and Blind*** Rosemary O'Keeffe, Cian O'Murchu, and Alan Mathewson – Tyndall National Institute; Salvatore Gnecchi and Steven Buckley – SensL	***7. 4:45 PM - High-Performance Metal-based Nanocomposite Thermal Interface Materials Toward Enhanced Cooling Efficiency in Electronic Applications*** Cengiz Yegin and Nirup Nagabandi – Incendium Technologies LLC; Mustafa Akbulut – Texas A&M University

Program Sessions: Thursday, May 31, 8:00 a.m. - 11:40 a.m.

Session 13: Fan-Out and Interposer Interconnections	Session 14: Advanced Substrates and Flip Chip Applications	Session 15: Warpage Control in Assembly Processes
Committee: Interconnections	**Committee: Advanced Packaging joint with Assembly & Manufacturing Technology**	**Committee: Assembly & Manufacturing Technology**
Room: Harbor Island 1	**Room: Harbor Island 2**	**Room: Harbor Island 3**
Session Co-Chairs: **Katsuyuki Sakuma – IBM Corporation** **Email: ksakuma@us.ibm.com** **Jean-Charles Souriau – CEA Leti** **Email: jcsouriau@cea.fr**	**Session Co-Chairs:** **Markus Leitgeb – AT&S** **Email: m.leitgeb@ats.net** **Steffen Kroehnert – Amkor Technology Holding B.V., Germany** **Email: steffen.kroehnert@amkor.com**	**Session Co-Chairs:** **Valerie Oberson – IBM Canada Ltd** **Email: voberson@ca.ibm.com** **Jin Yang – Intel Corporation** **Email: jin1.yang@ieee.org**
1. 8:00 AM - Chip Stackable, Ultra-Thin, High-Flexibility 3D FOWLP (3D SWIFT(R) Technology) for Hetero-integrated Advanced 3D WL-SiP WonMyoung Ki, WonGeol Lee, IlBok Lee, InSu Mok, WonChul Do, Curtis Zwenger, Moh Kolbehdari, Alex Copia,Suresh Jayaraman, and KangWook Lee – Amkor Technology, Inc.	***1. 8:00 AM - 2.5D Glass Panel Embedded (GPE) Packages with Better I/O Density, Performance, Cost and Reliability than Current Silicon Interposers and High-Density Fan-Out Packages*** Giback Park, Han-Wen Chen – Applied Materials Inc.; Siddharth Ravichandran, Tailong Shi, Fuhan Liu, Vanessa Smet, Venky Sundaram, Tailong Shi, Chintan Buch, and Rao Tummala – Georgia Institute of Technology; Shuhei Yamada – Murata Manufacturing Co., Ltd.	***1. 8:00 AM - Reduce the Wafer Warpage Introduced by Cu in RDL Through Adjusting the Cooling Temperatures*** Gong Cheng, Gaowei Xu, Wei Gai, and Le Luo – Shanghai Institute of Microsystem and Information Technology
2. 8:25 AM - High-Performance, High-Density RDL for Advanced Packaging Chun Hui Yu, L. J. Yen, C. Y. Hsieh, C. H. Hsieh, C. S. Liu, KC Yee, C. T. Wang, Victor C. Y. Chang, J. S. Hsieh, and Doug C. H. Yu – Taiwan Semiconductor Manufacturing Company	***2. 8:25 AM - Analysis of Warpage and Stress Behavior in a Fine Pitch Multi-Chip Interconnection with Ultrafine-Line Organic Substrate (2.1D)*** Chen-Yu Huang, Yuan-Hung Hsu, Ying-Ju Lu, Kuo-Hua Yu, Wen-Shan Tsai, Chang-Fu Lin, and C. Key Chung – Siliconware Precision Industries Co., Ltd.	***2. 8:25 AM - Ultra-Thin 50 µm Fan-Out Wafer Level Package: Development of an Innovative Assembly and De-Bonding Concept*** Markus Woehrmann, Tanja Braun, Kai Zoschke, and Michael Toepper – Fraunhofer IZM; Klaus-Dieter Lang – Technical University Berlin
3. 8:50 AM - Warpage Measurements and Characterizations of Fan-Out Wafer-Level Packaging (FOWLP) with Large Chips and Multiple Re-Distributed Layers (RDLs) J. Lau, M. Li, M. Li, K. Janadhanan, W. Kai, N. Fan and E. Kuah - ASM Pacific Technology; I. Xu, T. Chen, Z. Li and K.H. Tan – JCAP; R. Beica - The Dow Chemical Company; Q.X. Yong and C. Xi - Huawei Technologies Co. Ltd.; S. Chen and W. Bao - Disco Hi-Tec China Co. Ltd.	***3. 8:50 AM - A Novel Application of Chemical Mechanical Polishing for Panel Level Organic and Glass Substrate*** Shyh-Lian Cheng, Wei-Chun Chen, Yu Hua Chen, Puru Lin, and Cheng-Ta Ko – Unimicron Technology Corp.	***3. 8:50 AM - Design Guideline of 2.5D Package with Emphasis on Warpage Control and Thermal Management*** Jisun Hong and Kyongsei Cho – Samsung Electronics Company, Ltd.; Seungbae Park, Shuai Shao, Yuling Niu, Huayan Wang, and Van Lai Pham – Binghamton University
Refreshment Break: 9:15 a.m. - 10:00 a.m. Bayview Pavilion		
4. 10:00 AM - Development of Novel Fine Line 2.1 D Package with Organic Interposer Using Advanced Substrate-based Process Weii-Chung Chen, Chiu-Wen Lee, Min-Hua Chung, Chaung-Chi Wang, Shang-Kun Huang, Yen-Sen Liao, Hung-Chun Kuo, and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.	***4. 10:00 AM - Various Chip Attach Evaluations in a Fine Bump Pitch and Substrate Flip-Chip Package*** Chi-Yuan Chen, Ian Hsu, and Stanley Lin – MediaTek, Inc.; KeonTaek Kang and Ming-Che Hsieh – STATS ChipPAC Pte. Ltd.	***4. 10:00 AM - Stacking Yield Prediction of Package-on-Package Considering the Statistical Distributions of Top/Bottom Package Warpages and Solder Ball Heights*** Hsiu-Ping Wei and Bongtae Han – University of Maryland
5. 10:25 AM - Micro Bump System for 2nd Generation Silicon Interposer with GPU and High Bandwidth Memory (HBM) Concurrent Integration Jaesik Lee, Chun Yang Lee, Chongho Kim, and Shantanu Kalchuri – Nvidia Corporation	***5. 10:25 AM - The Effect of the SnAg Solder Joint Morphology on the Thermal Cycle Reliability of 40 µm Fine-Pitch Cu-pillar/ SnAg Micro Bump Interconnection*** SeYong Lee, HanMin Lee, JongHo Park, SangMyung Shin, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Woojeong Kim and Taejin Choi – Doosan Corporation Electro-Materials BG	***5. 10:25 AM - Warpage Control During Mass Reflow Flip-Chip Assembly Using Temporary Adhesive Bonding*** Normand-Pierre Goodhue, David Danovitch, and Jeff Moussodji – Université de Sherbrooke; Benoit Papineau and Eric Duschesne – IBM Corporation
6. 10:50 AM - Low-Cost Panel-Based 1-2 Micron RDL Technology with Lower Resistance than Si BEOL for Large Packages Fuhan Liu, Rui Zhang, Bartlet DeProspo, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Hirokaza Ito – JSR Corporation	***6. 10:50 AM - Chip-Package Interaction Challenges for Large Die Applications*** Z. Wu, C. Carey, S. Donavan, D. Hunt, P. Justison, T. Anemikos and J. Cincotta – GLOBALFOUNDRIES; H. Gagnon, O. Chacon, R. Martel and T. Wassick – IBM Corporation	***6. 10:50 AM - Fabrication and Characterization of Epoxy Molding Films (EMFs) for Wafer-Level and Panel-Level and Fan-Out Packages*** JongHo Park, HanMin Lee, SeYong Lee, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Youjin Kyung, Jung Hak Kim, and Kwangjoo Lee – LG Chem R&D Center
7. 11:15 AM - Advanced Anodic Aluminum Oxide Interposer Fabrication and 3D Embedded Inductors Hsiang Yu Chan, Mark Bachman, and Guann Pyng Li – University of California, Irvine	***7. 11:15 AM - Injection of Molten Solder (IMS) Technology for Solder Bumping on Wafers, Ceramic/Organic/Flexible Substrates, and Si via Filling from Fine Pitch to Large Pitch*** Jae-Woong Nah, Li-Wen Hung, Paul Andry, and John Knickerbocker – IBM Corporation	***7. 11:15 AM - Determination of a Meaningful Warpage Acceptance Criterion for Large PBGA Components Through the Correlation with Scattering in Material Properties*** Qiming Zhang, Jeffery C. C. Lo, and S. W. Ricky Lee – The Hong Kong University of Science & Technology; Wei Xu – Huawei Technologies Co., Ltd.

Program Sessions: Thursday, May 31, 8:00 a.m. - 11:40 a.m.

Session 16: Advances in Interconnect Reliability and Techniques	Session 17: Technology Advances in Nano, Biochemical, Thermal and Flexible Applications	Session 18: Silicon Photonics
Committee: Applied Reliability	**Committee: Emerging Technologies**	**Committee: Optoelectronics**
Room: Nautilus 1 & 2	**Room: Nautilus 3 & 4**	**Room: Nautilus 5**
Session Co-Chairs: **S. B. Park – Binghamton University** **Email: sbpark@binghamton.edu** **Tz-Cheng Chiu – National Cheng Kung University** **Email: tcchiu@mail.ncku.edu.tw**	**Session Co-Chairs:** **Hongqing Zhang – IBM Corporation** **Email: zhangh@us.ibm.com** **Ajit Dubey – GLOBALFOUNDRIES** **Email: ajitmdubey@gmail.com**	**Session Co-Chairs:** **Takaaki Ishigure – Keio University** **Email: ishigure@appi.keio.ac.jp** **Soon Jang – ficonTEC USA** **Email: soon.jang@ficontec.com**
1. 8:00 AM - Reliability of Copper, Gold, Silver, and PCC Wirebonds Subjected to Harsh Environment Pradeep Lall and Shantanu Deshpande – Auburn University; Luu Nguyen – Texas Instruments, Inc.	***1. 8:00 AM - Development of Integrated Thermistor Sensor and Heating Electrode for Renal Denervation Procedure*** Ruiqi Lim, Ming-Yuan Cheng, Weiguo Chen, David Sze Wai Choong, and Yuandong Gu – Institute of Microelectronics; Sebastian Song, Jae Hyung Park, Jung Soo Oh, and Eul Joon Park – Handok Kalos Medical Inc.	***1. 8:00 AM - Backside Optical I/O Module for Si Photonics Integrated with Electrical ICs Using Fan-Out Wafer-Level Packaging Technology*** Hiroshi Uemura, Kaori Warabi, Kazuya Ohira, Yoichiro Kurita, Haruhiko Yoshida, and Hideto Furuyama – Photonics Electronics Technology Research Association; Yoshiaki Sugizaki and Hideki Shibata – Toshiba Corporation
2. 8:25 AM - Study of Interface Micro-Voids Between Sputter Cu & Plating Cu: The Role of Photoresist Y. B. Ou, T. L. Yang, W. C. Wu, B. T. Chen, K. Y. Lee, H. L. Huang, C. S. Liu, P. Pang, E. Chen, K.C. Liu, M. Liao and H. Ku – Taiwan Semiconductor Manufacturing Company	***2. 8:25 AM - Nanomembrane Hybrid Electronics for Wireless Detection of Sourness and Saltiness Toward an Artificial Taste System*** Yongkuk Lee, Yun Soung Kim, Musa Mahmood, Wong-Hong Yeo, and Saswat Mishra – Georgia Institute of Technology	***2. 8:25 AM - Single Mode Optical Coupling Technology Using Movable Micro-Mirror Array and Surface Emitting DFB Laser Array for High-Density 3-D Integration*** Takanori Suzuki, Koichiro Adachi, Yasunobu Matsuoka, and Shigehisa Tanaka – Oclaro Japan, Inc.
3. 8:50 AM - Prediction of Statistical Distribution of Vibration-induced Solder Fatigue Failure Considering Intrinsic Variations of Mechanical Properties of Anisotropic Sn-rich Solder Alloys Bulong Wu, Hsiu Ping Wei, Yu-Hsiang Yang, and Bongtae Han – University of Maryland	***3. 8:50 AM - Cost-Efficient Formation of Flexible Pressure Sensor with Micropillar Arrays by Metal-Assisted Chemical Etching for Wearable Electronic Skin*** Yougen Hu, Xinyu Zhang, Pengli Zhu, Tao Zhao, Yuan Zhang, and Rong Sun – Shenzhen Institutes of Advanced Technology; Ching-Ping Wong – The Chinese University of Hong Kong	***3. 8:50 AM - 3D System-on-Packaging Using Through Silicon Via on SOI for High-Speed Optical Interconnections with Silicon Photonics Devices for Application of 400 Gbps and Beyond*** Do-Won Kim, Hong Yu Li, Ka Fai Chang, Woon Leng Loh, Ser Choong Chong, Hong Cai, and Surya Bhattacharya – Institute of Microelectronics, A*STAR
Refreshment Break: 9:15 a.m. - 10:00 a.m. Bayview Pavilion		
4. 10:00 AM - Experimental Strain Energy Densities Dissipated in SAC305 Solder Joints During Different Thermal Cycling Conditions Using Strain Gages Measurements Jean-Baptiste Libot, Philippe Milési, and Frédéric Dulondel – Safran Electronics & Defense; Joël Alexis, Lionel Arnaud, and Olivier Dalverny – University of Toulouse - INP/ENIT	***4. 10:00 AM - A Harmonic RF Phase-Shifter Based Wireless pH Sensor*** Saikat Mondal, Deepak Kumar, Saranraj Karuppuswami, and Prem Chahal – Michigan State University	***4. 10:00 AM - Broadband, Polarization-Insensitive Lensed Edge Couplers for Silicon Photonics*** Bradley Snyder, Guy Lepage, Sadhishkumar Balakrishnan, Peter Verheyen, Marianna Pantouvaki, Philippe Absil, and Joris Van Campenhout – IMEC
5. 10:25 AM - Understanding the Impact of PCB-Changes in the Latest Published JEDEC Board Level Drop Test Method Varun Thukral, Jeroen Zaal, Romuald Roucou, Jeroen Jalink, and Rene Rongen – NXP Semiconductors	***5. 10:25 AM - Integration of Chip-Scale SERF Atomic Magnetometers for Magnetoencephalography Measurement*** Guoliang Li, Jintang Shang, Yu Ji, Lin Lu, and Zhihua Pan – Southeast University	***5. 10:25 AM - 400 Gbps 2-Dimensional Optical Receiver Assembled on Wet Etched Silicon Interposer*** Chenhui Li, Ripalta Stabile, Teng Li, Finn Kraemer, and Oded Raz – Eindhoven University of Technology
6. 10:50 AM - Non-destructive Inspection of Flip-Chip BGA Solder Ball Defects Using Two Laser Beam Probe Ultrasonic Inspection Technique Chidinma Imediegwu, Vishnu Reddy, Charles Ume, and Aaron Mebane – Georgia Institute of Technology; Kola Akinade, Amiya Chaudhuri, Bryan Rogers, Mark Hill, and Cherif Guirguis – Cisco Systems, Inc.; Tae-Kyu Lee – Portland State University	***6. 10:50 AM - Cu-In Fine-Pitch-Interconnects with Enhanced Shear Strength*** Steffen Bickel, Robert Höhne, and Joerg Meyer – Technical University Dresden; Iuliana Panchenko and M. Juergen Wolf – Fraunhofer IZM-ASSID	***6. 10:50 AM - EOCB-Platform for Integrated Photonic Chips Direct-on-Board Assembly within Tb/s Applications*** Tobias Lamprecht and Felix Betschon – Vario-Optics AG; Alex Bruderer and Romeo Premerlani – Varioprint AG; Joris Lambrecht and Hannes Ramon – IDLab, Ghent University-IMEC; Xin Yin – Ghent University-IMEC
7. 11:15 AM - Enhanced Design and Reliability Analysis of Copper Post Wafer-Level Package Kuei Hsiao Kuo, Austin Chen, Yen Neng Wang, Jiunn Jie Wang, Jovi Chang, Feng Lung Chien, and Rick Lee – Siliconware Precision Industries Co. Ltd.	***7. 11:15 AM - Study of Wearables with Embedded Electronics through Experiments and Simulations*** Joseph May, Christopher May, Justin Chow, and Suresh Sitaraman – Georgia Institute of Technology	***7. 11:15 AM - Integrated Multi-Wavelength Laser Source for Sensing*** G. Paré-Olivier, S. Ayotte, F. Costin, A. Babin, M. Morin, B. Filion, K. Bédard, B. Ghislain, E. Girard-Deschênes, P. Chrétien, L. P. Perron, C. A. Davidson, D. D'amato, M. Laplante and J. Blanchet-Létourneau - TeraXio

Program Sessions: Thursday, May 31, 1:30 p.m. - 5:10 p.m.

Session 19: Interconnect Reliability	Session 20: MEMS, Sensor, IoT and Flex	Session 21: Materials and Process Trends for Fan-Out Wafer-Level Packaging
Committee: Interconnections joint with Applied Reliability	**Committee: Advanced Packaging**	**Committee: Materials & Processing**
Room: Harbor Island 1	**Room: Harbor Island 2**	**Room: Harbor Island 3**
Session Co-Chairs: **Chuan Seng Tan – Nanyang Technological University** **Email: tancs@alum.mit.edu** **Keith Newman – AMD** **Email: keith.newman@amd.com**	**Session Co-Chairs:** **Joseph W. Soucy – Draper Laboratory** **Email: jsoucy@draper.com** **Allyson Hartzell – Veryst Engineering** **Email: AHartzell@veryst.com**	**Session Co-Chairs:** **Kimberly Yess – Brewer Science** **Email: kyess@brewerscience.com** **Tanja Braun – Fraunhofer IZM** **Email: tanja.braun@izm.fraunhofer.de**
1. 1:30 PM - Characterization of Material Damage and Microstructural Evolution Occurring in Lead-Free Solders Subjected to Cyclic Loading Md Mahmudur Chowdhury, Mohd Aminul Hoque, Nianjun Fu, Jeffrey Suhling, Sa'd Hamasha, and Pradeep Lall – Auburn University	***1. 1:30 PM - Development of a High-Resolution Magnetic Field Position Sensor System Based on a Through Silicon Via First Integration Concept*** Kai Zoschke and Hermann Oppermann – Fraunhofer IZM; Johannes Paul, Heiko Knoll, and Franz-Josef Braun – Sensitec GmbH; Monika Saumer and Martin Theis – University of Applied Sciences Kaiserslautern; Peter Frank – Sandvik; Andreas Lenkl and Fabian Klose	***1. 1:30 PM - Warpage Control of Liquid Molding Compound for Fan-Out Wafer-Level Package*** Yosuke Oi, Yasuhito Fujii, Takashi Hiraoka, Yukio Yada, and Katsushi Kan – Nagase ChemteX Corporation
2. 1:55 PM - Effects of Au and Pd in Pad Surface Finish on Electro-Migration of Flip Chip Interconnection Between Cu-Pillar and Sn-Bi Solder Alloy System Kei Murayama, Mitsuhiro Aizawa, and Kiyoshi Oi – Shinko Electric Industries Company, Limited	***2. 1:55 PM - High Dielectric Constant Molding Compounds for Fingerprint Sensor Packages*** Tom Tang, Kelly Chen, Kevin Yeh, Terry Tsai, Max Lu, Jensen Tsai, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.	***2. 1:55 PM - Warpage Analysis with Newly Molding Material of Fan-Out Panel-Level Package and the Board Level Reliability Test Results*** Kazuhiro Kikuchi, Yuusuke Nedzu, and Takashi Sugino – Lintec Corporation
3. 2:20 PM - The Stress State of BGA Solder Joints Influenced by the Grain Orientations of Neighboring Joints Andreas Lövberg and Per-Erik Tegehall – Swerea IVF AB	***3. 2:20 PM - Concept for Using MID Technology for Advanced Packaging*** Marc Wurz, Sebastian Bengsch, Ing Wurz, and Sebastian Beringer – Institute of Micro Production Technology; Bernd Roesener – LPKF Laser & Electronics AG	***3. 2:20 PM - The Impact of Thermal Shrinkage of Glass Carriers on Achieving Fine-Pitch Wiring through Fan-Out WLP/PLP Process*** Shuhei Nomura and Kazutaka Hayashi – Asahi Glass Co., Ltd.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Bayview Pavilion		
4. 3:30 PM - Microstructure Evolution of Cu/In/Cu Joints after Solid-Liquid Interdiffusion Yu Shan Chiu and C. Robert Kao – National Taiwan University	***4. 3:30 PM - Chipless RFID with Fully Inkjet Printed Tag: A Practical Case Study for Low-Cost Smart Packaging Applications*** Jarrid Wittkopf, Ning Ge, Robert Ionescu, Doug Pederson, Wagston Staehler, and Helen Holder – Hewlett Packard Inc.	***4. 3:30 PM - Advances in Temporary Bonding and Release Technology for Ultrathin Substrate Processing and High-Density Fan-Out Device Build-Up*** Alain Phommahaxay, Arnita Podpod, John Slabbekoorn, Erik Sleeckx, Gerald Beyer, and Eric Beyne – IMEC; Alice Guerrero, Dongshun Bai, and Kim Arnold – Brewer Science
5. 3:55 PM - Isothermal Fatigue of Interconnections in Flexible Hybrid Electronics Based Human Performance Monitors R. Sivasubramony, N. Adams, M. Alhendi, G. S. Khinda, M. Z. Kokash, J. P. Lombardi, A. Raj, S. Thekkut, D. L. Weerawarne, M. Yadav, A. V. Zachariah, M. D. Poliks and P. Borgesen – Binghamton University; N. C. Stoffel, D. M. Shaddock and L. Yin – GE Global Research	***5. 3:55 PM - Low Temperature Solder Attach of SnAgCu Bumped Components for a Flexible Hybrid Electronics Based Medical Monitor*** Thaer Alghoul, Manu Yadav, Sanoop Thekkut, Rajesh Sivasubramony, Christopher Greene, Mark Poliks, and Peter Borgesen – Binghamton University; Luke Wentlent and Michael Meilunas – Universal Instruments; Nancy Stoffel, David Shaddock and Liang Yin – GE Global Research	***5. 3:55 PM - Novel Microwave Process for RDL Photosensitive Dielectric Polymer Curing on FOWLP Reconstructed Wafer*** Kazunori Yamamoto, Chun-Mei Wang, and Xiang-Yu Wang – Institute of Microelectronics; Tuck-Foong Koh and Felix Deng – Applied Materials
6. 4:20 PM - Board Level Reliability Investigation of Fan-Out Wafer Level Package Stephen Hou, K. H. Tsai, M. F. Wu, M. F. Ku, P. H. Tsao, and L. H. Chu – Taiwan Semiconductor Manufacturing Company	***6. 4:20 PM - Mechanical Strength Characterization of Direct Bond Interfaces for 3D-IC and MEMS Applications*** B. Lee, R. Katkar, G. Gao, G. Fountain, S. Lee, L. Wang, C. Mandalapu, C. Uzoh and L. Mirkarimi – Xperi; B. Sykes and M. Litjens – Xyztec; Y. Niu, S. Shao, J. Wang and S. Park – Binghamton University	***6. 4:20 PM - Fabrication of Fine Via and Line / Space in Low CTE Film for Panel Fan-Out Using a Dry Etching Technology*** Muneyuki Sato, Takahide Murayama, Tetsushi Fujinaga, and Yasuhiro Morikawa – ULVAC, Inc.
7. 4:45 PM - Multi-Axis Loading Impact on Thermo-Mechanical Stress-Induced Damage on WLCSP and Components with Via-in Pad Plated Over (VIPPO) Board Design configuration Andy Hsiao, Tae-Kyu Lee and Mohamed Sheikh – Portland State University; Weidong Xie and Steven Perng – Cisco Systems, Inc.; Edward Ibe and Karl Loh – Zymet	***7. 4:45 PM - Study on an Improved Wafer-Level Fabrication Process to Achieve Size Uniformity for Micro Glass Shell Resonators*** Zhaoxi Su, Jintang Shang, and Bin Luo – Southeast University; Ching-Ping Wong – The Chinese University of Hong Kong	***7. 4:45 PM - Reliability Studies of Excimer Laser-Ablated Microvias Below 5 Micron Diameter in Dry Film Polymer Dielectrics for Next Generation, Panel-Scale 2.5D Interposer RDL*** Chandrasekharan Nair, Bartlet DeProspo, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Habib Hichri and Markus Arendt – SUSS Microtec Photonic Systems, Inc.

Program Sessions: Thursday, May 31, 1:30 p.m. - 5:10 p.m.

Session 22: Thermal Mechanical Modeling and Characterization	Session 23: RF and THz Module Components	Session 24: Optical Module Integration
Committee: Thermal/Mechanical Simulation & Characterization	**Committee: High-Speed, Wireless & Components**	**Committee: Optoelectronics**
Room: Nautilus 1 & 2	**Room: Nautilus 3 & 4**	**Room: Nautilus 5**
Session Co-Chairs: **Pradeep Lall– Auburn University** **Email: lall@auburn.edu** **Yong Liu – ON Semiconductor** **Email: Yong.Liu@onsemi.com**	**Session Co-Chairs:** **Craig Gaw – NXP Semiconductor** **Email: c.a.gaw@ieee.org** **Amit P. Agrawal – Microsemi Corporation** **Email: amit.agrawal@microsemi.com**	**Session Co-Chairs:** **Hiren Thacker – Tech301** **Email: hiren@tech301.com** **Ajey Jacob – GLOBALFOUNDRIES** **Email: ajey.jacob@globalfoundries.com**
1. 1:30 PM - Seal Ring Toughness Characterization by Numerical and Experimental Approaches Idir Raid, Sébastien Gallois-Garreignot, and Vincent Coutellier – STMicroelectronics; Rafael Estevez – SIMaP	***1. 1:30 PM - Package Co-Design of a Fully Integrated Multimode 76-81GHz 45nm RFCMOS FMCW Automotive Radar Transceiver*** Minhong Mi, Jie Chen, Meysam Moallem, Ming Li, and Rajen Murugan – Texas Instruments, Inc.	***1. 1:30 PM - Direct Fabrication for Polymer Optical Waveguide in PMT Ferrule Using the Mosquito Method*** Takaaki Ishigure, Hikaru Masuda, Chinami Marushima, Kumi Date, and Tadayuki Enomoto – Keio University
2. 1:55 PM - Reliability Life Assessment of WLCSP Using Different Creep Models K. N. Chiang, V. Ramachandran, K. C. Wu, and C. C. Lee – NTHU	***2. 1:55 PM - Embedded Active Elements in 3D Printed Structures for the Design of RF Circuits*** Mohd Ifwat Mohd Ghazali, Saikat Mondal, Saranraj Karuppuswami, and Premjeet Chahal – Michigan State University	***2. 1:55 PM - Solder-Reflowable, High-Throughput Fiber Assembly Achieved by Partitioning of Adhesive Functions*** Alexander Janta-Polczynski, Elaine Cyr, Richard Langlois, Paul Fortier, Yoichi Taira, Nicolas Boyer, and Tymon Barwicz – IBM Corporation
3. 2:20 PM - On the Uniqueness and Sensitivity of Nanoindentation Testing for Determining the Elastic and Plastic Material Properties of Electroplating Copper Filled in Through-Silicon-Via (TSV) Liangbiao Chen and Yong Liu – On Semiconductor; Fei Qin – Beijing University of Technology; Mahmound El Barbary and Xuejun Fan – Lamar University	***3. 2:20 PM - Miniaturized High-Performance Filters for 5G Small-Cell Applications*** Muhammad Ali, Atom Watanabe, Markondeya Raj Pulugurtha, Venkatesh Sundaram, Manos M. Tentzeris, Fuhan Liu, and Rao R. Tummala – Georgia Institute of Technology	***3. 2:20 PM - Low Reflectance and Reflowable Thermoplastic Optical Lens Without AR Coating*** Takuro Watanabe, Sho Yakabe, and Takayuki Shimazu – Sumitomo Electric Industries, Ltd.; Ryohei Hokari and Kazuma Kurihara – National Institute of Advanced Industrial Science and Technology; Shouhei Okabe – Sumitomo Electric Fine Polymer, Inc.
Refreshment Break: 2:45 p.m. - 3:30 p.m. Bayview Pavilion		
4. 3:30 PM - Co-Design for Extreme Large Package Solution with Embedded Fine Pitch Interposer (EFI) Technology Faxing Che, David Ho, and T. C. Chai – Institute of Microelectronics	***4. 3:30 PM - 3D-IPD with High Aspect Ratio Cu Pillar Inductor*** Cheng-Yuan Kung, Chien-Hua Chen, Teck Chong Lee, Hung-Yi Lin, Shiuan-Yu Lin, Yu-Chang Hsieh, Pao-Nan Lee, and Chen-Chao Wang – Advanced Semiconductor Engineering Group	***4. 3:30 PM - Wide Range 2D InP Chip-to-Fiber Alignment Through Bimorph Piezoelectric Actuators*** Simone Cardarelli, Nicola Calabretta, Ripalta Stabile, and Kevin Williams – Technical University Eindhoven; Xiao Luo and Jan Mink – Vtec
5. 3:55 PM - Study of Polyimide in Chip Package Interaction for Flip-Chip Cu-Pillar Package Wei Wang, Dingyou Zhang, Yangyang Sun, David Rae, Lily Zhao, Jiantao Zheng, Mark Schwarz, Milind Shah, and Ahmer Syed – Qualcomm, Inc.	***5. 3:55 PM - Ultra-Compact, High-Performance, 3D-IPD Integrated Using Conformal 3D Interconnects*** Ayad Ghannam, Alessandro Magnani, David Bourrier, and Thierry Parra – 3DiS Technologies S.A.S.	***5. 3:55 PM - Co-integration of High-Bandwidth Photonic and Electronic RDL on 2.5D Glass Interposers Using Low Optical Absorption Photoimageable Dielectric Polymer*** Rui Zhang, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology; Michael Gallagher and Ed Anzures – Dow Chemical Company
6. 4:20 PM - A Study of Organic Chip Carrier Fatigue Cracking Shidong Li, Sushumna Iruvanti, Kamal Sikka, and Rui Wang – IBM Corporation	***6. 4:20 PM - Glass in Electronic Packaging and Integration: High Q Inductances for 2.35 GHz Impedance Matching in 0.05 mm Thin Glass Substrates*** Martin Letz and Matthias Jotz – SCHOTT AG; Zihan Wu, Sukhadha Viswanathan, P Markondeya Raj, Venkatesh Sundaram, and Rao Tummala – Georgia Institute of Technology; Holger Maune and Matthias Jost – Technical University of Darmstadt, IMP	***6. 4:20 PM - Thin Glass Based Optical Sub-Assemblies For Embedding in Electronic Systems*** Wojciech Lewoczko-Adamczyk, Gunnar Böttger, Henning Schröder, Klaus-Dieter Lang, and Martin Schneider-Ramelow – Fraunhofer Institute for Reliability and Microintegration
7. 4:45 PM - Developments for Highly Reliable Electronics – Experiments on Combined Thermal and Vibration Loading Karsten Meier and Karlheinz Bock – Technical University Dresden; Mike Roellig – Fraunhofer IKTS	***7. 4:45 PM - Through Glass Via (TGV) Based Band Pass Filter for 5G Communications*** Renuka Bowrothu and Yong-Kyu Yoon – University of Florida; Jay Zhang – Corning, Inc.	***7. 4:45 PM - Integration of Ball Lens in Through-Package Via to Enable Photonic Chip-to-Board Coupling*** Nivesh Mangal, Jeroen Missinne, and Geert Van Steenberge – Ghent University/IMEC; Joris Van Campenhout and Brad Snyder – IMEC

Program Sessions: Friday, June 1, 8:00 a.m. - 11:40 a.m.

Session 25: Fabrication and Characterization of TSV	Session 26: Wafer-Level Packaging Fan-In and Fan-Out Key Developments	Session 27: Automotive and Power Electronics
Committee: Interconnections	**Committee: Assembly & Manufacturing Technology joint with Advanced Packaging**	**Committee: Advanced Packaging**
Room: Harbor Island 1	**Room: Harbor Island 2**	**Room: Harbor Island 3**
Session Co-Chairs: **Dingyou Zhang – Qualcomm Technologies, Inc.** **Email: zhangdingyou04@gmail.com** **Wei-Chung Lo – ITRI** **Email: lo@itri.org.tw**	**Session Co-Chairs:** **Jan Vardaman – Techsearch International** **Email: jan@techsearchinc.com** **Andrew Kim – Intel Corporation** **Email: hyoung.il.kim@intel.com**	**Session Co-Chairs:** **Young-Gon Kim – Integrated Device Technology, Inc.** **Email: young.kim@idt.com** **Subhash L. Shinde – Notre Dame University** **Email: sshinde@nd.edu**
1. 8:00 AM - Low-Cost, Self-Formed Vertical Nanowires with Aspect Ratio > 100x in Deep Si-Trenches for Future 3D-LSI/IC Applications Murugesan Mariappan, Takafumi Fukushima, JiChel Bea, Hiroyuki Hashimoto, and Mitsumasa Koyanagi – Tohoku University	***1. 8:00 AM - Development of WLCSP for Accelerometer Packaging with Vertical CuPd Wire as Through Mold Interconnection (TMI)*** Zhaohui Chen, Boon Long Lau, Zhipeng Ding, Eva Leong Ching Wai, Beibei Han, Lin Bu, Hyun-Kee Chang and Tai Chong Chai – Institute of Microelectronics - A*STAR	***1. 8:00 AM - Embedded Components for High-Temperature Automotive Applications*** Stephanie Groß, Bernhard Schuch, and Wolfgang Grübl – Continental
2. 8:25 AM - First Demonstration of Silicon-Like >250 I/O per mm per layer Multilayer RDL on Glass Panel Interposers by Embedded Photo-Trench and Fly Cut Planarization Bartlet DeProspo, Fuhan Liu, Venkatesh Sundaram, Chandra Nair, and Rao Tummala – Georgia Institute of Technology; Frank Wei and Ye Chen – Disco Corporation; Atsushi Kubo – TOK	***2. 8:25 AM - Fan-Out Package: Performance and Scalability Perspective*** Jong Heon Kim, Yong Tae Kwon, Yong Ho Kwon, Yong Woon Yeo, Young Mo Lee, Yoon Mook Park, Eung Ju Lee, Jun Kyu Lee and Nam Chul Kim – Nepes Corporation; Sangdon Lee, Seongwook Choi and Yoonyoung Bae – Giparang, Inc.; Young June Park – Seoul National University	***2. 8:25 AM - New Failure Mechanism in High-Temperature Resin Materials*** Michael Guyenot, D. Maas, and Roumen Ratchev – Robert Bosch GmbH; Ali Khoshamouz and Thomas Gottwald – Schweizer Electronic AG; Sascha Kreuer – Isola Group
3. 8:50 AM - Dielectric Quality of 3D Capacitor Embedded in Through-Silicon Via (TSV) Ye Lin and Chuan Seng Tan – Nanyang Technological University	***3. 8:50 AM - Board Level Reliability Enhancement of WLCSP with Large Chip Size*** Pei-Haw Tsao, T. H. Lu, T. M. Chen, K. C. Chang, C. M. Kuo, M. J. Lii, and L. H. Chu – Taiwan Semiconductor Manufacturing Company	***3. 8:50 AM - Next Generation of Automotive Radar with Leading-Edge Advances in SiGe Devices and Glass Panel Fan-Out Packaging*** Tailong Shui, Yunyi Gong, Siddharth Ravichandran, Venky Sundaram, John D. Cressler, and Rao Tummala – Georgia Institute of Technology
Refreshment Break: 9:15 a.m. - 10:00 a.m. Harbor Island Foyer & Nautilus Foyer		
4. 10:00 AM - Experimental Assessment and Analysis of the Influence of Radiation on Through-Silicon Vias Qinghua Zeng, Jing Chen, and Yufeng Jin – Peking University	***4. 10:00 AM - Controlling Underfill Lateral Flow to Improve Component Density in Heterogeneously Integrated Packaging Systems*** Christophe Faucher-Courchesne and David Danovitch – Université de Sherbrooke; Lise Brault, Marie-Claude Paquet, and Eric Turcotte – IBM Corporation	***4. 10:00 AM - Solderless Leadframe Assisted Wafer-Level Packaging Technology for Power Electronics*** Kremena Vladimirova and Julie Widiez – CEA-LETI; Jean-Christophe Crebier – CNRS-G2ELab; Bastien Letowski, Pierre Perreau, Gregory Enyedi, Perceval Coudrain and Nicolas Rouger - University Grenoble Alpes
5. 10:25 AM - Co-Deposition of Nano-Size SiC particles in Micro-Via Houya Wu, Yan Wang, Fuliang Wang, Zhuo Chen, Hu He, and Liancheng Wang – Central South University	***5. 10:25 AM - Dual-Carrier Process using Mechanical and Laser Release Technologies for Advanced Wafer-Level Packaging*** Michelle Fowler, Ram Trichur, John Massey, and Matt Koch – Brewer Science	***5. 10:25 AM - Material Characterization of Advanced Cement-Based Encapsulation Systems for Efficient Power Electronics With Increased Power Density*** B. Boettge, F. Naumann, S. Klengel and M. Petzold - Fraunhofer Institute for Microstructure of Materials and Systems IMWS; S. Behrendt and R. Eisele - FuE-Zentrum Fachhochschule Kiel GmbH; M. G. Scheibel and A. Z. Miric - Heraeus Deutschland GmbH & Co. KG; S. Kaessner, G. Hejtmann - Robert Bosch GmbH; and K. G. Nickel - University of Tuebingen
6. 10:50 AM - A Study of Crystal Orientation of Solder TSVs Yuki Ohara, Yuki Inagaki, Atsushi Mizutani, and Kazushi Asami – DENSO Corporation	***6. 10:50 AM - Optimization of Electrodeposited Copper for Sub 5 µm L/S RDL Lines by Plating Additives*** Ralf Schmidt and T. Beck – Atotech Deutschland GmbH; R. Rooney and A. Gewirth – University of Illinois	***6. 10:50 AM - Mechanism of Ultrasonic-Assisted Sintering of Cu@Ag NPs Paste in Air for High-Temperature Power Device Packaging*** Hongjun Ji and Mingyu Li – Harbin Institute of Technology (Shenzhen)
7. 11:15 AM - Characterization of Optical End-point Detection for Via Reveal Processing Anne Jourdain, Nina Tutunjyan, Joeri DeVos, Stefano Sardo, Daniele Piumi, Andy Miller, Eric Beyne and Nouredine Rassoul – IMEC; Edward Walsby, Huma Ashraf and Dave Thomas – SPTS Technologies	***7. 11:15 AM - UBM/RDL Deposition by PVD for FOWLP in High Volume Production*** Chris Jones, Tony Wilby, Paul Densley, and Stephen Burgess – SPTS Technologies Ltd.	***7. 11:15 AM - Design Consideration of a 3D Stacked Power Supply on Chip*** Kota Ono, Kengo Hiura, and Satoshi Matsumoto – Kyushu Institute of Technology

Program Sessions: Friday, June 1, 8:00 a.m. - 11:40 a.m.

Session 28: High-Speed and High-Bandwidth Packaging	Session 29: Modeling of Power Electronics	Session 30: Emerging Materials and Technologies
Committee: High-Speed, Wireless & Components	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: Materials & Processing**
Room: Nautilus 1 & 2	**Room: Nautilus 3 & 4**	**Room: Nautilus 5**
Session Co-Chairs: **Rockwell Hsu – Cisco Systems, Inc.** **Email: rohsu@cisco.com** **Zhaoqing Chen – IBM Corporation** **Email: zhaoqing@us.ibm.com**	**Session Co-Chairs:** **Ning Ye – Western Digital** **Email: ning.ye@wdc.com** **Xuejun Fan – Lamar University** **Email: xuejun.fan@lamar.edu**	**Session Co-Chairs:** **Bing Dang – IBM Research** **Email: dangbing@us.ibm.com** **Lewis Huang – Senju Electronic** **Email: lewis@senju.com.tw**
1. 8:00 AM - Electrical Characterization of High Performance Fine Pitch Interconnects in Silicon Interconnect Fabric SivaChandra Jangam, Adeel Ahmed Bajwa, Kannan Kalappurakal Thankappan, Premsagar Kittur, and Subramanian Srikantes Iyer – University of California, Los Angeles	***1. 8:00 AM - Prognostication of Damage on Automotive Underhood Electronics Subjected to Temperature and Vibration*** Pradeep Lall, Tony Thomas, and Jeff Suhling – Auburn University	***1. 8:00 AM - On-Chip Solid-State CMOS Compatible Micro-Supercapacitors*** Rickard Andersson, Amin Muhammad Saleem, and Vincent Desmaris – Smoltek AB; Bo Song and C. P. Wong – Georgia Institute of Technology
2. 8:25 AM – High Bandwidth Memory Interface on Organic Substrate: Challenge to Electrical Design Vadim Heyfitch, Shen Dong, Nanju Na, Hong Shi, Jaspreet Gandhi, Jane Xi, and Susan Wu – Xilinx, Inc.	***2. 8:25 AM - Interface Fracture Toughness Characterization in Electronic Packages Using the Crack Surface Displacement Extrapolation Method*** Przemyslaw Gromala, Mateus Jeronimo, and Alexandru Prisacaru – Robert Bosch GmbH; Marcus Schulz and Juergen Keller – AMIC GmbH	***2. 8:25 AM - Fabrication of High Capacitance Density Capacitor Using Spray Coated Ba0.6Sr0.4TiO3 Thin Films*** Emannuel Testi, Isabelle Bord Majek, Gilles Philippot, Cyril Aymonier– Université de Bordeaux; Jean Audet and Roxan Lemire – IBM Canada Ltd, Laurent Bechou and Dominique Drouin – Université de Sherbrooke
3. 8:50 AM - Advanced Fan-Out Package Performance SI/PI/Thermal Performance Analysis of Novel RDL Packages Se-Ho You, Seonghwan Jeon, Dan (Kyung Suk) Oh, Kilsoo Kim, Jaechoon Kim, Seung-Yong Cha, Gyoungbum Kim – Samsung Electronics Company, Ltd.	***3. 8:50 AM - Simulation for Enhancing Automotive Power Module DBC Reliability During Assembly Process*** Yong Liu and Qiuxiao Qian – ON Semiconductor	***3. 8:50 AM - Structuring Methods of Polymers for Low-Cost Sensor Manufacturing*** Sebastian Bengsch and Marc Wurz – Institute of Micro Production Technology; Maximilian Aue and Sascha de Wall – Leibniz University Hanover
Refreshment Break: 9:15 a.m. - 10:00 a.m. Harbor Island Foyer & Nautilus Foyer		
4. 10:00 AM - FCBGA Fundamental Technology Realizing 56 Gbps PAM-4 System with 50 cm Electric Transmission Kazuyuki Nakagawa, Keita Tsuchiya, Shinji Katayama, Yoshiaki Sato, Hiroyuki Uchida, and Shinji Baba – Renesas Electronics Corporation; Norio Chujo, Masayoshi Yagyu, and Yutaka Uematsu – Hitachi, Ltd.	***4. 10:00 AM - A Methodology to Integrate Thermo-Mechanical Reliability Predictions into Co-Design of Flip-Chip-On-Lead Devices*** Siva Gurrum, Manu Prakuzhy, Guangxu Li, Hung-Yun Lin, Saumya Gandhi, J. Carlos Arroyo, Frank Mortan, and Amit Nangia – Texas Instruments, Inc.	***4. 10:00 AM - Solely Calcine Controlled Ferroelectricity and Resistivity of Barium Titanate Thin Films and Their Advanced Memory Applications*** Todd Schumann, Xiaochen Zhu, Jacob Neff, Arthur Hebard, Henry Zmuda, and Yong-Kyu Yoon – University of Florida
5. 10:25 AM - Desensitization Design and Analysis for Highly Integrated RFSoC and DRAM Stacked-Die Design Sheng Mou Lin, Chih-Chun Hsu, Yi-An Hsu, Fu-Yi Han, Duen-Yi Ho, Wen-Zhou Wu, and Charles Nan-Cheng Chen – Mediatek, Inc.	***5. 10:25 AM - High Power-Density 3D Integrated Power Supply Module Based on Panel-Level PCB Embedded Technology*** Fengze Hou, Xueping Guo, Qidong Wang,Tingyu Lin, and Liqiang Cao – Institute of Microelectronics of Chinese Academy of Sciences; Wenbo Wang, J. A. Ferreira and G.Q. Zhang – Delft University of Technology; Tingyu Lin – National Center for Advanced Packaging	***5. 10:25 AM - Electrochemical Analysis of Mechanically Flexible Magnesium-ion Battery Electrodes in a Polymer Gel Perchlorate Electrolyte*** Todd Houghton and Hongbin Yu – Arizona State University
6. 10:50 AM - Thermal Stability of Cu/Co Metaconductor and Its Millimeter Wave Applications Timothy Clingenpeel, Seahee Hwangbo, Nicolas Garraud, David Arnold, and Yong-Kyu Yoon – University of Florida	***6. 10:50 AM - Mars 2020 Rover Laser Power Supply Thermomechanical Analysis*** Juan Cepeda-Rizo – Jet Propulsion Laboratory	***6. 10:50 AM - Demonstration of Hermetic Sealing on Ultra-Thin, Wafer-Integrated Aluminum-Polymer Capacitors for High-Voltage and High-Temperature Applications*** Robert Spurney, Himani Sharma, P. M. Pulugurtha, and Rao Tummala – Georgia Institute of Technology; Naomi Lollis and Mitch Weaver – AVX Corporation; Saumya Gandhi and Matt Romig – Texas Instruments, Inc.
7. 11:15 AM - Comparative Study on Electrical Performance of eWLB, M-Series and Fan-Out Chip Last Chih-Yi Huang, Tsun-Lung Hsieh, Po-Chih Pan, Ming-Fong Jhong, Chen-Chao Wang, Sheng-Chi Hsieh – Advanced Semiconductor Engineering Inc.	***7. 11:15 AM - Mechanical Modelling of High-Powered Lateral IGBT for LED Driver Applications*** Chris Bailey, P. Rajaguru, and Hua Lu – University of Greenwich; Alberto Castellazzi and Mattia Antonini – University of Nottingham; Vasantha Pathirana, Nishad Udugampola, and Florin Udrea – University of Cambridge; Paul Mitchelson and Samer Aldhaher – Imperial College	***7. 11:15 AM - Hydrothermal Exfoliation for 2D Boron Nitride Nanosheets*** Guang Yang, Haixu Wang, Ning Wang, Rong Sun and Ching-Ping Wong – Shenzhen Institute of Advanced Technology

Program Sessions: Friday, June 1, 1:30 p.m. - 5:10 p.m.

Session 31: Advanced Wirebond and Interconnect Technologies	Session 32: Heterogeneous Integration	Session 33: Next-Generation Materials and Processes for Through Vias and 3D Interconnects
Committee: Interconnections	**Committee: Advanced Packaging**	**Committee: Materials & Processing**
Room: Harbor Island 1	**Room: Harbor Island 2**	**Room: Harbor Island 3**
Session Co-Chairs: **Li Li – Cisco Systems, Inc.** **Email: LiLi2@cisco.com** **Bernd Ebersberger – Intel Corporation** **Email: bernd.ebersberger@intel.com**	**Session Co-Chairs:** **Luke England – GLOBALFOUNDRIES** **Email: luke.england@globalfoundries.com** **Kuldip Johal – Atotech** **Email: kuldip.johal@atotech.com**	**Session Co-Chairs:** **Praveen Pandojirao-S – Johnson & Johnson** **Email: praveen@its.jnj.com** **Qianwen Chen – IBM Corporation** **Email: chenq@us.ibm.com**
1. 1:30 PM - Effects of Epoxy Molding Compound on Electrical Resistance Degradation of Pd-Coated Cu Wire Bonds in the 175 °C to 225 °C Range Michael Hook and Michael Mayer – University of Waterloo; Stevan Hunter – ON Semiconductor	***1. 1:30 PM - Void-Free Copper Pillar Hybrid Wafer Bonding Using a BCB Based Polymer Adhesive and Chemical Mechanical Polishing*** Michael Gallagher, Julia Kozhukh, Matthew VanHanehem, Edgardo Anzures, Rosemary Bell and Masaki Kondo – DowDupont Electronic Materials	***1. 1:30 PM - Extreme Thinning of Si Wafers for Via-Last and Multi Wafer Stacking Applications*** Anne Jourdain, Joeri De Vos, Nouredine Rassoul, Houman Zahedmanesh, Andy Miller, Gerald Beyer, Eric Beyne, and Dave Thomas – SPTS; Edward Walsby, Jash Patel, Oliver Ansell, Huma Ashraf, and Dave Thomas – SPTS; Shifang Li, Timothy Chang, Stephen Hiebert, Moritz Stoerring and Andrew Cross – KLA-Tencor
2. 1:55 PM - Molecular Dynamics Simulation of Microwelds Formation and Breakage During Ultrasonic Copper Wire Bonding Yangyang Long, Bo He, Weizhe Cui, Bo He,Xiaoying Zhuang, and Jens Twiefel – Leibniz Universität Hannover	***2. 1:55 PM - Heterogeneous Integration Challenges within Wafer Level Fan-Out SiPs for Wearables and IoT*** Alberto Martins, Marcio Pinheiro, Ana Filipa Ferreira, Rodrigo Almeida, F. Matos, J. Oliveira, and Rui Pedro Silva -- Amkor Technology, Inc.; H. M. Santos and H. Gamboa -- INESC TEC; M. C. Monteiro -- Fraunhofer Portugal AICOS	***2. 1:55 PM - Development of a Polyimide/ SiC-Whisker/Nano-Particles Composite with High Thermal Conductivity and Low Coefficient of Thermal Expansion as Dielectric Layer for Interposer Application*** Yunna Sun, Jiangbo Luo, Yan Wang, Zhuoqing Yang, and Guifu Ding – Shanghai Jiao Tong University; Zhenqian Wang – Clemson University
3. 2:20 PM - Investigation for Highly Reliable Free Air Ball Formation for Silver Wire Noritoshi Araki, Ryo Oishi, and Takashi Yamada – Nippon Micrometal Corporation; Yasutomo Ichiyama - Nippon Steel & Sumikin Technology	***3. 2:20 PM - Embedded Silicon Fan-Out (eSiFO): A Promising Wafer-Level Packaging Technology for Multi-Chip and 3D System Integration*** Shuying Ma, Jiao Wang, Fengxia Zheng, Zhiyi Xiao, Teng Wang, and Daquan Yu – Huantian Technology (Kunshan) Electronics Co., Ltd.	***3. 2:20 PM - An Advanced Photosensitive Dielectric Material for High-Density RDL with Ultra-Small Photo-Vias and Ultra-Fine Line/Space in 2.5D Interposers and Fan-Out Packages*** Daichi OKamoto, Yoko Shibasaki Daisuke, Shibata and Tadahiko Hanada - Taiyo Ink Mfg. Co. Ltd.; Fuhan Liu, Venky Sundaram and Rao R. Tummala - Georgia Institute of Technology
Refreshment Break: 2:45 p.m. - 3:30 p.m. Harbor Island Foyer & Nautilus Foyer		
4. 3:30 PM - Corrosion Mechanisms of Cu Wire Bonding on Al Pads Wentao Qin, Harold Anderson, Tom Anderson, George Chang, and Denise Barrientos – ON Semiconductor	***4. 3:30 PM - "Hole-In-One TSV," a New Via Last Concept for High-Density 3D-SOC Interconnects*** Joeri De Vos, Stefaan Van Huylenbroeck, Anne Jourdain, Nancy Heylen, Lan Peng, Geraldine Jamieson, Nina Tutunjyan, Stefano Sardo, Andy Miller, and Eric Beyne – IMEC	***4. 3:30 PM - Highly Productive Solder Interconnect Formation by Bump Stabbing for 3D-TSV Die Stacking*** Shizu Fukuzumi, Hitoshi Onozeki, Naoya Suzuki, and Toshihisa Nonaka – Hitachi Chemical Co., Ltd.
5. 3:55 PM - Low-Temperature Solder – A Breakthrough Technology for Surface Mounted Devices Shubhada Sahasrabudhe, Scott Mokler, Mukul Renavikar, Sandeep Sane, Eric Brigham, Kevin Byrd, Owen Jin, Satish Parupalli, Pubudu Goonetilleke, and Nilesh Badwe – Intel Corporation	***5. 3:55 PM - Flexible (1mm bending radius) Biocompatible Heterogeneous Fan-Out Wafer-Level Platform With the Lowest Reported Die-Shift (<6 µm) and Reliable Flexible Cu-Based Interconnects*** Amir Hanna, Takafumi Fukushima, Arsalan Alam, Steven Moran, William Whitehead, Siva Jangam, S. Pal, G. Ezhilarasu, R. Irwin, Adeel Bajwa, and Subramanian Iyer -- University of California, Los Angeles	***5. 3:55 PM - Reliability Studies of 5 µm Diameter Photo Vias With Daisy Chain Resistance Using Dry Film Photosensitive Dielectric Material*** Atsushi Kubo and Tomoyuki Ando – Tokyo Ohoka Kogyo Co., Ltd.; Chandrasekharan Nair, Bartlet DeProspo, Fuhan Liu, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology
6. 4:20 PM - Advances in Wire Bonding Technology to Overcome Resonance Conditions Aashish Shah, Jon Brunner, Gary Schulze, Ivy Qin, Bob Chylak, and Nelson Wong – Kulicke and Soffa Industries, Inc.	***6. 4:20 PM - Heterogeneous Multi-Die Stitching: Technology Demonstration and Design Considerations*** Paul Jo, Md Obaidul Hossen, Xuchen Zhang, Yang Zhang, and Muhannad Bakir – Georgia Institute of Technology	***6. 4:20 PM - Metal-Alloy Cu Surface Passivation Leads to High Quality Fine-Pitch Bump-Less Cu-Cu Bonding for 3D IC and Heterogeneous Integration Applications*** Asisa Kumar Panigrahi – Koneru Lakshmaiah Education Foundation- Hyderabad; Hemanth Kumar Cheemalamarri, Satish Bonam, Tamal Ghosh, Nirupam Paul, Siva Rama Krishna Vanjari, Paul K. Brince, Tamal Ghos and Shiv Govind Singh – Indian Institute of Technology Hyderabad
7. 4:45 PM - 3D Antenna-in-Package Design with Metallic Coating Technology Chih-Chun Hsu, Sheng-Mou Lin, Ying-Chih Chen, Wen-Zhou Wu, Che-Ya Chou and Charles Nan-Cheng Chen – MediaTek, Inc.; Gavin Gao and Chen-Chao Wang – Advanced Semiconductor Engineering, Inc.	***7. 4:45 PM - Heterogeneous Integration Technology Demonstrations for Future Healthcare, IoT, and AI Computing Solutions*** J.U. Knickerbocker, R. Budd, B. Dang, Q. Chen, E. Colgan, L.W. Hung, S. Kumar, K. W. Lee, M. Lu, J. W. Nah, R. Narayanan, K. Sakuma, V. Siu, and B. Wen – IBM Corporation	***7. 4:45 PM - Interconnection Process Using Laser and Hybrid Underfill for LED Array Module on PET Substrate*** Kwang-Seong Choi, Leeseul Jeong, Keon-Soo Jang, Seok Hwan Moon, Hyun-Cheol Bae, Wagno Alves Braganca Junior, leeseul Jeong, Keon-Soo Jang and Yong-Sung Eom – Electronics and Telecommunications Research Institute; Min Kyo Cho and Seung Il Chang – Beyond! Technology Innovator

Program Sessions: Friday, June 1, 1:30 p.m. - 5:10 p.m.

Session 34: Fan-Out Wafer-Level Package Reliability	Session 35: Multiphysics and Solder Joint Reliability	Session 36: Power Delivery Solutions for Components and Systems
Committee: Applied Reliability	**Committee: Thermal/Mechanical Simulation & Characterization**	**Committee: High-Speed, Wireless & Components**
Room: Nautilus 1 & 2	**Room: Nautilus 3 & 4**	**Room: Nautilus 5**
Session Co-Chairs: **Darvin R. Edwards – Edwards Enterprise Consulting, LLC** **Email: darvin.edwards1@gmail.com** **Pilin Liu – Intel Corporation** **Email: pilin.liu@intel.com**	**Session Co-Chairs:** **Christopher J. Bailey – University of Greenwich** **Email: C.Bailey@greenwich.ac.uk** **Wei Wang – Qualcomm Technologies, Inc.** **Email: weiwng@qti.qualcomm.com**	**Session Co-Chairs:** **Rajen M Murugan – Texas Instruments** **Email: r-murugan@ti.com** **P. Markondeya Raj– Georgia Institute of Technology** **Email: raj@ece.gatech.edu**
1. 1:30 PM - Reliability of Fan-Out Wafer-Level Packaging (FOWLP) with Large Chips and Multiple Re-Distributed Layers (RDLs) Y. M. Cheung, Nelson Fan, Ji Hao, Wu Kai, Eric Kuah, John Lau, Ming Li, Penny Lo, Eric Ng, Lei Yang and Margie Li - ASM; Qing Xiang Yong, Cao Xi, Koh Sau Wee, Jiang Ran and Zhong Cheng - Huawei Technologies Co. Ltd.; Tony Chen, Iris Xu, Zhang Li and Kim Hwee Tan - Jiangyin Changdian Advanced Packaging Co. Ltd.; Rozalia Beica - Dow Chemical Company; Sze Pei Lim and N. C. Lee - Indium Corporation; Cheng-Ta Ko, Henry Yang and Y. H. Chen - Unimicron Technology Corporation; Mian Tao, Jeffery Lo and Ricky Lee - Hong Kong University of Science and Technology	***1. 1:30 PM - Numerical Multiphysics Model for Cu-Al Wire Bond Corrosion Subjected to Highly-Accelerated Stress Test*** Pradeep Lall and Yihua Luo – Auburn University; Luu Nguyen – Texas Instruments, Inc.	***1. 1:30 PM - Analog Power Filtering: Modeling, Measuring & Verifying Analog PI*** Layne Berge, Matt Doyle, and Kyle Schoneck – IBM Corporation
2. 1:55 PM - Passivation Materials for a Reliable Fine Pitch RDL Stéphane Moreau, Nacima Allouti, Céline Ribière, David Bouchu, Jean Charbonnier, Jean-Philippe Michel, Nicolas Buffet, and Pascal Chausse – CEA-LETI	***2. 1:55 PM - Smart Packaging – Microscopic Temperature and Moisture Sensors Embedded in a Flip-Chip Package*** Aurore Quelennec, Yosri Ayadi, Quentin Vandin, and Dominique Drouin – Université de Sherbrooke; Éric Duchesne – IBM Canada, Ltd.; Hélène Frémont – Université de Bordeaux	***2. 1:55 PM - Improved Staggered Through Silicon Via Inductors for RF and Power Applications*** Xiao Sun, Geert Van der Plas, and Eric Beyne – IMEC
3. 2:20 PM - Experimentally Minimizing the Gap Distance Between Extra Tall Packages and PCB Using the Digital Image Correlation (DIC) Method Van Lai Pham, Yuling Niu, Jing Wang, Huayang Wang, Shuai Shao, Charandeep Singh and Seungbae Park – Binghamton University; Cheng Zhong, Sau Wee Koh and Jifan Wang – Huawei Technology Co., Ltd.	***3. 2:20 PM - Improving Solder Joint Reliability for PoP Packages in Current Mobile Ecosystem*** Karthikeyan Dhandapani, Jiantao Zheng, Brian Roggeman, and Marcus Hsu – Qualcomm, Inc.	***3. 2:20 PM - Realization of High Electrical Performance On-Chip Thick Copper Inductor Package by Via Interface Process Improvement for Metal Contact*** Ting-Li Yang, S. B. Yang, W. L. Huang, C. C. Chen, C. C. Kuo, G. C. Huang, K.Y. Wu, T.C. Chang, C. C. Hsu, C. L. Chang, H. L. Huang, Harry Ku, Edward Chen, K. C. Liu, Marvin Liao, and Alex Kalnitsky – Taiwan Semiconductor Manufacturing Company
Refreshment Break: 2:45 p.m. - 3:30 p.m. Harbor Island Foyer & Nautilus Foyer		
4. 3:30 PM - Reliability of Ultra-thin Embedded Silicon Fan-out (eSiFO) Package Directly Assembled on PCB for Mobile Applications Cheng Chen and Lixi Wan – Institute of Microelectronics of Chinese Academy of Sciences; Teng Wang, Daquan Yu, Shuying Ma, and Zhiyi Xiao – Huatian Technology (Kunshan) Electronics Co., Ltd.; Kai Zhu – Huatian Technology (Xi'an) Electronics Co., Ltd.	***4. 3:30 PM - Experimental Investigation on Temperature and Mean Stress Effects on High Cycle Fatigue Behavior of SnAgCu-Solder Alloy*** Youssef Maniar, Georg Konstantin, and Alexander Kabakchiev – Robert Bosch GmbH; Peter Binkele and Siegfried Schmauder – University of Stuttgart	***4. 3:30 PM - An Approach for PDN Simplification of a Mobile Processor*** Sungwook Moon, Seungki Nam, Jungil Son, and Sunha Lee – Samsung Electronics Company, Ltd.
5. 3:55 PM - Interfacial Strength Characterization and Simulation on Stacked Copper-Polymer Structures in Fan-Out Packages Chia-Kuei Hsu, Po-Yao Lin, Wen-Yi Lin, Ming-Chih Yew, Shu-Shen Yeh, Kuang-Chun Lee, Jin-Hua Wang, Po-Chen Lai, Che-Chia Yang, and Shin-Puu Jeng – Taiwan Semiconductor Manufacturing Company	***5. 3:55 PM - Water Effects in Polymers Through Molecular Dynamics*** Nancy Iwamoto – Honeywell International, Inc.	***5. 3:55 PM - Design Optimization and Accurate Extraction of On-Die Decoupling Capacitors for High-Performance Applications*** Xiaoping Liu, Jihong Ren, Wendem Beyene, Simon Ku, Chin Hong Heah, and Sherman Hsu – Intel Corporation
6. 4:20 PM - Effects of Underfill on Thermo-Mechanical Behavior of Fan-out Wafer Level Package Used in PoP: An Experimental Study by Advancements of Real-Time Moiré Interferometry Bulong Wu and Bongtae Han – University of Maryland College Park	***6. 4:20 PM - Comprehensive Study on 2.5D Package Design for Board-Level Reliability in Thermal Cycling and Power Cycling*** Shuai Shao, Yuling Niu, Jing Wang, Ruiyang Liu, and Seungbae Park – Binghamton University; Hohyung Lee, Gamal Refai-Ahmed, Laurene Yip – Xilinx, Inc.	***6. 4:20 PM - Signal and Power Integrity Analysis of InFO Interconnect for Networking Application*** Po-Hao Chang, Chia-Yuan Hsieh, Chun-Wei Chang, Chih-Lun Chuang, and Chen-Feng Chiang – Mediatek, Inc.
7. 4:45 PM - Reliability Study of Large Fan-Out BGA Solution on FinFET Process C.K. Yu, W.S. Chiang, Cooper Peng, M.Z. Lin, Y.H. Fang, M.J. Lin, Benson Lin, Michael Huang, and P.S. Huang – MediaTek, Inc.	***7. 4:45 PM - Comparative Study on Mechanical and Thermal Performance of eWLB, M-Series and Fan-Out Chip Last Packages*** Meng-kai Shih, Ryan Chen, PeterBS Chen, Ying-Chih Lee, Karen Yu Chen, Ian Hu, Tang-Yuan Chen, Lung Tsai, Eatice Chen, Eddie Tsai, David Tarng, and Chih-Pin Hung – Advanced Semiconductor Engineering, Inc.	***7. 4:45 PM - A System-In-Package Based Energy Harvesting for IoT Devices With Integrated Voltage Regulators and Embedded Inductors*** Edward Lee, Mohammad Amir, Sridhar Sivapurapu, Colin Pardue, Hakki Torun, Mohamed Bellaredj, Madhavan Swaminathan, and Saibal Mukhopadhyay – Georgia Institute of Technology

Interactive Presentations: Wednesday, May 30, 9:00 a.m. - 11:00 a.m. and 2:00 p.m. - 4:00 p.m.

Wednesday, May 30, 2018
Session 37: Interactive Presentations 1
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Room: Nautilus Foyer, Lower Level
Session Co-Chairs:
Mark Eblen – Kyocera International SC
Email: mark.eblen@kyocera.com
Patrick Thompson – Texas Instruments, Inc.
Email: patrick.thompson@ti.com

1) Achieving of Intensified Conductive Interconnections for Flex-On-Flex by Using Metal Passivated Copper-Copper Thermocompression Bonding
Hemanth Kumar Cheemalamarri, Satish Bonam, Nirupam Paul, Siva Rama Krishna Vanjari, and Shiv Govind Singh – Indian Institute of Technology, Hyderabad; Asisa Kumar Panigrahi – KL University Hyderabad Campus

2) Reliability Test of Organic Substrate Processed by New Desmear Method "Photodesmear™"
Shinichi Endo, Tomoyuki Habu, and Yasushi Muto – Ushio Inc.; Shintaro Yabu – Ushio America Inc.

3) Highly Conductive Stretchable Electrically Conductive Composites by Halogenation Treatment and Its Application in Stretchable Electronics
Peng Zheng, Haoyue Zhuo, Yuxiao Zou, and Zhuo Li – Fudan University; Wei Guo and Hao Wu – Huazhong University of Science and Technology

4) Electroplating Enhanced Silver Nanowire Networks for Transparent Heaters
Shang Wang and Yanhong Tian – Harbin Institute of Technology

5) Low Transmission Loss Film Material for High-Speed/High-Frequency Devices
Takao Tanigawa, Shin Takanezawa, Minoru Kakitani, Kohji Morita, Mami Shimada, and Etsuo Mizushima – Hitachi Chemical Co. Ltd.

6) Wet-Spun Graphene Sheet as Flexible Heat Spreader for Efficient Thermal Management
Guang Yang, Yuze Yan, and Zhuo Li – Fudan University; Chaowei Li and Yagang Yao – Chinese Academy of Sciences

7) Aging Characteristics of Green Mold Compound for Use in Encapsulation of Microelectronic Devices
Subramani Manoharan, Carlos Morillo, and Patrick McCluskey – University of Maryland; Chandradip Patel and Steven Dunford – Schlumberger Technology Corporation

8) Effective Stress Relief Without Jeopardizing Reliability in Overmolded Packages With Stress Buffers
Amar Mavinkurve, Jeroen Zaal, Yukai Liang, Sean Xu, Antoine Storez, Seng Kiong Teng, Yuan Guo, and Sheila Chopin – NXP Semiconductors

9) High-Temperature Mechanical Behavior of SAC and SAC+X Lead-Free Solders
Mohammad Alam, Jeffrey Suhling, Pradeep Lall, K.M. Rafidh Hassan – Auburn University

10) Flexible Wearable Biometric Band and Smartphone Application for Prevention of Sudden Causes of Death
Pradeep Lall and Hao Zhang – Auburn University; Rahul Lall – Stanford University

11) Backward Compatible Connectors for Next Generation PCIe Electrical I/O
Lei Shan and Daniel Freidman – IBM Corporation; Craig Kennedy, Warren Persak, and Kevin Lau – Amphenol Corporation

12) PCB Pin Area Wire Modeling Based on Representative Layer 2D Misregistration
Zhaoqing Chen – IBM Corporation

13) Compact Low-Power Avionics for the Europa Lander Concept and Other Missions to Ocean Worlds
Don Hunter, Gary Bolotin, Doug Sheldon, Malcolm Lias, and Christopher Stell, and Jong-ook Suh – Jet Propulsion Laboratory

14) Optimization of Laser Release Process for Throughput Enhancement of Fan-Out Wafer-Level Packaging
Chia-Hsin Li, Qi Wu– Brewer Science, Inc.; Jay Su – Electronics and Optoelectronics Research Laboratories; Yu-Hua Chen – Unimicron Technology Corp; Yu-Min Lin – Electronics and Optoelectronics Research Laboratories; Xiao Liu– National Chiao Tung University; Jim-Wein Lin, Puru Lin, Cheng-Ta Ko, Yu-Hua Chen – Unimicron Technology Corp.; WenWei Shen, Tzu-Ying Kou, Shin-Yi Huang, Ang-Ying Lin, Yu-Min Lin, Kuan-Neng Chen – ITRI

15) Thermally Conductivity Underfill and Its Viscoelastic Properties Using Hexagonal Boron Nitride Nanofiller
Sara Razgaleh and Shyam Aravamudhan – Joint School of Nanoscience and Nanoengineering

16) Self-Assembly Technology for FlexTrate
Tak Fukushima – Tohoku University and University of California, Los Angeles; Yuki Susumago, Hisashi Kino, and Tetsu Tanaka – Tohoku University; Arsalan Alam, Amir Hanna, and Subramanian Iyer – University of California, Los Angeles

17) High-Performance EMI Shielding Materials and Spraying Process Parameters for High-Frequency FCBGA Package Application
Kisu Joo, Kyu Jae Lee, Jung Woo Hwang, Jin-Ho Yoon, Yoon-Hyun Kim, Joo-Wook Park, and Se Young Jeong – Ntrium Incorporation; Myung Jin Yim – Intel Corporation

18) Physical Aging of Epoxy Molding Compound and Its Influences on the Warpage of Reconstituted Wafer
Tz-Cheng Chiu and En-Yu Yeh – National Cheng Kung University; Wei-Jie Yin, Yu-Ting Yang, Dao-Long Chen, and Yi-Hsiu Tseng – Advanced Semiconductor Engineering, Inc.

19) High Thermal Conductive Semi-Sintering Die Attach Paste
Rajasekhar Peddi, Wei Yao, Kily Wu, Robin Fu, and Hoseun Yoo – Henkel Corporation

20) Non-Destructive Assessment of the Porosity in Ag-sinter Joints Using Acoustic Waves
Sebastian Brand, Bianca Böttge, Michael Kögel, Falk Naumann, and Frank Altmann – Fraunhofer IMWS; Jurrian Zijl and Sebastiaan Kersjes – BESI Netherlands; Thomas Behrens – Infineon Technologies

22) Reliability Study and Finite Element Modeling of a Wearable Sensor Patch (WSP) to Monitor ECG Signals
Varun Soman, Mark Poliks, and James Turner – Binghamton University; Mark Schadt, Michael Shay, and Frank Egitto – i3 Electronics, Inc.

Wednesday, May 30, 2018
Session 38: Interactive Presentations 2
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Nautilus Foyer, Lower Level
Session Co-Chairs:
Rao Bonda
Amkor Technology
Email: rao.bonda@amkor.com
John Hunt
Advanced Semiconductor Engineering, Inc.
Email: john.hunt@aseus.com

1) Fabrication and Characteristics of Spin-on Dielectric for Multi-level Interconnect in WLP
Changmin Song, Sarah Kim, and Sungdong Kim – Seoul National University of Science and Technology

2) High Density TSV-Free Interposer (TFI) Packaging with Submicron Cu Damascene RDLs for Integration of CPU/GPU and HBM
Masaya Kawano, Chun-Mei Wang, Hong-Yu Li, Mian-Zhi Ding, Sharon Lim, Teck-Guan Lim, Zi-Hao Chen, and Fa-Xing Che – IME

3) Dynamic Warpage Analysis of QFP Packages During Soldering Reflow Process and Thermal Cycle
Marco Rovitto, Arianna Morelli, Carlo Passagrilli, and Claudio Maria Villa – STMicroelectronics

4) Improvement of Mechanical Properties of Zn Added Sn58Bi Alloy by Zn Segregation on the Sn-Bi Phase Boundaries During Thermal Aging
Shiqi Zhou, Omid Mokhtari, and Hiroshi Nishikawa – Osaka University

5) Low Dielectric Properties Encapsulation for High-Frequency Devices
Naoki Kanagawa, Daisuke Sasaki, and Shigeru Yamatsu – Panasonic Corporation

6) Controlling Die Warpage by Applying Under Bump Metallurgy for Fan-Out Package Process Applications
Hwan-Pil Park and Young-Ho Kim – Hanyang University; Young-Moon Jang and Sung-Hoon Choa – Seoul National University of Science and Technology

7) Influence of Metallization and Size on Conductive Properties of Metal-Coated Polymer Particles in Anisotropic Conductive Adhesive
Molly Bazilchuk and Helge Kristiansen – Conpart AS; Jianying He – Norwegian Institute of Science and Technology

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 11-18 for location.

8) Demonstration of a Heterogeneously Integrated System-on-Wafer (SoW) Assembly
Adeel Ahmad Bajwa – University of California, Los Angeles and K&S; SivaChandra Jangam, Randall Irwin, Boris Vaisband, Saptadeep Pal, Mark Goorsky, and Subramanian Iyer – University of California, Los Angeles

9) Novel Temporary Adhesive Materials for RDL-First Fan-Out Wafer-Level Packaging
Hong Zhang, Xiao Liu, Rama Puligadda, Shawna RIckard, and Tony Flaim – Brewer Science, Inc.

10) The Reliability and the Effect of NCA Trapping in Thermo-compression Flip-Chip Solder Joints Fabricated Using Sn-Ag Solder Capped 40 µm Pitch Cu Pillar Bumps and Low Temperature Curable Non-conductive Adhesive (NCA)
Jae-Yong Park, Hwan-Pil Park, Seongchul Kim, and Young-Ho Kim – Hanyang University; Taeyoung Lee and Sehoon Yoo – Korea Institute Industrial Technology

11) Performance of Fine and Ultra-Fine Lead-Free Powders for Solder Paste Applications
Amir Nobari and Sylvain St-Laurent – 5N Plus Micro Powders Inc.; Yannig Thomas – National Research Council Canada; Arslane Bouchemit and Gilles L'Espérance – École Polytechnique de Montréal

12) Laser Based Full Cut Dicing Evaluations for Thin Si Wafers
Jeroen van Borkulo, Paul Verburg, and Richard van der Stam – ASM Pacific Technology

13) Thermal Design and Characterization of High-Power SiC Inverter with Low Profile and Enhanced Thermal Performance
Gongyue Tang, Tai Chong Chai, and Xiaowu Zhang – IME

14) Challenges of Large Body FCBGA on Board Level Assembly and Reliability
Fletcher (Cheng Piao) Tung, Chung (Hsiang Chun) Chen, Max (Chin Yu) Lu, Jensen Tsai, and Yu-Po Wang – Siliconware Precision Industries Co., Ltd.

15) Optimization of Via Bottom Cleaning for Bumpless Interconnects and Wafer-On-Wafer (WOW) Integration
Youngsuk Kim, S. Kodama, Y. Mizushima, N. Araki, and T. Ohba – Tokyo Institute of Technology; C. Hsiao, H. Chang, and C. Lin – Industrial Technology Research Institute of Taiwan

16) Design, Fabrication, and Characterization of TSV Interposer Integrated 3D Capacitor for SIP Applications
Jiwei Li and Shenglin Ma – Xiamen University; Huan Liu, Wei Wang, Yufeng Jin, Yong Guan, and Jing Chen – Peking University; Min Miu – Beijing Information Science and Technology University; Liulin Hu and Shuwei He – Chengdu Garner Haiwei Co., Ltd.

17) High-Speed Precision Handling Technology of Micro-Chip for Fan-Out Wafer Level Packaging (FOWLP) Application
Qianwen Chen, Li-wen Hung, Bing Dang, Bo Wen, Russell Budd, Jae-Woong Nah, Evan Colgan, and John Knickerbocker – IBM Corporation

18) A Novel Inorganic Substrate by Three-Dimensionally Stacked Glass Core Technology
Toshiki Iwai, Taiji Sakai, Daisuke Mizutani and Seiki Sakuyama – Fujitsu Laboratories, Ltd.; Kenji Iida, Takayuki Inaba, Hidehiko Fujisaki, and Yoshinori Miyazawa - Fujitsu Interconnect Technologies, Ltd.

19) High-Reliability Sintered Silver-Indium Bonding With Anti-Oxidation Property for High-Temperature Applications
Chun An Yang and C. Robert Kao – National Taiwan University; Hiroshi Nishikawa – Osaka University; Chin C. Lee – University of California, Irvine

20) RF Characterization, Analysis and Miniaturization Impact of RDL Interconnects
Hélène Jacquinot, Roselyne Ségaud, Lucile Arnaud, Jean-Charles Barbe, and Séverine Cheramy – CEA-LETI; Kévin Morot, Alexis Farcy, and Rémi Velard – ST-Microelectronics; Thierry Lacrevaz and Bernard Flechet – IMEP-LAHC

21) Integration of the SERF Magnetometer and the Mz Magnetometer Using Micro-Fabricated Alkali Vapor Cell
Jin Zhang, Jintang Shang, Yu Ji, Guoliang Li, Lin Lu, and Zhihua Pan – Southeast University; Ching-Ping Wong – The Chinese University of Hong Kong

22) Integrated Copper Heat Spreaders in Glass Panel Embedded Packages with Near-Zero Thermal Interface Resistance
Nithin Nedumthakady, Bartlet DeProspo, Venkatesh Sundaram, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology; Sean Garrison, Kyle Byers, and Barbara Reed – Honeywell Federal Manufacturing and Technologies, LLC; Chris Gibson and Michael Elsbury - Sandia National Labs

23) Investigation of Material Dynamic Processes During Shear Test of Heavy Wire Bond Contacts
Robert Klengel, Sebastian Tismer, Falk Naumann, and Sandy Klengel – Fraunhofer IMWS

24) Leading-Edge and Ultra-Thin 3D Glass-Polymer 5G Modules With Seamless Antenna-to-Transceiver Signal Transmissions
Atom Watanabe, Tong-Hong Lin, Markondeya R. Pulugurtha, Venky Sundaram, Manos M. Tentzeris, and Rao R. Tummala – Georgia Institute of Technology; Tomonori Ogawa – Asahi Glass Company

25) Effect of Surface Finish and High Bi Solder Alloy on Component Reliability In Thermal Cycling
Sa'd Hamasha, Francy Akkara, Jeffery Suhling, John Evans, Mohammed Abueed, Mumen Rababah, Cong Zhao and Sianan Su – Auburn University

26) Electromigration Behavior and Mechanical Properties of the Whole Preferred Orientation Intermetallic Compound Interconnects for 3D Packaging
Mingliang Huang, Lin Zou, and S. Q. Yin – Dalian University of Technology

Thursday, May 31, 2018
Session 39: Interactive Presentations 3
9:00 AM - 11:00 AM
Committee: Interactive Presentations
Room: Nautilus Foyer, Lower Level
Session Co-Chairs:
Nam Pham
IBM Corporation
Email: npham@us.ibm.com
Ibrahim Guven
Virginia Commonwealth University
Email: iguven@vcu.edu

1) 3D Stacking Process With Thermo-Sonic Bonding Using Non-Conductive Film
Shigeru Yamatsu, Kazuki Watanabe, Naoki Kanagawa, Teppei Kojio, and Takatoshi Ishikawa, Panasonic Corporation

2) 2D Magnetic Inductors for DC-DC Converters on Glass Interposer
Vincent Lafage, Yann Beillard, and Dominique Drouin – Université de Sherbrooke; Arvind Sridhar and Thomas Brunschwiler – IBM Zurich

3) Modeling and Characterization of a Hermetic Ceramic Package and Its Performance Impact on a 1.5-7V Input, 3-A, Radiation-Hardened Ultra-Low Dropout (LDO) Regulator
Javier Valle, Li Ming, Jeff Holloway, and Leon Stiborek – Texas Instruments, Inc.

4) Electrical Characterization of a High-Speed HBM Interface for a Low-Cost Interposer
Andy Heinig, Fabian Hopsch, and Michael Dittrich – Fraunhofer IIS/EAS

5) Millimeter-Wave Wireless Chip-to-Chip (C2C) Communications in 3D System in Packaging (SiP) Using Compact Through Glass Via (TGV)-integrated Antennas
Seahee Hwangbo and Yong-Kyu Yoon – University of Florida; Aric Shorey – Corning, Inc.

6) Reliability of Sintered and Soldered High-Power Chip Size Packages and Flip-Chip LEDs
Alexander Hanss, Maximilian Schmid, Gordon Elger, and Sri Krishna Bhogaraju – Technische Hochschule Ingolstadt; Fosca Conti – University of Padova

7) Comparison of Package-on-Package Technologies Utilizing Flip Chip and Fan-Out Wafer Level Packaging
Amy Lujan – SavanSys Solutions LLC

8) Fork Type Structure of Silicon Waveguide for Optical Coupling Efficiency Optimization
Meiju Lu – Advanced Semiconductor Engineering, Inc.; Warren Wang, OnionZY Yang, Shian Tu, Meiju Lu, Jihan Chen, and Vincent Lin – Corporate R&D / Optical Communication SiP Technology

9) MEMS Optical Packaging Technology Trends and Challenges
John Miranda – STATS ChipPAC, Inc.; TaeKeun Lee – STATS ChipPAC Korea, Ltd.

10) Effect of Improved Optimization of DFE Equalization on Crosstalk and Jitter in High-Speed Links With Multi-Level Signal
Nana Dikhaminjia and M. Tsiklauri – Ilia State University; Han Deng, Jiayi He, and James Drewniak – Missouri University of S&T; Arun Chada and Bhyrav Mutnury – Dell, Inc.

Thursday & Friday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 15-22 for locations.

11) Copper Transparent Antennas on Flexible Glass by Subtractive and Semi-Additive Fabrication for Automotive Applications
Jack Lombardi, Robert Malay, and Mark Poliks – Binghamton University; James Schaffner and Hyok Jae Song – HRL Laboratories; Ming-Huang Huang and Scott Pollard – Corning, Inc.; Timothy Talty – General Motors

12) Correlated Model for Wafer Warpage Prediction of Arbitrarily Patterned Films
Gregory Ostrowicki, Siva Gurrum, and Amit Nangia – Texas Instruments, Inc.

13) Thermomechanical Properties of Fan-Out Wafer-Level Package with Various Chip and Mold Thickness
Haksan Jeong, Woo-Ram Myung, Kwang-Ho Jung, and Seung-Boo Jung – Sungkyunkwan University

14) Design of a Compact Broadband Butler Matrix and Its Application in Organic Beam-Former at the 5 GHz Band
Chung-Yi Hsu, Chia-Ling Chiang, and Lih-Tyng Hwang – National Sun Yat-Sen University; Fa-Shian Chang – Cheng Shiu University

15) Three-Dimensional Simulation of Effects of Microstructure Evolution and Interfacial Delamination on Cu Protrusion in Copper Filled Through Silicon Vias by Combined Monte Carlo and Finite Element Methods
Shui-Bao Liang, Chang-Bo Ke, Cheng Wei, Min-Bo Zhou, and Xin-Ping Zhang – South China University of Technology

16) Electrical Design for the Development of FOWLP for HBM Integration
Teck Guan Lim and David Ho Soon Wee – Institute of Microelectronics

17) Accurate Electrical Modeling of Through Silicon Via with Minority Carrier Redistribution Effect
Huan Liu, Runiu Fang, and Xin Sun – Peking University; Min Miao – Beijing Information Science and Technology University; Yufeng Jin – Shenzhen Graduate School of Peking University

18) Thermal and Electrical Characterization of TSV Interposer Embedded With Microchannel for 2.5D Integration of GaN RF Devices
Han Cai and Shenglin Ma –Xiamen University; Wei Wang, Yufeng Jin, and Jing Chen – Peking University; Weiwei Xiang and Jian Zhang – Southwest China Research Institute of Electronic Equipment; Liulin Hu and Shuwei He - Chengdu Ganide Technology Co., Ltd.

19) Alternative Deposition Solution for Cost Reduction of TSV Integration
Julien Vitiello and Fabien Piallat – KOBUS

20) Evaluation of Mechanical Stress Induced During IC Packaging
Vladimir Cherman, Melina Lofrano, Mario Gonzalez, Francisco Cadacio Jr., Kenneth June Rebibis, and Eric Beyne – IMEC; Akihito Takano and Mitsutoshi Higashi – Shinko Electric Industries, Co. Ltd.

21) Wireless EAS Sensor Tags for Volatile Profiling in Food Packages
Saranraj Karuppuswami, Mohd Ifwat Mohd Ghazali, Saikat Mondal, and Premjeet Chahal – Michigan State University

22) High Throughput and Improved Edge Straightness for Memory Applications Using Stealth Dicing
Natsuki Suzuki and Takayuki Oba – Tokyo Institute of Technology; Yuta Kondo, Takeshi Sakamoto, Kazuhiro Atsuki, and Naoki Uchiyama – Hamamatsu Photonics K.K.

23) Thick 3D Printed RF Components: Transmission Lines and Bandpass Filters
Kyoung Youl Park – Agency for Defense Development; Mohd Ifwat Ghazali and Premjeet Chahal – Michigan State University; Nophadon Wiwatcharagoses – King Mongkut's University of Technology North Bangkok

24) Introduction of a New Metric for the Solder Joint Reliability Assessment of BGA Packages on System Level
Fabian Schempp, Marc Dressler, Daniel Kraetschmer, and Friederike Loerke – Robert Bosch GmbH; Juergen Wilde – University of Freiburg, IMTEK

25) Compact Optical Coherent Receiver for Avionics Applications
Simon Ayotte, Ghislain Bilodeau, Jocelyn Blanchet-Létourneau, Michel Morin, Pascal Deladurantaye, Francois Costin, André Babin, Louis-Philippe Perron, Guillaume Brochu, C. A. Davidson, D. D'Amato, É. Girard-Deschênes, P. Chrétien, M. Laplante, M. Drolet, G. Paré-Olivier – Teraxion

26) Parylene as a Dielectric Material for Electronic Applications in Space
Franz Selbmann – Fraunhofer ENAS; Mario Baum - TU Bergakademie Freiberg & Fraunhofer ENAS Chemnitz; Maik Wiemer - Fraunhofer ENAS Chemnitz; Yvonne Joseph - TU Bergakademie Freiberg; Thomas Otto - TU Chemnitz & Fraunhofer ENAS Chemnitz

27) On Using Packaging Parasitics to Implement a Tunable Matching Circuit for Low Power Wake-Up Receivers
Jack Ou – California State University, Northridge

Thursday, May 31, 2018
Session 40: Interactive Presentations 4
2:00 PM - 4:00 PM
Committee: Interactive Presentations
Room: Nautilus Foyer, Lower Level
Session Co-Chairs:
Swapan Bhattacharya
Engent Inc.
Email: Swapan.bhattacharya@engentaat.com
Mark Poliks
Binghamton University
Email: mpoliks@binghamton.edu

1) Practical Design Method to Reduce Crosstalk for Silicon Wafer Integrated Fan-Out Technology (SWIFT)
HoJeong Lim, JeongKyu Yang, and Ruben Fuentes – Amkor Technology, Inc.

2) Fully Inkjet-Printed Three-Dimensional Bandpass Filter on Liquid Crystal Polymer Substrate
Hsuan-Ling Kao – Chang Gung University; Cheng-Lin Cho – National Tsing Hua University

3) A Dynamic Bending Method for PoP Package Board Level Reliability Validation
Jeffrey Lee and Cheng-Chih Chen – iST-Integrated Service Technology Inc; Lane Brown, Esme Mehretu, Thomas Obrien, and Feng Lu – Motorola Lenovo

4) Eliminating Harmful Intermetallic Compound Phase in Silver Wire Bonding by Alloying Silver with Indium
Chin C. Lee and Jiaqi Wu – University of California, Irvine

5) Cyanate Ester/Epoxy Co-Curing System With Thermal Stabilizers for High-Temperature Stability
Fan Wu, Bo Song, Kyoung-Sik Moon, and C.P. Wong – Georgia Institute of Technology

6) Demonstration of 28 GHz Band Pass Filter Toward 5G Using Ultra Low Loss and High Accuracy Through Quartz Vias
Yoichiro Sato and Nobutaka Kidera – Asahi Glass Co., Ltd.

7) Micromesh-Enabled Low-Cost Thermal Ground Planes for High Heat Flux Power Electronics
Shanshan Xu, Ryan Lewis, Rongfu Wen, Ronggui Yang, and Y.C. Lee – University of Colorado, Boulder; Luu Nguyen and Woochan Kim-Texas Instruments, Inc.

8) 3D Integration of Physics System Using Foldable Packaging for MEMS Atomic Clocks
Jongcheol Park, Tae Hyun Kim, Hee Yeoun Kim, Gil Sun Roh, Gapseop Sim, HaeCheol Hwang, and JinWon Ko – National NanoFab Center; Taeg Yong Kwon and Hyun Gue Hong – Korea Research Institute of Standards and Science

9) Die Edge Crack Propagation Modeling for Risk Assessment of Advanced Technology Nodes
Tingge Xu, Zhuo-Jie Wu, Haojun Zhang, Carole Graas, and Patrick Justison – GLOBALFOUNDRIES

10) Development of a Through-Silicon Via (TSV) Process Module for Multi-Project Wafer SiGe BiCMOS and Silicon Interposer
Matthias Wietstruck, Steffen Marschmeyer, Philipp Kulse, Thomas Voß, Marco Lisker, Andreas Krüger, Dirk Wolansky, Mirko Fraschke, and Mehmet Kaynak – IHP

11) A New, Efficient Method for Preparation of 3D Integrated Systems by Laser Techniques
Robert Klengel, Sandy Klengel, Georg Schusser, and Michael Krause – Fraunhofer IMWS

12) Effect of Interaction Between Multiple Defects on Z-Depth Estimate in Lock-In Thermography Applications
Bharath Viswanath Ravi, Mayue Xie, and Deepak Goyal – Intel Corporation

13) Practical High-Speed PCB Stackup Tool – Generation and Validation
Wei Jiang, Kevin Cai, and Bidyut Sen – Cisco Systems, Inc; Guoan Wang – University of South Carolina

14) Volatile Molecular Sensors Using Terahertz Resonators on Porous Substrates
Saranraj Karuppuswami, Jennifer Byford, and Premjeet Chahal – Michigan State University

15) Effects of the Adhesion Strength on the Bending Fatigue Behavior of Cu Pattern Laminated Fabrics Using B-Stage Non-Conductive Films (NCFs)
Seung-Yoon Jung and Kyung-Wook Paik – Korea Advanced Institute for Science and Technology

16) Process Development of 4-die Stack Module Using Moldable Underfill
Ser Choong Chong, Hongyu Li, Ling Xie, Simon Boon Lim, and Zhaohui Chen – Institute of Microelectronics

17) Integrated Fully Solid-State Capacitor Based on Carbon Nanofibers and Dielectrics
Rickard Andersson, Amin Muhammad Saleem, and Vincent Desmaris – Smoltek AB

Wednesday & Thursday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 11-18 for location.

18) Effects of ACFs Modulus and Adhesion Strength on the Bending Reliability of CIF (Chip-in-Flex) Packages in Thermal and Humid Conditions
Tae-Ik Lee, Taek-Soo Kim, Kyung-Wook Paik, and Ji-Hye Kim – Korea Advanced Institute of Science and Technology

19) Warpage Simulation / Experiments and Analysis of 12" Wafer-Level Fan-Out Packaging Technology
Jia-Shen Lan and Mei-Ling Wu – National Sun Yat-sen University; Shang Lee, Yaochen Wang, Brian Wu, and Chiyu Wang – Advanced Semiconductor Engineering, Inc.

20) Design Considerations of a Matching Circuit for Low-Power Wake-Up Receivers
Jie Geng, Hongwen Zhang and Francis Mutuku – Indium Corporation

21) Warpage and Reliability Challenges for Stacked Silicon Interposer Technology in Large Packages
Scott McCann, HoHyung Lee, Gamal Refai-Ahmed, Tom Lee, and Suresh Ramalingam – Xilinx, Inc.; Ning-Cheng Lee – Indium Corporation

22) Effect of Shallow Cycling on Flexible Power-Source Survivability Under Bending Loads and Operating Temperatures Representative of Stresses of Daily Motion
Pradeep Lall and Amrit Abrol – Auburn University; Jason Marsh – NextFlex; Ben Leever – US AFRL

23) Nanomechanical Characterization of Intermetallic Compounds in Lead Free Solder Joints
Abdullah Fahim, Sudan Ahmed, Jeffrey Suhling, and Pradeep Lall – Auburn University

24) Fan-Out Wafer Level Packaging for Heterogeneous Integration
John Lau, Ming Li, Margie Li, Nelson Fan, Eric Kuah, Y. M. Cheung, Eric Ng, Penny Lo, Wu Kai, and Ji Hao – ASM Pacific Technology, Ltd.; Tony Chen, Iris Xu, Zhang Li, and Kim Hwee Tan – Jiangyin Changdian Advanced Packaging Co. Ltd.; Qing Xiang Yong, Zhong Cheng, Koh Sau Wee, Jiang Ran, and Cao Xi – Huawei Technologies Co. Ltd.; Rozalia Beica – Dow Chemical Company; Sze Pei Lim and N. C. Lee – Indium Corporation; Cheng-Ta Ko, Henry Yang, and Y. H. Chen – Unimicron Technology Corporation; Mian Tao, Jeffrey Lo, and Ricky Lee – Hong Kong University of Science and Technology

Friday, June 1, 2018
Session 41: Student Interactive Presentations
8:30 AM - 10:30 AM
Committee: Interactive Presentations
Room: Nautilus Foyer, Lower Level
Session Co-Chairs:
Michael Mayer
University of Waterloo
Email: mmayer@uwaterloo.ca
Pavel Roy Paladhi
IBM Corporation
Email: Pavel.Roy.Paladhi@ibm.com

1) Broad-Band Dielectric Probes for On-Wafer Characterization of Terahertz Devices
Jennifer Byford and Premjeet Chahal – Michigan State University

2) Machine Learning Driven Advanced Packaging and Miniaturization of IoT for Wireless Power Transfer Solutions
Hakki Torun, Colin Pardue, Mohamed Belladredj, Anto K. Davis, and Madhavan Swaminathan – Georgia Institute of Technology

3) Application of Additive Manufacturing Technologies for Realization of Multilayer Microstrip Directional Filter
Ilona Piekarz, Jakub Sorocki, Slawomir Gruszczynski, and Krzysztof Wincza – AGH University of Science and Technology; John Papapolymerou – Michigan State University

4) 3D Printed Liquid Jet Impingement Cooler: Demonstration, Opportunities and Challenges
Tiwei Wei, Herman Oprins, Vladimir Cherman, Ingrid De wolf, and Eric Beyne – IMEC; Martine Baelmans and Shoufeng Yang – KU Leuven

5) Design and Surface Modification of PET Substrates Using UV/Ozone Treatment for Roll-to-Roll Processed Solar Photovoltaic (PV) Module Packaging
Bo Song, Jinho Hah, Kyoung-sik Moon, C.P. Wong, and Samuel Graham – Georgia Institute of Technology

6) A Study on the High-Frequency Performance and Physical Modelling of ACFs Joints Using Coplanar Waveguide for Flex-on-Board Applications
Shuye Zhang, Tiesong Lin, and Peng He – Harbin Institute of Technology; Junyong Park, Gapyeol Park, Huijin Song, Joungho Kim, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

7) Low-Temperature Cu-Cu Bonding by Anti-Oxidative Copper Nanoparticle Paste
Yun Mou, Yang Peng, Junjie Li, Hao Cheng, Xingxing Liu, and Mingxiang Chen – Huazhong University of Science and Technology

8) Deep Understanding of the Role of Cu in RDL to Warpage by Exploring the Warpage Evolution With Microstructural Changes
Gong Cheng, Gaowei Xu, Wei Gai, and Le Luo – Shanghai Institute of Microsystem and Information Technology

9) A 56 Gbps I/O Interface Design with Exact Power Source Simulation - Total I/O Circuit Design with over 28 GHz from Driver to Receiver Device Models
Daisuke Ogawa, Chihiro Ueda, Kaoru Hashimoto, and Kanji Otsuka – Meisei University; Daisuke Iguchi, Yusuke Taira, Nobutaka Hara, and Yusuke Niisaka – Fuji Xerox Co., Ltd.; Naoto Yoshii – Murata Manufacturing Co., Ltd.

10) Enhancements on Underfill Materials' Thermal Conductivity by Insulation Coating Layer Control of Conductive Particles
Tae-Ryong Kim – Seoul National University/Ntrium; Kisu Joo and Se Young Jeong – Ntrium Incorporation; Boo Taek Lim and Boung Ju Lee – National Nanofab Center; Sung-Soon Choi – Korea Electronics Technology Institute; Euijoon Yoon – Seoul National University

11) Fabrication of Fe-3.5 wt.%Si Magnetic Cores for Power Electronic Converters by Selective Laser Melting
Wangyun Li, Jing Wang, Guang Chen, Daniel Engstrom, and Changqing Liu – Loughborough University; Xinping Zhang – South China University of Technology; Adam Walker and Gaurang Vakil – University of Nottingham; Andrew Forsyth – University of Manchester

12) Accurate Core Alignment for Polymer Optical Waveguide in the Mosquito Method for High-Efficient Coupling
Takaaki Ishigure, Kumi Date, and Yoshie Morimoto – Keio University

13) Synthesis of a Graphene Carbon Nanotube Hybrid Film by Joule Self-Heating CVD for Thermal Applications
Josef Hansson, Majid Kabiri Samani, Andreas Nylander, Nan Wang, Torbjörn Nilsson, and Johan Liu – Chalmers University of Technology; Lilei Ye – SHT Smart High Tech AB

14) Size and Shape Effect in the Determination of the Fracture Strength of Silicon Nitride in MEMS Structures at High Temperatures
Alex Axel Navarrete Gonzalez, Eric Brace, and Patricia Nieva – University of Waterloo

15) A Study on the Curing Properties and Viscosities of Non-Conductive Films (NCFs) for Sn-Ag Solder Bump Flip Chip Assembly
HanMin Lee, SeYong Lee, JongHo Park, and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology; Chang-kyu Chung, Kyung-Woon Jang, Il Kim, and SeongWoo Choi – Samsung Electronics Company, Ltd.

16) Suspended Microstrip Low-Pass Filter Realized Using FDM Type 3D Printing with Conductive Copper-Based Filament
Jakub Sorocki, Ilona Piekarz, Slawomir Gruszczynski, and Krzysztof Wincza – AGH University of Science and Technology; John Papapolymerou – Michigan State University

17) Modeling and Design of 2.5D Package With Mitigated Warpage and Enhanced Thermo-Mechanical Reliability
Jing Wang, Yuling Niu, and Seungbae Park – Binghamton University; Alexander Yatskov – Juniper Networks

18) Piezoelectric Ceramics and Flexible Printed Circuits (FPCs) Interconnection Using Anisotropic Conductive Films (ACFs) for Ultrasound Transducers Assembly
Jae-Hyeong Park and Kyung-Wook Paik – Korea Advanced Institute of Science and Technology

19) Design, Fabrication and Characterization of a Novel TSV Interposed Integrated Inductor for RF Applications
Yunheng Sun, Yufeng Jin, Wei Wang, and Jing Chen – Peking University; Han Cai, Jiwei Li, and Shenglin Ma – Xiamen University; Min Miao – Beijing Information Science and Technology University; Liulin Hu and Shuwei He – Chengdu Ganide Technology

20) A Novel Integration of Stereolithography and Inkjet Printing for Multichip Modules with High Frequency Packaging Applications
Ryan Bahr, Bijan Teharani, and Manos Tentzeris – Georgia Institute of Technology; Kyle Byers – Honeywell International, Inc.

Thursday & Friday Refreshment Breaks: 9:15 a.m. - 10:00 a.m. and 2:45 p.m. - 3:30 p.m. • See pages 15-22 for locations.

Technology Corner Exhibits

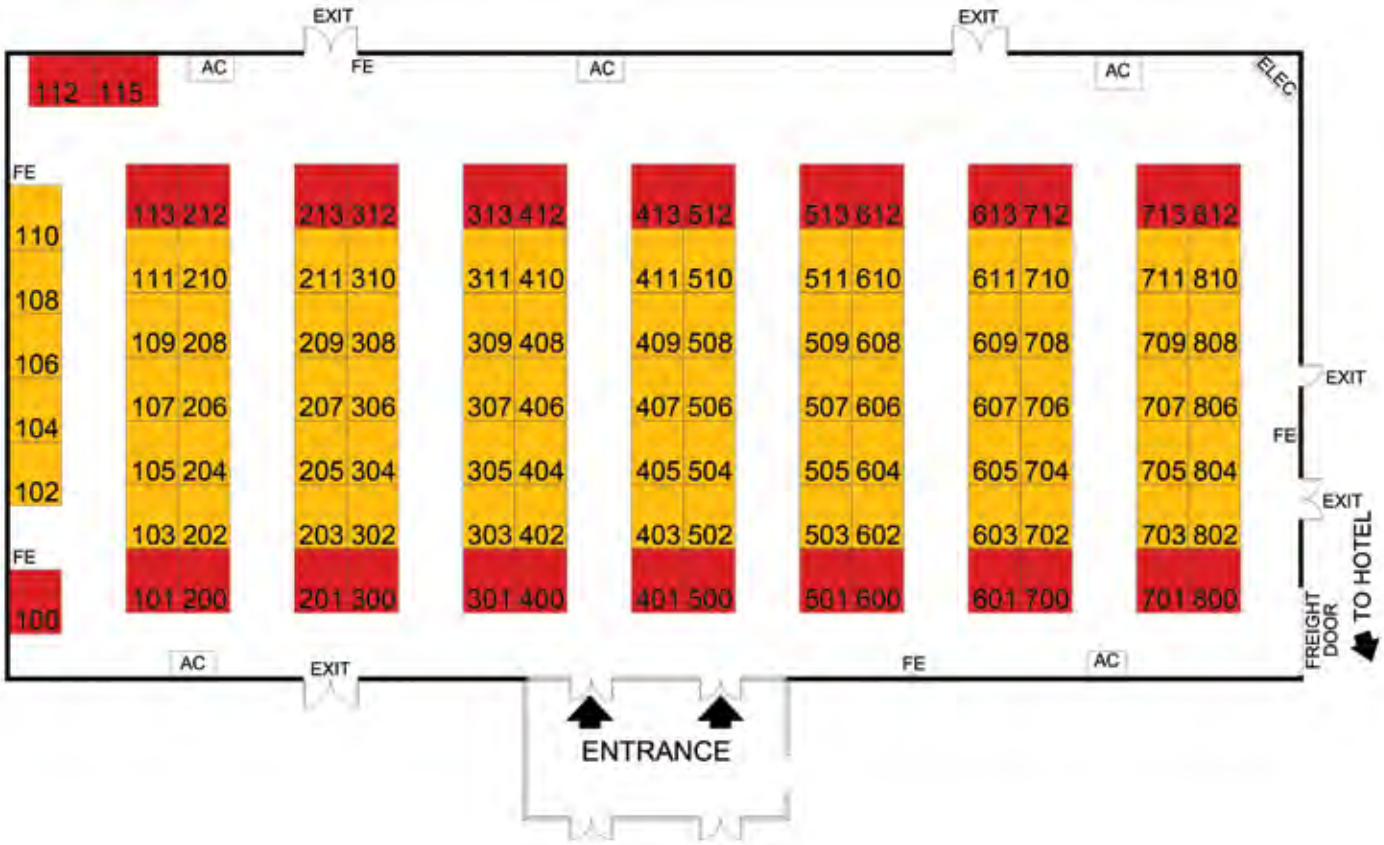
Wednesday, May 30

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 6:30 p.m.

Thursday, May 31

9:00 a.m. - 12:00 Noon / 1:30 p.m. - 4:00 p.m.

Bayview Pavilion



Interactive Presentation Sessions

Wednesday, May 30

Session 37: 9:00 a.m. - 11:00 a.m. / Session 38: 2:00 p.m. - 4:00 p.m.

Thursday, May 31

Session 39: 9:00 a.m. - 11:00 a.m. / Session 40: 2:00 p.m. - 4:00 p.m.

Friday, June 1

Session 41: 8:30 a.m. - 10:30 a.m.

Nautilus Foyer, Lower Level

TECHNOLOGY CORNER EXHIBITORS

3D Systems Packaging Research Center(PRC)
Georgia Institute of Technology
813 Ferst Drive, NW
Atlanta, GA 30332-0560
Phone: +1-404-894-9097
Fax: +1-404-894-3842
www.prc.gatech.edu
Contacts: Dr. Venky Sundaram
Prof. Rao R. Tummala
Emails: vs24@gatech.edu
rao.tummala@ece.gatech.edu
Booth 412

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Hillsboro, OR 97124
Phone: +1-714-745.3193
Fax: +1-503-844-9308
www.agcem.com
Contact: Vern Stygar
Email: vstygar@agcem.com
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473 Sapena Ct. #12
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Phone: +1-480-821-5000
www.amkor.com
Email: sales@amkor.com
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Tokyo, 101-8101 Japan
Phone: +81-3-3296-3991
www.asahi-kasei.co.jp/asahi/en/
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Fax: +1-408-636-9485
www.aseglobal.com
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Email: patricia.macleod@aseus.com
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Phone: +1-602-437-4892
Cell: +1-480-560-0020
www.asmpacific.com
Contact: Terence DeCoteau
Email: terence.decoteau@asmpt.com
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ATO Tech Germany GmbH
Erasmussstr.20
Berlin, Germany 10553
Phone: +49 30/34985-220
Contact: Daniel Schmidt
Email: Daniel.schmidt@atotech.com
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Small Scale Systems Integration and Packaging (S3IP) Center
P.O. Box 6000
Binghamton, NY 13902-6000
Phone: +1-607-777-7270
Contact: Steve Czarnecki
Email: czar@binghamton.edu
Booth 309
The S3IP is a research and development organization that addresses research challenges in electronics packaging system design, process development, prototyping, and manufacturing for academia and the microelectronics industry. Located at Binghamton University, the Center brings together partners from government, industry and academia, providing opportunities for collaborations that will advance microelectronics research and development, with particular focus on electronics packaging design and manufacturing technology; thermal analysis and management for electronics; characterization of materials, surfaces, and physical interfaces for electronics devices and assemblies; and failure analysis and reliability improvement for electronics. Subject areas addressed include packaging of microelectronics, 2.5D/3D chip assemblies, power electronics, and integrated photonics.

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Fax: +1-408-987-9484
www.camtek.com
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www.usa.canon.com/industrial
Contact: Doug Shelton
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38054 Grenoble Cedex 9, France
Phone: +33633661323
www.leti-cea.com/cea-tech/leti/english
Contact: Severine Cheramy
Email: severine.cheramy@cea.fr
Booth 105
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Circuits Multi-Projets (CMP)
46 Avenue Felix Vialet
38000 Grenoble, France
Phone: +33 476 57 46 17
Fax: +33 476 47 38 14
http://mycmp.fr
Contact: Dr. Olivier Guiller
Email: olivier.guiller@mycmp.fr
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Fax: +1-508-222-0220
www.alsic.com
Contact: Tim Davis
Email: tim@jdm-associates.com
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990 N. Bowser, Suite 860
Richardson, TX 75081
Phone: +1-972-664-1568
Fax: +1-972-664-1569
www.covinc.com
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Phone: +1-480-345-9895
www.decatechnologies.com
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Email: garry.pycroft@decatechnologies.com
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Santa Clara, CA 95054-3011
Phone: +1-408-987-3776
Fax: +1-408-987-3785
www.discousa.com
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Email: aris_b@discousa.com
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Contact: Hiromichi Asahara
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8555 Riverside Pkwy.
Tempe, AZ 85284
Phone: +1-602-282-1000
www.versummaterials.com
Contact: Diane Scheele
Email: diane.scheele@versummaterials.com
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A Division of Merck, KGaA Darmstadt, Germany
6555 Nancy Ridge Dr. #100
San Diego, CA 92121
Phone: +1-858-831-0010
Fax: +1-858-455-7108
www.emdgroup.com
Contact: Shaun Bennett
Email: Shaun.Bennett@emdgroup.com
Booth 313

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St Petersburg, Florida, 33716
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Fax: +1-727-201-4605
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7700 South River Parkway
Tempe, AZ 85284
Phone: +1-480-305-2400
Fax: +1-480-305-2401
www.evgroup.com
Email: SalesNorthAmerica@EVGroup.com
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ficonTEC
25 Calle Canela
San Clemente, CA 92673
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Fax: +1-949-388-1489
www.ficontec.com
Contact: Soon Jang
Email: soon.jang@ficontec.com
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www.finetechusa.com
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Heideallee 19
06120 Halle (Saale), Germany
Phone: +49 345-55 89 130
Fax: +49 345-55 89 101
www.cam.fraunhofer.de
Contact: Prof. Dr. Matthias Petzold
Email: matthias.petzold@imws.fraunhofer.de
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13355 Berlin, Germany
Phone: +49 30-46403-100
Fax: +49 30-46403-111
www.izm.fraunhofer.de
Contact: Georg Weigelt
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Fax: +1-714-368-2265
www.henkel.com/electronics
Contact: Eva Laus
Email: electronics@henkel.com
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24 Union Hill Rd
Conshohocken, PA 19428
Phone: +1-610-825-6050
www.heraeus-electronics.com
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Email: james.wertin@heraeus.com
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Fax: +81-3-5533-7077
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Phone: +1-805-482-2870
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Research Triangle Park, NC 27709
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Fax: +1-919-541-1142
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Contact: Alan Huffman
Email: Alan.Huffman@micross.com
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The hermetic packages meet or exceed package evaluation requirements per MI-PRF-38534, Table C-VI. Hermeticity of the packages is less than 10-10 atm cc/sec per MIL-STD-883, method 1014, condition A4. MSI is ISO 9001 certified. Compliance includes RoHS, REACH, and DFAR. Standard deliveries start in just 2 WEEKS!

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Phone: +1-408-516-4611
Fax: +1-408-516-4617
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Phone: +1-215-355-2460
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Phone: +1-408-404-0304
www.nepes.us
Contact: Masayuki Oe
Mobile: +1-669-264-6385
Email: sales@nepes.us
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12701 Grand River Ave.
Brighton, MI 48116
Phone: +1-810-220-4360
Fax: +1-810-220-4300
www.nikonmetrology.com
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Phone: +1-510-445-5400
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2747 Loker Avenue
West Carlsbad, CA 92010
Phone: +1-925-246-1662
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Contact: Aram Kardjian
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Contact: Jim Ries
Email: jries@sonoscan.com
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Website: www.ntktech.com
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Email: mstoops@ntktech.com
Booth 507
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Phone: +82-31-6131147
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Fax: +1-760-931-5191
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Contact: Janine Powell
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Email: tae.yi@us.panasonic.com
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Panasonic Factory Solutions Company of America (PFSA) develops and supports innovative manufacturing processes around the core of circuit manufacturing technologies and computer-integrated manufacturing software—thereby, contributing to the growth and prosperity of our customers' businesses regardless of their mix or volume.

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10900 N. Tantau Ave., Suite 200
Cupertino, CA 95014
Phone: +1-408-861-3979
Fax: +1-408-861-3990
www3.panasonic.biz/em/e/guidance
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Since the founding of our company in 1918, we at Panasonic have been providing better living for our customers, always making people central to our activities, and thus focusing on people's lives. Going forward from this, and based on our innovative electronics technology, we will continue to provide a wide variety of products, systems and services.

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St. Petersburg, FL 33716
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Fax: +1-727-577-7035
www.plasmatherm.com
Email: sales@plasmatherm.com
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Plasma-Therm® is a leading provider of advanced plasma processing equipment. Plasma-Therm systems perform critical process steps in the fabrication of integrated circuits, micro-mechanical devices, solar power cells, lighting, and components of products from computers and home electronics to military systems and satellites. Specifically, Plasma-Therm systems employ innovative technology to etch and deposit thin films. The company's Mask Etcher® series for photomask production has exceeded technology roadmap milestones for more than 15 years. Plasma-Therm's Singulator® systems bring the precision and speed of plasma dicing to chip-packaging applications. Manufacturers, academic and governmental institutions depend on Plasma-Therm equipment, designed with "lab-to-fab" flexibility to meet the requirements of both R&D and volume production. Plasma-Therm's products have been adopted globally and have earned their reputation for value, reliability, and world-class support. Customers consistently rank Plasma-Therm among the top equipment suppliers, with multiple awards in the annual VLSIresearch Customer Satisfaction Survey, including being named "Ranked 1st" Etch and Clean Equipment Supplier five years in a row.

Promex Industries Inc.
3075 Oakmead Village Drive
Santa Clara, CA 95051
Phone: +1-408-496-0222
www.promex-ind.com
Contact: Rosie Medina
Email: rmedina@promex-ind.com
Booth 408

Promex provides heterogeneous assembly processing integrating conventional surface mount technology (SMT) with semiconductor microelectronic packaging and assembly methods for flip chip or chip/wire devices. The company operates a 30,000 sq. ft. assembly facility with Class 100 and 1000 clean rooms in Silicon Valley that is ISO 13485:2003, ISO 9001:2008 certified, ITAR registered and compliant to regulatory requirements for medical products. With a highly skilled engineering team, Promex combines broad technical capabilities, advanced packaging, and microelectronics assembly expertise with scalable manufacturing capacity to produce new medical and bioscience products from concept to production.

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177 US Hwy # 1, No. 306
Tequesta, FL 33469 USA
Phone: +1-404-964-3791
Fax: +1-877-738-8263
Int'l Fax: +1-973-273-2132
www.puretechnologies.com
Contact: Jerry Cohn
Email: jerry@puretechnologies.com
Booth 402

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QualiTau
830 Maude Ave.
Mountain View, CA 94043
Phone: +1-650-282-6226
Fax: +1-650-230-9192
www.qualitau.com
Email: sales@qualitau.com
Booth 307

QualiTau offers a variety of reliability test equipment for characterization and development of new materials used in the manufacturing of Integrated Circuits, as well as process monitoring and process qualification. The MIRA, Infinity, ACE, and Multi-Probe reliability test systems perform tests for Hot Carrier Injection (HC), Dielectric Breakdown (TDDB), and electromigration(EM) of interconnects, TSV, Solder Bump (8 amperes max) at test temperatures of up to 450°C. QualiTau's Test Lab service is ideal for both fabless companies and foundries seeking: Reliable, independent evaluation and analysis. Virtual capacity during times of under-capacity. Cost-effective means of performing tests on an irregular or infrequent basis. A productive and beneficial way to test drive the equipment before committing to a purchase.

Quik-Pak, a Division of Promex
10987 Via Frontera
San Diego, CA 92127
Phone: +1-858-674-4676
FAX: +1-858-674-4681
www.icproto.com
Contact: Casey Krawiec
Email: casey@icproto.com
Booth 408

Quik-Pak, a division of Promex, provides IC packaging, assembly, and wafer preparation services in its ISO 9001:2008 and ITAR registered facility in San Diego, California. Quik-Pak manufactures over molded QFN/DFN packages and pre-molded air cavity QFN packages that provide a fast, convenient solution for prototype to full production needs. Same-day assembly services are provided to shorten time to market. Due to customer demand, Quik-Pak now provides high volume IC assembly services utilizing its automated assembly and molding equipment for production runs in the 10,000s of units. In addition to wire bond assembly, the company assembles flip chips, BGAs, stacked die, sensors, MEMS, and chip-on-board and chip-on-flex assemblies.

Royce Instruments
480 Technology Way
Napa, CA 94558
Phone: +1-707-255-9078
Fax: +1-707-255-9079
www.royceinstruments.com
Contact: Bill Coney
Email: bconey©royceinstruments.com
Booth 108

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16 Jonspin Road
Wilmington, MA 01887
Phone: +1-978-253-6200
Fax: +1-978-658-6349
www.rudolphtech.com
Email: info@rudolphtech.com
Booth 409
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520 Park East Blvd.
New Albany, IN 47150
Phone: +1-812-944-6733
Fax: +1-812-948-5047
www.samtec.com
Contact: Glenn Dixon
Email: glenn.dixon@samtec.com
Booths 602, 604
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Sanyu Rec Company Ltd.
3-5-1 Doucho, Takatsuki
Osaka 569-8558, Japan
Phone: +81-8-0618-73654
www.sanyu-rec.jp
Contact: Yuki Ishikawa
Email: ishikawa@sanyu-rec.jp
Booth 106
Sanyu Rec Company Ltd. is a Japanese electronics material supplier to the semiconductor market place including LED market. With creative development and numerous proprietary technologies, SANYU REC contributes to these growth fields which are driven by environmental considerations and mobile applications. SANYU REC has provided a variety of products centering on encapsulation materials like liquid MUF (mold underfill) material to the market. Capillary underfill, die attach materials, and mold sheets are also in our main product lines. Not only these materials but also VPES (vacuum printing equipment) and pressure oven are in our product lines to offer comprehensive solutions to the customers, which distinguishes us from our competitors. SANYU REC is continuing our effort in development of unique and new technologies, such as LED, one of the areas SANYU REC promotes the shift to.

SavansSys
10409 Peonia Court
Austin, TX 78733
Phone: +1-512-402-9943
www.savansys.com
Contact: Amy Palesko
Email: amyl@savansys.com
Booth 102
SavanSys is the industry standard choice for electronics manufacturing cost modeling. The company began in the mid-nineties with a focus on multi-chip module and PCB fabrication and assembly before expanding into electronics packaging. SavanSys provides both cost modeling services and software products and maintains an extensive library of manufacturing activity costs. Projects range from multi-year ventures focused on detailed supply chain modeling to one-time projects comparing a new technology to the current industry standard. All SavanSys projects and products use activity based cost modeling, which is a bottom-up approach to cost that aggregates individual cost contributors (labor, material, throughput, equipment cost, etc.) for every step in a process flow.

SCHOTT North America, Inc.
400 York Avenue
Duryea, PA 18642, USA
Contact: Dave Vanderpool
Phone: +1-407-288-7695
Fax: +1-407-321-8847
www.us.schott.com
Email: dave.vanderpool@us.schott.com
Booth 308
SCHOTT Advanced Optics is a valuable partner for its customers in developing products and customized solutions for applications in optics, lithography, astronomy, opto-electronics, life sciences, and research. With a product portfolio of more than 120 optical glasses, special materials and components, we master the value chain: from customized glass development to high-precision optical product finishing and metrology. SCHOTT is one of the world's leading suppliers of thin and ultra-thin glass wafers and substrates made of different materials in sizes of between 4" and 12", with various surface qualities and customized features. The use of proprietary production processes, a wide selection of different materials, and continuous expansion of state-of-the-art processing capabilities make SCHOTT's wafer offerings unique in the industry. Process Capabilities include polishing, structuring, edge treatment, ultrasonic washing, and clean room packaging. SCHOTT's portfolio of Thin and Ultra-Thin glasses includes: AF 32® eco, an alkali-free flat glass with a CTE matched to silicon; D 263® eco, a high CTE and high transmission glass; SCHOTT AS 87 eco, a ultra-thin and toughenable glass; B 270®, a crown glass with extremely high CTE; and MEMpax®, an anodic bondable glass with a CTE corresponding to silicon. The portfolio is supplemented by FLEXINITYTM, SCHOTT's glass structuring revolution.

Senju Comtek
2989 San Ysidro Way
Santa Clara, CA 95051
Phone: +1-408-234-4792
Fax: +1-408-963-5399
www.senju-m.co.jp/en
Contact: Ayano Kawa
Email: akawa@senju.com
Booth 611
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SET North America
343 Meadow Fox Ln.
Chester, NH 03036
Phone: +1-603-548-7870
Fax: +1-603-887-2000
www.set-na.com
Contact: Matt Phillips
Email: mphillips@set-na.com
Booth 601

To enable high-density interconnect, SET-North America offers surface preparation and high-accuracy bonding tools with unparalleled performance. For removing native oxides, residual organics or other bond inhibitors, the ONTOS7 Atmospheric Plasma Surface Preparation tool cleans and passivates bonding surfaces to provide high-quality bonds with superior electrical and mechanical integrity. This tool is also effective in activating surfaces to enhance wetting and wicking for aqueous processes or underfill materials. The device bonders manufactured by SET are globally renowned to deliver unsurpassed bonding accuracy (±0.5 µm) at high temperatures and forces for chips and substrates ranging from tiny, fragile components up to 300 mm wafers. With a product portfolio ranging from manually loaded versions to fully-automated operation, SET offers bonding and nanoimprint solutions with high flexibility and field-proven reliability.

SHENMAO AMERICA, Inc.
2156 Ringwood Ave.
San Jose, CA 95131
Phone: +1-408-943-1755
www.shenmao.com
Contact: Hans Schiesser
Mobile: +1-408-529-6626
Email: hschiesser@shenmao.us
Booth 107

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Shin-Etsu MicroSi, Inc.
10028 S. 51st St.
Phoenix, AZ 85044
Phone: +1-480-893-8898
Fax: +1-480-893-8637
www.microsi.com
Email: info@microsi.com
Booth 306

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Shinkawa USA, Inc.
1177 S. Porter Court
Gilbert, AZ 85296
Phone: +1-480-831-7988
www.shinkawa.com/en/
Contact: Doug Day
Email: d_day@shinkawausa.com
Booth 104

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Shinko Electric America
1280 East Arques Avenue MS 275
Sunnyvale, CA 94085
Phone: +1-408-232-0493
Fax: +1-408-955-0368
www.shinko.com
Contact: Michael Hudgens
Email: Michael.hudgens@shinko.com
Booth 512

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SPTS Technologies Ltd.
Ringland Way, Newport, NP18 2TA
Phone: 0044 1633 414 000
www.SPTS.com
Contact: Greg Hollingshead
Email: Greg.Hollingshead@orbotech.com
Booth 200

SPTS Technologies, an Orbotech company, designs, manufactures, sells, and supports advanced etch, PVD, CVD and MVD® wafer processing equipment and solutions for the global semiconductor and micro-device industries, with focus on the Advanced Packaging, MEMS, high-speed RF device, power management and LED manufacturing. With the acquisition of SPTS, Orbotech is able to offer a broader range of process solutions for Advanced Packaging, which includes Orbotech's Inkjet/3D printing solutions for die level printing and UV Laser Drilling for through mold vias. SPTS has manufacturing facilities in Newport, Wales and Allentown, Pennsylvania, and operates across 19 countries in Europe, North America and Asia-Pacific.

STATS ChipPAC, a JCET Company
46429 Landing Parkway
Fremont, CA 94538
Phone: +1-510-979-8000
Fax: +1-510-979-8001
www.statschippac.com
Contact: Lisa Lavin
Email: Lisa.Lavin@statschippac.com
Booth 201

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2675 Antler Drive
Carson City, NV 89701
Phone: +1-619-208-0748
www.taiyo-hd.co.jp/en/
Contact: Yuya Suzuki
Email: YuyaS@taiyo-america.com
Booth 605
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TATSUTA USA Inc.
101 Metro Drive, Suite 355
San Jose, CA 95110
Phone: +1-408-642-1938
Fax: +1-408-982-3391
www.tatsuta.com
Contact: Mike Sakaguchi
Email: m-sakaguchi@tatsuta.com
Booth 700
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TDK Corporation
475 Half Day Road
Suite 100
Lincolnshire, IL 60069
Tel: +1-847-795-2163
www.tdk.com
Contact: Philip Couts
Email: philip.couts@us.tdk.com
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TechSearch International Inc.
4801 Spicewood Springs Rd., Ste 150
Austin, TX 78759
Phone: +1-512-372-8887
Fax: +1-512-372-8889
www.techsearchinc.com
E-mail: tsi@techsearchinc.com
Contacts: Jan Vardaman and Becky Travelstead
Booth 400
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TECNISCO, LTD.
2-2-15, Minami-Shinagawa
Shinagawa-ku
Tokyo, 1400004, JAPAN
Phone: +81-3-3472-6963
Fax: +81-3-3472-1316
www.tecnisco.co.jp/en/
Contact: Haruka Aizawa
Email: h-aizawa@tecnisco.co.jp
Booth 110
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ThreeBond International, Inc.
6184 Schumacher Park Dr.
West Chester, OH 45069
Phone: +1-408-638-7091
Fax: +1-513-779-7375
www.threebond.com
Contact: Kensuke Kitamura
Email: kkitamura@threebond.com
Booth 804
Since founded in 1955 in Japan, Threebond has been offering the adhesive/sealant products globally with its cutting-edge technologies. Threebond has developed networks across six regions: Japan, North/central Americas, south America, Europe, Asia, and China. Threebond offers unique products such as hot water removable temporary bonding adhesive, UV-curing black adhesive, 60°C x 1 minute curing elastic adhesive, moisture blocking adhesive, UV-activated dual curing epoxy, ultra low viscosity (2cP) UV-curing adhesive, high thermally conductive epoxy, etc. Over 1,600 products will provide solutions to the problems you are facing. Ask Threebond if you need any specific adhesives or sealants.

Teikoku Taping Systems
5090 N 40th St. Ste. 140
Phoenix, AZ 85018
Phone: +1-602-367-9916
www.teikoku-taping.com
Contact: Robert Garrett
Email: robert.garrett@teikoku-taping.com
Booth 710
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TOK America
190 Topaz St.
Milpitas, CA 95035
Phone: +1-408-934-8904
www.tok.co.jp
Contact: Yoshi Arai
E-mail: Yoshi.arai@tokamerica.com
Booth 303
TOK's unique packaging / MEMS manufacturing technologies, in terms of both materials and equipment. We have developed and commercialized optimal photoresists and processing equipment for a range of packaging processes. Photoresists for packaging are available for a wide range of production technologies including wafer-level CSP, SiP, RDL, TAB

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Toray International America
411 Borel Ave., Suite 520
San Mateo, CA 94402
Phone: +1-650-341-7152
Fax: +1-650-341-0845
www.toray.US/products
Contact: Hiroyuki Niwa
Email: h.niwa@toray-intl.com
Booths 405, 407

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Towa USA Corporation
1430 Tulley Rd., Ste. 416
San Jose, CA 95122
Phone: +1-408-779-4440
Fax: +1-408-779-4413
www.towajapan.co.jp/en/
Contact: Naoki Hamada
Email: n_hamada@towajapan.co.jp
Booth 701

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TRESKY GmbH
Neuendorfstrasse 19 B
16761 Hennigsdorf
Germany
Phone: +49 (0) 3302 866 92-0
www.tresky.de/en/
Contact: Daniel Schultz
Email: daniel.schultze@tresky.de
Booth 607

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Unisem
2241 Calle de Luna
Santa Clara, CA 95054
Phone: +1-408-734-3222
Fax: +1-408-562-9971
www.unisemgroup.com
Contact: Gil Chiu
Email: gchiu@unisemgroup.com
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611, rue Aristide Berges
ZA du Pre Millet
38330 Montbonnot Saint Martin, France
Phone: +33-456-52-6800
Contact: Tim Anderson
Email: contact@unity-sc.com
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UnitySC is recognized worldwide as a key player in inspection and metrology, combining advanced technologies in automated optical inspection and 3D imaging with microscopy, temporal-mode interferometry, and spectrometry, which enables customers to deliver higher yields and faster time to market. UnitySC provides standard and customized solutions adapted to specific industrial needs and constraints, enabling a new era in process control. Headquartered in Grenoble, France, the company maintains offices in Taiwan and is supported by a network of representatives and distributors. Customers include the largest foundries, integrated device manufacturers, outsourced semiconductor assembly and test service providers, and R&D centers.

Xperi - Invensas
3025 Orchard Parkway
San Jose, CA 95134
Phone: +1-408 321 6000
Fax: +1-408 321 8257
www.xperi.com
Contact: Andrew Kim
Email: Andrew.kim@xperi.com
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XYZTEC
55 Sterling Street
Clinton, MA 01510
Phone: +1-978-880-2598
www.xyztec.com
Contact: Tom Haley
Email: tom.haley@xyztec.com
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Livermore, CA 94551
Phone: +1-925-373-8353
www.yieldengineering.com
Contact:Nicole Williams-Pruitt
Email:nwilliams-pruitt@yieldengineering.com
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www.yole.fr
Contact Camille Veyrier
Email: veyrier@yole.fr
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Pleasanton, CA 94588
Phone: +1-925-701-3600
www.zeiss.com/pcs
Contact: Victoria Doll
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Phone: +1-408-890-2831
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+1-613-720-2994

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+1-319-295-6687

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lo@itri.org.tw
+886-3-591-7024

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+49-162-8514983

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Gordon Elger
Technische Hochschule Ingolstadt
gordon.elger@thi.de
+49-841- 934-8284

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Ping Zhou
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pzhou@ldxoptronics.com
+1-865-981-8822

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mmayer@uwaterloo.ca
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John Hunt
Advanced Semiconductor Engineering, Inc.
john.hunt@aseus.com
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1 Research Circle, Niskayuna, NY 12309 Phone: +1-518-587-3429
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Abstracts must be received by October 8, 2018. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

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69th ECTC Professional Development Courses Chair
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Phone: +1-512-845-3287
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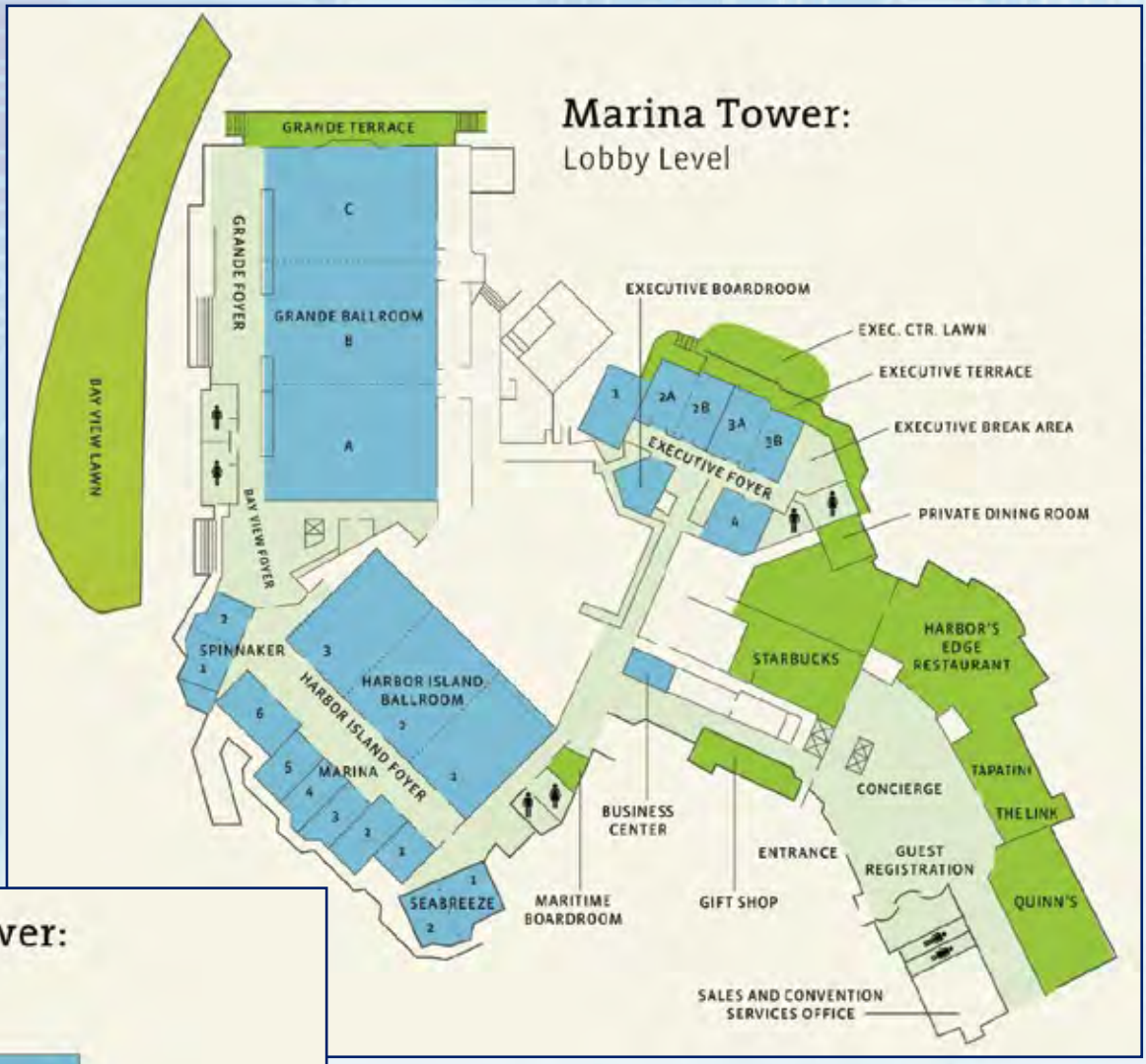


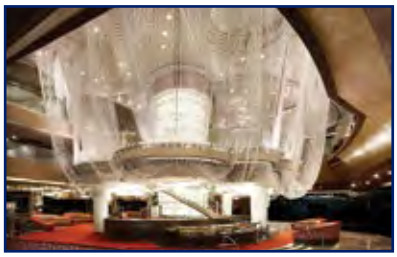
69TH ELECTRONIC COMPONENTS & TECHNOLOGY CONFERENCE

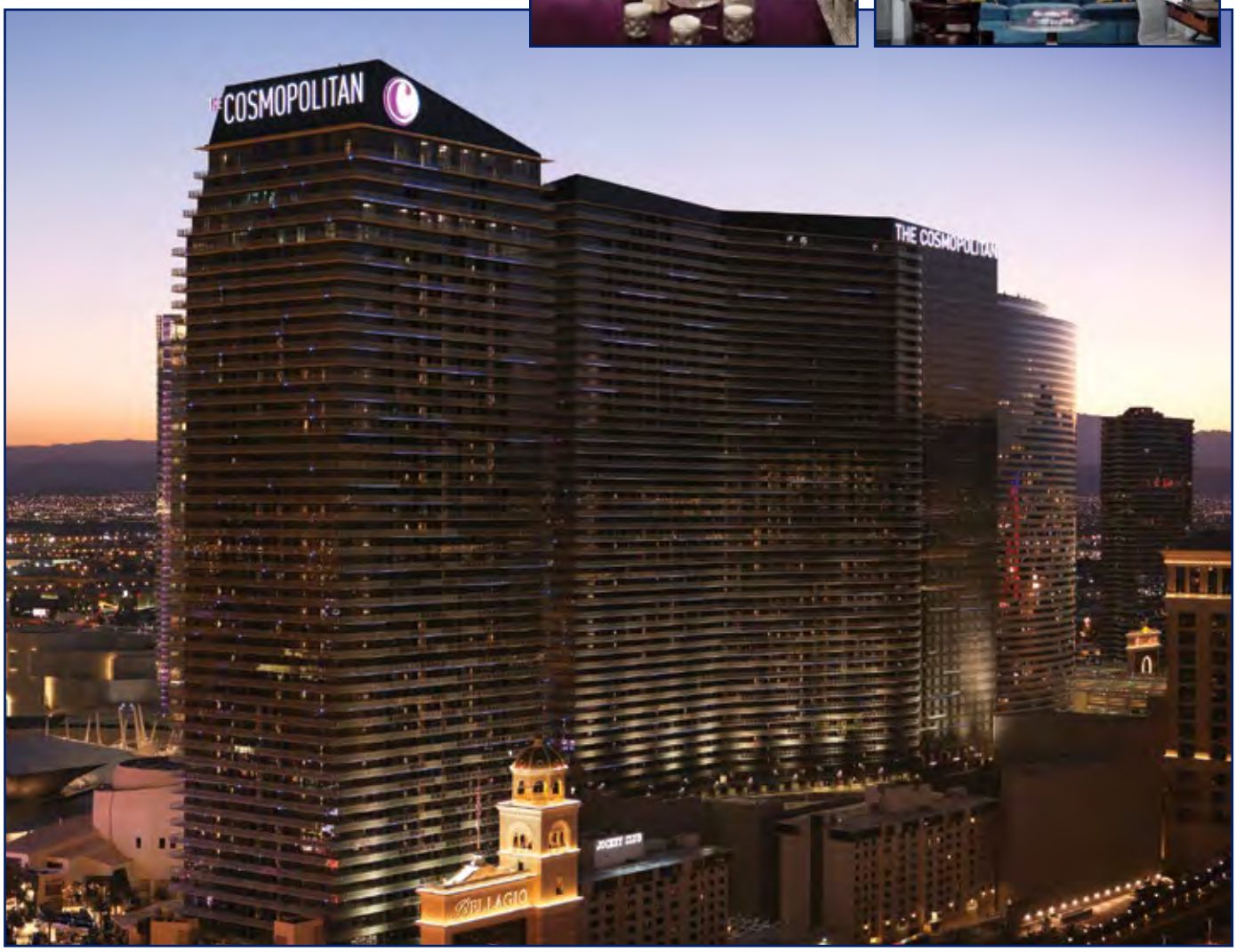
The Cosmopolitan of Las Vegas
Las Vegas, Nevada, USA
May 28 - May 31, 2019

The spectacular city of Las Vegas awaits you in 2019. As the entertainment capital of the world, there are over 100 spectacular live shows and entertainment venues to see daily. Las Vegas also touts world-class cuisine with an array of restaurants by world famous chefs.

Next year ECTC will be back at The Cosmopolitan hotel located directly adjacent to the world-renown Bellagio and its famed fountain show. The hotel itself is a $4 billion stunning architectural statement with a chandelier bar that spans two stories. It also has some of the country's top chefs, three distinctive pools, and 44,000 square feet of salon, spa, and fitness areas.

Should you want to put aside Vegas' bright lights and casinos, visit many of the natural wonders that surround this city. Over five major parks and wonders are in close proximity. From Red Rock Canyon to Death Valley or Hoover Dam to Grand Canyon National Park, there is so much to do and see.





Conference At A Glance

REGISTRATION

Monday
3:00 p.m. - 5:00 p.m.

Tuesday
6:45 a.m. - 5:00 p.m.

Wednesday
6:45 a.m. - 4:00 p.m.

Thursday
7:30 a.m. - 4:00 p.m.

Friday
7:30 a.m. - 12:00 p.m.
Bayview Foyer

TECHNOLOGY CORNER EXHIBITS

Wednesday
9:00 a.m. - 12:00 p.m.
1:30 p.m. - 5:30 p.m.
Reception - 5:30 p.m. - 6:30 p.m.

Thursday
9:00 a.m. - 12:00 p.m.
1:30 p.m. - 4:00 p.m.
Bayview Pavilion

TUESDAY - FRIDAY

Speaker Preparation Room
7:00 a.m. – 5:00 p.m.
Marina 3

TUESDAY ONLY

PDC Instructors and Proctors Briefing & Breakfast
7:00 a.m. – 7:45 a.m.
Grande Ballroom B

Professional Development Courses (PDCs)
8:00 a.m. – Noon
1:15 p.m. - 5:15 p.m.
See page 9 for locations

EPS Heterogeneous Integration Roadmap Workshop
8:00 a.m. – 5:00 p.m.
Executive Center 1 & 4

Special Sessions: Emerging Technologies Special Session
10:00 a.m. – 11:30 a.m.
Grande Ballroom C

ECTC Special Session
2:00 p.m. – 3:30 p.m.
Grande Ballroom C

Refreshment Breaks
10:00 a.m. – 10:20 a.m.
3:00 p.m. – 3:20 p.m.
Harbor Island Foyer, Grande Ballroom A Foyer, and Nautilus Foyer

Lunch for PDCs
12 p.m. Noon
Grande Ballroom B

Technology Corner SetUp
1:00 p.m. – 5:00 p.m.
Bayview Pavilion

ECTC Student Reception
5:00 p.m. – 6:00 p.m.
Executive Center 3

General Chair's Speakers Reception
6:00 p.m. – 7:00 p.m.
Grande Ballroom B
By invitation only

Young Professionals Panel and Reception
7:00 p.m. – 7:45 p.m.
Harbor Island 3

ECTC Panel Session
7:45 p.m. – 9:15 p.m.
Harbor Island 1 & 2

WEDNESDAY - FRIDAY

Speakers Breakfast
7:00 a.m. – 7:45 a.m.
Grande Ballroom A

Sessions
8:00 a.m. – 11:40 a.m. or
1:30 p.m. – 5:10 p.m.
see pages 11 - 22 for specifics

Sessions 1, 7, 13, 19, 25, 31
Harbor Island 1

Sessions 2, 8, 14, 20, 26, 32
Harbor Island 2

Sessions 3, 9, 15, 21, 27, 33
Harbor Island 3

Sessions 4, 10, 16, 22, 28, 34
Nautilus 1 & 2

Sessions 5, 11, 17, 23, 29, 35
Nautilus 3 & 4

Sessions 6, 12, 18, 24, 30, 36
Nautilus 5

Interactive Presentations
9:00 a.m. - 11:00 a.m. or
2:00 p.m. - 4:00 p.m.
8:30 a.m. - 10:30 a.m. on Friday
see pages 23 - 26 for specifics

Sessions 37 - 41
Nautilus Foyer

Lunch
12 p.m. - 1:15 p.m.
Grande Ballroom

Refreshment Breaks
9:15 a.m. – 10:00 a.m.
2:45 p.m. – 3:30 p.m.

Wednesday & Thursday
Bayview Pavilion

Friday
Harbor Island Foyer
Nautilus Foyer

WEDNESDAY ONLY

Women's Panel & Reception
6:30 p.m. – 7:30 p.m.
Harbor Island 3

ECTC Plenary Session
7:30 p.m. – 9:00 p.m.
Harbor Island 1 & 2

THURSDAY ONLY

68th ECTC Gala Reception
6:30 p.m. – 7:30 p.m.
Bayview Lawn
(Backup Location: Grande Ballroom)

IEEE EPS Seminar
8:00 p.m. – 9:30 p.m.
Harbor Island 1 & 2

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