ACCEDE 2022 Workshop on COTS
Components for Space Applications

COTS in ESA missions: lessons learnt

Silvia Massetti/Karin Lundmark

21/10/2022

ESA UNCLASSIFIED – For ESA Official Use Only

COTS in ESA missions; lessons learnt

Outline

- Looking back – also on problems
- Looking at current situation
- Lessons learnt from CPPA test campaigns

COTS in ESA missions; lessons learnt

Looking back

- Nothing new!
- First wave of COTS started in the 90ies.
  - Synergies with military e g through PURE (Plastic Used in Rugged Environment council)
- Also increase of photonics made use of COTS necessary
  - Synergies with telecom through Telcordia (still used)
- Normative references;
  - RNC-CNES-Q-ST-60-100 issue 1 2003
  - PEM-INST-001 200
  - ECSS-Q-ST-60-13C 2013
- Early 2000 missions using COTS include Proba 2,GAIA, METOP, Goce and SMOS

PLASTIC PACKAGED IC IN SPACE APPLICATION
TWO CASE STUDIES OF PEM EVALUATION

Karin Lundmark
Saab Ericsson Space
405 25 Gothenburg, SWEDEN
phone: +46 31 735 40 45
telefax: +46 31 735 40 00
karin.lundmark@space.se

from ESCCON 2000

Abstract

This paper will describe two cases of PEM evaluation for space application. They differ in many ways, e. g.:

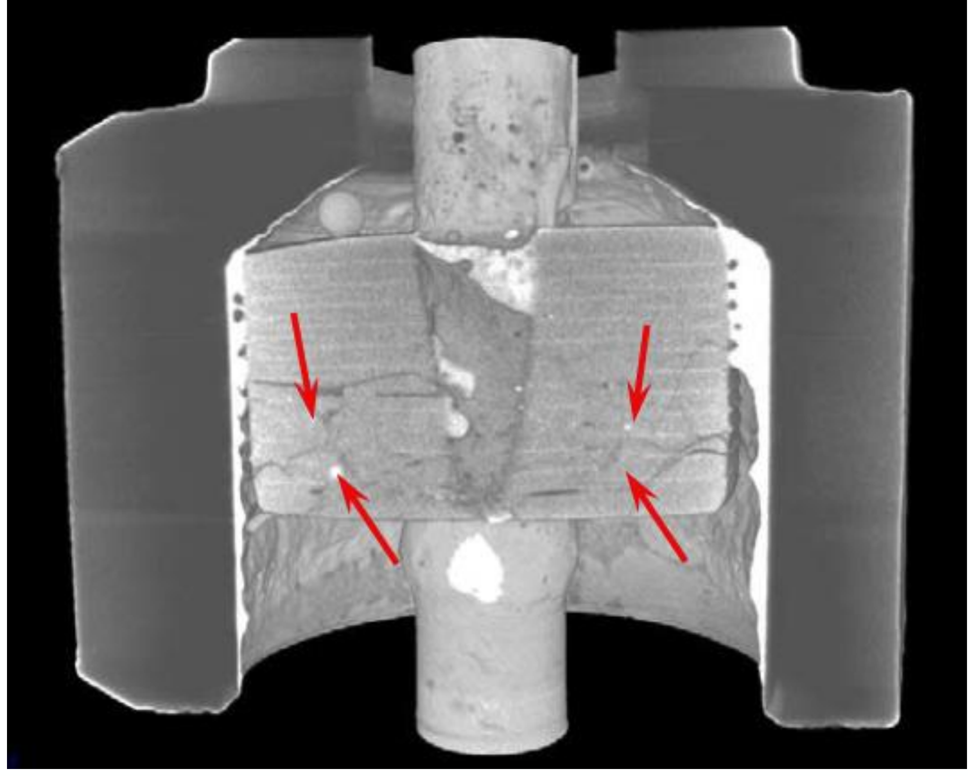
- digital versus analogue part
- program requirements
- test on sample basis only versus screening and sample testing

Focus will be mainly on the second evaluation, which is in process. The PEM in this study is an 8-bit A/D converter, AD9054 from Analog Devices. First case was a DRAM, KM44V16004BK-6 from Samsung.

COTS in ESA missions; lessons learnt

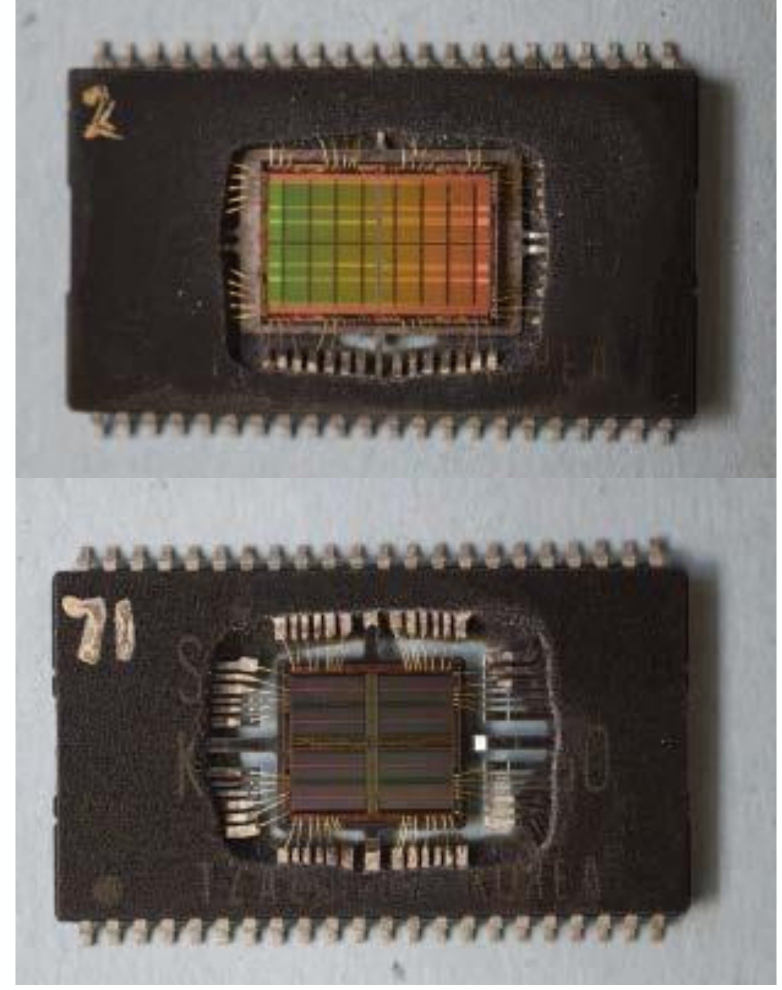
Looking back – in-orbit failures

Instrument catastrophic failure due to feed through filter



PCNS Passive Components Networking Days 2017

Mass memory latch-up due to mix of die revisions in single date code.

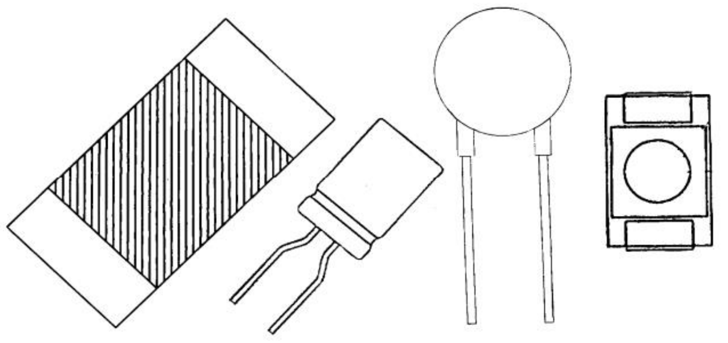


COTS in ESA missions; lessons learnt

Looking at current situation

- All missions now use COTS
- Extensive use of COTS for performance, availability and cost.
- Updated and new normative references, ECSS tailoring and guidelines exist but
  - is the COTS question now reduced to use as is?
- Synergies with automotive AECQ.
- ESA is, and have been, extensively supporting COTS test campaigns.
- COST for COTS testing is high, some historic numbers
  - ADS presented in ESCCON 2011 1.3 Meuro for GAIA (5 ICs)
  - CNES presented in Seressa 2017 total cost from 150keuro for simple IC to 1.5Meuro for complex IC
- No accurate numbers for support to lower class programs which may be addressing e g test at board or unit level.

STRESS TEST QUALIFICATION
FOR
PASSIVE COMPONENTS



Automotive Electronics Council
Component Technical Committee

PLATO COTS CASE

- Just after the adoption, PLATO payload consortia already identified the need of a specific list of COTS Ics to be used in both Normal and Fast Front Electronic Unit
    - Heritage from Euclid design
    - High cost of similar space qualified ICs and due to the high number of components needed to complete the project, space qualified alternative was not compatible with funding scheme
    - High power consumption of similar space qualified parts
    - Specific performance not available in space qualified similar components

The results of COTS evaluation needed to be available and successfully completed before accepting the COTS into the FM H/W baseline and hence for the EQM. Therefore the activities needed to be planned and initiated well in advance w.r.t. the date for which the funding resources of the members of payload consortia could be available

THIS WAS ONE OF THE MAIN REASON FOR SETTING UP A CPPA FOR PAYLOAD

PLATO COTS CASE: LIST OF COTS UNDER EVALUATION

- **EL7457CSZ-T7:** 40MHz Non-Inverting Quad CMOS Driver ideal for driving highly capacitative loads , like CCD (2.19$ per piece, 1000 pieces procured)
  - Pure tin finish, no traceability to the lot
- **AD8021ARZ-REEL7:** Low Noise, High Speed Amplifier for 16-Bit Systems ideal as ADC pre amplifier (1.31$ per piece, 2000 pieces procured)
  - Pure tin finish, no traceability to the lot
- **AD8065ARZ-REEL7:** High Performance, 145 MHz FastFET Op Amps with exceptionally low noise operation (7.0 nV/√Hz and 0.6 fA/√Hz) as well as very high input impedance (1.62$ per piece, 1004 pieces procured)
  - Pure tin finish, no traceability to the lot
- **ADS1258MPHPTEP:** 16-CHANNEL, 24-BIT ANALOG-TO-DIGITAL CONVERTER, delta-sigma (ΔΣ) (~ 17$ per piece, 277 pieces procured)
  - Lot traceability insured in the CoC , NO pure tin finish
- **AD7961BCPZ:** 16-Bit, 5 MSPS PulSAR Differential ADC ideal for high speed data acquisition (~ 20$ per piece, 490 pieces procured)
  - QFN package with bottom contacts in pure tin and vertical side in Cu; no retinning (RFD); no lot traceability
- **DG612DY:** High-Speed, Low-Glitch D/CMOS Analog Switches (0.8 euro per piece -2000 pieces procured)
  - Obsolete parts, lot traceability and wafer lot traceability in the CoC, same wafer lot of Euclid one; no pure tin
- **C1812C104J1GACAUTO** from KEMET: Automotive,C0G Ceramic, 0.1 uF, 5%, 100 VDC, Ultra-stable, Sn matte, ~0.5 euro (1 reel)

EVALUATION PROGRAM

RECEIVING 100% of samples
INCOMING 100% of samples (DPR + EVI 100 % NOTE 1
+ Serialization "internal procedure")

- OUTGASSING
  ECSS-Q-ST-70-02C
  NOTE 2
  Qty: TBD samples
- EVALUATION
  C/A
  According to Para.6
  Qty: 5 samples
- EVALUATION
  ELECTRICAL
  CHARACTERIZATION
  According to Para.7
  Qty: 10 samples
- EVALUATION
  RVT (TID)
  According to
  PTO-ATN-PL-PLA-0015
  Qty: 11 samples
- EVALUATION
  RVT (SEE)
  According to
  HRX/SEP/00151
- EVALUATION
  LIFE TEST
  According to Para. 10
  Qty: 10 samples
  - DPA
    According to Para. 11
    Qty: 3 samples
- SCREENING
  According to Para. 12
  Qty: 100 % samples
- EVALUATION
  THB
  According to Para. 8
  Qty: 10 samples
- EVALUATION
  T/C
  According to Para. 9
  Qty: 10 samples

THB → ← HAST

Test sequence.

Parts with pure tin finish have been submitted to retinning process without stand-off and then to retinning verification program.
All the evaluation program with the exception of TID/SEE/CA and outgassing have been performed on retinned samples

TID was not performed on DG612DY because from same wafer lot than Euclid one . SEE was performed because not performed in the frame of Euclid.
SEE was not performed on AD8021 and AD8065 because bipolar technology

ELECTRICAL PERFORMANCE IN APPLICATION CONDITION

- Electrical test condition very rarely can be exactly performed with the precision that the set up at manufacturer premises can reach.
- Complex device requires to be tested in ATE (automatic test equipment)
- There are also problems of calibration and possible offset between the set up designed by the test house and the one used by manufacturer
- Test set up could be complex and requires effort, time and skills to be designed, to develop software and to calibrate the system. Example
- In addition for the WCA , users need to understand drift and worst case of electrical characteristic in the specific operating condition (generally not available in data sheet). Example
- **No support from manufacturer is available**

Test set up / Test conditions / Acceptable Limits needs to be negotiated carefully with the user and test house in order to reduce COST, TIME and RISK

CSAM METHODOLOGY AND NCR

- C-SAM (C mode scanning acoustic microscopy) is used to detect delamination, voids, defects in plastic packages and in the interface between the plastic package and the die or the lead frame.
- It is required by ECSS-Q-ST-60-13C Rev.1 in CA and before preconditioning and thermal cycling in evaluation and LAT
- It is widely used by some ICs manufacturers. The method used is J-STD-020E
- Most of the plastic COTS line items under evaluation showed frequent and important delaminations.
- Some of them already at time T0 : they were not removed from testing but on purpose submitted to stressful test like THB, thermal cycling to verify the evolution
- There were also cases of severe delaminations observed along lead fingers but the subsequent cross –section was not able to reveal
- Many lots (like DG612DY and ADS1258) were showing delaminations at time T0 with important evolutions during life test. However no effect in the electrical characteristic was observed. Many packages show also inhomogeneity clusters most of the time due to density inhomogeneity in plastic polymerizations or small voids far from the chip surface

All NCRs relevant to CSAM were analysed in details, at the end they were closed with use as is based essentially on the general good electrical behaviour of the parts

CSAM to be used only for qualitative analysis? How TI and ST will approach their “0” delamination approach in plastic line for space or in LEO line?

IS SCREENING USEFUL?

There were many discussions during the revision of ECSS-Q-60-13C (new revision finally published in May 2022) on the utility of performing screening.

- Some primes pointed out the risk of performing 100% electrical test on FM parts.
- if not calibrated and verified properly, test set up can induce unexpected electrical over stress that can jeopardise the reliability of the parts
- Test conditions need to be controlled carefully and established with care (e.g. temperature of burn in cannot just be based on the condition applied in reliability report of the manufacturers . Some time manufacturers run life test in special carrier in order to be able to push higher the temperature)

So screening is dangerous?

Among 6 ICs under test we had no reject in electrical test during screening in 5 out 6 cases.

BUT

EL7457CSZ-T7 lot had indeed 32 rejects for parameters out of limits in electrical measurement in low-room-high temperature over 760 screened S/Ns

A different lot of EL7457CSZ-T7 underwent to evaluation and screening in Euclid with more benign statistics. So if we would have accepted the heritage approach: no failure in previous lot hence screening not useful – these 32 failures would have escaped and accepted for flight

SOME LESSON LEARNT from SEE TEST CAMPAIGN

- It is important to design carefully the test set up in order to be able to command also reset pin or power down mode pins if exist to recover from a SEFI

- Test procedures should carefully take into account SEFI and do not apply directly hard power down in case of stuck output or anomalous output values

- User of COTS devices should be deeply involved in the design of the test set up and in the test procedures approval in order to gather results that are representative and can give useful input to FDIR, WCA, availability analysis, and design of possible mitigation strategies

- SEFI and long errors could have very different signatures and are quite frequent in ADC and DAC

ECSS-Q-ST-60-13C Rev1 vs. classical approach

The case of automotive capacitors procured before/after the new revision of 60-13

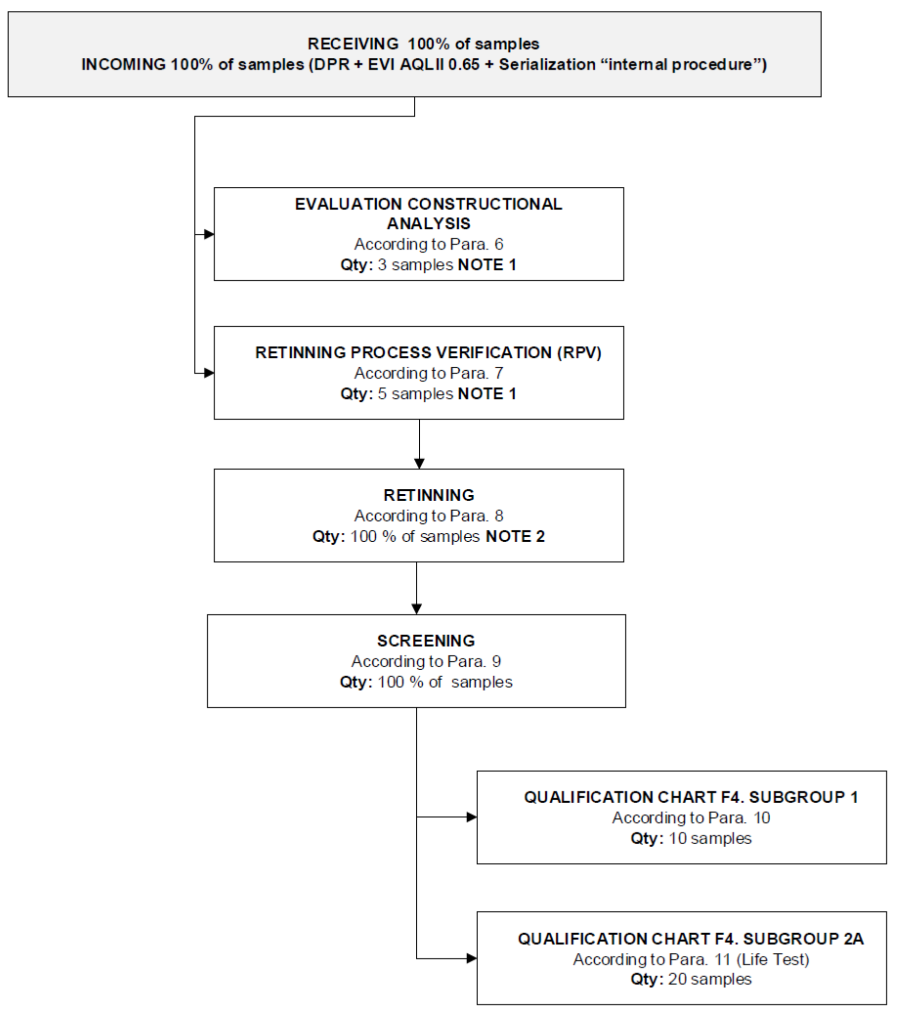


FIGURE 1: TEST SEQUENCE

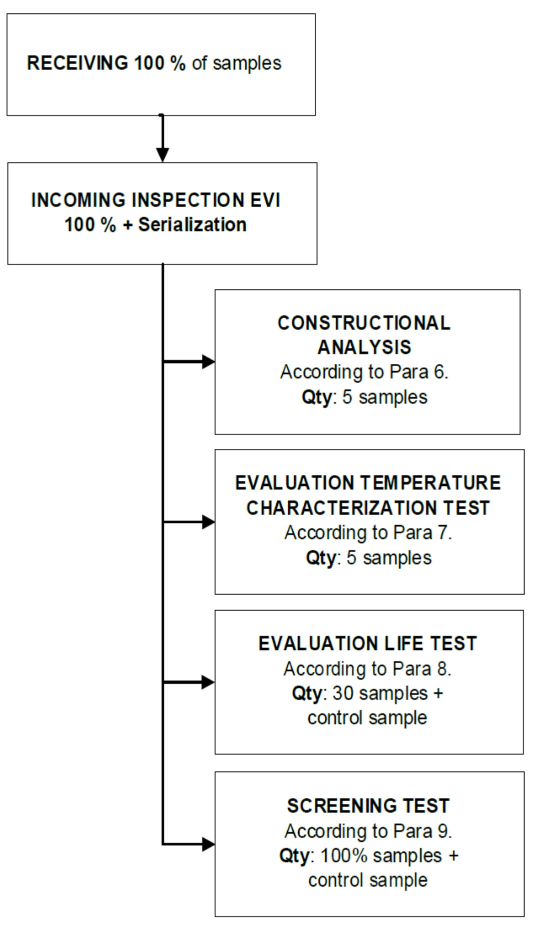


FIGURE 1: TEST SEQUENCE

Cost saving of ECSS-Q-60-13C Rev.1 for AUTO Capacitors is ~ 35%

Time saving of ECSS-Q-60-13C Rev.1 for AUTO Capacitors is ~ 12 weeks

ECONOMIC EFFORT

Total cost for ESA :
~ 637Keuro

Total cost for users:
~ 364Keuro

~ 2 years for completion of COTS evaluation /screening

Required full time expert test engineers to design and develop reliable/calibrated test set up and relevant SW

User	Description
CNFEMS	DG612DY-EVAL (WO-3)
CFFEDL	AD8021ARZ-EVAL (WO-5)
CNFEMS	EL7457CSZ-EVAL (WO-4)
CFFEDL	1258MEP Linearity (WO-2)
CFFEDL	1258MEP SEE (WO-5)
CNFEMS	EL7457CSZ SEE (WO-5)
CNFEMS	AD8065ARZ-EVAL (WO-5)
CNFEMS	AD7961BCPZ-EVAL (WO-4)
CNFEMS/ CFFEDL	GAIN STABILITY (WO-4)
CNFEMS/ CFFEDL	Swicth on at -45ºC (WO-5)
CNFEMS	AD7962BCPZ SEFI (WO-6)
CFFEDL	1258MEP-EVAL (WO-6)
CFFEDL	KEMET C1812C104J1GACAUTO Evaluation (WO-9)