TOE10G-IP Demo on VC707 Instruction

Rev1.0   13-Jun-14

This document describes the instruction to run TOE10G-IP for transferring 10-Gb data between VC707 development board and PC through 10Gigabit Ethernet. This demo can select to run with supported and not supported Jumbo frame PC.

1   Environment Setup

As shown in Figure 1, to run TOE10G-IP send demo, please prepare
1) VC707 Development board
2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
3) 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between VC707 Development board and PC
4) micro USB cable for programming FPGA between VC707 Development board and PC
5) "send_tcp_client_10G.exe" and "recv_tcp_client_10G.exe", provided by Design Gateway, which are test application available on PC
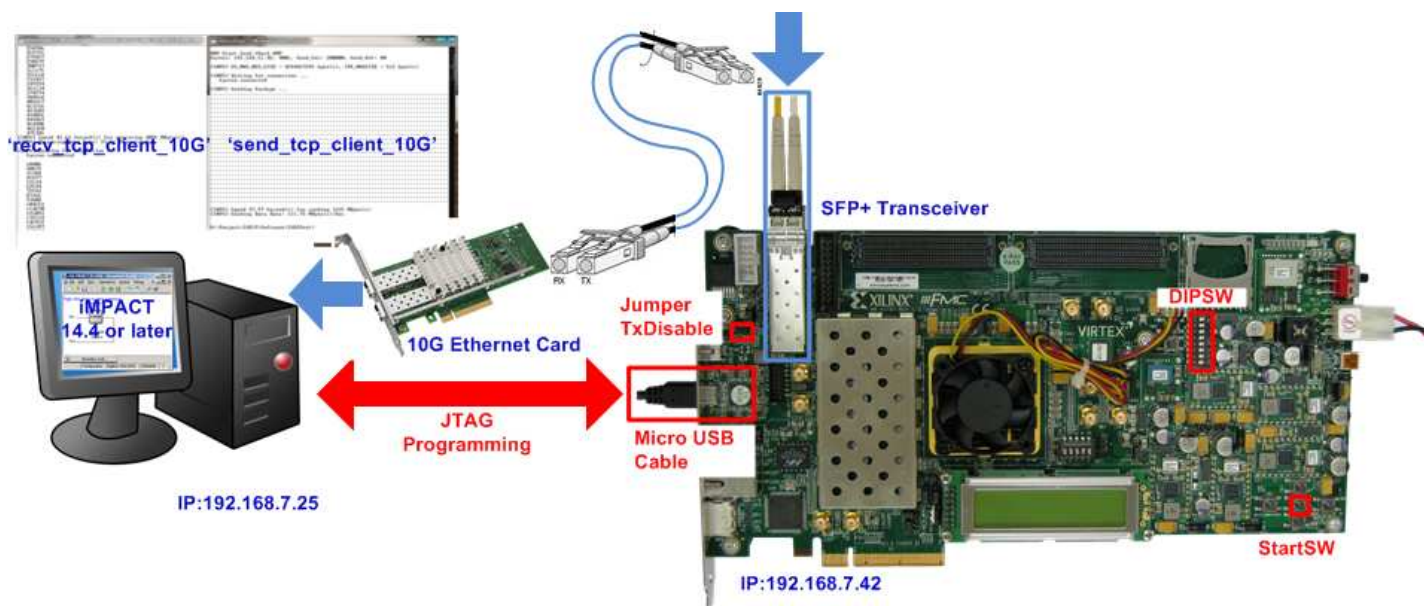

Figure 1 TOE10G-IP Demo Environment Setup

Note: Test result in this document is captured by using following test environment.
[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html
[2] 10-Gigabit SFP+ Transceiver: Avago AFBR-703SDZ
http://www.avagotech.com/pages/en/fiber_optics/ethernet/10_gbe/afbr-703sdz/
[3] Fiber Optical Cable: TE Connectivity 2105027-3
http://www.te.com/catalog/pn/en/2105027-3
[4] PC: Motherboard ASUS P8Z77-V, 8 GB RAM, 64-bit Windows7 OS

2   Demo description

There are two test modes, i.e. sending mode and receiving mode between VC707 development board, running as TCP Server, and PC which running as TCP Client. Each transfer mode requires different test application on PC and different DIPSW setting on VC707 development board. The definition of DIPSW and LED on VC707 development board are described in Table 1 and Table 2.

Table 1 DIPSW Setting Definition

DIPSW	OFF	ON
Bit 1	Sending mode by using non-Jumbo frame (1456 bytes)	Sending mode by using Jumbo frame (8960 bytes)
Bit 2	Sending mode	Receiving mode
Bit 3	Receiving mode without data verification	Receiving mode with data verification

Table 2 LED Definition

GPIO LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (SW6-CenterSW) has already been pressed and confirm IP address setting on PC that is correct.
1	BLINK: Operation timeout or cable lost	Normal operation
2	Sending mode in Jumbo frame.	Sending mode in non-jumbo frame
3	BLINK: data verification is fail in receiving mode ON: Port is established.	No operation

Note:
- DIPSW setting must not be changed during operation.

More details about each test mode are follows.

2.1 Sending mode

In this mode, 32 GB data will be transferred from VC707 development board to PC, and "recv_tcp_client_10G.exe" application will operate on PC for data verification. If data value is not correct, test application will show error message on console.

User can select 2 transfer packet sizes by DIPSW[1] setting, i.e. 1456 data byte for running with not supported Jumbo frame PC, and 8960 data byte for running with supported Jumbo frame PC. User can confirm this setting from LED2 status.

The operation sequence for sending mode is follows.
1) TOE10G-IP within VC707 development board initializes parameters in system such as Packet size, transfer size, MAC and IP address, and then waits open connection from PC.
2) Test application on PC opens connection to connect with VC707 development board, and wait data sending.
3) TOE10G-IP starts to send 32 GB data to PC while PC verifies receiving data that is correct.
4) After all data are transferred, TOE10G-IP sends packet to close connection.
5) PC sends acknowledge to close connection. Then, operation will run as loop from Step2) to Step5) until operation cancelled.

2.2 Receiving mode

In this demo, data will be transferred from PC to VC707 development board. By using "send_tcp_client_10G.exe" operating on PC, data will be sent out until number of transferred data equal to setting value. This test can run as 2 modes, i.e. performance test and data verification.

In performance test, all '0' data will be sent out from PC and verification module within VC707 development board will be OFF for achieving best performance transfer. In data verification mode, 32-bit increment data will be generated from PC and verification module will be ON for data verification. LED error will blink if any error is detected. Verification ON/OFF within hardware is set from DIPSW[3] while test application can be set as option value in command line.

The operation sequence for receiving mode is follows.
1) Similar to Step 1) in Sending mode.
2) Test application on PC opens connection to connect with VC707 development board, and then start transferring all '0' or increment data out until complete.
3) TOE10G-IP receives data and verify data if enable.
4) After all data are transferred, Test application sends packet to close connection.
5) TOE10G-IP sends acknowledge to close connection. This mode will run only 1 time, not in repeat loop like Sending mode.

3 PC Setup

Before running demo, user needs to setup network setting on PC as follows.
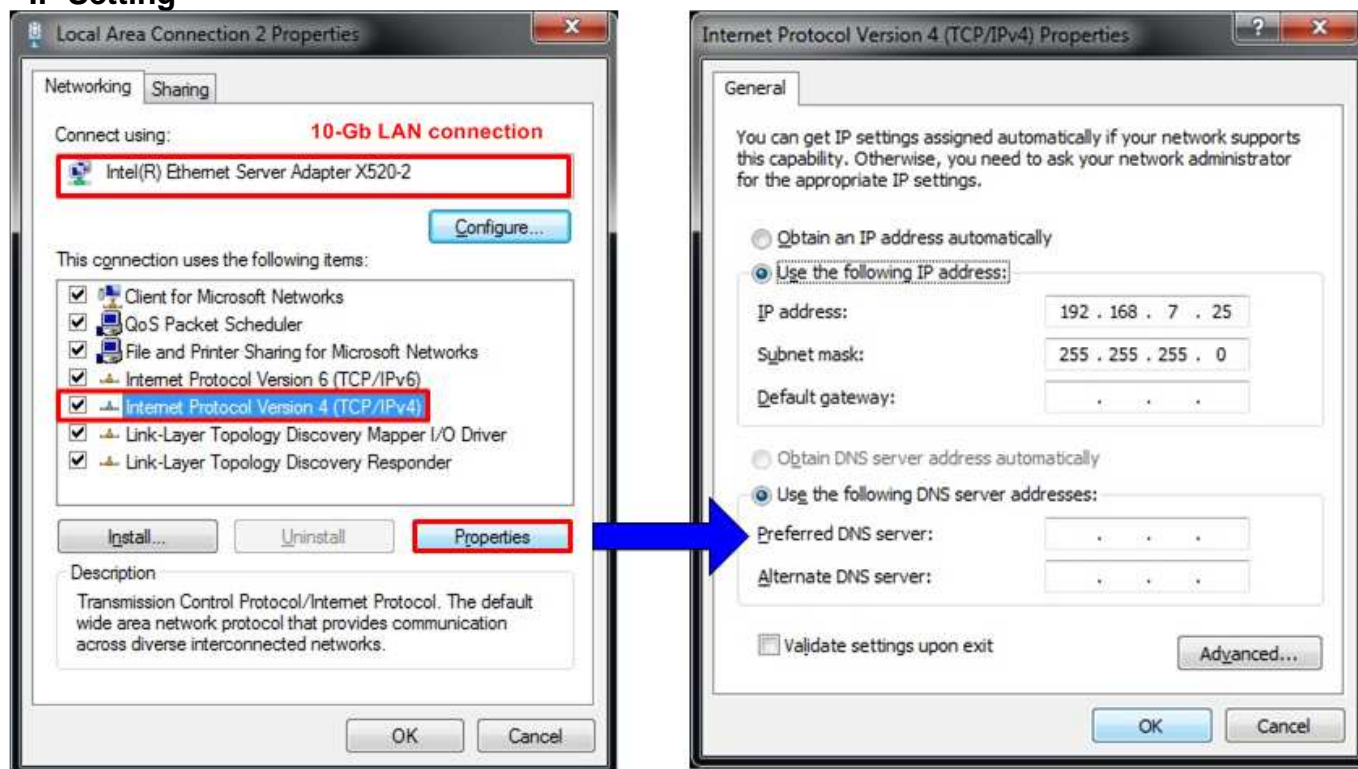
3.1 IP Setting

Figure 2 IPv4 Setting

- Open Local Area Connection Properties of 10-Gb connection, as shown in left window of Figure 2.
- Select "TCP/IPv4" and then click Properties.
- Set IP address = 192.168.7.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 2.
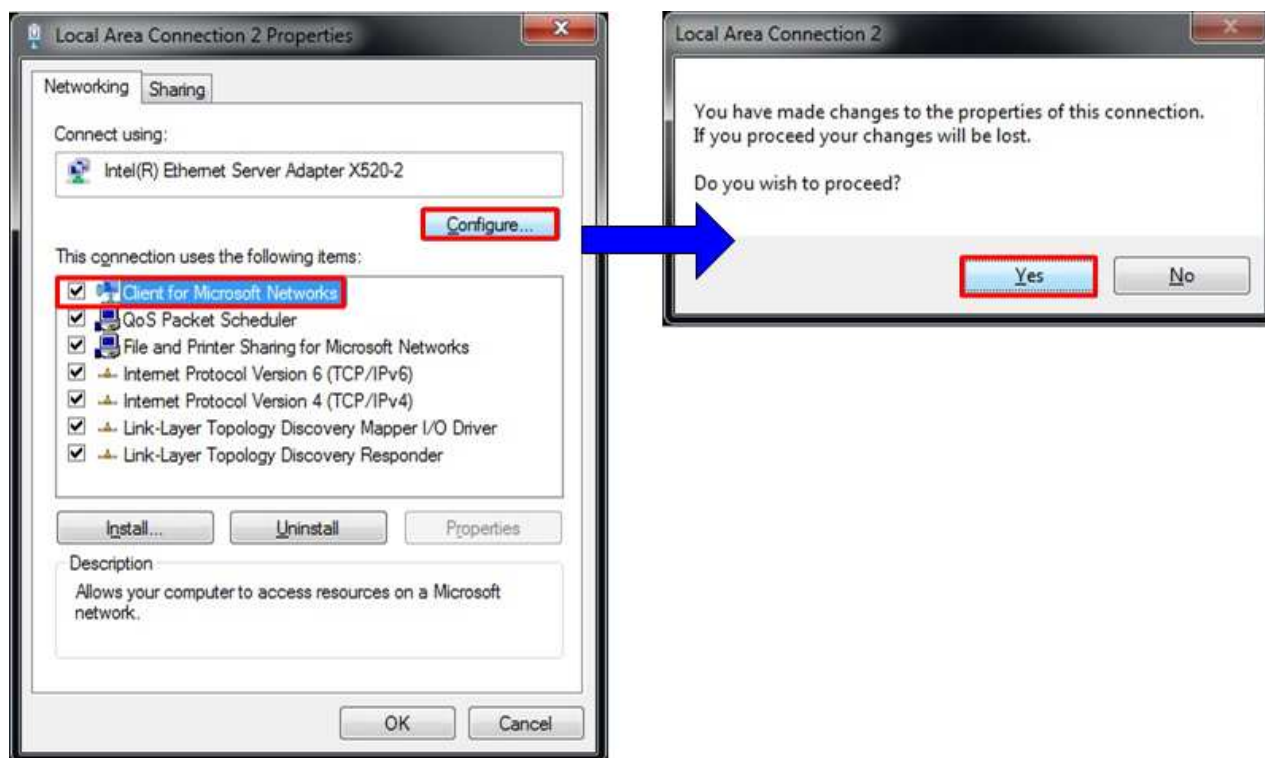
3.2   Speed and Frame Setting

Figure 3 Network Configure

- On Local Area Connection Properties window, select "Client for Microsoft Networks", and then click "Configure", as shown in Figure 3.
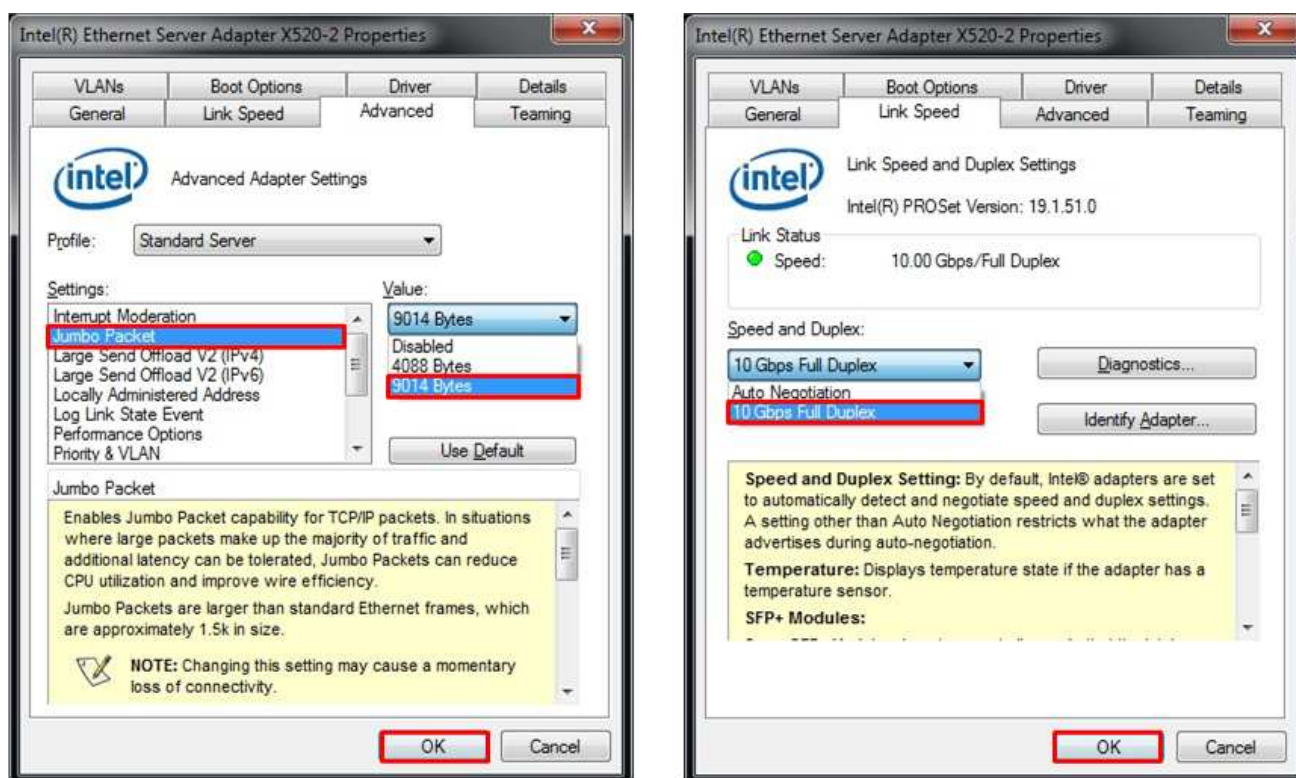
Figure 4 Link speed and Jumbo frame setup

- On Advanced Tab, select "Jumbo Packet" and then set Value to "9014 Bytes" for Jumbo Frame support or set value to "Disabled" for non-Jumbo Frame support, as shown in left window of Figure 4.
- On Link Speed, select "10 Gbps Full Duplex" for running 10-Gigabit transfer test, as shown in right window of Figure 4.
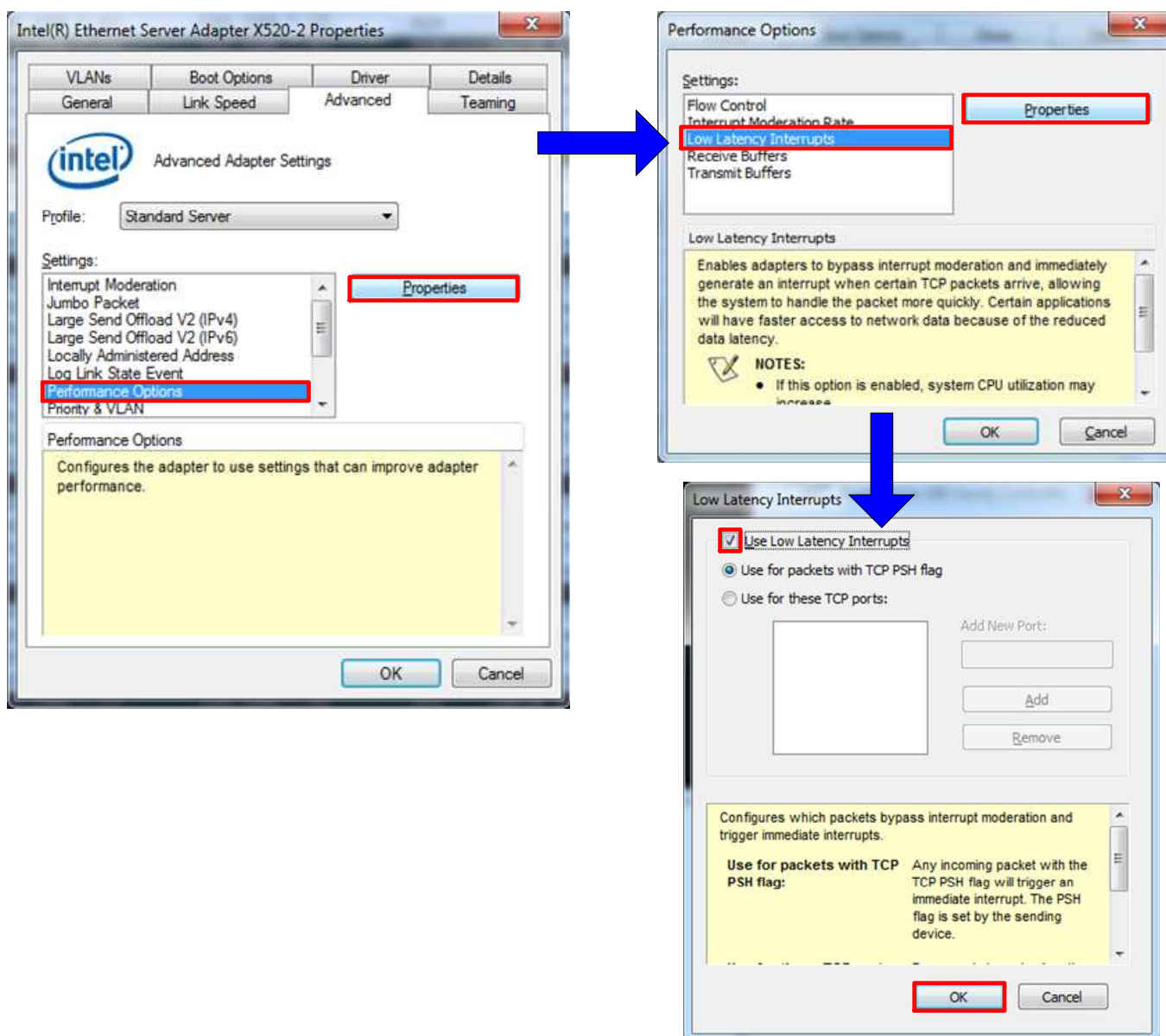
Figure 5 Performance Options

- On Advanced Tab, select "Performance Options" and click "Properties" button.
- On "Performance Options" window, select "Low Latency Interrupts" and click "Properties" button.
- On "Low Latency Interrupts" window, select "Use Low Latency Interrupts" and click "OK" button.
- Click "OK" button to save and exit all setting windows.

4 How to run demo

Both Sending and Receiving demo requires same initial steps to set up hardware as follows.

-    Insert Jumper to pin1-2 at J6 connector to enable SFP+, as shown in Figure 6.

Figure 6 Insert Jumper at J6 connector

-    Connect micro USB cable from VC707 development board to PC, and connect power supply to VC707 board.
-    Insert SFP+ transceiver with optical cable to SFP on KC705.
-    Insert another SFP+ transceiver with optical cable to PC.
-    Set up network setting on PC, following Topic 3.
-    Power on VC707 development board.
-    Open iMPACT and download bit file to VC707 development board, as shown in Figure 7.
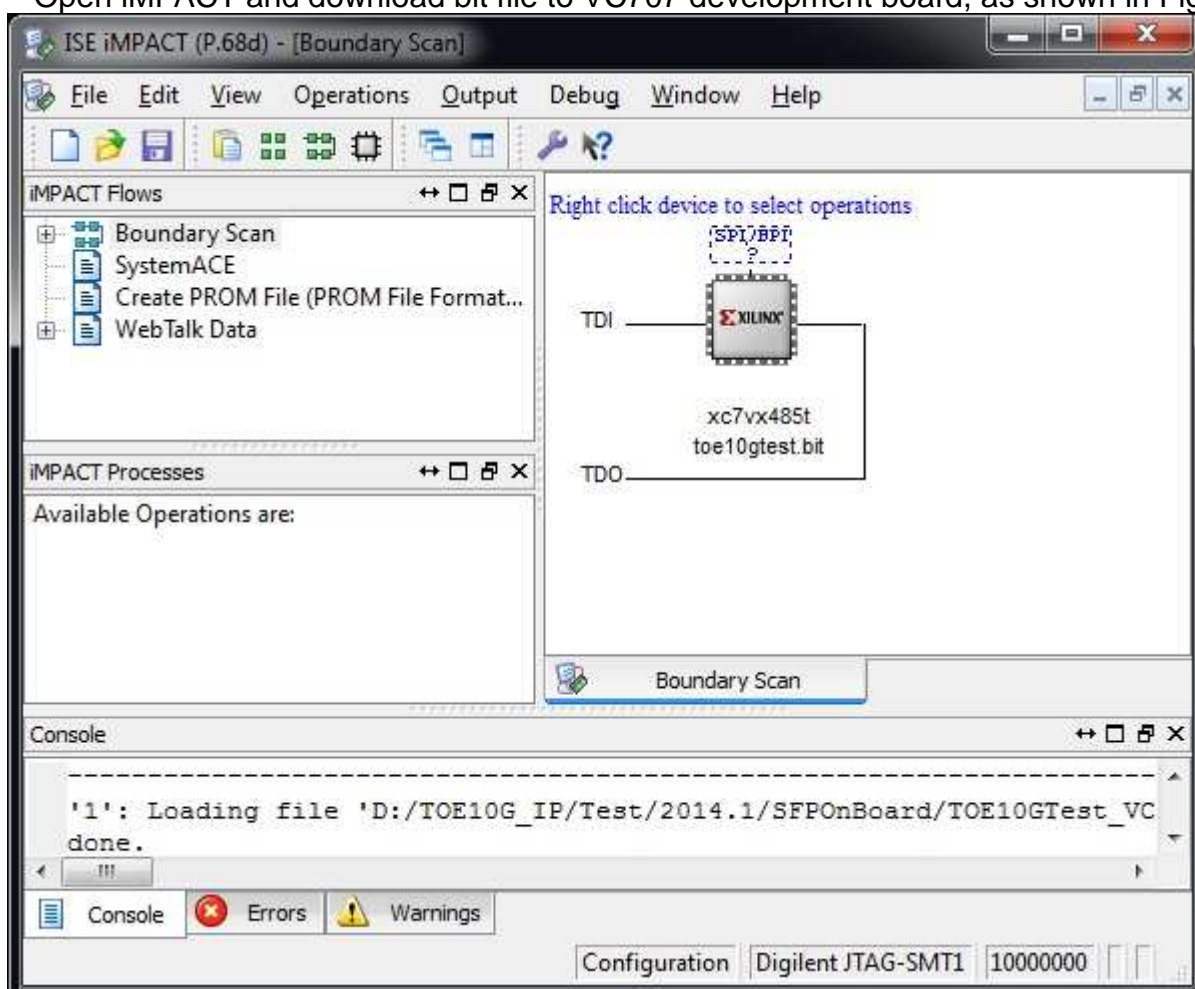
Figure 7 Programmer Environment

- Press StartSW as shown in Figure 1(SW6) to initialize parameter in system, and then LED0 will turn on, as shown in Figure 8 and Figure 9 following DIPSW[1] setting.

Figure 8 LED Status after push StartSW when DIPSW[1]=OFF

Figure 9 LED Status after push StartSW when DIPSW[1]=ON

Now system is ready to transfer data. The step to test Sending and Receiving data is described in next topic.
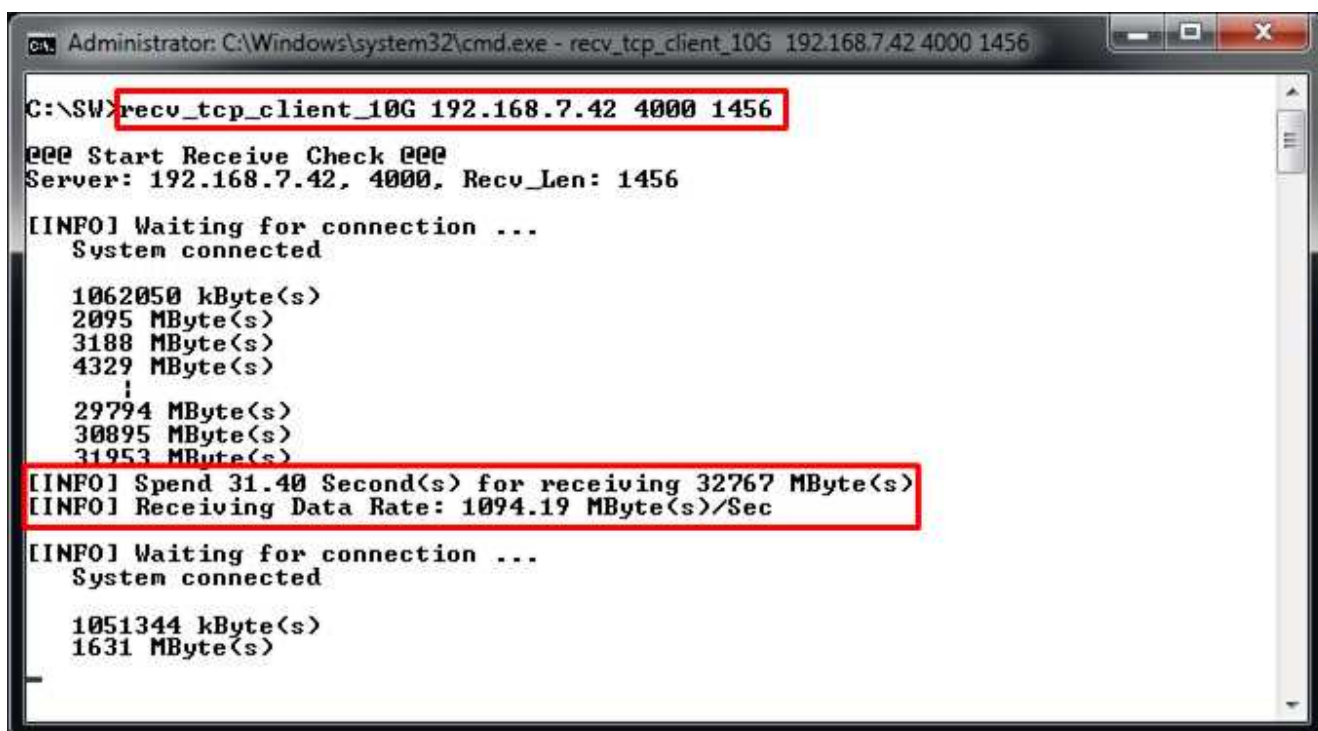
Note:
- Transfer performance on the demo depends on Test PC performance to send and receive data through 10-Gigabit Ethernet

4.1   Run Sending Demo

Sending demo will operate in loop and user needs to cancel the application to stop the test, so the logic will hang to wait TestPC acknowledge.

4.1.1   Non-Jumbo frame mode
- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = OFF and confirm that LED2 status is OFF.
- Open "command prompt" on PC, and run "recv_tcp_client_10G" test application by following command
  >> recv_tcp_client_10G <FPGA IP address> <FPGA port number> <number of data in packet>
  For example,
  >> recv_tcp_client_10G 192.168.7.42 4000 1456
  Note: This demo fixes IP address, port number, and number of data. So, please don't change any value without vhdl code modification.
- Test application displays current packet number during transferring and time usage with performance will be displayed when complete each loop transfer, as shown in Figure 10.
- User can cancel operation by pressing "Ctrl+C".

Figure 10 Non-Jumbo frame Sending Demo

Figure 11 LED Status when running Sending Demo with Non-Jumbo frame

4.1.2 Jumbo frame mode
- Set DIPSW[2] = OFF to run Sending demo.
- Set DIPSW[1] = ON and confirm that LED status is ON.
- Open "command prompt" on PC, and run "recv_tcp_client_10G" test application by following command
  >> recv_tcp_client_10G 192.168.7.42 4000 8960
  Note: This demo fixes IP address, port number, and number of data. So, please don't change any value without vhdl code modification.
- Test application displays current packet number during transferring and time usage with performance will be displayed when complete each loop transfer, as shown in Figure 12.
- User can cancel operation by pressing "Ctrl+C".

Figure 12 Jumbo frame Sending Demo

Figure 13 LED Status when running Sending Demo with Jumbo frame

4.2 Run Receiving Demo

4.2.1 Performance test mode
- Set DIPSW[2] = ON to run Receiving demo.
- Set DIPSW[3] = OFF.
- Open "command prompt" on PC, and run "send_tcp_client_10G" test application by following command

  >> send_tcp_client_10G <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>
   - Similar to Sending demo, IP address and port number cannot change without hdl code modification.
   - User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 2097152 means 32 GBytes data is transferred. Valid range of transfer size is 1 – 2097152.
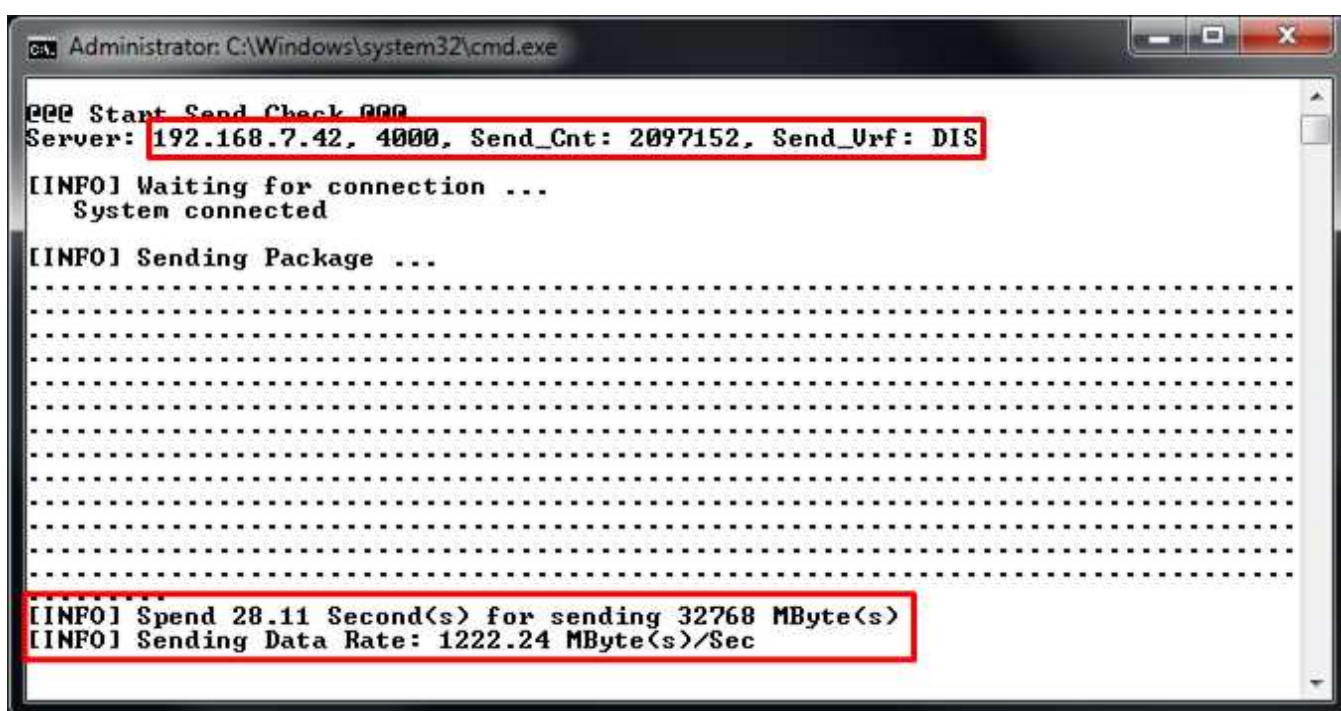   - Mode: '0'- All '0' pattern are sent for performance test.

  For example,
  >> send_tcp_client_10G 192.168.7.42 4000 2097152 0

- Test application displays "…" during transferring packet and time usage with performance will be displayed when complete data transfer, as shown in Figure 15.

Figure 14 Command line for receiving demo on Performance test mode

Figure 15 Receiving Demo on Performance test mode

4.2.2   Verification mode
  - Set DIPSW[2] = ON to run Receiving demo.
  - Set DIPSW[3] = ON to enable verification module.
  - Open "command prompt" on PC, and run "send_tcp_client_10G" test application by following command
    >> send_tcp_client_10G <FPGA IP address> <FPGA port number> <transfer size in 16kbyte unit> <mode>
      o Similar to Sending demo, IP address and port number cannot change without vhdl code modification.
      o User can set transfer size in 16kByte unit which is buffer size in test application. In this example, 100000 means 32 Gbytes data is transferred. Valid range of transfer size is 1 – 2097152.
      o Mode: '1'- 32-bit increment data are sent for data verification.

    For example,
    >> send_tcp_client_10G 192.168.7.42 4000 2097152 1
  - Test application displays "…" during transferring packet and time usage with performance will be displayed when complete data transfer, as shown in Figure 17.

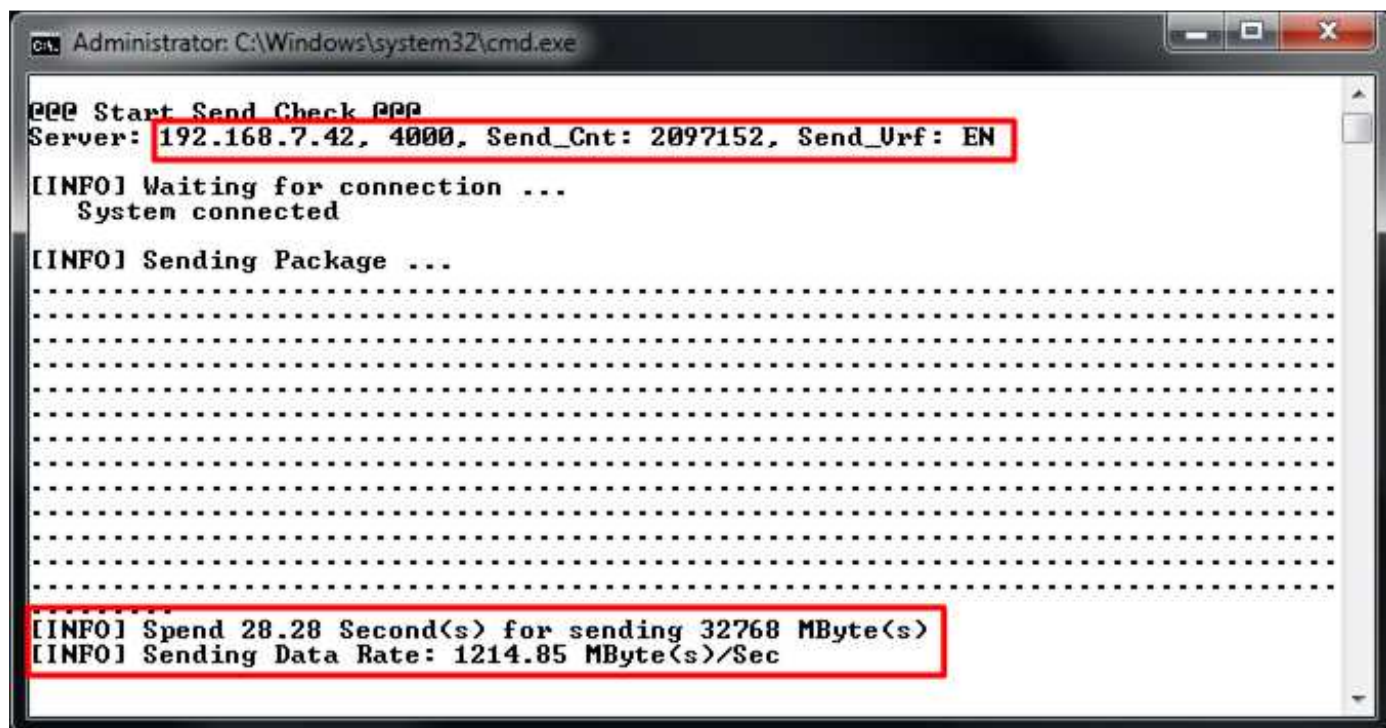Figure 16 Command line for receiving demo on Verification mode

Figure 17 Receiving Demo on Verification mode

  - LED3 will blink if any error data detects from Verification module.

5 Revision History

Revision	Date	Description
1.0	13-Jun-14	Initial version release