

### Features

- Operating voltage: 3.3V
- Low power consumption at 56mW
- Power-down mode: Under 1 $\mu$ A (clock timing keep low)
- 16-bit 6 MSPS A/D converter
- Guaranteed no missing codes
- Supports CDS/SHA mode
- 1~6 programmable gain
- $\pm 200$ mV programmable offset
- Input clamp circuitry
- Internal voltage reference
- Multiplexed byte-wide output (8+8 format)
- Programmable 3-wire serial interface
- 3.3V digital I/O compatibility
- 28-pin SSOP (209mil) package

### Applications

Low power flatbed document scanners

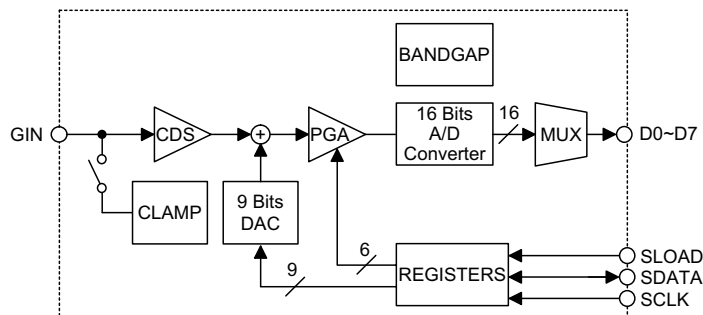
### General Description

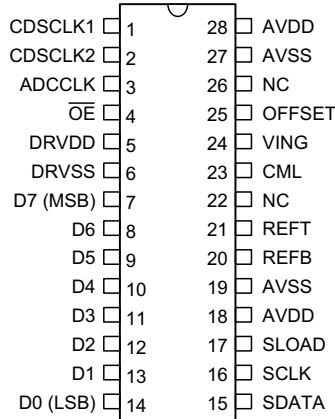
The HT82V36 is a complete analog signal processor for CCD imaging applications. It features a 1-channel architecture designed to sample and condition the outputs of linear CCD arrays. It consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), and a low power 16-bit A/D converter.

The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 16-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface, which provides gain, offset and operating mode adjustments.

### Block Diagram



**Pin Assignment**


**HT82V36  
- 28 SSOP-A**

**Pin Description**

Pin No.	Pin Name	I/O	Description
1	CDSCLK1	DI	CDS reference clock pulse input
2	CDSCLK2	DI	CDS data clock pulse input
3	ADCCLK	DI	A/D sample clock input
4	OE	DI	Output enable, active low
5	DRVDD	P	Digital driver power
6	DRVSS	P	Digital driver ground
7~14	D7~D0	DO	Digital data output
15	SDATA	DI/DO	Serial data input/output
16	SCLK	DI	Clock input for serial interface
17	SLOAD	DI	Serial interface load pulse
18, 27	AVSS	P	Analog ground
19, 28	AVDD	P	Analog supply
20	REFB	AO	Reference decoupling
21	REFT	AO	Reference decoupling
23	CML	AO	Internal reference output
24	VING	AI	Analog input
25	OFFSET	AO	Clamp bias level decoupling
22, 26	NC	—	No connection

**Absolute Maximum Ratings**

Supply Voltage ..... $V_{SS}-0.3V$  to  $V_{SS}+3.6V$       Storage Temperature ..... $-50^{\circ}C$  to  $125^{\circ}C$   
 Input Voltage ..... $V_{SS}-0.3V$  to  $V_{DD}+0.3V$       Operating Temperature ..... $-25^{\circ}C$  to  $75^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
<b>Logic Inputs</b>							
V <sub>IH</sub>	High Level Input Voltage	—	—	0.8×V <sub>DD</sub>	—	—	V
V <sub>IL</sub>	Low Level Input Voltage	—	—	—	—	0.2×V <sub>DD</sub>	V
I <sub>IH</sub>	High Level Input Current	—	—	—	10	—	μA
I <sub>IL</sub>	Low Level Input Current	—	—	—	10	—	μA
C <sub>IN</sub>	Input Capacitance	—	—	—	10	—	pF
<b>Logic Outputs</b>							
V <sub>OH</sub>	High Level Output Voltage	—	—	V <sub>DD</sub> -0.5	—	—	V
V <sub>OL</sub>	Low Level Output Voltage	—	—	—	—	0.5	V
I <sub>OH</sub>	High Level Output Current	—	—	—	1	—	mA
I <sub>OL</sub>	Low Level Output Current	—	—	—	1	—	mA

**A.C. Characteristics**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
<b>Maximum Conversion Rate</b>							
t <sub>MAX</sub>	CDS/SHA Mode	—	—	6	—	—	MHz
<b>Accuracy (Entire Signal Path)</b>							
	ADC Resolution	—	—	—	16	—	
	Integral Nonlinear (INL)	—	—	—	±16	—	LSB
	Differential Nonlinear (DNL)	—	—	-1	—	2	LSB
	Offset Error	—	—	-100	TBD	100	mV
	Gain Error	—	—	—	TBD	—	%FSR
<b>Analog Inputs</b>							
R <sub>FS</sub>	Full-scale Input Range	—	—	1.3	1.4	1.6	Vp-p
V <sub>i</sub>	Input Limits	—	—	AVDD-0.3	—	AVDD+0.3	V
C <sub>i</sub>	Input Capacitance	—	—	—	TBD	—	pF
I <sub>i</sub>	Input Current	—	—	—	TBD	—	μA
<b>Amplifiers</b>							
	PGA Gain at Minimum	—	—	—	1	—	V/V
	PGA Gain at Maximum	—	—	—	5.85	—	V/V
	PGA Gain Resolution	—	—	—	6	—	Bits
	Programmable Offset at Minimum	—	—	—	-200	—	mV
	Programmable Offset at Maximum	—	—	—	200	—	mV
	Offset Resolution	—	—	—	9	—	Bits
<b>Temperature Range</b>							
t <sub>A</sub>	Operating	—	—	0	—	70	°C
<b>Power Supplies</b>							
V <sub>ADD</sub>	AVDD	—	—	3	3.3	3.6	V
V <sub>DRDD</sub>	DRVDD	—	—	3	3.3	3.6	V
<b>Power Consumption</b>							
P <sub>tot</sub>	Total Power Consumption	—	—	—	56	—	mW

**Timing Specification**

Symbol	Parameter	Min.	Typ.	Max.	Unit
<b>Clock Parameters</b>					
$t_{ADCLK}$	Pixel Rate Clock	166	—	—	ns
$t_{ADH}$	ADCCLK Pulse High Width	80	—	—	ns
$t_{ADL}$	ADCCLK Pulse Low Width	80	—	—	ns
$t_{C1}$	CDSCLK1 Pulse Width	20	—	—	ns
$t_{C2}$	CDS Mode CDSCLK2 Pulse Width	20	—	—	ns
$t_{C3}$	SHA Mode CDSCLK2 Pulse Width	40	—	—	ns
$t_{C2ADF}$	CDSCLK2 Falling to ADCCLK Falling	60	—	—	ns
$t_{ADFC1}$	ADCCLK Falling to CDSCLK1 Rising	2	—	—	ns
$t_{ADFC2}$	ADCCLK Falling to CDSCLK2 Rising	2	—	—	ns
$t_{AD}$	Analog Sampling Delay	5	—	—	ns
<b>Serial Interface</b>					
$f_{SCLK}$	Maximum SCLK Frequency	10	—	—	MHz
$t_{LS}$	SLOAD to SCLK Setup Time	10	—	—	ns
$t_{LH}$	SCLK to SLOAD Hold Time	10	—	—	ns
$t_{DS}$	SDATA to SCLK Rising Setup Time	10	—	—	ns
$t_{DH}$	SCLK Rising to SDATA Hold Time	10	—	—	ns
$t_{RDV}$	Falling to SDATA Valid	10	—	—	ns
<b>Data Output</b>					
$t_{OD}$	Output Delay	—	8	—	ns
	Latency (Pipeline Delay)	—	9	—	Cycles

**Functional Description**
**Integral Nonlinear (INL)**

Integral nonlinear error refers to the deviation of each individual code from a line drawn from zero scale through positive full scale. The point used as zero scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

**Differential Nonlinear (DNL)**

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

**Offset Error**

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage.

The offset error is the deviation of the actual first code transition level from the ideal level.

**Gain Error**

The last code transition should occur for an analog value 1/2 LSB below the nominal full-scale voltage.

Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

**Aperture Delay**

The aperture delay is the time delay that occurs when a sampling edge is applied to the HT82V36 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the aperture delay is measured from each clock's falling edge to the instant the actual internal sample is taken.

**Internal Register Descriptions**

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	0	1	1	CDS on	Clamp Voltage	Enable Power Down	Output Delay	1byte out
Reserved	0	0	1									
Reserved	0	1	0									
PGA	0	1	1	X	0	0	MSB					LSB
Reserved	1	0	0									
Reserved	1	0	1									
Offset	1	1	0	MSB								LSB
Reserved	1	1	1									

**Internal Register Map**

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Set to 1	Set to 1	CDS operation	Clamp bias	Power-down	Output delay	1 byte out (High-byte only)
				1=CDS mode*	1=2.5V*	1=On	1=On	1=On
				0=SHA mode	0=2V	0=Off (Normal)*	0=Off*	0=Off*

**Configuration Register Settings**

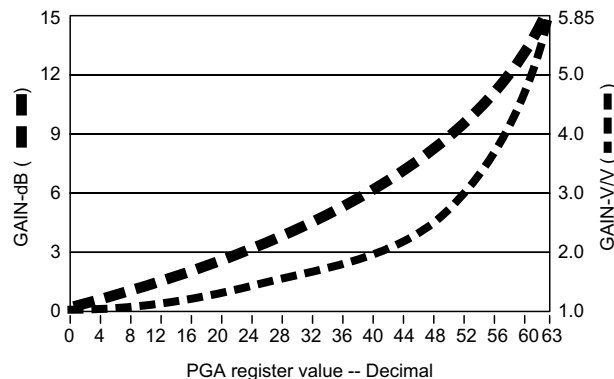
Note: \* Power-on default value

**PGA Gain Register**

Bits D7 and D6 in the register must be set low, and bits D5 through D0 control the gain range in 64 increments. See figure for a graph of the PGA gain versus PGA register code. The coding for the PGA register is straight binary, with an all zero words corresponding to the minimum gain setting (1x) and an all one word corresponding to the maximum gain setting (5.85x).

The PGA has a gain range from 1x (0dB) to 5.85x (15.3dB), adjustable in 64 steps. The Figure shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear in dB, the gain in V/V varies in non-linear proportion with the register code, according to the following the equation:  $Gain = \frac{5.85}{1 + 4.85 \times (\frac{63 - G}{63})}$

Where G is the decimal value of the gain register contents, and varies from 0 to 63.


**PGA Gain Transfer Function**

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (dB)
Set to 0	Set to 0	Set to 0	MSB					LSB		
0	0	0	0	0	0	0	0	0*	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
					.				.	.
					.				.	.
0	0	0	1	1	1	1	1	0	5.43	14.7
0	0	0	1	1	1	1	1	1	5.85	15.3

**PGA Gain Register Settings**

Note: \* Power-on default value

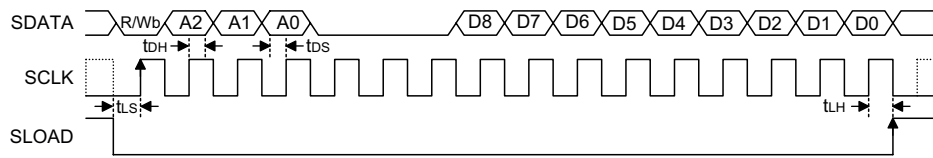
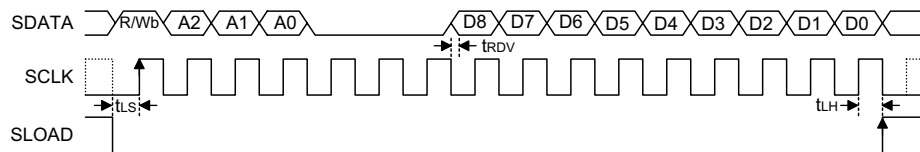
**Offset Register**

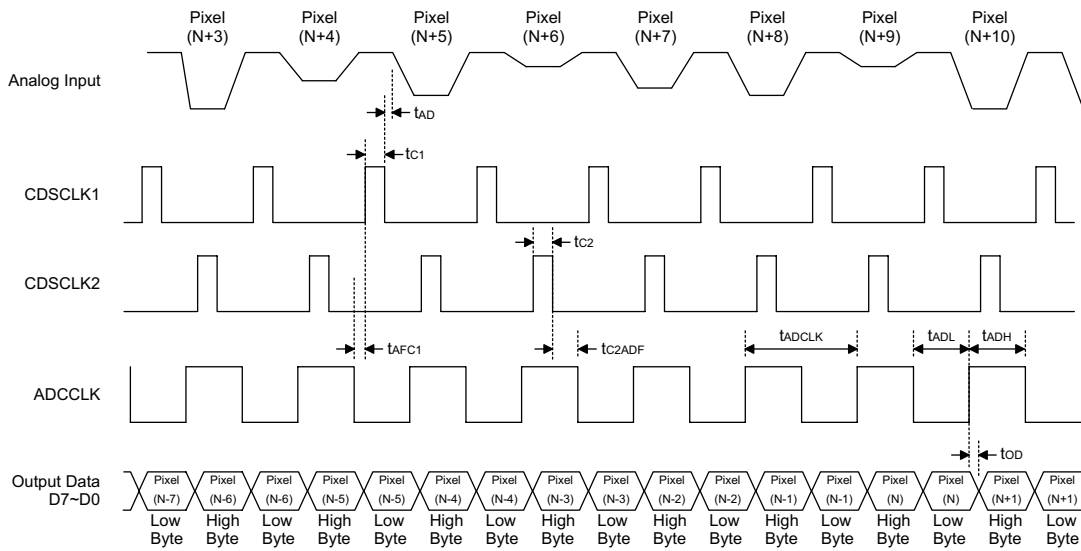
Bits D8 through D0 control the offset range from -200mV to 200mV in 512 increments.

The coding for the offset registers is sign magnitude, with D8 as the sign bit. The Table shows the offset range as a function of the bits D8 through D0.

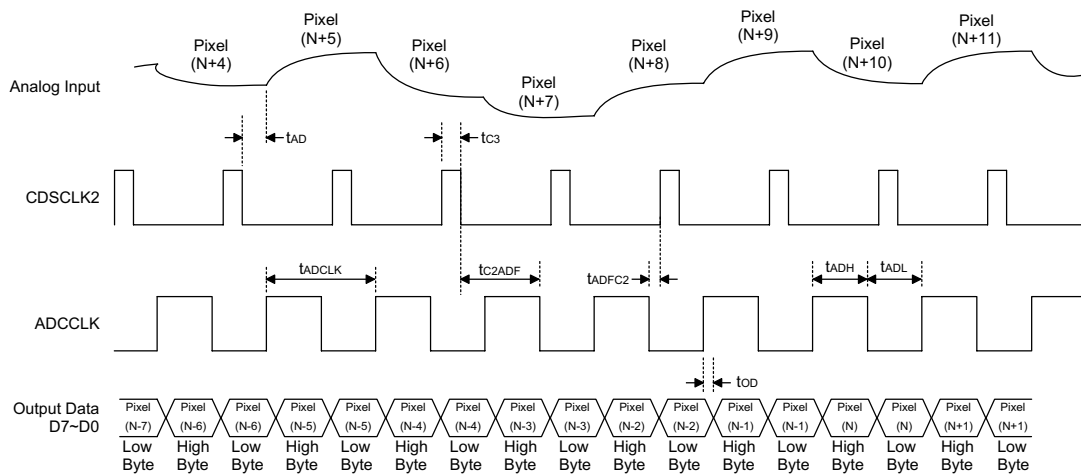
D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0*	0
0	0	0	0	0	0	0	0	1	0.78
					.				.
					.				.
0	1	1	1	1	1	1	1	1	200
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	-0.78
					.				.
					.				.
1	1	1	1	1	1	1	1	1	-200

Note: \* Power-on default value

**Timing Diagrams**

**Serial Write Operation Timing**

**Serial Read Operation Timing**



1-Channel CDS Mode Timing



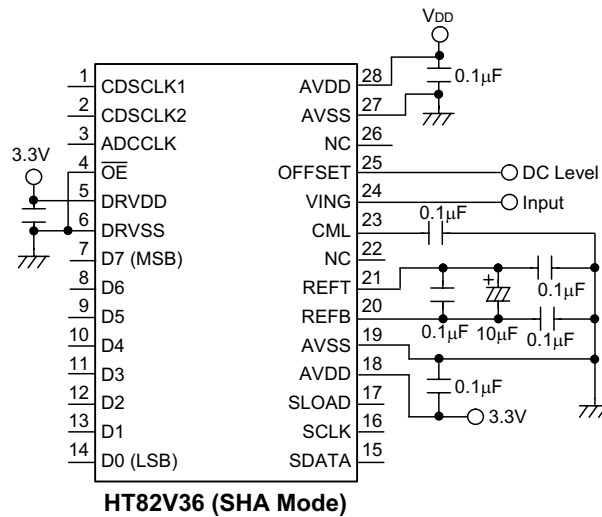
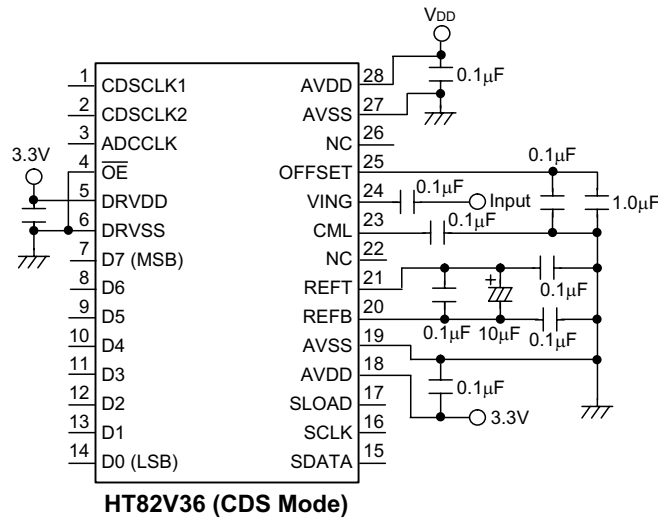
1-Channel SHA Mode Timing

### Application Circuits

The recommended circuit configuration for 1-channel CDS mode operation is shown below.

The recommended input coupling capacitor value is 0.1 $\mu$ F (see circuit operation section for more details).

A single ground plane is recommended for the HT82V36. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the HT82V36. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. All 0.1 $\mu$ F decoupling capacitors should be located as close as possible to the HT82V36 pins.

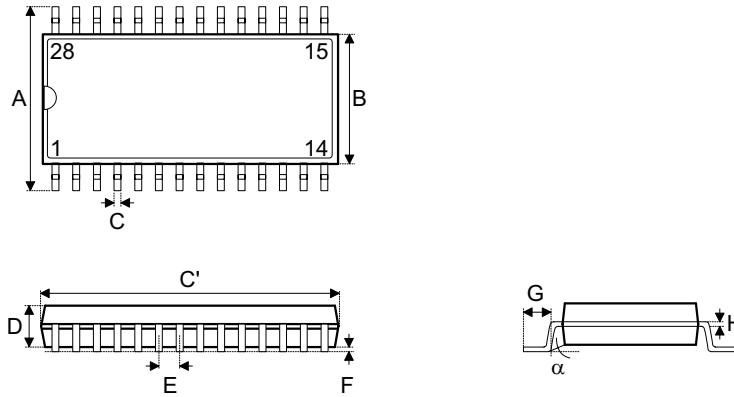


**Note:** For the SHA Mode, all of the above considerations also apply, except that the analog input signal is directly connected to the HT82V36 without using a coupling capacitor. The OFFSET pin should be grounded if the input to the HT82V36 is to be referenced to ground, or a dc offset voltage should be applied to the OFFSET pin in situation where a coarse offset needs to be removed from the input.



**Package Information**

**28-pin SSOP (209mil) Outline Dimensions**



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	291	—	323
B	196	—	220
C	9	—	15
C'	396	—	407
D	65	—	73
E	—	25.59	—
F	4	—	10
G	26	—	34
H	4	—	8
$\alpha$	0°	—	8°

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