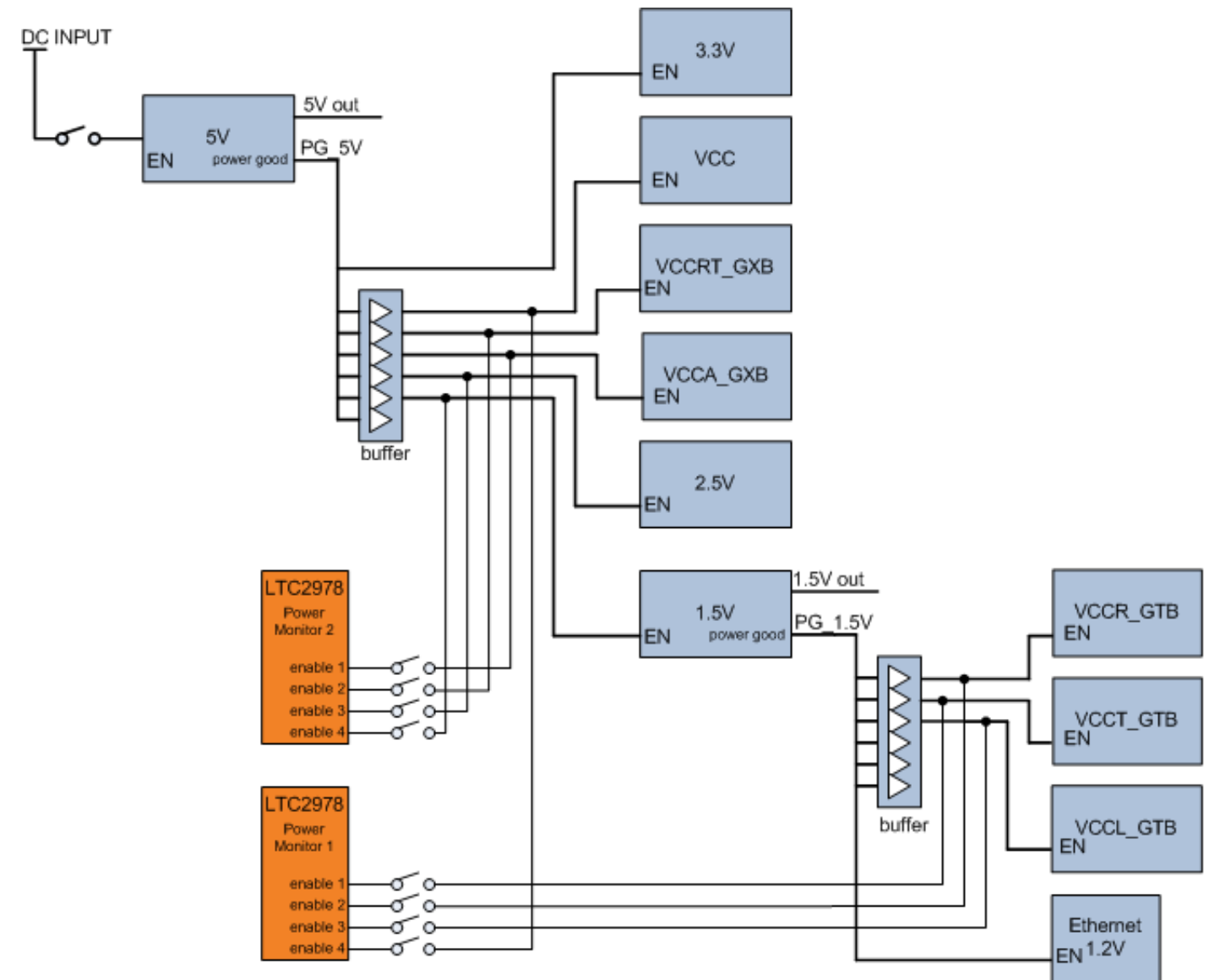
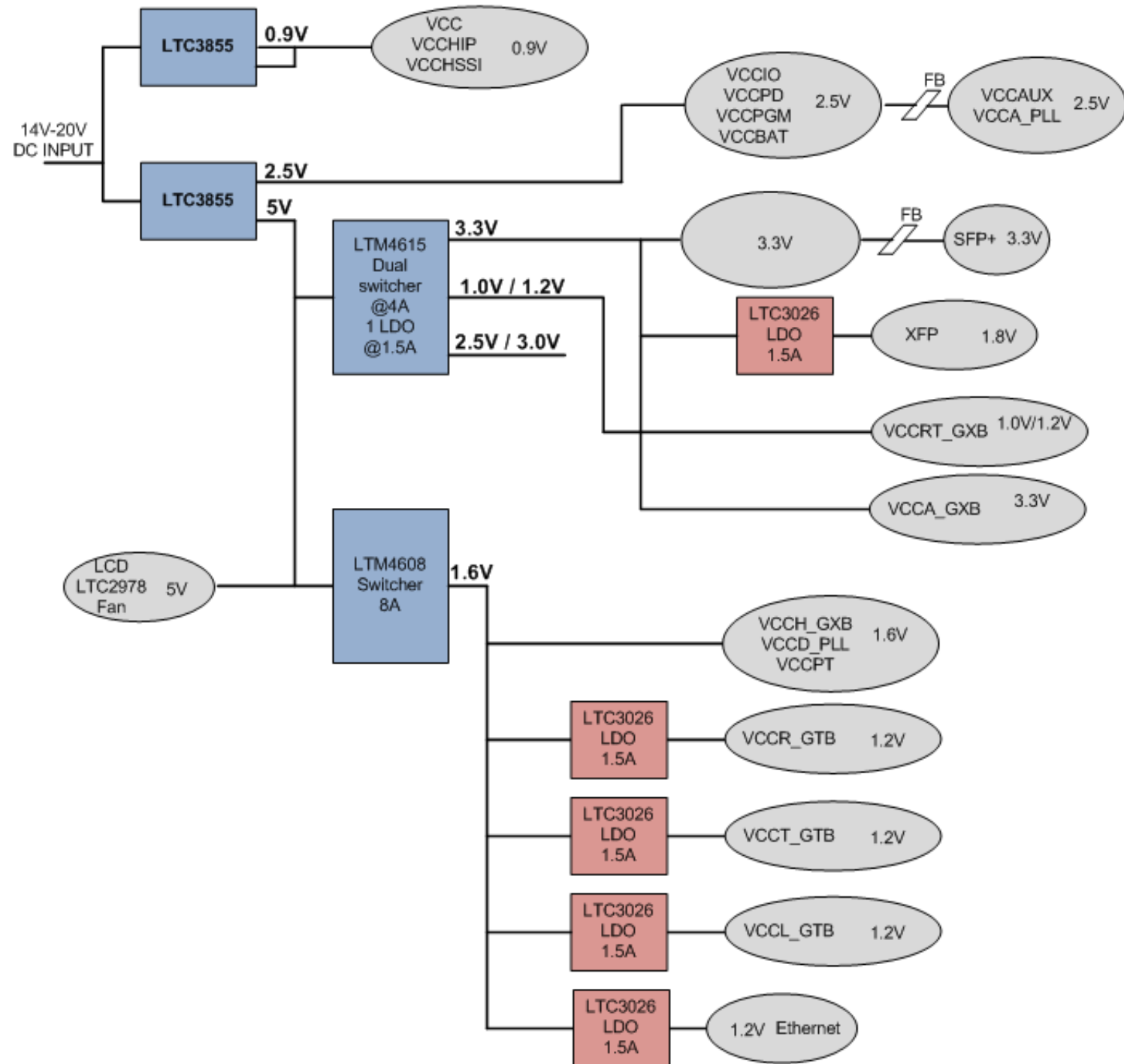


PAGE	DESCRIPTION
1	block diagram, revision history
2	power tree
3	power - DC-Input / 2.5V / 5V
4	power - S5GT_VCC
5	power - 3.3V / VCCA / VCCRT
6	power - 1.6V / Ethernet / XFP
7	power - XCVR - GTB
8	power - S5GT decoupling
9	power monitor - VCC / GTB
10	power monitor - GXB
11	temperature sense
12	USB blaster
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14	flash
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16	switches / LEDs / LCD
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20	XFP interface
21	SMA's / SFP+ interface
22	clocks - core
23	clocks - ss / 50MHz
24	clocks - XCVR left blocks
25	clocks - XCVR right blocks
26	S5 configuration / JTAG
27	S5 bank 3
28	S5 bank 4
29	S5 bank 7
30	S5 bank 8
31	S5GX - block left 0-1
32	S5GX - block left 2-3
33	S5GT - block right 0-1
34	S5GT - block right 2-3
35	S5GT FPGA / XCVR power
36	S5GT - GND



Power Tree / Power Sequence

Power Tree – ES Devices



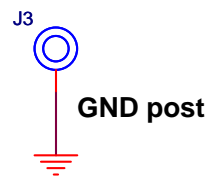
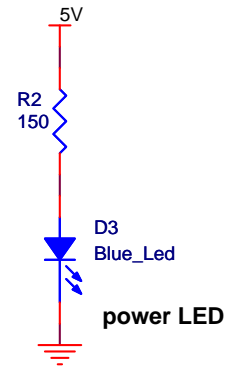
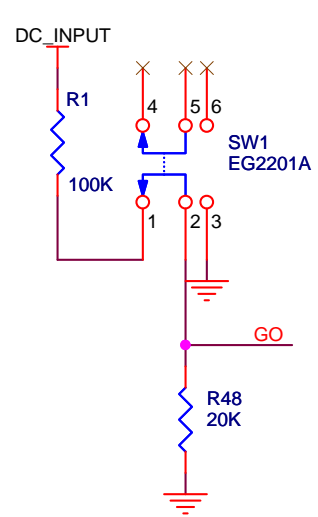
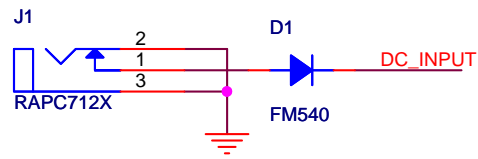
Power Sequence



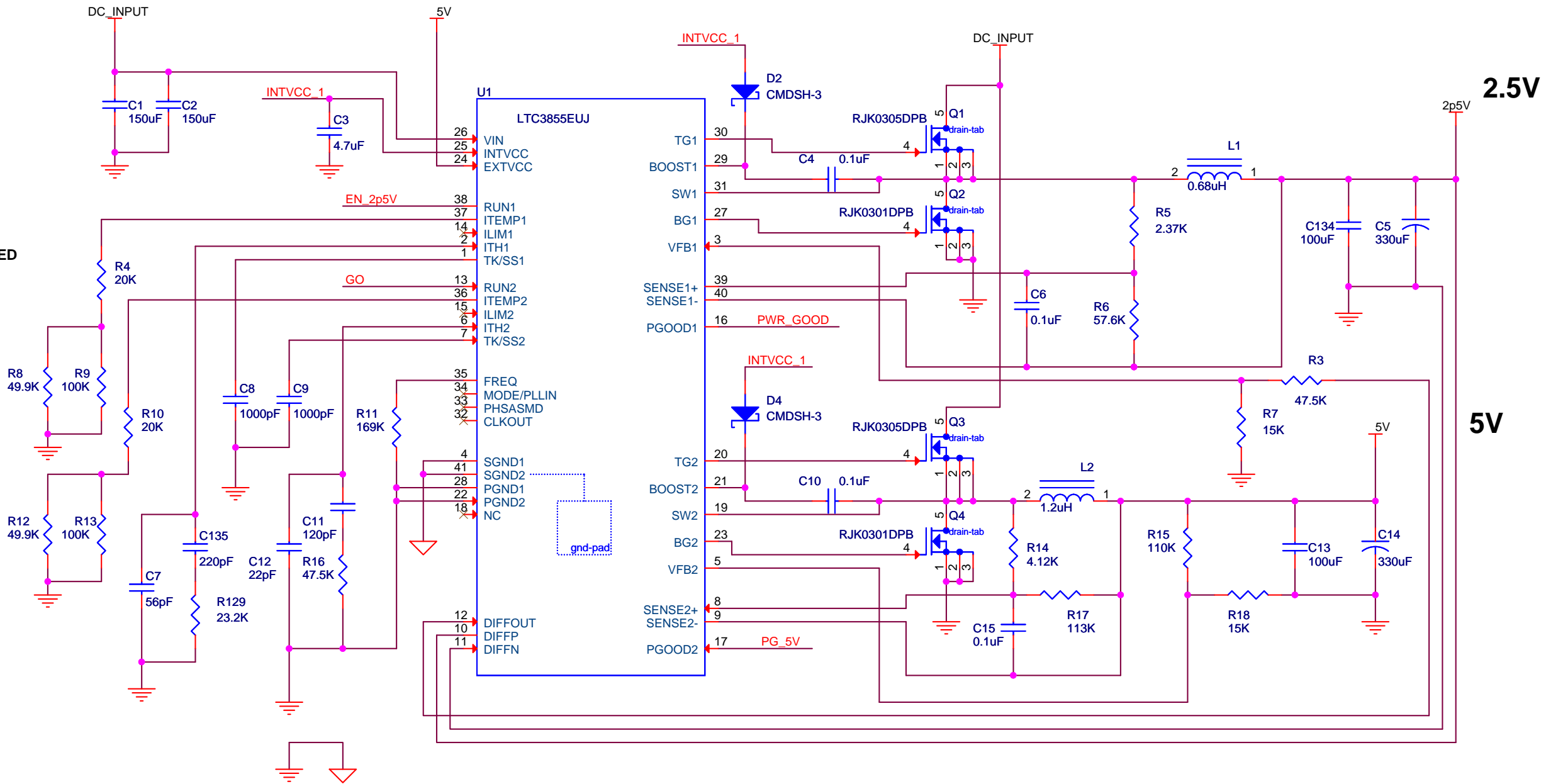
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PWR - DC-Input - 2.5V / 5V

14V-20V DC INPUT



- STD0F1 Standoff Hole
- STD0F2 Standoff Hole
- STD0F3 Standoff Hole
- STD0F4 Standoff Hole
- STD0F5 Standoff Hole
- STD0F6 Standoff Hole

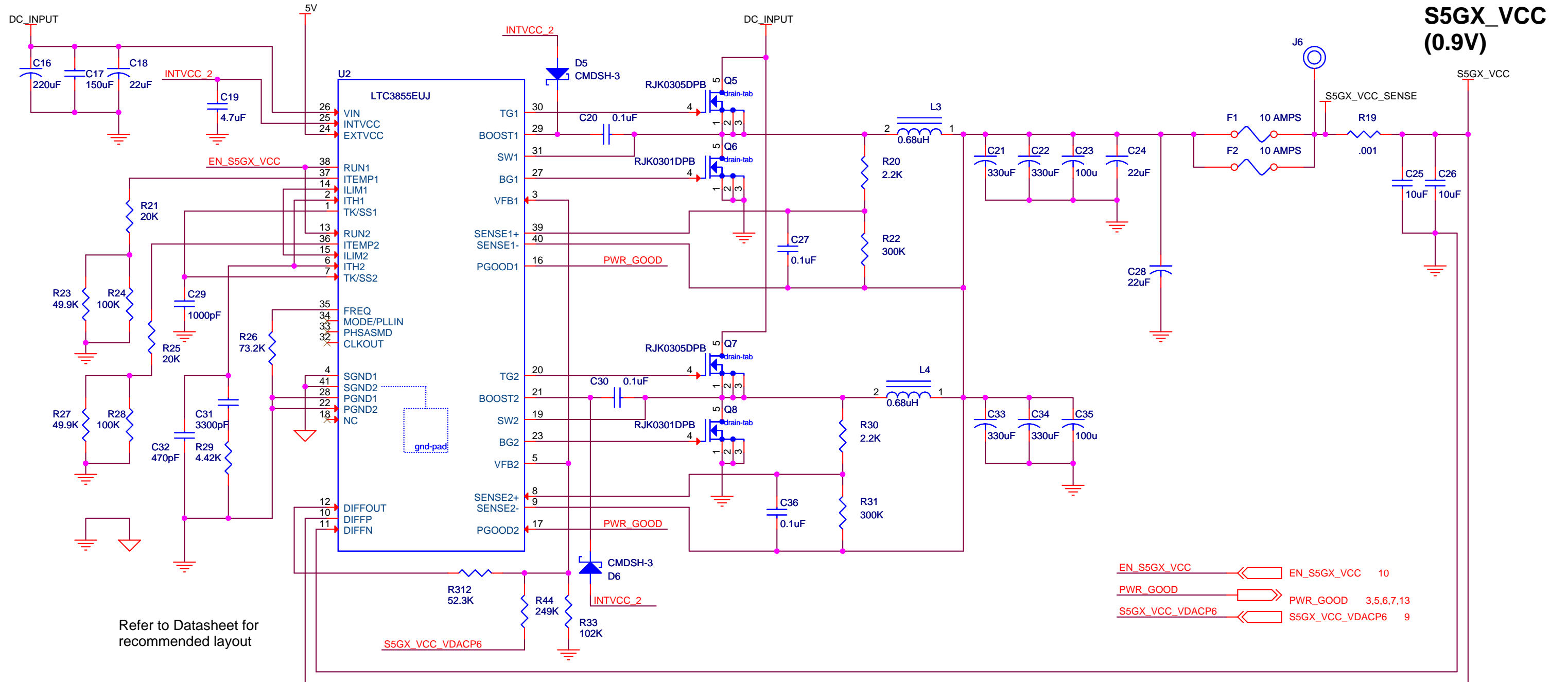


EN_2p5V <--> EN_2p5V 10
 PWR_GOOD <--> PWR_GOOD 4,5,6,7,13
 PG_5V <--> PG_5V 5,10



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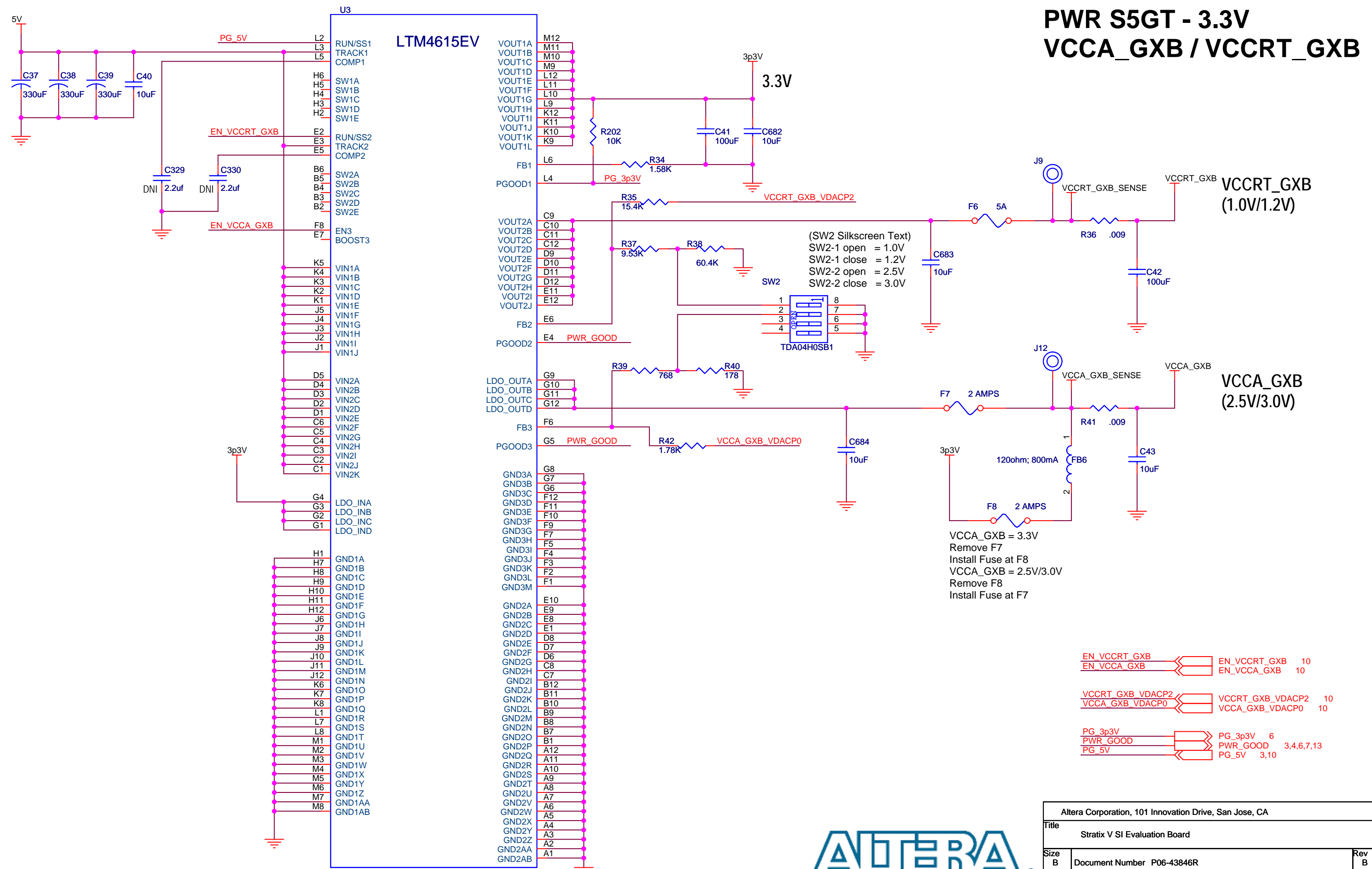
PWR S5GX - VCC



- EN_S5GX_VCC <<< EN_S5GX_VCC 10
- PWR_GOOD >>> PWR_GOOD 3,5,6,7,13
- S5GX_VCC_VDACP6 <<< S5GX_VCC_VDACP6 9



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PWR S5GT - 3.3V VCCA_GXB / VCCRT_GXB

(SW2 Silkscreen Text)
 SW2-1 open = 1.0V
 SW2-1 close = 1.2V
 SW2-2 open = 2.5V
 SW2-2 close = 3.0V

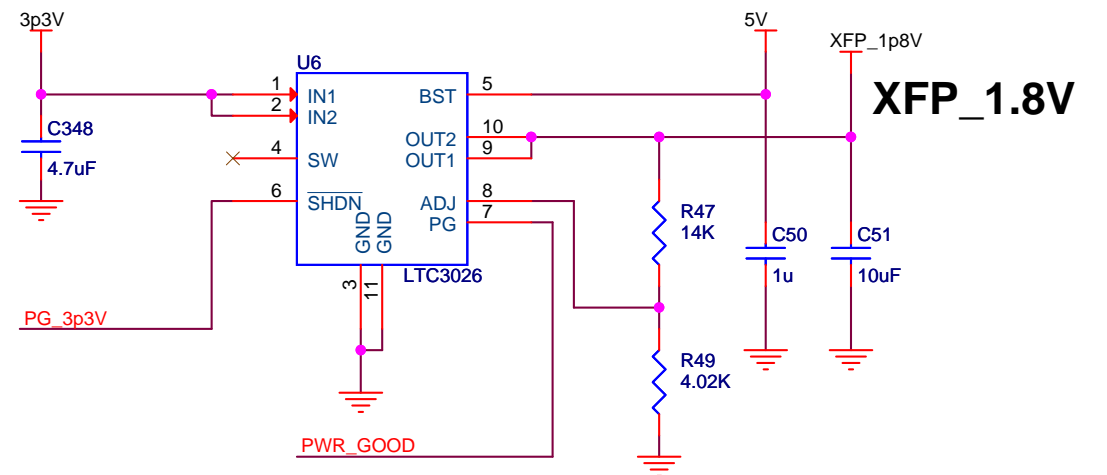
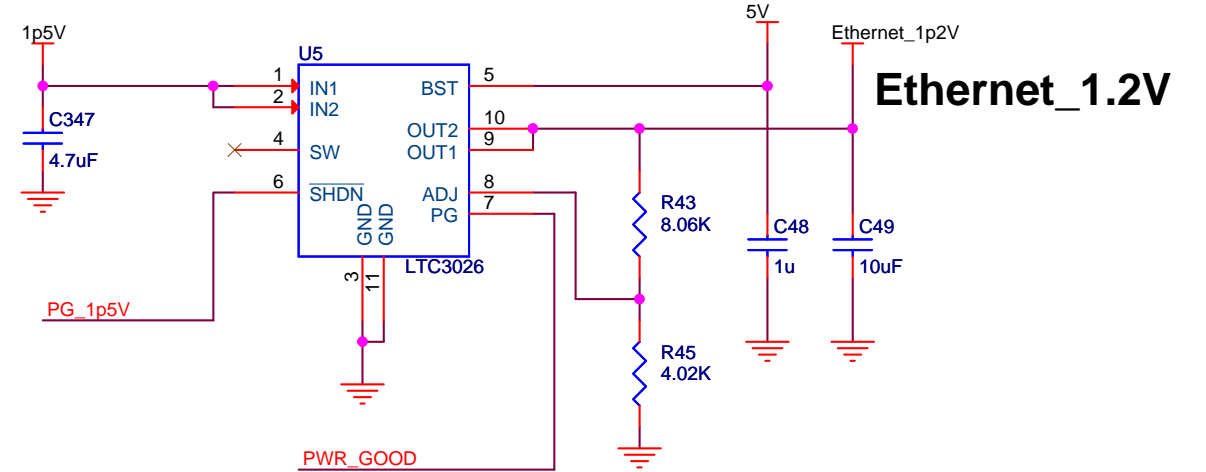
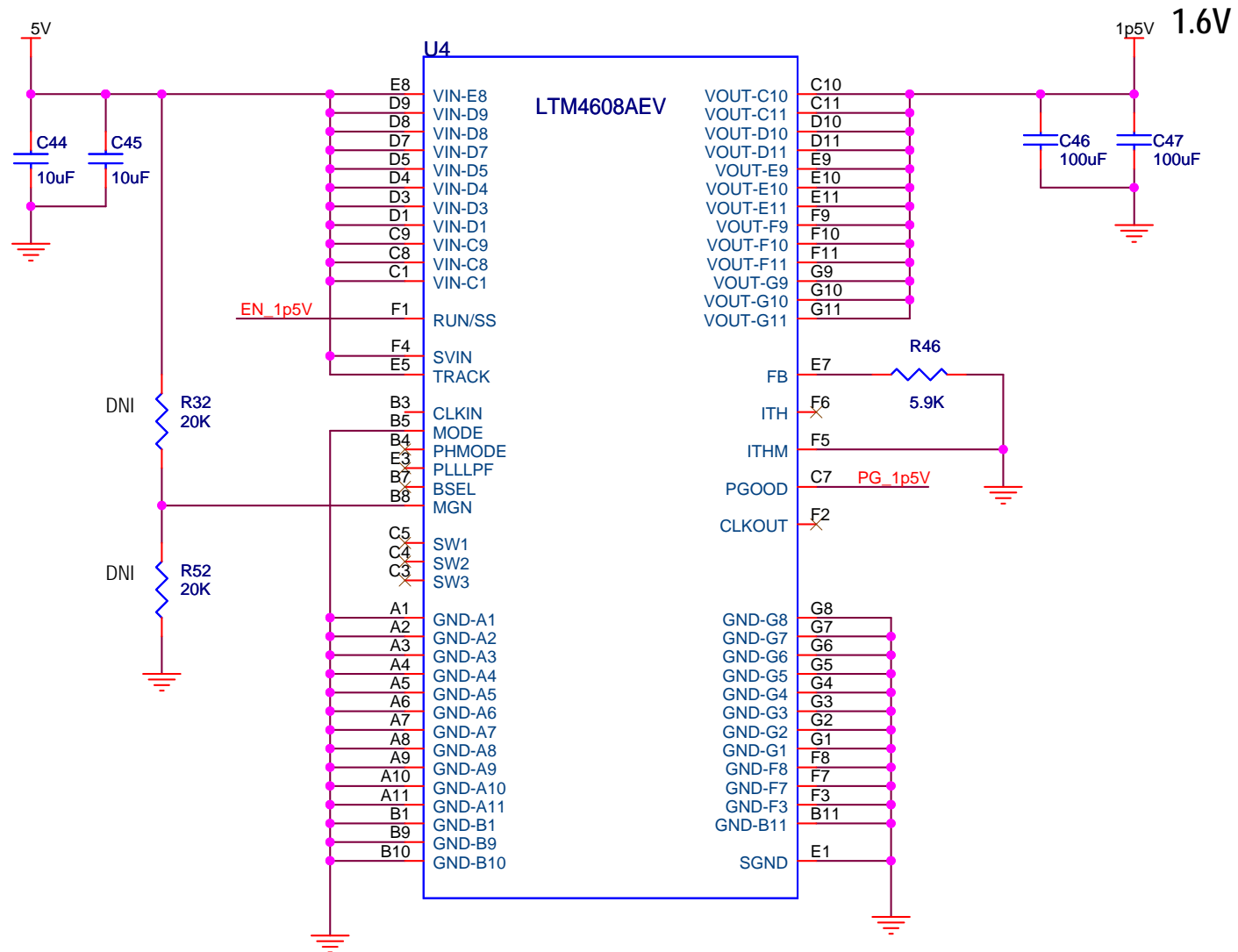
VCCA_GXB = 3.3V
 Remove F7
 Install Fuse at F8
 VCCA_GXB = 2.5V/3.0V
 Remove F8
 Install Fuse at F7

EN_VCCRT_GXB	EN_VCCRT_GXB	10
EN_VCCA_GXB	EN_VCCA_GXB	10
VCCRT_GXB_VDACP2	VCCRT_GXB_VDACP2	10
VCCA_GXB_VDACP0	VCCA_GXB_VDACP0	10
PG_3p3V	PG_3p3V	6
PWR_GOOD	PWR_GOOD	3,4,6,7,13
PG_5V	PG_5V	3,10

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PWR S5GT - 1.6V (Ethernet / XFP)

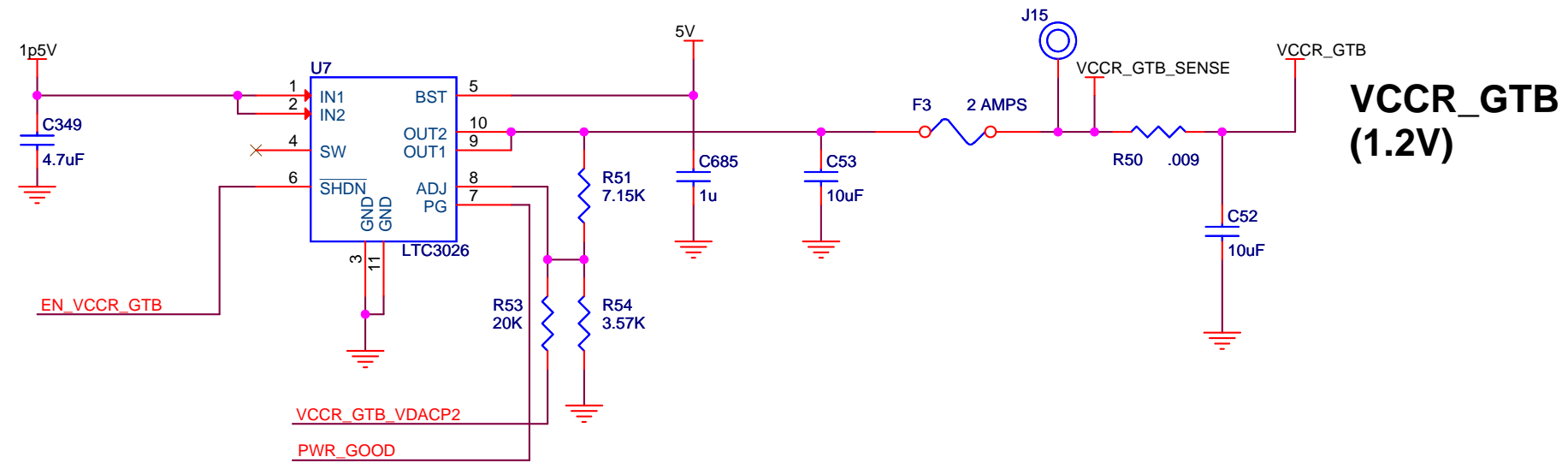


PWR_GOOD	PWR_GOOD	3,4,5,7,13
PG_1p5V	PG_1p5V	10
PG_3p3V	PG_3p3V	5
EN_1p5V	EN_1p5V	10

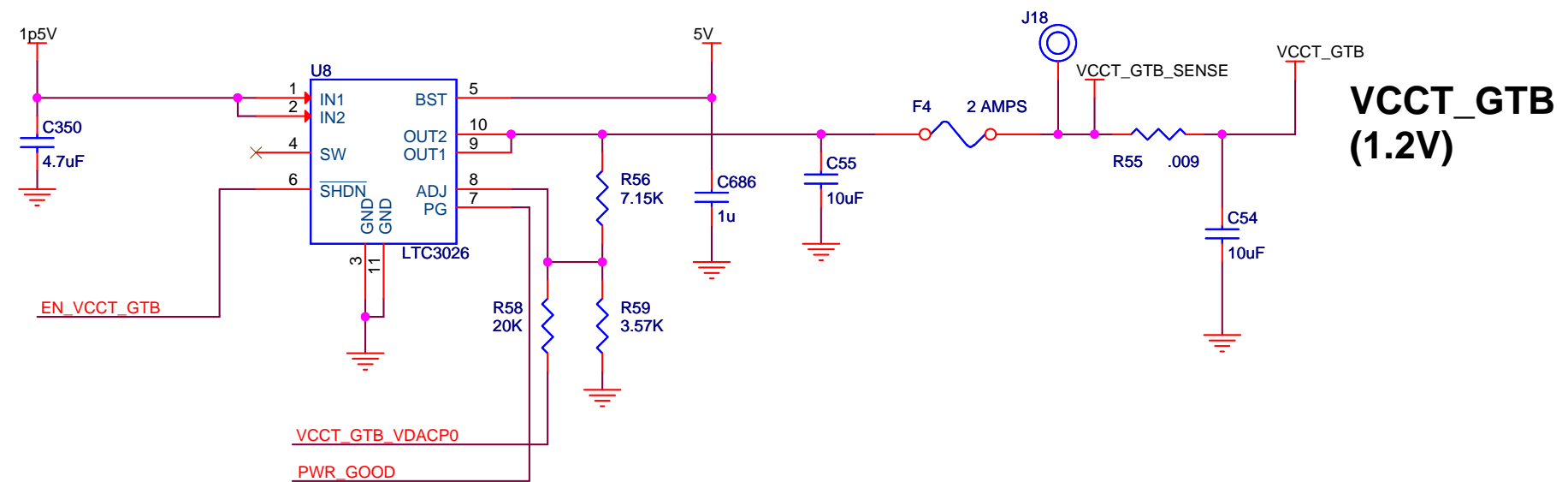


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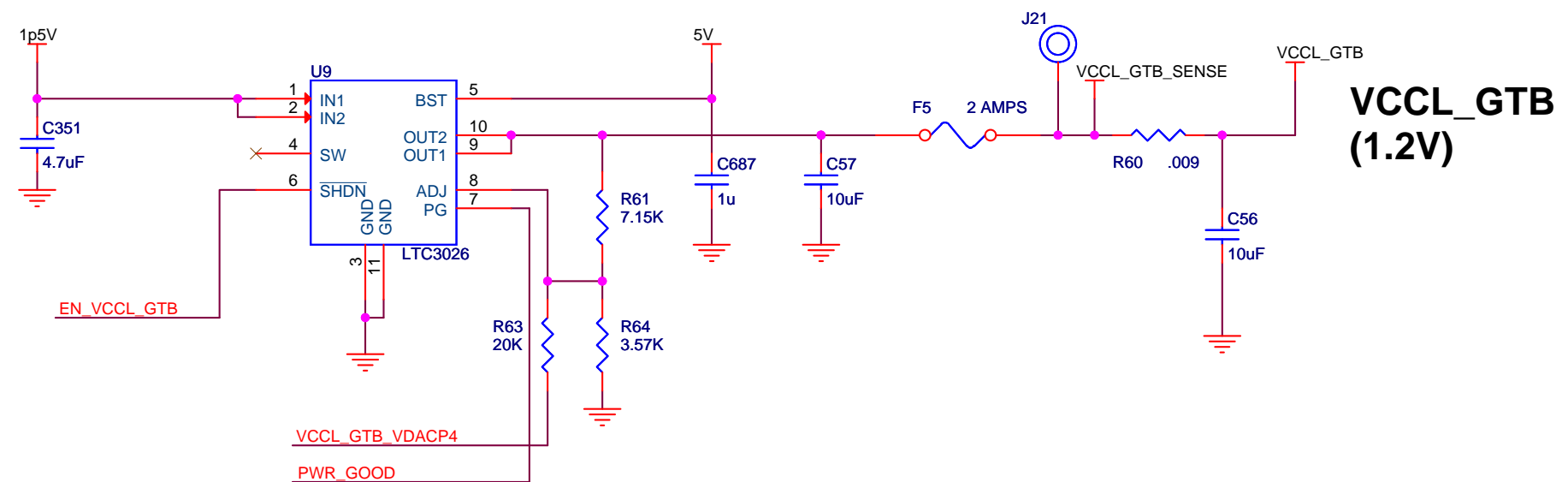
PWR XCVR - GTB



**VCCR_GTB
(1.2V)**



**VCCT_GTB
(1.2V)**



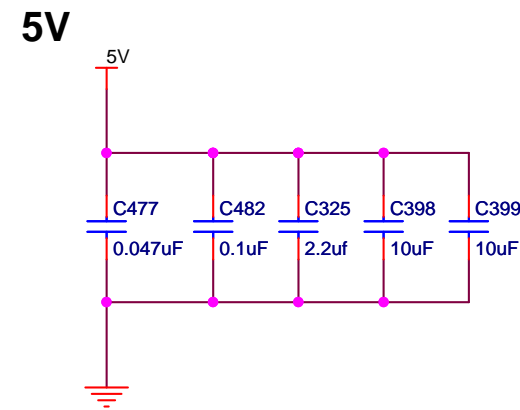
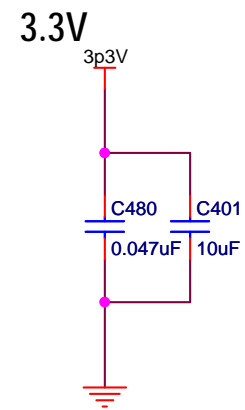
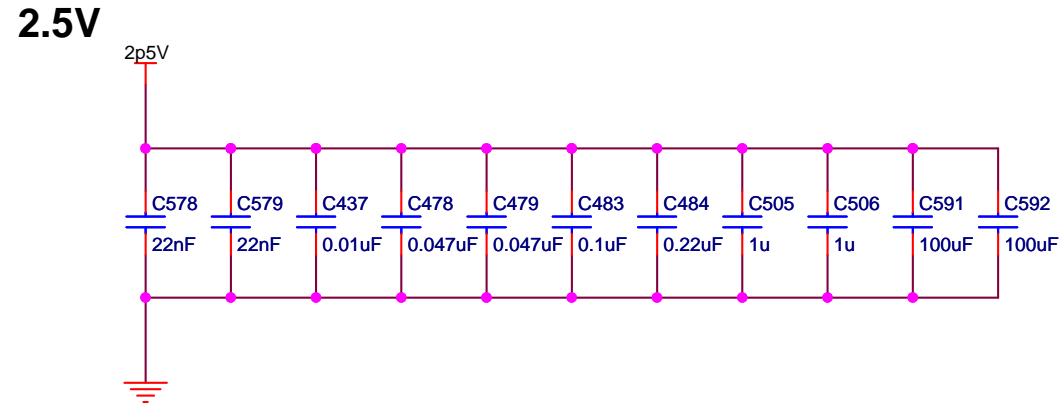
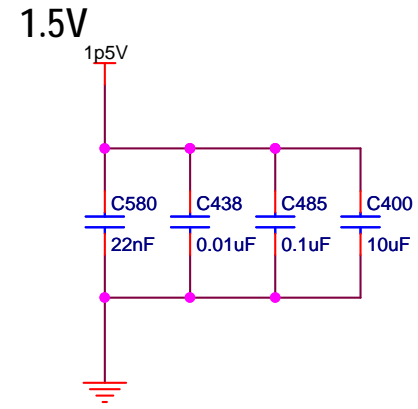
**VCCL_GTB
(1.2V)**

PWR_GOOD	→	PWR_GOOD	3,4,5,6,13
EN_VCCR_GTB	→	EN_VCCR_GTB	10
EN_VCCT_GTB	→	EN_VCCT_GTB	10
EN_VCCL_GTB	→	EN_VCCL_GTB	10
VCCT_GTB_VDACP0	→	VCCT_GTB_VDACP0	9
VCCR_GTB_VDACP2	→	VCCR_GTB_VDACP2	9
VCCL_GTB_VDACP4	→	VCCL_GTB_VDACP4	9

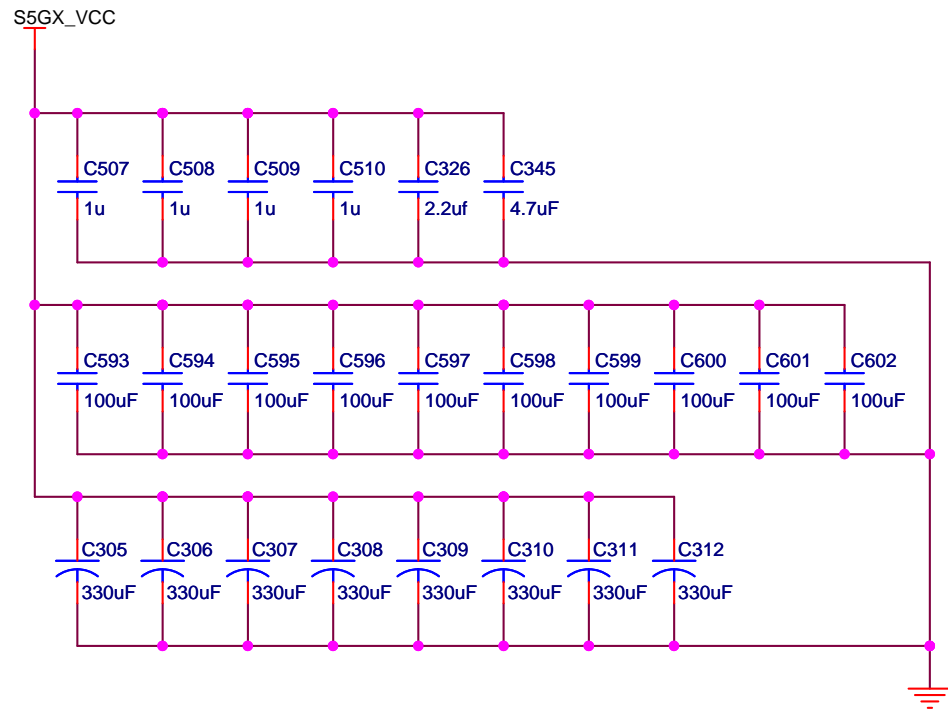


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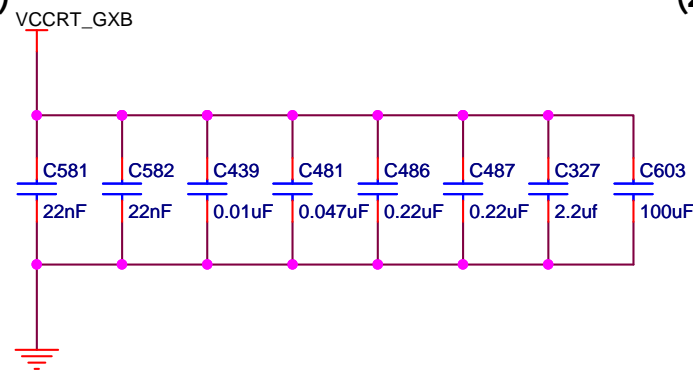
PWR S5GT - Decoupling



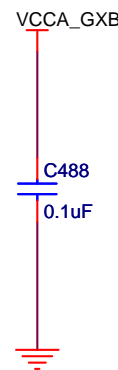
S5GX_VCC (0.85V)



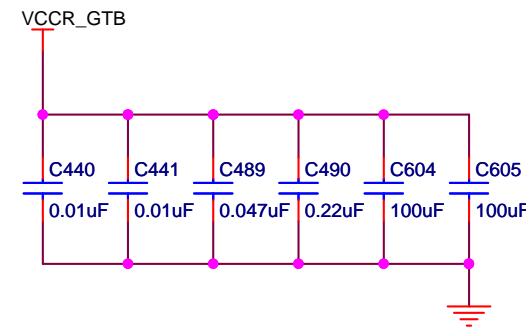
VCCRT_GXB (0.85V/1.0V)



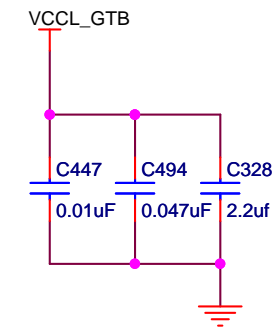
VCCA_GXB (2.5V/3.0V)



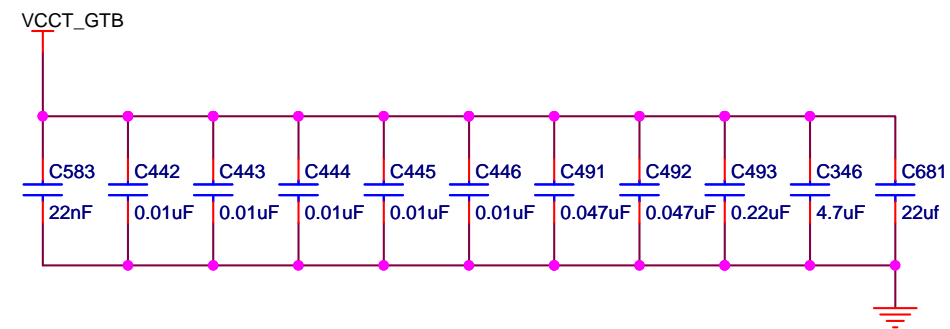
VCCR_GTB (1.0V)



VCCL_GTB (1.0V)

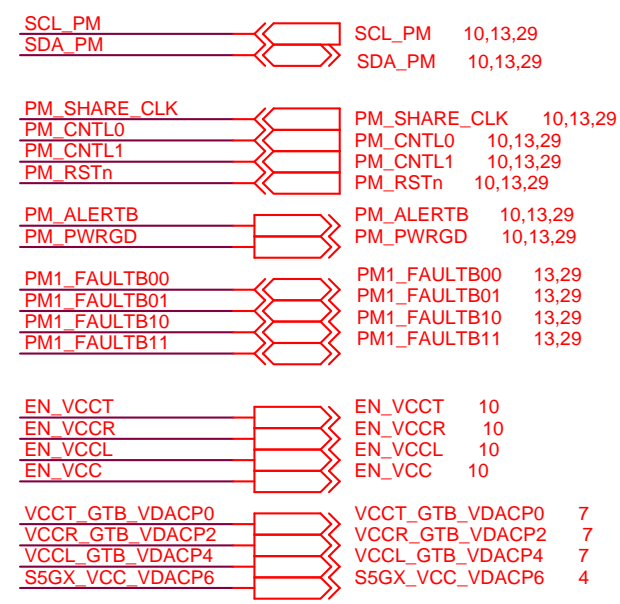
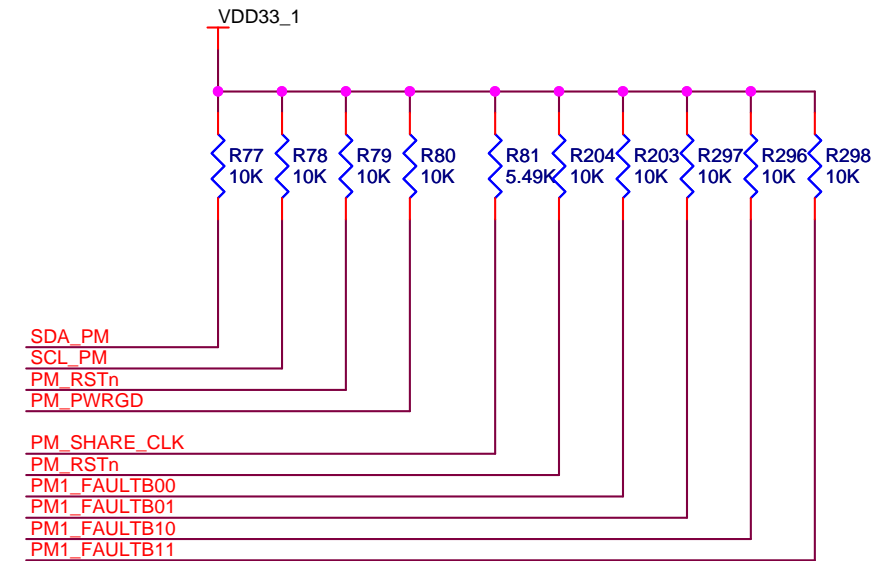
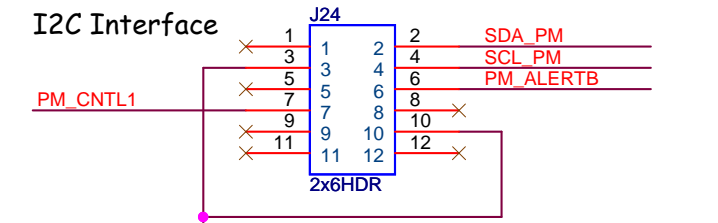
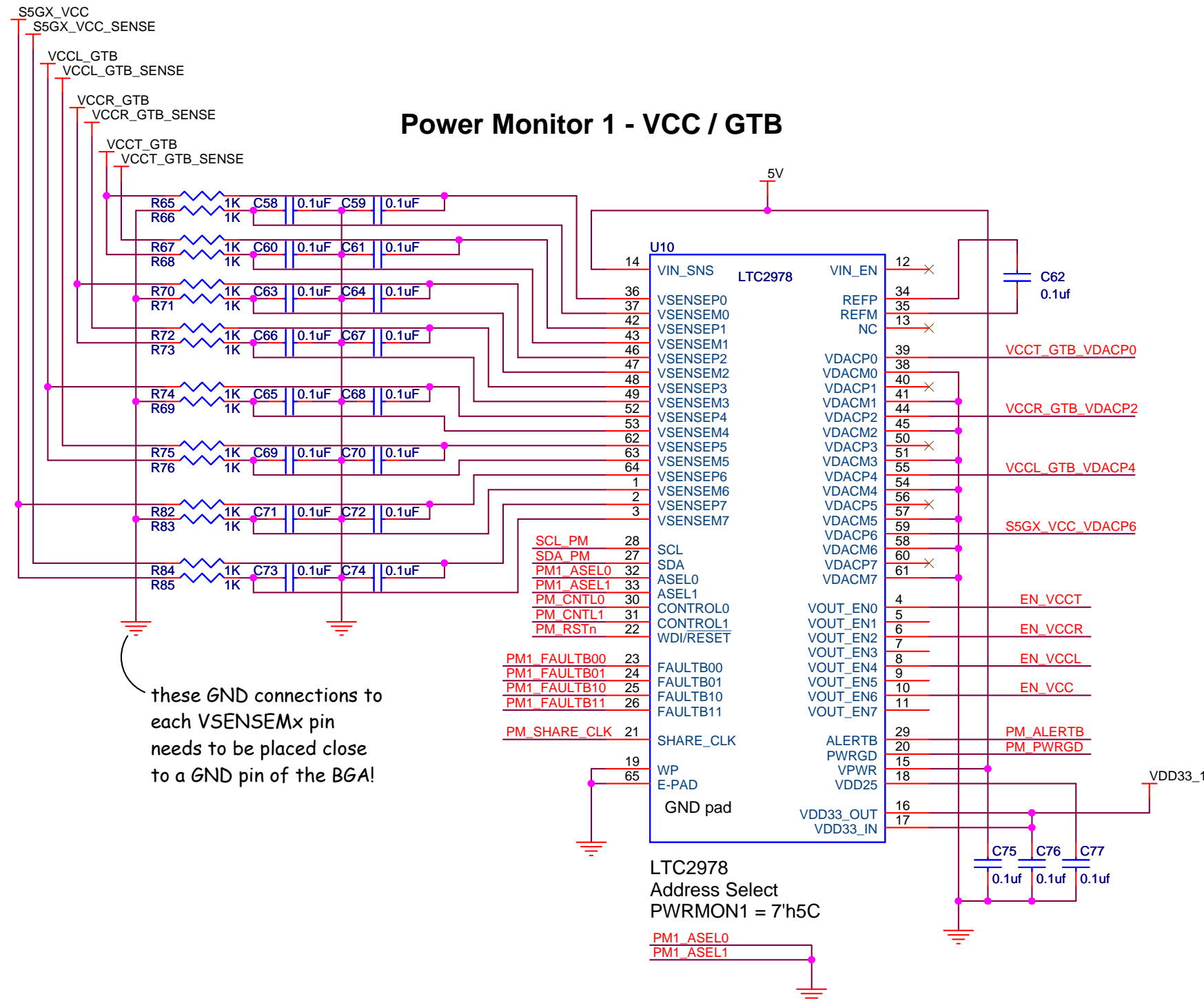


VCCT_GTB (1.0V)



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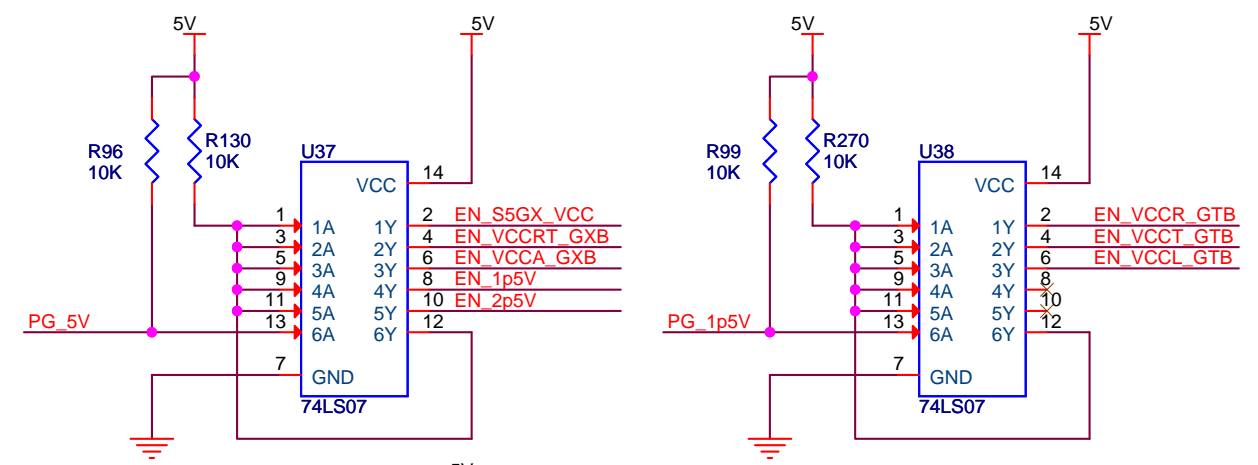
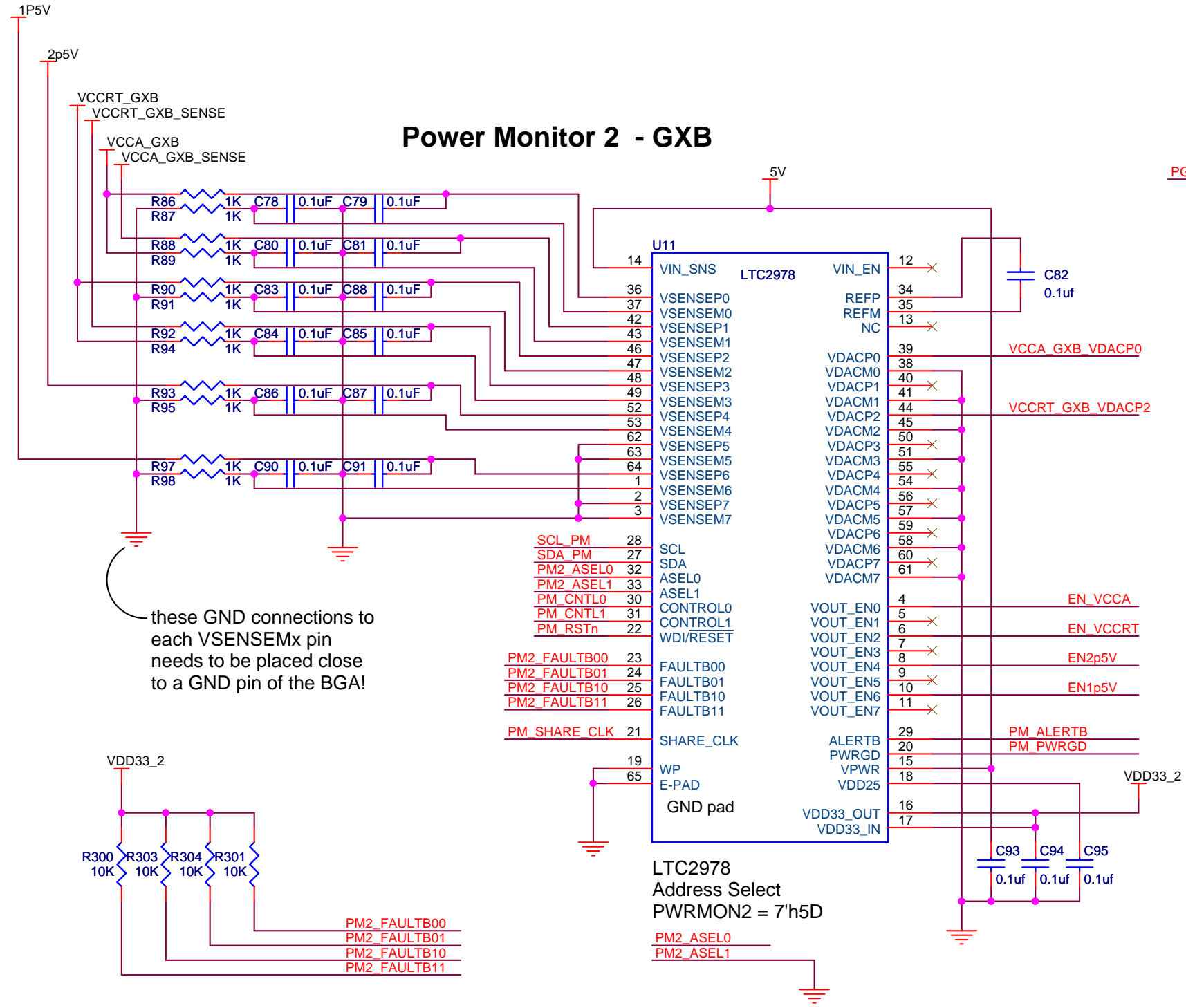
Power Monitor 1 - VCC / GTB



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Power Monitor 2 - GXB

Power Monitor 2 - GXB

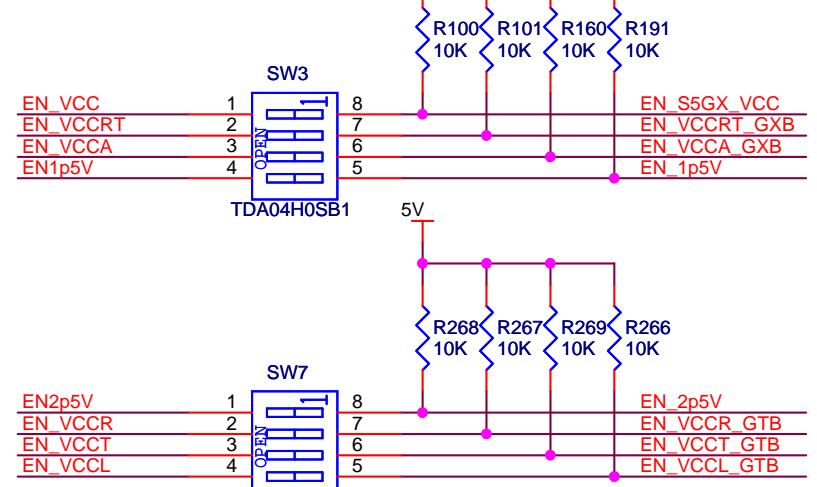


Sequence Enable - Switch 3

SW3-1 open = bypass PM control - S5GX_VCC
 SW3-1 close = PM sequence enabled - S5GX_VCC
 SW3-2 open = bypass PM control - VCCRT_GXB
 SW3-2 close = PM sequence enabled - VCCRT_GXB
 SW3-3 open = bypass PM control - VCCA_GXB
 SW3-3 close = PM sequence enabled - VCCA_GXB
 SW3-4 open = bypass PM control - 1p5V
 SW3-4 close = PM sequence enabled - 1p5V

Sequence Enable - Switch 7

SW7-1 open = bypass PM control - 2p5V
 SW7-1 close = PM sequence enabled - 2p5V
 SW7-2 open = bypass PM control - VCCR_GTB
 SW7-2 close = PM sequence enabled - VCCR_GTB
 SW7-3 open = bypass PM control - VCCT_GTB
 SW7-3 close = PM sequence enabled - VCCT_GTB
 SW7-4 open = bypass PM control - VCCL_GTB
 SW7-4 close = PM sequence enabled - VCCL_GTB



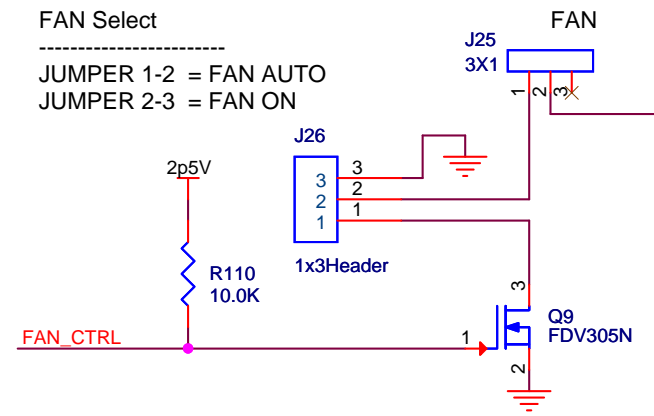
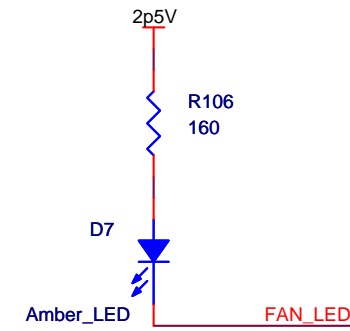
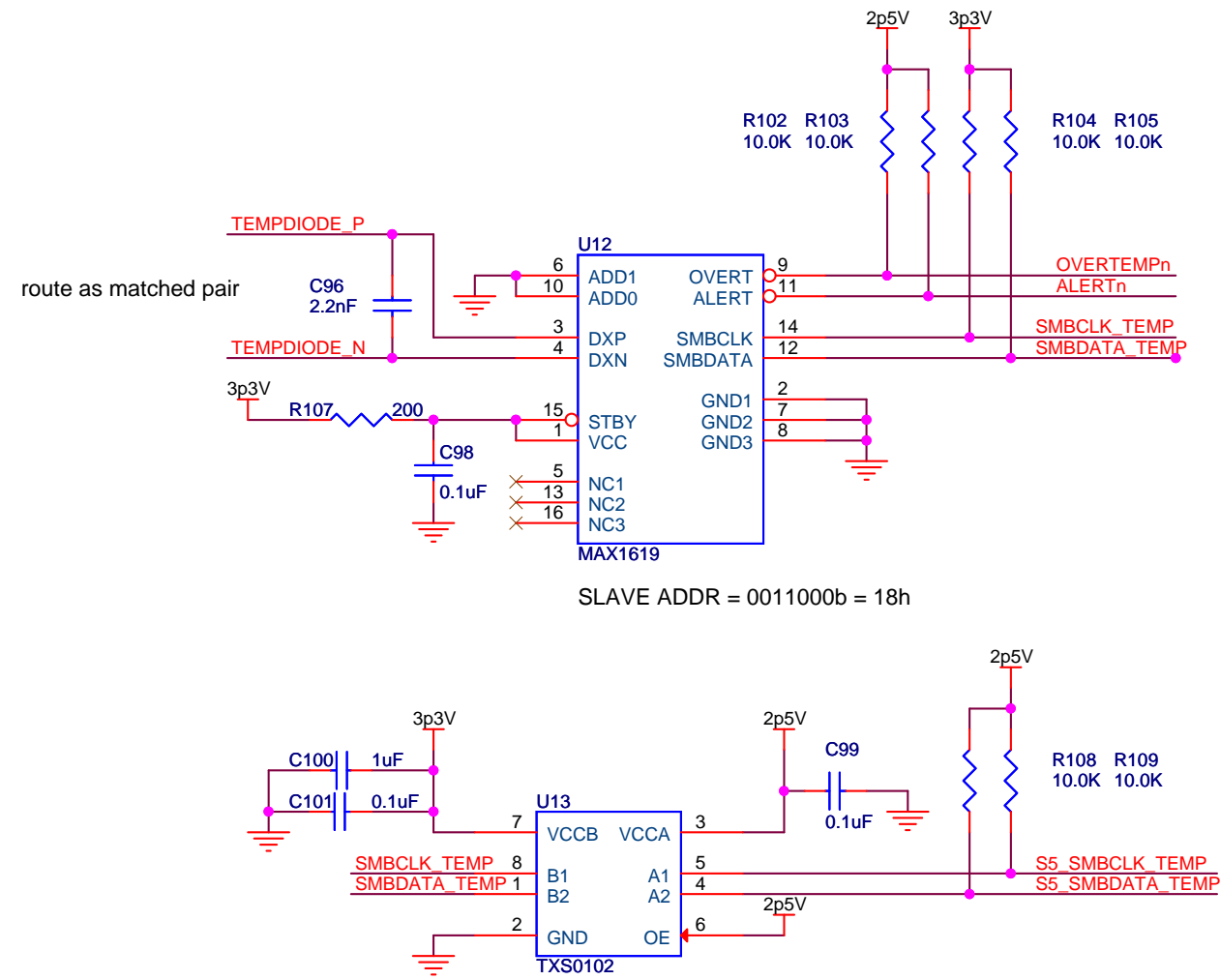
SCL_PM	SCL_PM	9,13,29	PG_5V	PG_5V	3,5
SDA_PM	SDA_PM	9,13,29	PG_1p5V	PG_1p5V	6
PM_SHARE_CLK	PM_SHARE_CLK	9,13,29	EN_S5GX_VCC	EN_S5GX_VCC	4
PM_CNTL0	PM_CNTL0	9,13,29	EN_VCCR_GTB	EN_VCCR_GTB	5
PM_CNTL1	PM_CNTL1	9,13,29	EN_VCCA_GXB	EN_VCCA_GXB	5
PM_RSTn	PM_RSTn	9,13,29	EN_1p5V	EN_1p5V	6
PM_ALERTB	PM_ALERTB	9,13,29	EN_2p5V	EN_2p5V	3
PM_PWRGD	PM_PWRGD	9,13,29	EN_VCCR_GTB	EN_VCCR_GTB	7
PM2_FAULTB00	PM2_FAULTB00	13,29	EN_VCCT_GTB	EN_VCCT_GTB	7
PM2_FAULTB01	PM2_FAULTB01	13,29	EN_VCCL_GTB	EN_VCCL_GTB	7
PM2_FAULTB10	PM2_FAULTB10	13,29	EN_VCC	EN_VCC	9
PM2_FAULTB11	PM2_FAULTB11	13,29	EN_VCCR	EN_VCCR	9
			EN_VCCT	EN_VCCT	9
			EN_VCCL	EN_VCCL	9
			VCCA_GXB_VDACP0	VCCA_GXB_VDACP0	5
			VCCRT_GXB_VDACP2	VCCRT_GXB_VDACP2	5

LTC2978
 Address Select
 PWRMON2 = 7'h5D

these GND connections to each VSENSEmx pin needs to be placed close to a GND pin of the BGA!



Temperature Measure

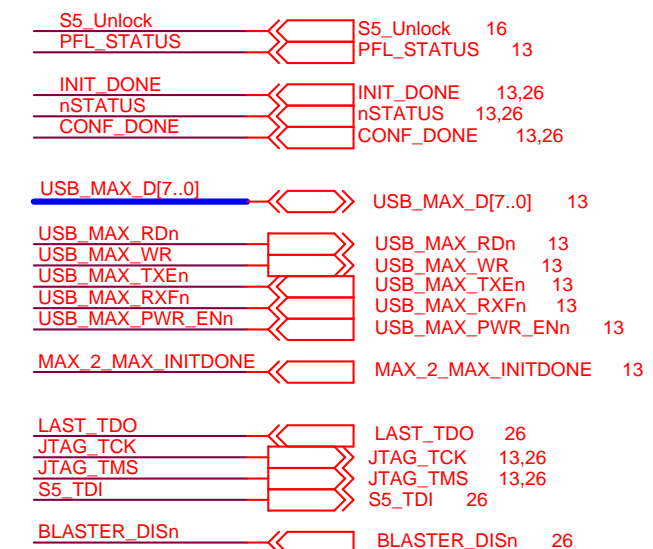
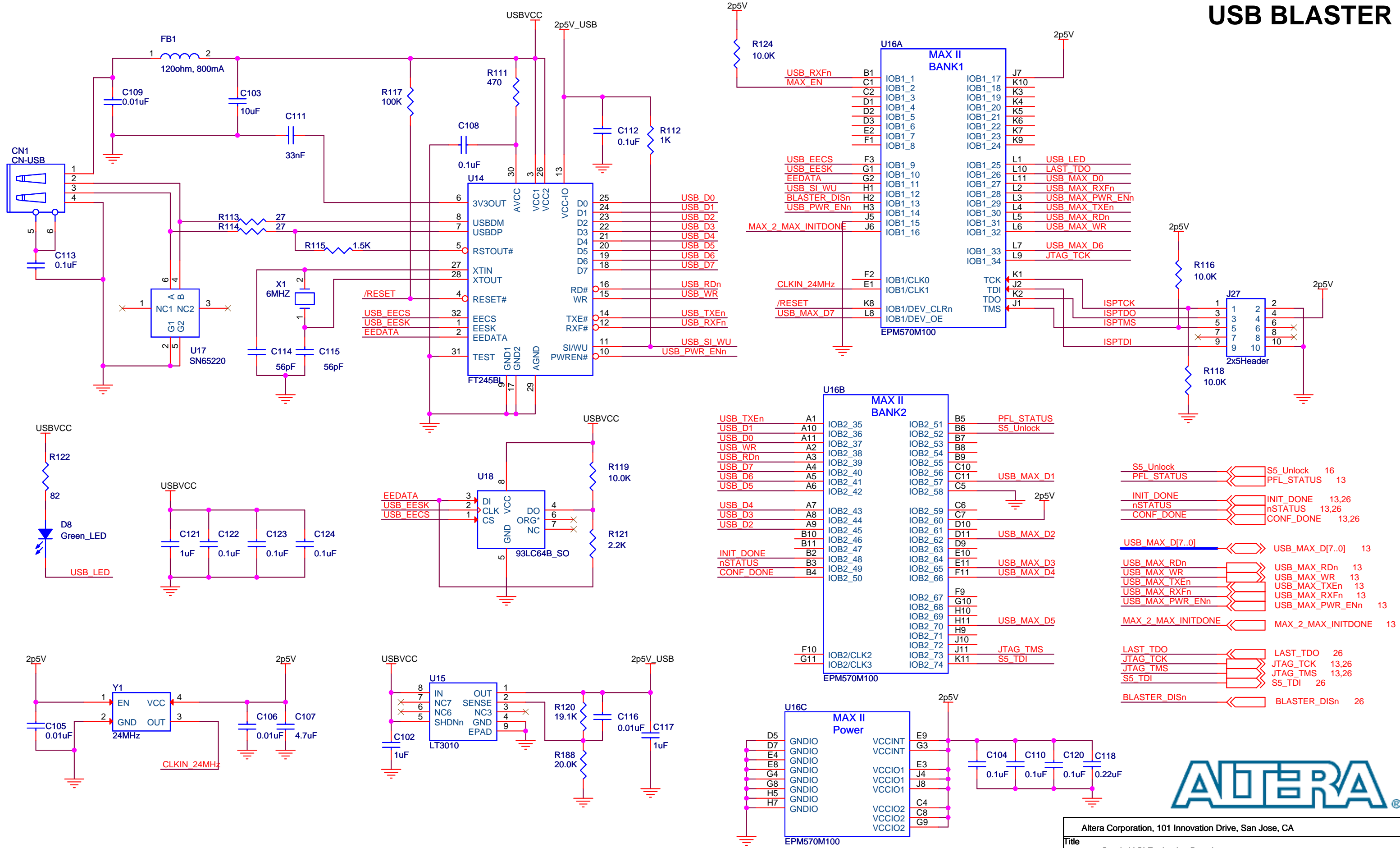


S5_SMBCLK_TEMP	S5_SMBCLK_TEMP	13,29
S5_SMBDATA_TEMP	S5_SMBDATA_TEMP	13,29
FAN_CTRL	FAN_CTRL	13,29
FAN_LED	FAN_LED	13,29
OVERTEMPn	OVERTEMPn	13,29
ALERTn	ALERTn	13,29
TEMPDIODE_P	TEMPDIODE_P	26
TEMPDIODE_N	TEMPDIODE_N	26



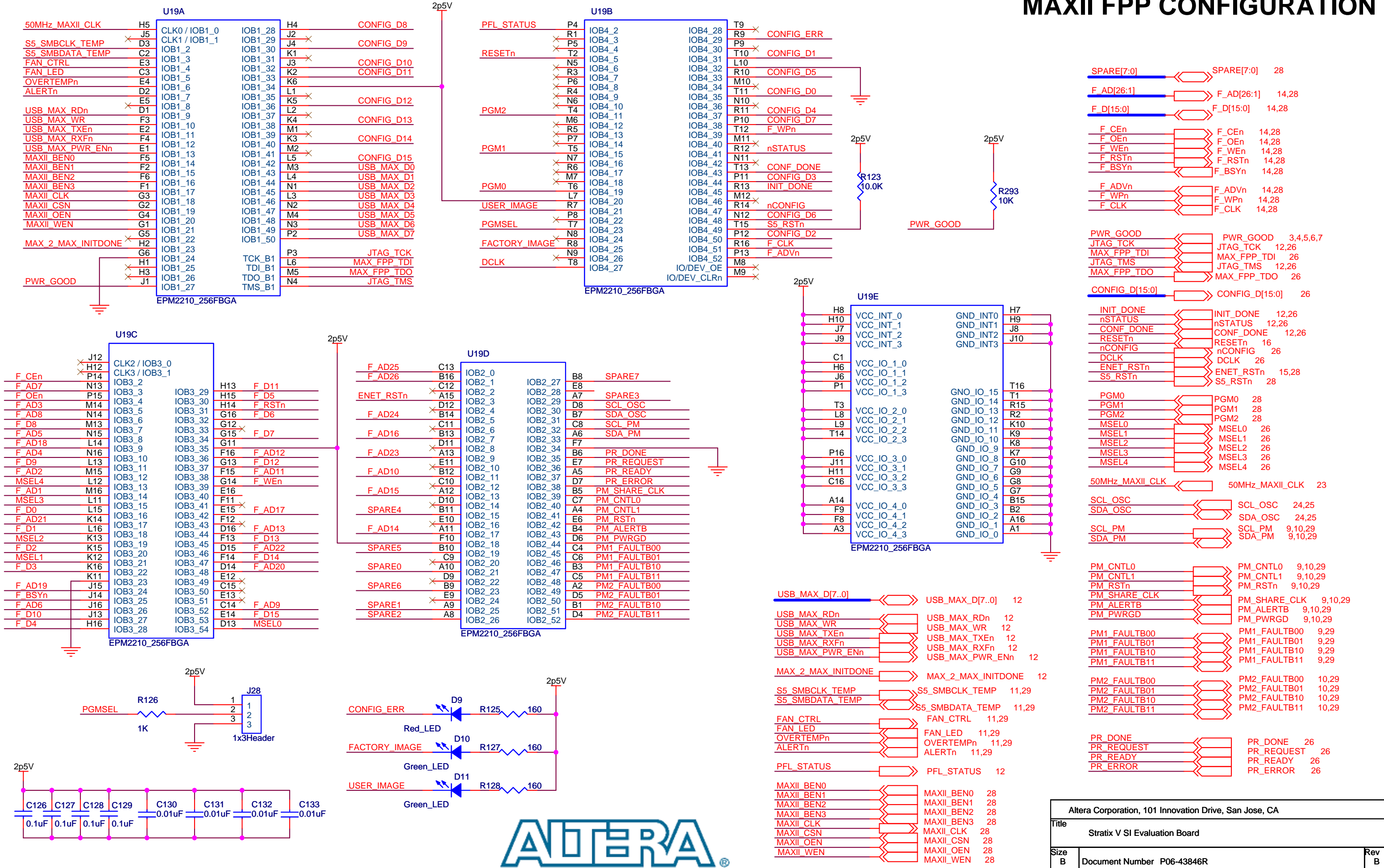
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USB BLASTER



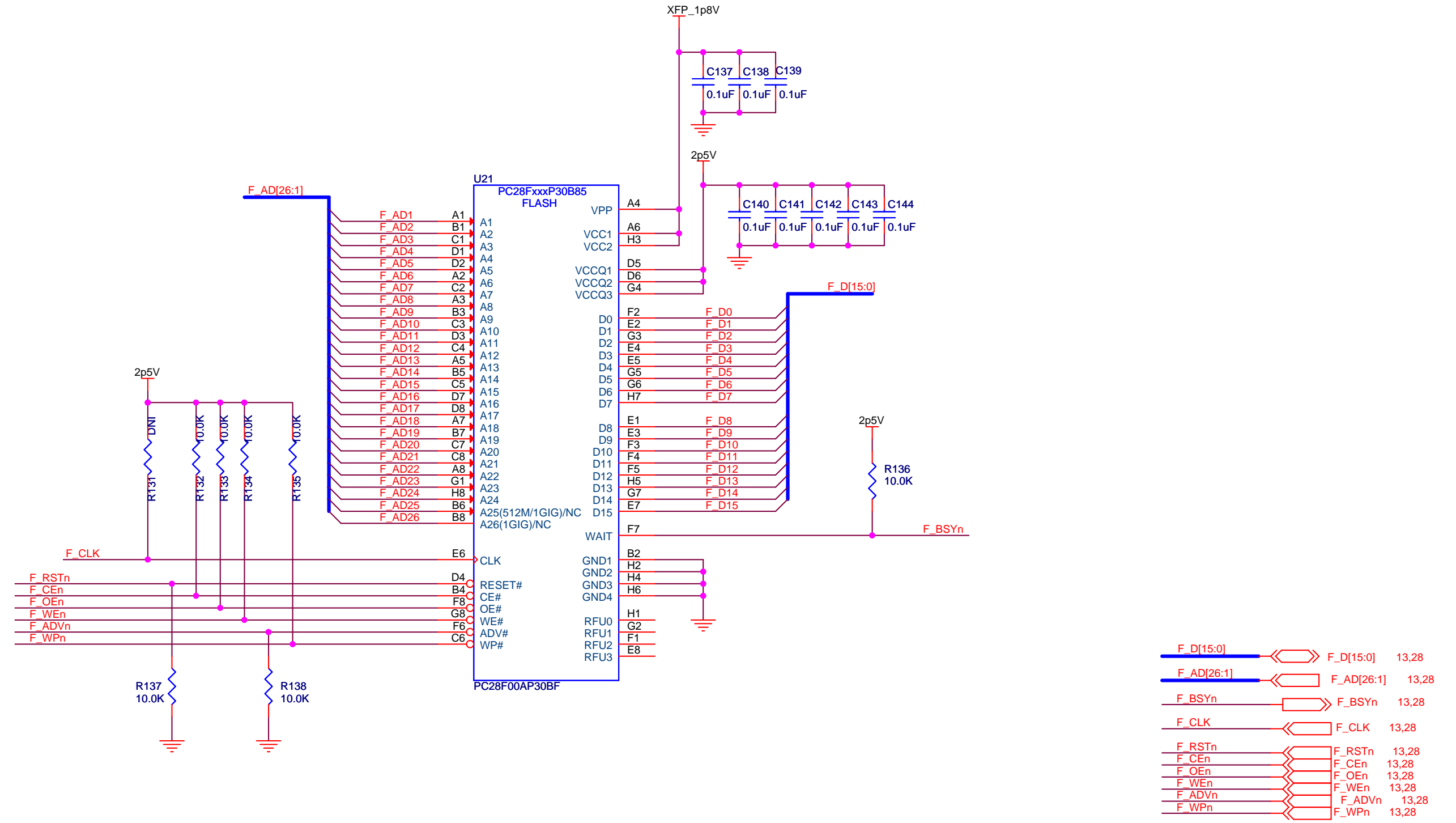
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MAXII FPP CONFIGURATION



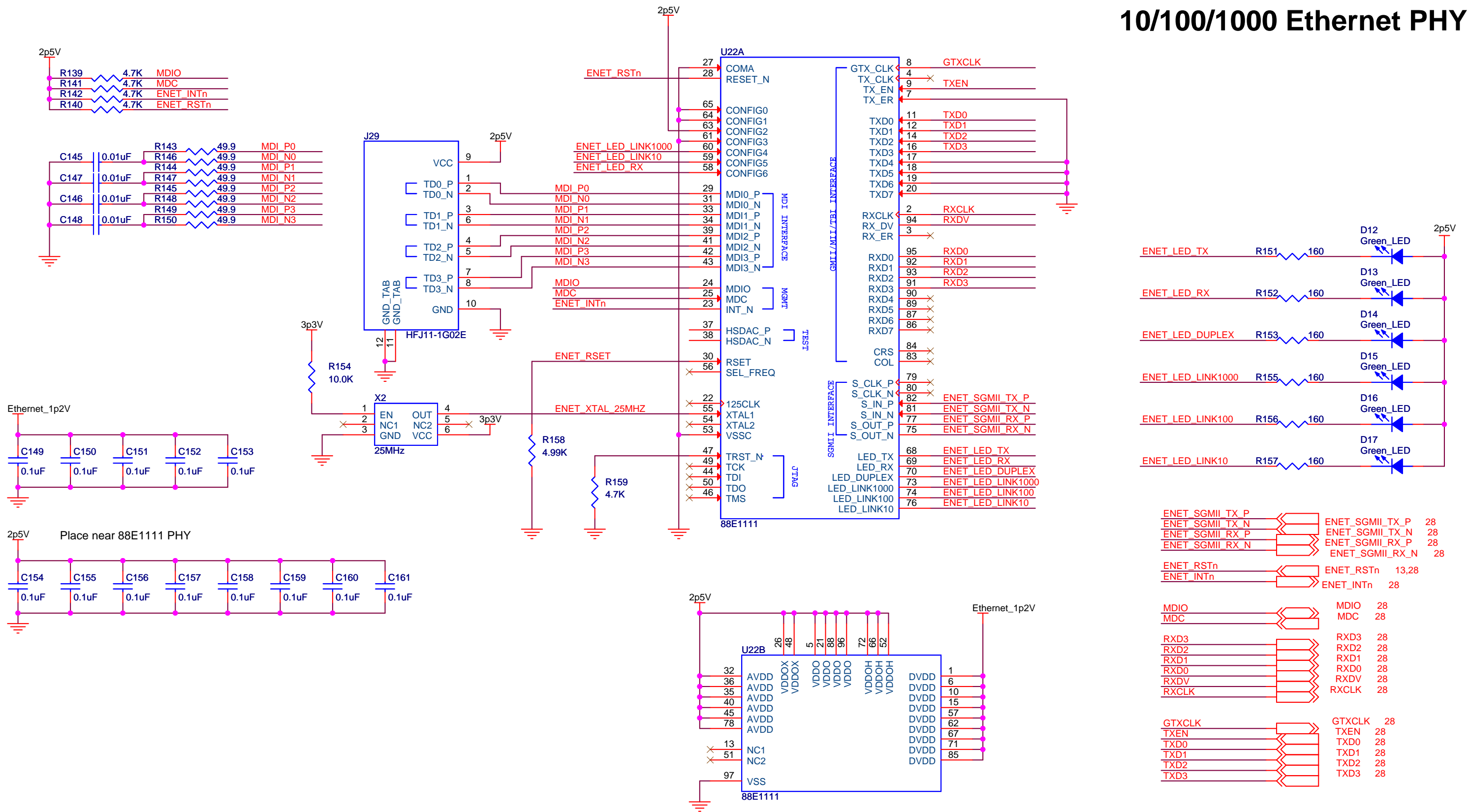
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FLASH MEMORY

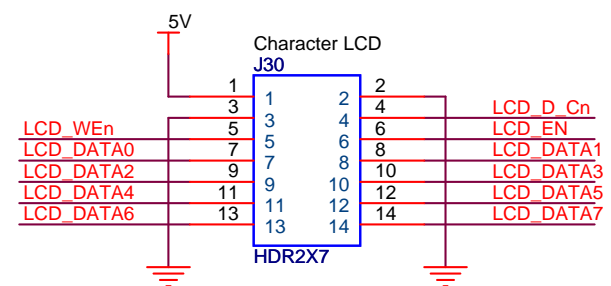
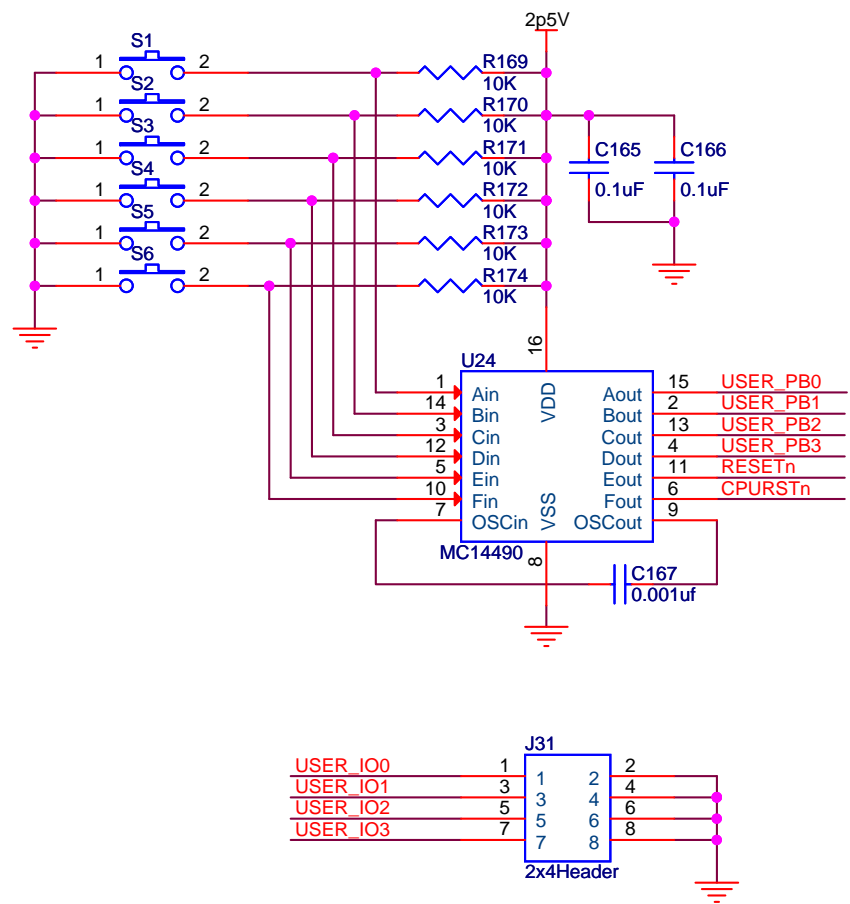
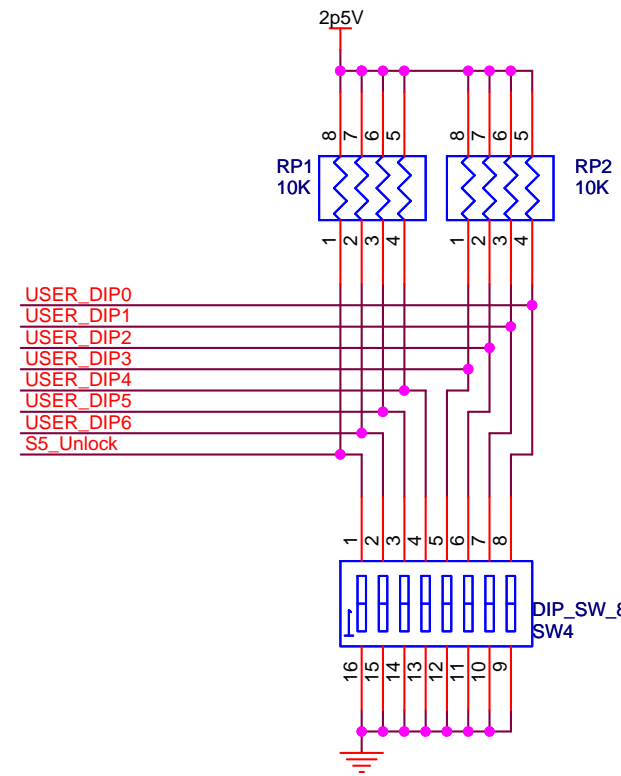
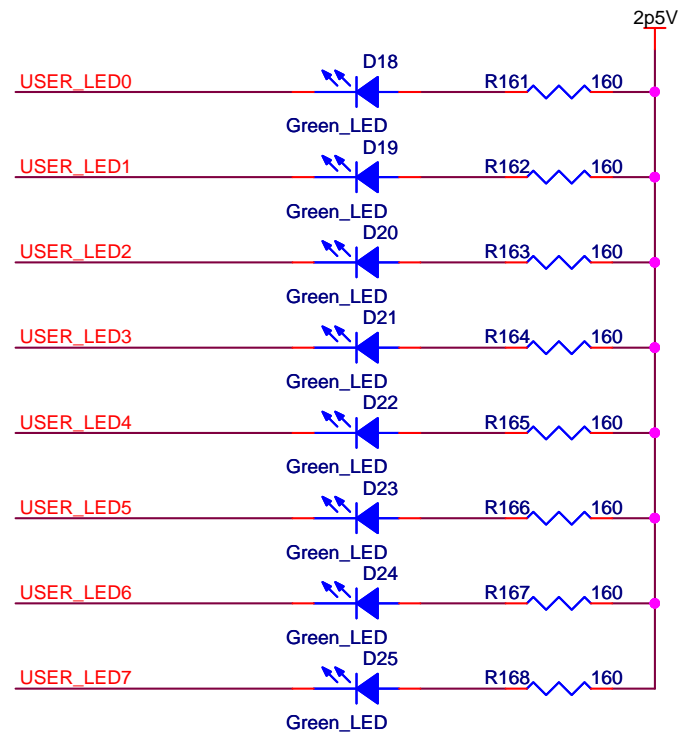


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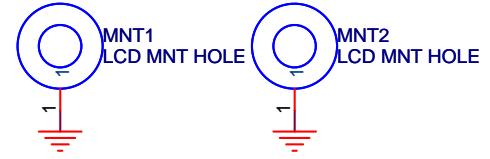
10/100/1000 Ethernet PHY



BUTTONS, SWITCHES, LEDS, LCD DISPLAY



LCD DISPLAY HEADER



USER_IO0	USER_IO0	30
USER_IO1	USER_IO1	30
USER_IO2	USER_IO2	30
USER_IO3	USER_IO3	30

USER_DIP0	USER_DIP0	30
USER_DIP1	USER_DIP1	30
USER_DIP2	USER_DIP2	30
USER_DIP3	USER_DIP3	30
USER_DIP4	USER_DIP4	30
USER_DIP5	USER_DIP5	30
USER_DIP6	USER_DIP6	30
S5_Unlock	S5_Unlock	12

USER_PB0	USER_PB0	30
USER_PB1	USER_PB1	30
USER_PB2	USER_PB2	30
USER_PB3	USER_PB3	30
RESETn	RESETn	13
CPURSTn	CPURSTn	30

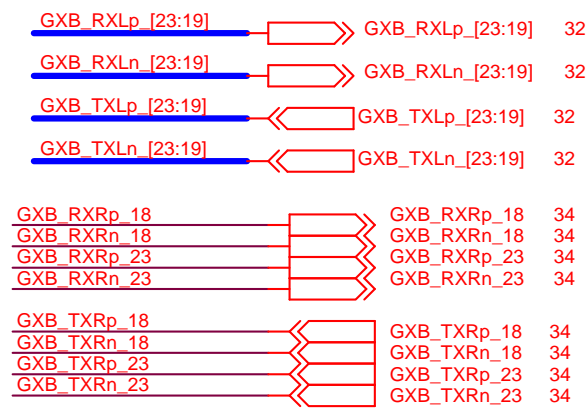
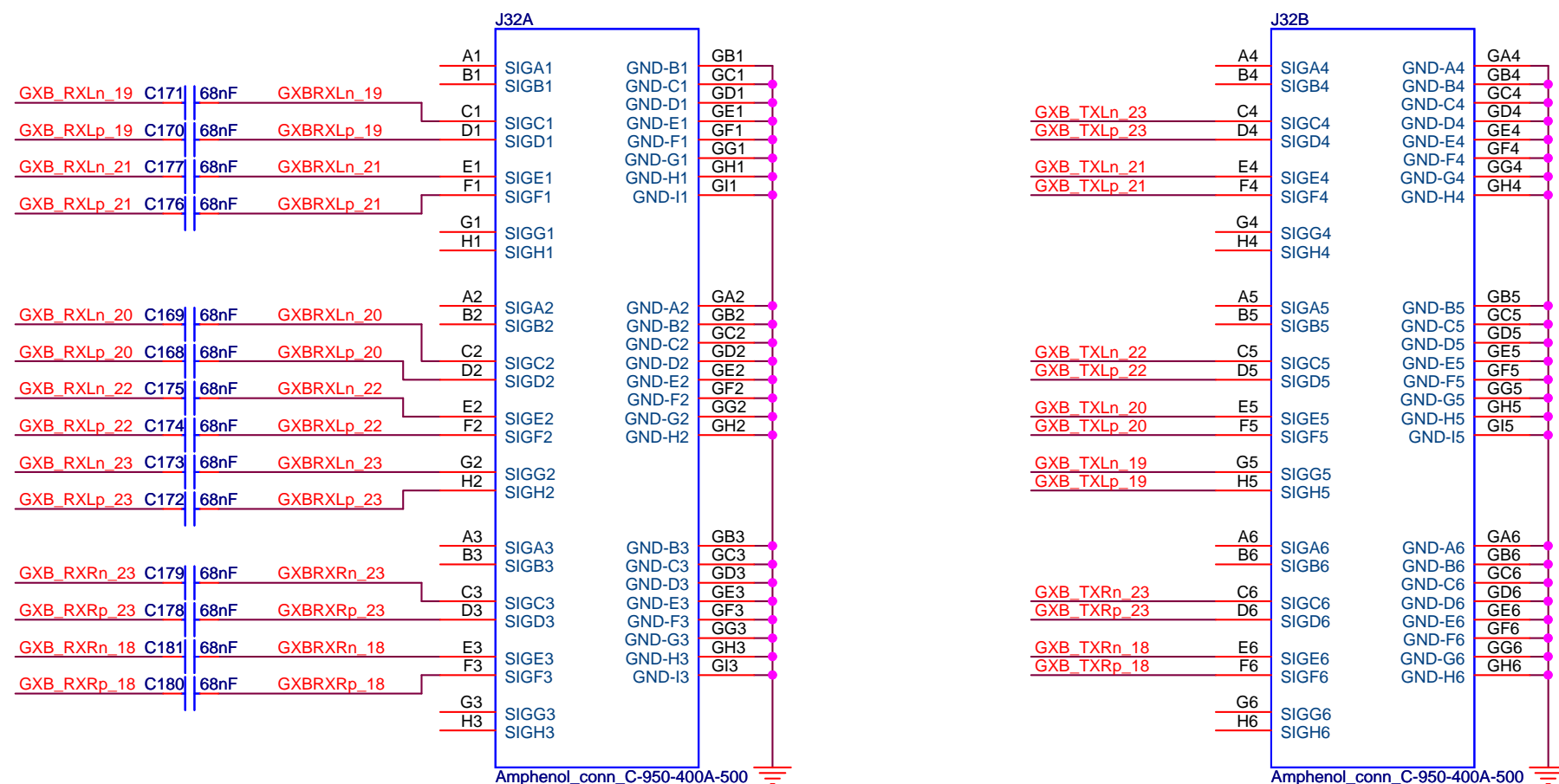
USER_LED0	USER_LED0	30
USER_LED1	USER_LED1	30
USER_LED2	USER_LED2	30
USER_LED3	USER_LED3	30
USER_LED4	USER_LED4	30
USER_LED5	USER_LED5	30
USER_LED6	USER_LED6	30
USER_LED7	USER_LED7	30

LCD_D_Cn	LCD_D_Cn	29
LCD_EN	LCD_EN	29
LCD_WEn	LCD_WEn	29
LCD_DATA0	LCD_DATA0	29
LCD_DATA1	LCD_DATA1	29
LCD_DATA2	LCD_DATA2	29
LCD_DATA3	LCD_DATA3	29
LCD_DATA4	LCD_DATA4	29
LCD_DATA5	LCD_DATA5	29
LCD_DATA6	LCD_DATA6	29
LCD_DATA7	LCD_DATA7	29



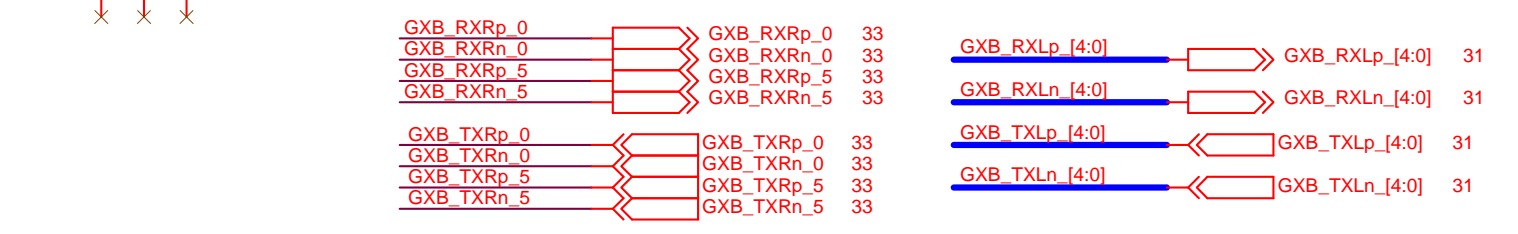
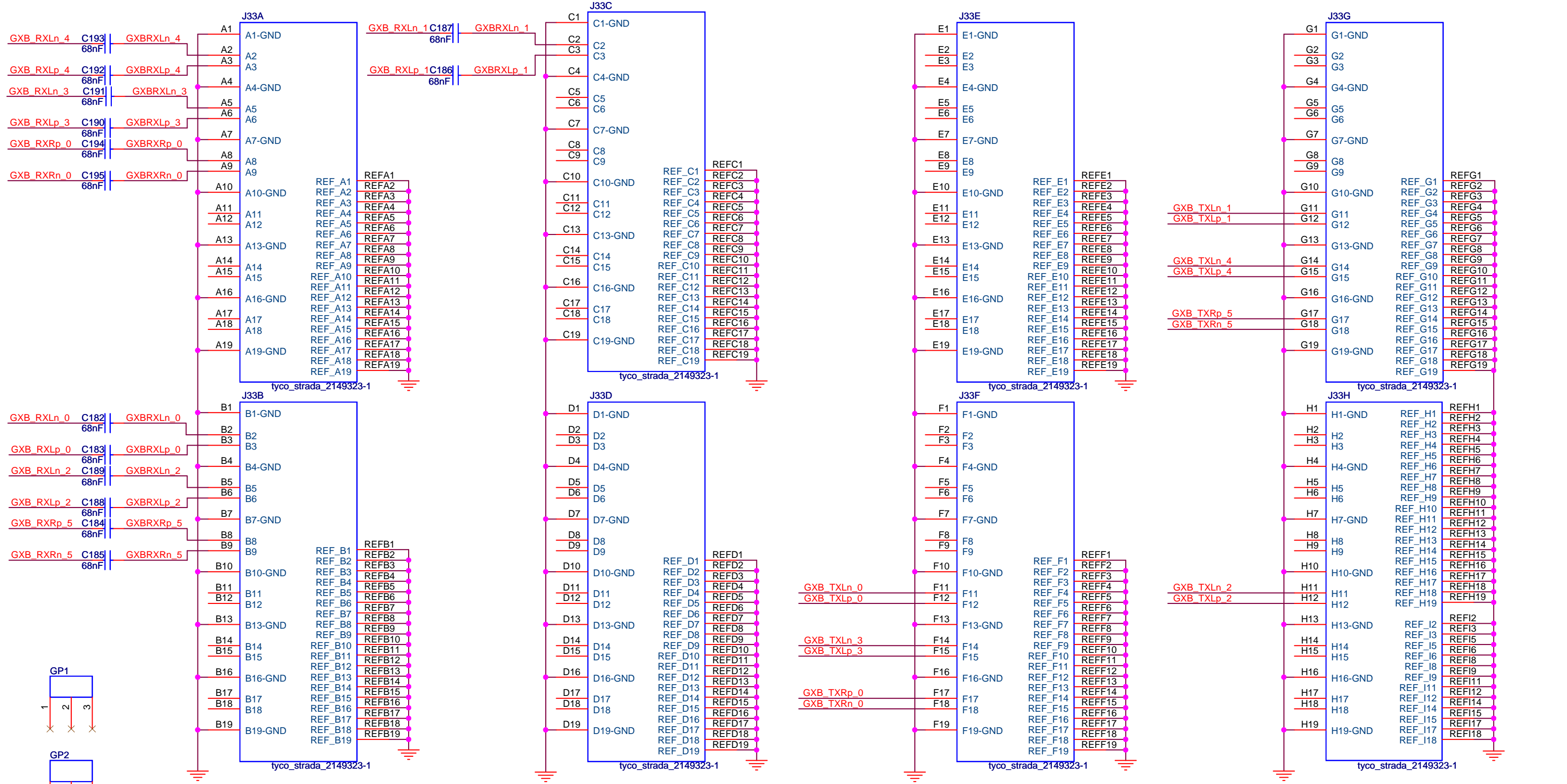
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FCI / Amphenol Backplane Interface



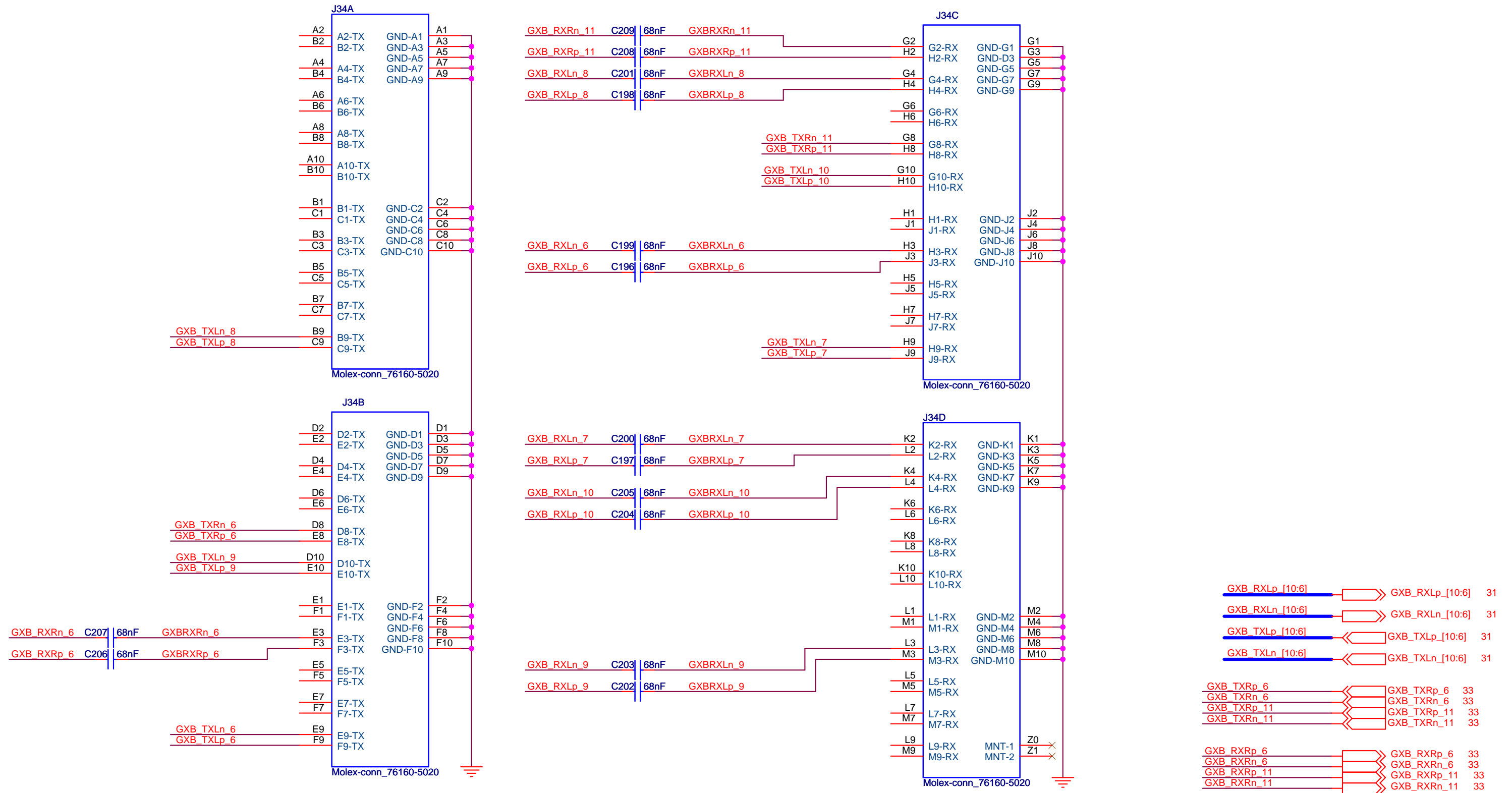
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Tyco Backplane Interface



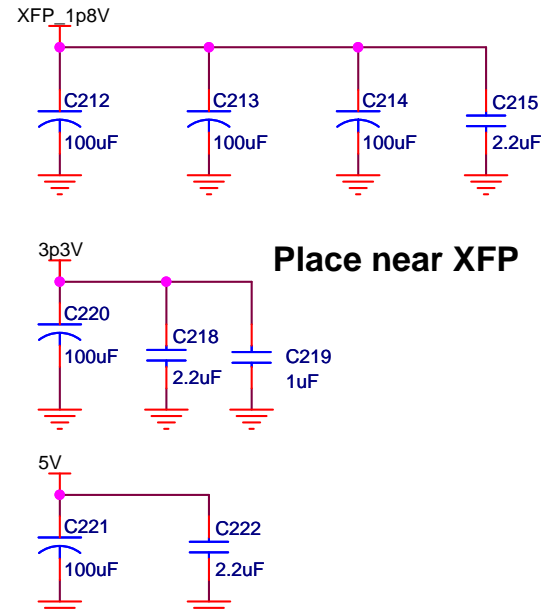
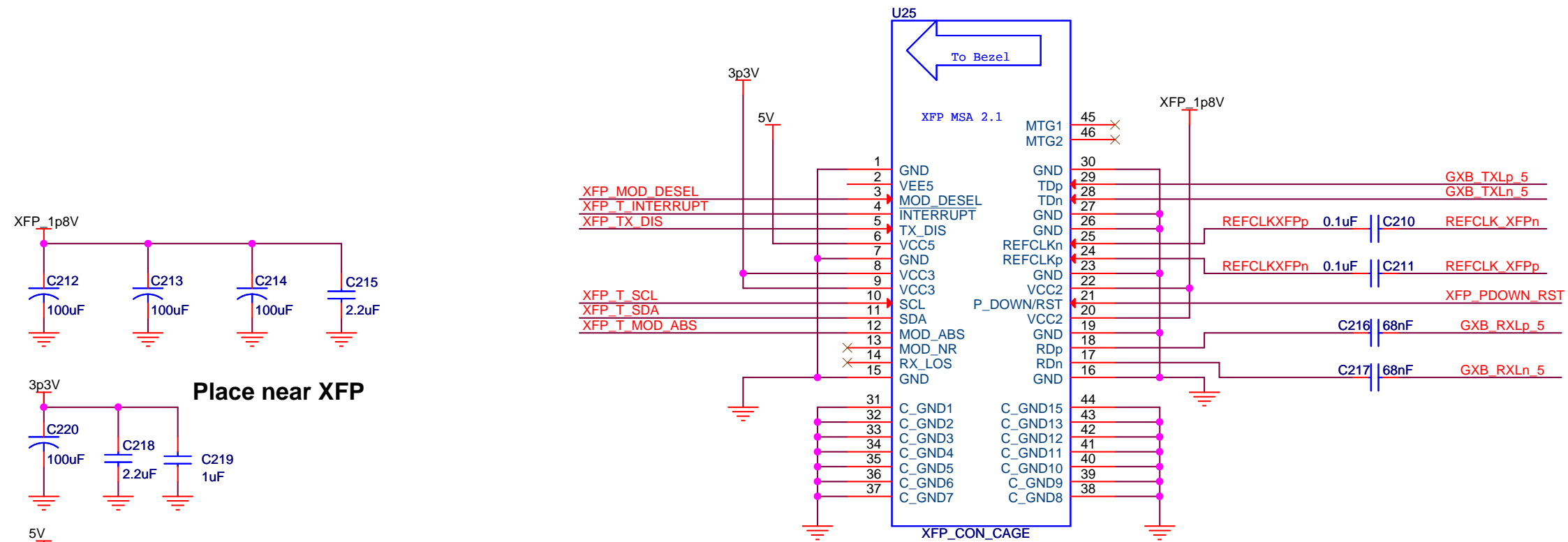
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Molex Backplane Interface

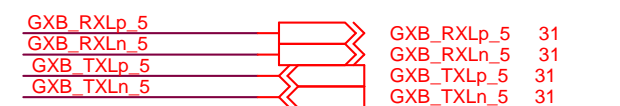
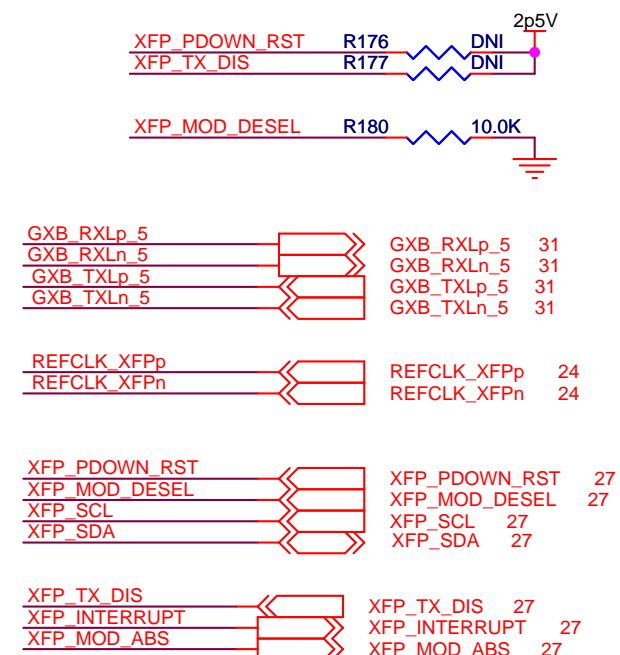
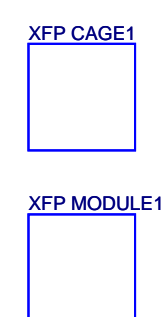
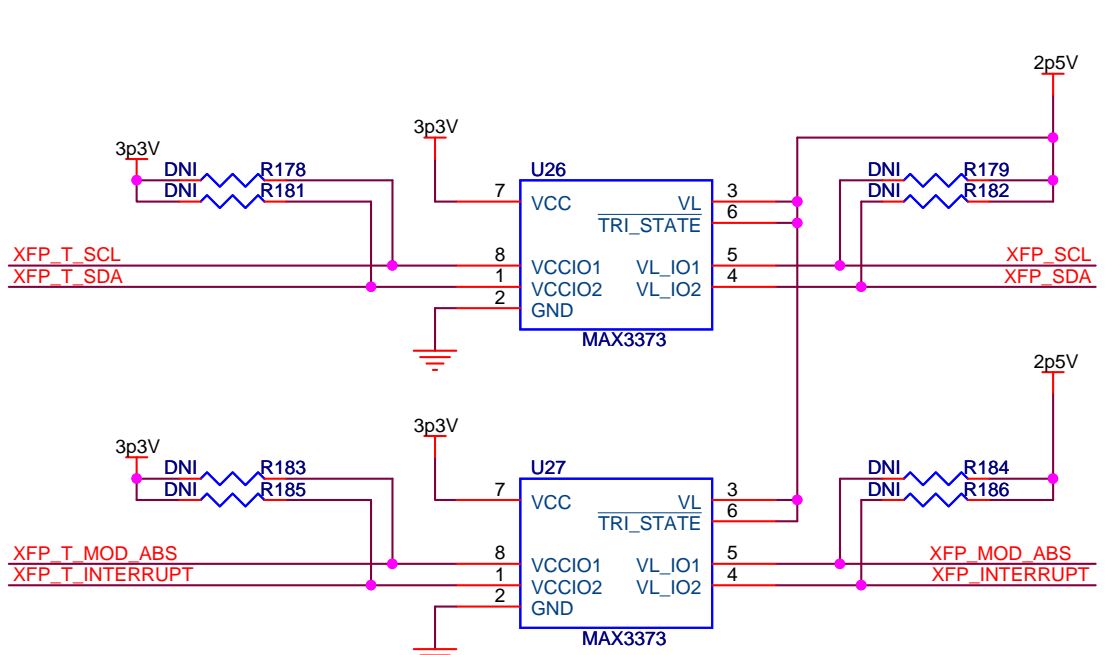


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XFP Interface

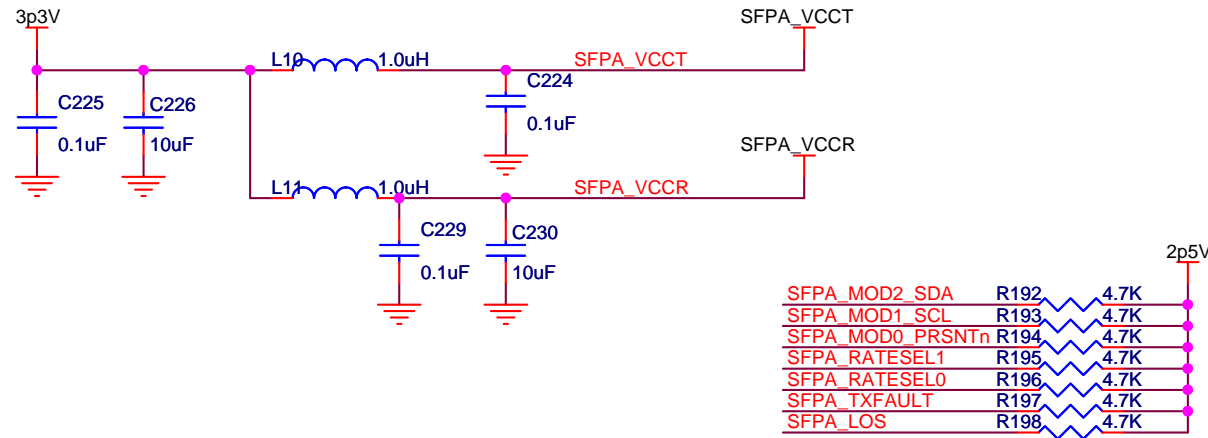


Place near XFP

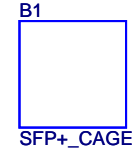
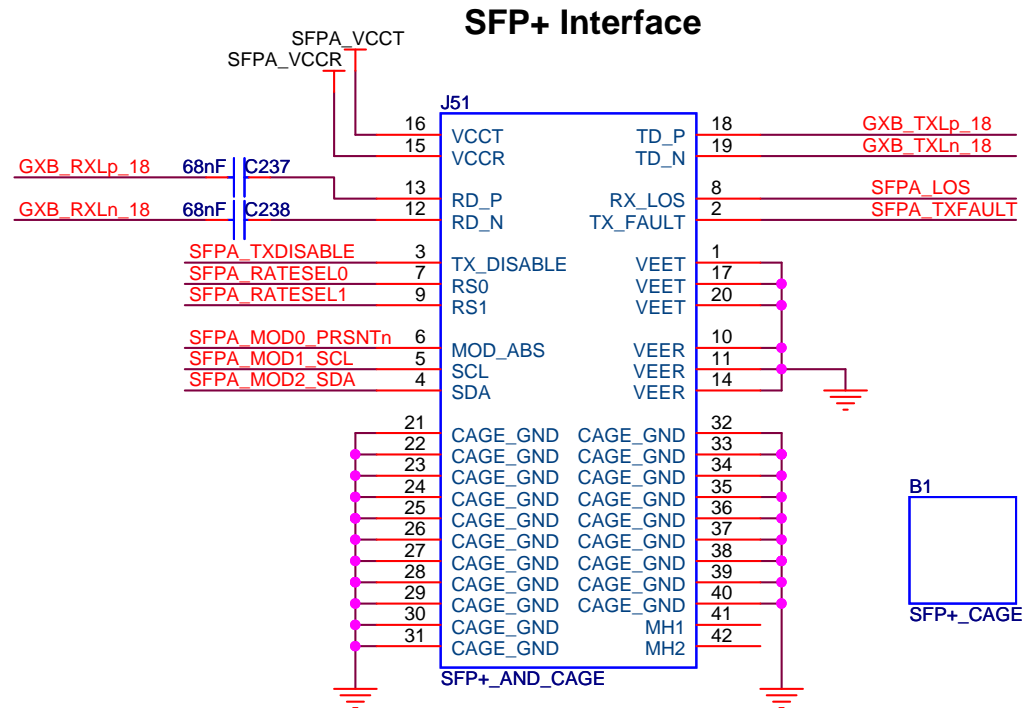


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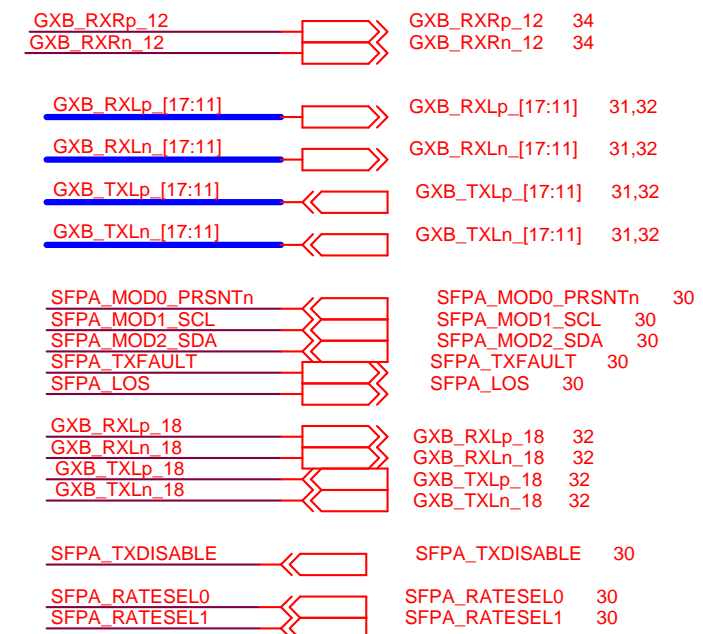
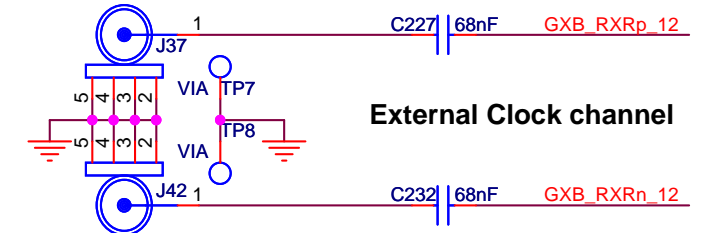
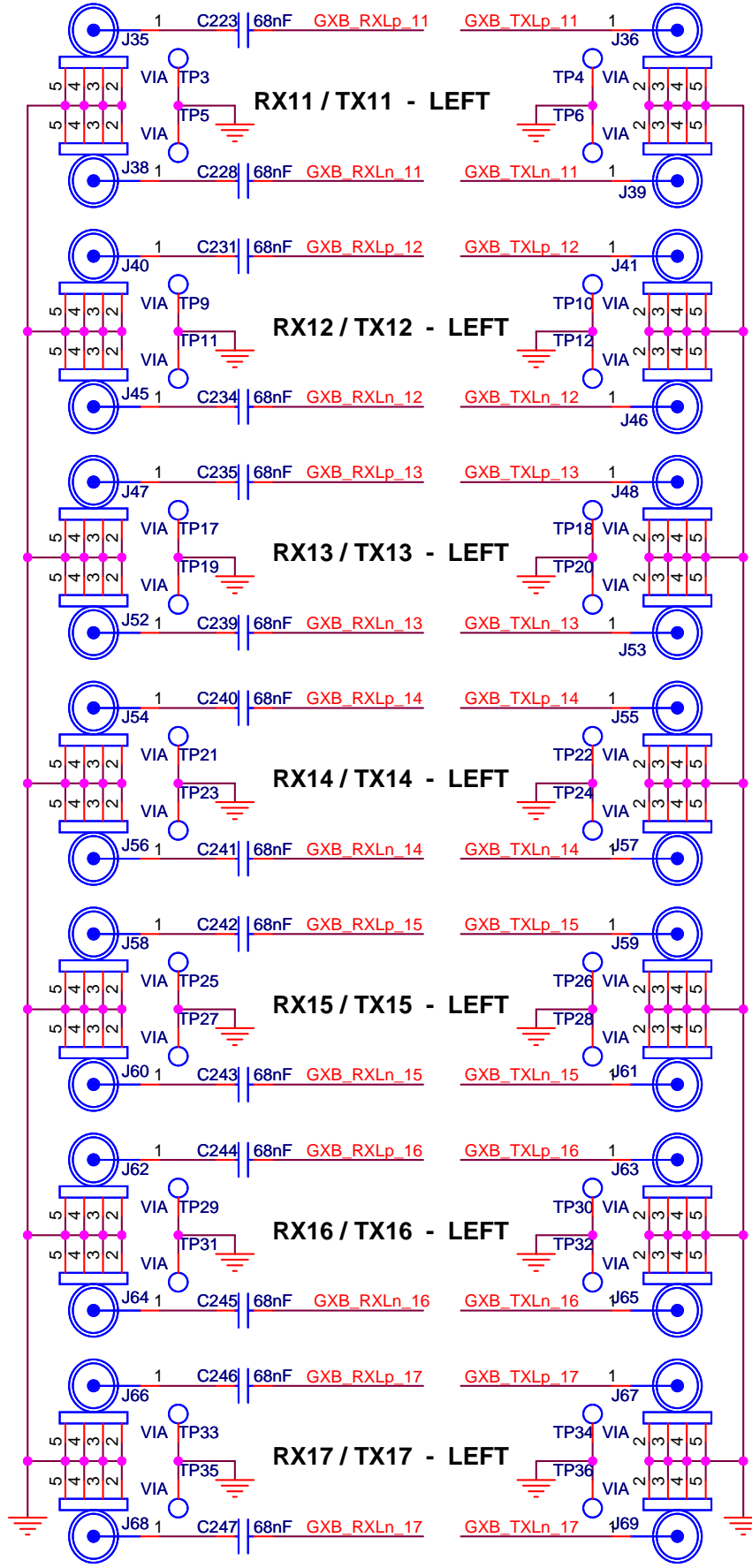
SMAs / SFP+ Interface



SFPA_MOD2_SDA	R192	4.7K
SFPA_MOD1_SCL	R193	4.7K
SFPA_MOD0_PRSNTn	R194	4.7K
SFPA_RATESEL1	R195	4.7K
SFPA_RATESEL0	R196	4.7K
SFPA_TXFAULT	R197	4.7K
SFPA_LOS	R198	4.7K

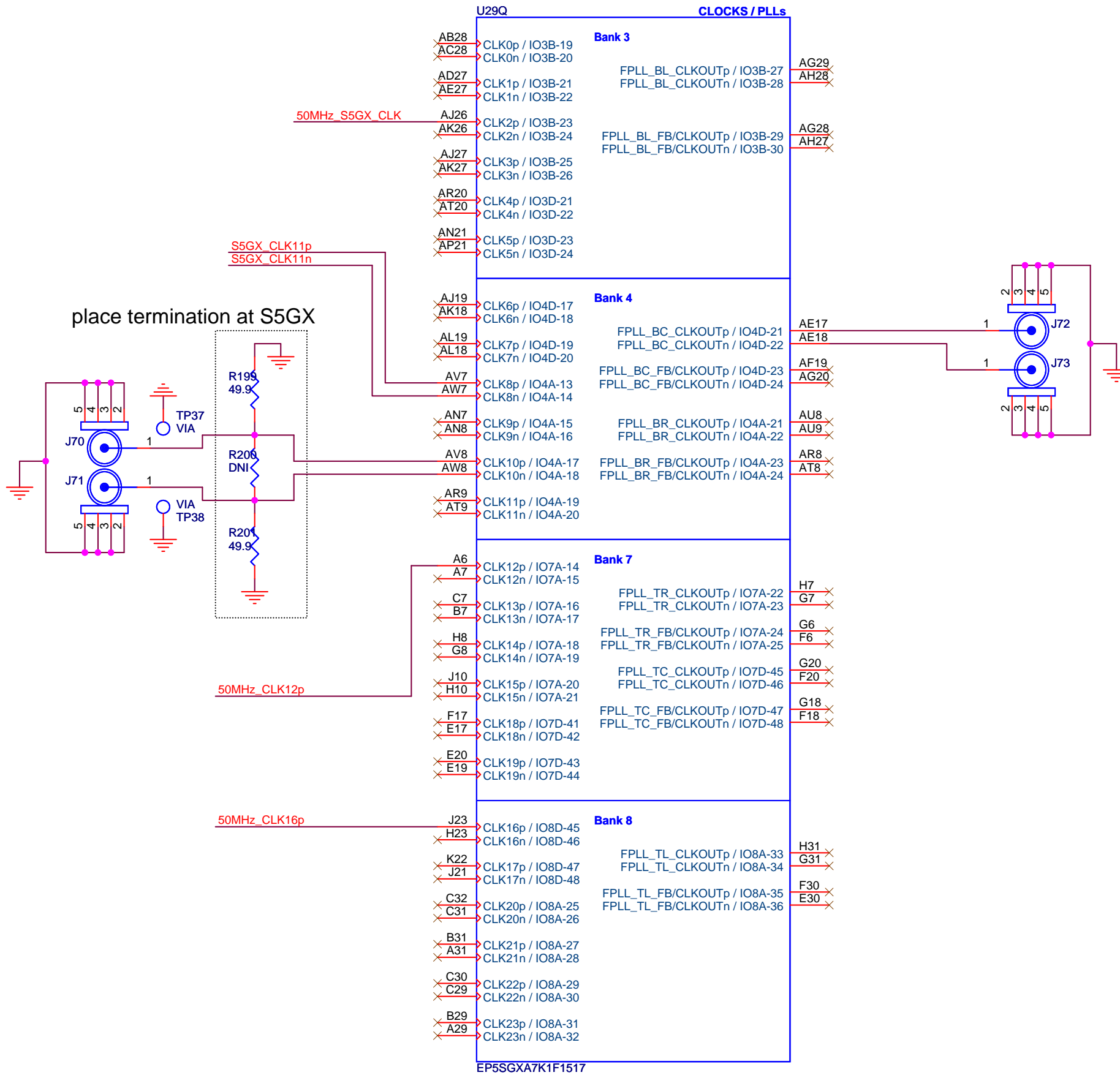


- NOTE 1: 1uH ferrite bead should provide a real impedance of 220-ohms at 100MHz
- NOTE 2: Bypass Capacitors should be placed as close to the 20-pin connector as possible
- NOTE 3: Assuming that the Stratix V GX board shares a common 3.3 volt power plane that the open drain IO pins can be pulled-up on. This assumption is made to simplify such that the Tx_Fault and Rx_LOS signals do not need to be pulled-up by the Protocol IC (Stratix IV GX) as specified in the MultiSource Agreement (MSA).
- NOTE 4: Assuming that the 100-ohm termination on the Stratix V GX device will be implemented via the on-chip termination circuit.
- NOTE 5: Going to use the SPLC-20 SFP Optical SONET OC-48 transceiver, but not limited to this. Any MSA SFP compliant transceiver should be able to be plugged in.



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GLOBAL CLOCKS



50MHz_CLK12p	50MHz_CLK12p	23
50MHz_CLK16p	50MHz_CLK16p	23
50MHz_S5GX_CLK	50MHz_S5GX_CLK	23
S5GX_CLK11p	S5GX_CLK11p	23
S5GX_CLK11n	S5GX_CLK11n	23



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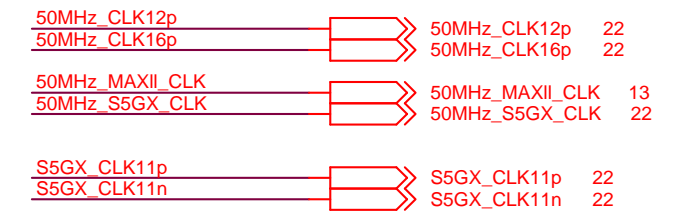
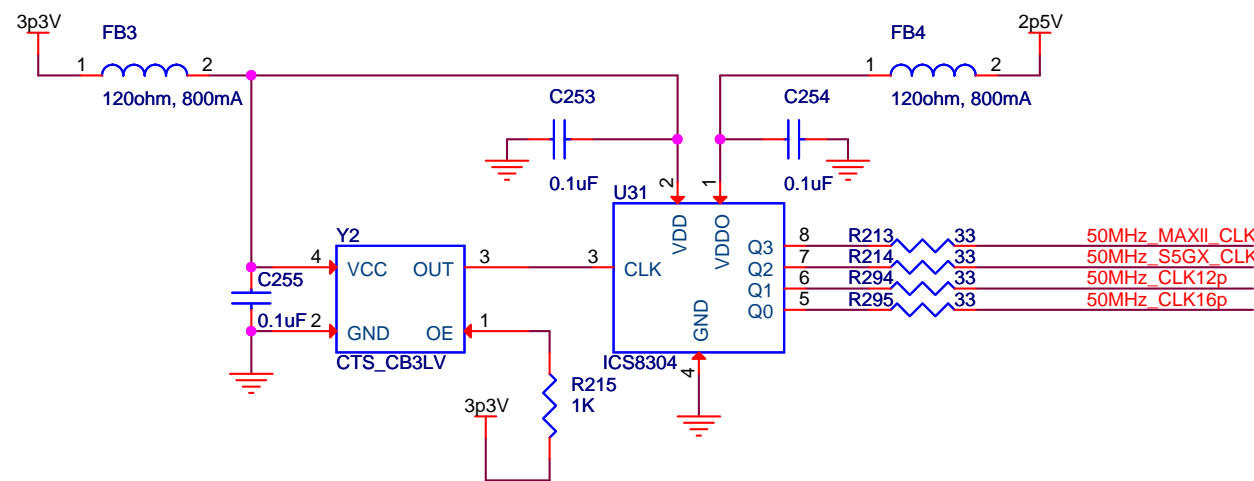
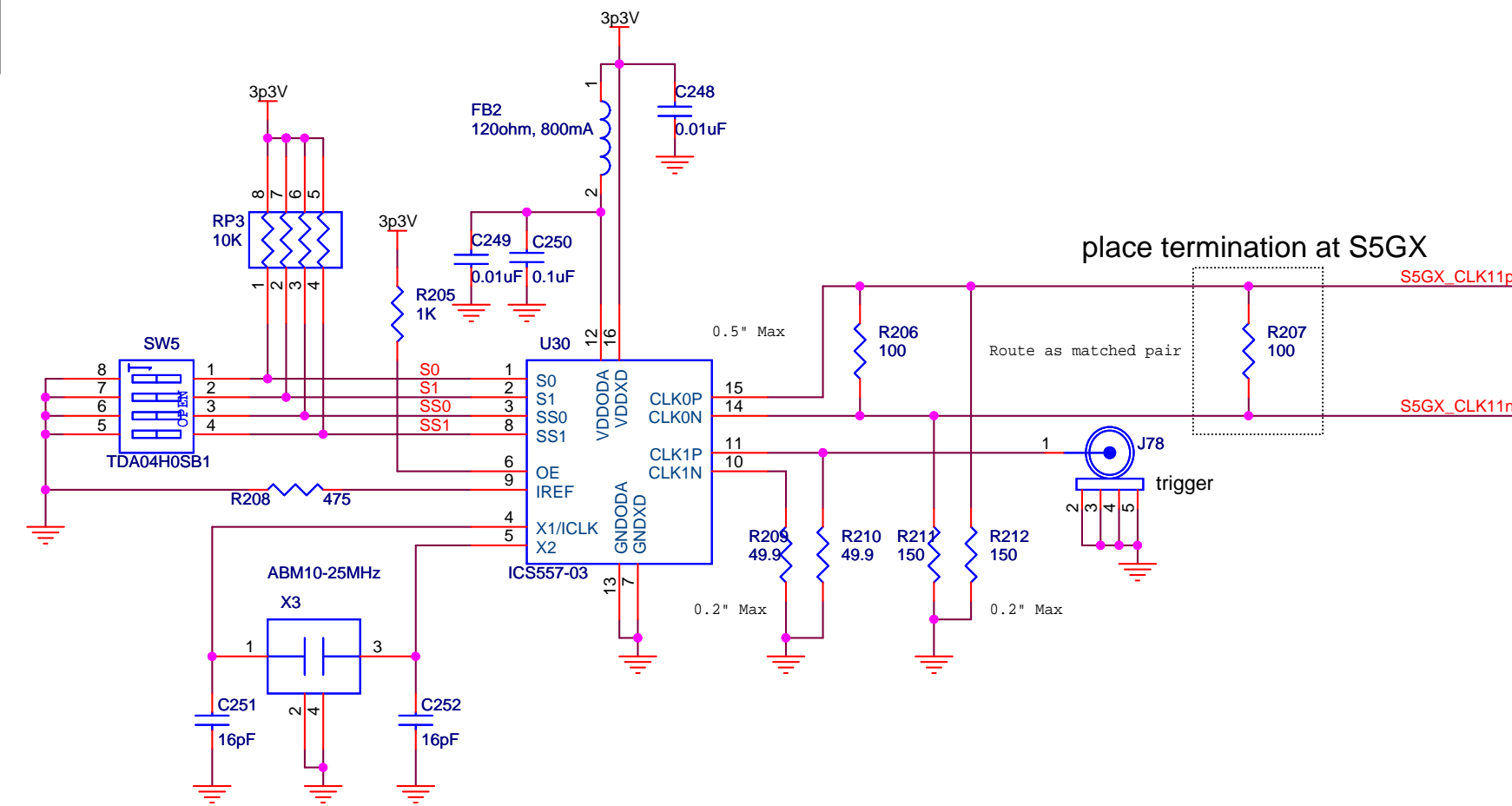
Spread Spectrum / 50MHz Clocks

Output Select Table 1(MHz)

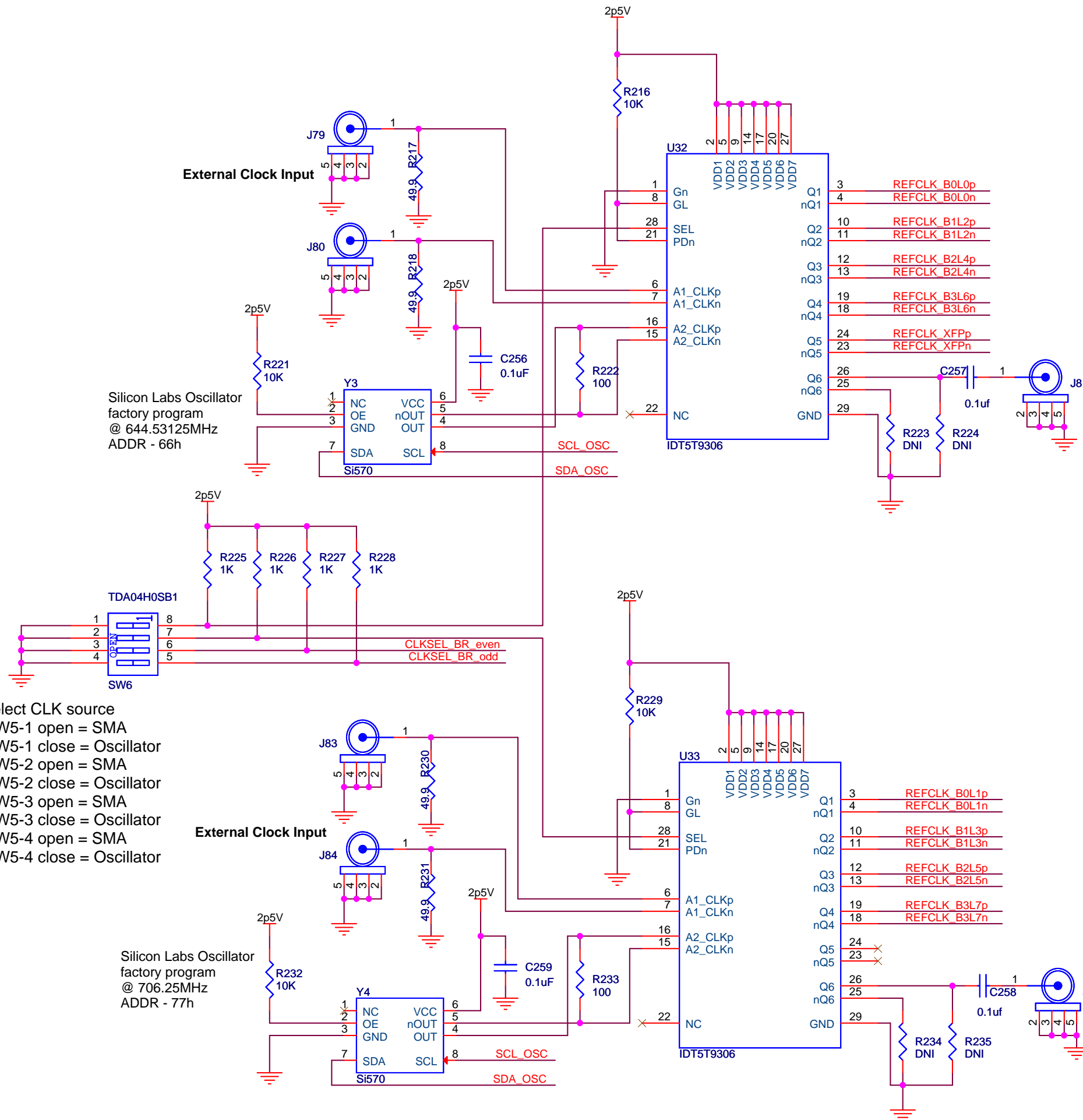
S1	S0	CLK(1:0), CLK(1:0)
0	0	25M
0	1	100M
1	0	125M
1	1	200M

Spread Selection Table 2

SS1	SS0	Spread %
0	0	Center ± 0.25
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread



XCVR Clocks - Left Blocks

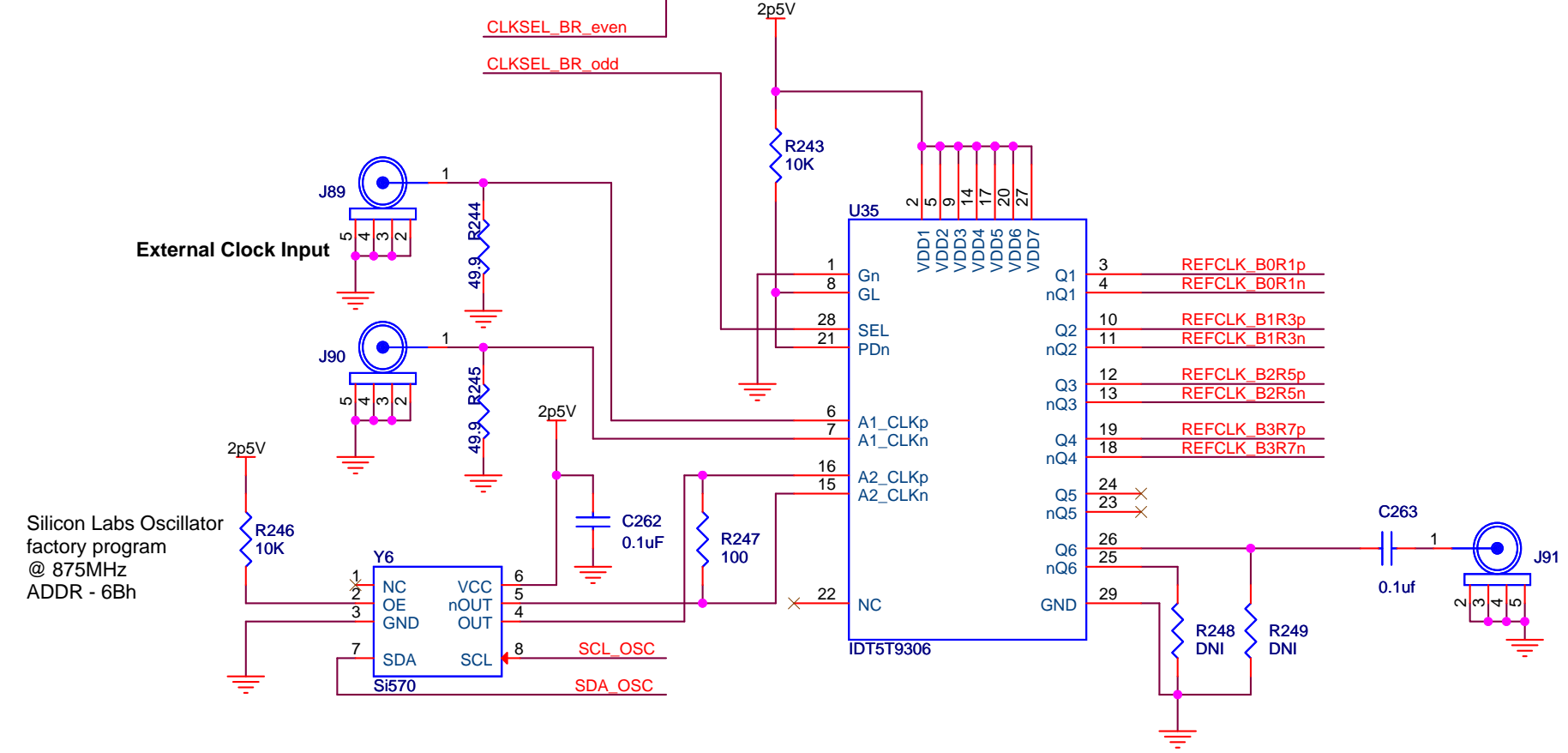
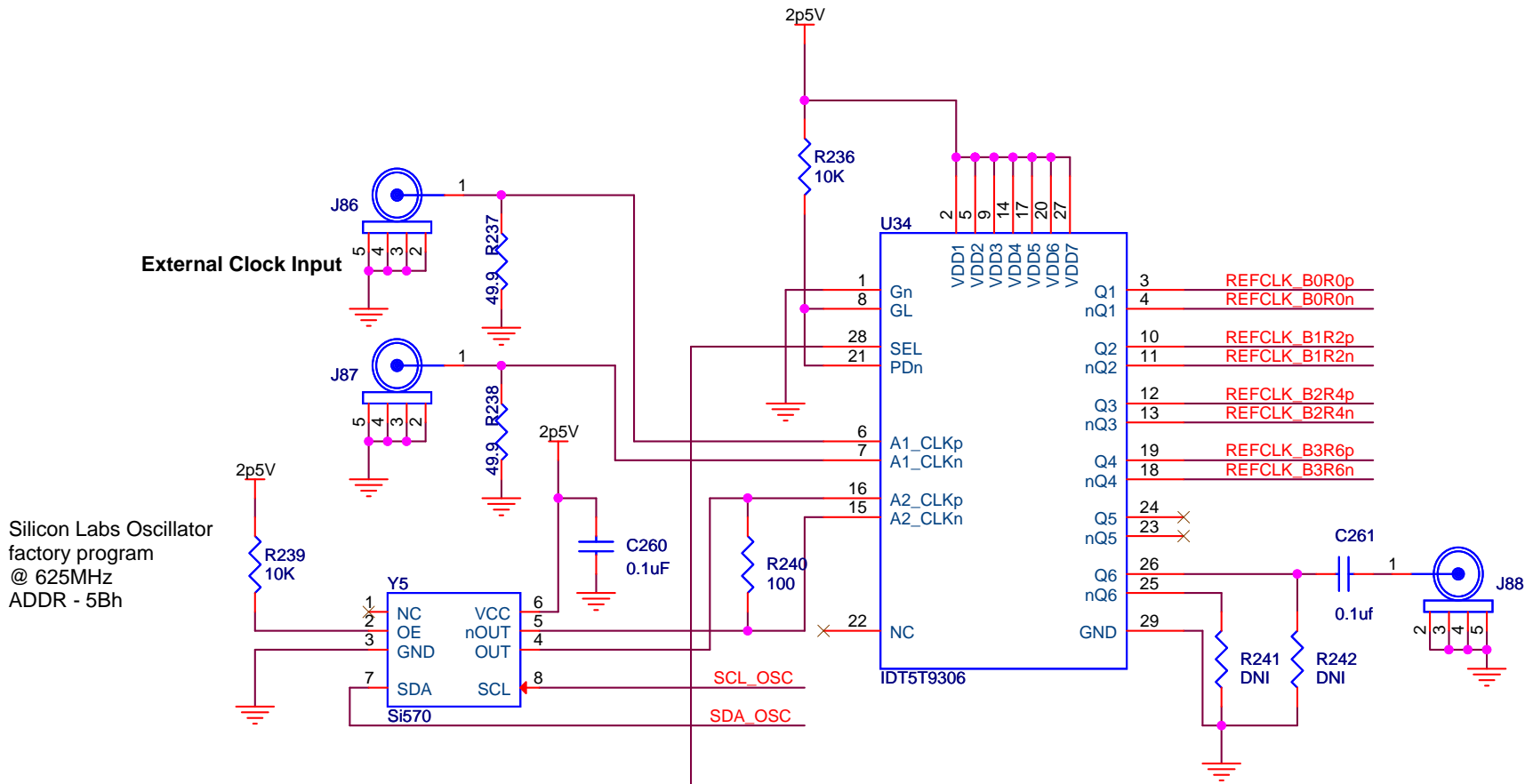


select CLK source
 SW5-1 open = SMA
 SW5-1 close = Oscillator
 SW5-2 open = SMA
 SW5-2 close = Oscillator
 SW5-3 open = SMA
 SW5-3 close = Oscillator
 SW5-4 open = SMA
 SW5-4 close = Oscillator

CLKSEL_BR_even	CLKSEL_BR_even	25
CLKSEL_BR_odd	CLKSEL_BR_odd	25
SCL_OSC	SCL_OSC	13,25
SDA_OSC	SDA_OSC	13,25
REFCLK_B0L0p	REFCLK_B0L0p	31
REFCLK_B0L0n	REFCLK_B0L0n	31
REFCLK_B1L2p	REFCLK_B1L2p	31
REFCLK_B1L2n	REFCLK_B1L2n	31
REFCLK_B2L4p	REFCLK_B2L4p	32
REFCLK_B2L4n	REFCLK_B2L4n	32
REFCLK_B3L6p	REFCLK_B3L6p	32
REFCLK_B3L6n	REFCLK_B3L6n	32
REFCLK_B0L1p	REFCLK_B0L1p	31
REFCLK_B0L1n	REFCLK_B0L1n	31
REFCLK_B1L3p	REFCLK_B1L3p	31
REFCLK_B1L3n	REFCLK_B1L3n	31
REFCLK_B2L5p	REFCLK_B2L5p	32
REFCLK_B2L5n	REFCLK_B2L5n	32
REFCLK_B3L7p	REFCLK_B3L7p	32
REFCLK_B3L7n	REFCLK_B3L7n	32
REFCLK_XFPp	REFCLK_XFPp	20
REFCLK_XFPn	REFCLK_XFPn	20



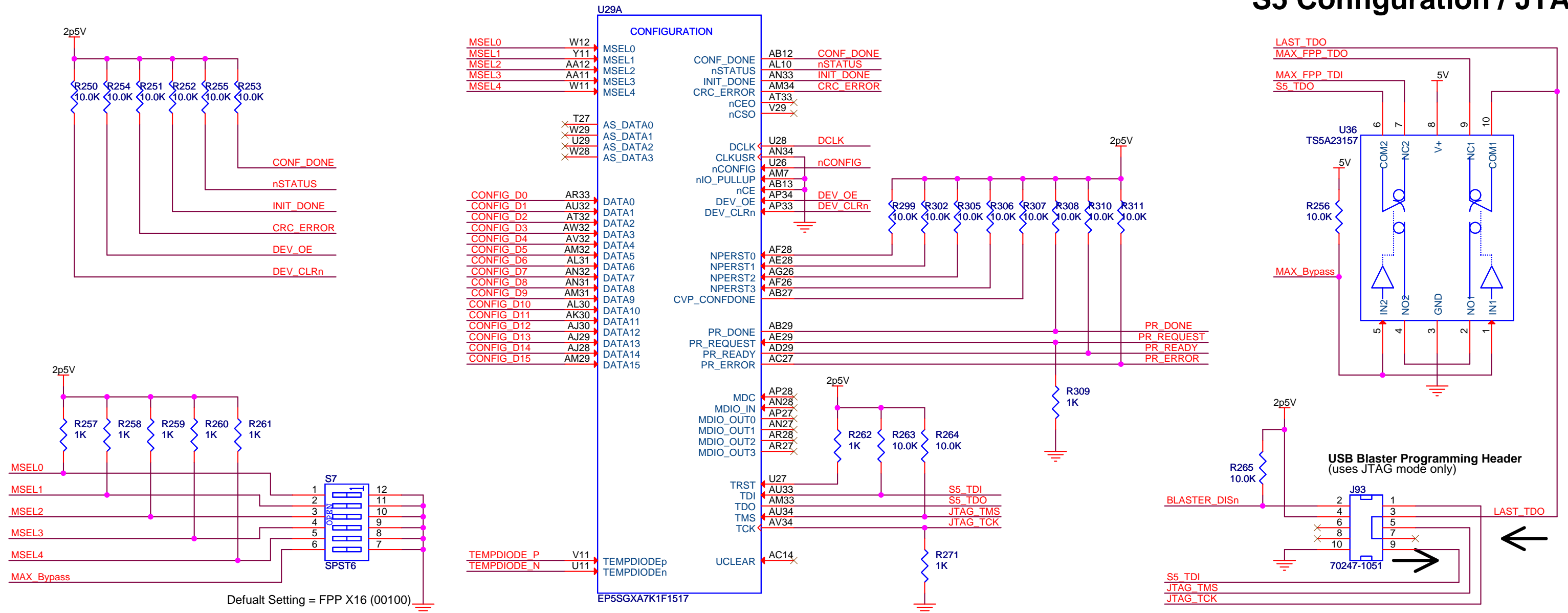
XCVR Clocks - Right Blocks



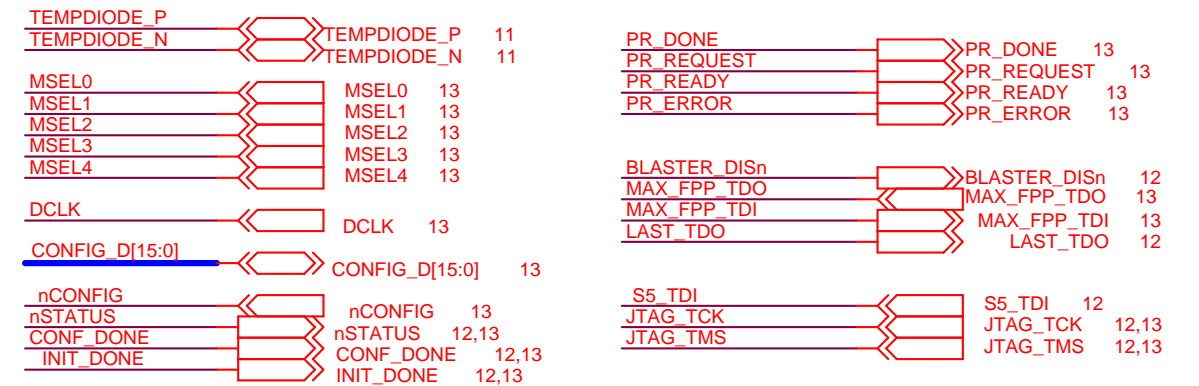
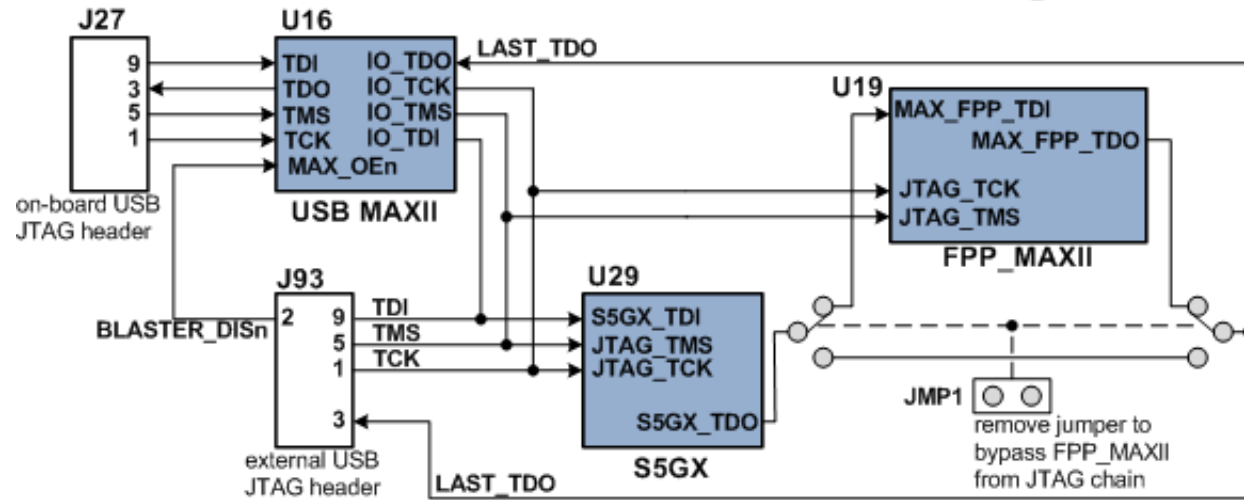
CLKSEL_BR_even	CLKSEL_BR_even	24
CLKSEL_BR_odd	CLKSEL_BR_odd	24
SCL_OSC	SCL_OSC	13,24
SDA_OSC	SDA_OSC	13,24
REFCLK_B0R0p	REFCLK_B0R0p	33
REFCLK_B0R0n	REFCLK_B0R0n	33
REFCLK_B1R2p	REFCLK_B1R2p	33
REFCLK_B1R2n	REFCLK_B1R2n	33
REFCLK_B2R4p	REFCLK_B2R4p	34
REFCLK_B2R4n	REFCLK_B2R4n	34
REFCLK_B3R6p	REFCLK_B3R6p	34
REFCLK_B3R6n	REFCLK_B3R6n	34
REFCLK_B0R1p	REFCLK_B0R1p	33
REFCLK_B0R1n	REFCLK_B0R1n	33
REFCLK_B1R3p	REFCLK_B1R3p	33
REFCLK_B1R3n	REFCLK_B1R3n	33
REFCLK_B2R5p	REFCLK_B2R5p	34
REFCLK_B2R5n	REFCLK_B2R5n	34
REFCLK_B3R7p	REFCLK_B3R7p	34
REFCLK_B3R7n	REFCLK_B3R7n	34



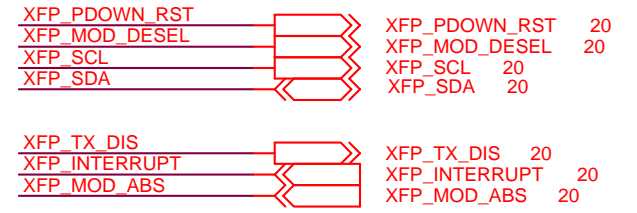
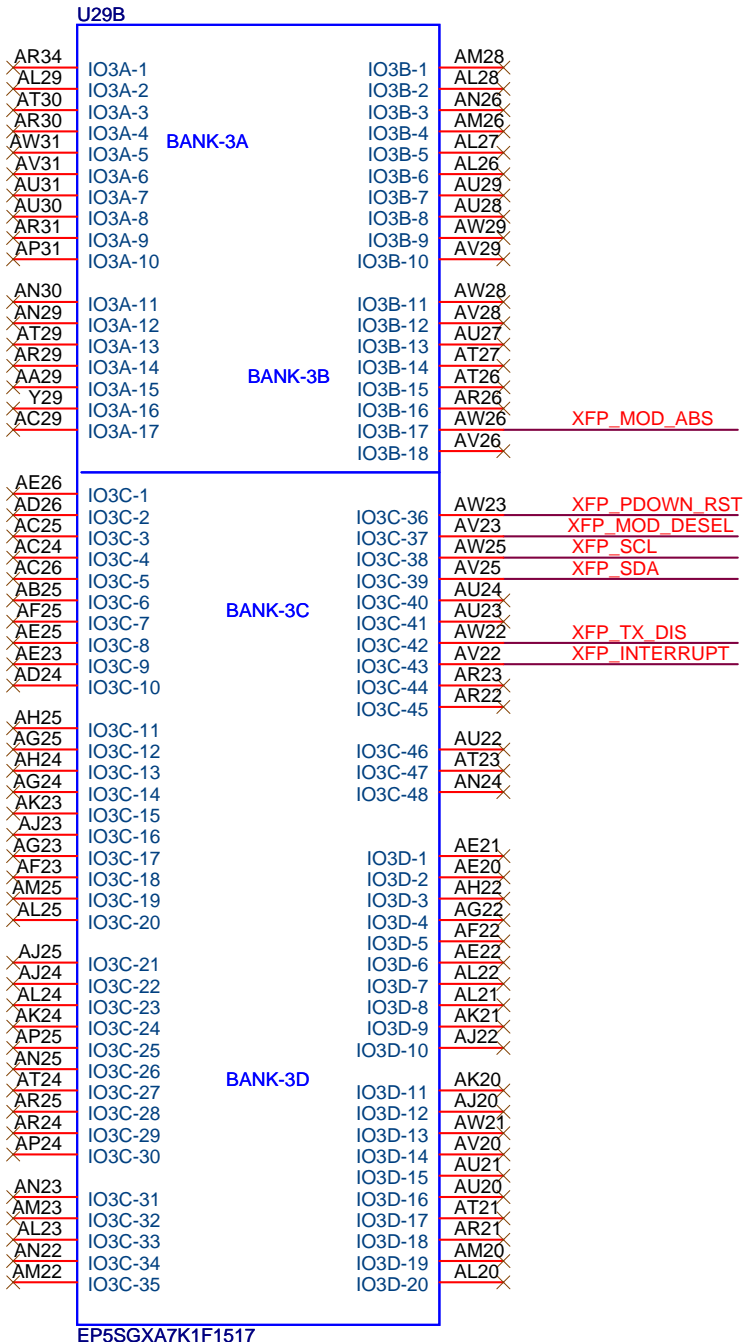
S5 Configuration / JTAG



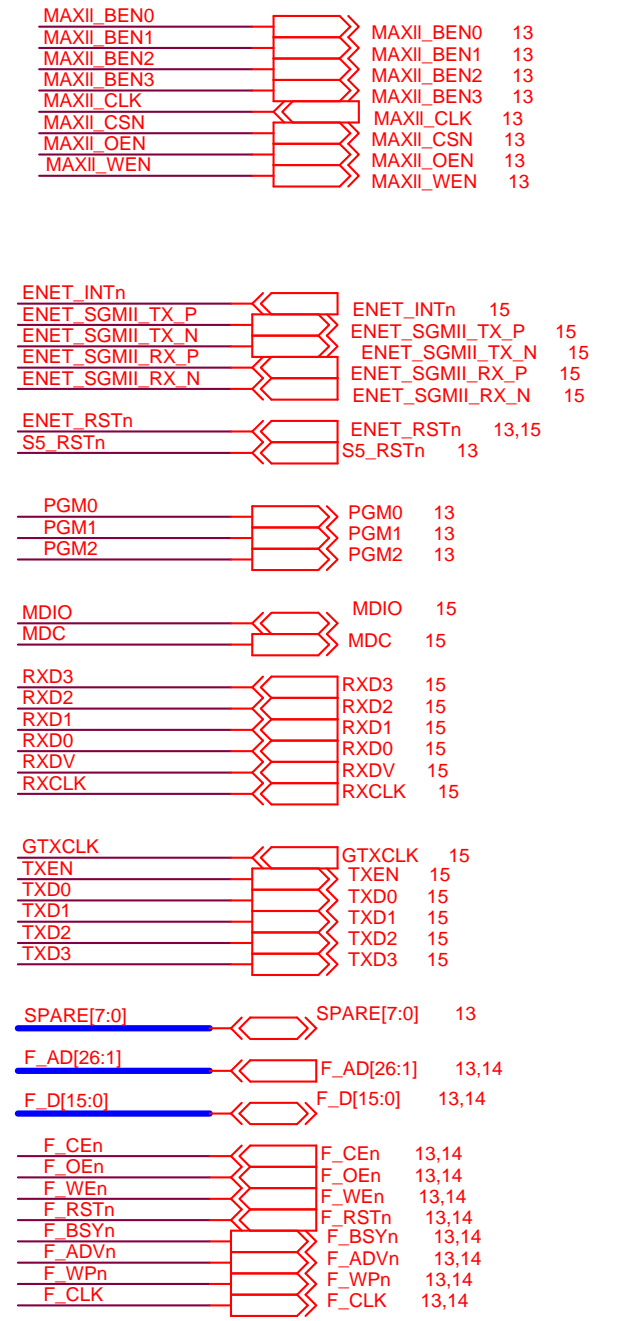
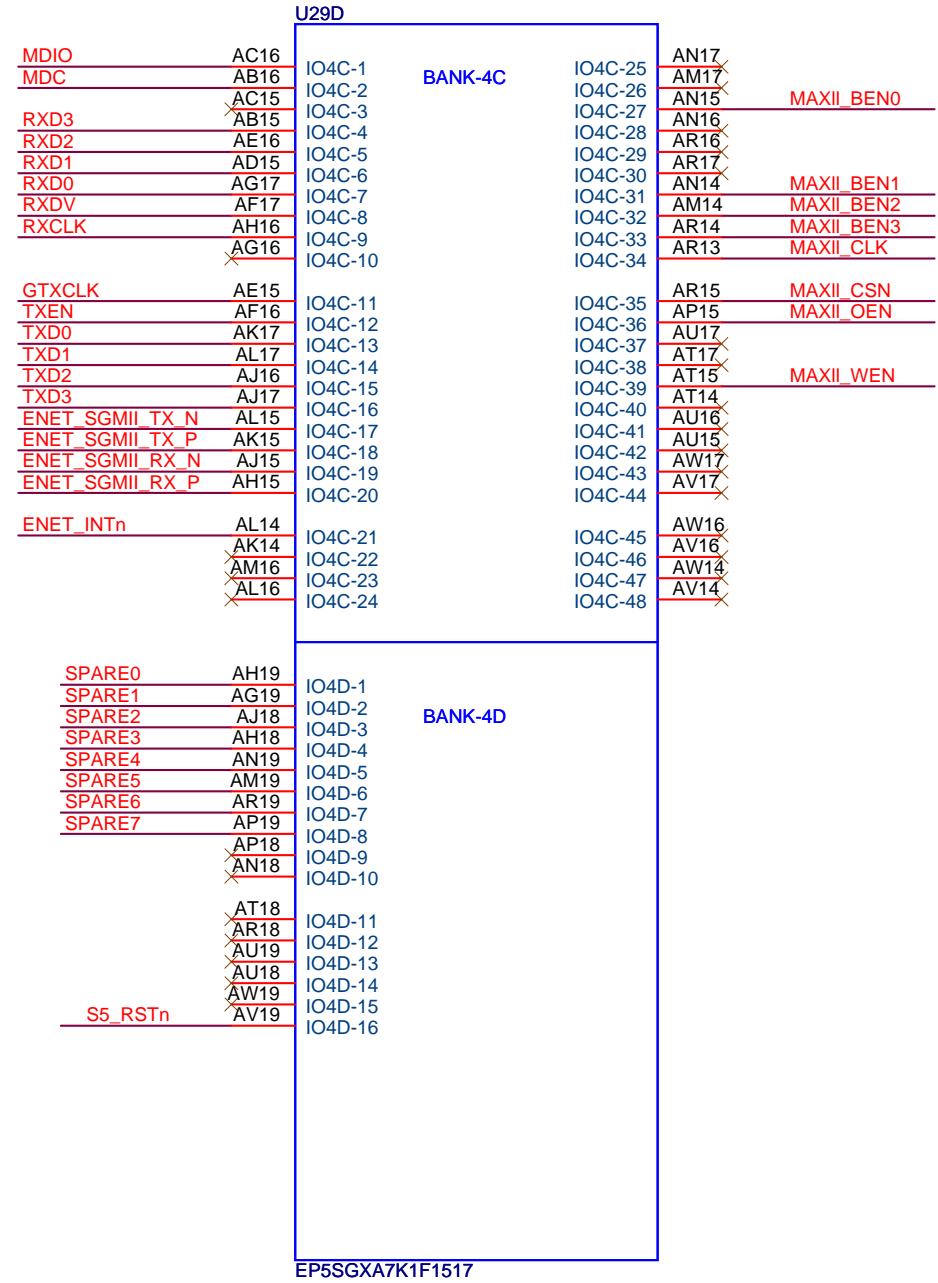
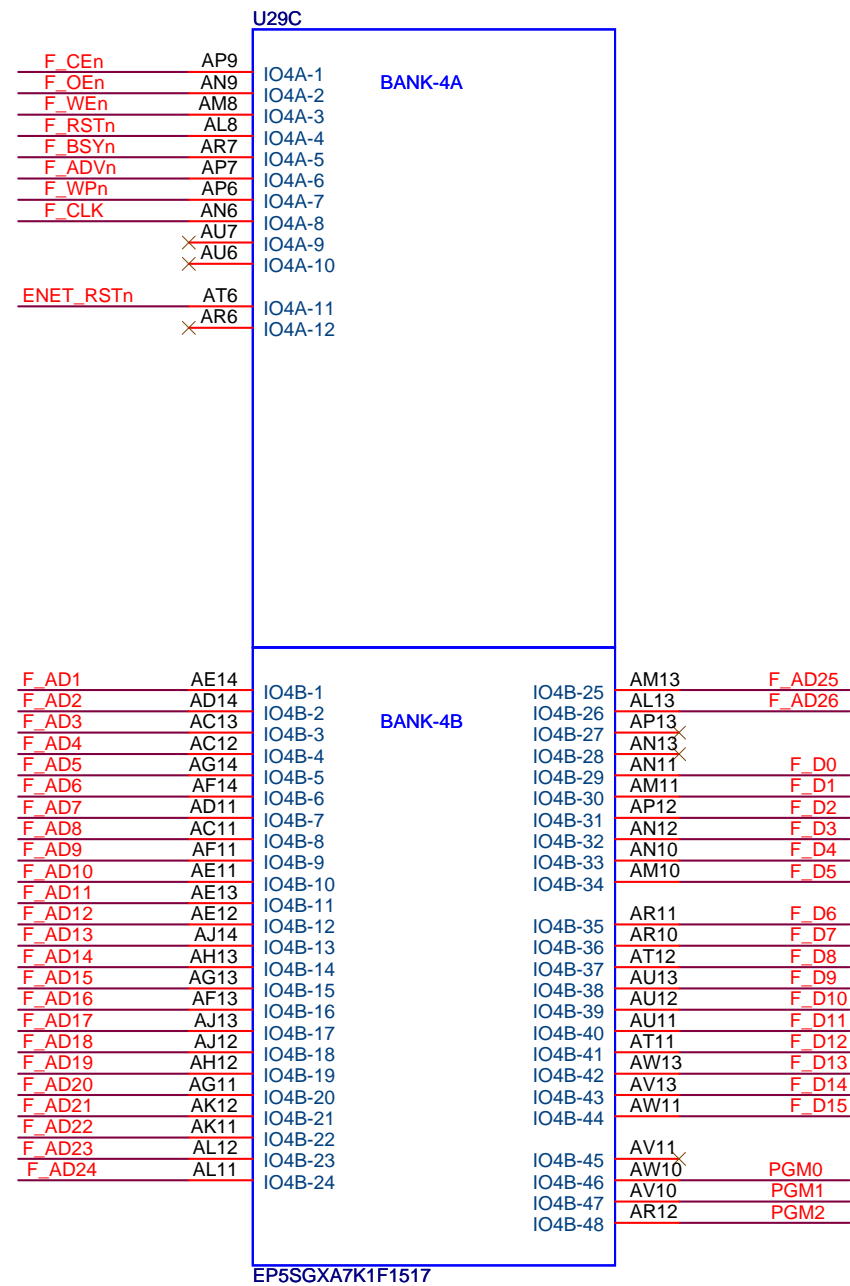
JTAG Chain Block Diagram

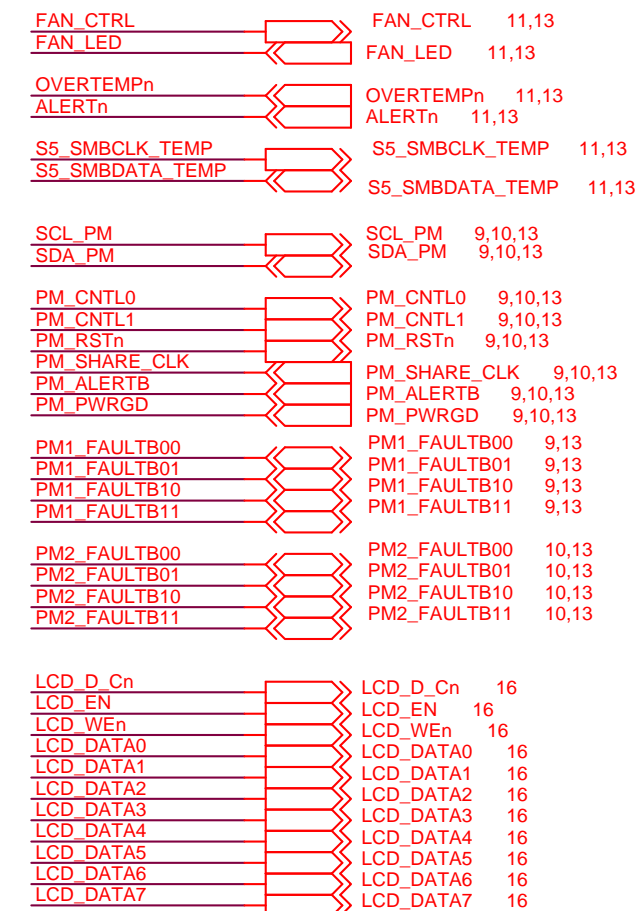
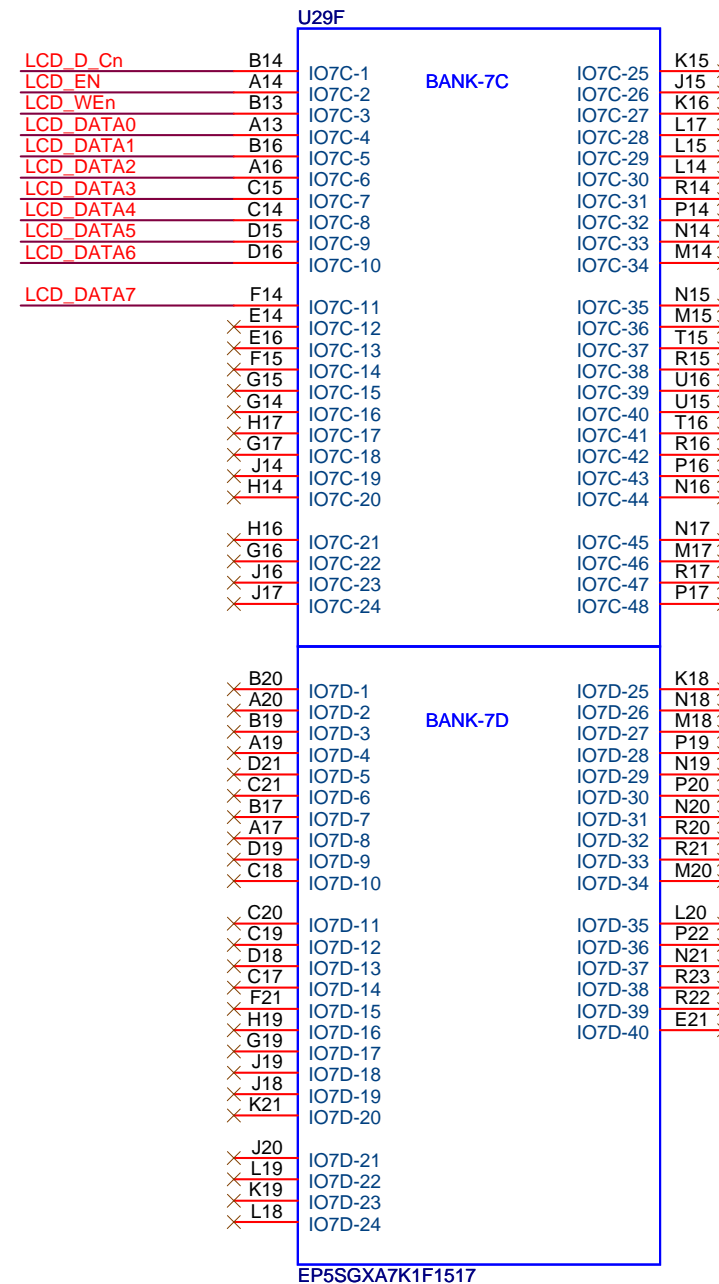
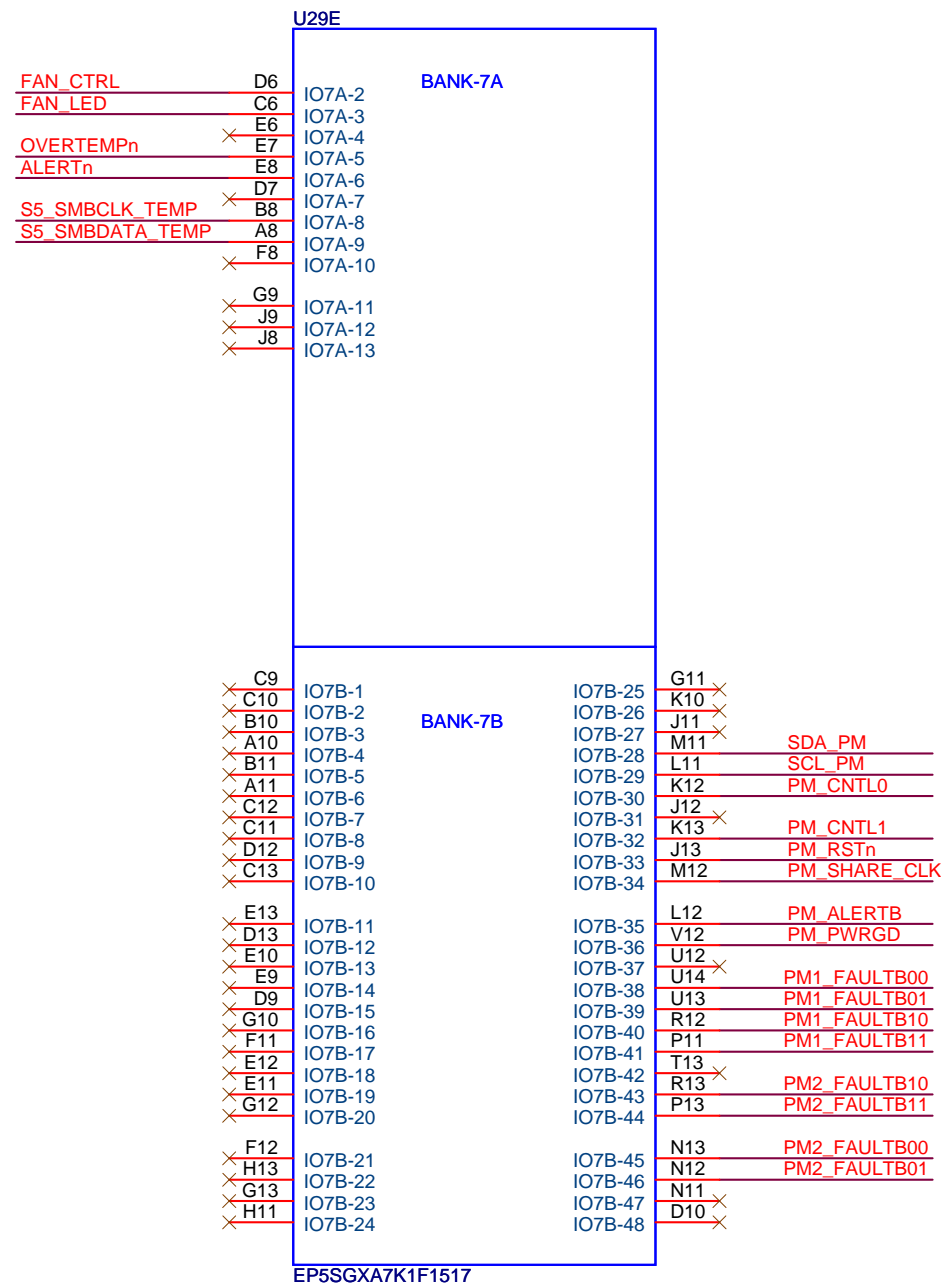


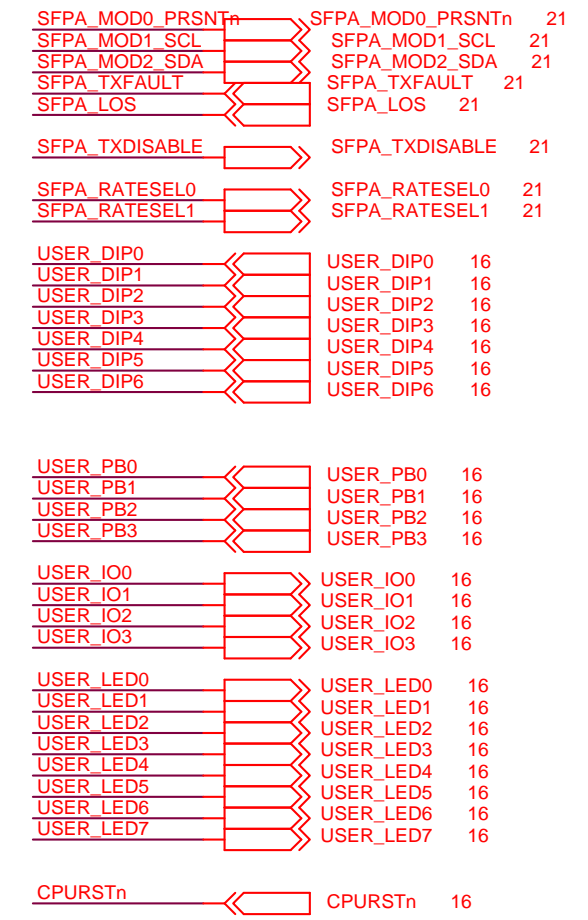
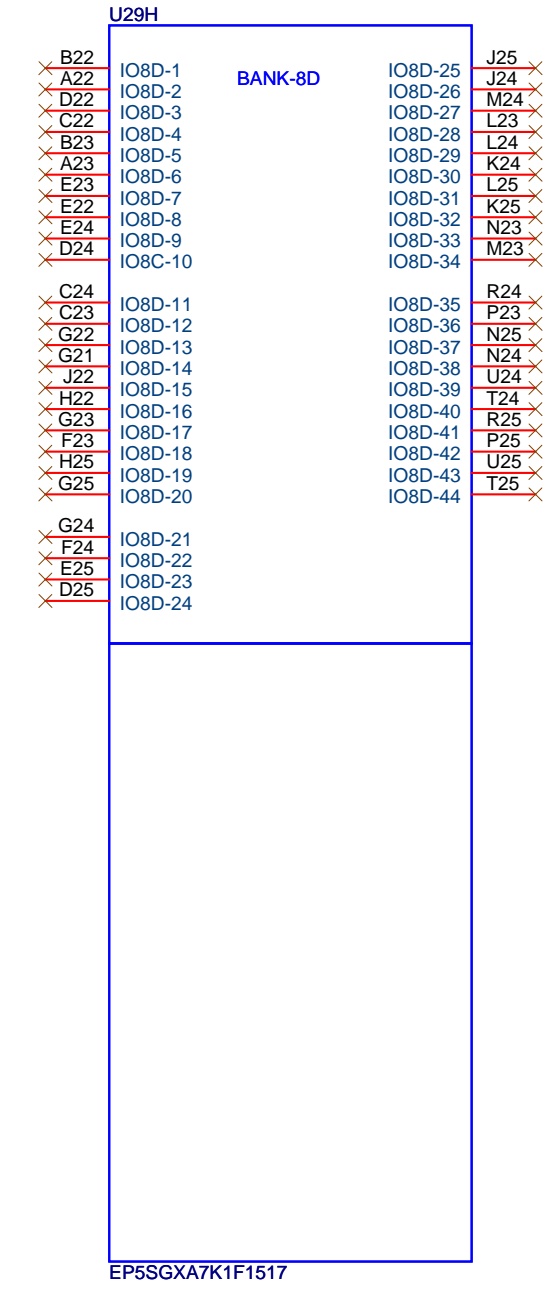
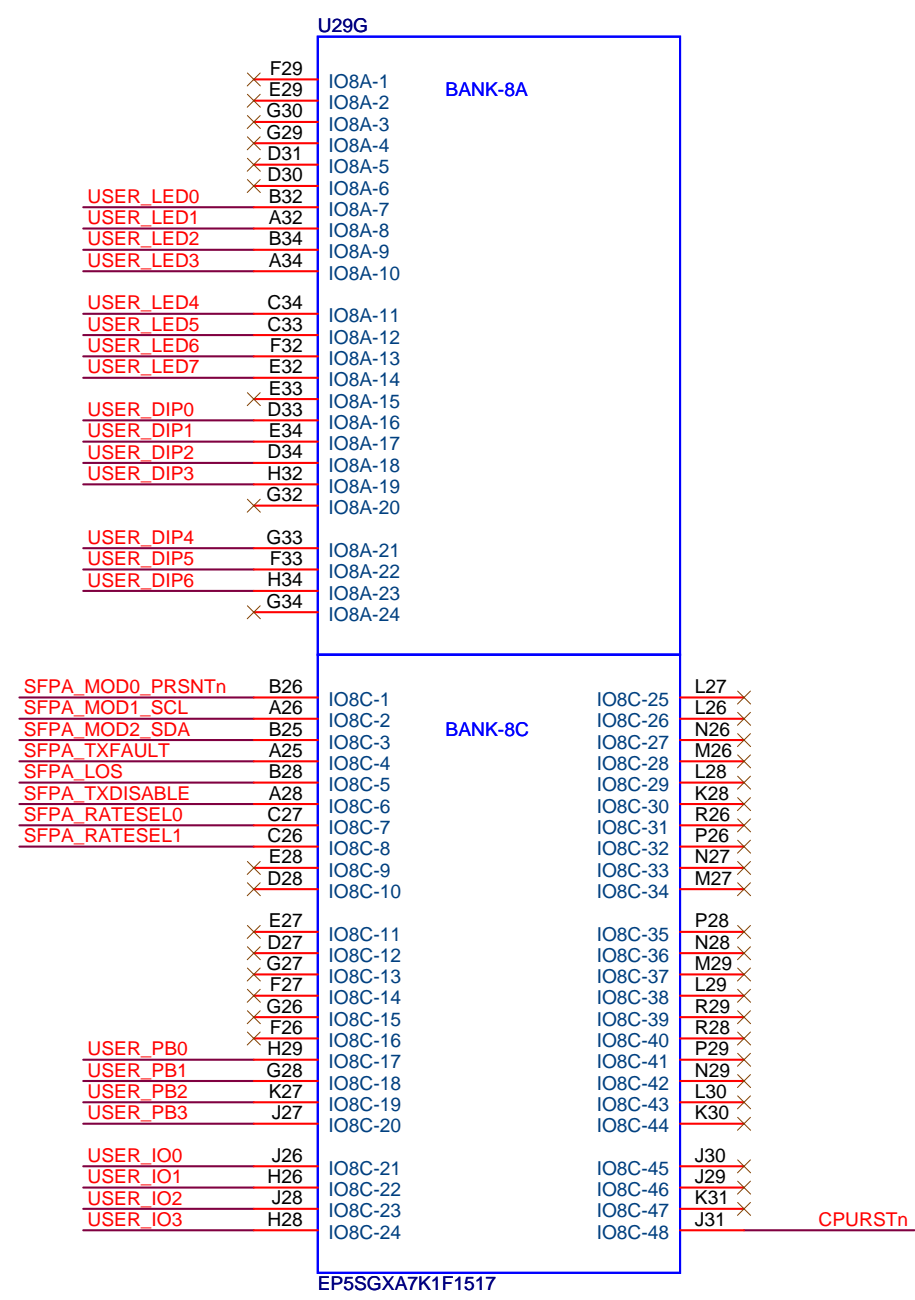
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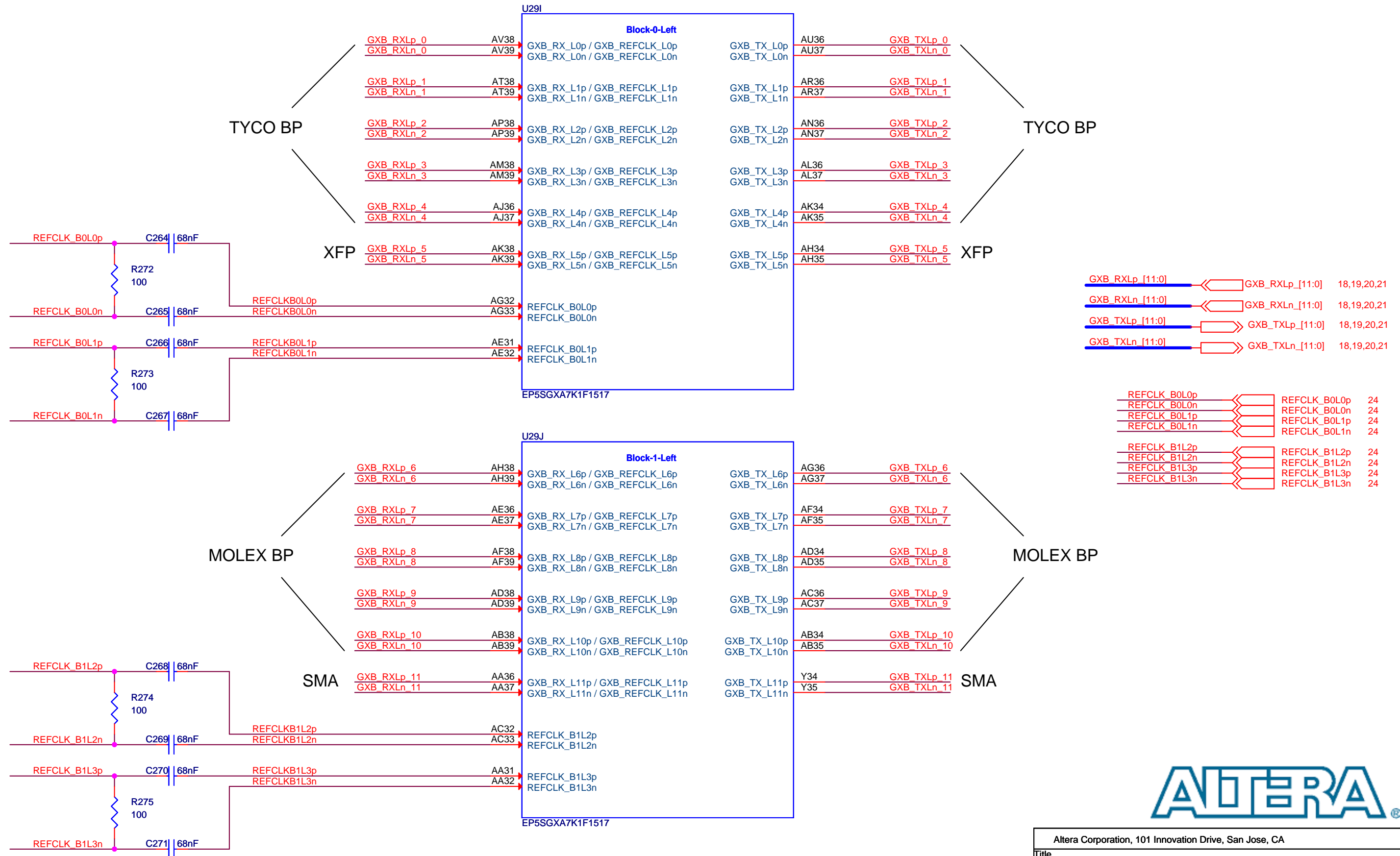
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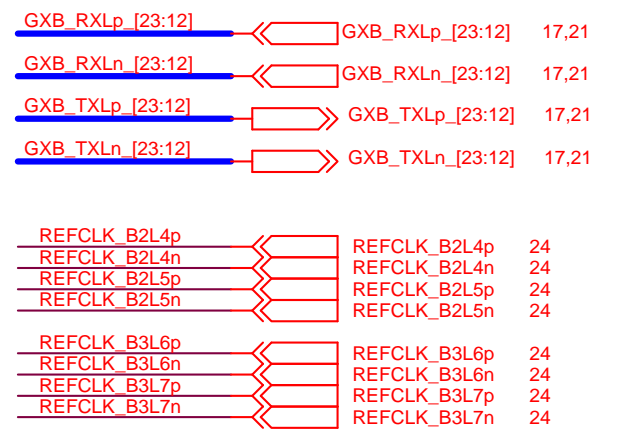
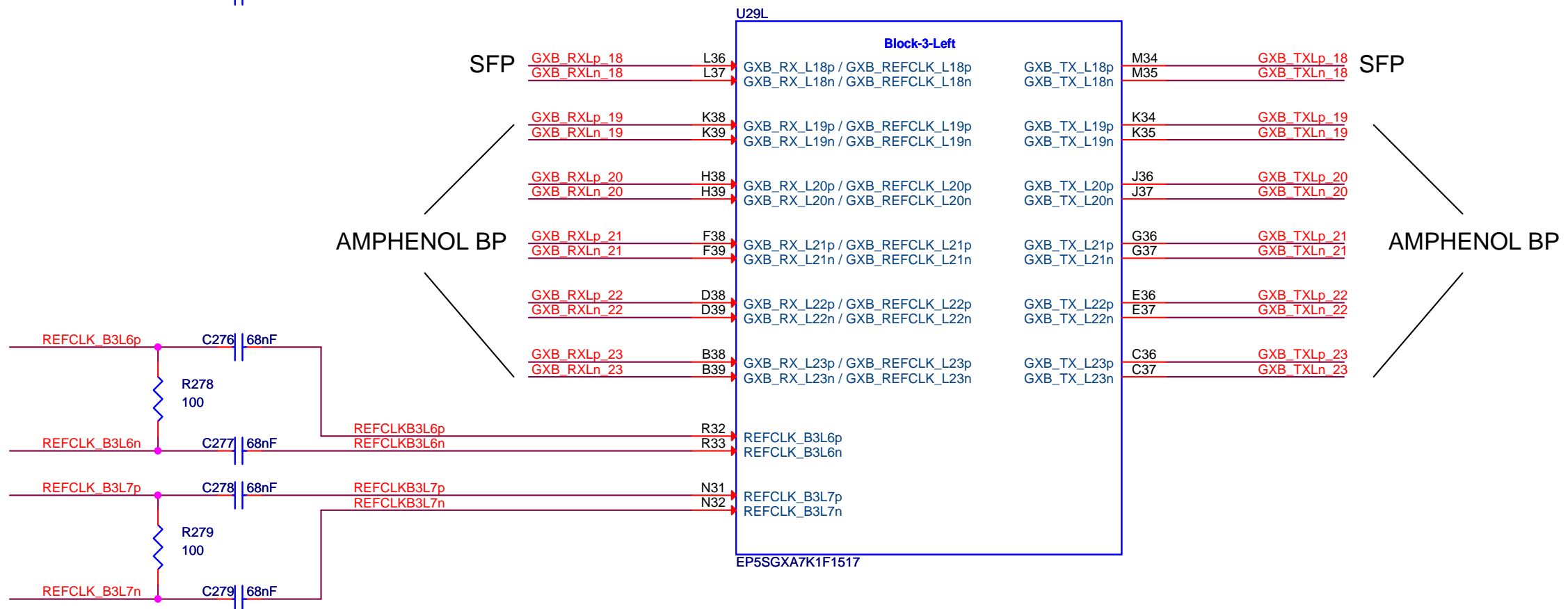
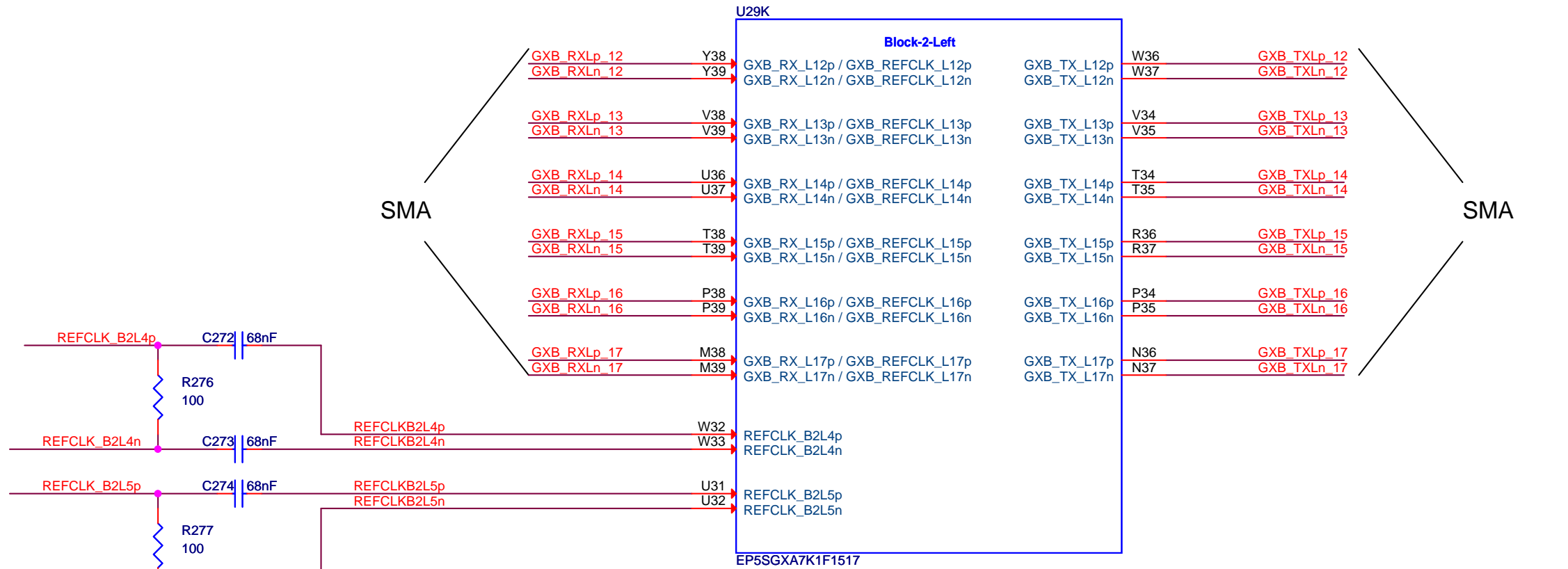




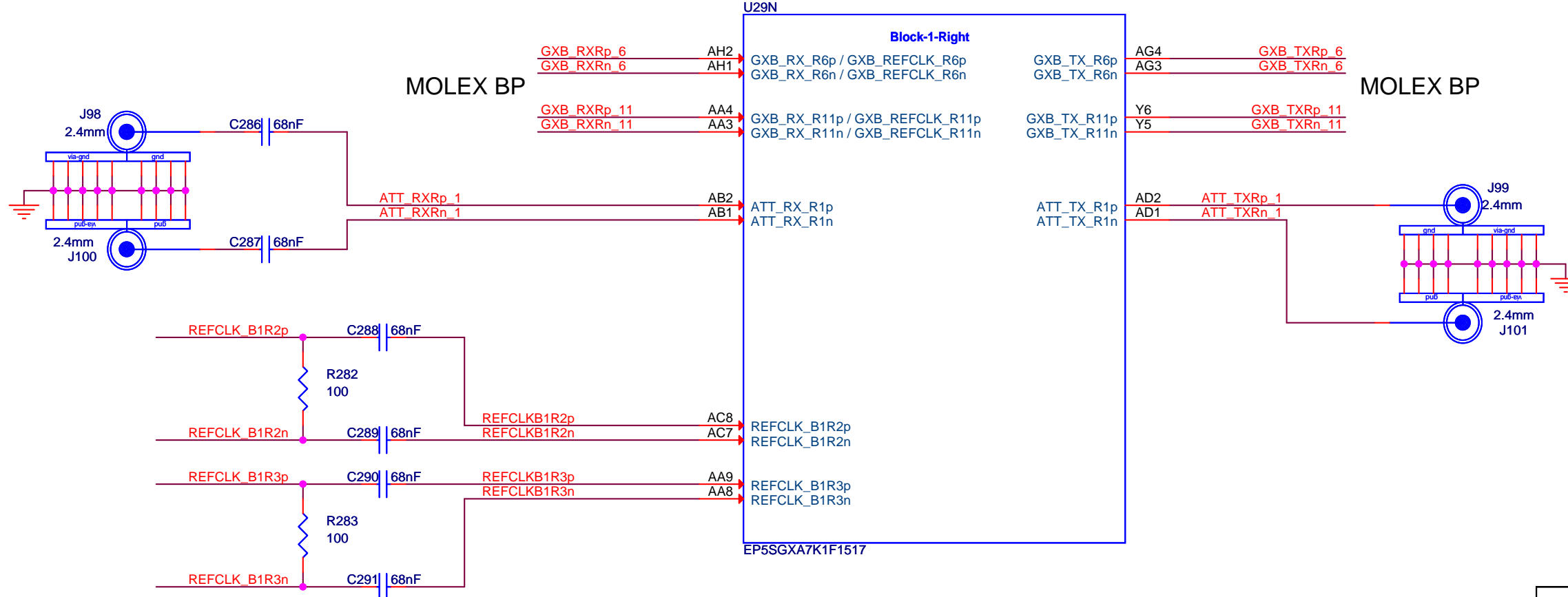
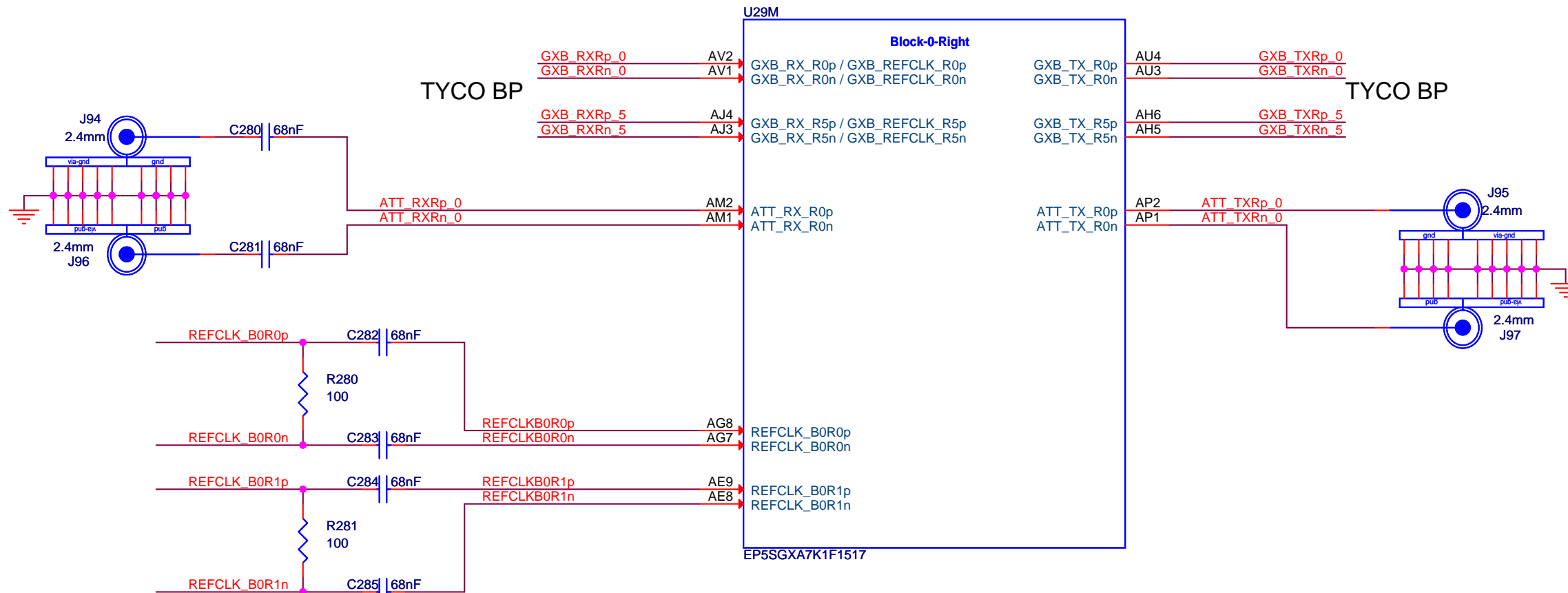
XCVR Left Blocks 0/1



XCVR Left Blocks 2/3



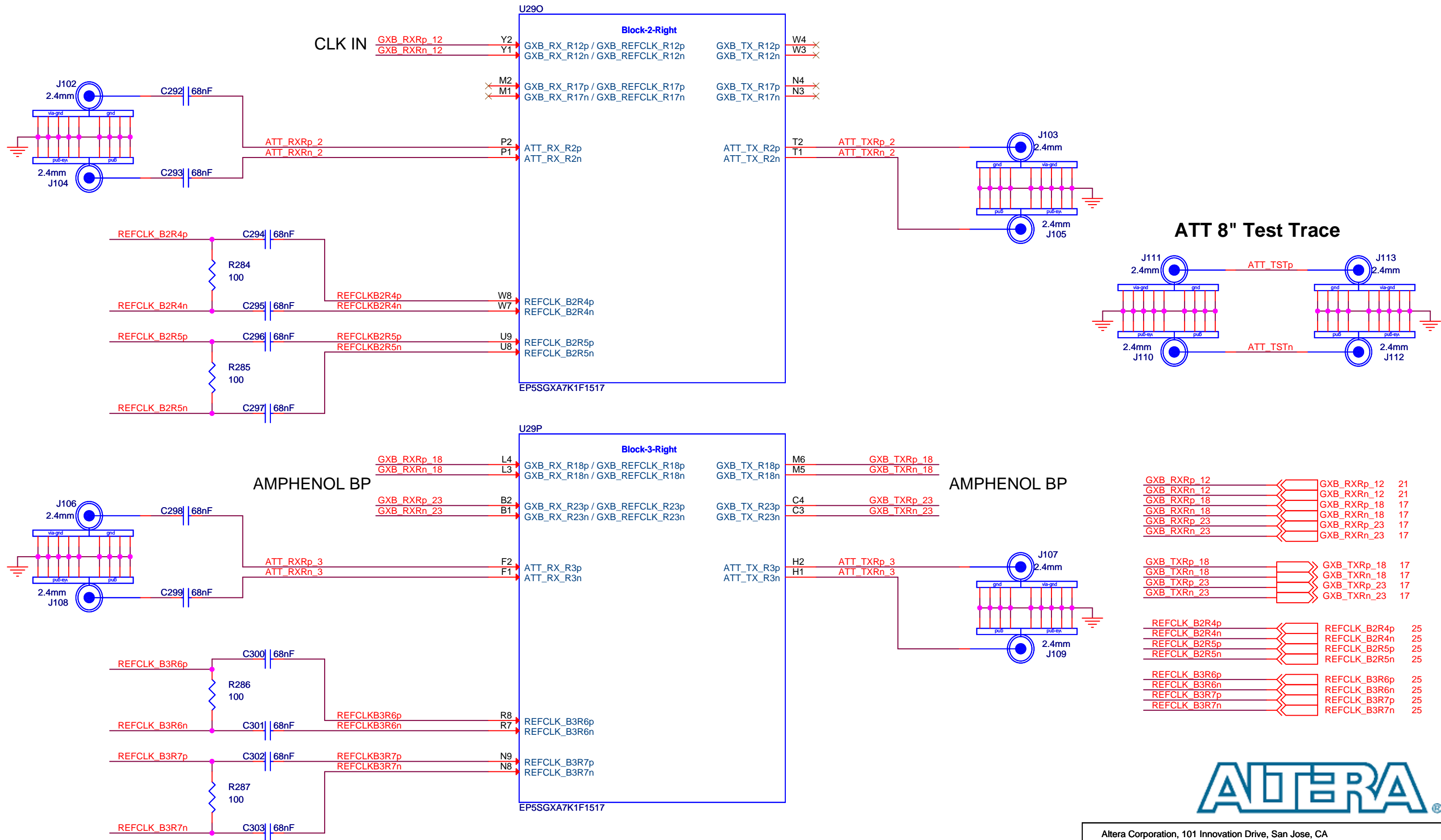
XCVR Right Blocks 0/1



GXB_RXRp_0	GXB_RXRp_0	18
GXB_RXRn_0	GXB_RXRn_0	18
GXB_RXRp_5	GXB_RXRp_5	18
GXB_RXRn_5	GXB_RXRn_5	18
GXB_RXRp_6	GXB_RXRp_6	19
GXB_RXRn_6	GXB_RXRn_6	19
GXB_RXRp_11	GXB_RXRp_11	19
GXB_RXRn_11	GXB_RXRn_11	19
GXB_TXRp_0	GXB_TXRp_0	18
GXB_TXRn_0	GXB_TXRn_0	18
GXB_TXRp_5	GXB_TXRp_5	18
GXB_TXRn_5	GXB_TXRn_5	18
GXB_TXRp_6	GXB_TXRp_6	19
GXB_TXRn_6	GXB_TXRn_6	19
GXB_TXRp_11	GXB_TXRp_11	19
GXB_TXRn_11	GXB_TXRn_11	19
REFCLK_B0R0p	REFCLK_B0R0p	25
REFCLK_B0R0n	REFCLK_B0R0n	25
REFCLK_B0R1p	REFCLK_B0R1p	25
REFCLK_B0R1n	REFCLK_B0R1n	25
REFCLK_B1R2p	REFCLK_B1R2p	25
REFCLK_B1R2n	REFCLK_B1R2n	25
REFCLK_B1R3p	REFCLK_B1R3p	25
REFCLK_B1R3n	REFCLK_B1R3n	25



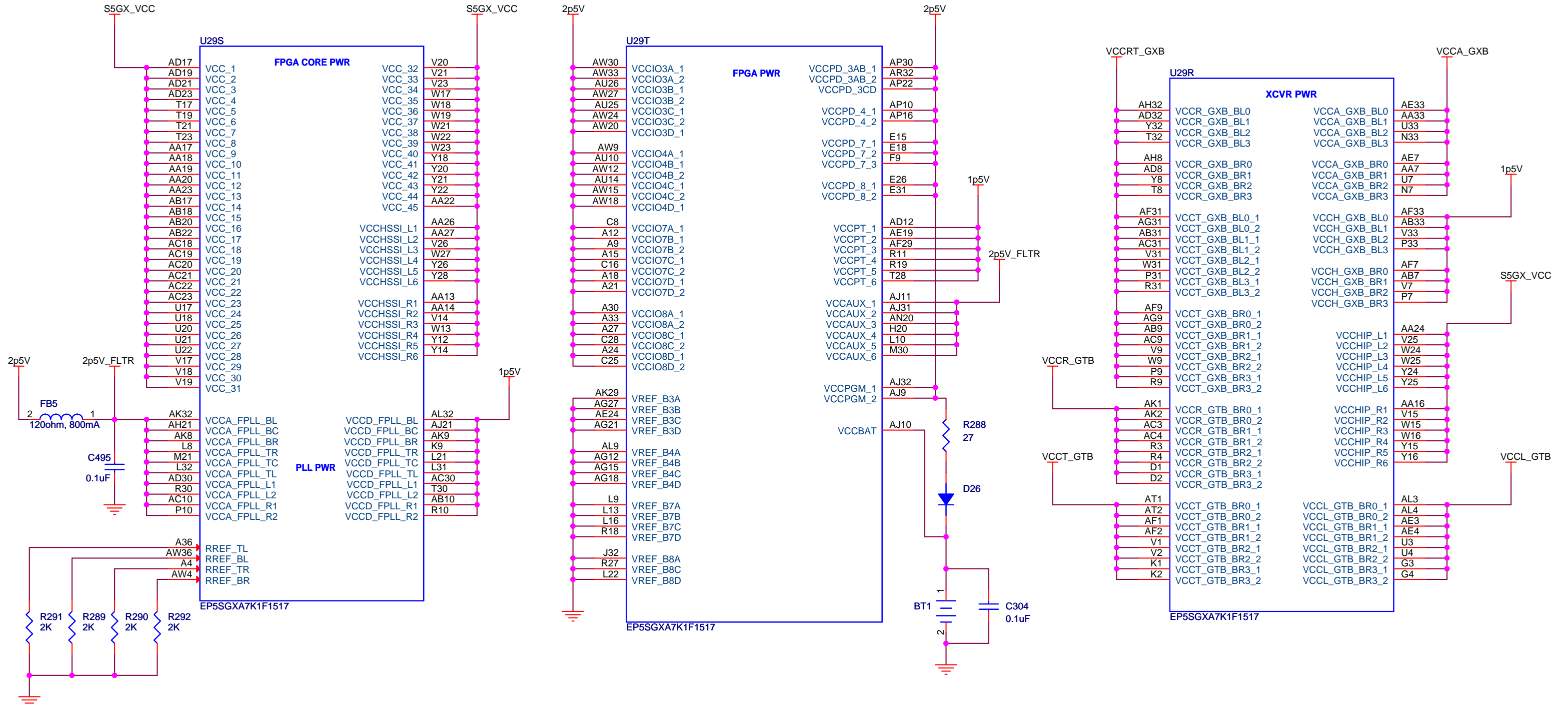
XCVR Right Blocks 2/3



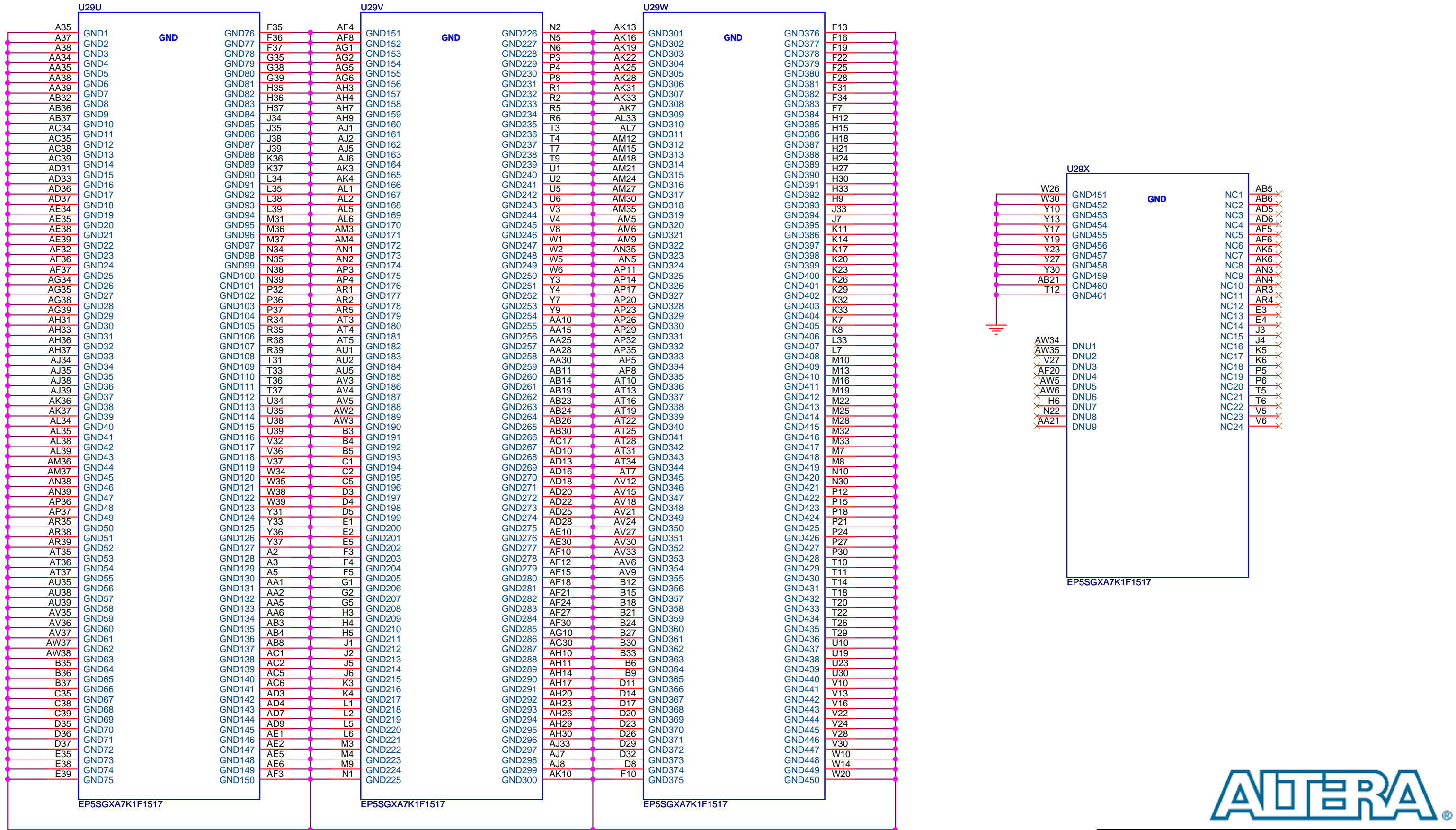
GXB_RXRp_12	GXB_RXRp_12	21
GXB_RXRn_12	GXB_RXRn_12	21
GXB_RXRp_18	GXB_RXRp_18	17
GXB_RXRn_18	GXB_RXRn_18	17
GXB_RXRp_23	GXB_RXRp_23	17
GXB_RXRn_23	GXB_RXRn_23	17
GXB_TXRp_18	GXB_TXRp_18	17
GXB_TXRn_18	GXB_TXRn_18	17
GXB_TXRp_23	GXB_TXRp_23	17
GXB_TXRn_23	GXB_TXRn_23	17
REFCLK_B2R4p	REFCLK_B2R4p	25
REFCLK_B2R4n	REFCLK_B2R4n	25
REFCLK_B2R5p	REFCLK_B2R5p	25
REFCLK_B2R5n	REFCLK_B2R5n	25
REFCLK_B3R6p	REFCLK_B3R6p	25
REFCLK_B3R6n	REFCLK_B3R6n	25
REFCLK_B3R7p	REFCLK_B3R7p	25
REFCLK_B3R7n	REFCLK_B3R7n	25



FPGA / XCVR Power



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