Compal Confidential

Lotus M/B Schematics Document

14": Elise; 15.6" Exige

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2011/10/27
Version 0.1

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
Custom	LA-8551P	0.1

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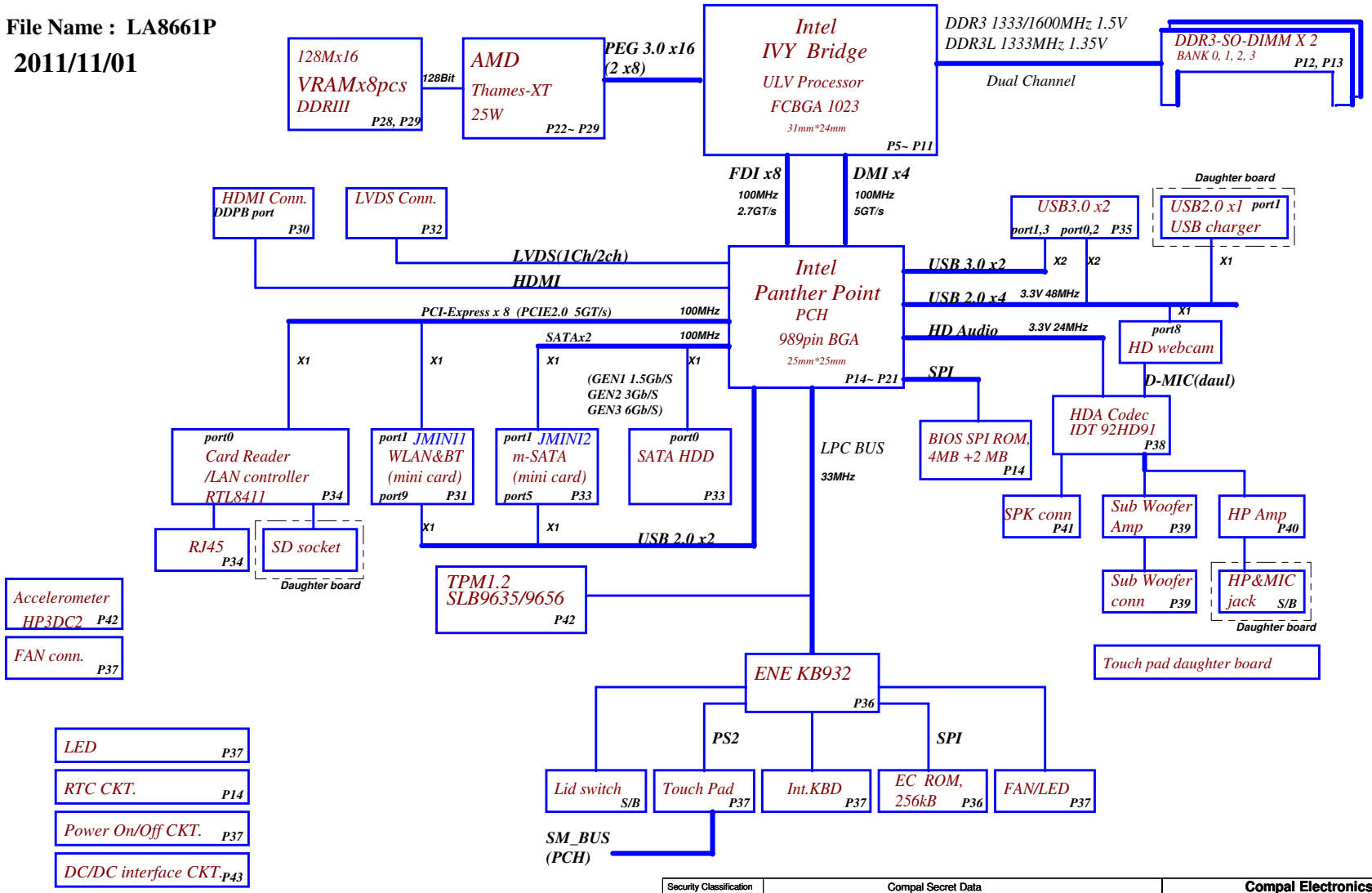
Model Name : Lotus

File Name : LA8661P

2011/11/01



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Compal Electronics, Inc.			
Title	Block Diagrams		
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QAU30/50 (LA-8661P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+VGA_CORE	GPU power	PX	OFF	OFF
+3VGS	GPU power	PX	OFF	OFF
+1.8VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF
+1.0VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	V
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	SATA, JHDD1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (left Side)
		1	USB2.0 (right Side)
	UHCI1	2	USB2.0 (left Side)
		3	None
	UHCI2	4	None
		5	None
	UHCI3	6	None
		7	None
EHCI2	UHCI4	8	Camera
		9	Mini Card(WLAN& BT)
	UHCI5	10	None
		11	None
	UHCI6	12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	USB3.0 (left Side)
	4	None

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	PCIE LAN CARD READER	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	mini WLAN	CLKOUTFLEX2	None
	CLKOUT_PCIE2	None	CLKOUTFLEX3	DGPU_PRSNT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

BY SKU		
TPM	9635@	9656@
CPU	CPUUMA1@ CPUUMA2@ CPUDIS@	
VRAM	X76@ M2G@	H2G@ S2G@

Option	@	CONN@	USB30@	PX@	UMA@	DIS@	THA@
UMA	X	X	V	X	V	X	X
DIS	X	X	V	V	X	V	V

Symbol Note :
: means Digital Ground

: means Analog Ground

Project ID	30UMA@	30DIS@	50UMA@	50DIS@

PCB	LA-8661P	LA-8662P
	PX@	UMA@

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Title: Notes List

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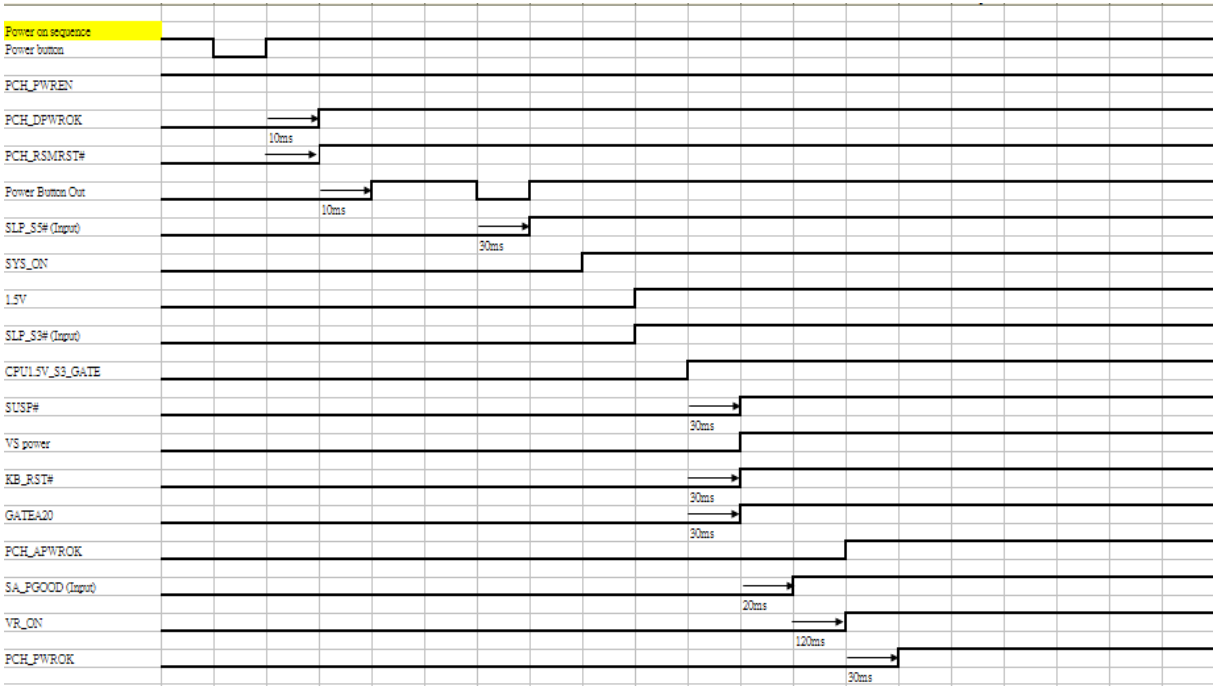

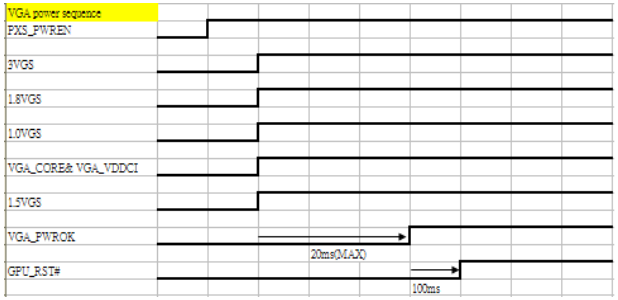

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Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

Size	Document Number	Rev
B		0.1

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UCPU1 CPUDIS01@
i5-2467M CPU
SA00004X000

UCPU1 CPUDIS02@
i5-2367M CPU
SA000051H20

UCPU1 CPUDIS03@
i5-2367M CPU
SA000051H20

UCPU1 CPUDIS04@
i5-3317U CPU
SA00005K600

UCPU1 CPUUMA3@
i5-2367M CPU
SA000051H20

UCPU1 CPUUMA4@
17W 1.7GHz GT2 ES2 QBP7
SA00005B010

UCPU1 CPUUMA5@
17W 1.7GHz no cnfig ES2 QBTQ
SA00005B020

UCPU1 CPUUMA1@
17W 1.5GHz GT2 ES2 QBP8
SA00005AZ10

UCPU1 CPUUMA2@
17W 1.5GHz no cnfig ES2 QBTP
SA00005AZ20

Sandy Bridge:
Intel Core i5-2467M: SA00004X000 (4619HY32L01)

Ivy Bridge:
1.5GHz GT2 ES2 QBP8: SA00005AZ10 (4619HZ32L01)
1.5GHz ES2 QBTP: SA00005AZ20(4619HZ32L02)

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

+VCCP

RC1 24.9_0402_1%

CU65 0.1U_0402_16V4Z

Add CU65 0.1U as EMI request. 12.19

UCPU1A @

PEG_ICOMPI G3
PEG_ICOMPO G1
PEG_RCOMPO G4
PEG_COMP

<PEG>

DMI
<16> DMI_CRX_PTX_N0 M2 DMI_RX#[0]
<16> DMI_CRX_PTX_N1 P6 DMI_RX#[1]
<16> DMI_CRX_PTX_N2 P1 DMI_RX#[2]
<16> DMI_CRX_PTX_N3 P10 DMI_RX#[3]
<16> DMI_CRX_PTX_P0 N3 DMI_RX[0]
<16> DMI_CRX_PTX_P1 P7 DMI_RX[1]
<16> DMI_CRX_PTX_P2 P3 DMI_RX[2]
<16> DMI_CRX_PTX_P3 P11 DMI_RX[3]
<16> DMI_CTX_PRX_N0 K1 DMI_TX#[0]
<16> DMI_CTX_PRX_N1 M8 DMI_TX#[1]
<16> DMI_CTX_PRX_N2 N4 DMI_TX#[2]
<16> DMI_CTX_PRX_N3 R2 DMI_TX#[3]
<16> DMI_CTX_PRX_P0 K3 DMI_TX[0]
<16> DMI_CTX_PRX_P1 M7 DMI_TX[1]
<16> DMI_CTX_PRX_P2 P4 DMI_TX[2]
<16> DMI_CTX_PRX_P3 T3 DMI_TX[3]

FDI
<16> FDI_CTX_PRX_N0 U7 FDI0_TX#[0]
<16> FDI_CTX_PRX_N1 W11 FDI0_TX#[1]
<16> FDI_CTX_PRX_N2 W1 FDI0_TX#[2]
<16> FDI_CTX_PRX_N3 AA6 FDI0_TX#[3]
<16> FDI_CTX_PRX_N4 W6 FDI1_TX#[0]
<16> FDI_CTX_PRX_N5 V4 FDI1_TX#[1]
<16> FDI_CTX_PRX_N6 Y2 FDI1_TX#[2]
<16> FDI_CTX_PRX_N7 AC9 FDI1_TX#[3]
<16> FDI_CTX_PRX_P0 U6 FDI0_TX[0]
<16> FDI_CTX_PRX_P1 W10 FDI0_TX[1]
<16> FDI_CTX_PRX_P2 W3 FDI0_TX[2]
<16> FDI_CTX_PRX_P3 AA7 FDI0_TX[3]
<16> FDI_CTX_PRX_P4 W7 FDI1_TX[0]
<16> FDI_CTX_PRX_P5 T4 FDI1_TX[1]
<16> FDI_CTX_PRX_P6 AA3 FDI1_TX[2]
<16> FDI_CTX_PRX_P7 AC8 FDI1_TX[3]
<16> FDI_FSYNC0 AA11 FDI0_FSYNC
<16> FDI_FSYNC1 AC12 FDI1_FSYNC
<16> FDI_INT U11 FDI_INT
<16> FDI_LSYNC0 AA10 FDI0_LSYNC
<16> FDI_LSYNC1 AC8 FDI1_LSYNC

Intel(R) FDI

PCI EXPRESS - GRAPHICS

<PEG>

+VCCP

RC88@ 10K_0402_5%
RC2 24.9_0402_1%

EDP_COMP AF3 eDP_COMPIO
AD2 eDP_ICOMPO
AG11 eDP_HPD#
AG4 eDP_AUX#
AF4 eDP_AUX
AC3 eDP_TX#[0]
AC4 eDP_TX#[1]
AE11 eDP_TX#[2]
AE7 eDP_TX#[3]
AC1 eDP_TX[0]
AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]

eDP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

NOTE:eDP_COMPIO and eDP_ICOMPO should not be left floating even if Internal Graphic is disabled since they are shared with other interfaces

PEG_RX#[0] J21
PEG_RX#[1] B22
PEG_RX#[2] D21
PEG_RX#[3] A19
PEG_RX#[4] D17
PEG_RX#[5] B14
PEG_RX#[6] D13
PEG_RX#[7] A11
PEG_RX#[8] B10
PEG_RX#[9] G8
PEG_RX#[10] A8
PEG_RX#[11] B6
PEG_RX#[12] H8
PEG_RX#[13] E5
PEG_RX#[14] K7
PEG_RX#[15] H22

PEG_RX[0] K22
PEG_RX[1] K19
PEG_RX[2] C21
PEG_RX[3] D19
PEG_RX[4] C19
PEG_RX[5] D16
PEG_RX[6] C13
PEG_RX[7] D12
PEG_RX[8] C11
PEG_RX[9] C9
PEG_RX[10] F8
PEG_RX[11] C8
PEG_RX[12] C5
PEG_RX[13] H6
PEG_RX[14] F6
PEG_RX[15] K6

PEG_TX#[0] G22
PEG_TX#[1] C23
PEG_TX#[2] D23
PEG_TX#[3] F21
PEG_TX#[4] H19
PEG_TX#[5] C17
PEG_TX#[6] K15
PEG_TX#[7] F17
PEG_TX#[8] F14
PEG_TX#[9] A15
PEG_TX#[10] J14
PEG_TX#[11] H13
PEG_TX#[12] M10
PEG_TX#[13] F10
PEG_TX#[14] D9
PEG_TX#[15] J4

PEG_TX[0] F22
PEG_TX[1] A23
PEG_TX[2] D24
PEG_TX[3] F21
PEG_TX[4] G19
PEG_TX[5] B18
PEG_TX[6] K17
PEG_TX[7] G17
PEG_TX[8] E14
PEG_TX[9] C15
PEG_TX[10] K13
PEG_TX[11] G13
PEG_TX[12] K10
PEG_TX[13] G10
PEG_TX[14] D8
PEG_TX[15] K4

IVY-BRIDGE_BGA1023

10/05 Change to 0.22uF.

Typ- suggest 220nF. The change in AC capacitor value from 180nF to 265nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Buffered reset to CPU

Reset# signal is driven by the PCH to multiple agents on the platform.
PCH Reset# output DC levels are 0-V and 3.3 V.
processor Reset input DC levels are 0V and 1.0 V.
Processor high-voltage level is lower than PCH high voltage level, therefore a voltage level shifter is required on the Reset# signal.
In order for Reset# to meet the signal quality requirement at the input to the processor OD buffer must be placed on the motherboard between the PCH and the processor.

+3VS
CC1 0.1U_0402_16V4Z
+VCCP
RC3 75_0402_5%
UC1
SN74LVC1G07DCKR_SC70-5
<17,22,31,34,36,42> PLT_RST#
PLT_RST#
BUFO_CPU_RST#
RC4 43_0402_1%
BUF_CPU_RST#
RC6 @ 750_0402_1%
R375 @ 0_0402_5%

Requires a series resistor of 43±5% between processor and PCH. It also a needs an Rtt of 75±5% to VCCP after the OD buffer and before the series resistor.

This pin is for compability with future platforms. A pull up resistor to VCCIO is required if connected to the DF_TVS strap on the PCH.

PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

SI2 change to 0201
12.19

UCPU1B @

<18> H_SNB_IVB#
PROC_SELECT# F49
PROC_DETECT# C57
@RC7 10K_0201_5%
PAD T5 @
CATERR# C49
<18,36> H_PECI
PECI A48
<36,46> H_PROCHOT#
H_PROCHOT# RC10 56_0402_5%
PROCHOT# C45
<18> H_THRMTRIP#
H_THEMTRIP# R RC12 0_0402_5%
THERMTRIP# D45

MISC
THERMAL

BCLK J3
BCLK# H2
CLK_CPU_DMI <15>
CLK_CPU_DMI# <15>
100MHz
DPLL_REF_CLK AG3
DPLL_REF_CLK# AG1
RC85 1K_0402_5%
RC84 1K_0402_5%
+VCCP

CLOCKS

XDP_DBRESET# RC5 1K_0201_5%
+3VS

SI2 change to 0201
12.19

SM_DRAMRST# AT30
H_DRAMRST#
H_DRAMRST# <7>
SM_RCOMP[0] BE44
SM_RCOMP[1] BE43
SM_RCOMP[2] BG43
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2

DDR3 MISC

PAD
PAD @ T35
T39 @
PRDY# N53
PREQ# N55
TCK L56
TMS L55
TRST# J58
XDP_TCK
XDP_TMS
XDP_TRST#
TDI M60
TDO L59
XDP_TDI
XDP_TDO
DBR# K58
XDP_DBRESET#
RC17 0_0201_5%
XDP_DBRESET#
XDP_DBRESET# <16>
12/16:Change to 0201 for SI2

BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61
XDP_BPM#4_R
XDP_BPM#5_R
XDP_BPM#6_R
XDP_BPM#7_R
T60 @PAD
T61 @PAD
T62 @PAD
T63 @PAD

JTAG & BPM

PWR MANAGEMENT

IVY-BRIDGE_BGA1023

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

Processor Pullups

+VCCP
RC8 62_0402_5% H_PROCHOT#
RC11 10K_0201_5% H_CPUPWRGD_R

SI2 change to 0201
12.19

SI2 change to 0201
12.19

<16> H_PM_SYNC
H_PM_SYNC_R RC13 0_0201_5%
PM_SYNC C48
<18> H_CPUPWRGD
H_CPUPWRGD_R RC16 0_0201_5%
UNCOREPWRGOOD B46
UNCOREPWRGOOD:非CORE外的電OK
PM_SYS_PWRGD_BUF
PM_DRAM_PWRGD_R RC18 130_0402_5%
SM_DRAMPWROK BE45
SM_DRAMPWROK:DRAM power ok
BUF_CPU_RST# D44
RESET#

SI2 change to 0201
12.19

+3VS
RC81 10K_0402_5%
CC2 0.1U_0402_16V4Z
+3V_PCH
UC2 74AHC1G09GW_TSSOP5
@RC27 0_0402_5%
<16> SYS_PWROK
<16> PM_DRAM_PWRGD
RC28 200_0402_5%
PM_SYS_PWRGD_BUF
+1.5V_CPU_VDDQ
RC25 200_0402_5%
@ RC29 39_0402_5%
Part Number = SA00003Y000
<43,52> SUSP
SUSP
@ QC1 2N7002_SOT23

11.06 Change to +3V_PCH

DDR3 Compensation Signals

SM_RCOMP0 RC23 140_0402_1%
SM_RCOMP1 RC24 25.5_0402_1%
SM_RCOMP2 RC26 200_0402_1%

PU/PD for JTAG signals

XDP_TMS T40 @PAD
XDP_TDI T41 @PAD
XDP_TDO T42 @PAD
XDP_TCK T43 @PAD
XDP_TRST# T46 @PAD

SI2 change to 0201
12.19

C263 0.1U_0201_16V4Z
XDP_TRST#
C264 220P_0402_50V7K
PLT_RST#
C265 @ 100P_0402_50V8J
PM_SYS_PWRGD_BUF
C266 220P_0402_50V7K
BUF_CPU_RST#

XDP_DBRESET#_R CC4 0.1U_0201_16V4Z
H_CPUPWRGD_R C118 220P_0402_50V7K

SI2 change to 0201
12.19

6/27 Add ESD solution

2011.10.18 delete all reserved XDP conponent.
Just reserve test point for XDP.

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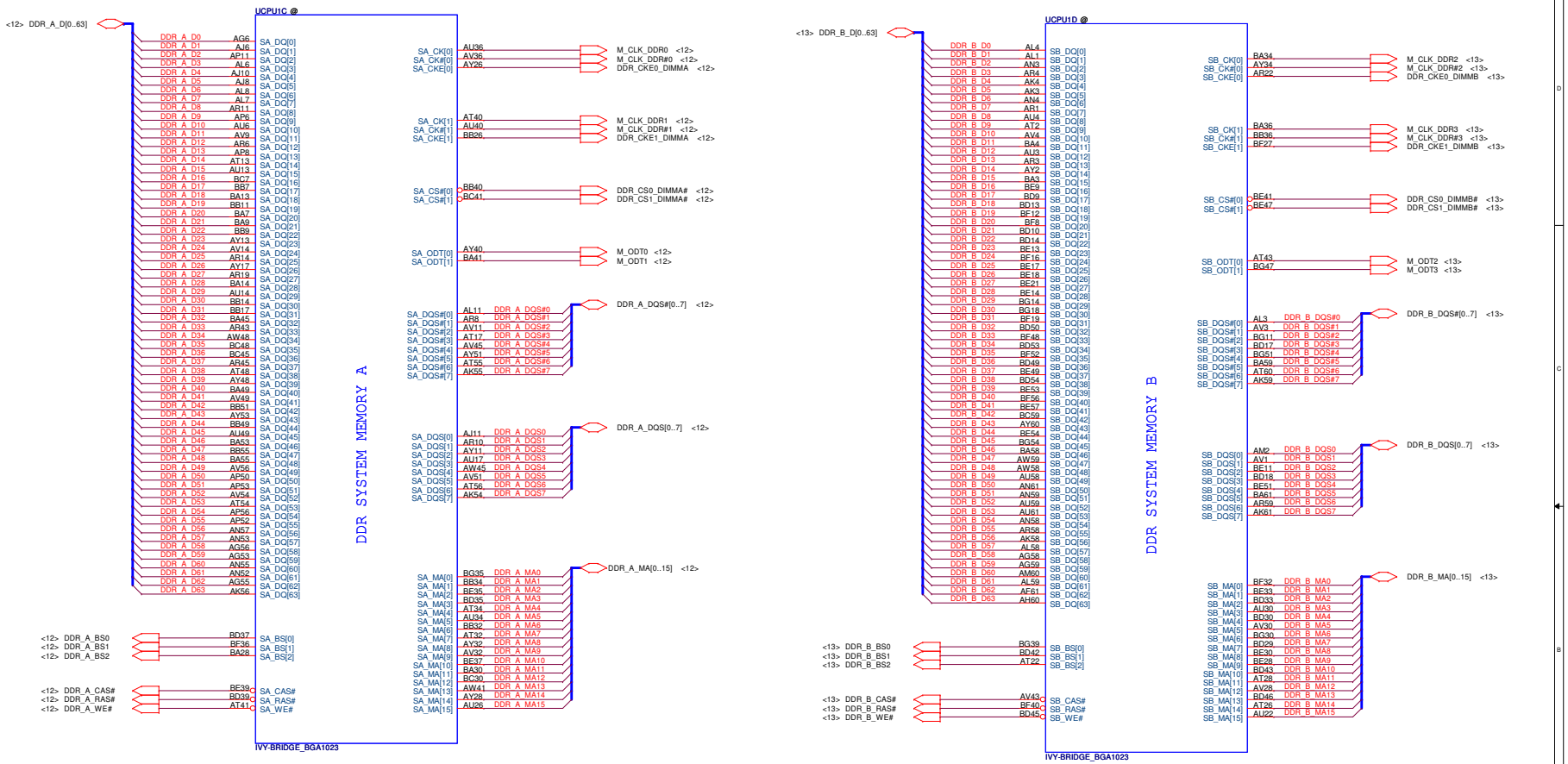

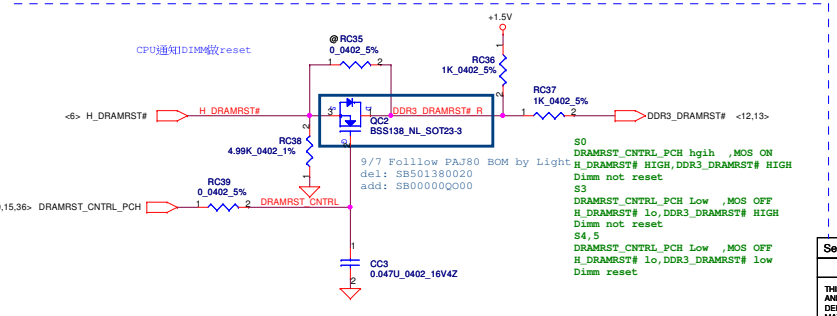

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Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
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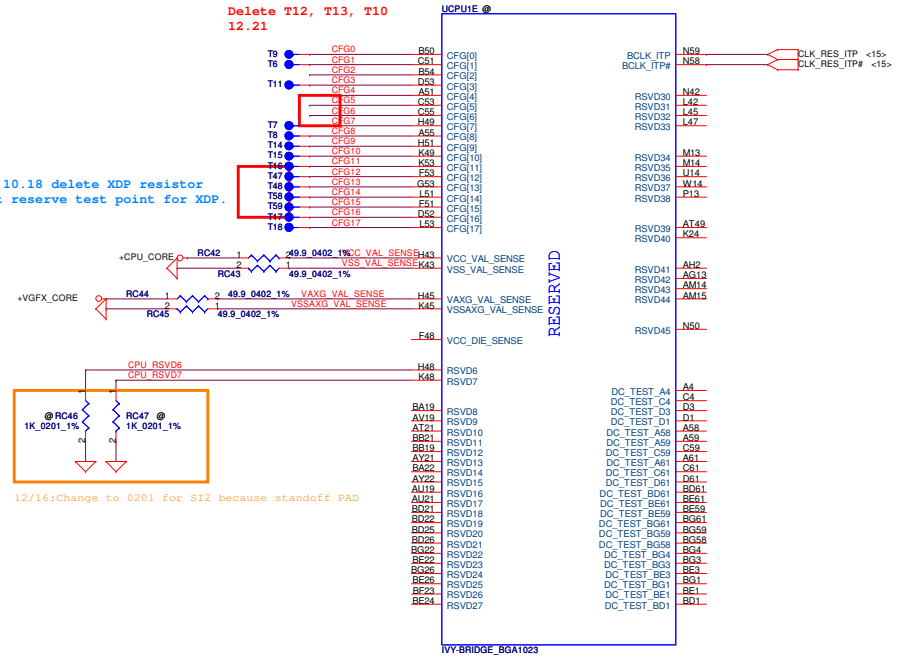
Change to part G.

Delete T12, T13, T10
12.21

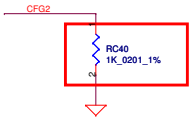
2011.10.18 delete XDP resistor
just reserve test point for XDP.



12/16:Change to 0201 for SI2 because standoff PAD

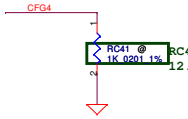
CFG Straps for Processor

PEG bus is reversed, need to PD.
11.01



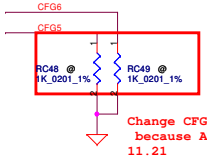
RC40 SI2 change to 0201
12.19

PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



RC41 SI2 change to 0201
12.19

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

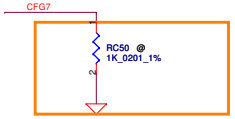


RC48, RC49 SI2 change to 0201
12.19

Change CFG[6:5] to 11 = 1 x 16 PCI Express
because AMD driver can't install issue
11.21

PCIE Port Bifurcation Straps	
CFG[6:5]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express *

12/16:Change to 0201 for SI2 because standoff PAD



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

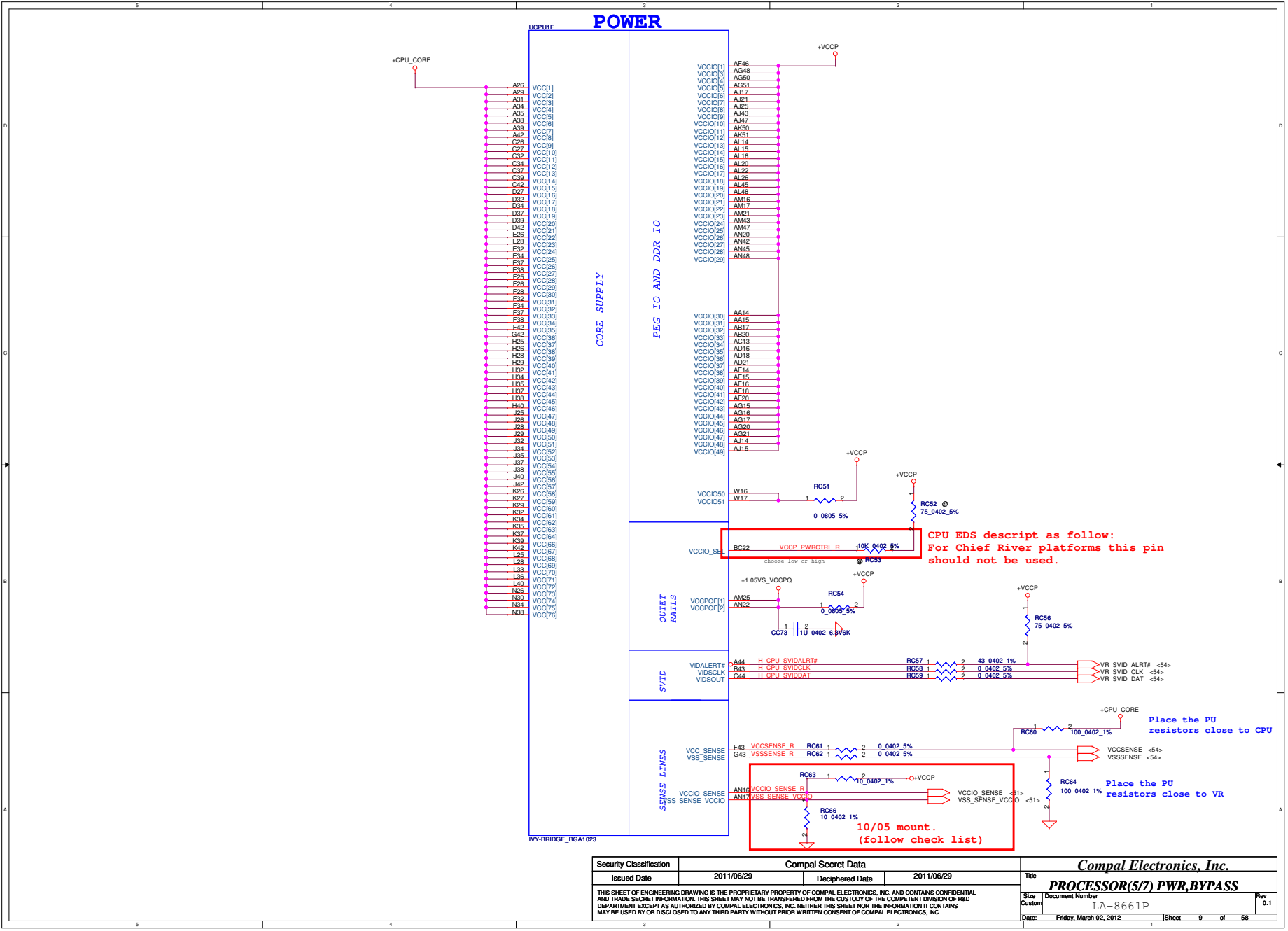
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
Custom	LA-8661P	0.1

Date: Friday, March 02, 2012 Sheet 8 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-8661P	0.1

Date: Friday, March 02, 2012 Sheet 9 of 58

POWER

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

+V_SM_VREF should have 20 mil trace width

10/03 add +V_DDR_REFB

Check with Power Team CC100 (330UF) can be taken off. 10.31

QC4 Change to SA0000JA00 for small package 1016

+1.5V_CPU_VDDQ Source

Follow DG 0.71 page 6

SI# BOM Change CC118 0.1u 25V form 0.1u 16V

For Chief River only

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

10/03 add +V_DDR_REFB

Delete CC25 330U cap 10.19 (after check with power)

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

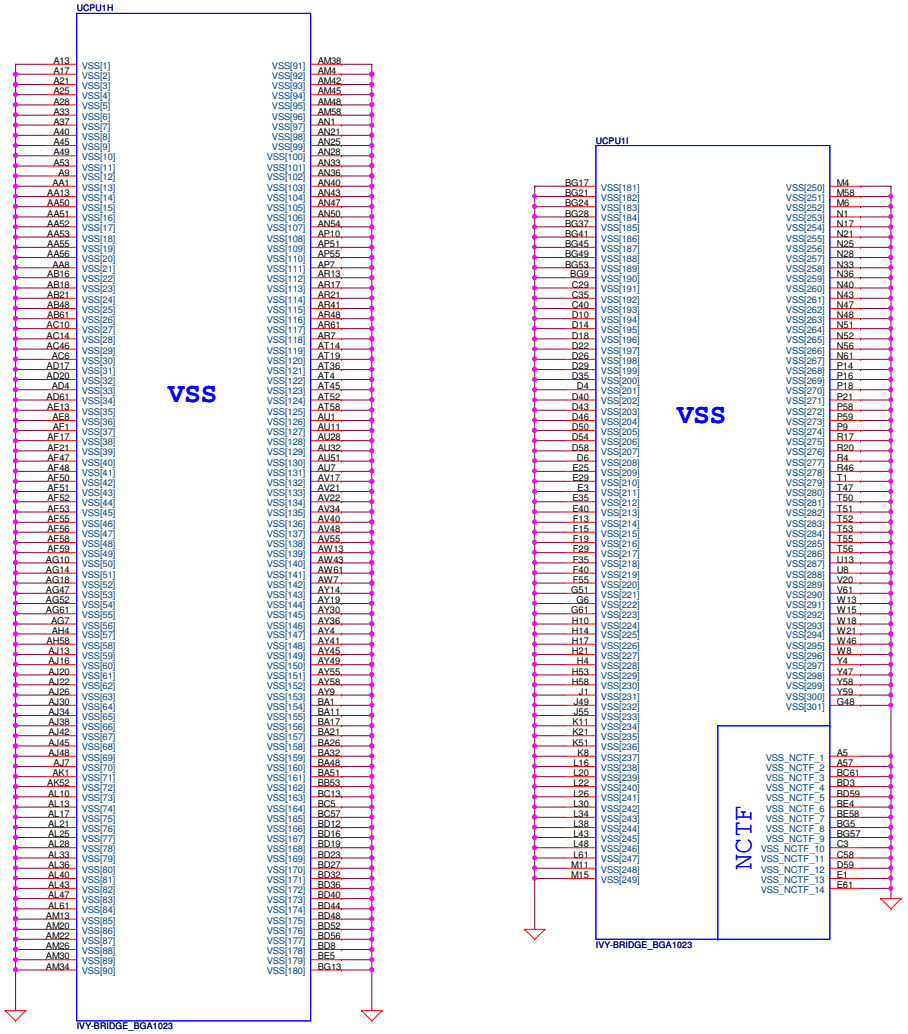
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom	LA-8661P	0.1

Date: Friday, March 02, 2012 | Sheet 10 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

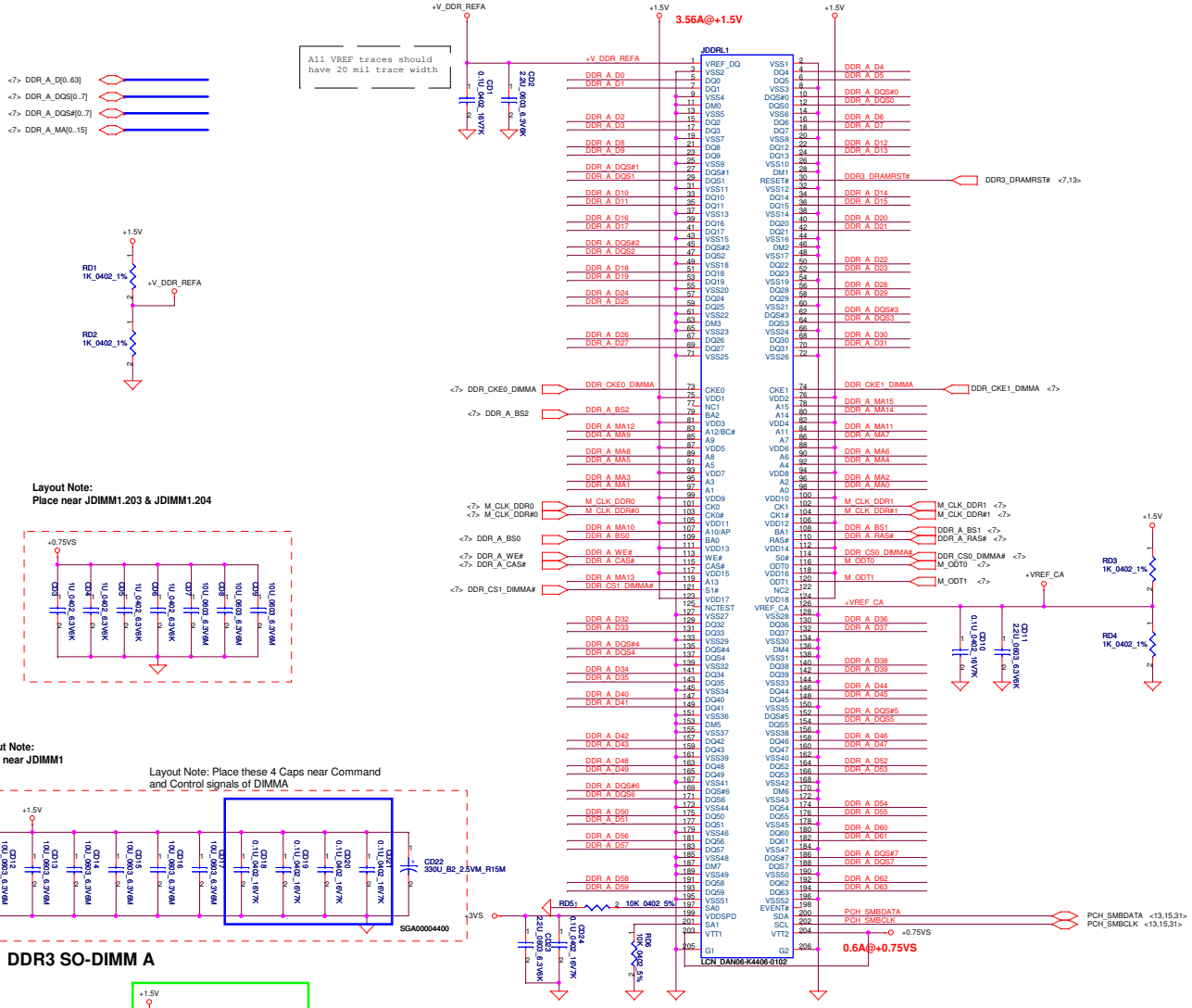
Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Friday, March 02, 2012 | Sheet 11 of 58

DDR3 SO-DIMM A

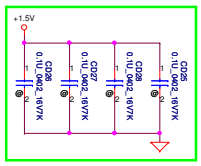


Layout Note:
Place near JDIMM1.203 & JDIMM1.204

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

SGA00004400



SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	DDRIII DIMM		
Size: C	Document Number: LA-8661P		Rev: 0.1
Date: Friday, March 02, 2012	Sheet 12 of 58		

DDR3 SO-DIMM B

10/03 change to +V_DDR_REFB

3.56A@+1.5V

All VREF traces should have 20 mil trace width

<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_MA[0..15]

Delete DDR_B_DM[0..7]

JDDRL2

LCN_DAN06-K4406-0102

10/03 change to +V_DDR_REFB

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

DDR3 SO-DIMM B

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

10/03 change to +VREF_CB

10/05 change to PH.

Standard
<Address(SA1,SA0):10>

0.6A@+0.75VS

Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: DDRIII-DDRH

Size	Document Number	Rev
	LA-8661P	0.1

Date: Friday, March 02, 2012 Sheet 13 of 58

PCH_RTCX1
PCH_RTCX2
RH115 10M_0402_5%
32.768K 12.5PF Q13MC1460017100
CH2 18P_0201_50V8J
CH3 18P_0201_50V8J
YH1

+RTCVCC
This is needed to reduce leakage from Coin Cell Battery in G3 state
RH116 1M_0402_5%
SM_INTRUDER#

9/7 SMT memo:Follow PM requirement change R1 p/n into PV BOM
R1: SA00004EES0
R3: SA00004QOB0

UH1A

+RTCVCC
CH4 1U_0402_6.3V6K
CLRP1 SHORT PADS
RH117 20K_0402_5%
RH118 20K_0402_5%
CH5 1U_0402_6.3V6K
CLRP2 SHORT PADS
CLP1 & CLP2 place near DIMM

PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

FWH0 / LAD0 C38 LPC_AD0 → LPC_AD0 <31,36,42>
FWH1 / LAD1 A38 LPC_AD1 → LPC_AD1 <31,36,42>
FWH2 / LAD2 B37 LPC_AD2 → LPC_AD2 <31,36,42>
FWH3 / LAD3 C37 LPC_AD3 → LPC_AD3 <31,36,42>
FWH4 / LFRAME# D36 LPC_FRAME# → LPC_FRAME# <31,36,42>
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 SERIRQ → SERIRQ <36,42>
LPC

EC,TPM and Debug card.

HDA_BITCLK_AUDIO <38> RH119 33_0402_5% HDA_BIT_CLK
HDA_RST_AUDIO# <38> RH120 33_0402_5% HDA_RST#
HDA_SYNC_AUDIO <38> RH121 33_0402_5% HDA_SYNC_R
+5VS
Prevent back drive issue.
QH1 SB000002X00 BSS138W-7-F_SOT323-3
HDA_SDIN0 <38>
RH158 1M_0402_5%
RH122 @ 0_0402_5%
7/12 SI add 1M pull down

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDOUT A36 HDA_SDO
C36 HDA_DOCK_EN# / GPIO33
N32 HDA_DOCK_RST# / GPIO13
IHDA

9/7 SMT memo:Follow intel ME update requirement
add: RH123
<36> HDA_SDO RH123 0_0402_5% HDA_SDOUT
<38> HDA_SDOUT_AUDIO RH125 33_0402_5% HDA_SDOUT

SI2 delete RH128& RH127 200 ohm for CPU screw PAD
12.19
+3V_PCH
@RH129 200_0402_5%
PCH_JTAG_TDO RH133 100_0201_1%
PCH_JTAG_TMS RH134 100_0402_1%
PCH_JTAG_TDI RH135 100_0402_1%

PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

SI2 change to RH133 0201
12.19
51_0402_5% RH150 PCH_JTAG_TCK

Delete RH151& CH1 for EMI reserve.
01.18

PCH_SPI_CLK T3 SPI_CLK
PCH_SPI_CS0# Y14 SPI_CS0#
PCH_SPI_CS1# T1 SPI_CS1#
PCH_SPI_SI V4 SPI_MOSI
PCH_SPI_SO U3 SPI_MISO
SPI

PANTHER-POINT_FCBGA989

SATA 6G

SATA0RXN AM3 SATA_PRX_DTX_N0 <33>
SATA0RXP AM1 SATA_PRX_DTX_P0 <33>
SATA0TXN AP7 SATA_PTX_DRX_N0 <33>
SATA0TXP AP5 SATA_PTX_DRX_P0 <33>
SATA HDD

SATA1RXN AM10 SATA_PRX_DTX_N1 <33>
SATA1RXP AM8 SATA_PRX_DTX_P1 <33>
SATA1TXN AP11 SATA_PTX_DRX_N1 <33>
SATA1TXP AP10 SATA_PTX_DRX_P1 <33>
JMINI2 SSD

SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN V7
SATA4RXP V5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATA

SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP RH130 37.4_0402_1%
+1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP RH132 49.9_0402_1%
+1.05VS_SATA3
SATA3RBIAS AH1 RBIAS_SATA3 RH137 750_0402_1%
20mils
+RTCVCC
W=20mils
CH7 1U_0402_6.3V6K
Place CH95 close to PCH.

SATALED# P3 SATA_LED# → SATA_LED# <34>
SATA0GP / GPIO21 V14 HDDHALT_LED# → HDDHALT_LED# <34>
SATA1GP / GPIO19 P1 BBS_BIT0_R RB0 10K_0201_5%
+3VS

SI2 change to 0201
12.19

SI2 change to RH133 0201
12.19

SPI BIOS Pinout
(1)CS# (2)DO (3)WP# (4)GND (5)DIO (6)CLK (7)HOLD# (8)VCC
W25X32

SPI BIOS Pinout
(1)CS# (2)DO (3)WP# (4)GND (5)DIO (6)CLK (7)HOLD# (8)VCC
W25X32

SPI ROM FOR ME (4MByte)
Change BIOS ROM power rail to +3VS
2012.01.08

SI stuff RH142, RH175, RH176, RH235
11.22

+3VS
RH141 3.3K_0402_5%
PCH_SPI_CS0# RH142 0_0402_5% PCH_SPI_CS0#_R
PCH_SPI_SO RH175 33_0402_5% PCH_SPI_SO_RIC
PCH_SPI_WP# RH145 3.3K_0402_5%
UH2 MX25L3206EM2I-12G_SO8
CS# SO/SIO1 WP# GND VCC HOLD# SCLK SI/SIO0
PCH_SPI_HOLD# RH144 3.3K_0402_5%
PCH_SPI_CLK_RIC RH176 33_0402_5% PCH_SPI_CLK
PCH_SPI_SI_RIC RH235 33_0402_5% PCH_SPI_SI
CH6 0.1U_0201_16V4Z

SPI ROM FOR Win8 (2MByte)

SI stuff RH315, RH323, RH312, RH321
11.22

+3VS
RH304 3.3K_0402_5%
PCH_SPI_CS1# RH315 0_0402_5% PCH_SPI_CS1#_R
PCH_SPI_SO RH323 33_0402_5% PCH_SPI_SO_LIC
PCH_SPI_WP# RH302 3.3K_0402_5%
UH5 MX25L1606EM2I-12G_SO8
CS# SO WP# GND VCC HOLD# SCLK SI
PCH_SPI_HOLD# RH301 3.3K_0402_5%
PCH_SPI_CLK_LIC RH312 33_0402_5% PCH_SPI_CLK
PCH_SPI_SI_LIC RH321 33_0402_5% PCH_SPI_SI
CH8 0.1U_0201_16V4Z
20mils

SI2 change to 0201
12.19
+3VS
SERIRQ RH131 10K_0402_5%
HDDHALT_LED# RH136 10K_0402_5%
SATA_LED# RH138 10K_0201_5%
HDA_SPKR RH139 1K_0402_5%
LOW=Default
HIGH=No Reboot

+RTCVCC
PCH_INTVRMEN RH124 330K_0402_5%
PCH_INTVRMEN RH126 330K_0402_5%
INTVRMEN
H : Integrated VRM enable
L : Integrated VRM disable

HDA_SDO
ME debug mode , this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden
HDA_SDOUT RH140 1K_0402_5%
+3V_PCH
Low = Disabled
High = Enabled

RTC Battery
+RTCBATT
1K_0402_5% RH148 10mils 20mils
DH1 BAV70W 3P C/C_SOT-323
<BOM Structure>
JRTC1 ACES_50271-0020N-001
+3VLP

HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
+3V_PCH
HDA_SYNC RH149 1K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC
Size: Document Number: LA-8043P
Rev: 0.1
Date: Friday, March 02, 2012 Sheet 14 of 58

PV# 9/13 change power rail form +3VALW->+3V_PCH

10/03 change to PCIE port1.

PCIE LAN/Card Reader

Mini card WLAN

UH1B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

PANTHER-POINT_FCBGA989

SI2 change to 0201 12.19

PCIE LAN/Card Reader

MiniWLAN

SI2 change to 0201 12.19

SI2 change to 0201 12.19

SI2 change to 0201 12.19

Change WL_OFF# to GPIO45 (pull-high) +3V_PCH 2012.01.04

SI2 YH2 change to SJ10000DJ00 12.19

Reserve for EMI please close to UH1

12/16:Change to 0201 for SI2

If use extenal CLK gen, please place close to CLK gen else, please place close to PCH

100MHz

100MHz

SI# 8/8 Add SML1CLK/SML1DATA for EC detect Thermal

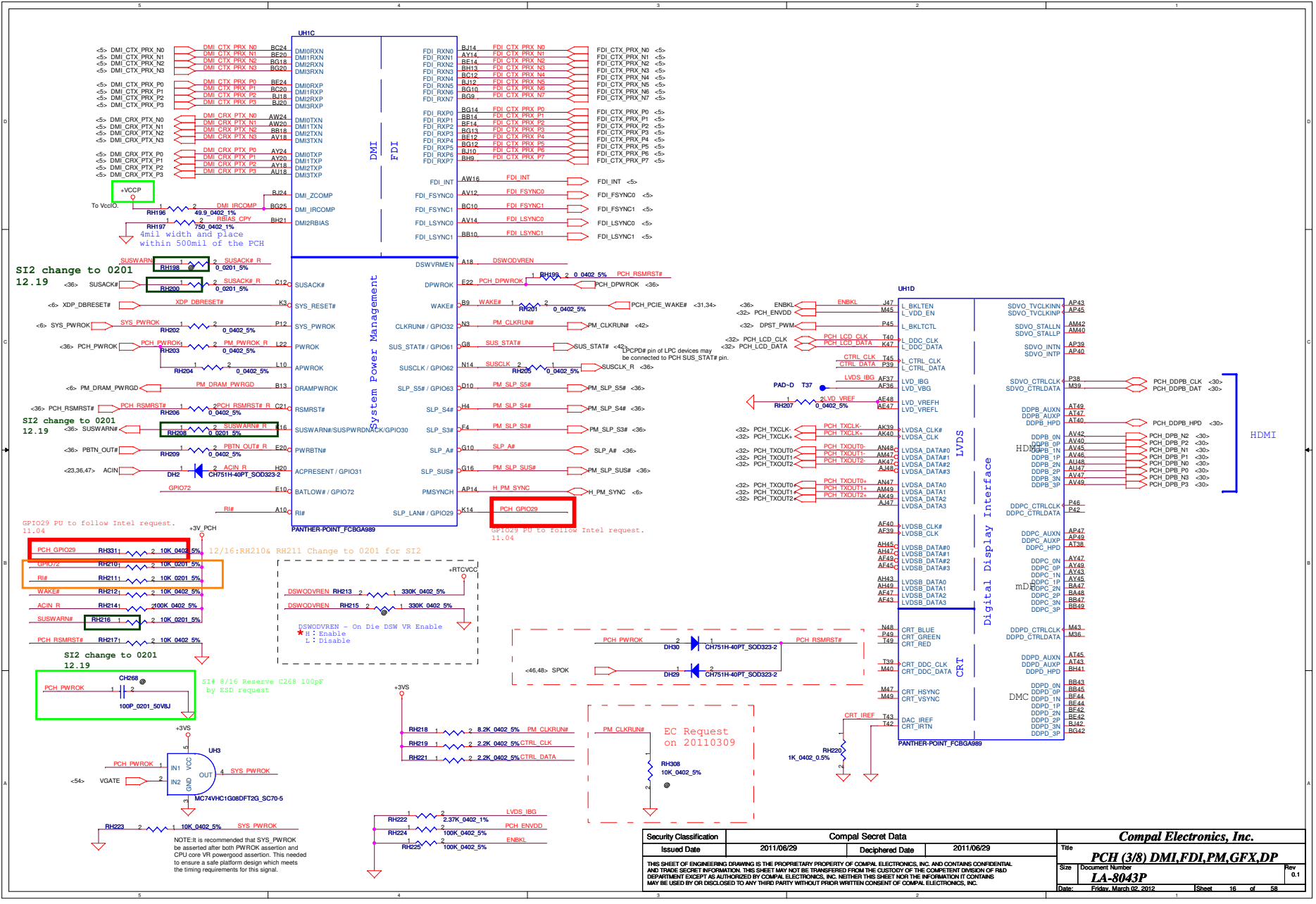
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: | Document Number: LA-8043P | Rev: 0.1

Date: Friday, March 02, 2012 | Sheet 15 of 58



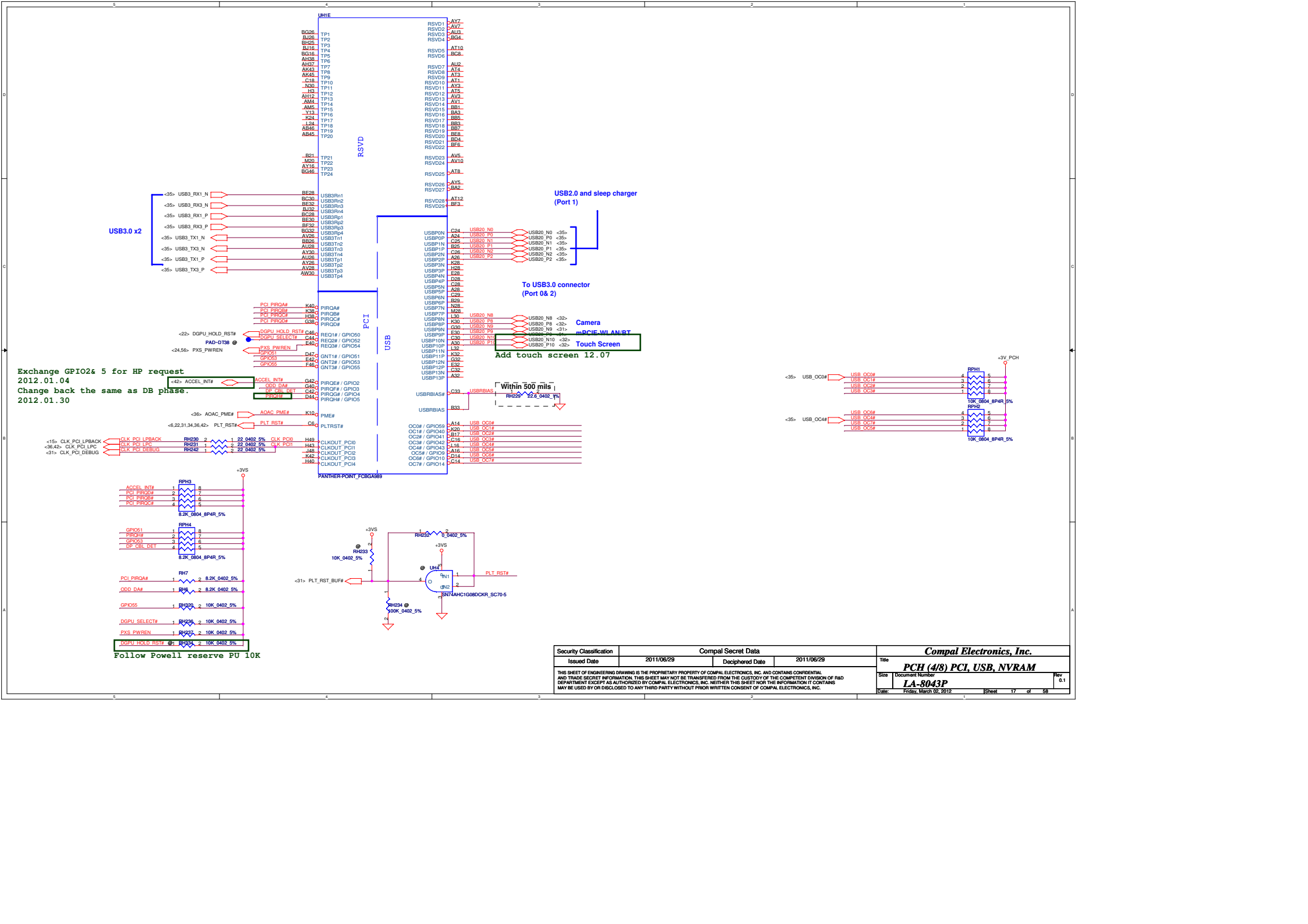
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
	LA-8043P	0.1

Date: Friday, March 02, 2012 Sheet 16 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

Size	Document Number	Rev
	LA-8043P	0.1

Date: Friday, March 02, 2012 | Sheet 17 of 58

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

GPIO27
PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

DB# 10/20 Reserve GPIO 36 pull up resistor and add pull down resistor

Refer Powell change BT_ON to GPIO34 10.21

GPIO 69 follow Intel's request PU. 11.04

This signal should be connected to the processor's UNCOREPWRGD input to indicate when the processor power is valid.

Layout note: CLOSE TO THE BRANCHING POINT

12/16:Change to 0201 for SI2

SI2 change to 0201 12.19

SI2 change to 0201 12.19

12/20:Delete RH253 for SI2

SI2 change to 0201 12.19

Refer Powell change BT_ON to GPIO34 10.21

SI# 8/8 change PCH_WAN_RADIO_OFF# to PCH_GPIO35

PANTHER-POINT_FCBGA989

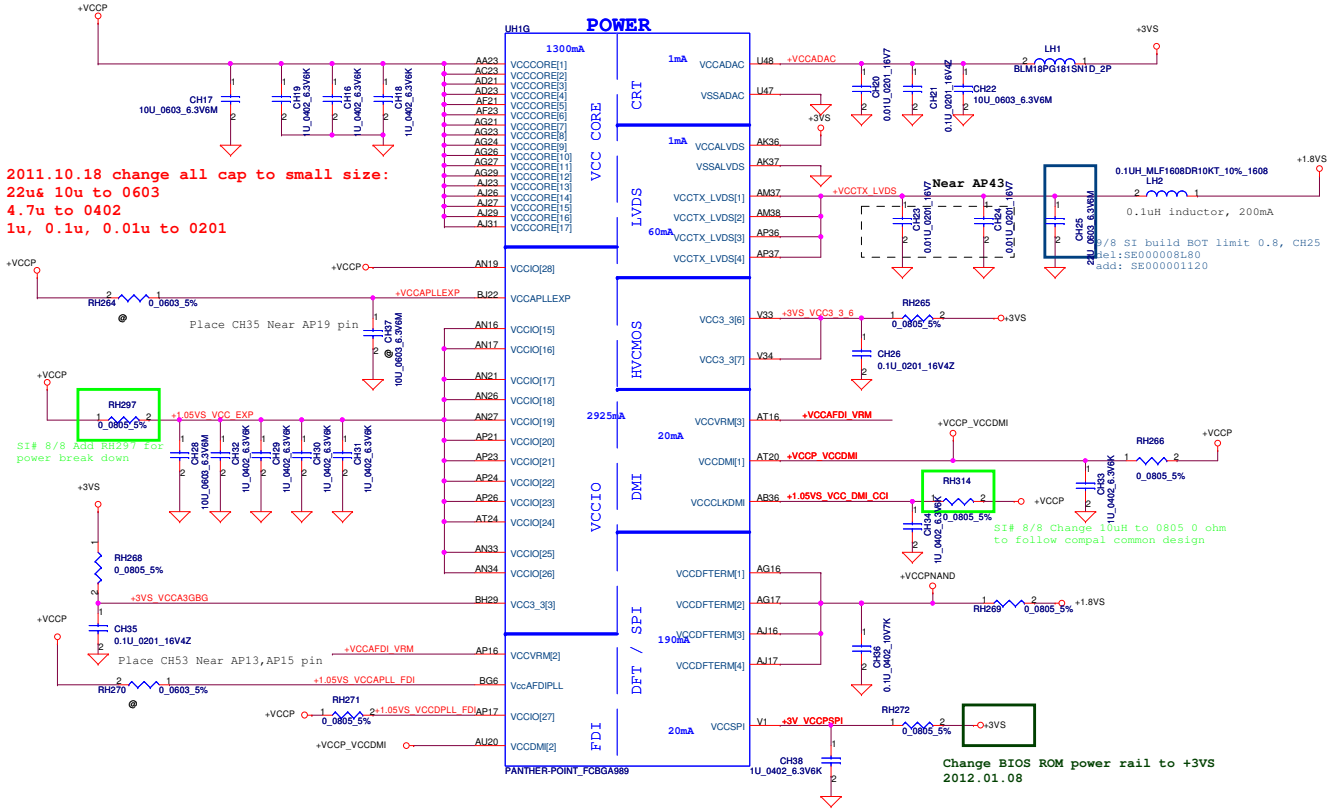
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

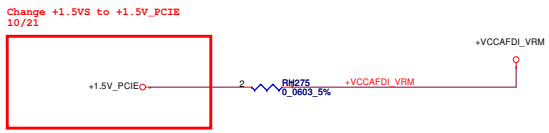
Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: | Document Number: LA-8043P | Rev: 0.1

Date: Saturday, March 03, 2012 | Sheet 18 of 58





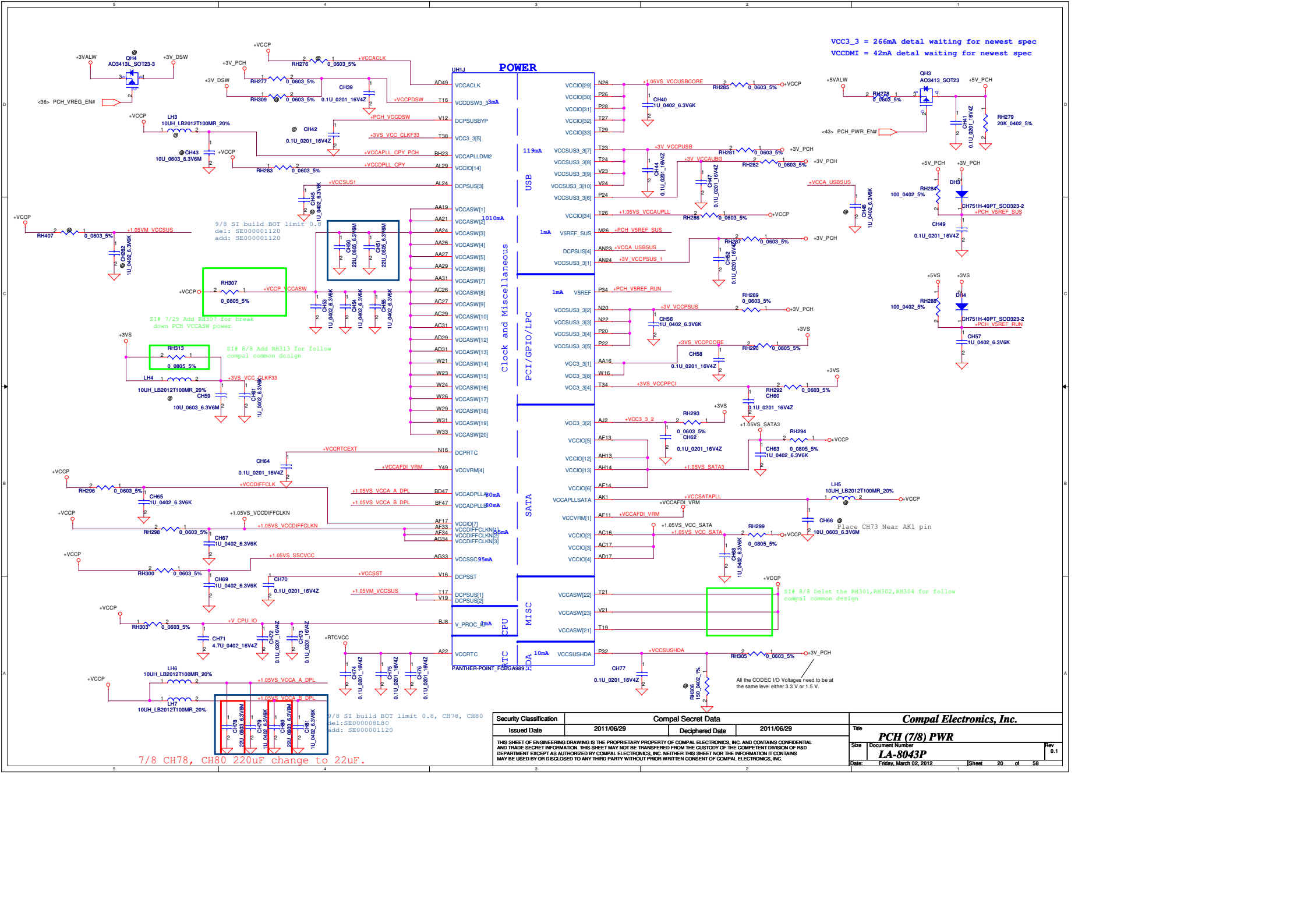
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: | Document Number: LA-8043P | Rev: 0.1

Date: Friday, March 02, 2012 | Sheet 19 of 58


VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec
POWER
UH1J
PANTHER-POINT_FCBGA989
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
HDA
9/8 SI build BOT limit 0.8
del: SE000001120
add: SE000001120
SI# 7/29 Add RH307 for break down PCH VCCASW power
SI# 8/8 Add RH313 for follow compal common design
SI# 8/8 Delet the RH301,RH302,RH304 for follow compal common design
Place CH73 Near AK1 pin
All the CODEC I/O Voltages need to be at the same level either 3.3 V or 1.5 V.
9/8 SI build BOT limit 0.8, CH78, CH80
del:SE000008L80
add: SE000001120
7/8 CH78, CH80 220uF change to 22uF.
Security Classification
Compal Secret Data
Issued Date
2011/06/29
Deciphered Date
2011/06/29
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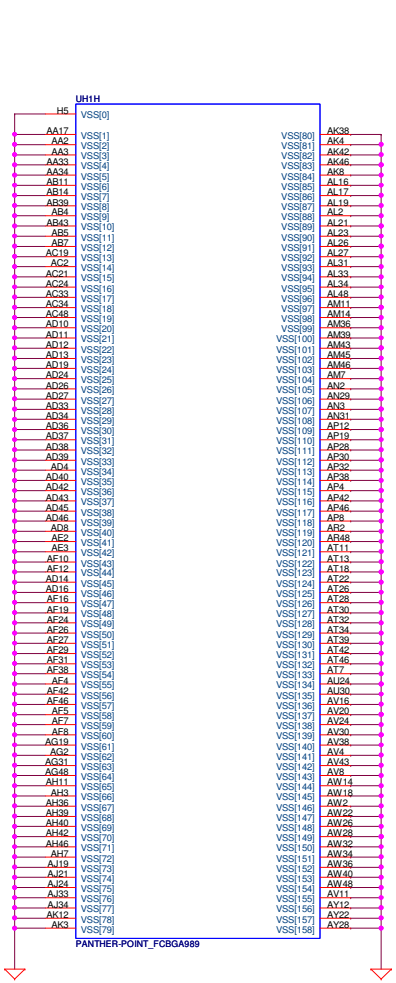
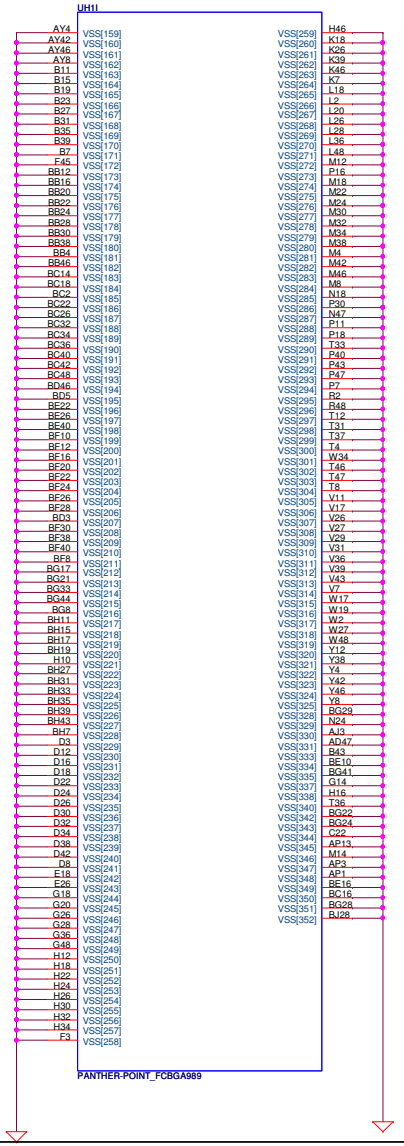
Compal Electronics, Inc.
Title
PCH (7/8) PWR
Size
Document Number
LA-8043P
Rev
0.1
Date: Friday, March 02, 2012
Sheet 20 of 58





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-8043P	0.1

Date: Friday, March 02, 2012 | Sheet 21 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_PCIE/LVDS

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 22 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 23 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_BACO POWER

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 24 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SetmourXT_M2_PWR_GND

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 25 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 26 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 27 of 58

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 28 of 58

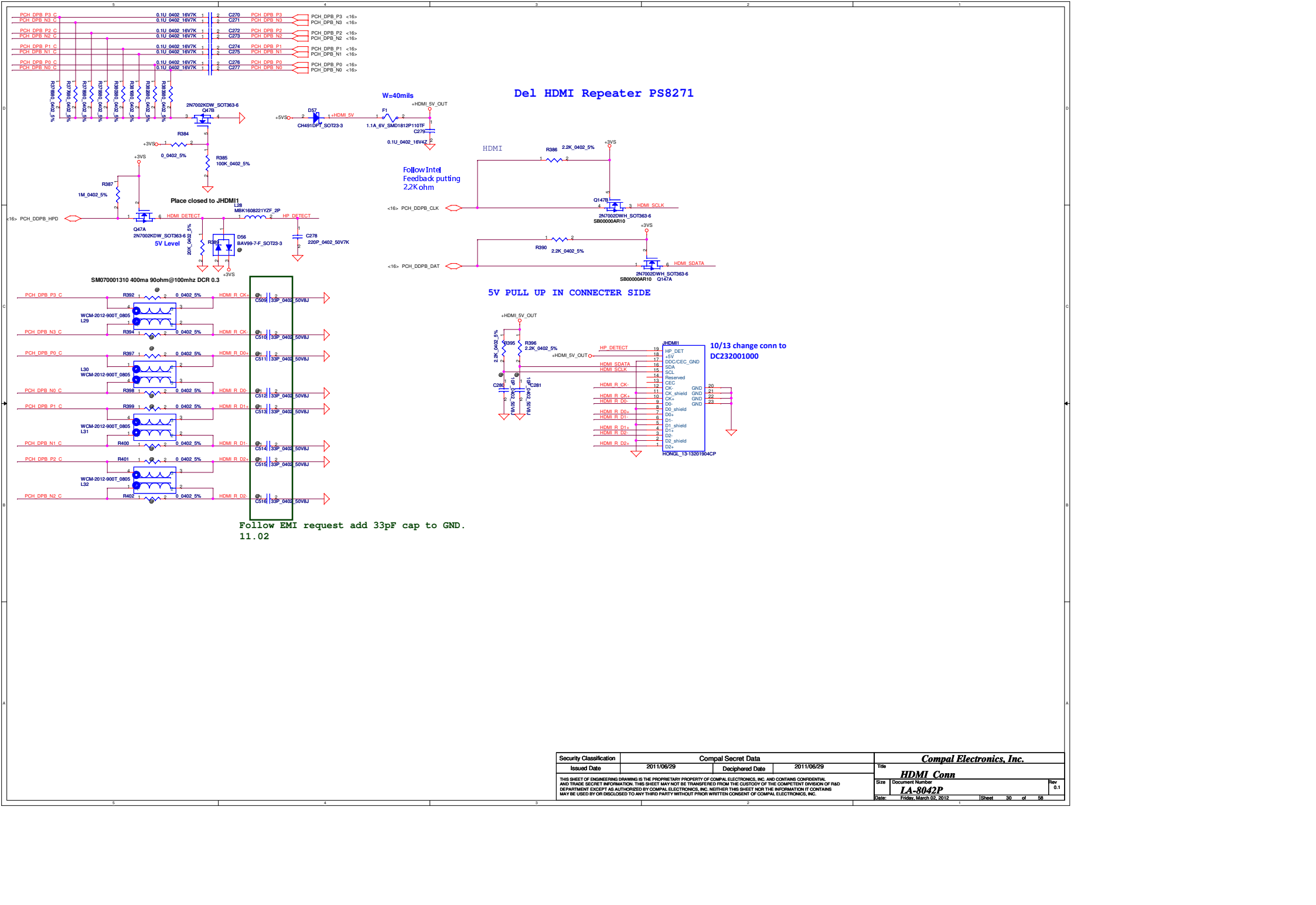
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

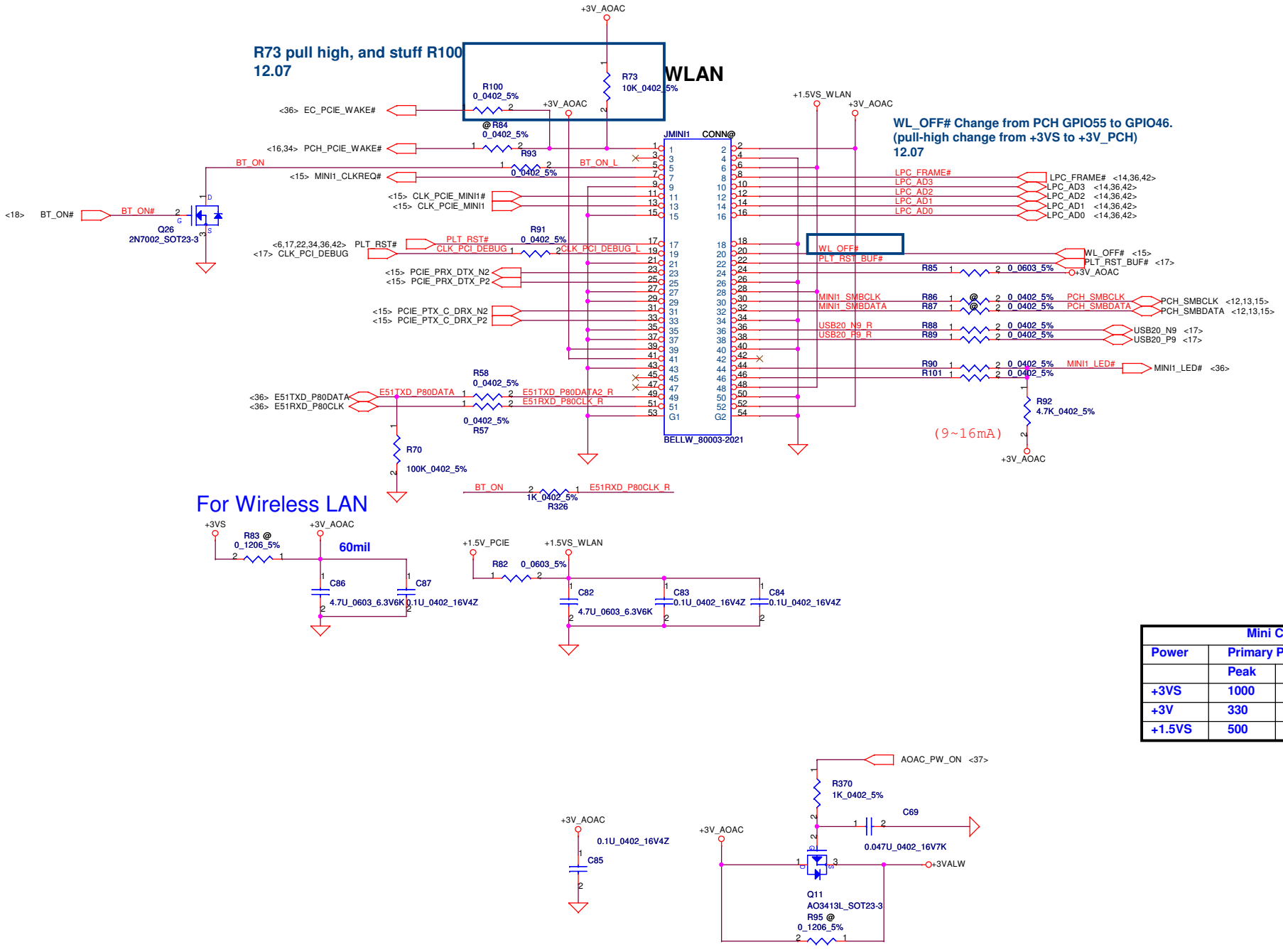
Size	Document Number	Rev
C	LA7691P	0.1

Date: Friday, March 02, 2012 Sheet 29 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title: HDMI Conn			
Size	Document Number: LA-8042P		Rev: 0.1
Date: Friday, March 02, 2012		Sheet 30 of 58	



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title: MiniCard & WLan			
Size	Document Number: LA-8042P		Rev: 0.1
Date: Friday, March 02, 2012	Sheet 31 of 58		

SI# 8/15 R62 change to +3VALW, R61change to 10 ohm, R63 change to 200K ohm

LCD POWER CIRCUIT

+LCDVDD
R61 100_0603_5%
+3VALW
R62 100K_0402_5%
R63 200K_0402_5%
Q6A DMN66D0LDW-7_SOT363-6
C61 0.047U_0402_16V7K
<16> PCH_ENVDD
PCH_ENVDD
Q6B DMN66D0LDW-7_SOT363-6

+3VS
W=60mils
C55 4.7U_0603_6.3V6K
Q7 AO3413L_SOT23-3
+LCDVDD
W=60mils
C63 0.1U_0402_16V4Z
C62 4.7U_0603_6.3V6K

9/8 SI build BOT limit 0.8, CH55
del: SE053475Z80
add: SE107475K80

9/8 SI build BOT limit 0.8, C62
del: SE053475Z80
add: SE107475K80

Place closed to JLVDS1
+3VS
+LCDVDD
C56 0.1U_0402_16V4Z
C57 10U_0603_6.3V6M
C58 0.1U_0402_16V4Z

INVPWR_B+
W=60mils
L7 FBMA-L11-201209-221LMA30T_0805
B+
C59 680P_0402_50V7K
C60 68P_0402_50V8J
SM010014520 3000ma
220ohm@100mhz
DCR 0.04

LCD/LED PANEL Conn.

W=60mils W=60mils

+3VS
R64 2.2K_0402_5% LCD_CLK
R65 2.2K_0402_5% LCD_DATA
@C64 10P_0402_50V8J
@C65 10P_0402_50V8J

C66 220P_0402_50V7K INVTPWM
C67 220P_0402_50V7K DISPOFF#

+3VS& +5VS for touch screen (choose one when getting spec) 12.09

Change to smaller package
01.16

R156 0_0402_5%
L11
<17> USB20_P8
<17> USB20_N8
USB20_P8_R
USB20_N8_R
Part Number = SM070002900
WCM-1210HS-900T_4P
R229 0_0402_5%

Delete INVT_PWM because EC pin 25 need to connect to BATT_TEMPA

<16> DPST_PWM
R197 0_0402_5%
INVTPWM
R72 10K_0402_5%

R157 0_0402_5%
L12
<17> USB20_P10
<17> USB20_N10
USB20_P10_R
USB20_N10_R
<36>
WCM-2012-900T_4P
R230 0_0402_5%

Port 10 for touch screen
12.07

+LCDVDD
+5VS
JLVDS1
<16> PCH_LCD_CLK
<16> PCH_LCD_DATA
PCH_LCD_CLK
R193 0_0402_5% LCD_CLK
R194 0_0402_5% LCD_DATA
USB20_P10_R
USB20_N10_R
BKOFF#
R74 10K_0402_5%
<6> PCH_TXOUT1-
<6> PCH_TXOUT1+
<6> PCH_TXOUT0-
<6> PCH_TXOUT0+
<6> PCH_TXOUT2+
<6> PCH_TXOUT2-
<16> PCH_TXCLK+
<16> PCH_TXCLK-

For easier layout routing
change the pin order 12.08

INVTPWM
BKOFF#
USB20_N8_R
USB20_P8_R
INVPWR_B+
+3VS
<38> D_MIC_CLK
<38> D_MIC_DATA
D_MIC_CLK
D_MIC_DATA
STARC_111H40-100000-G4-R

D8
D_MIC_CLK
D_MIC_DATA
TVNST52302AB0_SOT523-3
Change to SCA00001W00
01.16

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

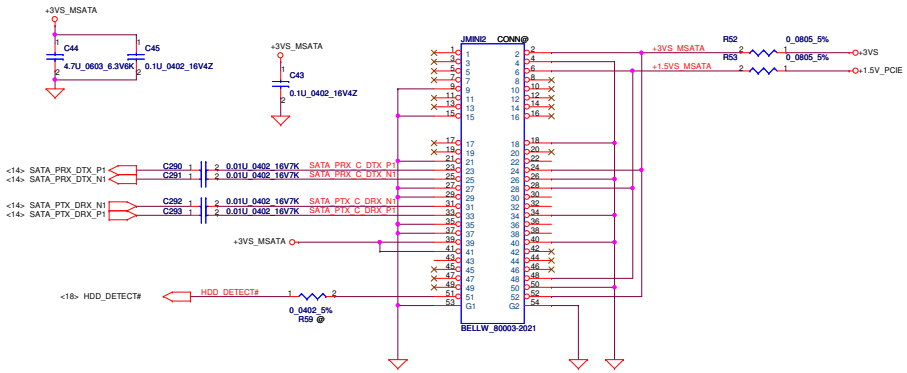
Compal Electronics, Inc.

Title: LVDS Connector

Size | Document Number: LA-8042P | Rev: 0.1

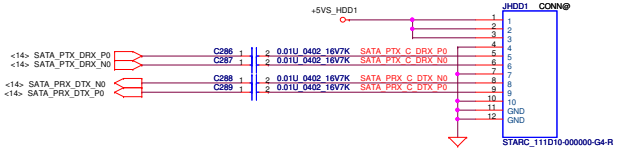
Date: Friday, March 02, 2012 | Sheet 32 of 58

mSATA Conn.

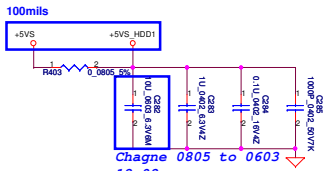


Exchange port 0 & port 1 for SI as customer request
11.30

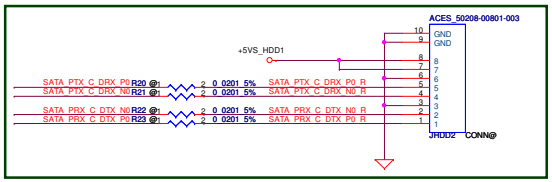
Change footprint to Starconn (PAD is bigger)
11.30



SATA connector



Chagne 0805 to 0603
12.08



Co-layout for wire type connector
01.16
Change connector to ACES_50376
01.31
Change connector to ACES_50208 because current limit issue
02.06

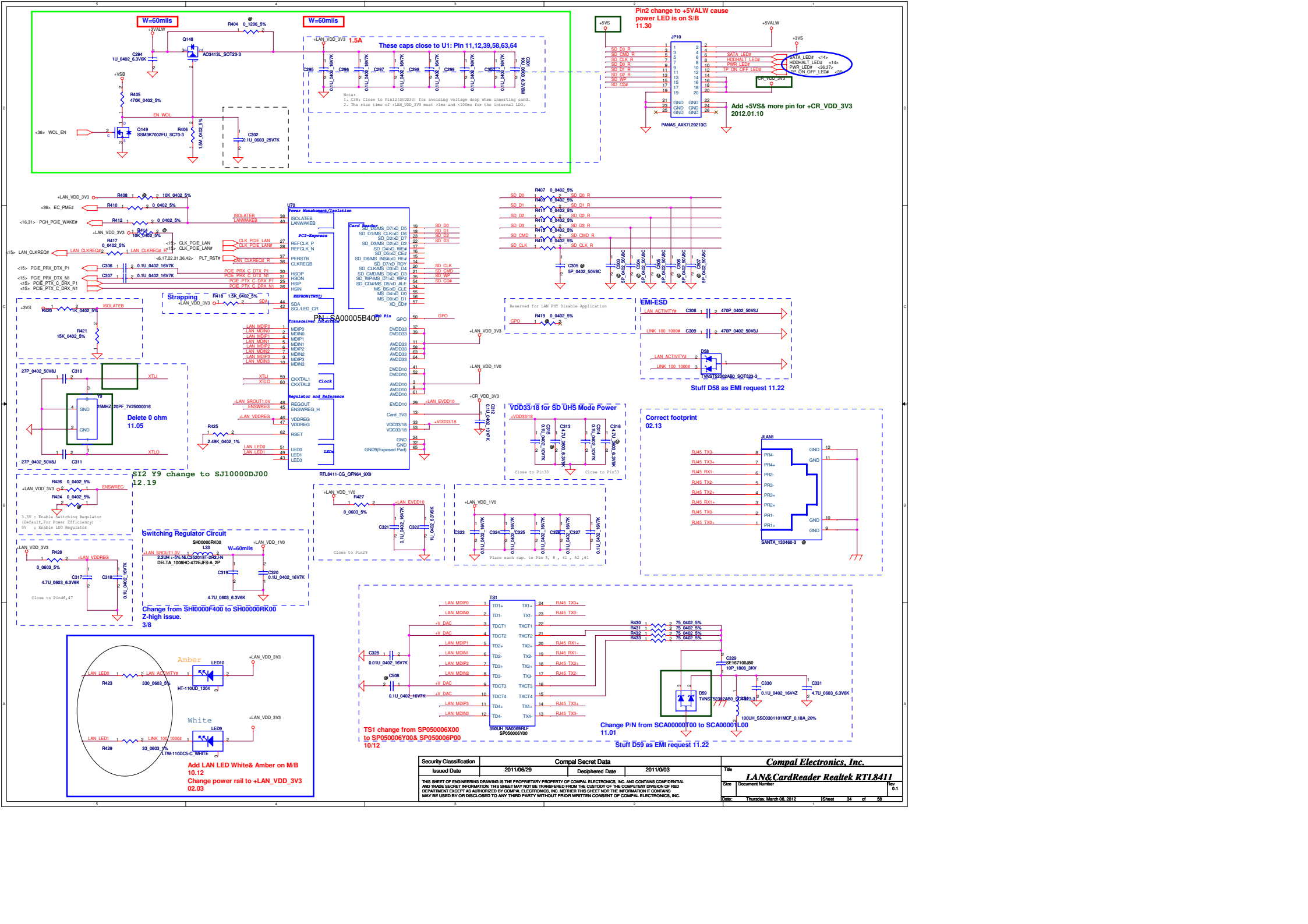
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: mSATA Connector

Size	Document Number	Rev
C	LA-8042P	0.1

Date: Friday, March 02, 2012 Sheet 33 of 58



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/0/03

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Compal Electronics, Inc.

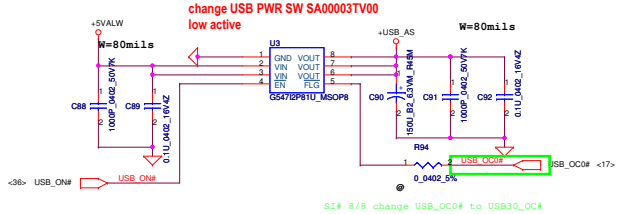
Title: **LAN&CardReader Realtek RTL8411**

Size | Document Number | Rev 0.1

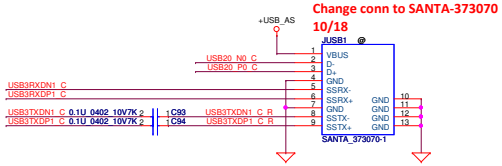
Date: Thursday, March 08, 2012 | Sheet 34 of 58

USB3.0

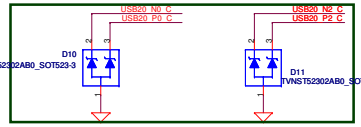
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

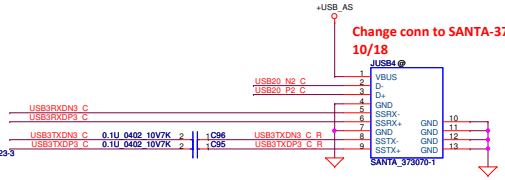


Change conn to SANTA-373070
10/18

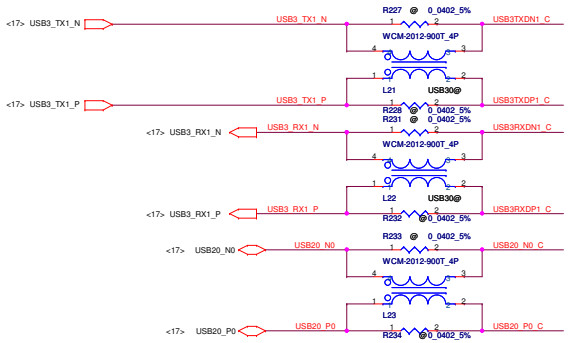


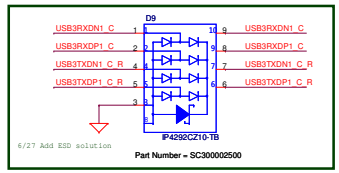
Change P/N from SCA00000T00 to SCA00001L00
11.01
Change P/N to SCA00001W00 for smaller size, 10*10 choke
02.13

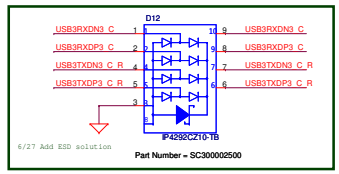


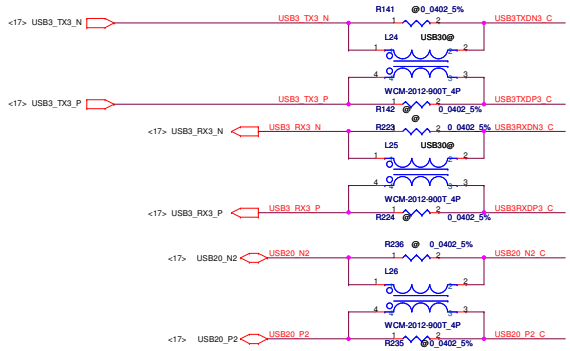


Change conn to SANTA-373070
10/18









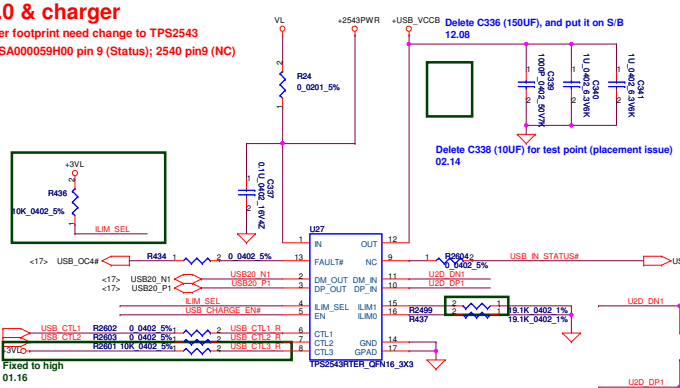
USB2.0 & charger

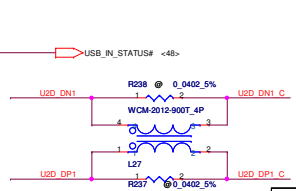
USB charger footprint need change to TPS2543
TPS2543 : SA000059H00 pin 9 (Status); 2540 pin9 (NC)

Delete C336 (150UF), and put it on S/B
12.08

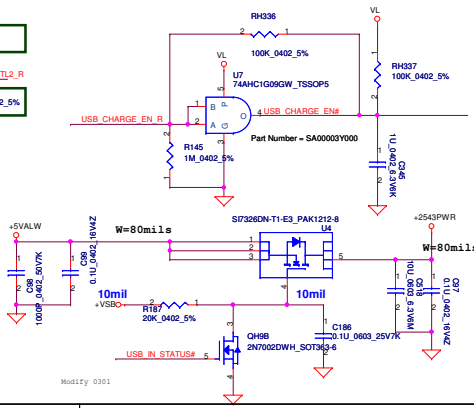
Delete C338 (10UF) for test point (placement issue)
02.14

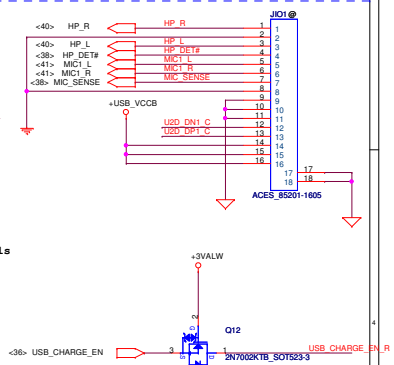
Delete pull-high resistors
01.16





Follow EMI request add choke
11.08





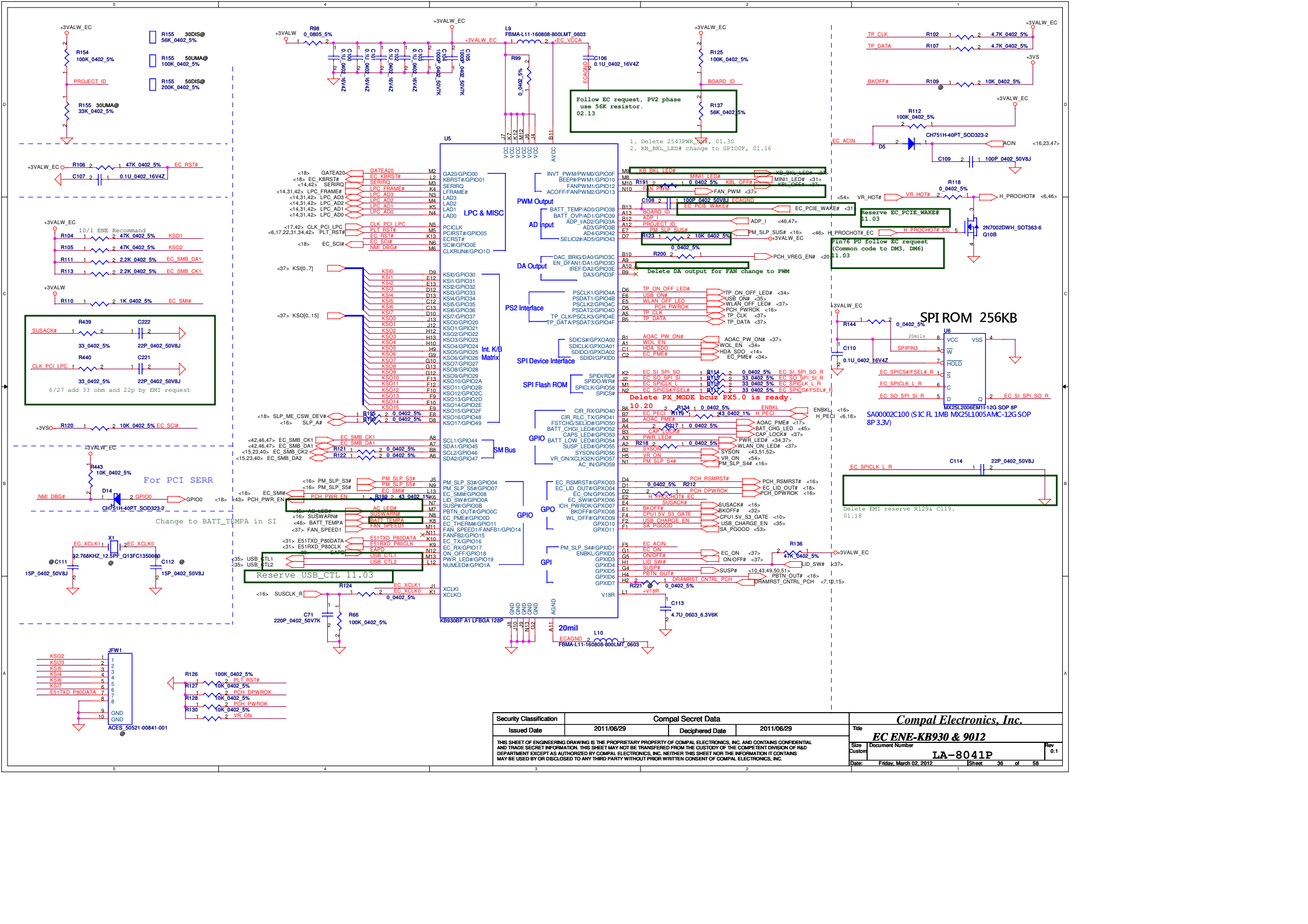
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: USB Con & Daughter Con

Size: C | Document Number | Rev: 0.1

Date: Monday, March 05, 2012 | Sheet 35 of 58


U5
KB930BF A1 LFBGA 128P
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
SPI ROM 256KB
SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)
Follow EC request, PV2 phase use 56K resistor. 02.13
1. Delete 2543PWR_GATE, 01.30
2. KB_BKL_LED# change to GPIO0F, 01.16
Reserve EC_PCIE_WAKE# 11.03
Pin76 PU follow EC request (Common code to DM3, DM6) 11.03
Delete DA output for FAN change to PWM
Delete PX_MODE bcuz PX5.0 is ready. 10.20
Delete EMI reserve R129& C119. 01.18
Change to BATT_TEMPA in SI
For PCI SERR
Reserve USB_CTL 11.03
6/27 add 33 ohm and 22p by EMI request
10/1 ENE Recommand
20mil
Security Classification
Compal Secret Data
Issued Date
2011/06/29
Deciphered Date
2011/06/29
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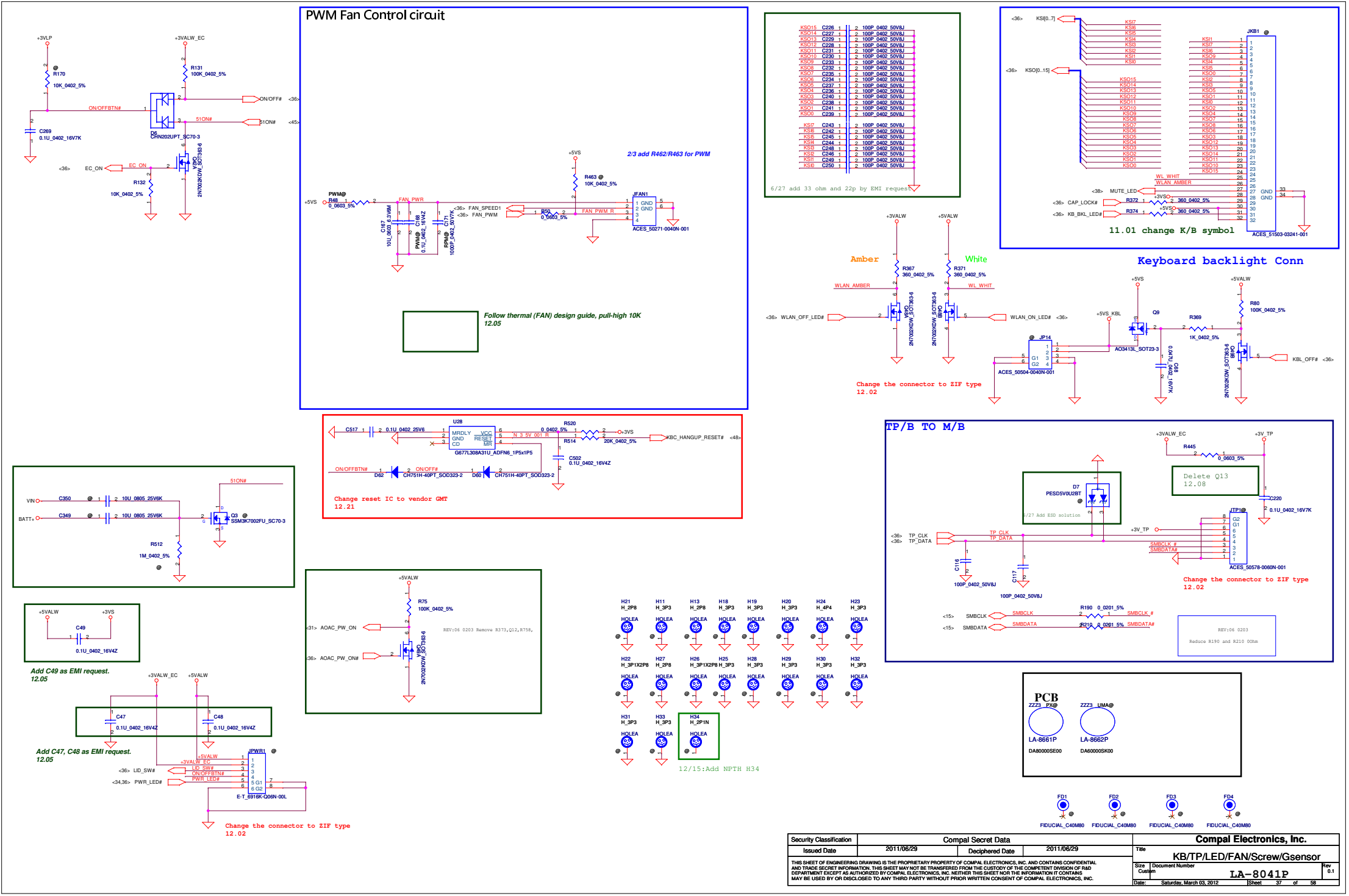
Compal Electronics, Inc.
Title
EC ENE-KB930 & 9012
Size
Custom
Document Number
LA-8041P
Rev
0.1
Date:
Friday, March 02, 2012
Sheet
36
of
58


PWM Fan Control circuit
2/3 add R462/R463 for PWM
Follow thermal (FAN) design guide, pull-high 10K
12.05
6/27 add 33 ohm and 22p by EMI request
11.01 change K/B symbol
Keyboard backlight Conn
Amber
White
Change the connector to ZIF type
12.02
Change reset IC to vendor GMT
12.21
TP/B TO M/B
Delete Q13
12.08
Change the connector to ZIF type
12.02
Add C49 as EMI request.
12.05
Add C47, C48 as EMI request.
12.05
Change the connector to ZIF type
12.02
12/15:Add NPTH H34
PCB
LA-8661P
LA-8662P
Security Classification
Compal Secret Data
Issued Date
2011/06/29
Deciphered Date
2011/06/29
Compal Electronics, Inc.
KB/TP/LED/FAN/Screw/Gsensor
LA-8041P
Rev 0.1
Saturday, March 03, 2012
Sheet 37 of 58

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Place AVDD ,PVDD,and DVDD capacitor close to Codec

Follow EMI request, reserve cap.
11.03

Correct CA508 circuitry.
12.05

Place C208 close to Codec

Place C209,C210,CA87,CA89 close to Codec

Follow EMI request, reserve cap.
11.03

SB Beep

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

PLACE CLOSE TO U1 PIN 14

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

HP Jack

Ext MIC

Internal SPKR(front stereo speaker)

9/27 LDO TPS793475DBVR for audio power

Change UA2 P/N to SA00005J000 just for HP project.
02.06

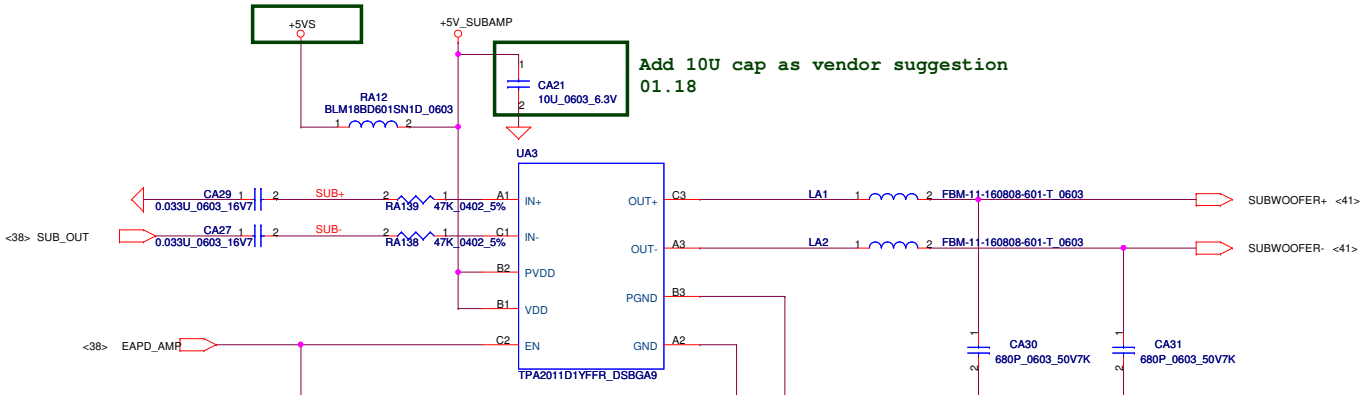
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

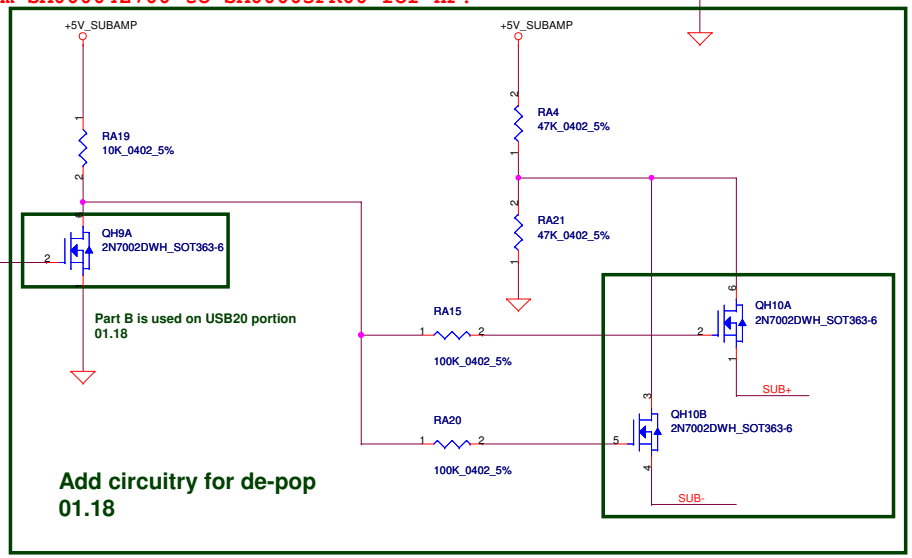
Compal Electronics, Inc.

Title: Audio IDT 92HD91

Size	Document Number	Rev
Custom		0.1

Date: Friday, March 02, 2012 Sheet 38 of 58





QH10 must change to BJT before SMT
(Footprint is compatible from BJT& MOTFET)
01.18
BJT P/N: SB00000VH00

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

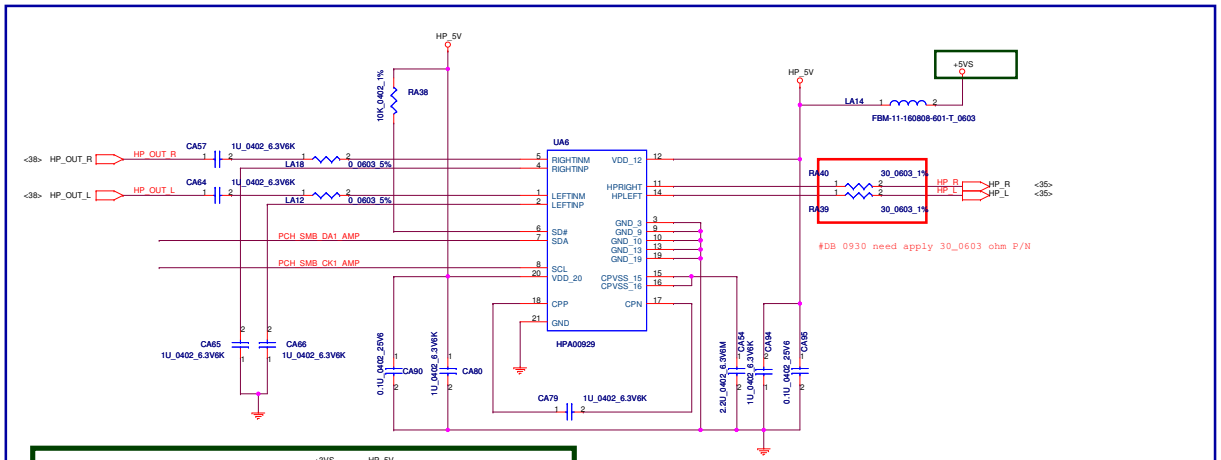
Compal Electronics, Inc.

Title: Audio Woofer Amplifier

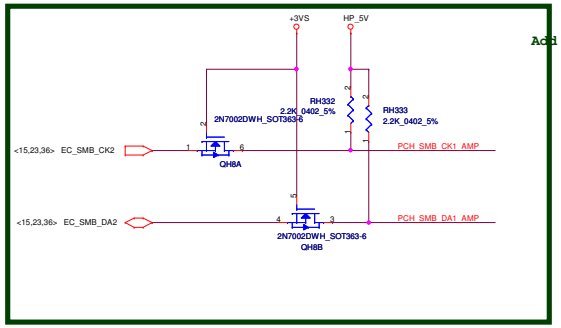
Size	Document Number	Rev
B		0.1

Date: Friday, March 02, 2012 Sheet 39 of 58

Headphone amplifier



Add level shift 11.06



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

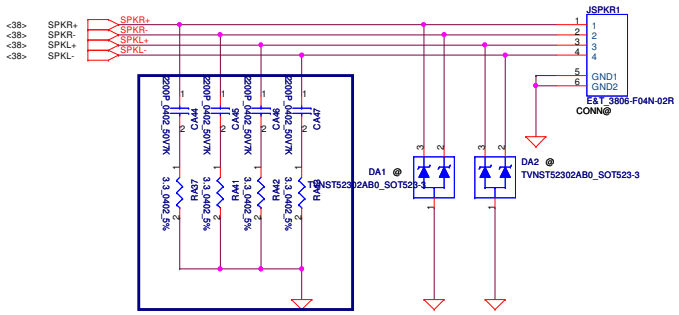
Compal Electronics, Inc.

Title: Audio SPK/HP Amplifier

Size: Custom | Document Number | Rev: 0.1

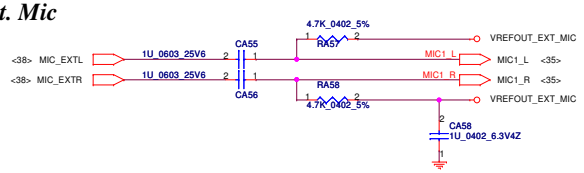
Date: Wednesday, March 07, 2012 | Sheet 40 of 58

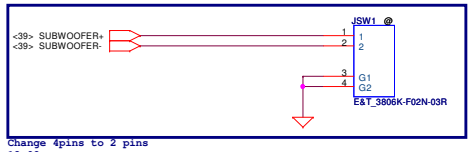
Front Speaker Connector 1



Need place rear Audio Codec (UA5)

Ext. Mic





Change 4pins to 2 pins
12.08

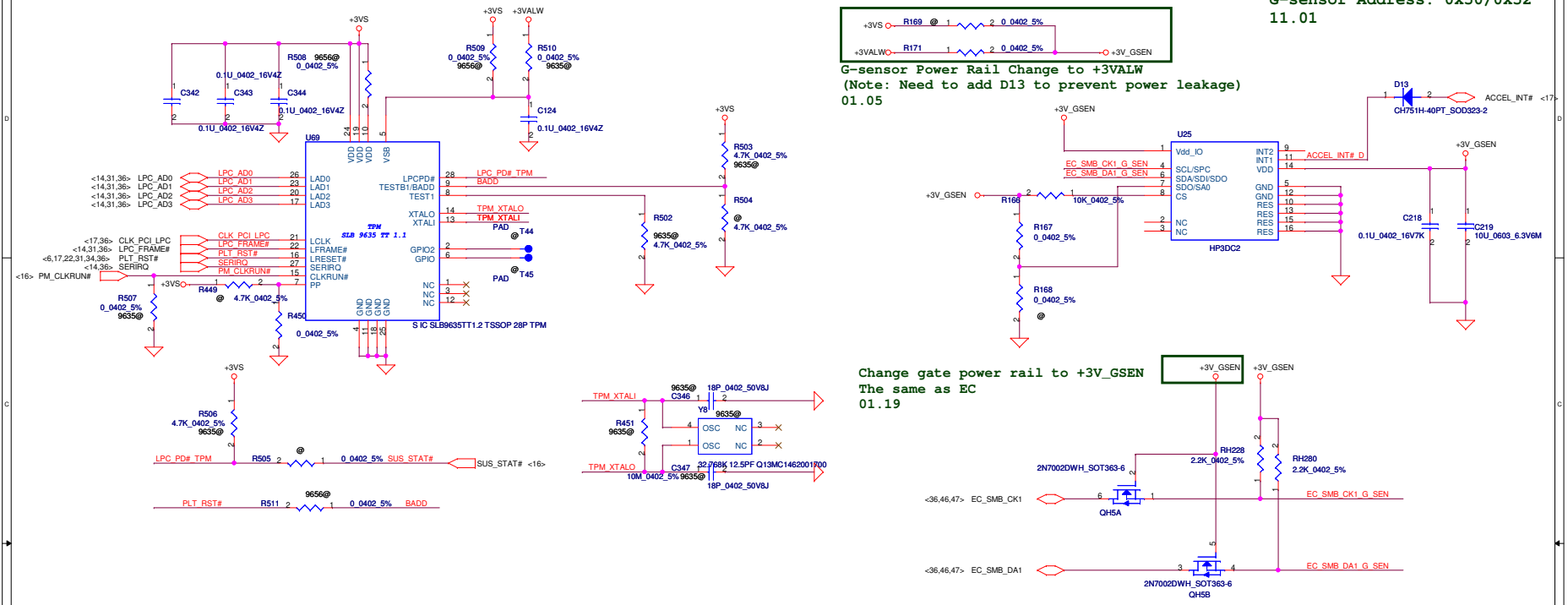
Security Classification	Compal Secret Data		
Issued Date	2009/04/07	Deciphered Date	2012/10/21

Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

Size	Document Number	Rev
Custom	PAV10	0.1

Date: Friday, March 02, 2012 | Sheet 41 of 58



G-sensor Address: 0x50/0x52
11.01

G-sensor Power Rail Change to +3VALW
(Note: Need to add D13 to prevent power leakage)
01.05

Change gate power rail to +3V_GSEN
The same as EC
01.19

Security Classification	Compal Secret Data		
Issued Date	2006/09/25	Deciphered Date	2006/09/25

Compal Electronics, Inc.

Title: **TCG/BIOS ROM/PS2/LED/SW**

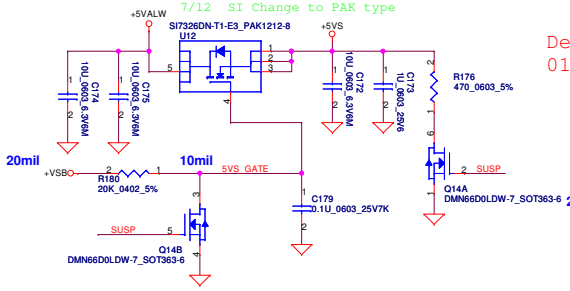
Size	Document Number	Rev
	LA3262P_DIS__M64	0.1

Date: Wednesday, March 07, 2012 | Sheet 42 of 58

10.21 Change to PAK type

+5VALW TO +5VS

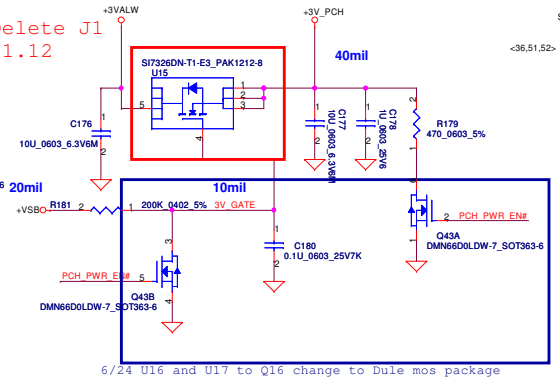
7/12 SI Change to PAK type



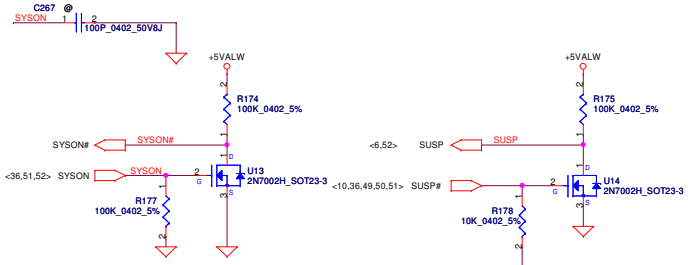
+3VALW TO +3VALW(PCH AUX Power)

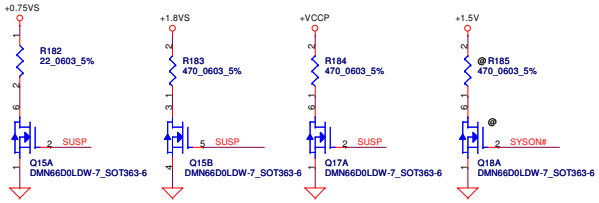
Short J1 for PCH VCCSUS3.3

Delete J1 01.12

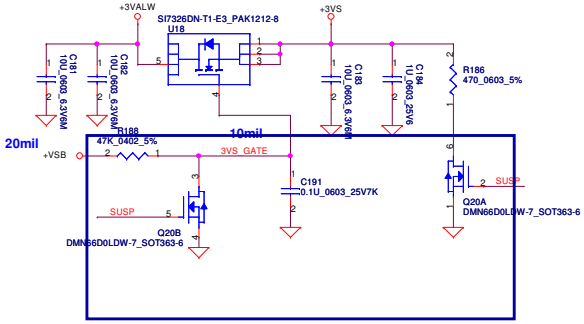


6/24 U16 and U17 to Q16 change to Dule mos package

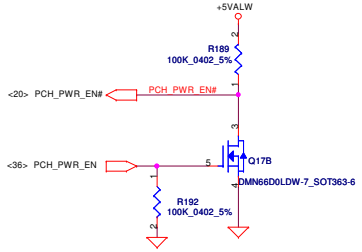




+3VALW TO +3VS



6/24 Q20 and Q21 to Q20 change to Dule mos package



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-8661P	0.1

Date: Friday, March 02, 2012 Sheet 43 of 58

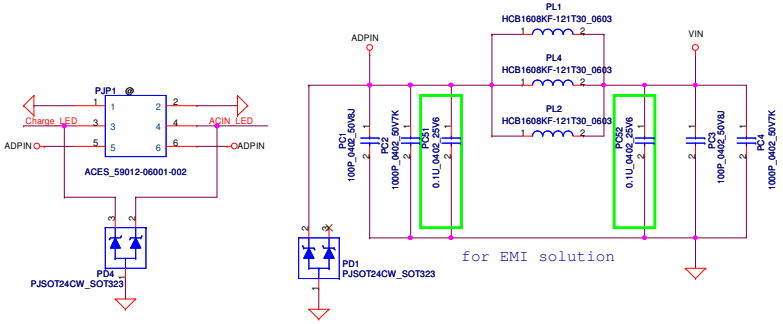
	QAZ60 Strap pin Table		@:un_install	
	Netname	setting	BOM config	
CPU	CFG2	1	RC40 @	1: Normal Operation; Lane # definition matchessocket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @	1 : Disabled; No Physical Display Portattached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @	H : Integrated VRM enable L : Integrated VRM disable
	HDA_SPKR	L	RH139 @	H:No Reboot L:Default
	HDA_SYNC	H	RH149	This signal has a weak internal pull-downOn Die PLL VR is supplied by H:1.5V when smapled high L:1.8V when sampled low Needs to be pulled High for Huron River platfrom
	HDA_SDOUT	L	RH140 @	ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @	On Die DSW VR Enable H : Enable L : Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @	On-Die PLL Voltage Regulator This signal has a weak internal pull up H : On-Die voltage regulator enable L : On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246	FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
	GPIO27	H	RH250 @	PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable

Compal Electronics, Inc.

Title: Strap pin table

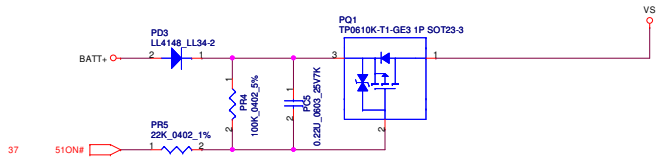
Size: Custom | Document Number: LA-8041P | Rev: 0.1

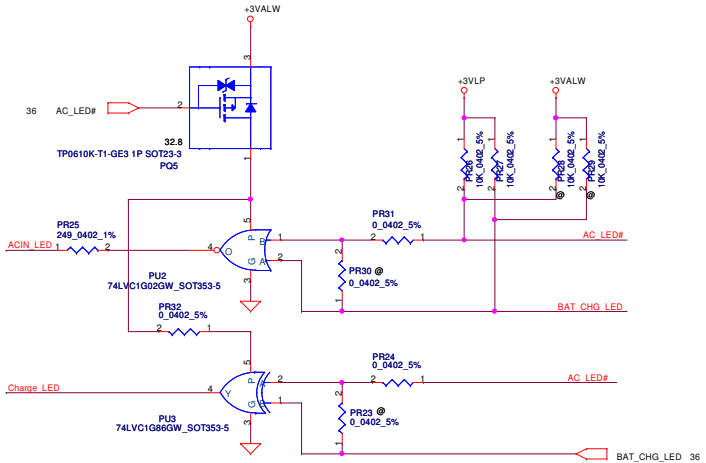
Date: Friday, March 02, 2012 | Sheet 44 of 58



ESD diode : SCA00001G00

KBC output		Input to Battery		
AC_LED#	BAT_CHG_LED	ACIN_LED	Charge_LED	LED Status
0	0	1	0	White LED light
0	1	0	1	Amber LED light
1	0	0	0	X (don't care)
1	1	0	0	X (don't care)





Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

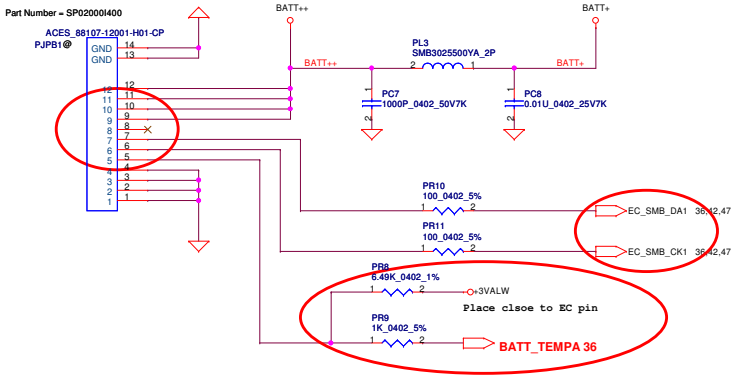
Compal Electronics, Inc.

Title: PWR- DCIN / Vin Detector

Size	Document Number	Rev
Custom	LA-8551P	0.1

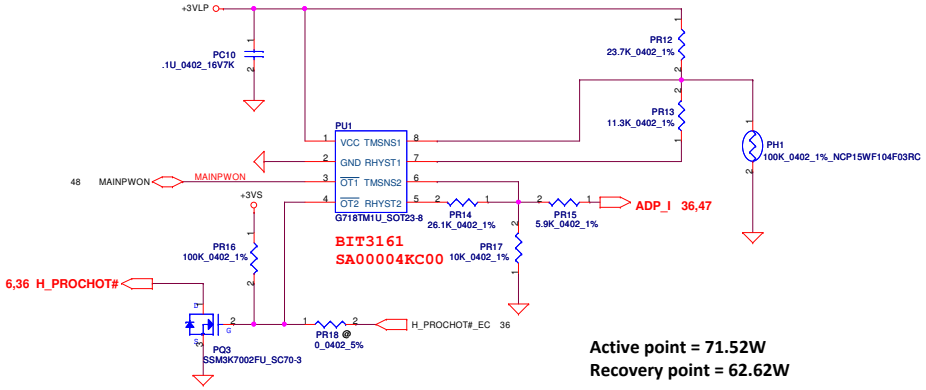
Date: Saturday, March 03, 2012 Sheet 45 of 59

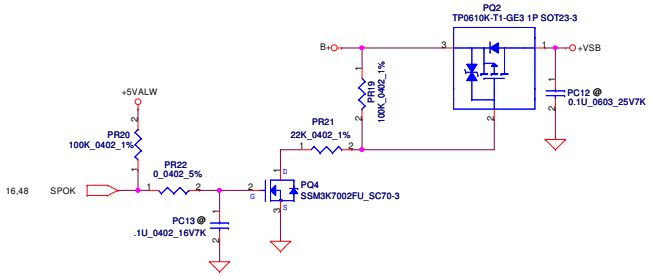
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)



PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)
Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K





Active point = 71.52W
Recovery point = 62.62W

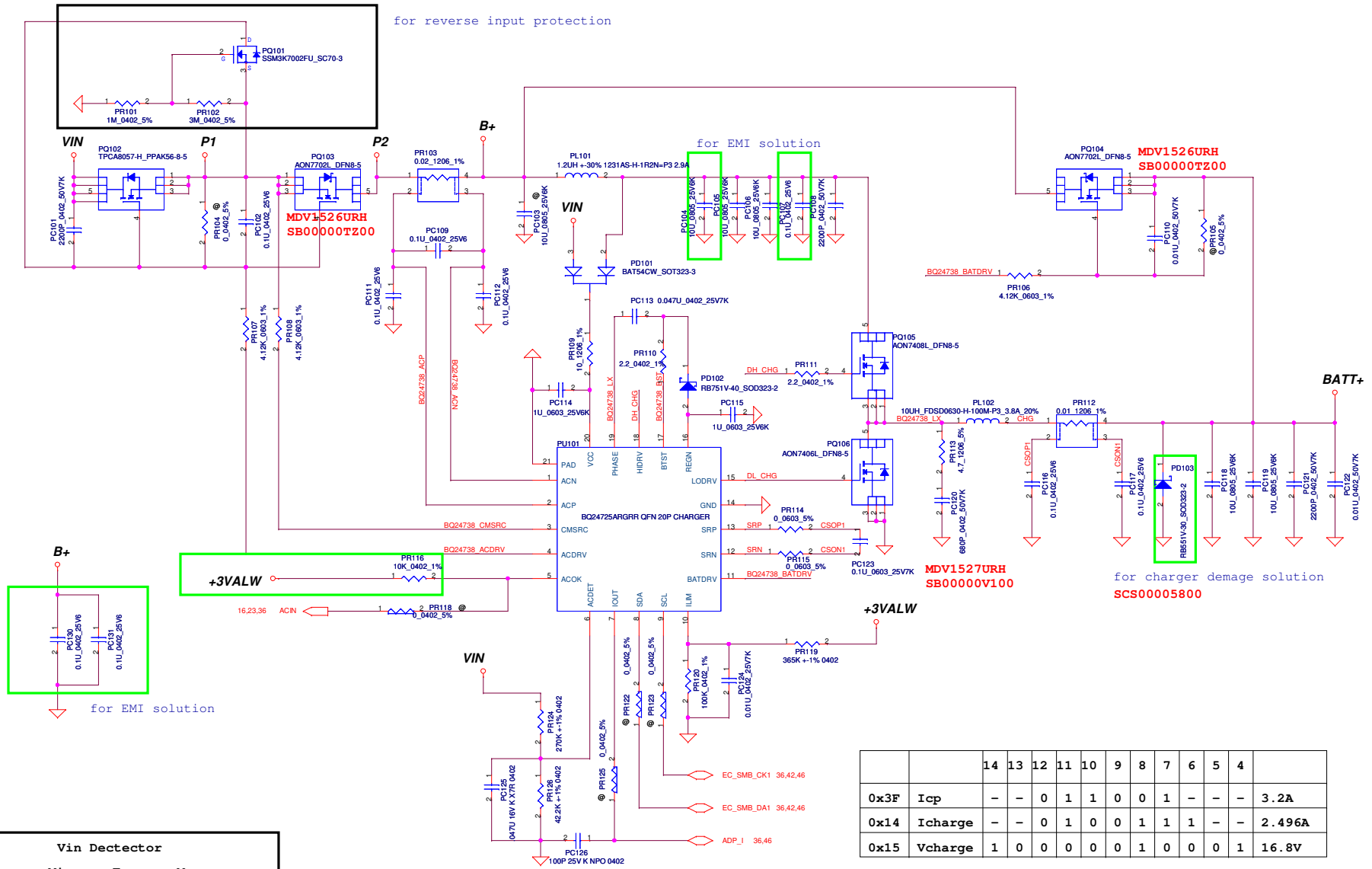
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- BATTERY CONN

Size	Document Number	Rev
Custom	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 46 of 59



		14	13	12	11	10	9	8	7	6	5	4	
0x3F	Icp	-	-	0	1	1	0	0	1	-	-	-	3.2A
0x14	Icharge	-	-	0	1	0	0	1	1	1	-	-	2.496A
0x15	Vcharge	1	0	0	0	0	0	1	0	0	0	1	16.8V

Vin Dectector

	Min.	Typ.	Max.
L-->H	17.45V	17.92V	18.42V
H-->L	16.89V	17.52V	18.16V

ILIM and external DPM
3.54A

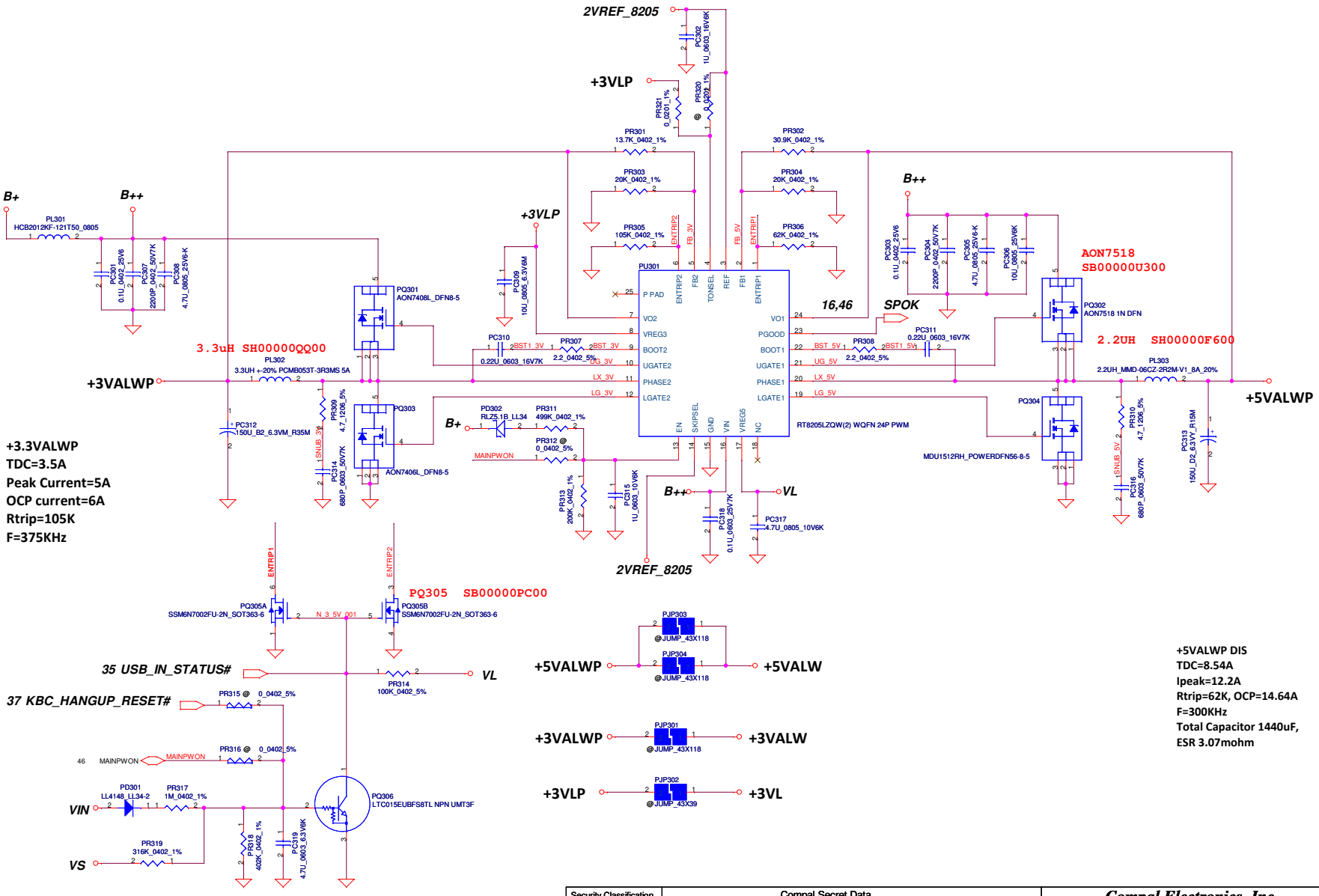
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- CHARGER

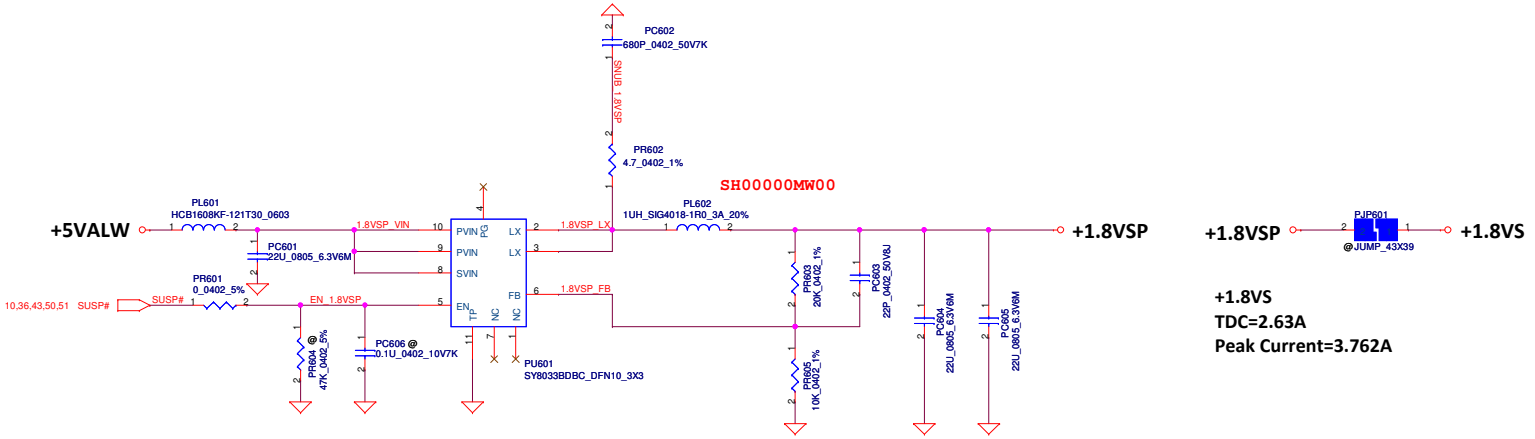
Size	Document Number	Rev
	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 47 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- 3VALWP/5VALWP		
Size: Custom	Document Number: LA-8551P		Rev: 0.1
Date: Saturday, March 03, 2012	Sheet 48 of 59		



+1.8VS
TDC=2.63A
Peak Current=3.762A

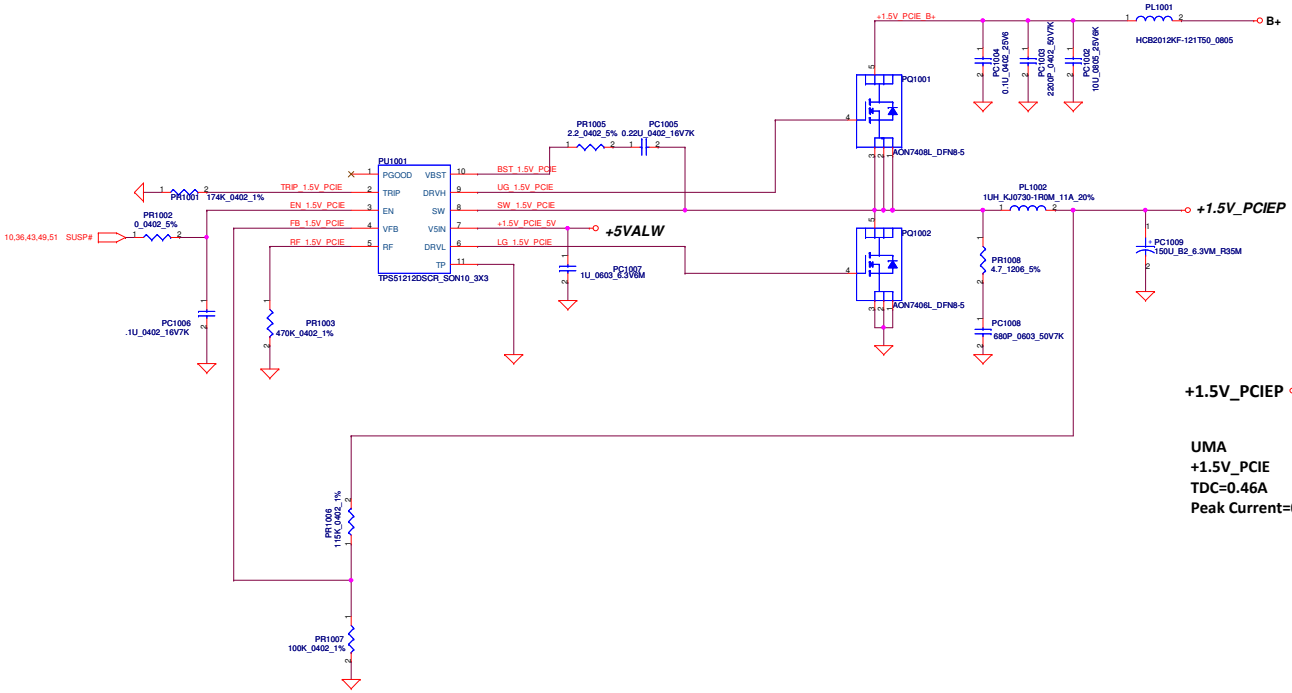
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: **PWR- 1.8VS**

Size	Document Number	Rev
	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 49 of 59



+1.5V_PCIEP — PJP1001 JUMP_43X118 — +1.5V_PCIE

UMA	DIS
+1.5V_PCIE	+1.5V_PCIE
TDC=0.46A	TDC=6A
Peak Current=0.66A	Peak Current=8A

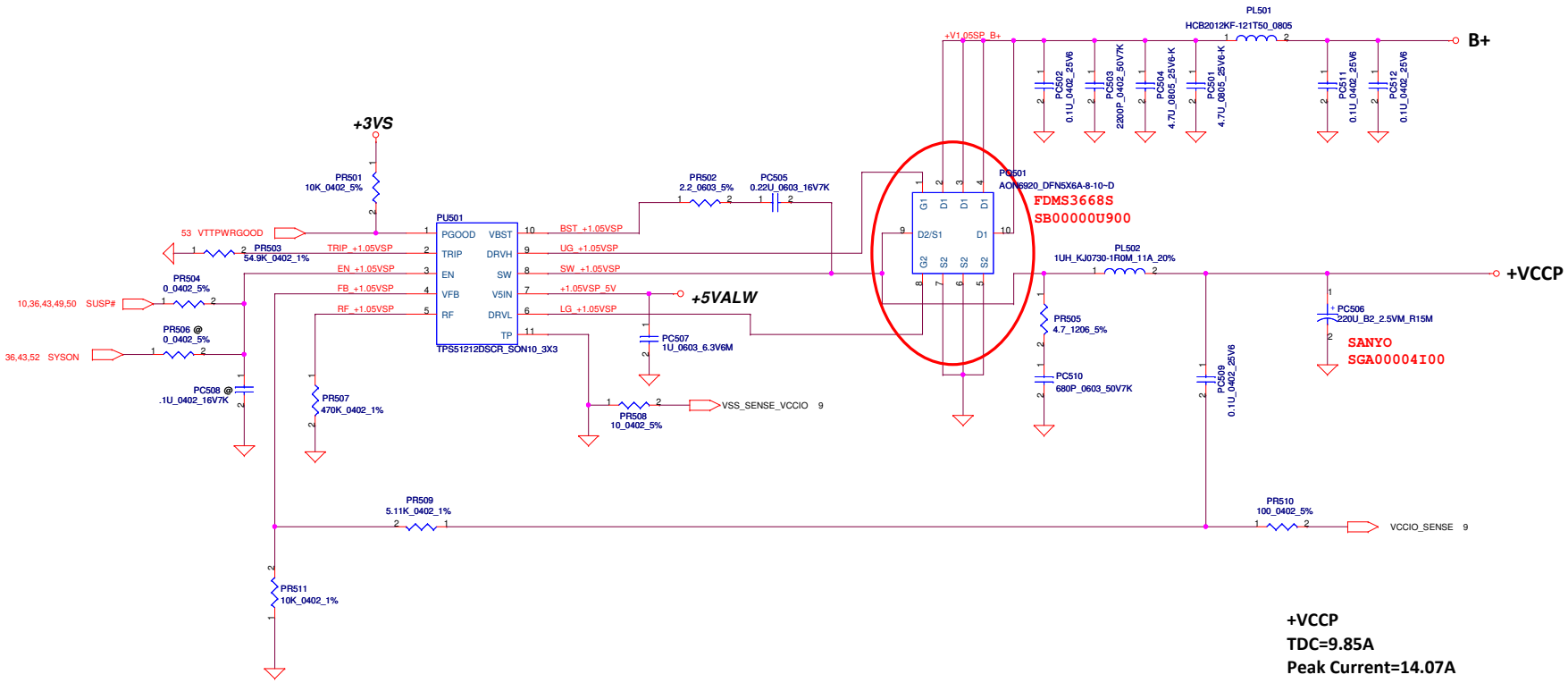
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- VGA_VDDC

Size	Document Number	Rev
C	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 50 of 59



+VCCP
TDC=9.85A
Peak Current=14.07A
OCP current=16.88A
Rtrip = 54.9K

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

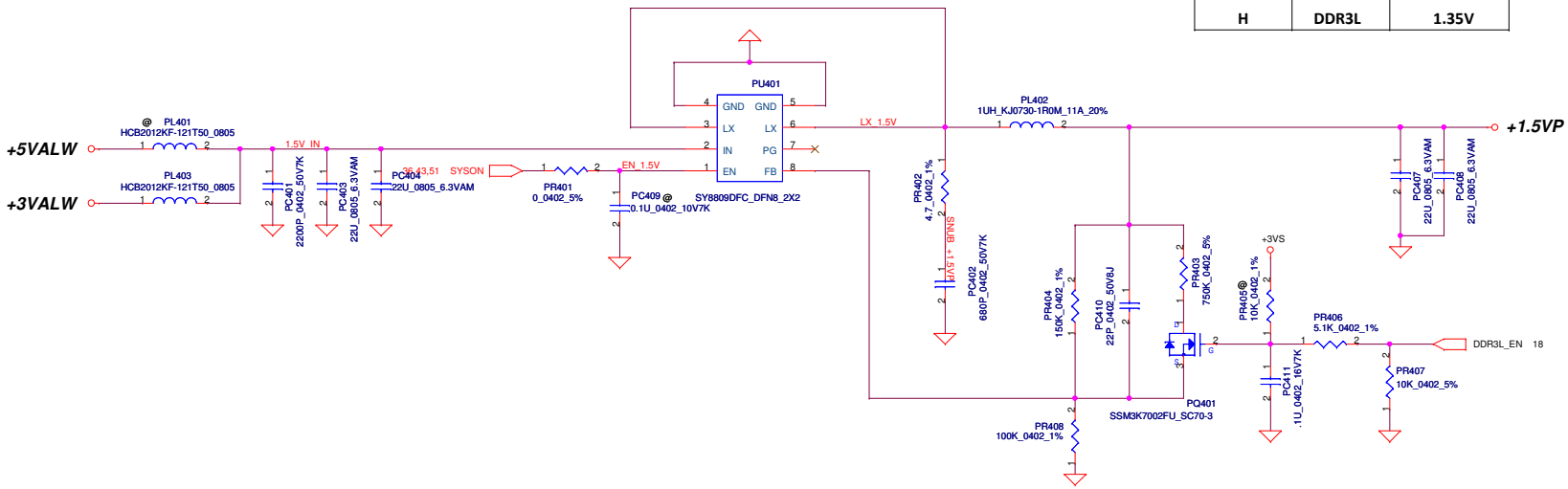
Compal Electronics, Inc.

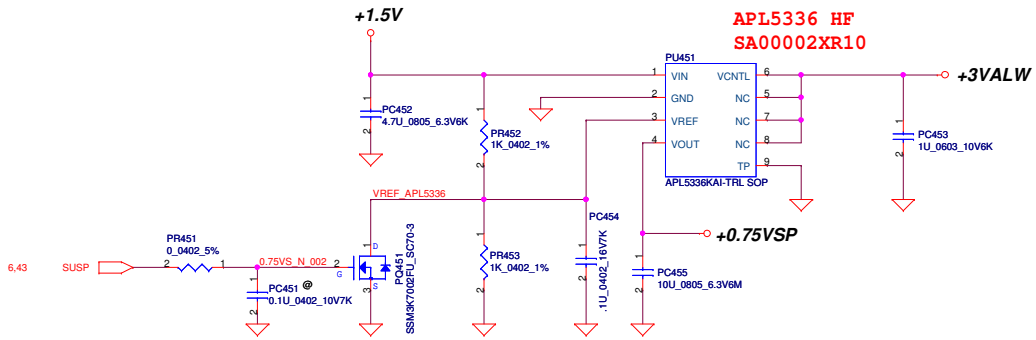
Title: **PWR- VCCP**

Size	Document Number	Rev
Custom	LA-8551P	0.1

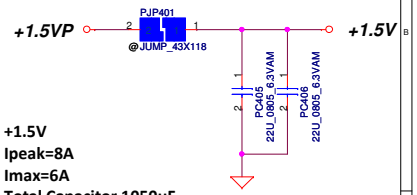
Date: Saturday, March 03, 2012 | Sheet 51 of 59

DDR3L_EN		1.5VP
L	DDR3	1.5V
H	DDR3L	1.35V





+0.75VSP
TDC=1.4A
Peak Current=2A



+1.5V
Ipeak=8A
Imax=6A
Total Capacitor 1050uF,
ESR 4.43mohm

HW side:
C106 330uF 17m
C218 390uF 10m
VGA@ CV122 390uF 10m
@ C189 330uF 15m

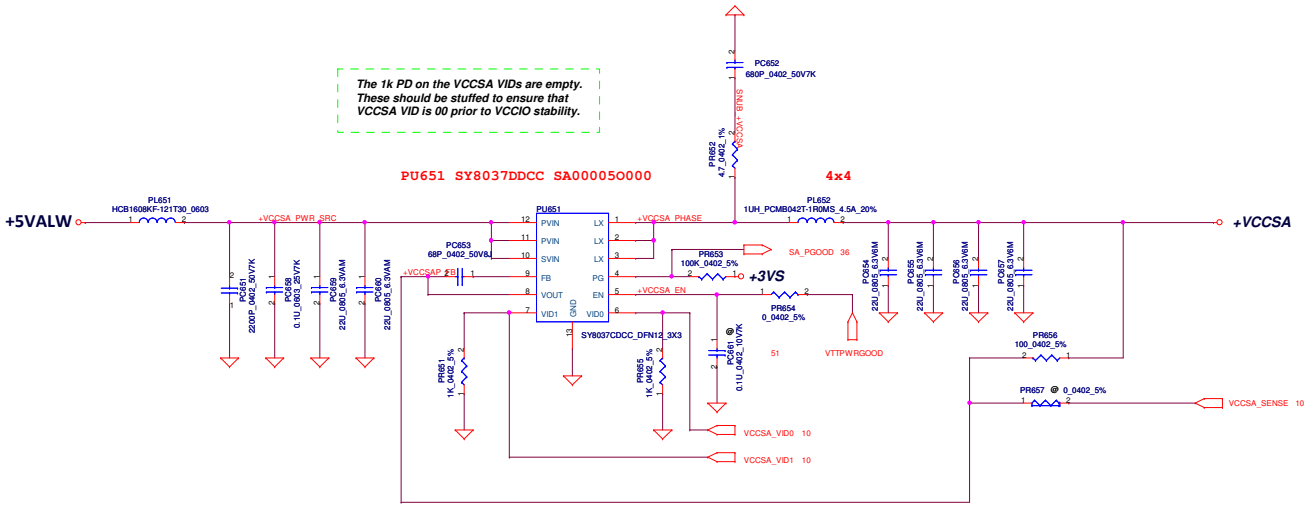
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- 1.5VP/0.75VSP

Size	Document Number	Rev
Custom	LA-8551P	0.1

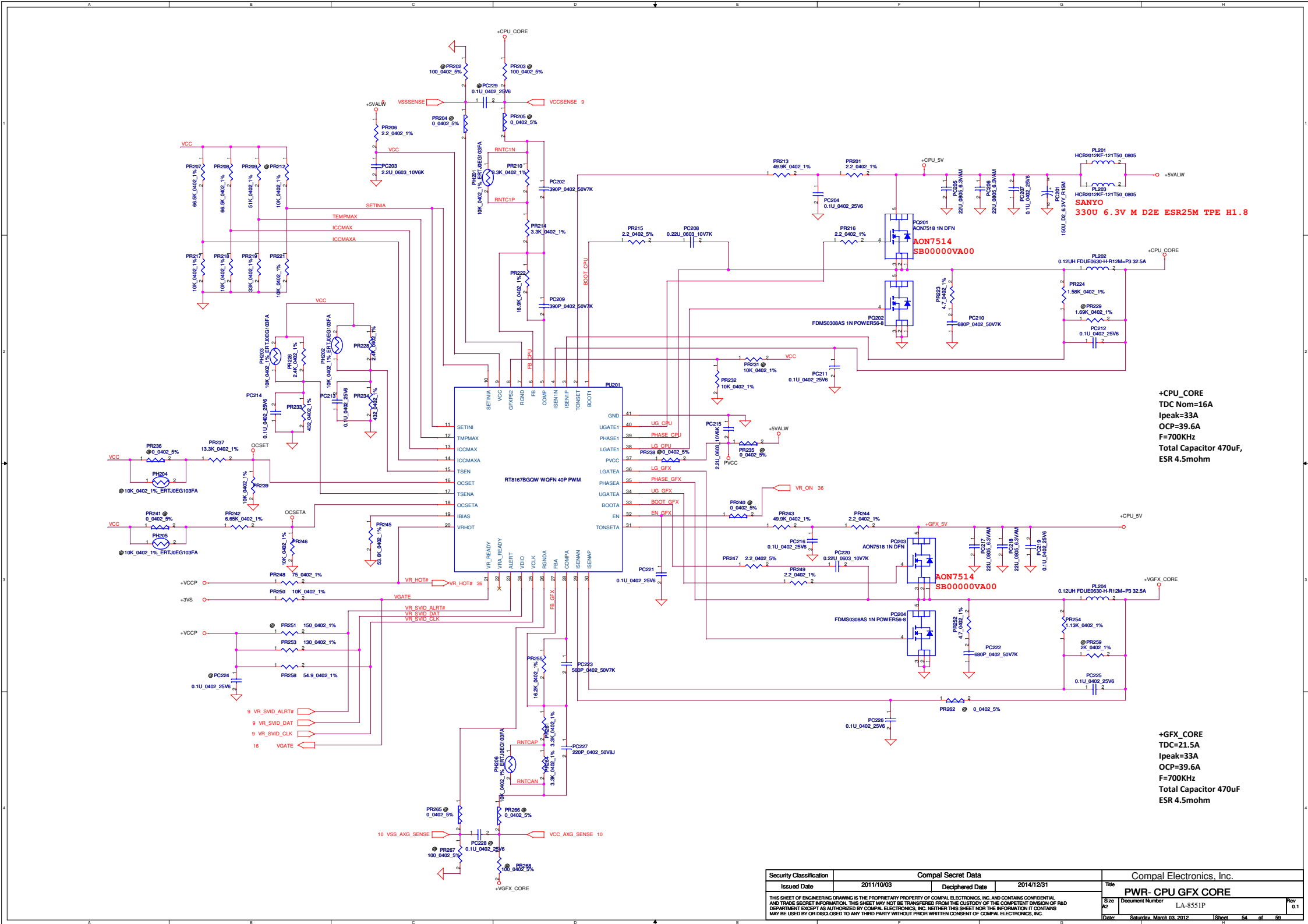
Date: Saturday, March 03, 2012 Sheet 52 of 59



+VCCSA
Itdc=3A
Imax=4A

Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- VCCSA		
Size C	Document Number LA-8551P		Rev 0.1
Date: Saturday, March 03, 2012	Sheet 53 of 59		



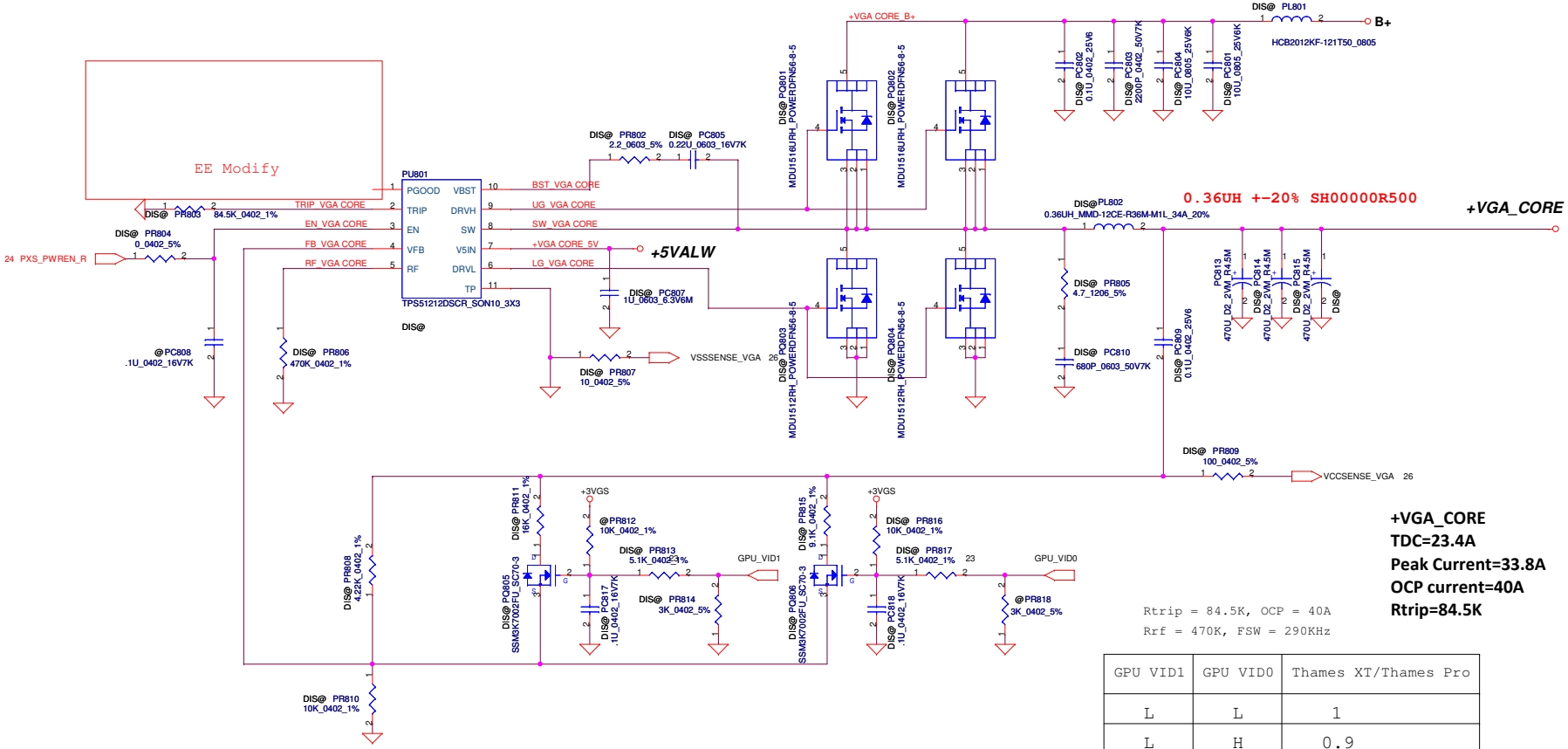
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- CPU GFX CORE

Size	Document Number	Rev
A2	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 54 of 59



Rtrip = 84.5K, OCP = 40A
Rrf = 470K, FSW = 290KHz

+VGA_CORE
TDC=23.4A
Peak Current=33.8A
OCP current=40A
Rtrip=84.5K

GPU VID1	GPU VID0	Thames XT/Thames Pro
L	L	1
L	H	0.9
H	L	0.94
H	H	0.875

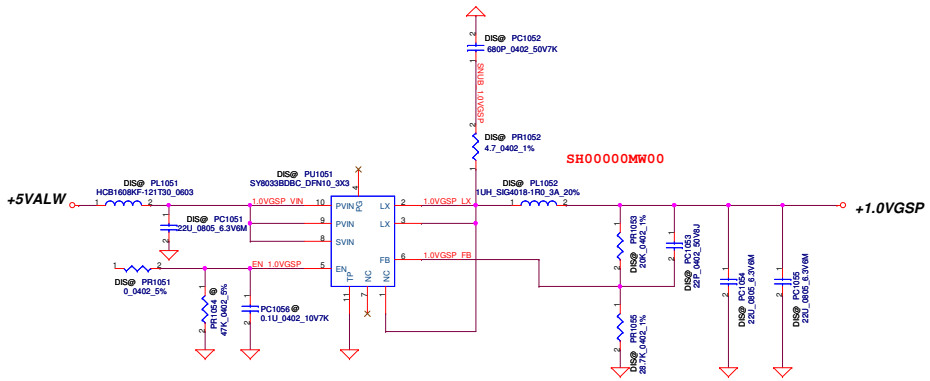
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

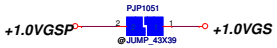
Compal Electronics, Inc.

Title: **PWR- VGA_VDDC**

Size	Document Number	Rev
Custom	LA-8551P	0.1

Date: Wednesday, March 07, 2012 Sheet 55 of 59





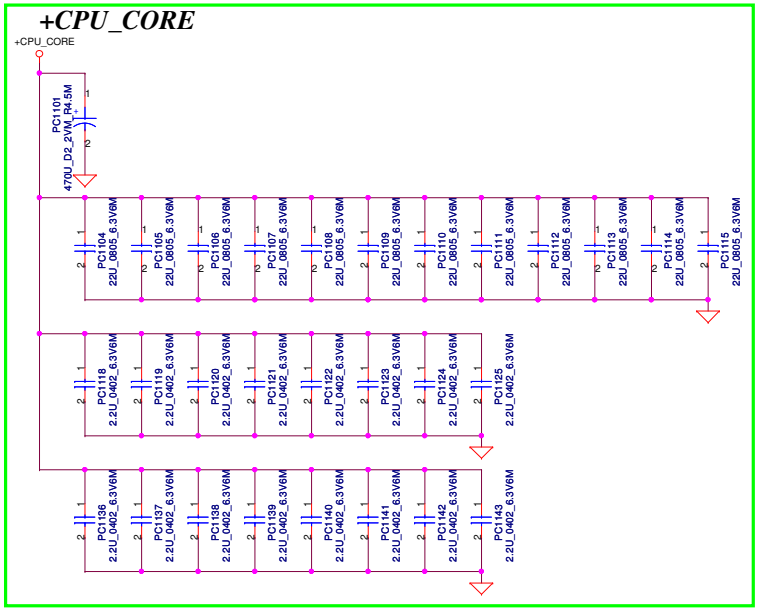
+1.0VSP
TDC=1.54A
Peak Current=2.2A

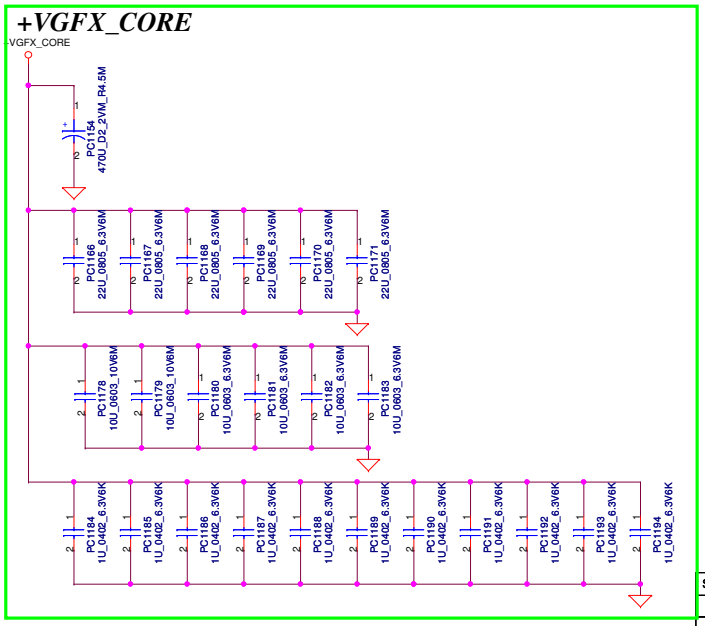
Compal Electronics, Inc.

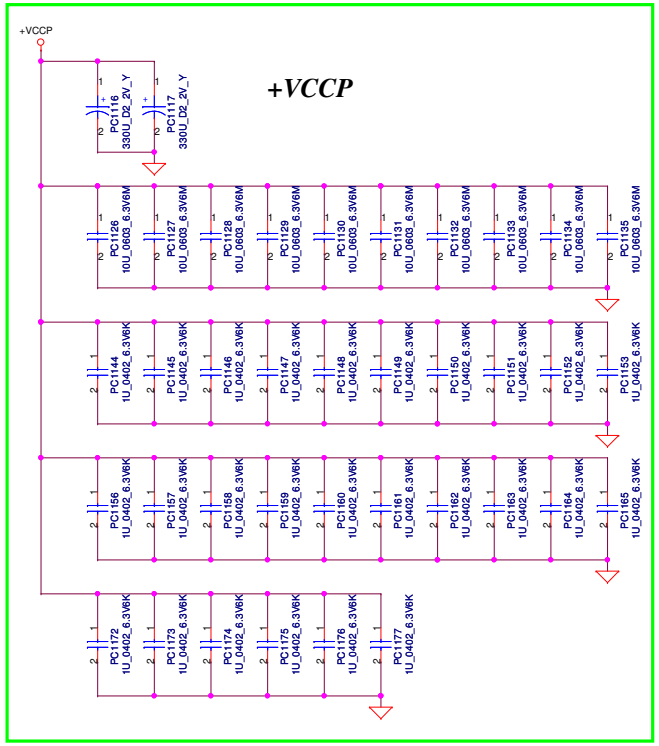
Title: **PWR- VGA 1.0VGSP**

Size	Document Number	Rev
C	LA-8551P	0.1

Date: Monday, March 05, 2012 Sheet 56 of 59







Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size	Document Number	Rev
	LA-8551P	0.1

Date: Saturday, March 03, 2012 Sheet 57 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	change PC111 to 0402	2011/11/28		For layout space		
2	47	remove PR121	2011/11/28		0ohm, not needed		
3	47	change PR124 to 270K, PR126 to 42.2K	2011/11/28		change Vin detector setting		
4	47	change PC125 to 0.047uF	2011/11/28				
5	47	change PR125 to 0ohm, PC126 to 100pF	2011/11/28		FAE review recommand		
6	47	change PR119 to 365K	2011/11/28		modify charge Ilimit to 3.54A		
7	47	change PR111 to 0ohm	2011/11/28				
8	47	add PL101	2011/11/28				
9	46	delete PD5, PD6	2011/11/28		imbedded battery, ESD diode is not needed		
10	46	SMC, SMD exchange	2011/11/28				
11	46	delete pin8 and pin5, add battery temp sense at pin5.	2011/11/28		EC request to need one detect pin if SMB communication fail.		
12	47	change PQ302 to AON7518	2011/11/28				
13	50, 52	change PU1001, PU401 from SY8036HDBC to SY8036LDBC	2011/11/28				
14	53	change PU651 from SY8037DCC to SY8037ADCC	2011/11/28				
15	52	add PQ401, PR406, PR407, PC411	2011/11/28				
16	56	change PR1055 to 28.7K	2011/11/28		for correct 1.0V voltage		
17	54	change PL202, PL204 to SH00000PP00, 0.12uH	2011/11/28				
18	54	change PU201 to RT8167, SA00005AU00	2011/11/28				
19	54	change PQ201, PQ203 to AON7518, SB00000U300	2011/11/28				
20	54	change PQ202, PQ204 to FDMS0308AS, SB00000U400	2011/11/28				
21	55	change PL802 to 0.36uH, SH00000HD00	2011/11/28				
22	52	change PU401 to SY8809DFC	2011/11/29				
23	45, 48	change PD2, PD301 DIO CD4148WN-1 1206	2011/11/29		For cost and layout space		
24	51	add PC511, PC512	2011/12/11				
25	54	change PL201 to 0805, and add PL203	2011/12/11				
26	48	add PR320	2011/12/11		tune frequency		
27	55	change PC813, PC814, PC815, PC816 tp 330uF 9m	2011/12/11				
28	47	change PQ101 to SB000009610	2011/12/11				
29	54	change PR210, PR214, PR261, PR264 to 3.3K; PR222 to 15.8K; PR255 to 10.5K; PC202, PC209 to 270p; PC223 to 220p; PC227 to 560p; PR224, PR254 to 1.82K; PR207 to 127K	2011/12/11		Fine tune CPU, GFX transient		
30	47, 54	change PR111, PR110, PR216, PR249 to 2.2 ohm	2011/12/12		For EMI solution		
31	53, 56	change PL602, PL1052 to SH00000MW00	2011/12/12		For crack issue		
32	55	change PL802 to SH00000HQ00	2011/12/12		For thermal solution		
33	48	change PL303 to SH000000N00	2011/12/12		For thermal solution		
34	47	change PR114, PR115 to 0 ohm	2011/12/14		Prevent charger damaged by negative output voltage		
35	54	change PR207 to 66.5K	2011/12/14		For GFX GT2 current limit		
36	54	change PR237 to 23.7K +-1% 0402	2011/12/23				
37	54	change PR241 to 1/16W 0 +-5% 0402	2011/12/23				
38	54	change PR242 to 23.7K +-1% 0402	2011/12/23				
39	47	change PQ103, PQ104 to SB00000TZ00	2011/12/23				
40	47, 48	change PQ106, PQ303 to SB00000H700	2011/12/23				
41	54	change PR210,PR261,PR264 to 3.3K +-1% 0402	2011/12/23				
42	53	change PL651 to SY8037CDCC	2012/1/11		For latch mode		
43	57	change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/11		For height limit		
44	46	Delete PC11	2012/1/12		For ME request		

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
45	47	change PR114 to 10, PR115 to 6.8ohm, add PD103	2012/1/30		For Charger issue		
46	47	Add PC130, PC131, PC104, PC107	2012/1/30		For EMI solution		
47	48	Add PR321	2012/1/30		Choose working frequency to improve efficiency and thermal		
48	50	change 1.5VPCIE Circuit	2012/1/30		Change input voltage form 5V to 19V to slove thermal issue		
49	52	Add PL403	2012/1/30		Choose input voltage to slove thermal issue		
50	54	Change PR224 to1.58Kohm, PC209 to 220PF, PC202 to 390PF, PR222 to 16.9Kohm, PR237 to 21.5K	2012/1/30		Base on SI layout, FAE review recommand value		
51	48	change PL303 to SH00000F600	2012/1/30		For thermal issue		
52	45	Delete PD2, PR2, PR3, PC6	2012/1/30		For Layout space		
53	47, 48, 54	Change PQ302, PQ201, PQ203 to AON7514	2012/1/30		For efficiency		
54	51	Delete PJP501	2012/1/30		For Layout space		
55	55	Change PC813, PC814, PC815 to 470uF, delete PC816 Change PL802 0.36uF to 13*13*3.5 size	2012/1/30		For thermal issue		
56	55	Add PC820, PC821, PC822	2012/1/30		For VGA transient voltage		
57	57	Change PC1180, PC1181, PC1182, PC1183 to SE000005T80	2012/1/30		For ME request		
58	47	change PQ102 to TPCA8057	2012/1/30				
59	54	change PC223 to 560pF, PC227 to 220pF	2012/2/17		For FAE suggesstion		
60	48	change PQ302 to AON7518	2012/2/17		For efficiency		
61	55	change PL802 to 13*13*3 size	2012/2/17		For thermal solution		
62	47	change PR114, PR115 to 0 ohm, PD103 to SCS00005800	2012/2/17		For HP and soucer request		
63	54	change PC201 to 330uF	2012/2/17		For acoustic solution		
64	45	change LED circuit	2012/2/23				
65	48	change PL303 to 3.3uH 10*10*3H, PC313 to 150U_B2_6.3VM_R35M, remove 5V output jumper	2012/2/23		For thermal solution		
66	53	change PU651 to SY8037DDCC	2012/2/23		For ULV CPU and latch mode		
67	55	change PR812 and PR816 power to +3VGS	2012/2/23		For leakage issue		
68	45	change LED circuit	2012/2/29				
69	54	change PC209 to 390pF, PR237 to 13.3Kohm, PR254 to 1.13Kohm, PR255 to 16.2Kohm, PR242 to 6.65Kohm	2012/2/29		Base on PV layout		
70	45	change PL1, PL2 to 0603 size, add PL4	2012/2/29		EMI request		

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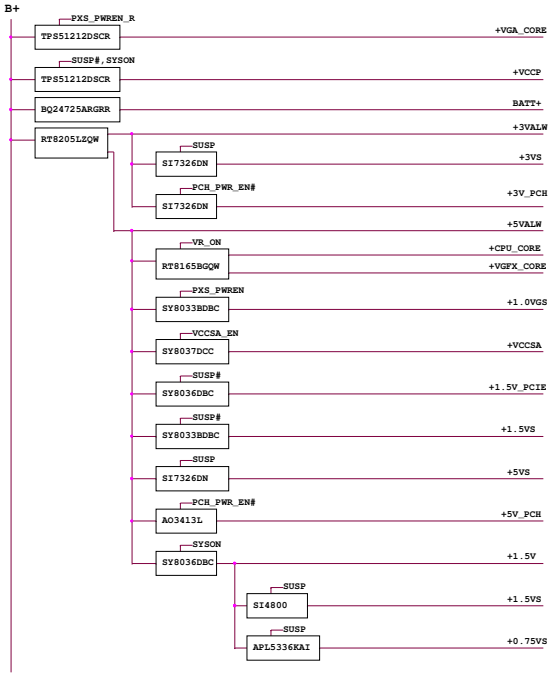

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