Mini Cool Edge I/O Series Connector

Overview

ACES MCIO Series is designed as a low-profile connector with high density and a high-speed solution that can help clients design server and networking equipment for high data rate signal transmission.

It’ s also compatible with SNIA SFF-TA-1016 and PCIe Gen5 standard defined by PCI-SIG. To meet the demand for higher speed requirements, ACES offers products that can transmit the high-speed signal up to 56G PAM4/PCIe Gen5 based on clients’ needs.

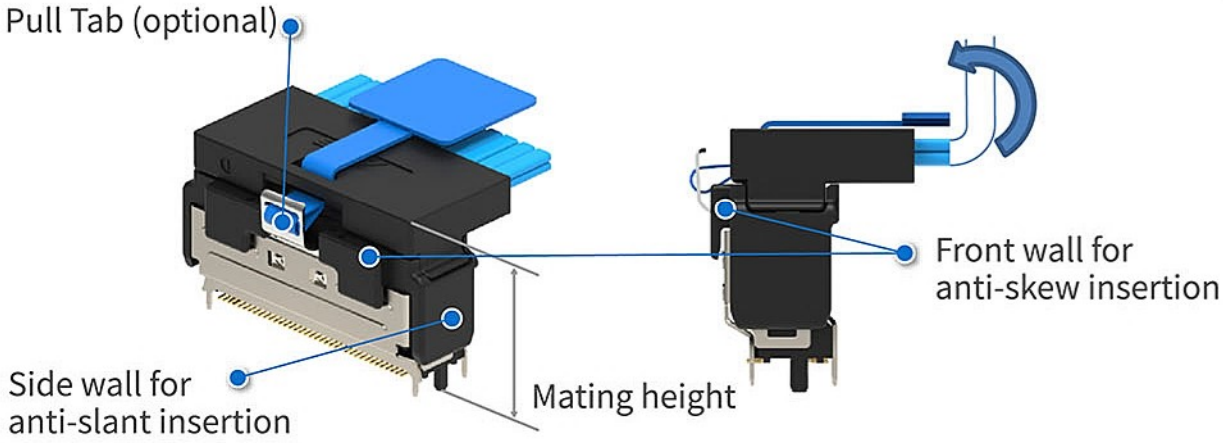
Features

- 0.60mm pitch.
- Straight, right angle, side exit, and customized cable plugs are available.
- High-speed PCIe Gen5/56Gb PAM4 capability.
- Patent licensing from Amphenol Corporation.
- Allows internal/external system strategy and flexibility.
- Supports 85Ω/92Ω impedance applications.
- 4X(38pin), 8X (74pin), 16X (124pin), 20X (148pin) connectors are available.
- 30 AWG cable.

Applications

- Server/Storage devices
- Bulk cable form factor restrictions
- Multi-lane storage devices
- Data center & Networking equipment
- Internal cable solutions
  - Chip to chip
  - Chip to backplane
  - PCB card edge (BTB) solutions
  - Chip to I/O
  - Board to board

MCIO Series for Internal Cable Solutions



Various Cable Exit Directions

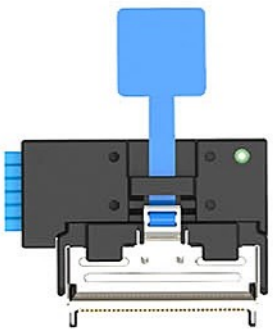
Straight Cable Exit

18.4mm

Right Angle Cable Exit

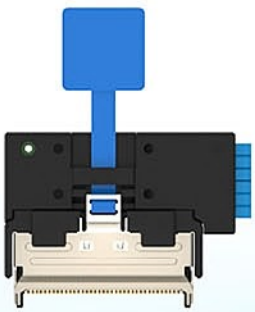
15.9mm

Left Side Cable Exit



23.45mm

Right Side Cable Exit



23.45mm

Right Angle Connector Type

8.27mm

MCIO Connector Family Status

MCIO Connector Vertical Type

P/N	Description	Circuits	Status	
			85ohm	92ohm
52729-038XX-XXX	Vertical type with 30u" Au plating	38(4X)	Available	Available
52729-074XX-XXX	Vertical type with 30u" Au plating	74(8X)	Available	Available
52729-124XX-XXX	Vertical type with 30u" Au plating	124(16X)	Available	Preparing
52729-148XX-XXX	Vertical type with 30u" Au plating	148(20X)	Available	Preparing

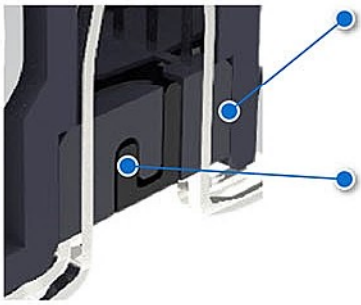
MCIO Connector Vertical Type

P/N	Description	Circuits	Status	
			85Ω	92Ω
52730-038XX-XXX	Right Angle type with 30u" Au plating	38(4X)	Available	Preparing
52730-074XX-XXX	Right Angle type with 30u" Au plating	74(8X)	Available	Preparing
52730-124XX-XXX	Right Angle type with 30u" Au plating	124(16X)	Available	Preparing
52730-148XX-XXX	Right Angle type with 30u" Au plating	148(20X)	Preparing	Preparing

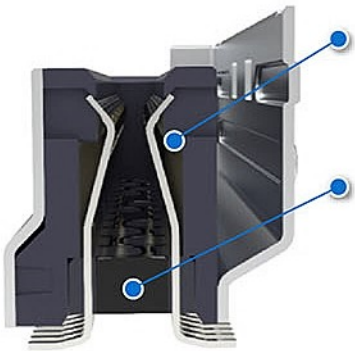
Note:
Other circuits options such as 56(4X+S+P), 100(16X), 140(16X+S+P) could be customized.
The soldering pin length of the shell could be customized for different PCB thickness applications.

MCIO 8X Vertical Connector

MCIO Connector Vertical Type



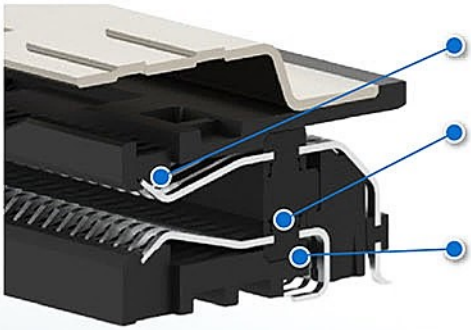
- Assembled by interlocking up and down can increase structural stability.
- The conductive plastic does not need to touch the terminal. It helps improving high frequency performance.



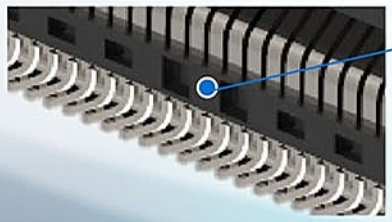
- Contact under the plastic reduces the damage.
- GND pin with conductive plastic reduces the crosstalk.

MCIO 8X Right Angle Connector

Features of R/A Type Connector



- Contact under the plastic reduces the damage.
- The conductive plastic does not need to touch the terminal. It helps improving high frequency performance.
- GND pin with conductive plastic reduces the crosstalk.



- The solder tail are covered with plastic to increase the coplanarity stability

SI Performance Specification

- Evaluation for high-speed performance of the MCIO R/A connector:
  - 3D model: MCIO R/A type connector
  - Simulate software: ANSYS HFSS
- Specification:
  - SFF-TA-1002 Rev, 1.3 February 19, 2020
  - PCI CEM Rev, 5.0 Ver. 1.0 June 18, 2021
- Parameters included:
  - Insertion loss
  - Return loss
  - Near-end crosstalk (PSNEXT)
  - Far-end crosstalk (PSFEXT)

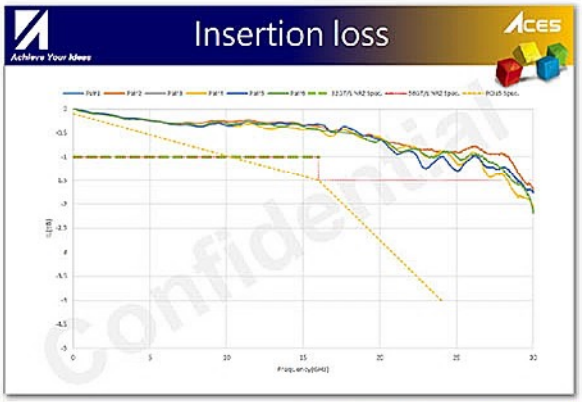
PCIe5 v1.0 Specification

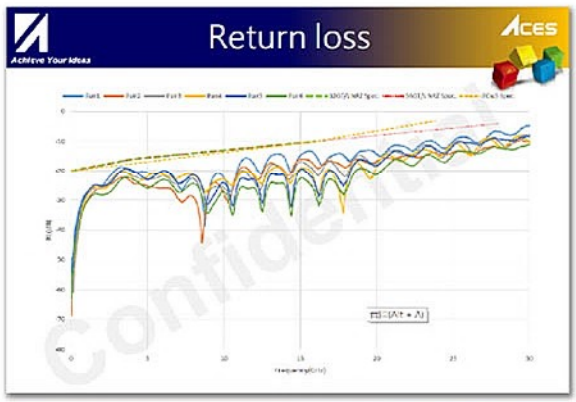
Table 6-7: Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

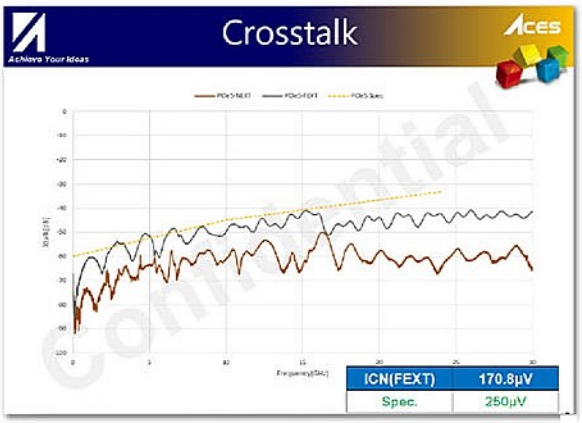
Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.5.1. 3. The test fixture effect shall be removed from the measured S parameters. See Note 1.	[-0.1 - 0.0875 * f] dB up to 16 GHz; [3.5 – 0.3125* f] dB for 16 < f ≤ 24 GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.5.1. 3. The test fixture effect shall be removed. See Note 1.	[-20 + 0.625* f] dB for f ≤ 16 GHz; [-24 + 0.875* f] dB for 16 < f ≤ 24 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The Near-End Crosstalk is the power sum crosstalk with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as listed in Table 6-10. 2. This is a differential crosstalk between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 3. If this frequency based DDNEXT requirement is not met, $ccICN_{NEXT}$ must be used to determine the crosstalk energy in the given frequency band using Equation 1 and must be less than the value indicated under the requirements column.	[1.5* f – 60] dB for f ≤ 10 GHz; [(5/6)* f – 53.33] dB for 10 < f ≤ 24 GHz; $ccICN_{NEXT}$ ≤ 250 µV for f_{max} = 24 GHz
Differential Far End Crosstalk (DDFEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The Far-End Crosstalk is the power sum crosstalk with respect to all pins 2 pairs away from opposite sides of the connector channel, as listed in Table 6-11. 2. This is a differential crosstalk between a victim differential signal pair and all the differential signal pins two pairs away. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 3. If this frequency based DDFEXT requirement is not met, $ccICN_{FEXT}$ must be used to determine the crosstalk energy in the given frequency band using Equation 2 and must be less than the value indicated under the requirements column.	[1.5* f – 60] dB f or f ≤ 10 GHz;; [(5/6)* f – 53.33] dB for 10 < f ≤ 24 GHz; $ccICN_{FEXT}$ ≤ 250 µV for f_{max} = 24 GHz

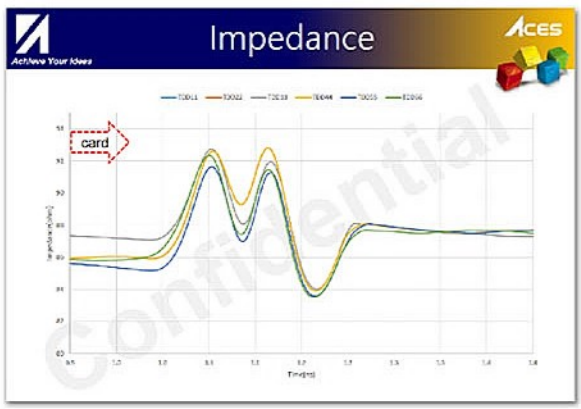
Mini Cool Edge I/O (PCIe Gen5)

SI Performance-8X, S/T



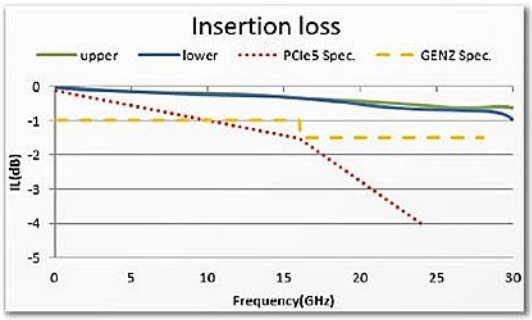


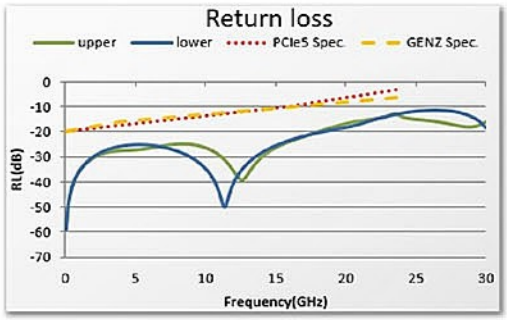


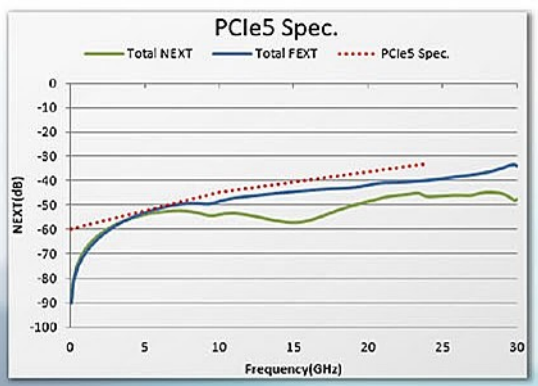


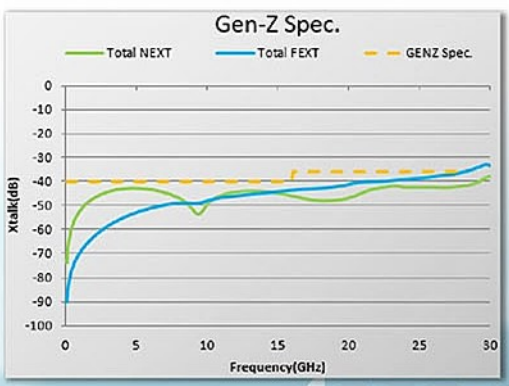
■ 56GT/s NRZ Spec. ■ PCIe® Gen5 Spec.

SI Performance-8X, R/A (Simulated)





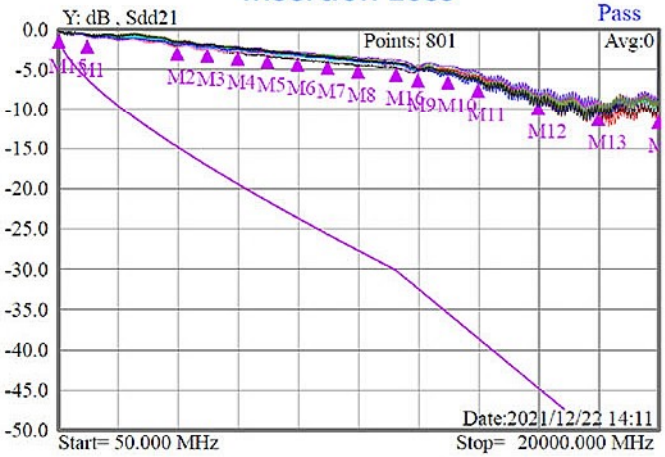




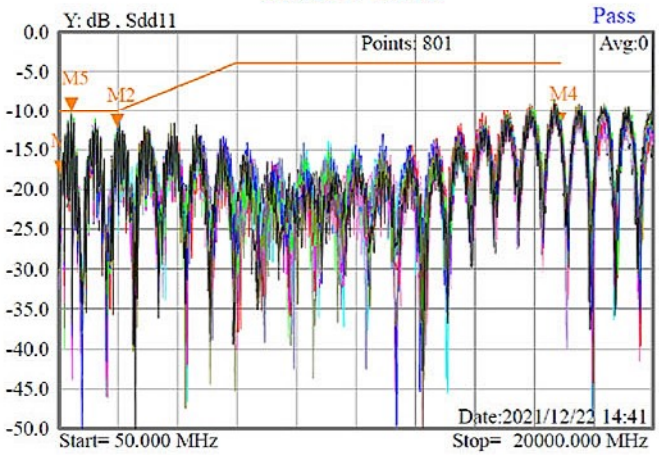
MCIO Cable S/T to S/T 1M (PCIe Gen5)

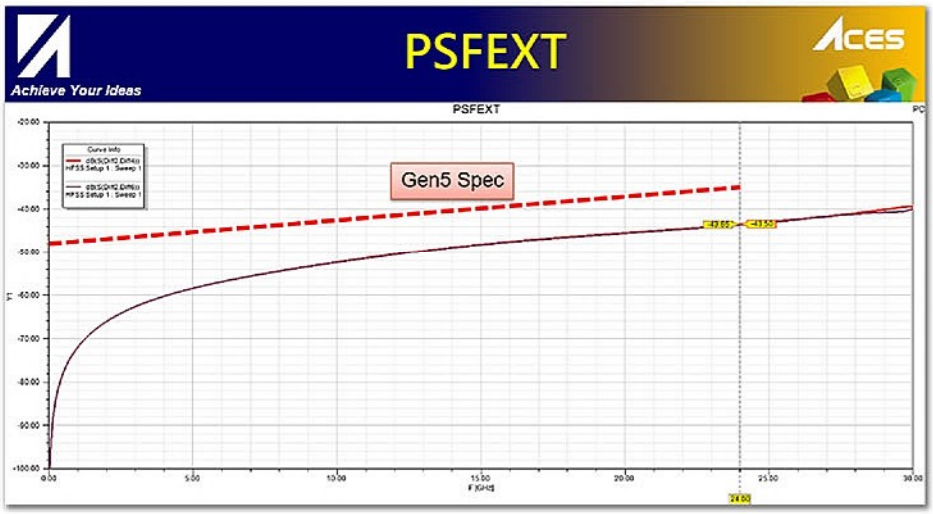
SI Performance-8X, S/T

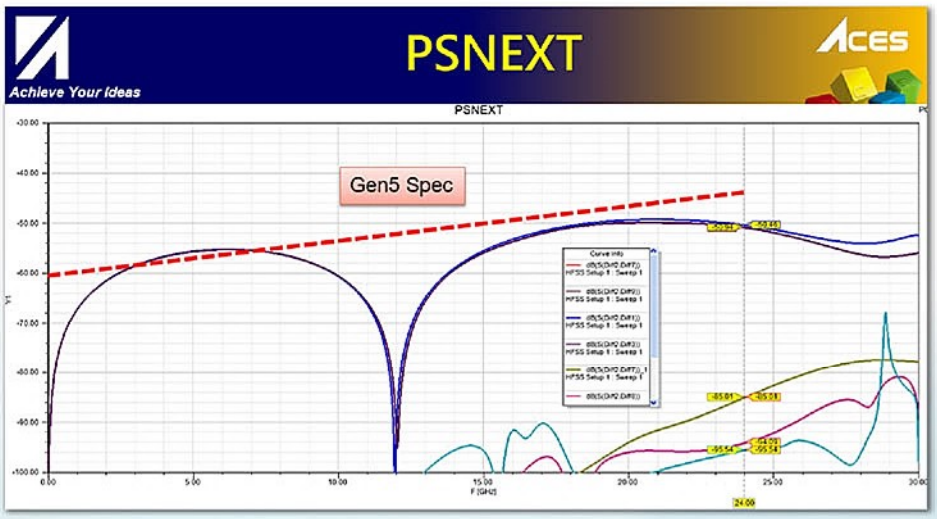
Insertion Loss



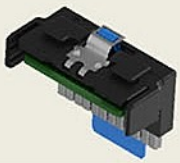
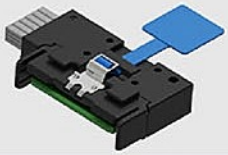
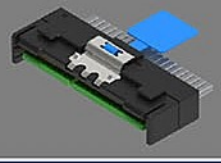
Return Loss







MCIO Cable Plug Family Status

	Straight (STR)	Right Angle (R/A)	Left Side Exit (LSE)	Right Side Exit (RSE)
4X (38pin)				
8X (74pin)				
16X (124pin)			Under Development	
24X (148pin)	Under Development			

★ The pull tab is optional.
★ 92Ω or 100Ω is customized.
★ Other pins such as 56(4X+S+P), 100(16X), 140(16X+S+P) could be customized.

Available
Tooling
Under development

MCIO Cable Plug Family P/N

Port	Pin	Type		ACES P/N
4i	38P	S/T	S/T	73800 - Series
4i	38P	S/T	LSE	73801 - Series
4i	38P	S/T	RSE	73802 - Series
4i	38P	S/T	R/A	73803 - Series
8i	74P	S/T	RSE	73806 - Series
8i	74P	S/T	R/A	73807 - Series
8i	74P	S/T	LSE	73808 - Series
8i	74P	S/T	S/T	73809 - Series
8i	74P	R/A	LSE	73811 - Series
16i	124P	Preparing		
24i	148P	Preparing		