AT65609EHV

Rad Hard, 5V, 128K x 8 Very Low Power CMOS SRAM

DATASHEET

Features

- Asynchronous SRAM
- Operating Voltage: 5V
- Read Access Time: 40 ns
- Write Cycle Time: 30 ns
- Very Low Power Consumption (Pre-RAD)
  - Active: 275 mW (Max)
  - Standby: 44 mW (Max)
- Wide Temperature Range: -55°C to +125°C
- 400 Mils Width Packages: FP32 and SB32
- TTL Compatible Inputs and Outputs
- No Single Event Latch-up below a LET Threshold of 80 MeV/mg/cm^2@125°C
- Radiation Tolerance(1)
  - Tested up to a Total Dose of 300 krads (Si)
  - RHA capability of 100 krad (Si) according to MIL STD 883 Method 1019
- ESD better than 4000V
- Deliveries at least equivalent to QML procurement according to MIL-PRF38535
- Pin to pin compatible with M65608E

Note: 1. tolerance to MBU's may need to be enhanced by the application

Description

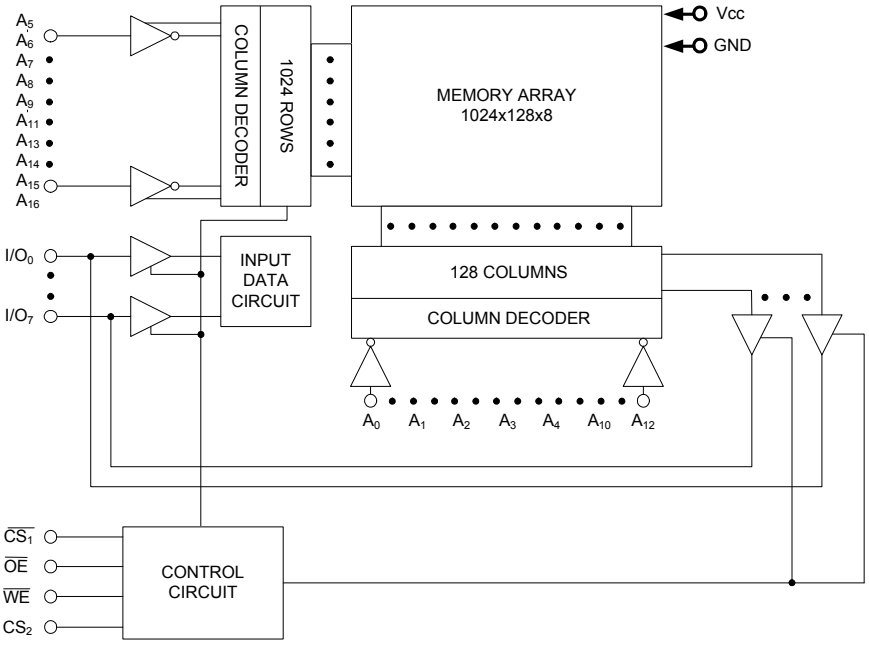
The AT65609EHV is a very low power CMOS static RAM organized as 131072 x 8 bits. Utilizing an array of six transistors (6T) memory cells, the AT65609EHV combines an extremely low standby supply current with a fast access time over the full military temperature range. The high stability of the 6T cell provides an excellent protection against soft errors due to noise.

The AT65609EHV is processed according to the methods of the latest revision of the MIL PRF 38535 or ESCC 9000.

It is manufactured on the same process as the MH1RT Rad-Hard sea of gates series.

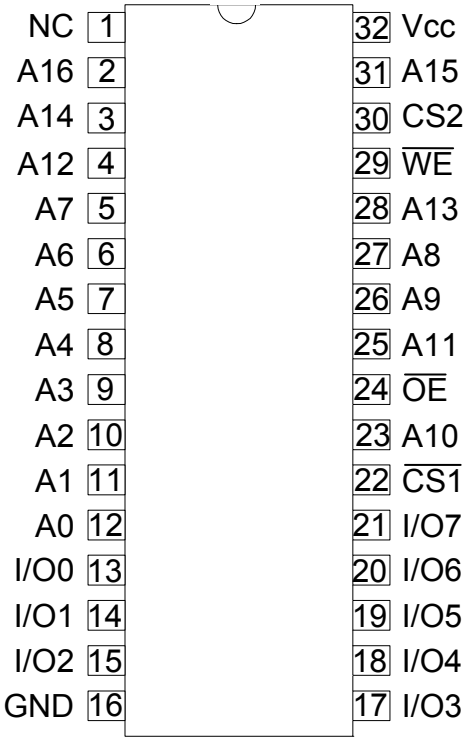
Table of Contents

1. Block Diagram



2. Pin Assignment

Figure 2-1. 32-lead DIL side-brazed or 32-lead Flat Pack - 400 Mils



Note: NC pin is not bonded internally and can be connected to GND or VCC.

3. Pin Description

Table 3-1. Pin Names

Names	Description
A0 - A16	Address inputs
I/O0 - I/O7	Data Inputs/Outputs
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Power

Table 3-2. Truth Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Inputs/ Outputs	Mode
H	X	X	X	Z	Deselect/Power-down
X	L	X	X	Z	Deselect/Power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Supply voltage to GND potential:-0.5V + 7.0V

DC input voltage:GND - 0.5V to VCC + 0.5

DC output voltage high Z state:GND - 0.5V to VCC + 0.5

Storage temperature:-65°C to +150°C

Output current from output pins (low):20 mA

Electro Static Discharge voltage with HBM method (MIL STD 883D method 3015): > 4000V

Electro Static Discharge voltage with Socketed CDM method (ANSI/ESD SP5.3.2-2004): > 1000V

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.**

4.2 Military Operating Range

Operating Voltage	Operating Temperature
5V ± 10%	-55°C to + 125°C°

4.3 Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.5	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	VCC + 0.5	V

4.4 Capacitance

Parameter	Description	Max	Unit
Cin(1)	Input low voltage	8	pF
Cout(1)	Output high voltage	8	pF

Note: 1. Guaranteed but not tested.

5. DC Parameters

5.1 DC Test Conditions (Pre and Post-Radiation)

TA = -55°C to + 125°C; GND = 0V; V_{CC} = 4.5V to 5.5V

Symbol	Description	Test Conditions	Min	Max	Unit
IIX	Input leakage current	GND <= Vin <= V_{CC}, GND <= Vout <= V_{CC}, Output Disabled.	-3	3	µA
IOZ	Output leakage current		-3	3	µA
VOL	Output low voltage	V_{CC} min. IOL = 8 mA	–	0.4	V
VOH	Output high voltage	V_{CC} min. IOH = -4 mA.	2.4	–	V

5.2 Power Consumption

Symbol	Description	Test Conditions	TAVAV/ TAVAW	Max		Unit
				Pre-RAD	Post-RAD	
ICCSB	Standby supply current (SMD Conditions)	V_{CC} max, F=0 Hz, $\overline{CS1}$ >= V_{IH} , CS2 <= V_{IL} ,		8	70	mA
ICCSB1	Standby supply current (SMD Conditions)	V_{CC} max, F=0 Hz, $\overline{CS1}$ >= V_{CC} - 0.2V, CS2 <= GND + 0.2V, Inputs=V_{IH} or V_{IL},		7	65	mA
ICCSB1	Standby supply current (Standard Conditions)	V_{CC} max, F=0 Hz, $\overline{CS1}$ >= V_{CC} - 0.2V, CS2 <= GND + 0.2V, Inputs=GND or V_{CC}		2	60 (2)	mA
ICCOPR	Dynamic operating current (READ)	V_{CC} max, F = 1/TAVAV, Iout = 0 mA, $\overline{CS1}$=V_{IL}, $\overline{OE}$=$\overline{WE}$=CS2=V_{IH}	40 ns(1)	50	115	mA
			50 ns(2)	45	110	mA
			100 ns(2)	40	105	mA
			250 ns(2)	25	90	mA
ICCOPW	Dynamic operating current (WRITE)	V_{CC} max, F = 1/TAVAW, Iout = 0 mA, $\overline{OE}$=CS2=V_{IH} $\overline{WE}$=$\overline{CS1}$=V_{IL}	35 ns(2)	50	115	mA
			40 ns(1)	45	110	mA
			50 ns(2)	40	105	mA
			100 ns(2)	30	95	mA
			250 ns(2)	25	90	mA

Note: 1. Parameters guaranteed and tested
2. Parameters guaranteed but not tested.

6. AC Parameters

6.1 Test Conditions

Input Pulse Levels: ..... GND to 3.0V

Supply Voltage: .....5 ±0.5V

Input Timing Reference Levels: 1.5V

6.2 Test Loads Waveforms

Figure 6-1. Test Loads

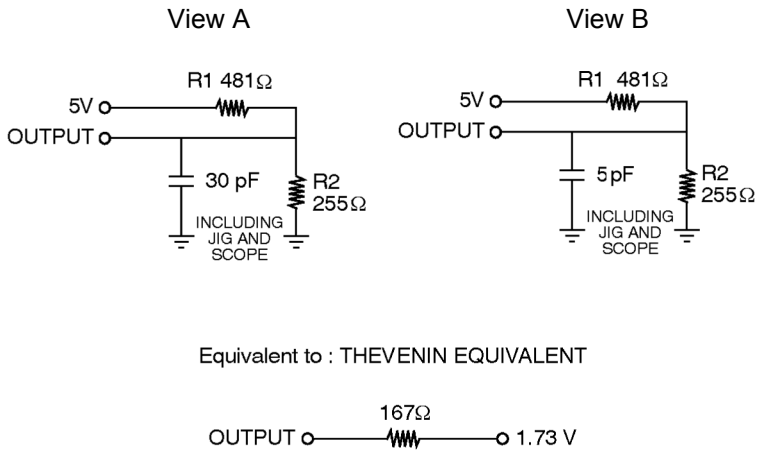
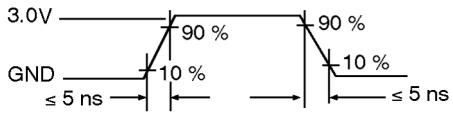


Figure 6-2. CMOS Input pulses

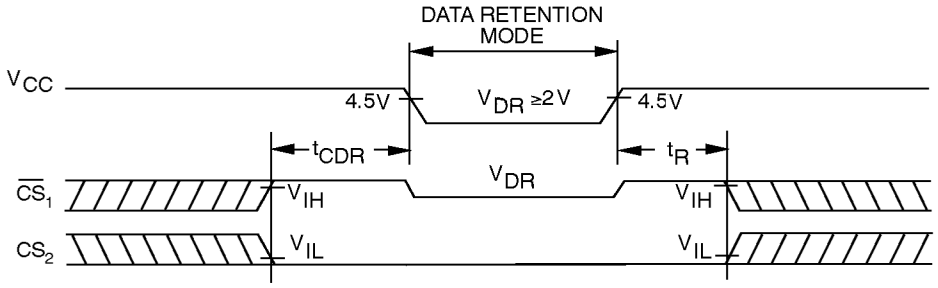


6.3 Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention chip select $\overline{CS1}$ must be held high within VCC to VCC -0.2V or, chip select CS2 must be held down within GND to GND +0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power up and power-down transitions $\overline{CS1}$ and $\overline{OE}$ must be kept between VCC + 0.3V and 70% of VCC, or with CS2 between GND and GND -0.3V.
4. The RAM can begin operation > TR ns after VCC reaches the minimum operation voltages (4.5V).

6.3.1 Timing



6.3.2 Data Retention Characteristics

Parameter	Description	Conditions	Min	Typ	Max		
				TA = 25 °C	Pre-RAD	Post-RAD	Unit
VCCDR	V_{CC} for data retention		2.0	–		–	V
TCDR	Chip deselect to data retention time		0.0	–		–	ns
TR	Operation recovery time		TAVAV(1)	–		–	ns
ICCDR1	Data retention current at 2.0V	$\overline{CS1}$ >= V_{CC}-0.2V CS2 <= 0.2V F= 0 Hz, All other inputs = 0.2V or V_{CC}-0.2V	–	0.1	1	40	mA
ICCDR2	Data retention current at 3.0V(2)		–	0.2	1.5	55	mA

Note: 1. TAVAV = Read Cycle Time
2. Parameters guaranteed, not tested.

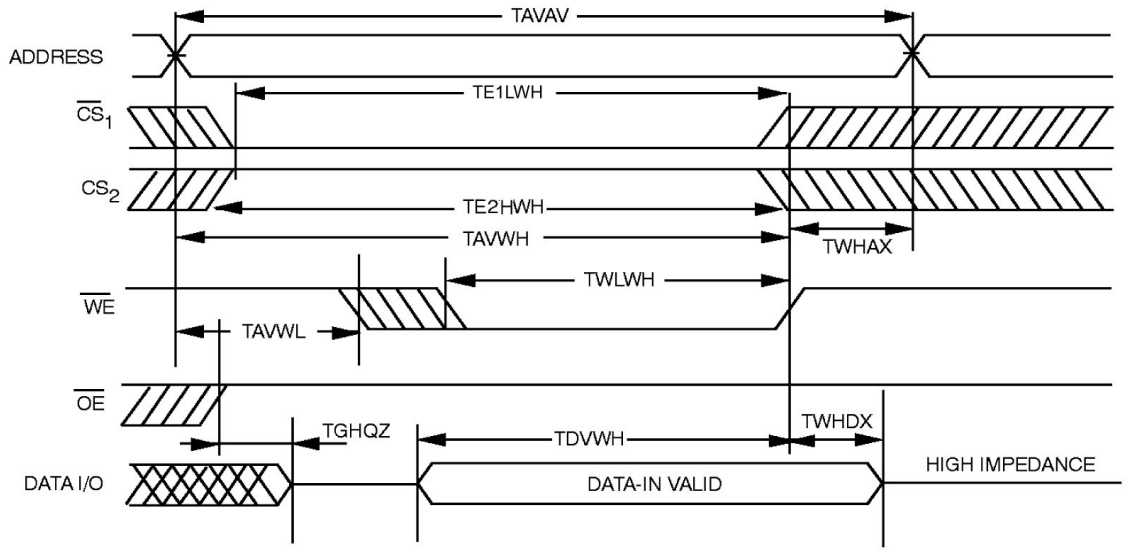
6.4 Write Cycle (Pre and Post-Radiation)

Symbol	Parameter	Min	Max	Unit
TAVAW	Write cycle time	30		ns
TAVWL	Address set-up time	0		ns
TAVWH	Address valid to end of write	28		ns
TDVWH	Data set-up time	15		ns
TE1LWH	$\overline{CS1}$ low to write end	28		ns
TE2HWH	CS2 high to write end	28		ns
TWLQZ	Write low to high Z[1]		8	ns
TWLWH	Write pulse width	26		ns
TWHAX	Address hold from to end of write	3		ns
TWHDX	Data hold time	0		ns
TWHQX	Write high to low Z[1]	5		ns

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF (see view B on Figure 6-1 on page 7).

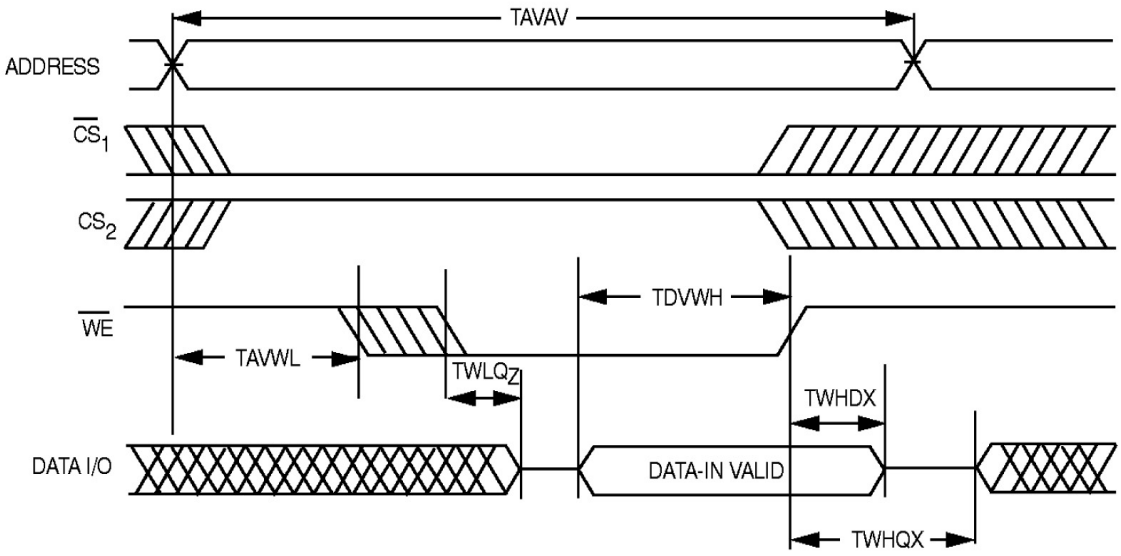
6.4.1 Write Cycle 1

$\overline{WE}$ Controlled, $\overline{OE}$ High During Write



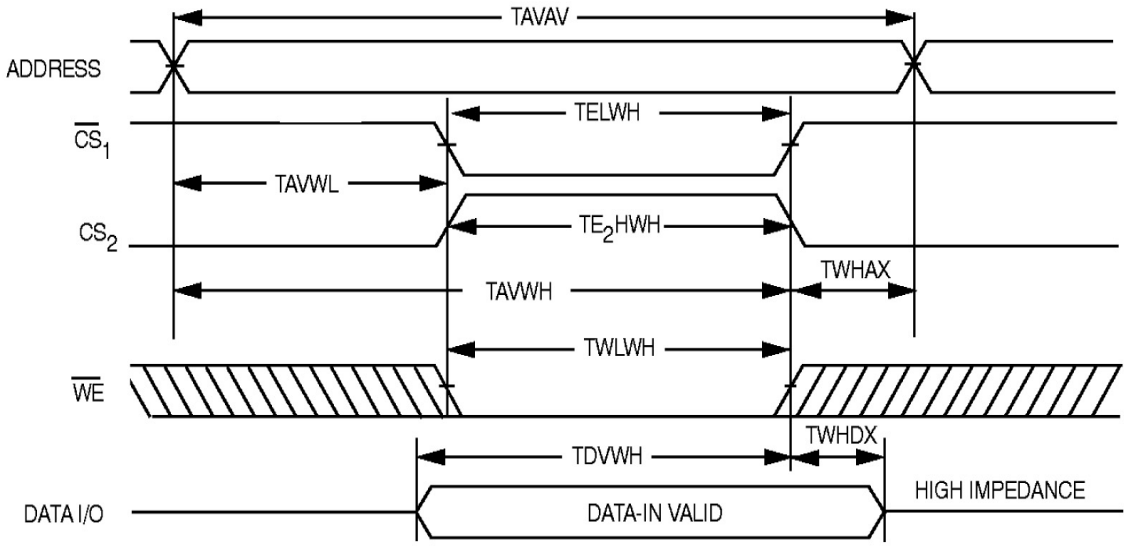
6.4.2 Write Cycle 2

$\overline{WE}$ Controlled, $\overline{OE}$ Low



6.4.3 Write Cycle 3

$\overline{CS1}$ or CS2 Controlled



Note: The internal write time of the memory is defined by the overlap of $\overline{CS1}$ Low and CS2 HIGH and $\overline{WE}$ LOW. Both signals must be actived to initiate a write and either signal can terminate a write by going in actived. The data input setup and hold timing should be referenced to the actived edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$ = V_{IH}.

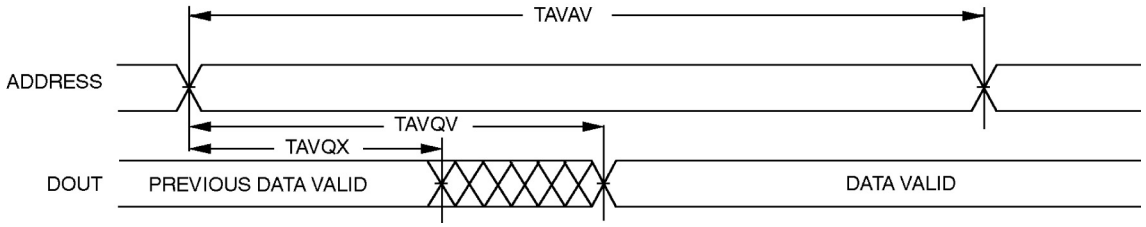
6.5 Read Cycle (Pre and Post-Radiation)

Symbol	Parameter	Min	Max	Unit
TAVAV	Read cycle time	40		ns
TAVQV	Address access time		40	ns
TAVQX	Address valid to low Z	3		ns
TE1LQV	Chip-select1 access time		40	ns
TE1LQX	$\overline{CS1}$ low to low Z(1)	3		ns
TE1HQZ	$\overline{CS1}$ high to high Z(1)		12	ns
TE2HQV	Chip-select2 access time		40	ns
TE2HQX	CS2 high to low Z(1)	3		ns
TE2LQZ	CS2 low to high Z(1)		12	ns
TGLQV	Output Enable access time		10	ns
TGLQX	$\overline{OE}$ low to low Z(1)	0		ns
TGHQZ	$\overline{OE}$ high to high Z(1)		10	ns

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF (see view B on Figure 6-1 on page 7).

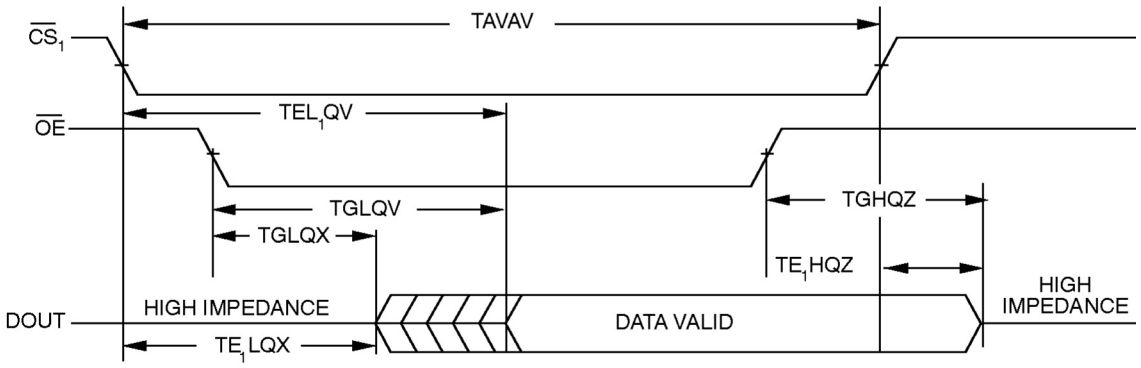
6.5.1 Read Cycle 1

Address Controlled ($\overline{CS1}$ = $\overline{OE}$ Low, CS2 = $\overline{WE}$ High)



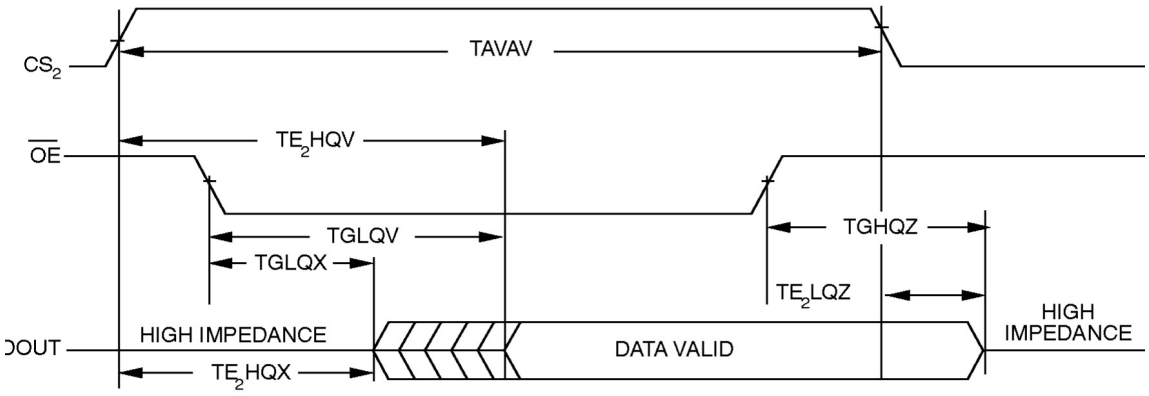
6.5.2 Read Cycle 2

$\overline{CS1}$ Controlled (CS2 = $\overline{WE}$ High)



6.5.3 Read Cycle 3

CS2 Controlled ($\overline{WE}$ High, $\overline{CS1}$ Low)

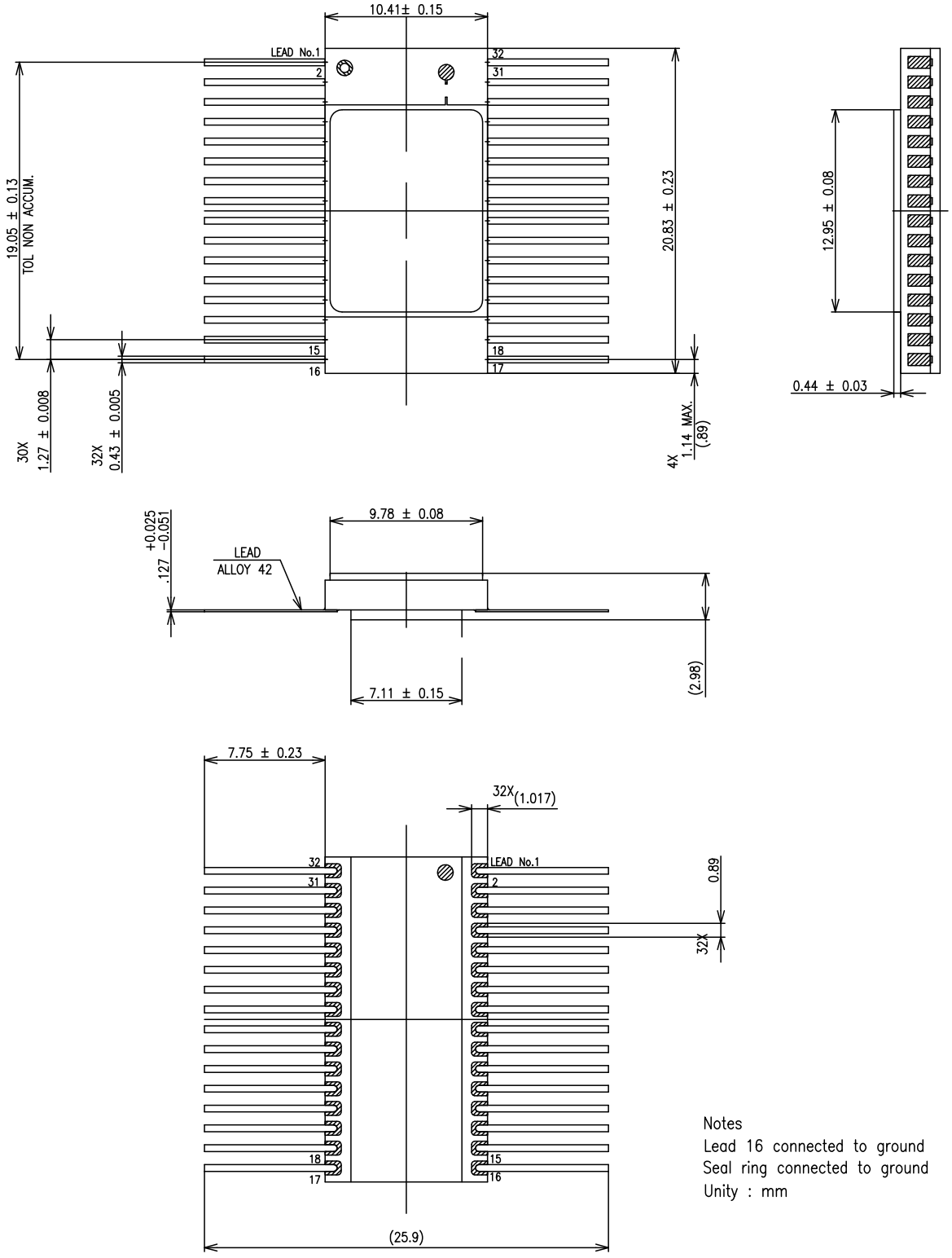


7. Ordering Information

Part Number	Temperature Range	Speed	Package	Test Flow
AT65609EHV-C940-E	25°C	40 ns	SB32.4	Engineering Samples
AT65609EHV-DJ40-E	25°C	40 ns	FP32.4	
5962-8959849QZC	-55° to +125°C	40 ns	SB32.4	QML Q
5962-8959849QTC	-55° to +125°C	40 ns	FP32.4	
5962-8959849VZC	-55° to +125°C	40 ns	SB32.4	QML V
5962-8959849VTC	-55° to +125°C	40 ns	FP32.4	
5962R8959849VZC	-55° to +125°C	40 ns	SB32.4	QML V RHA
5962R8959849VTC	-55° to +125°C	40 ns	FP32.4	

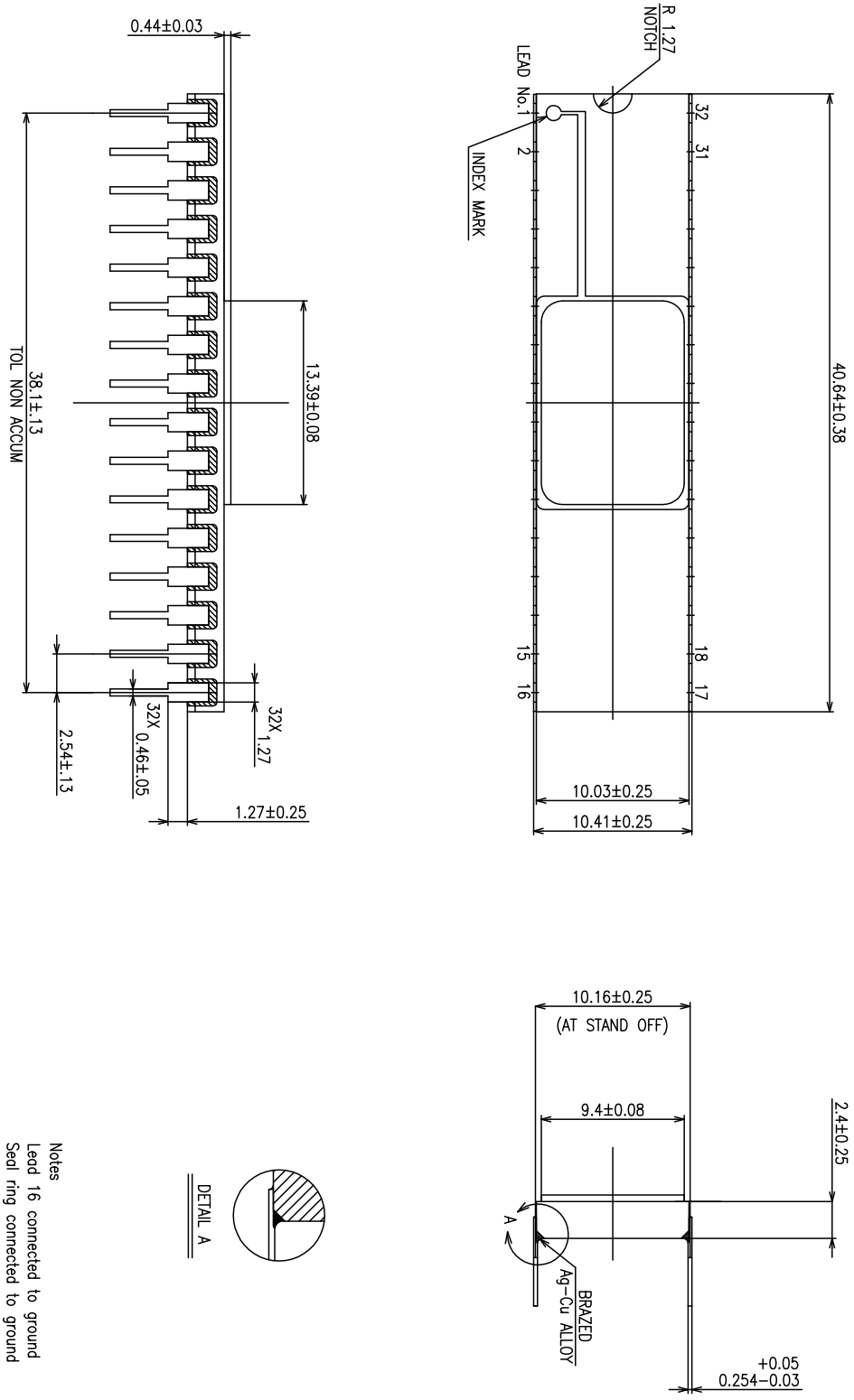
8. Package Drawings

8.1 32-lead Flat Pack 400 Mils



Notes
Lead 16 connected to ground
Seal ring connected to ground
Unity : mm

8.2 32-lead Side Brazed 400 Mils



9. Revision History

Doc. Rev.	Date	Comments
E	09/2014	Update: SMD part-numbers added in ordering information section Update: Footnote of 40 ns item changed in ICCOPW parameter in Power Consumption Section 5.2
D	11/2013	Add-on: MBU's note in features section Update: radiation tolerance specifications in features section Update: Block Diagram Update: AC Test conditions section
C	09/2013	Update: final datasheet release including characterization data Add-on: pre and post-RAD specifications Update: document template
B	11/2009	Update: total dose value in features section Add-on: ESD item in features section Add-on: ESD HBM improved and ESD Socketed CDM in Absolute Maximum Ratings Update: note 3 of Consumption Table Update: ordering information section
A	03/2009	Initial document release.

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