VSC8489

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8489 product family. It is meant to help customers achieve first-pass design success.

There are several members of the VSC8489 family namely, VSC8489-17, VSC8489-16, and VSC8489-02. This document mostly covers VSC8489-17, which is the most full-featured device in the family. On the other hand, the VSC8489-16 is a one-channel device, and the channel 1 pins are unused (no-connects). The VSC8489 must be configured after power-up, even for basic bring-up purposes. Use the Microchip supplied API and reference the sample application for examples of API calls.

These checklist items should be followed when utilizing the VSC8489 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Thermal Considerations"
- Section 5.0, "Media SerDes Interface"
- Section 6.0, "Host Interface (XAUI, RXAUI, and SGMII)"
- Section 7.0, "Reference Clocks"
- Section 8.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8489 implementor should have the following documents on hand:

- *VSC8489-17 Dual Channel WAN/LAN/Backplane RXAUI/XAUI to SFP+/KR 10 GbE SerDes PHY with VeriTime™ Data Sheet*
- *VSC8489-16 Single Channel WAN/LAN/Backplane RXAUI/XAUI to SFP+/KR 10 GbE PHY with Optional VeriTime™ Data Sheet*
- *VSC8489-02 Dual Channel WAN/LAN/Backplane RXAUI/XAUI to SFP+/KR 10 GbE SerDes PHY Data Sheet*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference is used for all ground pins. Use one or more continuous ground planes to ensure a low impedance ground path and a continuous ground reference for all signals. Section 4.0, "Thermal Considerations" also explains the importance of grounds for thermal dissipation.

3.0 POWER

- Table 3-1 show the power supply pins for VSC8489.

TABLE 3-1: POWER SUPPLY PINS

Name	Pin Number	Description	Comment
VDDAH	G4	1.0V power supply for host-side analog	Analog, use ferrite bead
VDDAH	G5	1.0V power supply for host-side analog	
VDDAH	J4	1.0V power supply for host-side analog	
VDDAH	J5	1.0V power supply for host-side analog	
VDDAL	F7	1.0V power supply for line-side analog	Analog, use ferrite bead
VDDAL	G7	1.0V power supply for line-side analog	
VDDAL	G9	1.0V power supply for line-side analog	
VDDAL	H9	1.0V power supply for line-side analog	
VDDAL	J7	1.0V power supply for line-side analog	
VDDHSL	F9	1.2V power supply for line-side I/Os	Analog, use ferrite bead
VDDHSL	F10	1.2V power supply for line-side I/Os	
VDDHSL	G10	1.2V power supply for line-side I/Os	
VDDHSL	H10	1.2V power supply for line-side I/Os	
VDDHSL	J9	1.2V power supply for line-side I/Os	
VDDHSL	J10	1.2V power supply for line-side I/Os	
VDDL	H4	1.0V power supply for chip core	Digital, no ferrite bead
VDDL	H5	1.0V power supply for chip core	
VDDL	H7	1.0V power supply for chip core	
VDDMDIO	C7	2.5V power supply for MDIO I/Os	Digital, no ferrite bead
VDDTTL	C9	2.5V power supply for non-MDIO digital I/Os	Digital, no ferrite bead
VDDTTL	M6	2.5V power supply for non-MDIO digital I/Os	

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. (See Table 3-2.) Note that the 1.0V maximum current values in this table include margins, so they sum to more than the maximum 1.0V current specification in the data sheet. The data sheet value is correct for overall power.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Power Rail	Voltage	Maximum Current
VDDAH	1.0V	1000 mA
VDDAL	1.0V	900 mA
VDDL	1.0V	2000 mA
VDDHSL	1.2V	150 mA
VDDMDIO + VDDTTL	2.5V	50 mA

3.2 Power Supply Planes

- VSC8489 requires three power rails: 2.5V, 1.2V, and 1.0V. The filtered analog 1.0V and 1.2V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).

  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see Section 3.4, "Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Analog Power Plane Filtering

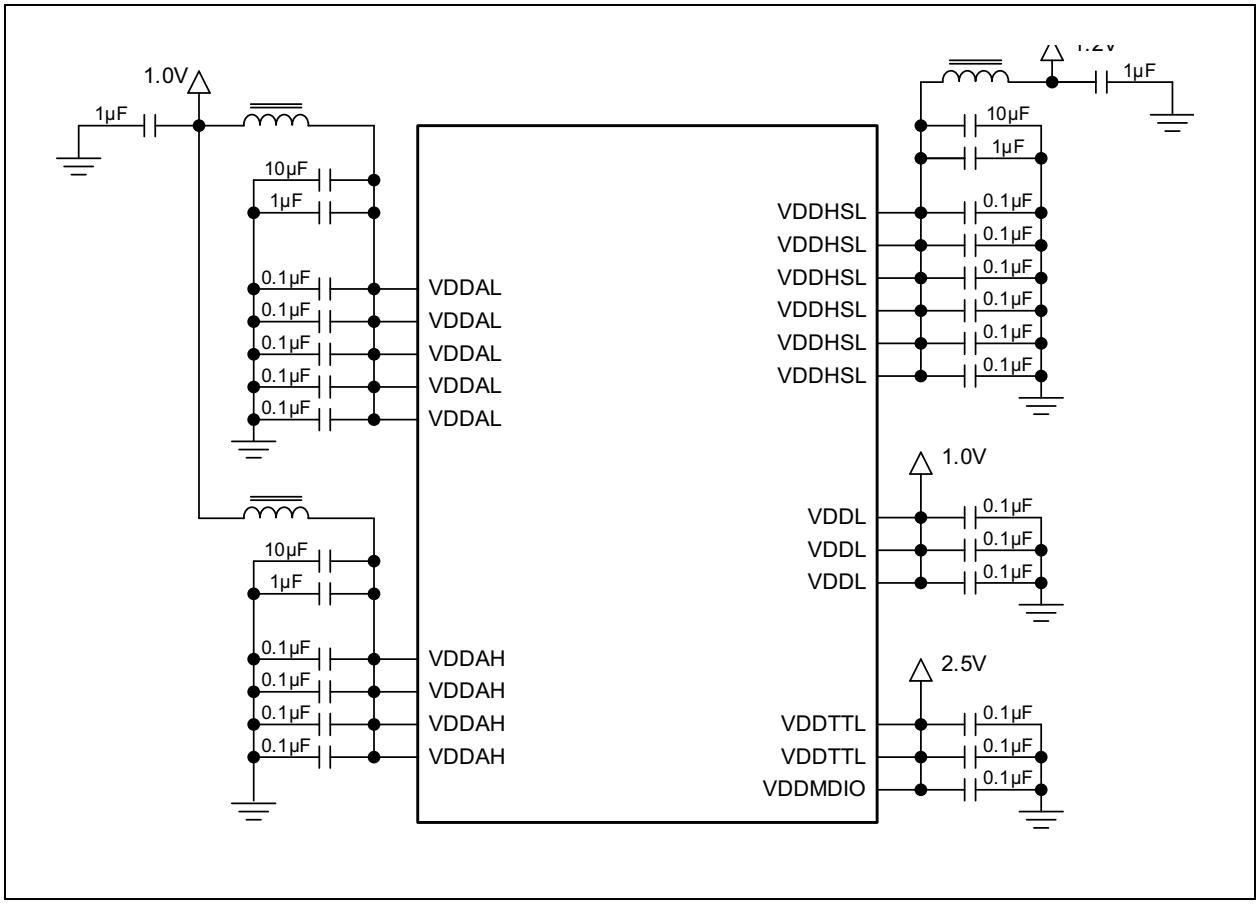
- The analog power supplies are:
  - **VDDAH**
  - **VDDAL**
  - **VDDHSL**
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended on the digital supplies **VDDL**, **VDDTTL**, and **VDDMDIO**.
- The chosen ferrite beads should have the impedance of 80Ω to 120Ω at 100 MHz, and the characteristics are specified in Table 3-3.

TABLE 3-3: FERRITE BEAD PARAMETERS

VSC8489 Analog Supply	Ferrite Bead Requirements	
	Current	Maximum DC Resistance
VDDAH	1000 mA	40 mΩ
VDDAL	1000 mA	40 mΩ
VDDHSL	150 mA	100 mΩ

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close to the VSC8489's power pins as possible for every pin.
- If the VSC8489 device is on the top-side of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

4.0 THERMAL CONSIDERATIONS

- For proper cooling, ensure efficient thermal dissipation by maximizing the number of via connections to the ground plane. Additional ground planes will enhance thermal dissipation and signal integrity performance.
- When connecting the thermal vias to ground planes, it is advisable to avoid thermal relief connection traces as shown on the left-hand side of Figure 4-1 as these are designed to prevent the flow of heat through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer as shown on the right-hand side of Figure 4-1.
- PCB thermal vias should connect to the solid ground planes within the board to dissipate heat below the package. A minimum of one-ounce copper cladding is recommended. Figure 4-2 shows a cross-section of the thermal via.

FIGURE 4-1: THERMAL VIAS

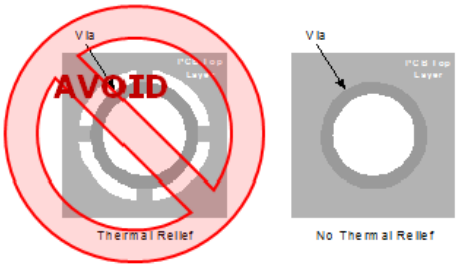
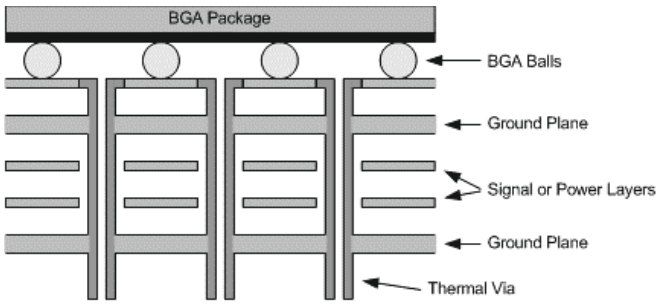


FIGURE 4-2: THERMAL GROUND PLANE CONNECTION



5.0 MEDIA SERDES INTERFACE

5.1 Media SerDes Design Rules

- Table 5-1 shows information on Media SerDes Interface. Best performance is achieved when SerDes traces are placed using the following design rules:
  - AC coupling capacitors are not needed for SFP+ and SFP applications because SFP+/SFP modules have AC coupling capacitors internally on both **TX** and **RX** signals.
  - Use AC coupling with 0.1 µF capacitors on **RXIN** and **TXOUT** for chip-to-chip applications. Place the capacitors at the receiving end of the signals.
  - Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
  - Traces should be of equal length (within 10 mils) on each differential pair to minimize skew.
  - Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
  - Spacing equal to five times the ground plane gap is recommended between adjacent tracks to reduce cross-talk between SerDes pairs. Minimum spacing of three times the ground plane gap is required.
  - Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to reduce the strength of any radiating spurious fields.
  - Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.
  - If a port is unused, both the **RXIN** and **TXOUT** pins can be left floating (no-connect).
  - If the **LOPC** pins are not used, pull them to ground with a resistor.

TABLE 5-1: MEDIA SERDES INTERFACE PINS

Pin Name	Pin Number	Type	Level	Description
RXIN0N	B13	I	CML	Receive channel 0 input data, complement
RXIN0P	B14	I	CML	Receive channel 0 input data, true
RXIN1N	L14	I	CML	Receive channel 1 input data, complement
RXIN1P	L13	I	CML	Receive channel 1 input data, true
TXOUT0N	D14	O	CML	Transmit channel 0 output data, complement
TXOUT0P	D13	O	CML	Transmit channel 0 output data, true
TXOUT1N	N13	O	CML	Transmit channel 1 output data, complement
TXOUT1P	N14	O	CML	Transmit channel 1 output data, true
LOPC0	D6	I	LVTTL	Loss of optical carrier, channel 0. Internally pulled high.
LOPC1	M7	I	LVTTL	Loss of optical carrier, channel 1. Internally pulled high.

5.2 Connecting to 10G SFP+ or 1G SFP

- Follow the succeeding guidelines for connecting the differential SerDes data pins to the SFP+/SFP (also referred to as SFP):
  - Connect the VSC8489 **TXOUT** pins directly to the **TD** input pins of the SFP.
  - Connect the VSC8489 **RXIN** pins directly to the **RD** output pins of the SFP.
  - External termination resistors and AC coupling capacitors are not needed on the PCB.
- Connection and use of the other SFP signals are at the discretion of the user.
- The **RX_LOS** output of the SFP can drive the **LOPC** input of the VSC8489 and/or the host device.
- VSC8489 **GPIO** pins can be configured as Two-Wire masters for accessing SFP registers via SDA and SCL. However, since this adds an additional layer of software complexity to manage these signals, it is extremely common for the SFP Two-Wire interface to be managed directly from the switch/MAC/ASIC host device. **GPIO** assignments are given in the table below.
- VSC8489 **GPIO** pins can also be assigned as inputs for the **MOD_ABS** (module absent) output of the SFP.
- All other SFP signals, if used, should be connected to the switch/MAC/ASIC host device and not to the VSC8489.
- All single-ended SFP outputs are open drain and require a pull-up resistor to 3.3V when used.
- All VSC8489 **GPIO** outputs are open drain and require a pull-up resistor. When connected to an SFP, the pull-up

voltage must be 3.3V and not 2.5V.

GPIO pin assignments are specified in Table 5-2 and Table 5-3.

TABLE 5-2: GPIO ASSIGNMENTS FOR TWO-WIRE MASTER

Channel	VSC8489 Pin	SFP+ Pin
Channel 0	GPIO_6 (pin K4)	SDA, pin 4
Channel 0	GPIO_7 (pin K5)	SCL, pin 5
Channel 1	GPIO_10 (pin L5)	SDA, pin4
Channel 1	GPIO_11 (pin L6)	SCL, pin 5

TABLE 5-3: GPIO ASSIGNMENTS FOR MOD_ABS INPUTS

Channel	VSC8489 Pin	SFP+ Pin
Channel 0	PHY GPIO_0 (pin D4) or GPIO_8 (pin K6)	MOD_ABS, pin 6
Channel 1	PHY GPIO_9 (pin L4)	MOD_ABS, pin 6

- Figure 5-1 and Figure 5-2 illustrate VSC8489 to SFP+ connections. Figure 5-1 shows a typical scenario wherein most SFP signals are connected to the Switch/MAC/ASIC host device rather than the VSC8489. Conversely, Figure 5-2 shows a less common scenario wherein the maximum number of SFP signals are connected to the VSC8489.

FIGURE 5-1: SFP+ CONNECTIONS WITH TWO-WIRE AND MOD_ABS TO THE SWITCH/MAC/ASIC

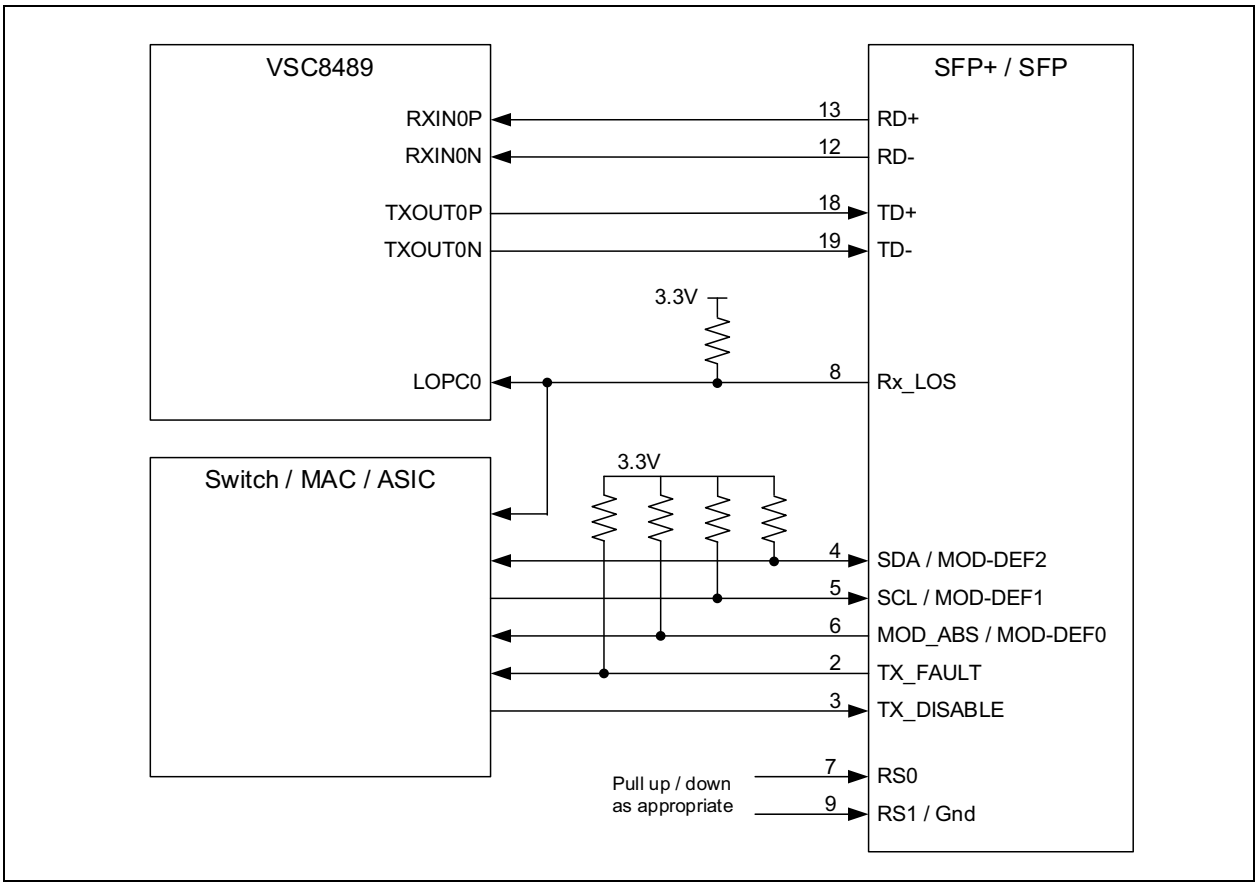
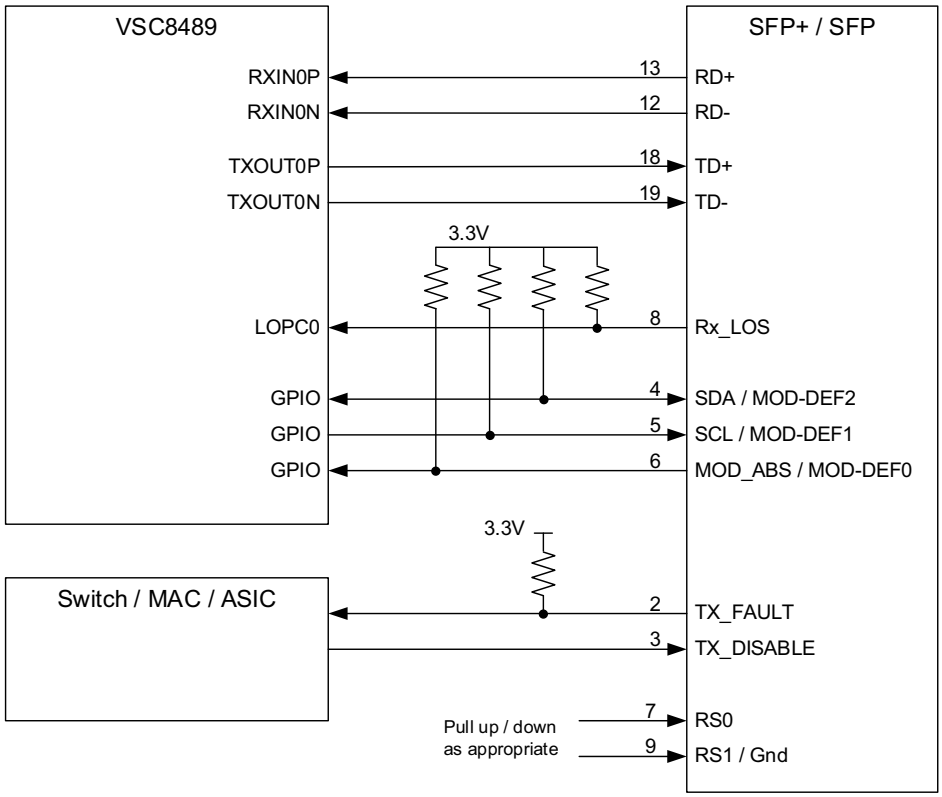


FIGURE 5-2: SFP+ CONNECTIONS WITH TWO-WIRE AND MOD_ABS TO THE VSC8489



6.0 HOST INTERFACE (XAUI, RXAUI, AND SGMII)

- Table 6-1 shows information on Host SerDes Interface.

TABLE 6-1: HOST SERDES INTERFACE PINS

Pin Name	Pin Number	Type	Level	Description
XRX0_0N	C2	I	CML	XAUI channel 0, **RX** path lane 0, serial data input, complement
XRX0_0P	C1	I	CML	XAUI channel 0, **RX** path lane 0, serial data input, true
XRX0_1N	D2	I	CML	XAUI channel 0, **RX** path lane 1, serial data input, complement
XRX0_1P	D1	I	CML	XAUI channel 0, **RX** path lane 1, serial data input, true
XRX0_2N	E2	I	CML	XAUI channel 0, **RX** path lane 2, serial data input, complement
XRX0_2P	E1	I	CML	XAUI channel 0, **RX** path lane 2, serial data input, true
XRX0_3N	F2	I	CML	XAUI channel 0, **RX** path lane 3, serial data input, complement
XRX0_3P	F1	I	CML	XAUI channel 1, **RX** path lane 3, serial data input, true
XRX1_0N	P2	I	CML	XAUI channel 1, **RX** path lane 0, serial data input, complement
XRX1_0P	N2	I	CML	XAUI channel 1, **RX** path lane 0, serial data input, true
XRX1_1N	P3	I	CML	XAUI channel 1, **RX** path lane 1, serial data input, complement
XRX1_1P	N3	I	CML	XAUI channel 1, **RX** path lane 1, serial data input, true
XRX1_2N	P4	I	CML	XAUI channel 1, **RX** path lane 2, serial data input, complement
XRX1_2P	N4	I	CML	XAUI channel 1, **RX** path lane 2, serial data input, true
XRX1_3N	P5	I	CML	XAUI channel 1, **RX** path lane 3, serial data input, complement
XRX1_3P	N5	I	CML	XAUI channel 1, **RX** path lane 3, serial data input, true
XTX0_0N	B6	O	CML	XAUI channel 0, **TX** path lane 0, serial data input, complement
XTX0_0P	A6	O	CML	XAUI channel 0, **TX** path lane 0, serial data input, true
XTX0_1N	B5	O	CML	XAUI channel 0, **TX** path lane 1, serial data input, complement
XTX0_1P	A5	O	CML	XAUI channel 0, **TX** path lane 1, serial data input, true
XTX0_2N	B4	O	CML	XAUI channel 0, **TX** path lane 2, serial data input, complement
XTX0_2P	A4	O	CML	XAUI channel 0, **TX** path lane 2, serial data input, true
XTX0_3N	B3	O	CML	XAUI channel 0, **TX** path lane 3, serial data input, complement
XTX0_3P	A3	O	CML	XAUI channel 0, **TX** path lane 3, serial data input, true
XTX1_0N	H2	O	CML	XAUI channel 1, **TX** path lane 0, serial data input, complement
XTX1_0P	H1	O	CML	XAUI channel 1, **TX** path lane 0, serial data input, true
XTX1_1N	J2	O	CML	XAUI channel 1, **TX** path lane 1, serial data input, complement
XTX1_1P	J1	O	CML	XAUI channel 1, **TX** path lane 1, serial data input, true
XTX1_2N	K2	O	CML	XAUI channel 1, **TX** path lane 2, serial data input, complement
XTX1_2P	K1	O	CML	XAUI channel 1, **TX** path lane 2, serial data input, true
XTX1_3N	L2	O	CML	XAUI channel 1, **TX** path lane 3, serial data input, complement
XTX1_3P	L1	O	CML	XAUI channel 1, **TX** path lane 3, serial data input, true

6.1 Host Serial Interface Design

- The host interface may be either XAUI, RXAUI, or 1GbE / SGMII. It is recommended to use the same configuration for both channels 0 and 1.
- XAUI (10G) uses all four **TX** path lanes and four **RX** path lanes per channel. (See Figure 6-1.)
- RXAUI (10G) uses lanes 0 and 2. Lanes 1 and 3 can be left floating (no-connect). (See Figure 6-2.)
- 1GbE (1.25 Gbps) or SGMII uses either lane 0 or 3 only. The other three lanes can be left floating (no-connect). (See Figure 6-3.)
- Check the signal directions, so that the outputs of one device connect to the inputs of the other device.
- Use AC coupling with 0.1 µF capacitors. Capacitors are best located close to the destination.
- The AC coupling capacitors are not required in cases wherein the driver satisfies the Common-mode voltage requirements of the receiver.
- The VSC8489 has internal termination on the **XRX** inputs, so external termination resistors are not needed. The host typically has internal termination also. If it does not, then 100Ω termination resistors may be needed on the XTX signals at the host's end.
- Best performance will result when SerDes traces are placed using the following design rules:
  - Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
  - Traces should be of equal length (within 30 mils) on each differential pair to minimize skew.
  - Traces should be run adjacent to a single ground plane to match impedance and minimize noise.
  - Spacing equal to five times the ground-plane gap between adjacent tracks is recommended to reduce cross-talk between SerDes pairs. A minimum spacing of three times the ground-plane gap is required.
  - Traces should avoid vias and layer changes. If layer changes cannot be avoided, mode-suppression vias should be included next to the signal vias to attenuate any radiating spurious fields.
  - Guard vias should be placed no greater than one-quarter wavelength apart around the differential pair tracks.

FIGURE 6-1: XAUI CONNECTIONS

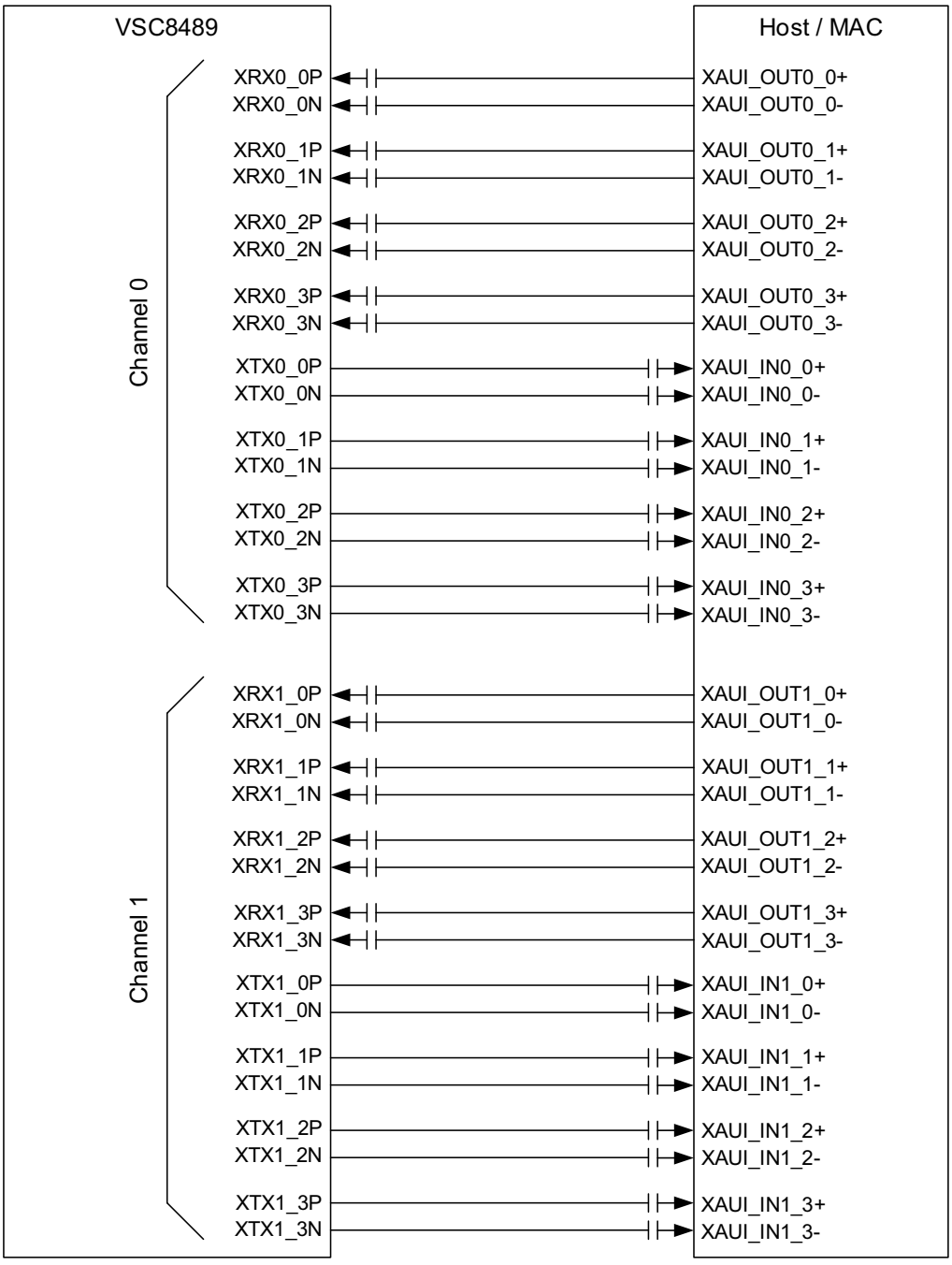


FIGURE 6-2: RXAUI CONNECTIONS

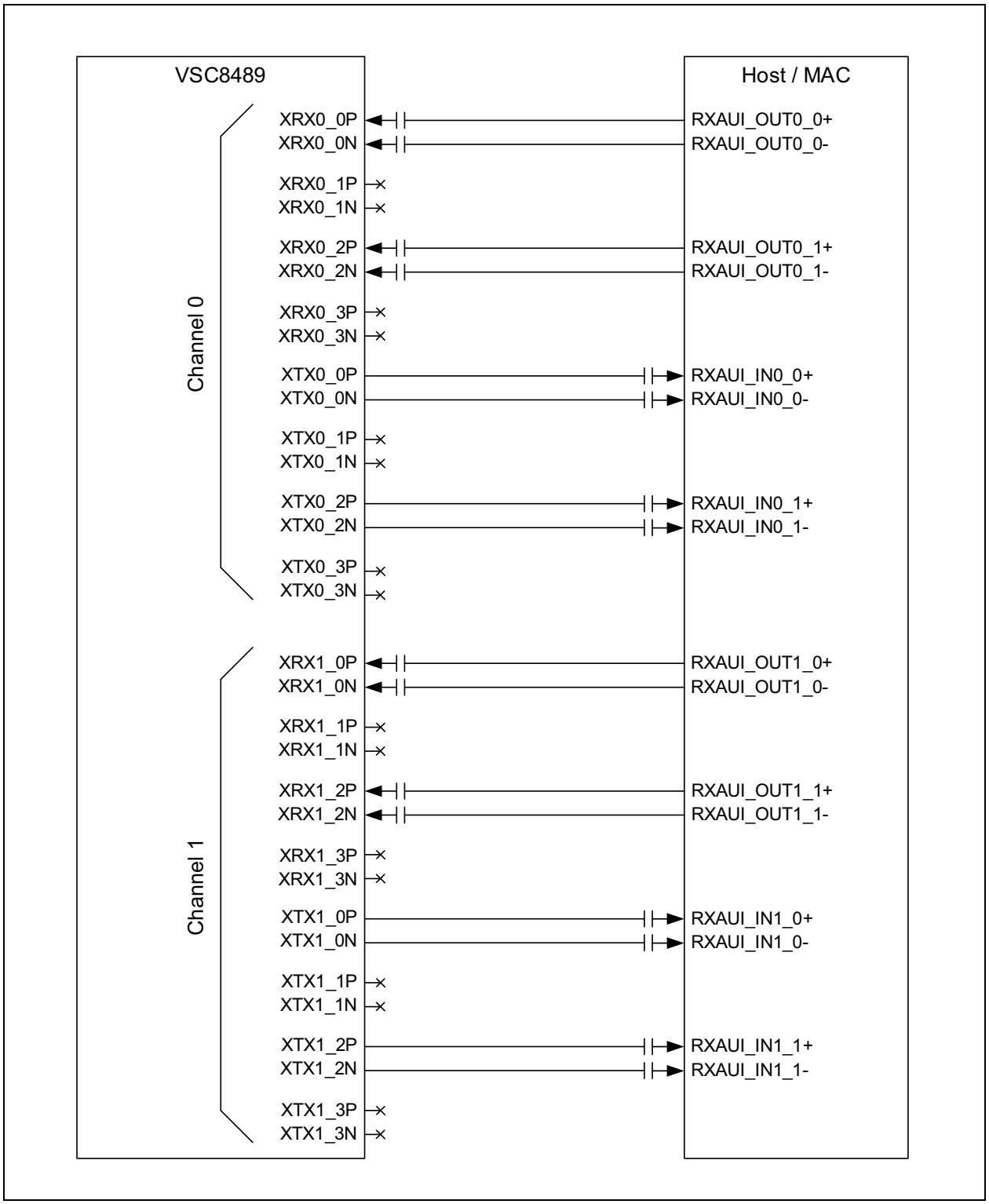
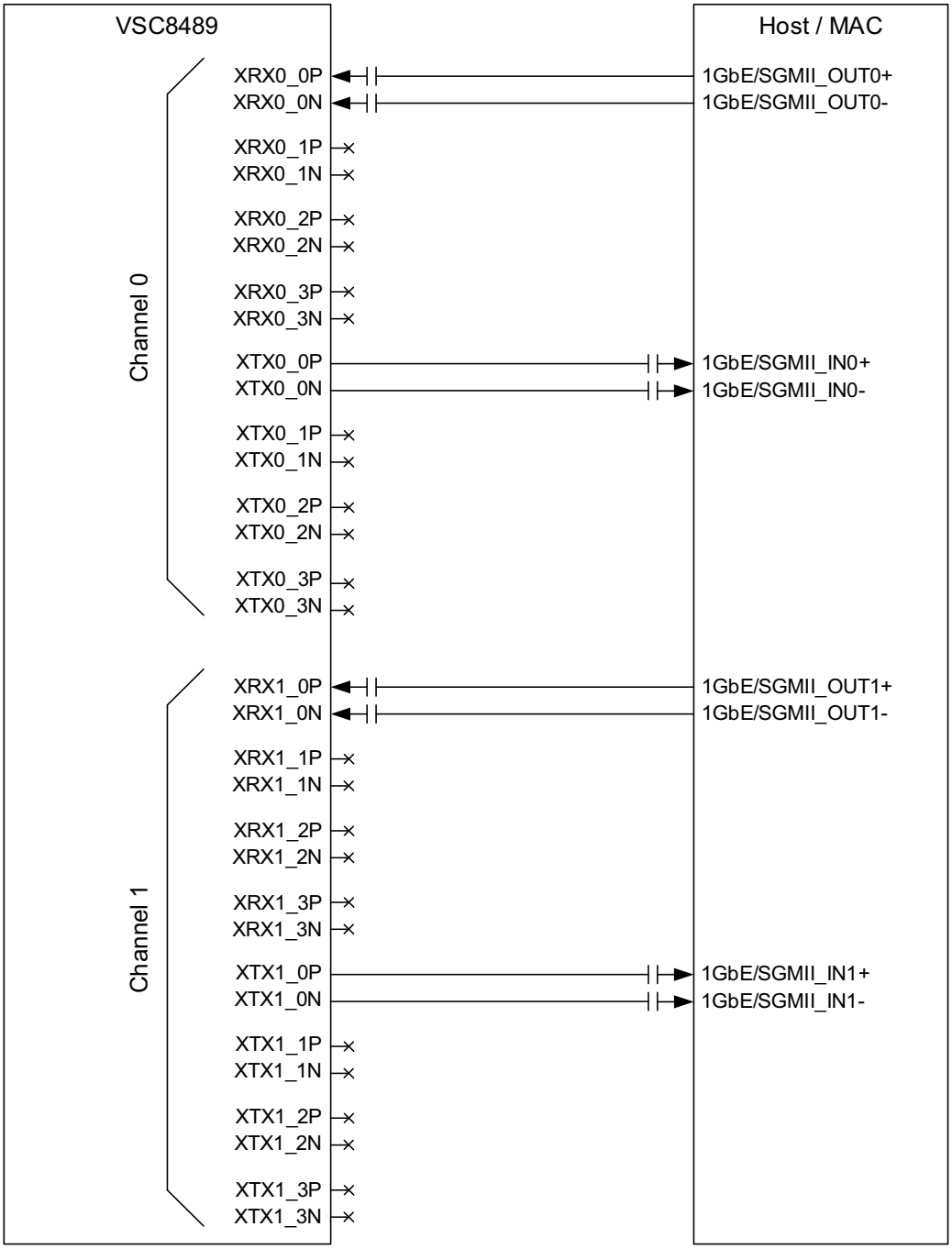


FIGURE 6-3: 1GBE/SGMII CONNECTIONS



Note: Either lane 0 or lane 3 may be used for 1GbE/SGMII.

7.0 REFERENCE CLOCKS

- Table 7-1 shows information on reference clocks.

TABLE 7-1: REFERENCE CLOCKS

Pin Name	Pin Number	Type	Level	Description
WREFCKN	J14	I	CML	WAN reference clock input, complement
WREFCKP	H14	I	CML	WAN reference clock input, true
XREFCKN	F14	I	CML	Reference clock input, complement
XREFCKP	F13	I	CML	Reference clock input, true
SREFCKN	J12	I	CML	SyncE reference clock input, complement
SREFCKP	H12	I	CML	SyncE reference clock input, true
MODE0	K11	I	LVTTL	Mode select input bit 0
MODE1	M9	I	LVTTL	Mode select input bit 1

7.1 Device Reference Clocks

The VSC8489 has three reference clock inputs, **WREFCK**, **XREFCK**, and **SREFCK**. SyncE applications may use either one or two clocks, while non-SyncE applications use only **XREFCK**. Using all three reference clocks is unnecessary.

- **WREFCK_P/N** may be used for one configuration of WAN plus SyncE as shown in Table 7-2.
- **XREFCK_P/N** is a required reference clock for all operating modes. The frequency may be either 125 MHz or 156.25 MHz. **XREFCK** may be an ordinary oscillator for non-SyncE applications or a hitless (DPLL) clock for SyncE applications. The clock speed is set by the MODE1 input. Users must take note of the following when setting the clock speed:
  - Pull MODE1 low for 156.25 MHz.
  - Pull MODE1 high for 125 MHz.
  - MODE0 must always be pulled low.
- **SREFCK_P/N** may be used for certain SyncE applications, but it is not required for SyncE. See Section 7.2, "Synchronous Ethernet" for more details.

Table 7-2 lists reference clock configurations for different modes:

TABLE 7-2: REFERENCE CLOCK CONFIGURATIONS

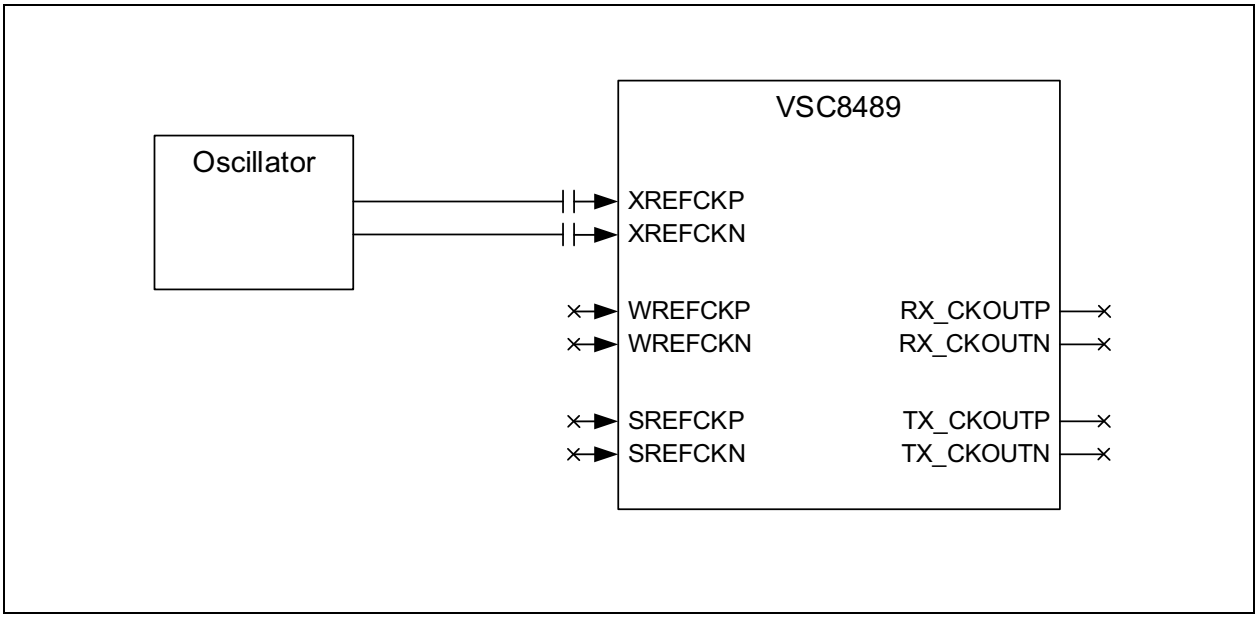
Mode	XREFCK	WREFCK	SREFCK	TX CMU REF	RX CMU REF
10.3125G LAN Single Ref.	156.25 MHz	—	—	XREFCK	XREFCK
9.95328G WAN Single Ref.	156.25 MHz	—	—	XREFCK	XREFCK
1.25G LAN Single Ref.	156.25 MHz	—	—	XREFCK	XREFCK
10.3125G LAN Single Ref.	125 MHz	—	—	XREFCK	XREFCK
9.95328G WAN Single Ref.	125 MHz	—	—	XREFCK	XREFCK
1.25G LAN Single Ref.	125 MHz	—	—	XREFCK	XREFCK
10.3125G Sync-E LAN Single Ref.	156.25 MHz (Hitless)	—	—	XREFCK	XREFCK
10.3125G Sync-E LAN Dual Ref.	156.25 MHz	—	161.13 MHz	SREFCK	XREFCK
	156.25 MHz	—	156.25 MHz	SREFCK	XREFCK
	156.25 MHz	—	125 MHz	SREFCK	XREFCK
9.95328G Sync-E WAN Single Ref.	156.25 MHz (Hitless)	—		XREFCK	XREFCK
9.95328G Sync-E WAN Dual Ref.	156.25 MHz	—	155.52 MHz	SREFCK	XREFCK
9.95328G Sync-E WAN Dual Ref.	156.25 MHz	155.52 MHz	—	WREFCK	WREFCK

TABLE 7-2: REFERENCE CLOCK CONFIGURATIONS (CONTINUED)

Mode	XREFCK	WREFCK	SREFCK	TX CMU REF	RX CMU REF
1.25G Sync-E LAN Single Ref.	156.25 MHz (Hitless)	—	—	XREFCK	XREFCK

- Users must ensure that the following are executed when using reference clocks:
  - Meet the jitter requirements from the data sheet.
  - Meet the amplitude specifications given in the data sheet. Note that **XREFCK_P/N** and **WREFCK_P/N** are configurable for either high-swing or low-swing inputs. An API call is used to configure it. **SREFCK_P/N** has a single amplitude range.
  - Traces are routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
  - Use AC coupling with 0.1 µF capacitors. Capacitors are best placed close to the reference clock input pins.
  - For some clock drivers, make sure that termination resistors are placed on the clock driver side. Termination resistors are not typically needed on the VSC8489 side of the capacitors.
  - All reference clocks must be free from glitches or must be hitless.
  - Unused reference clocks can be left floating (no-connect). See Figure 7-1.

FIGURE 7-1: REFERENCE CLOCK FOR NON-SYNCE



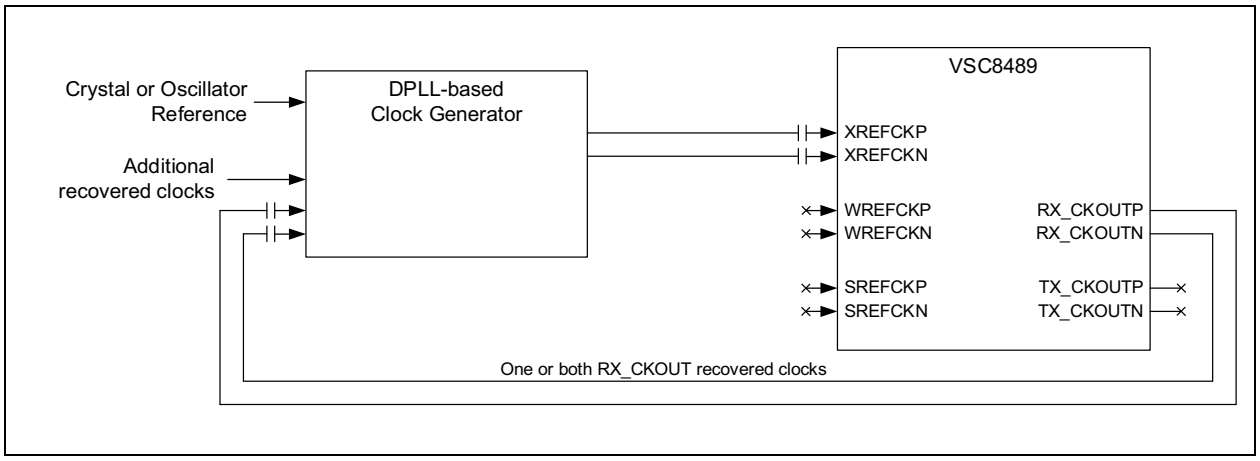
7.2 Synchronous Ethernet

There are multiple ways to implement clocking for Synchronous Ethernet. The two main ways are SyncE with Single Reference Clock and SyncE with non-hitless XREFCK, LAN Mode.

7.2.1 SYNCE WITH SINGLE REFERENCE CLOCK

- **Single clock LAN, external master:** In this configuration, a hitless (DPLL) clock chip drives **XREFCK**. The clock changes gradually to match an externally referenced synchronous Ethernet clock. The change must be hitless to avoid data corruption. One of the port recovered clocks, output on the **RXCKOUT** pins, can be used as reference to the clock chip. **WREFCK** and **SREFCK** are not used. See Figure 7-2.

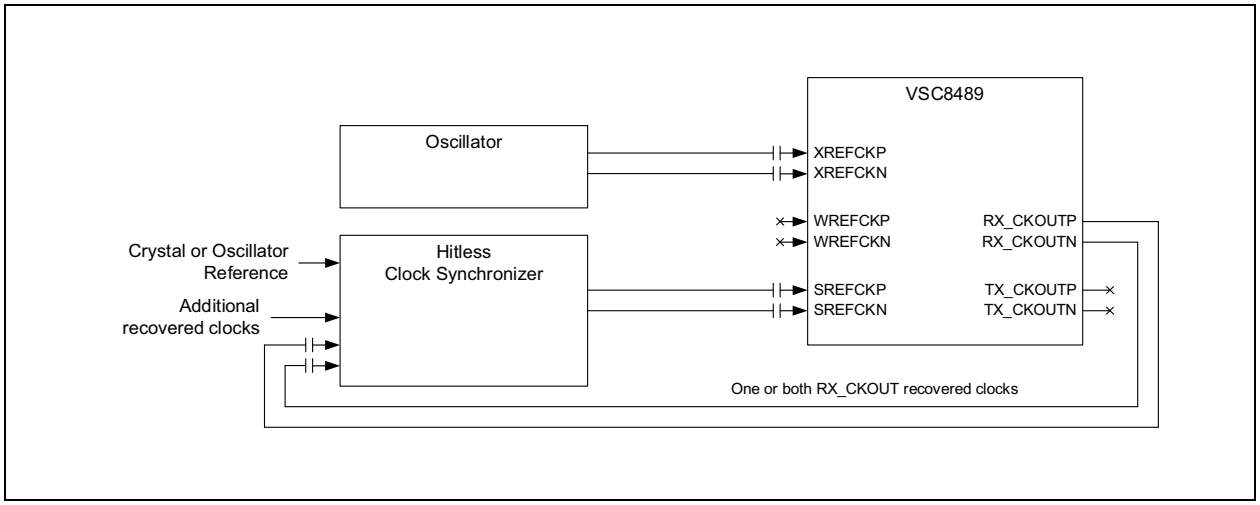
FIGURE 7-2: TYPICAL SYNCE CLOCK CONFIGURATION



7.2.2 SYNCE WITH NON-HITLESS XREFCK, LAN MODE

- **Dual clock LAN, external master:** In this configuration, the **XREFCK** remains connected to the stable 156.25 MHz system clock. All the line-side transmits are then synchronized to **SREFCK**. The F to delta F block accepts the **SREFCK** clock from external synchronous Ethernet master and generates the lane Sync signal to effectively synchronize all the line-side **TX** to this external clock. **SREFCK** must be 156.25 MHz. See Figure 7-3.

FIGURE 7-3: ALTERNATE SYNCE CLOCK CONFIGURATION



7.3 Output Clocks

- The output clocks of this device are specified in Table 7-3.

TABLE 7-3: OUTPUT CLOCKS

Name	Number	Type	Level	Description
RX0CKOUTN	A8	O	CML	Selectable clock output channel 0, complement. See register device 1, address A008.
RX0CKOUTP	B8	O	CML	Selectable clock output channel 0, true. See register device 1, address A008.
RX1CKOUTN	P7	O	CML	Selectable clock output channel 1, complement. See register device 1, address A008.
RX1CKOUTP	N7	O	CML	Selectable clock output channel 1, true. See register device 1, address A008.
TX0CKOUTN	A10	O	CML	Selectable clock output channel 0, complement. See register device 1, address A009.
TX0CKOUTP	B10	O	CML	Selectable clock output channel 0, true. See register device 1, address A009.
TX1CKOUTN	P9	O	CML	Selectable clock output channel 1, complement. See register device 1, address A009.
TX1CKOUTP	N9	O	CML	Selectable clock output channel 1, true. See register device 1, address A009.

- **RX0CKOUT** and **RX1CKOUT** can be used to output the line-side **RX** recovered clock for each port. Alternatively, they can output the line-side **TX** clock or host-side **RX** recovered clock.
- **TX0CKOUT** and **TX1CKOUT** can be used to output the line-side **TX** clock for each port. Alternatively, they can output the line-side **RX** recovered clock or the host-side **RX** recovered clock.
- For 10G LAN mode, the only available output frequency is 161.1328125 MHz. For 10G WAN mode, the only available frequency is 155.52 MHz. For 1G mode, the only available output frequency is 125 MHz. Take note of the following guidelines:
  - Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
  - Use AC coupling with 0.1 µF capacitors. Capacitors are best placed close to the reference clock input pins.
  - Any unused output clocks can be left floating (no-connect).

8.0 MISCELLANEOUS

8.1 Reset

- The VSC8489 must be reset at power-up. One option is to hold **RESETN** low for a minimum 1 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **RESETN** low for a minimum 1 ms after power up. **RESETN** is typically driven by a voltage monitor device or by the management processor or FPGA. See Table 8-1 for more information on the reference clocks.

TABLE 8-1: RESET PIN

Pin Name	Pin Number	Type	Level	Description
RESETN	C6	I	LVTTL	Reset. Low = Reset. Internally pulled high.

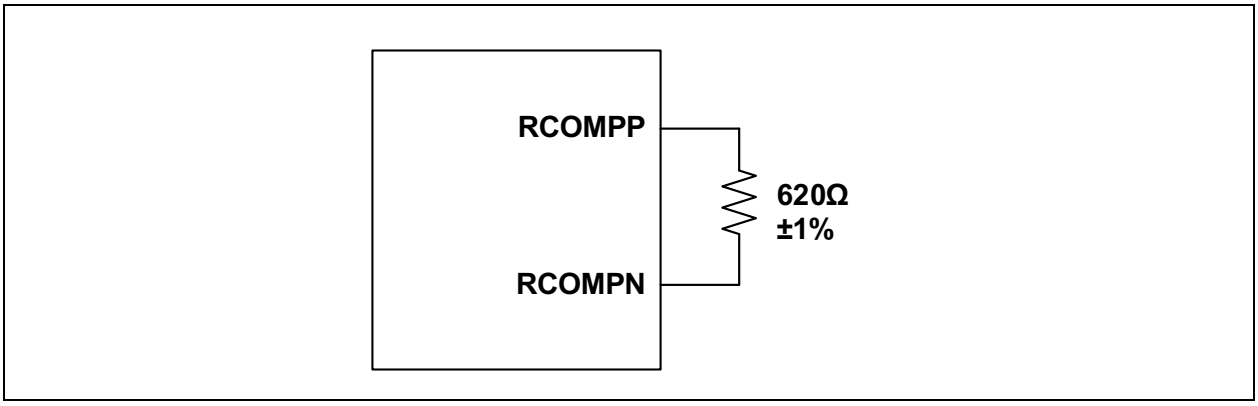
8.2 Reference Resistor

- Connect a 620Ω ±1% resistor between **RCOMPN** and **RCOMPP** as shown in Figure 8-1. Refer to Table 8-2 for additional details on the pins.

TABLE 8-2: REFERENCE RESISTORS

Pin Name	Pin Number	Type	Level	Description
RCOMPN	M11	—	Analog	Resistor comparator, complement
RCOMPP	L11	—	Analog	Resistor comparator, true

FIGURE 8-1: RCOMP RESISTOR



8.3 Serial Management Interfaces (SMI)

- The VSC8489 has SPI and MDIO management interfaces. Only one can be used at a time.
- SPI has the advantage of higher bandwidth and native addressing for 32-bit registers. (MDIO uses 16-bit data transfers, but the registers are 32 bits.)
- SPI is considered essential for MACSec or two-step 1588 due to performance reasons. MDIO performance is suitable for one-step 1588.
- Make sure to wait at least 105 ms after the rising edge of **RESETN** before initiating an SMI activity.
- A Two-Wire (I^2C) management interface is also available via **GPIO_2** and **GPIO_3** pins. However, it is not supported in the software API and is not recommended.

8.3.1 SPI MANAGEMENT INTERFACE

- The SPI interface is the recommended interface for managing the VSC8489, especially for two-step IEEE 1588 and MACSec applications. See the Design Considerations section of the data sheets specified in Section 2.1, "Required References" for the maximum SPI frequency. This interface operates at 2.5V but is 3.3V tolerant. Refer to Table 8-3 for pin information.
- If the SPI interface is unused, pull the input pins to **VDDTTL**.

TABLE 8-3: SPI MANAGEMENT PINS

Pin Name	Pin Number	Type	Level	Description
MISO	E11	O	LVTTL	SPI slave data output
MOSI	E9	I	LVTTL	SPI slave data input
SCK	D11	I	LVTTL	SPI slave clock input
SSN	D9	I	LVTTL	SPI slave chip select input

8.3.2 MDIO MANAGEMENT INTERFACE

- The maximum MDIO frequency is 2.5 MHz. This interface operates at 2.5V but is 3.3V tolerant.
- A pull-up resistor (~2 kΩ) is required on MDIO. Depending on the master device, a pull-up may also be needed on MDC.
- If multiple devices are on this bus, ensure that each device has a unique MDIO address as determined by the **PADDR[4:1]** pins.
- If the MDIO interface is unused, the pins can be left floating (no-connect). Refer to Table 8-4 for detailed information on **MDIO** pins.

TABLE 8-4: MDIO MANAGEMENT

Pin Name	Pin Number	Type	Level	Description
MDC	D7	I	LVTTL	MDIO clock input
MDIO	E7	B	LVTTLOD	MDIO data I/O
PADDR1	D10	I	LVTTL	MDIO port address bit 1. Internally pulled low.
PADDR2	C8	I	LVTTL	MDIO port address bit 2. Internally pulled low.
PADDR3	E10	I	LVTTL	MDIO port address bit 2. Internally pulled low.
PADDR4	E6	I	LVTTL	MDIO port address bit 2. Internally pulled low.

8.4 IEEE 1588 Signals

- The VSC8489-17 and VSC8489-16 support IEEE 1588, while the VSC8489-02 does not. For the VSC8489-02, leave all these pins floating (no-connect). See Table 8-5 for pin information.

TABLE 8-5: IEEE 1588 SIGNALS

Pin Name	Pin Number	Type	Level	Description
CLK1588N	E8	I	CML	1588 logic clock input, complement
CLK1588P	D8	I	CML	1588 logic clock input, true
SPI_CLK	K7	O	LVTTL	Push-out SPI clock output for 1588 timestamp
SPI_CS	L10	O	LVTTL	Push-out SPI chip select output for 1588 timestamp
SPI_DO	L7	O	LVTTL	Push-out SPI data output for 1588 timestamp

8.4.1 1588 LOGIC CLOCK

- The **CLK1588_P/N** input clock is used in most IEEE 1588 applications to clock the Local Time Counter (LTC). While it is also possible for the LTC to reference a data path clock or the host-side PLL instead of CLK1588_P/N, these options are not typically used.
- Design guidelines for **CLK1588_P/N** are as follows:

- **CLK1588_P/N** supported frequencies are 125, 156.25, 200, and 250 MHz.
- For 1588 boundary clock applications, **CLK1588** is typically supplied by a PLL-based reference.
- For 1588 transparent clock applications, **CLK1588** should be sourced from a frequency locked clock that is common to all other timestamping interfaces
- Traces should be routed as 50Ω (100Ω differential) controlled impedance transmission lines (microstrip or stripline).
- Use AC coupling with 0.1 µF capacitors. Capacitors are best located close to the destination.
- The clock inputs are internally terminated, so external resistors are not needed.
- If **CLK1588_P/N** are unused, they can be left floating (no-connect).

8.4.2 PUSH OUT SPI MASTER INTERFACE

- Serial time stamps can be pushed out on the **SPI_CLK**, **SPI_CS**, and **SPI_DO** output pins. This interface is more often used in two-step 1588 mode because of the higher rate of timestamps needing to be processed by the external processor or FPGA. For applications such as one-step transparent clock, it is typically not used. If unused, these pins can be left floating (no-connect). The signals are 2.5V LVTTL.

8.4.3 GPIO SIGNALS FOR 1588

- Several GPIO pins may be configured for 1588-specific functions as summarized in Table 8-6.

TABLE 8-6: GPIO PINS FOR 1588 FUNCTIONS

Pin	Function	Requirements
GPIO_0	1588-1PPS channel 0	Open-drain output, pull-up required if used
GPIO_1	1588-load/save	Input
GPIO_4	1588-1PPS channel 1	Open-drain output, pull-up required if used
GPIO_5	1588-PPS RI	Input
GPIO_9	1588-1PPS channel 1	Open-drain output, pull-up required if used
GPIO_11	1588-1PPS channel 1	Open-drain output, pull-up required if used

8.5 GPIO Pins

- The VSC8489 has 16 **GPIO** pins which may be used for general purpose I/O or for dedicated functions. Refer to Table 8-7 and Table 8-8.
- When used as outputs, these pins are open-drain and require a 2-kΩ-to-10-kΩ pull-up resistor.
- Any unused **GPIO** pins can be left floating (no-connect).
- When configured to an LED mode, a **GPIO** output is active low. Power for LEDs should be 3.3V, with a load resistor in series.

TABLE 8-7: GPIO PINS

Pin Name	Pin Number	Type	Level	Description
GPIO_0	D4	B	LVTTLOD	General purpose I/O 0
GPIO_1	D5	B	LVTTLOD	General purpose I/O 1
GPIO_2	E4	B	LVTTLOD	General purpose I/O 2
GPIO_3	E5	B	LVTTLOD	General purpose I/O 3
GPIO_4	F4	B	LVTTLOD	General purpose I/O 4
GPIO_5	F5	B	LVTTLOD	General purpose I/O 5
GPIO_6	K4	B	LVTTLOD	General purpose I/O 6
GPIO_7	K5	B	LVTTLOD	General purpose I/O 7
GPIO_8	K6	B	LVTTLOD	General purpose I/O 8
GPIO_9	L4	B	LVTTLOD	General purpose I/O 9
GPIO_10	L5	B	LVTTLOD	General purpose I/O 10

TABLE 8-7: GPIO PINS (CONTINUED)

Pin Name	Pin Number	Type	Level	Description
GPIO_11	L6	B	LVTTLOD	General purpose I/O 11
GPIO_12	C10	B	LVTTLOD	General purpose I/O 12
GPIO_13	C11	B	LVTTLOD	General purpose I/O 13
GPIO_14	N11	B	LVTTLOD	General purpose I/O 14
GPIO_15	P11	B	LVTTLOD	General purpose I/O 15

TABLE 8-8: GPIO FUNCTIONS

Pin	Configuration Registers	Function
GPIO_0	GPIO_0_Config_Status GPIO_0_Config2	Traditional I/O (default) Observed internal signals MOD_ABS_Channel_0 PMTICK ROSI frame pulse 0 TX Activity LED WIS_INTB 1588-1PPS channel 0 Leave unconnected when not used.
GPIO_1	GPIO_1_Config_Status GPIO_1_Config2	Traditional I/O (default) Observed internal signals ROSI_CLK_0 RX Activity LED WIS_INTA 1588-Load/Save Leave unconnected when not used.
GPIO_2	GPIO_2_Config_Status GPIO_2_Config2	Traditional I/O Observed internal signals Slave Two-Wire serial – SDA (default) ROSI_DATA_0 TX Activity LED WIS_INTB
GPIO_3	GPIO_3_Config_Status GPIO_3_Config2	Traditional I/O Observed internal signals Slave Two-Wire serial – SCL (default) TOSI_FRAME_PULSE_0 RX Activity LED WIS_INTB
GPIO_4	GPIO_4_Config_Status GPIO_4_Config2	Traditional I/O (default) Observed internal signals TOSI_CLK_0 TX Activity LED WIS_INTB 1588-1PPS channel 1
GPIO_5	GPIO_5_Config_Status GPIO_5_Config2	Traditional I/O (default) Observed internal signals TOSI_INPUT_0 RX Activity LED WIS_INTA 1588-PPS RI Leave unconnected when not used.

TABLE 8-8: GPIO FUNCTIONS (CONTINUED)

GPIO_6	GPIO_6_Config_Status GPIO_6_Config2	Traditional I/O (default) Observed internal signals Ch0 SFP 12C SDA ROSI_FRAME_PULSE_1 TX Activity LED WIS_INTB
GPIO_7	GPIO_7_Config_Status GPIO_7_Config2	Traditional I/O (default) Observed internal signals Ch0 SFP 12C SCL ROSI_CLK_1 RX Activity LED WIS_INTA
GPIO_8	GPIO_8_Config_Status GPIO_8_Config2	Traditional I/O (default) Observed internal signals MOD_ABS_Channel_0 PMTICK ROSI_DATA_1 TX Activity LED WIS_INTA
GPIO_9	GPIO_9_Config_Status GPIO_9_Config2	Traditional I/O (default) Observed internal signals MOD_ABS_Channel_1 PMTICK TOSI_FRAME_PULSE_1 RX Activity LED WIS_INTA 1588-1PPS channel 1
GPIO_10	GPIO_10_Config_Status GPIO_10_Config2	Traditional I/O (default) Observed internal signals Ch1 SFP 12C SDA TOSI_CLK_1 TX Activity LED WIS_INTB
GPIO_11	GPIO_11_Config_Status GPIO_11_Config2	Traditional I/O (default) Observed internal signals Ch1 SFP 12C SCL TOSI_INPUT_1 RX Activity LED WIS_INTA 1588-1PPS channel 1
GPIO_12	GPIO_12_Config_Status GPIO_12_Config2	Traditional I/O (default) Observed internal signals TX Activity LED WIS_INTA
GPIO_13	GPIO_13_Config_Status GPIO_13_Config2	Traditional I/O (default) Observed internal signals RX Activity LED WIS_INTA
GPIO_14	GPIO_14_Config_Status GPIO_14_Config2	Traditional I/O (default) Observed internal signals TX Activity LED WIS_INTA
GPIO_15	GPIO_15_Config_Status GPIO_15_Config2	Traditional I/O (default) Observed internal signals RX Activity LED WIS_INTA

8.6 JTAG

- If JTAG is not used, **TRSTB** should be pulled low. The other pins may be left floating (no connect). See Table 8-9 for JTAG pin information.

TABLE 8-9: JTAG PINS

Pin Name	Pin Number	Type	Level	Description
TCK	K9	I	LVTTL	Boundary scan, test clock input. Internally pulled high.
TDI	L8	I	LVTTL	Boundary scan, test data input. Internally pulled high.
TDO	K8	O	LVTTL	Boundary scan, test data output
TMS	M5	I	LVTTL	Boundary scan, test mode select. Internally pulled high.
TRSTB	K10	I	LVTTL	Boundary scan, test Reset input. Internally pulled high.

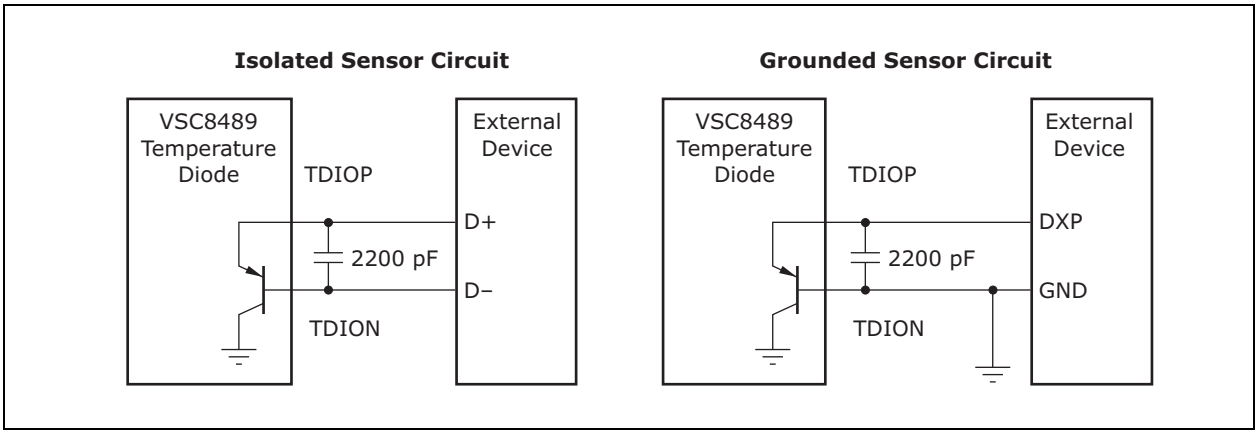
8.7 Temperature Sensor Diode

- The temperature sensor diode pins provide access to an on-die diode and internal circuitry for monitoring die temperature. (See Table 8-10.) To use it, connect an external thermal sensor, located on the board or in a stand-alone measurement kit.
- The cathode is connected internally to ground, so the temperature sensor must be chosen accordingly.
- Temperature measurement using a thermal diode is very sensitive to noise. Figure 8-2 illustrates a generic application design.

TABLE 8-10: TEMPERATURE SENSOR PINS

Pin Name	Pin Number	Type	Level	Description
TDION	B7	—	Analog	Temperature diode, negative (cathode)
TDIOP	A7	—	Analog	Temperature diode, positive (anode)

FIGURE 8-2: THERMAL DIODE CONNECTIONS



8.8 Unused Pins

- Follow the instructions given for these unused pins in Table 8-11.

TABLE 8-11: UNUSED PINS

Pin Name	Pin Number	Type	Level	Description
NC	M8	—	—	No connect (formerly labeled as ANATEST)
SCAN_EN	L9	I	LVTTL	Scan enable input, factory test purposes only. Keep connected to ground.

NOTES:

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	All ground pins connect to a single ground. Solid ground planes should be used.		
Section 3.0, "Power"	Section 3.1, "Current Requirements"	Ensure that the power rails can supply adequate current.		
	Section 3.2, "Power Supply Planes"	Make sure that the analog planes are filtered with ferrite beads, while digital planes are not. Consider possible resistive voltage drop in distribution.		
	Section 3.3, "Analog Power Plane Filtering"	Check if each analog power rail has ferrite bead filtering, with bulk capacitors on both sides of the bead and one capacitor near each power pin. Ferrite beads must meet current and DC resistance requirements. Consider DC voltage drop across the ferrite beads.		
	Section 3.4, "Decoupling Capacitors"	Ensure that there is one decoupling capacitor near each power pin and at least a 10 µF bulk capacitor per rail. See Figure 3-1.		
Section 4.0, "Thermal Considerations"		Do not use thermal relief for ground vias.		
Section 5.0, "Media SerDes Interface"	Section 5.1, "Media SerDes Design Rules"	Unless common mode voltages are compatible, make sure to use AC coupling caps for non-SFP applications. SFP modules include AC coupling. Follow good differential signal layout practices. Pull unused **LOPC** inputs low.		
	Section 5.2, "Connecting to 10G SFP+ or 1G SFP"	Take note that AC coupling caps are not needed. Connect **TXOUT** to **TD** of SFP and **RXIN** to **RD**. SFP single-ended outputs need pull-ups. Consider connecting the SFP Two-Wire and other controls to a host rather than the VSC8489. Other SFP status and control may also connect to the host.		
Section 6.0, "Host Interface (XAUI, RXAUI, and SGMII)"	Section 6.1, "Host Serial Interface Design"	Verify if XAUI uses all four lanes and RXAUI uses lanes 0 and 2. Check if 1GbE uses lane 0 (or 3). Make sure to leave unused lanes floating. Unless Common-mode voltage levels are compatible, use AC coupling. Follow good differential signal layout practices.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Reference Clocks"	Section 7.1, "Device Reference Clocks"	Check the table of clocking modes. **XREFCK** is required for all cases (125 MHz or 156.25 MHz). Usually **WREFCK** and **SREFCK** are not needed. Leave unused input clocks floating. Ensure jitter requirements are met.		
	Section 7.2, "Synchronous Ethernet"	Take note that the most common configurations use a hitless clock source for XREF. Recovered clocks on **RX_CKOUT** can be fed to the hitless clock source. Other configurations are possible and can use **SREFCK**.		
	Section 7.3, "Output Clocks"	The external receiver of the recovered clock for SyncE must be configured for the available output frequency: 10G LAN Mode = 161.1328125 MHz, 10G WAN mode = 155.52 MHz, and 1G mode = 125 MHz.		
Section 8.0, "Miscellaneous"	Section 8.1, "Reset"	Ensure that there is a rising edge on **RESETN** following power rails and clock being up.		
	Section 8.2, "Reference Resistor"	Make sure to connect a 620Ω ±1% resistor between **RCOMPN** and **RCOMPP**.		
	Section 8.3, "Serial Management Interfaces (SMI)"	Remember that among the three options (SPI, Two-Wire, and MDIO), only one can be used at a time. SPI is strongly recommended. MDIO is suitable only if MACSec and two-step 1588 are not used.		
	Section 8.4, "IEEE 1588 Signals"	Make sure to supply a quality clock for **CLK1588** input clock. The push-out SPI interface is only for outputting timestamps to the host processor. Some 1588 functions are available on **GPIO** pins.		
	Section 8.5, "GPIO Pins"	Take note that a variety of functions are available: interrupts, 1588, GPIO, etc. When output, they are open drain and require external pull-ups.		
	Section 8.6, "JTAG"	If JTAG is unused, **TRSTB** should be pulled low and the other JTAG pins can be left unconnected.		
	Section 8.7, "Temperature Sensor Diode"	If used, connect to an external temperature sensor device such as the MCP9902, with **TDIOP** connected to the positive node and **TDION** to the negative node.		
	Section 8.8, "Unused Pins"	Verify if pin L9 is connected to ground. Pin M8 should be left unconnected.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003602A (08-27-20)	Initial release	

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