SY88403BL

3.3V 4.25 Gbps CML Low-Power Limiting Post Amplifier with TTL LOS

Features

- Multi-Rate up to 4.25 Gbps Operation
- 5 mV_{PP} Input Sensitivity
- Low Noise 50Ω CML Data Outputs
  - 800 mV_{PP} Output Swing
  - 60 ps Edge Rates
  - 1ps_{RMS} Typ. Random Jitter
  - 10ps_{PP} Typ. Deterministic Jitter
- Chatter-Free Loss-of-Signal (LOS) Output
  - 3.5 dB Electrical Hysteresis
  - OC-TTL Output with Internal 4.75 kΩ Pull-Up Resistor
- Programmable LOS Sensitivity Using Single External Resistor
- Internal 50Ω Data Input Termination
- TTL /EN Input Allows Feedback from LOS
- Wide Operating Range:
  - Single 3.3V ±10% Power Supply
  - Industrial Temperature Range: −40°C to +85°C
- Available in a 16-pin QFN Package

Applications

- 1.062 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel
- Cable Driver
- Small Form Factor (SFF) and Small Form Factor Pluggable (SFP) Transceivers
- High-Gain Line Driver and Line Receiver

General Description

The SY88403BL is a low-power limiting post amplifier optimized for copper applications. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88403BL quantizes these signals and outputs typically 800 mV_{PP} voltage-limited waveforms.

The SY88403BL operates from a single +3.3V ±10% power supply, over an industrial temperature range of −40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 4.25 Gbps and as small as 5 mV_{PP} can be amplified to drive devices with CML inputs or AC-coupled PECL inputs.

The SY88403BL incorporates a loss-of-signal (LOS) open-collector TTL output with internal 4.75 kΩ pull-up resistor. A programmable loss-of-signal level set pin (LOSLVL) sets the sensitivity of the input amplitude detection.

LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable bar (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts the true output signal without removing the input signal. Typically, 3.5 dB LOS hysteresis is provided to prevent chattering.

Markets

- Copper Interconnect
- Datacom and Telecom
- Storage Area Network (SAN)

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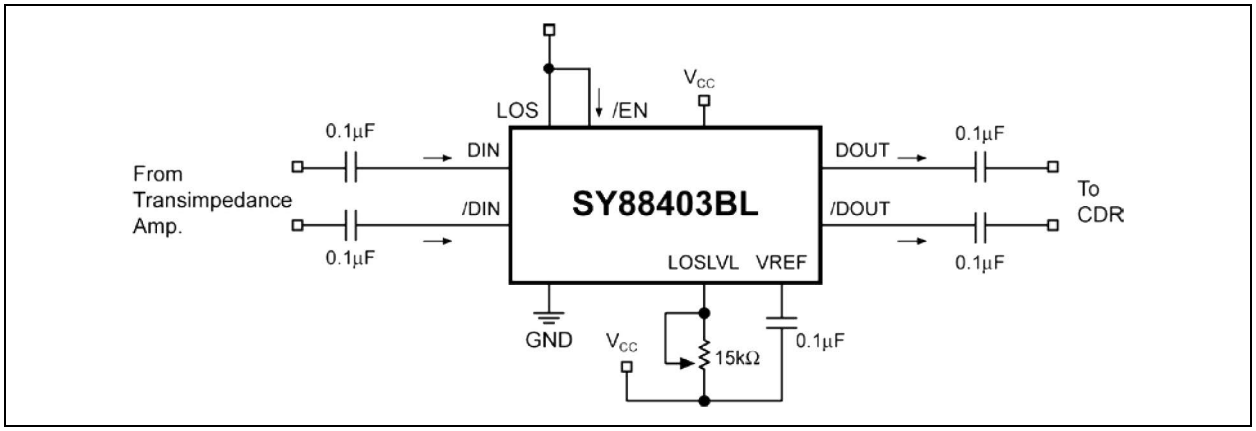
Typical Application Circuit



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... 0V to +7.0V
/EN, LOSLVL Voltage ..... 0V to V_{CC}
REF Current ..... ±1 mA
LOS Current ..... ±5 mA
DOUT, /DOUT Current ..... ±25 mA
DIN, /DIN Current ..... ±10 mA

Operating Ratings ‡

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V

† Notice: Permanent device damage may occur if ratings in the absolute maximum ratings section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

‡ Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V to +3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C; typical values at V_{CC} = +3.3V, T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{CC}	—	25	42	mA	3.3V, Note 1
		—	41	62	mA	3.3V, Note 2
REF Voltage	V_{REF}	—	V_{CC} – 1.3	—	V	—
LOSLVL Voltage Range	V_{LOSLVL}	VREF	—	V_{CC}	V	—
DOUT, /DOUT HIGH Voltage	V_{OH}	V_{CC} – 0.020	V_{CC} – 0.005	V_{CC}	V	Note 3
DOUT, /DOUT LOW Voltage	V_{OL}	V_{CC} – 0.475	V_{CC} – 0.400	V_{CC} – 0.350	V	3.3V, Note 3
DC Differential Output Voltage	V_{OD_DC}	700	800	950	mV	Note 3
Differential Output Offset	V_{OFFSET}	—	—	±80	mV	—
Single-Ended Output Impedance	Z_O	40	50	60	Ω	—
Single-Ended Input Impedance	Z_I	40	50	60	Ω	—

TTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.0V to 3.6V; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
LOS Output HIGH Level	V_{OH}	2.4	—	V_{CC}	V	Sourcing 100 µA
LOS Output LOW Level	V_{OL}	—	—	0.5	V	Sinking 2 mA
/EN Input HIGH Voltage	V_{IH}	2.0	—	—	V	—
/EN Input LOW Voltage	V_{IL}	—	—	0.8	V	—
/EN Input HIGH Current	I_{IH}	—	—	20	µA	V_{IN} = 2.7V
		—	—	100	µA	V_{IN} = V_{CC}
/EN Input LOW Current	I_{IL}	–0.3	—	—	mA	V_{IN} = 0.5V

Note 1: Excludes current of CML output stage. See “Detailed Description.”

2: Total device current with no output load.

3: Output levels are based on a 50Ω to V_{CC} load impedance. If the load impedance is different, the output level will be changed. Amplifier is in limiting mode. Measured at 155 Mbps with 20 mV_{PP} input and PRBS-23 data pattern and 50Ω load.

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AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V to +3.6V; T_A= –40°C to +85°C; R_L = 50Ω to V_{CC}; typical values at V_{CC} = +3.3V, T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Rise/Fall Time (20% to 80%)	t_r, t_f	—	60	120	ps	Note 1
Deterministic Jitter	t_{JITTER}	—	10	—	ps_{PP}	Note 2
Random Jitter		—	1	—	ps_{RMS}	Note 3
Differential Input Voltage Swing	V_{ID}	5	—	1800	mV_{PP}	See Figure 1
AC Differential Output Voltage	V_{OD_AC}	600	800	950	mV_{PP}	Note 4
LOS Release Time	t_{OFF}	—	2	10	µs	—
LOS Assert Time	t_{ON}	—	2	10	µs	—
Low LOS Assert Level	LOS_{AL}	—	8	—	mV_{PP}	R_{LOSLVL} = 15 kΩ, Note 5
Low LOS De-assert Level	LOS_{DL}	—	12	—	mV_{PP}	R_{LOSLVL} = 15 kΩ, Note 5
Low LOS Hysteresis	HYS_L	2	3.5	4.5	dB	R_{LOSLVL} = 15 kΩ, Note 6
Medium LOS Assert Level	LOS_{AM}	12	17	—	mV_{PP}	R_{LOSLVL} = 5 kΩ, Note 5
Medium LOS De-assert Level	LOS_{DM}	—	25	33	mV_{PP}	R_{LOSLVL} = 5 kΩ, Note 5
LOS Hysteresis	HYS_M	2	3.5	4.5	dB	R_{LOSLVL} = 5 kΩ, Note 6
High LOS Assert Level	LOS_{AH}	34	47	—	mV_{PP}	R_{LOSLVL} = 100Ω, Note 5
High LOS De-assert Level	LOS_{DH}	—	70	83	mV_{PP}	R_{LOSLVL} = 100Ω, Note 5
High LOS Hysteresis	HYS_H	2	3.5	4.5	dB	R_{LOSLVL} = 100Ω, Note 6
LOS Sensitivity Range	V_{SR}	20	—	35	mV_{PP}	—
Differential Voltage Gain	$A_{V(DIFF)}$	32	38	—	dB	—
Single-Ended Small-Signal Gain	S_{21}	26	32	—	dB	—

Note 1: Amplifier in limiting mode. Input is a 200 MHz square wave.

2: Deterministic jitter measured using 4.25 Gbps K28.5 pattern, V_{ID} = 20 mV_{PP}.

3: Random jitter measured using 4.25 Gbps K28.7 pattern, V_{ID} = 20 mV_{PP}.

4: Differential output swing measured at 4.25 Gbps with 20 mV_{PP} input and PRBS-23 data pattern and 50Ω load.

5: See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.

6: This specification defines electrical hysteresis as 20log(LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending on the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2 dB to 4.5 dB shown in the AC characteristics table will be 0.5 dB to 3 dB Optical Hysteresis.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+120	°C	—
Ambient Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 2)						
QFN (Still-Air)	θ_{JA}	—	61	—	°C/W	—
QFN	Ψ_{JB}	—	38	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

2: Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

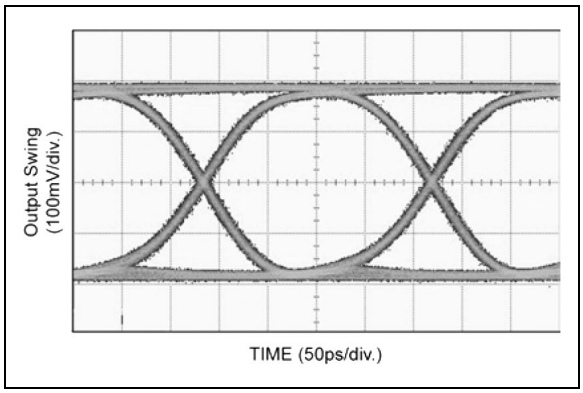

FIGURE 2-1: *3.3V, 25°C 20 mV_{PP} Input @4.25 Gbps 2^{23} – 1 PRBS, R_{LOAD} = 50 to V_{CC}.*

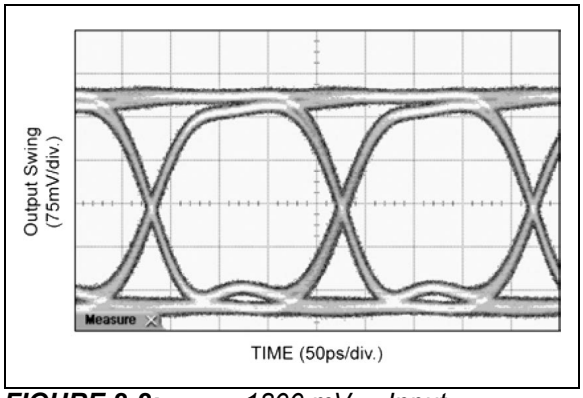

FIGURE 2-2: *1800 mV_{PP} Input @4.25 Gbps 2^{23} – 1 PRBS.*

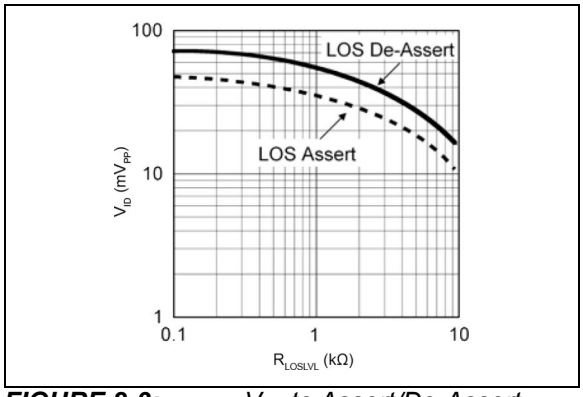

FIGURE 2-3: *V_{ID} to Assert/De-Assert LOS vs. R_{LOSLVL}.*

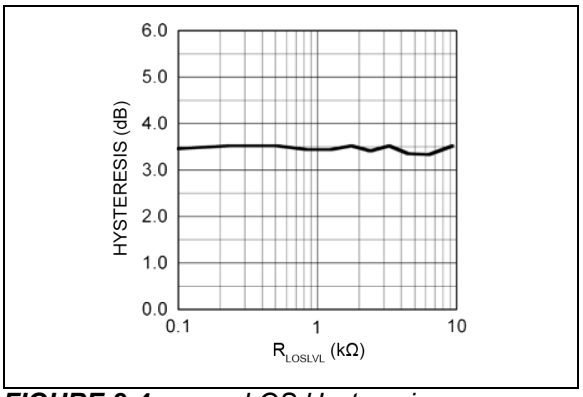

FIGURE 2-4: *LOS Hysteresis vs. R_{LOSLVL}.*

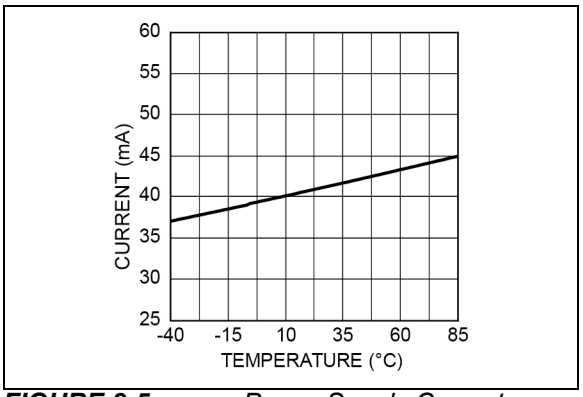

FIGURE 2-5: *Power Supply Current vs. Temperature.*

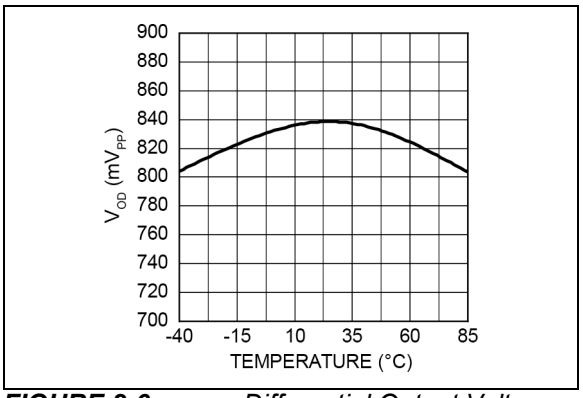

FIGURE 2-6: *Differential Output Voltage Swing vs. Temperature (Amplifier in Limiting Mode).*

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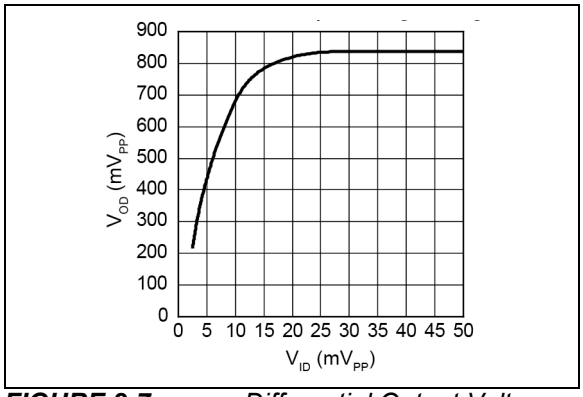
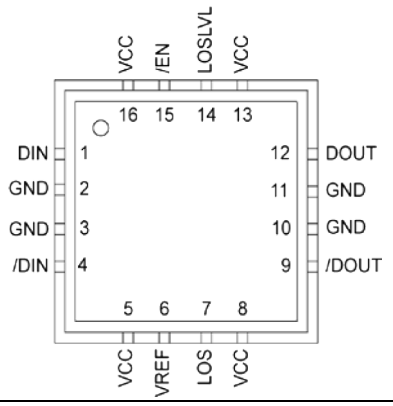


FIGURE 2-7: *Differential Output Voltage Swing vs. Differential Input Voltage Swing.*

3.0 PIN DESCRIPTIONS

Package Type

SY88403BL
16-Pin QFN



The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

QFN Pin Number	Pin Name	Type	Description
1, 4	DIN, /DIN	Differential Data Input	Differential Data Input. Each pin internally terminates to REF through 50Ω.
2, 3,10, 11 Exposed Pad	GND	Ground	Device Ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins.
5, 8, 13, 16	VCC	Power Supply	Positive Power Supply. Bypass with 0.1 µF||0.01 µF low ESR capacitors. 0.01 µF capacitors should be as close as possible to VCC pin.
6	VREF	—	Reference Voltage. Bypass with 0.01µF low ESR capacitor from VREF to VCC to stabilize LOS_{LVL} and V_{REF}.
7	LOS	Open Collector TTL Ouput with Internal 4.75kΩ Pull-Up Resistor	Loss-of-Signal: Asserts high when the data input amplitude falls below the threshold set by LOSLVL.
9, 12	DOUT, /DOUT	Differential CML Output	Differential Data Output.
14	LOSLVL	Input: Default is maxi-mum sensitivity.	Loss-of-Signal Level Set: A resistor from this pin to VCC sets the threshold for the data input amplitude at which the LOS output will be asserted.
15	/EN	TTL Input: Default is high.	Enable Bar: De-asserts true data output when high. Incorporates 25 kΩ pull-up to VCC.

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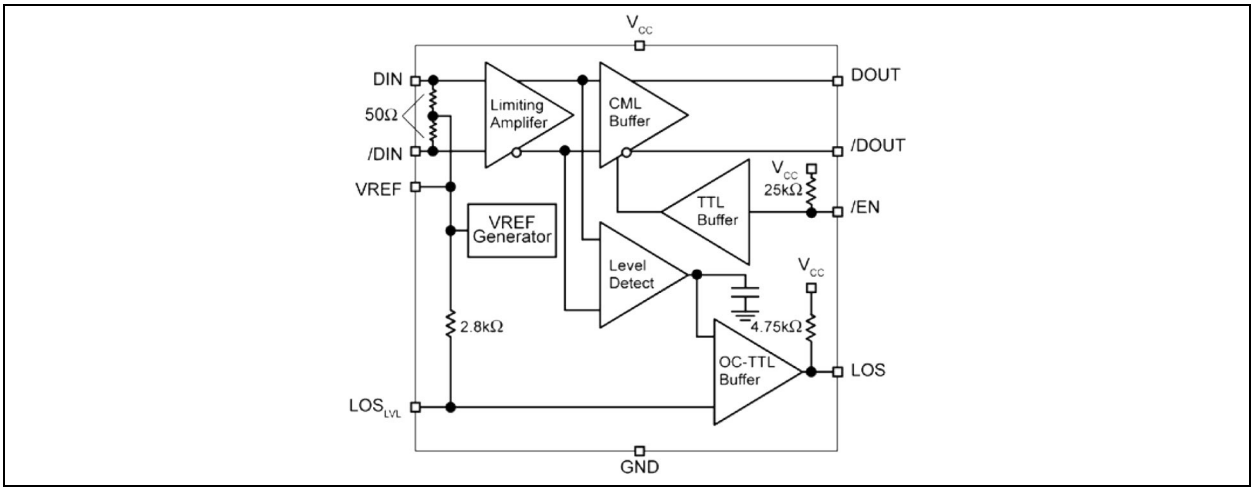
4.0 FUNCTIONAL DESCRIPTION

4.1 Functional Block Diagram



4.2 Detailed Description

The SY88403BL low-power limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 4.25Gbps and as small as 5 mV_{PP} can be amplified. Figure 4-1 shows the allowed input voltage swing. The SY88403BL generates an LOS output, allowing feedback to /EN for output stability. LOSLVL sets the sensitivity of the input amplitude detection.

4.2.1 INPUT AMPLIFIER/BUFFER

The SY88403BL's inputs are internally terminated with 50Ω to REF. If not affected by this internal termination scheme, upstream devices need to be AC-coupled to the SY88403BL's inputs. Figure 4-2 shows a simplified schematic of the input stage.

The high-sensitivity of the input amplifier allows signals as small as 5 mV_{PP} to be detected and amplified. The input amplifier allows input signals as large as 1800 mV_{PP}. Input signals are linearly amplified with a typically 38 dB differential voltage gain. Since it is a limiting amplifier, the SY88403BL outputs typically 800 mV_{PP} voltage-limited waveforms for input signals that are greater than 20 mV_{PP}. Applications requiring the SY88403BL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88403BL's input pins to ensure the best performance of the device.

4.2.2 OUTPUT BUFFER

The SY88403BL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} or equivalent for each output pin provides this. Figure 4-3 shows a simplified schematic of the output stage and includes an appropriate termination method. Of course, driving a downstream device with a CML input that is internally terminated with 50Ω to V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs typically 800 mV_{PP} waveforms across 25Ω total loads. The output buffer thus switches typically 16 mA tail-current. Figure 4-4 shows the power supply current measurement, which excludes the 16 mA tail-current.

4.2.3 LOSS-OF-SIGNAL

The SY88403BL incorporates a chatter-free loss-of-signal (LOS) open-collector TTL output with internal 4.75 kΩ pull-up resistor as shown in Figure 4-5. LOS is used to determine that the input amplitude is too small to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts low the true output signal without removing the input signals. Typically 3.5 dB LOS hysteresis is provided to prevent chattering.

4.2.4 LOSS-OF-SIGNAL LEVEL SET

A programmable loss-of-signal level set pin (LOSLVL) sets the threshold of the input amplitude detection. Connecting an external resistor between VCC and LOSLVL sets the voltage at LOSLVL. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF} as shown in Figure 4-6. If desired, an appropriate external voltage may be applied rather than using a resistor. The relationship between V_{LOSLVL} and R_{LOSLVL} is given by:

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EQUATION 4-1:

$$V_{LOSLVL} = V_{CC} - \left(1.3\frac{R_{LOSLVL}}{R_{LOSLVL} + 2.8}\right)$$

Where:

Voltages are in volts and resistances are in kΩ.

The smaller the external resistor, implying a smaller voltage difference from LOSLVL to VCC, lowers the LOS sensitivity. Hence, larger input amplitude is required to de-assert LOS. “Typical Operating Characteristics” contains graphs showing the relationship between the input amplitude detection sensitivity and R_{LOSLVL}.

4.2.5 HYSTERESIS

The SY88403BL provides typically 3.5 dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V_{IN}^2/R for an electrical signal. Hence the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88403BL provides typically 1.75 dB LOS optical hysteresis. As the SY88403BL is an electrical device, this datasheet refers to hysteresis in electrical terms. With 3.5 dB LOS hysteresis, a voltage factor of 1.5 is required to de-assert LOS.

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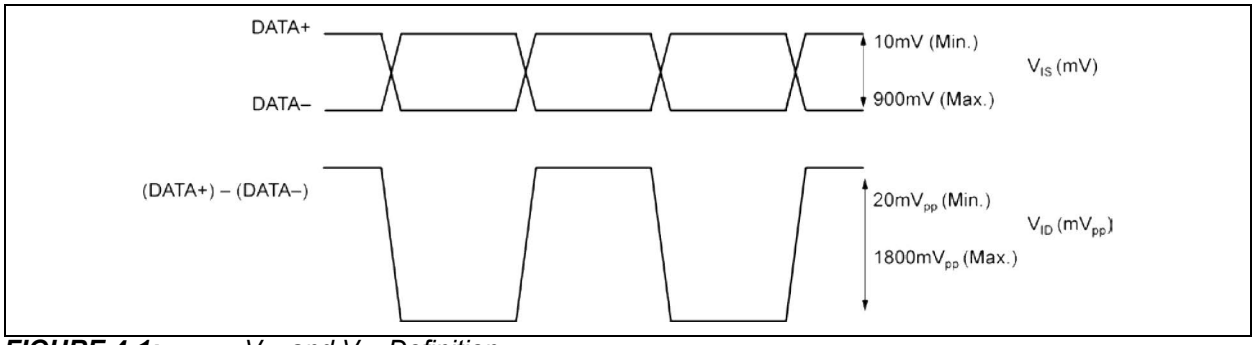


FIGURE 4-1: *V_{IS} and V_{ID} Definition.*

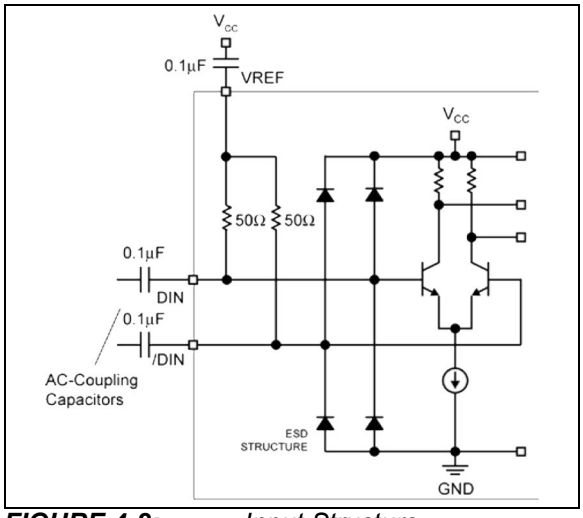


FIGURE 4-2: *Input Structure.*

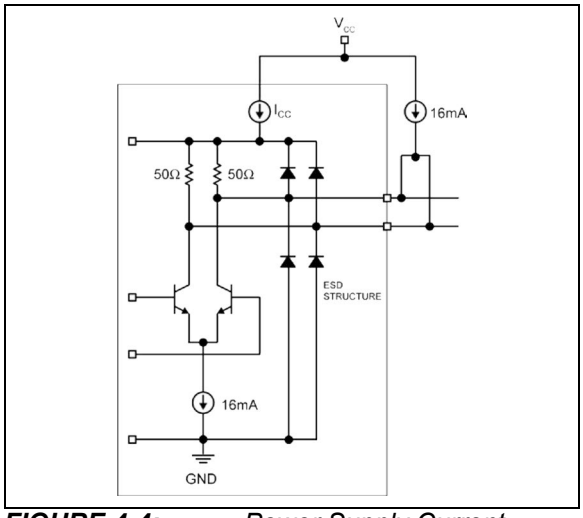


FIGURE 4-4: *Power Supply Current Measurement.*

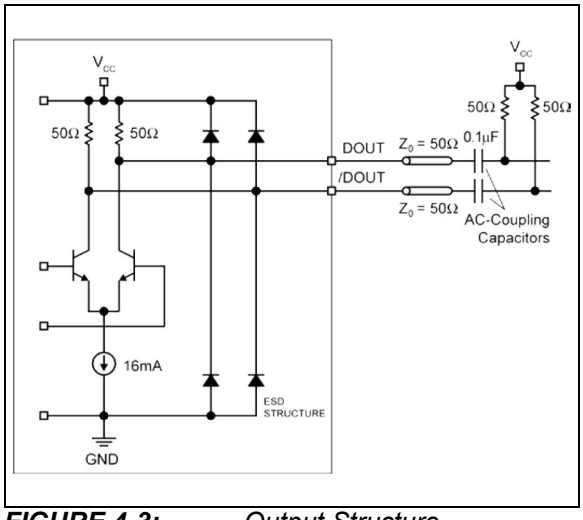


FIGURE 4-3: *Output Structure.*

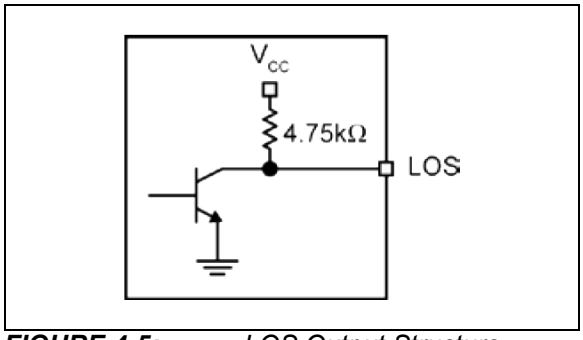


FIGURE 4-5: *LOS Output Structure.*

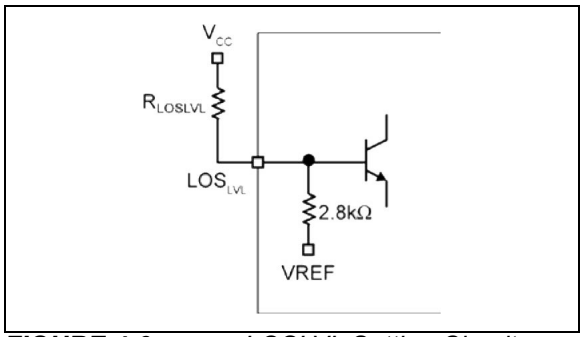
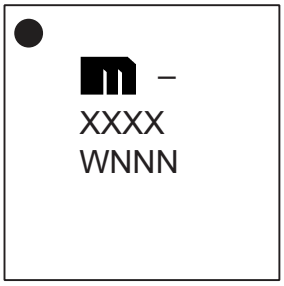


FIGURE 4-6: *LOSLVL Setting Circuit.*

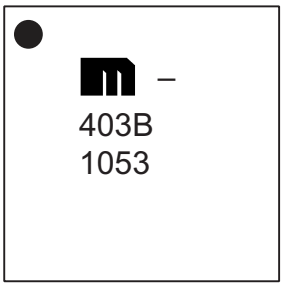
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Lead VQFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

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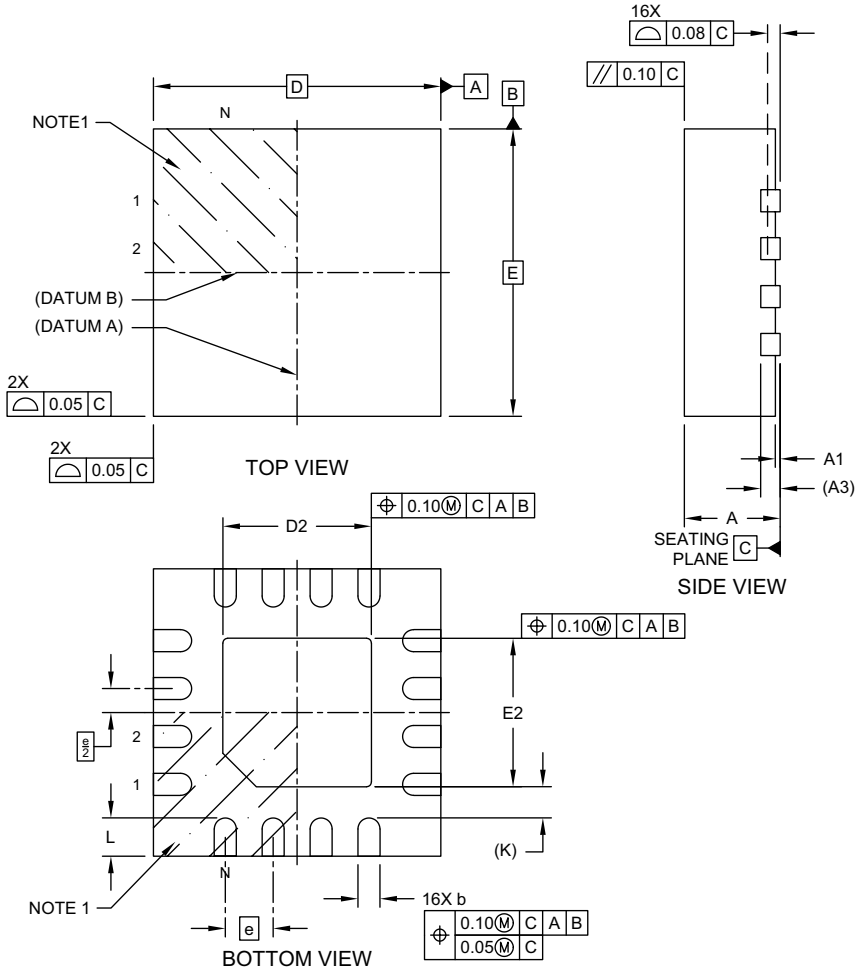
16-Lead QFN Package Outline and Recommended Land Pattern

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev B Sheet 1 of 2

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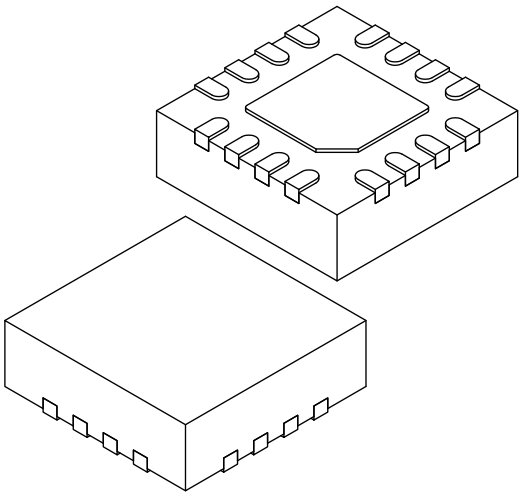
16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev B Sheet 2 of 2

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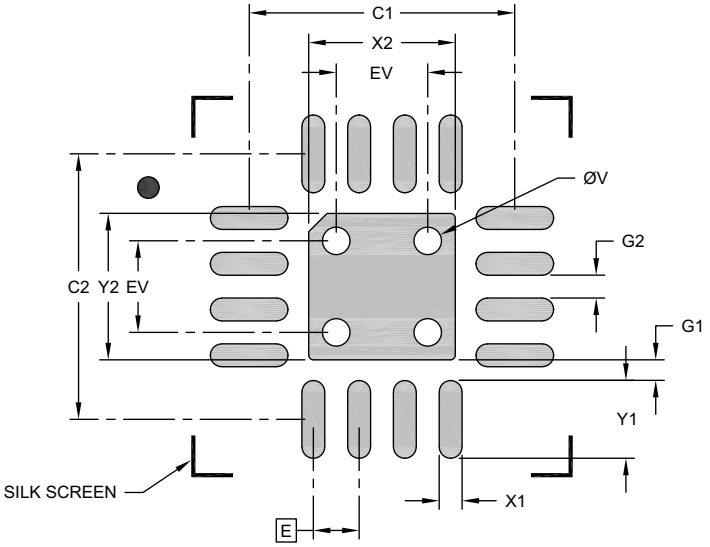

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (Xnn)	X1			0.25
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3103-NCA Rev B

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APPENDIX A: REVISION HISTORY

Revision A (February 2022)

- Converted Micrel document SY88403BL to Microchip data sheet DS20006650A.
- The MSOP package was removed as part of a recent update that happened prior to the document conversion.
- Minor text changes throughout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	X	X	-XX
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY88403B:	3.2 Gbps CML Limiting Post Amplifier with Wide Loss-of-Signal Detection Range
Supply Voltage:	L =	3.3V
Package:	M =	16-Lead 3 mm x 3 mm VQFN
Temperature Range:	G =	–40°C to +85°C
Media Type:	(blank)=	100/Tube
	TR =	1,000/Reel

Examples:

a) SY88403BLMG: SY88403B, 3.3V Supply Voltage, 16-Lead 3x3 VQFN, –40°C to +85°C Temp. Range, 100/Tube

b) SY88403BLMG-TR: SY88403B, 3.3V Supply Voltage, 16-Lead 3x3 VQFN, –40°C to +85°C Temp. Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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