OS81110 cPHY Evaluation Board User's Guide

AIS14001 V1.0.0

Supporting **MOST**® Networks

Media Oriented Systems Transport

MAY 2014

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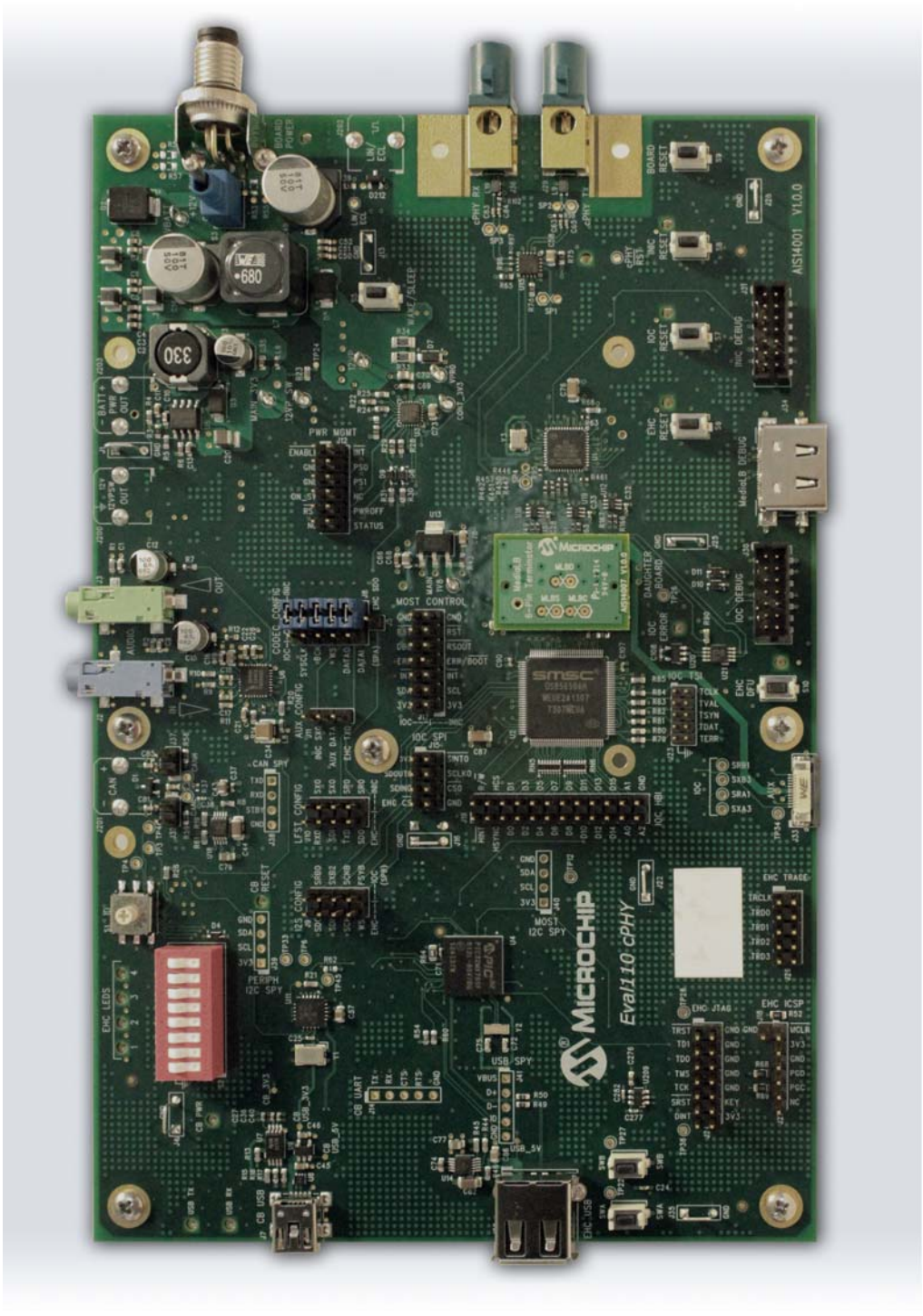
Conventions

The following abbreviations and symbols are used to improve readability.

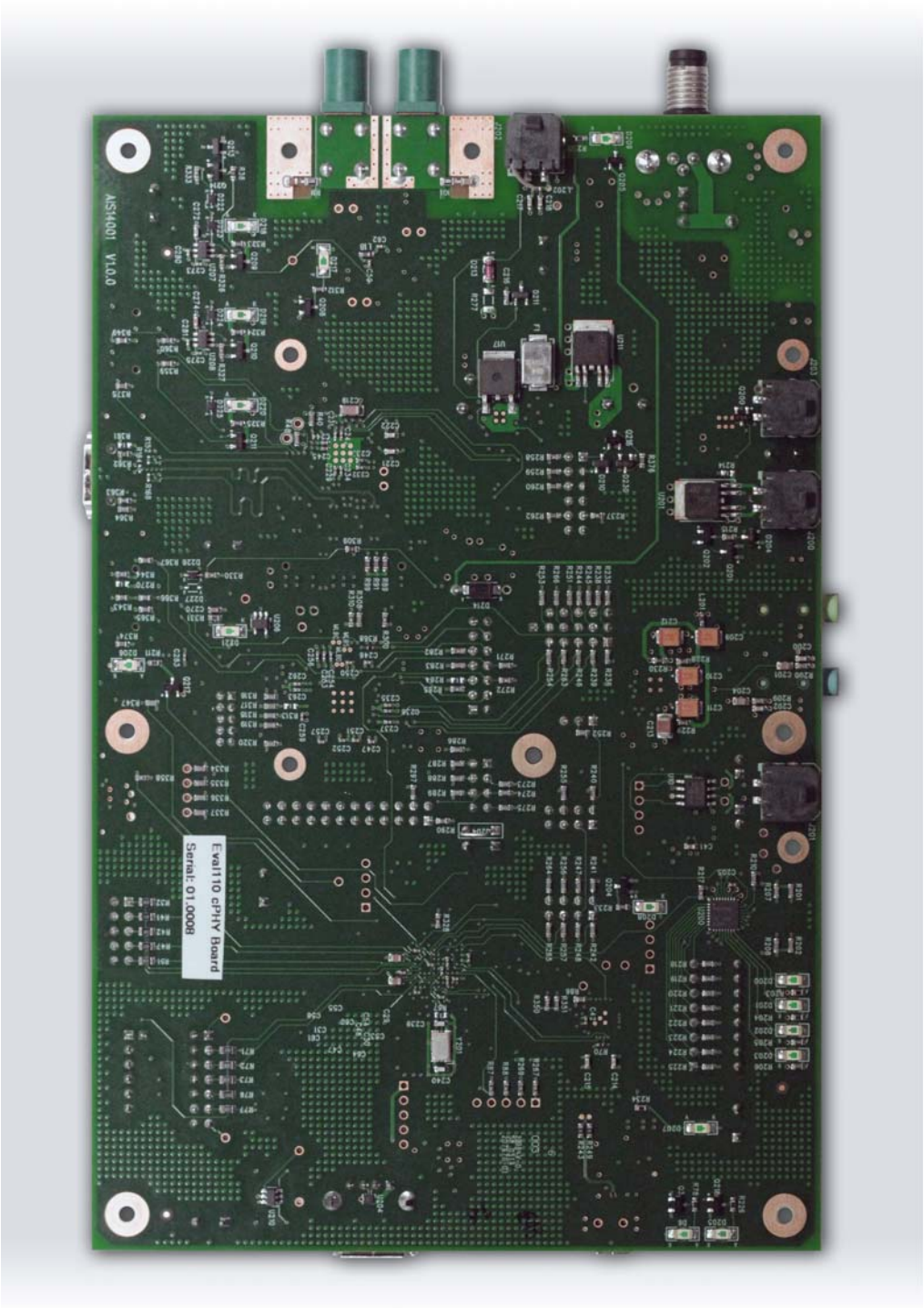
Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
SIGNAL	Signal Name
msb, lsb	Most significant bit, least significant bit
MSB, LSB	Most significant byte, least significant byte
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
code	Instruction code, or API function or parameter
Multi Word Name	Used for multiple words that are considered a single unit, such as: *Resource Allocate* message, or *Connection Label*, or *Decrement Stack Pointer* instruction.
Section Name	Emphasis, Reference, Section or Document name.
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

AIS14001 V1.0.0 FRONT PHOTO



The OS81110 cPHY Evaluation Board User's Guide contains schematics, assembly drawings, and layout plots corresponding to Evaluation Board AIS14001 V1.0.0. This board uses a Microchip OS81110 INIC (Intelligent Network Interface Controller) specifically for MOST150 protocol applications, including MOST ToGo Applications. Please note, the name "Eval110 cPHY Board" "Eval110," Eval110 MOST ToGo" and "Eval110-MTG" are also used within reference drawings and on the board itself. These alternative names all refer to the AIS14001 V1.0.0 hardware.

AIS14001 V1.0.0 BACK PHOTO



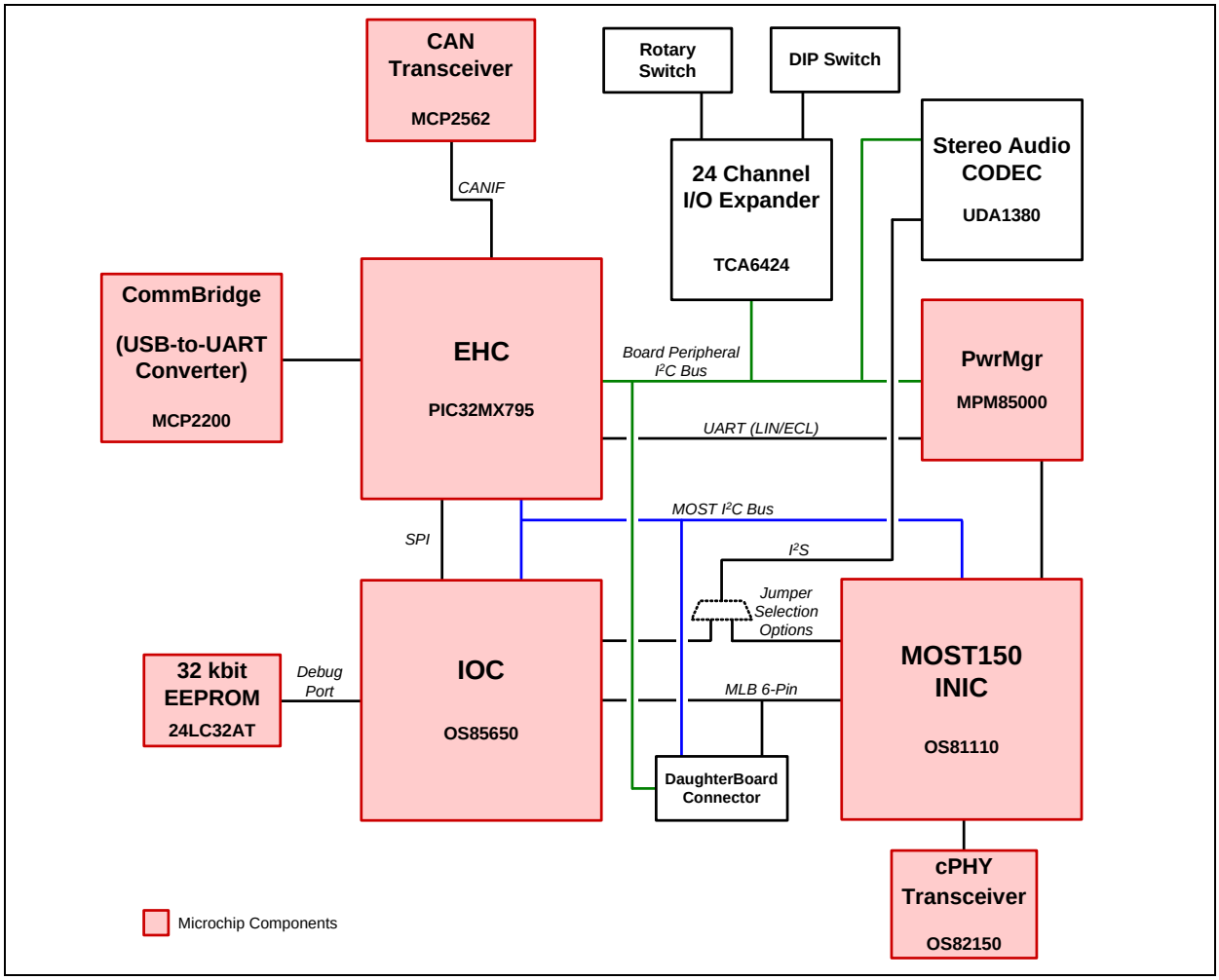
1.0 OVERVIEW

Microchip's OS81110 cPHY Evaluation Board, also referenced within this document as the "Eval110 cPHY Board" (AIS14001 V1.0.0) is a complete MOST150 Network device, utilizing the OS81110 *Intelligent Network Interface Controller* (INIC) device [1] and the OS82150 *MOST150 Coaxial Transceiver* device [2]. An on-board PIC32MX795 *External Host Controller* (EHC) [3] is available for development of custom application code or use of application code provided by Microchip. An integrated OS85650 *I/O Companion Chip* (IOC) [4] provides I/O port expansion for additional application flexibility. The Eval110 cPHY Board also supports power management, controlled by the MPM85000 *Automotive Power Management Device* (PwrMgr) [5], a MOST Network-compliant power management device.

The INIC Streaming Port, in conjunction with an on-board ADC and DAC, supports 2 channel (e.g. stereo) audio exchange on the network. The stereo audio CODEC device is capable of driving headphones at the audio output jack with stereo audio data it sinks from the network. Additionally, a line-level input jack connected to the CODEC supports sourcing stereo audio data to the network.

An overview of the Eval110 cPHY Board hardware is shown in Figure 1-1.

FIGURE 1-1: HARDWARE BLOCK DIAGRAM



Used in conjunction with other Microchip hardware, software, and tools, the Eval110 cPHY Board provides a platform for comprehensive understanding of a complete MOST150 Network device. While the Eval110 cPHY Board was developed for the MOST ToGo network demo system, it is also a useful as a stand alone evaluation board and reference design with both schematics and layouts for customer boards. The platform is also useful for software programmers writing custom EHC applications, as well as users who simply want to work with the standard EHC application code available for the board. Refer to the MOST ToGo Architecture and Implementation Guide [6] for information on standard EHC applications. Contact Microchip for information on available application code loads for the Eval110 cPHY Board.

1.1 Board Features

Primary hardware features of the Eval110 cPHY Board include:

- Integrated *Intelligent Network Interface Controller* (INIC)
- Integrated *MOST150 Coaxial Transceiver* for Coaxial Physical Layer (cPHY) interface to a MOST150 Network
- Integrated *I/O Companion Chip* (IOC), including DTCP coprocessor
- Integrated *External Host Controller* (EHC), supporting:
  - Dual-wire CAN interface in conjunction with on-board MCP2562 [24] CAN transceiver
  - USB host functionality with connection to external device(s) using standard Type A receptacle
  - UART connection to on-board MCP2200 [29] CommBridge (for USB debug print terminal output on PC)
- Feature set expansion via Daughter Board and Auxiliary connectors supporting additional application options (e.g. video sourcing/sinking and low frequency signal tunneling)
- Stereo audio capabilities (via INIC or IOC Streaming Port), supporting:
  - sourcing stereo audio to the network from an on-board line-level input jack, and
  - sinking stereo audio from the network and driving an on-board headphone jack
- MOST Network-compliant power management capabilities, including:
  - Network activity detection
  - Control of switched application power regulators (3.3 V and 1.8 V supplies)
  - Continuous 3.3 V power supply
  - EHC Reset generator based on 3.3 V switched power
  - INIC and IOC reset generator, powered by 3.3V switched power, conditional on 1.8V switched power
  - Support for *Sleep Power State* with very low quiescent current
  - INIC power management, including voltage level reporting per levels defined in the MOST Specification 3.0 [7]
  - Support for wakeup signaling and MOST System Test via MOST Electrical Control Line [8]
  - Serial interface for configuration and status information

1.2 Typical Applications

The INIC device contains the *INIC Software Stack* which manages the network with minimal interaction with the EHC. This allows network nodes to start up without having to wait for the EHC to power-up/initialize. Application functionality in MOST Network devices is implemented with Function Blocks (FBlocks). In addition to application FBlocks that may be supported by EHC application code, FBlock `INIC` (contained within the INIC itself) is used for configuring and controlling INIC. A complete FBlock `INIC` reference guide is available in the OS81110 MOST150 INIC API User's Manual [9].

The MOST ToGo boards are meant to serve as a platform to create a variety of example applications and support many different network configurations and demos. Therefore, application code for the on-board EHC may use only a subset of the available hardware devices and interfaces for communication. In general there are two main types of EHC application code for the Eval110 cPHY Board:

- A *Standard Application* uses simple I^2C communication between the INIC and the EHC to implement a basic network node. The application may also manage the on-board ADC and DAC (connected to the INIC Streaming Port) for sourcing/sinking stereo audio to/from the network. The on-board IOC is not used. These applications are good learning examples, and are suitable for simple synchronous sources and sinks.
- An *Expanded Application* includes use of the IOC and other EHC peripherals. The IOC can be utilized such that it is between the EHC and the INIC to take advantage of its high speed interfaces such as SPI. These applications offer the possibility of much higher asynchronous (packet data) bandwidth, with the added complexity of having to configure the IOC. The application may also include further functionality provided by external devices attached to the *DAUGHTERBOARD* connector (J21) or the *AUX* connector (J33).

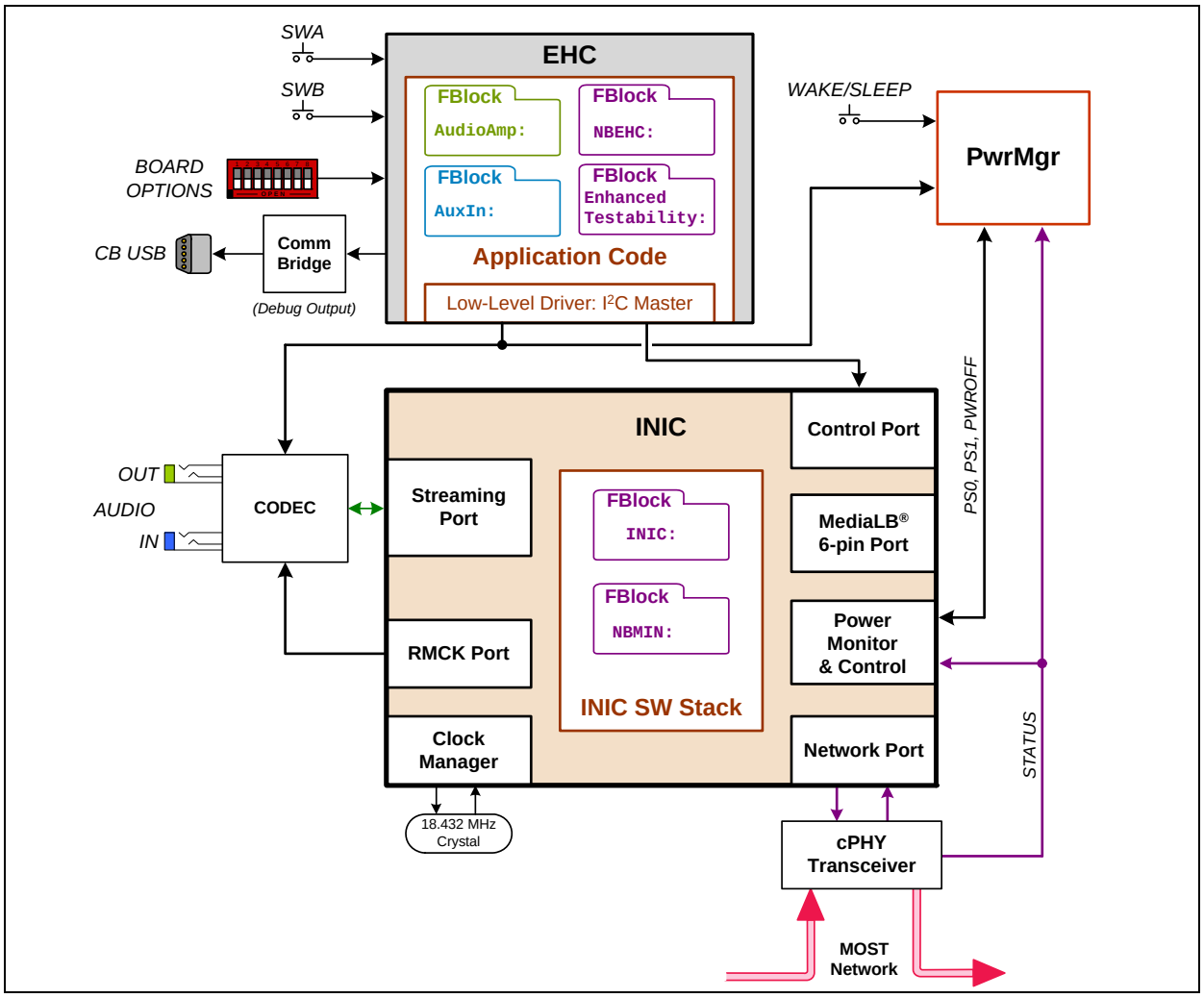
EHC application code for the Eval110 cPHY Board (including custom code) should provide a *Stand-Alone* mode option (typically implemented using the on-board DIP switch). When enabled, this mode should allow INIC to function completely independent of the EHC, with all INIC-EHC interaction disabled. This mode illustrates network interaction, independent of the application, where INIC powers up, enters the network, and autonomously manages the low-level network management functions.

1.2.1 STANDARD APPLICATION

In an Eval110 cPHY Board *Standard Application*, the EHC communicates with INIC (and other board peripherals) via the I^2C bus(es). Power management capabilities are available, and the INIC Streaming Port can be used for stereo audio exchange between the network and the *AUDIO IN* (J2) and *AUDIO OUT* (J3) jacks. The EHC may support FBlocks `AuxIn` and `AudioAmp` for managing the streaming audio exchange remotely. In an Eval110 cPHY Board *Standard Application*, the IOC is not used.

Figure 1-2 shows the Eval110 cPHY Board hardware components typically used by a *Standard Application*.

FIGURE 1-2: STANDARD APPLICATION DIAGRAM



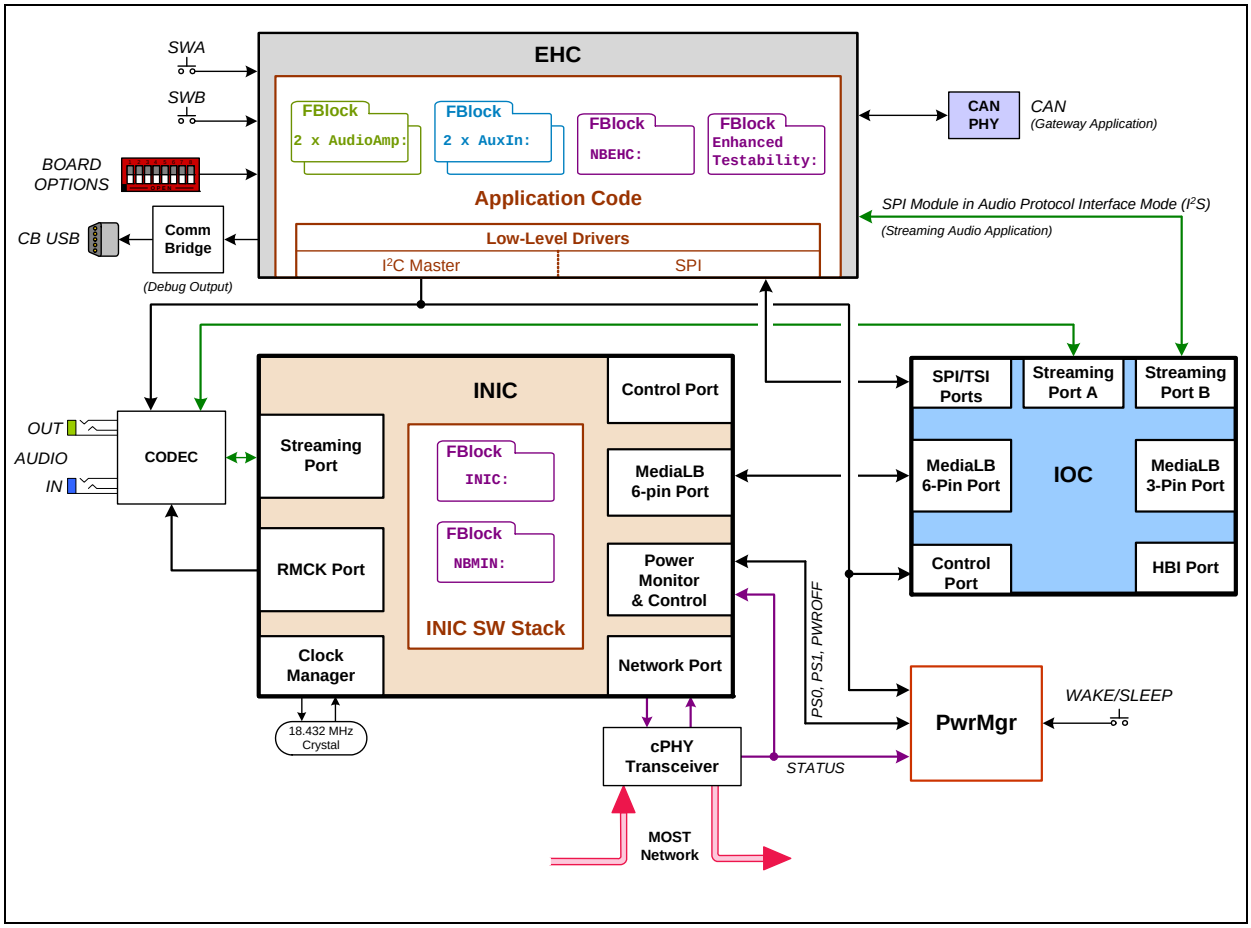
Contact Microchip for information on availability of *Standard Application* source code for the Eval110 cPHY Board.

1.2.2 EXPANDED APPLICATION

In an Eval110 cPHY Board *Expanded Application*, the functionality of a *Standard Application* is extended to include the IOC and other EHC interfaces and peripherals. An *Expanded Application* may also utilize the INIC-IOC communication via the *Media Local Bus* (MediaLB®) 6-pin interface. In this case, the IOC acts a bridge between the INIC and EHC for exchanging control and packet data types. The IOC Streaming Port A can be used for expanded streaming audio exchange between the network and the CODEC while IOC Streaming Port B is available for use with the EHC's SPI module operating in the *Audio Protocol Interface Mode*. The application may also include further functionality provided by external devices attached to the daughterboard connector (J21) or the auxiliary connector (J33).

Figure 1-3 shows the Eval110 cPHY Board hardware components typically used by an *Expanded Application*.

FIGURE 1-3: EXPANDED APPLICATION DIAGRAM



Contact Microchip for information on availability of *Expanded Application* source code for the Eval110 cPHY Board.

2.0 CONFIGURATION AND STATUS

2.1 LEDs

A number of LEDs are used on the Eval110 cPHY Board to convey board and application status information to the user. The following LEDs have dedicated functionality controlled by on-board hardware:

- The *BOARD POWER* red LED (D209) indicates that the INIC, IOC and EHC are powered up. The LED is lit when both the *MAIN_3V3* and *MAIN_1V8* supplies are on.
- The *CB PWR* red LED (D207) indicates that the CommBridge is powered up. The LED is lit when both the *CB_3V3* and *CB_1V8* supplies are on.
- The *LOCK* green LED (D217) is controlled by the INIC **ERR/$\overline{\text{BOOT}}$** pin. The LED is lit when the network is locked.
- The *IOC ERROR* orange LED (D221) is controlled by the IOC **ERROR** pin. An inverter is used so that this LED is lit whenever the IOC PLL is unlocked (i.e. error condition).
- The *INIC RESET* yellow LED (D218) is lit whenever the ***INIC_$\overline{\text{RST}}$*** signal is asserted (Section 4.1).
- The *IOC RESET* yellow LED (D219) is lit whenever the ***IOC_$\overline{\text{RST}}$*** signal is asserted (Section 4.3).
- The *EHC RESET* yellow LED (D220) is lit whenever the ***EHC_$\overline{\text{RST}}$*** signal is asserted (Section 4.4).
- The *EHC DFU* orange LED (D206) is lit whenever the ***EHC_DFU*** signal is asserted. Typically, this signal is only used when the EHC bootloader is active (i.e. during a firmware update).
- The *USB TX* yellow LED (D205) and *USB RX* green LED (D6) blink to indicate message exchange between the Comm Bridge and the EHC.

The remaining LEDs are general purpose LEDs available to the EHC application code, where:

- The green LED (D203) is active-low and available at I/O expander (U200) channel P14 (***$\overline{\text{LED1}}$***).
- The yellow LED (D202) is active-low and available on I/O expander (U200) channel P15 (***$\overline{\text{LED2}}$***).
- The orange LED (D201) is active-low and available on I/O expander (U200) channel P16 (***$\overline{\text{LED3}}$***).
- The red LED (D200) is active-low and available on I/O expander (U200) channel P17 (***$\overline{\text{LED4}}$***).

2.2 Switches

The Eval110 cPHY Board provides an 8-position DIP switch (*BOARD OPTIONS*, S2) for EHC configuration options. The exact functionality depends on the application code; however, DIP switch settings are typically latched at startup and used as run-time configuration settings. Examples of run-time options include enabling/disabling debug print output and enabling/disabling *Stand-Alone* mode.

> **Note:** DIP switch 6 is also used by hardware to override power management shut-down capabilities. Refer to Section 11.4 for more information.

The DIP switch itself is connected to the I/O expander (U200); therefore, the EHC uses the I^2C *Board Peripheral Bus* to determine the values. See Section 9.4.1 for more information about the EHC's I^2C buses. The DIP switch connections to the I/O expander are as follows:

- DIP switch 1 connects to U200 channel P00
- DIP switch 2 connects to U200 channel P01
- DIP switch 3 connects to U200 channel P02
- DIP switch 4 connects to U200 channel P03
- DIP switch 5 connects to U200 channel P04
- DIP switch 6 connects to U200 channel P05
- DIP switch 7 connects to U200 channel P06
- DIP switch 8 connects to U200 channel P07

The Eval110 cPHY Board also supports a 16-position rotary switch (*ID*, S1) which allows the user to set unique identifiers on up to 16 different MOST ToGo boards. EHC application code can set various application values/fields appropriately, based on the switch setting. One such example is setting the board's unique *ECL Node Class*, for use during the MOST System Test. Refer to the MOST Electrical Control Line Specification [8] for more information.

The Eval110 cPHY Board also supports two general-purpose push-button switches (SWA and SWB) connected to the EHC at RD8 and RE6, respectively. These switches are debounced by a specialized debounce device (U210) that uses a 40 ms qualification timer. The debounced outputs are push-pull outputs and do not require pull-up resistors.

3.0 POWER DISTRIBUTION

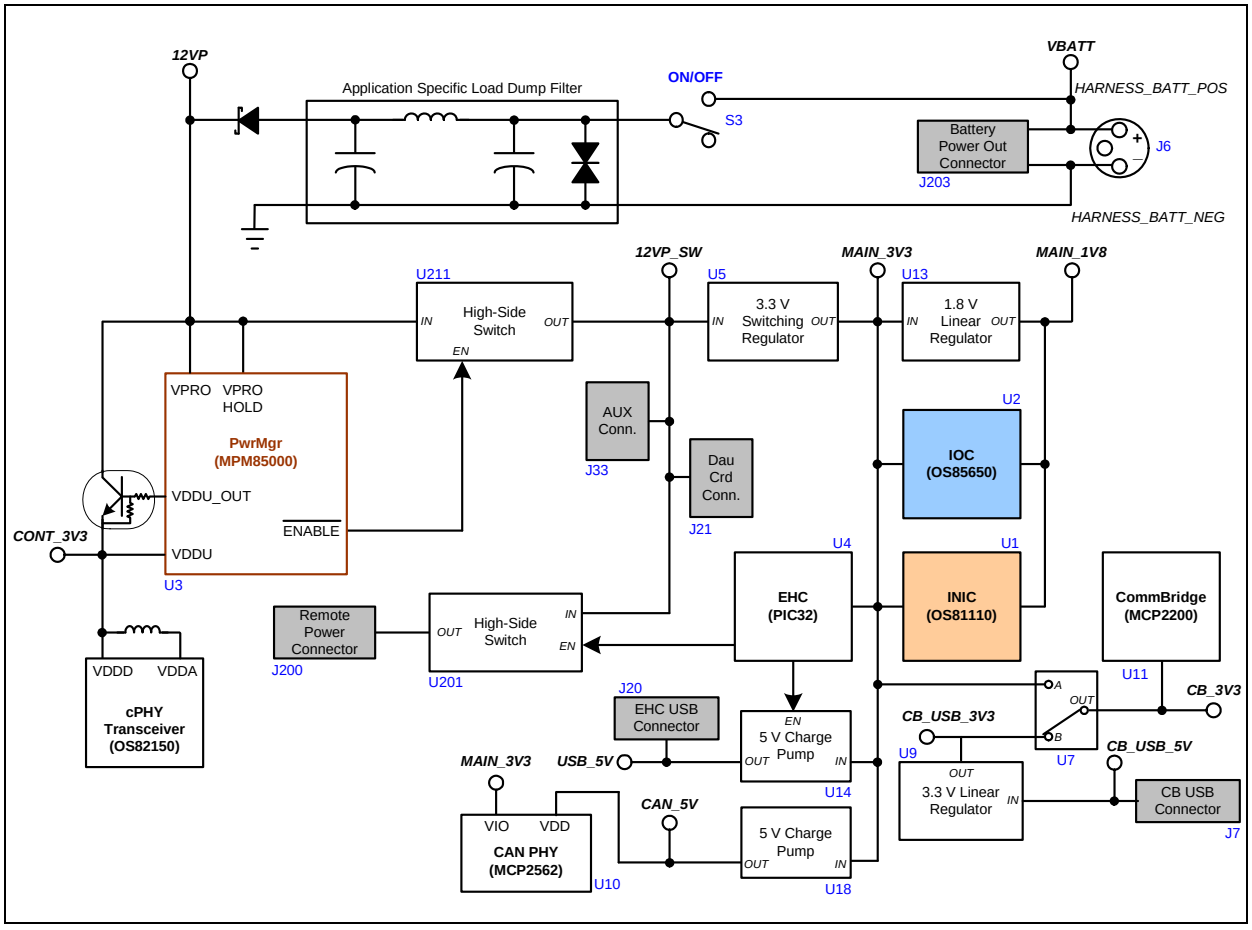
The Eval110 cPHY Board provides a single jack for supplying power to the module. The *BOARD POWER* jack (J6) supports a typical 12 V input using a Binder 99 3403 282 03 (or equivalent) connector. Once filtered, power from the power jack supplies the PwrMgr (U3). This power management device provides a continuous 3.3 V supply (*CONT_3V3*) for the cPHY transceiver (U15) and controls 12 V switched power (*12VP_SW*) that supplies the on-board 3.3 V and 1.8 V regulators (*MAIN_3V3* and *MAIN_1V8*, respectively). 12 V switched and protected power is also available at several headers for off-board use (J21, J200 and J33). To source the necessary current for the cPHY transceiver, an external NPN pass transistor is used at the PwrMgr. The PwrMgr also supports a *Sleep Power State*, where the board is mostly powered off (e.g. all switched supplies disabled). When the switched supplies are active, all board circuitry is powered.

A 2-position micro-fit Molex 43650-0209 connector (J203) provides external devices with direct access to unprotected and unswitched battery power from the cable harness. A second 2-position Molex connector (J200) and a firmware controlled switch (U201) allow the EHC to provide a connected load with protected and switched 12 V power.

The Eval110 cPHY Board includes a 5 V charge pump device (U14) to supply bus power for the USB type A receptacle (J20). This regulator is controlled by the EHC ***USB_VBUS_EN*** signal. The charge pump sources up to 125 mA for connected devices. A second 5 V charge pump powers the CAN transceiver. This charge pump is always enabled; therefore, the CAN CAN transceiver is powered whenever switched 3.3 V power (*MAIN_3V3*) is present.

Figure 3-1 shows an overview of the Eval110 cPHY Board power distribution scheme.

FIGURE 3-1: POWER DISTRIBUTION



For proper operation, the main board power switch (S3) must be *ON* and the main board power supply (e.g. through the *BOARD POWER* connector) must be above the minimum *Power On Voltage*, as defined in Appendix A: "Operating Conditions" on page 50. The power switch is not part of the power management architecture and should remain in the *ON* position for normal operation. When in the *Sleep Power State*, the power switch should not be used to power cycle the Eval110 cPHY Board, as the load-dump capacitors can maintain voltage for hundreds of seconds when the switch is in the *OFF* position.

Note:	Although the board contains typical load-dump circuitry, it is not guaranteed to pass any particular OEM specifications. For production systems, the load-dump circuitry should be designed to meet the required OEM specifications while ensuring that the PwrMgr and associated circuitry remain within their respective specifications at all times.

The Eval110 cPHY Board implements an automatic power switch (U7) to control the CommBridge power source. If the board is connected to a PC with a USB cable via J7, the CommBridge always runs from the external USB power (even when the board is in the *Sleep Power State*). If the external supply is removed, the CommBridge automatically switches over to the *MAIN_3V3* supply. Refer to Chapter 12.0 for more information on CommBridge functionality.

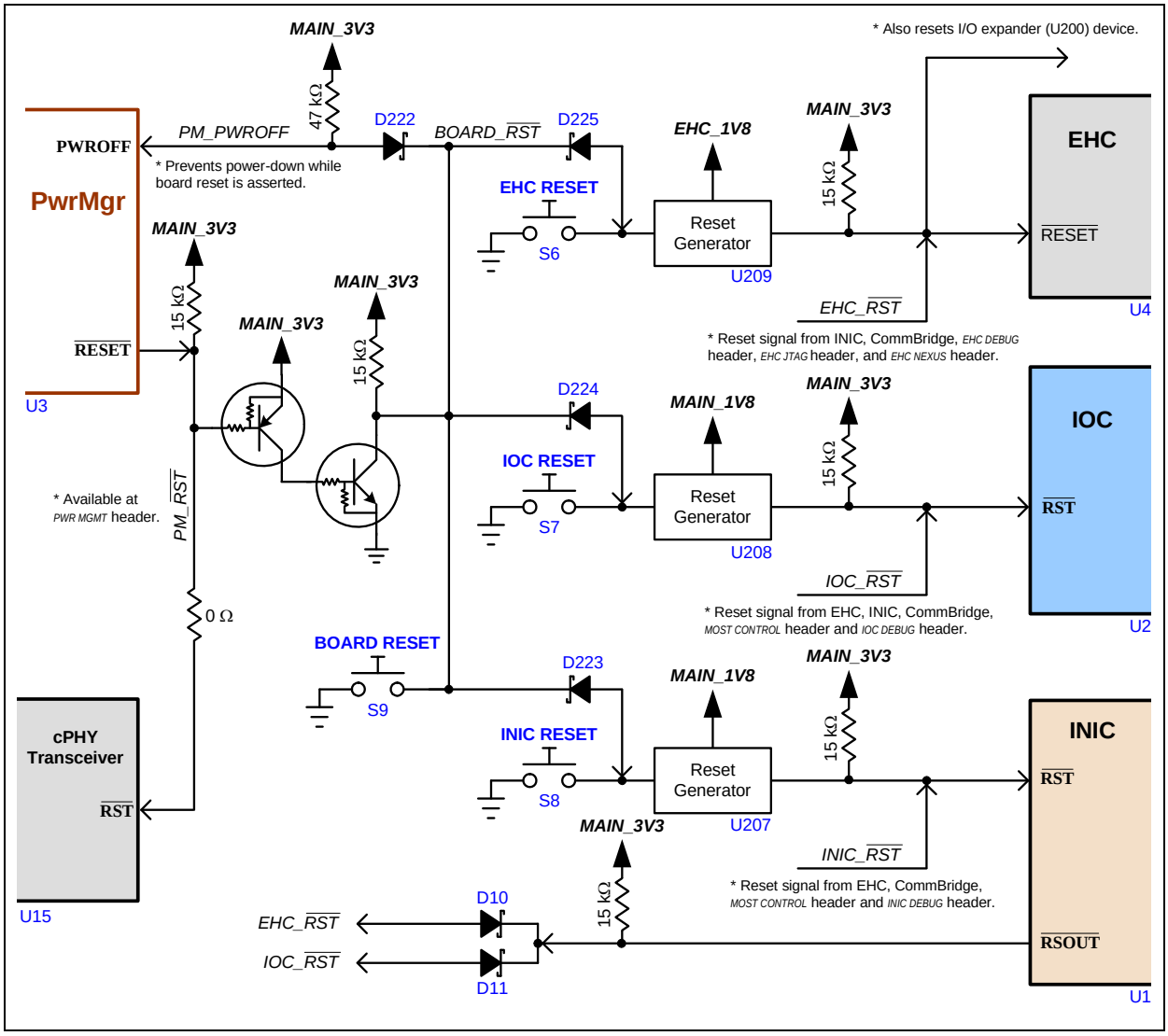
4.0 RESET ARCHITECTURE

The Eval110 cPHY Board provides the flexibility to reset the main devices on the board either simultaneously (via the *BOARD RESET* switch S9) or separately (via independent reset switches). The PwrMgr provides a system-wide POR signal and monitors the *MAIN 3V3* supply. Individual voltage supervisor devices monitor the secondary core supply for each main IC while simultaneously debouncing reset input signals from the hardware switches. Additionally:

- INIC and the IOC can be reset independently by the EHC,
- INIC and the IOC can be reset independently by the CommBridge,
- the IOC and EHC can be reset by INIC (via the $\overline{\text{RSOUT}}$ pin), and
- header access allows each reset signal to be controlled independently.

Figure 4-1 shows an overview of the Eval110 cPHY Board reset implementation.

FIGURE 4-1: BOARD RESET ARCHITECTURE



Note: The robust reset architecture shown above is provided on the Eval110 cPHY Board for flexibility in software development and is not required for production applications. Refer to the MOST INIC Hardware Concepts Technical Bulletin [10] for more information on typical ECU reset architectures.

4.1 INIC Reset

INIC on the Eval110 cPHY Board can be reset by:

- the PwrMgr internal reset generator (**$\overline{\text{RESET}}$** output pin) that monitors the 3.3 V supply (*MAIN_3V3*) for predefined under-voltage conditions,
- the on-board reset generator (U207) when the 1.8 V supply (*MAIN_1V8*) crosses a predefined threshold,
- the application (via EHC ***INIC_$\overline{\text{RST}}$*** signal ***RA9***),
- pressing the *INIC RESET* switch (S8),
- pressing the *BOARD RESET* switch (S9) when D223 is installed (default), or
- external devices connected to the *INIC DEBUG* or *MOST CONTROL* headers J31 and J17, respectively).

A yellow LED (D218) is lit whenever the ***INIC_$\overline{\text{RST}}$*** signal is driven low (active).

The Eval110 cPHY Board supports the use of INIC's application reset output. The INIC **$\overline{\text{RSOUT}}$** pin is connected to the reset input of the IOC and EHC. INIC drives **$\overline{\text{RSOUT}}$** low (and resets the IOC and EHC) when:

- the `INIC.Reset()` function is received from the network with the `EHC` parameter set (requires the `INIC.RemoteAccess()` function to be enabled), or
- a Watchdog timeout occurs while the `Mode` parameter of the `INIC.WatchdogMode()` function is set to `Reset`.

4.2 cPHY Transceiver Reset

The cPHY transceiver on the Eval110 cPHY Board can be reset by:

- the PwrMgr internal reset generator (**$\overline{\text{RESET}}$** output pin) that monitors the 3.3 V supply (*MAIN_3V3*) for predefined under-voltage conditions, or
- an external device connected to the *cPHY $\overline{\text{RST}}$* testpoint (TP47).

> **Note:** By design, the cPHY transceiver reset signal is isolated from all other device resets. To ensure MOST Network compliance, the cPHY transceiver should not be reset during an application reset condition at the INIC, IOC or EHC.

4.3 IOC Reset

The IOC on the Eval110 cPHY Board can be reset by:

- the PwrMgr internal reset generator (**$\overline{\text{RESET}}$** output pin) that monitors the 3.3 V supply (*MAIN_3V3*) for predefined under-voltage conditions,
- the on-board reset generator (U208) when the 1.8 V supply (*MAIN_1V8*) crosses a predefined threshold,
- INIC **$\overline{\text{RSOUT}}$** pin (as described in Section 4.1) when D11 is installed (default),
- the application (via EHC ***RB10***),
- pressing the *IOC RESET* switch (S7),
- pressing the *BOARD RESET* switch (S9) when D224 is installed (default), or
- external devices connected to the *IOC DEBUG* or *MOST CONTROL* headers (J30 and J17, respectively).

A yellow LED (D219) is lit whenever the ***IOC_$\overline{\text{RST}}$*** signal is driven low (active).

4.4 EHC Reset

The EHC can be reset on the Eval110 cPHY Board by:

- the INIC **$\overline{\text{RSOUT}}$** pin (as described in Section 4.1) when D10 is installed (default),
- pressing the *EHC RESET* switch ($S6_{1F}$),
- pressing the *BOARD RESET* switch (S9) when D225 is installed (default), or
- an external device (or jumper shunt) on any of the following headers:
  - *EHC ICSP* Programming/Debug header, J27
  - *EHC JTAG* header, J24
  - *CommBridge* GP0 signal

A yellow LED (D220) is lit whenever the EHC reset signal is driven low (active). The EHC reset signal (***EHC_$\overline{\text{RST}}$***) also issues reset conditions to on-board EHC peripheral devices such as the I/O expander (U200).

5.0 DAUGHTER BOARD AND AUXILIARY CONNECTORS

The Eval110 cPHY Board supports feature set expansion using off-board hardware by offering two connector options for interfacing to other PCBs and/or external devices. The first option is the 40-pin *DAUGHTERBOARD* connector (J21). The second option is the 12-pin *AUX* connector (J33). Refer to Section 5.3 for possible application examples utilizing these connectors.

5.1 Daughter Board Connector

The *DAUGHTERBOARD* connector is a high-speed, 44-pin, Samtec socket header (part number QSH-020-01-L-D-DP-A) that is designed to be mated with the Samtec QTH series of terminal headers. In order to provide clearance to all on-board components and headers, external PCBs connecting to J21 should utilize a QTH connector specifying a mated height of at least 11 mm. The *DAUGHTERBOARD* connector definition is provided in Table 5-1.

TABLE 5-1: DAUGHTER BOARD CONNECTOR DEFINITION

Pin # *	Net Name	Description / Notes
1		Unused signal - connects to TP26.
3	***DC_I/O_$\overline{INT}$***	Daughter Board I/O expander interrupt signal - connects to EHC RD6.
13	***DC_$\overline{ATT}$***	Daughter Board attached signal - connects to I/O expander channel P27 with a weak pull-up resistor. Should be tied directly to ground on the daughterboard PCB.
14	***DC_$\overline{READY}$***	Daughter Board ready signal - connects to EHC RE0. The daughterboard application should drive this signal low to indicate it is ready for access by the host application on the Eval110 cPHY Board.
15	***DC_$\overline{INT}$***	Daughter Board interrupt signal - connects to EHC RD13.
16	***DC_$\overline{RST}$***	Daughter Board reset input - connects to EHC RE3 through a 0 Ω resistor (R309). This signal can also be influenced by the ***IOC_$\overline{RST}$*** and ***EHC_$\overline{RST}$*** signals through series diode options.
17	***MLBSN***	Negative (differential) component of the MediaLB Signal line - connects to the far end of the MediaLB 6-pin bus after the IOC and INIC.
19	***MLBSP***	Positive (differential) component of the MediaLB Signal line - connects to the far end of the MediaLB 6-pin bus after the IOC and INIC.
21	***MLBDN***	Negative (differential) component of the MediaLB Data line - connects to the far end of the MediaLB 6-pin bus after the IOC and INIC.
23	***MLBDP***	Positive (differential) component of the MediaLB Data line - connects to the far end of the MediaLB 6-pin bus after the IOC and INIC.
25	***MLBCN***	Negative (differential) component of the MediaLB Clock line - connects to the far end of the MediaLB 6-pin bus after the IOC and INIC.
27	***MLBCP***	Positive (differential) component of the MediaLB Clock line - connects to the far end of the MediaLB 6-pin bus after the IOC and INIC.
29	***MOST_SCL***	I^2C Clock line - connects to the *MOST Control Bus* I^2C bus
30	***PERIPH_SCL***	I^2C Clock line - connects to the *Board Peripheral Bus* I^2C bus
31	***MOST_SDA***	I^2C Data line - connects to the *MOST Control Bus* I^2C bus
32	***PERIPH_SDA***	I^2C Data line - connects to the *Board Peripheral Bus* I^2C bus
33	***MAIN_1V8***	Main board 1.8 V switched power supply.
35	***MAIN_1V8***	Main board 1.8 V switched power supply.
37	***MAIN_3V3***	Main board 3.3 V switched power supply.
38	***12VP_SW***	Main board 12 V protected and switched battery power.
39	***MAIN_3V3***	Main board 3.3 V switched power supply.
40	***12VP_SW***	Main board 12 V protected and switched battery power.

* Connector pins omitted from this table are not connected on the Eval110 cPHY Board and are reserved for future use.

TABLE 5-1: DAUGHTER BOARD CONNECTOR DEFINITION (CONTINUED)

Pin # *	Net Name	Description / Notes
41	***GND***	Main board ground.
42	***GND***	Main board ground.
43	***GND***	Main board ground.
44	***GND***	Main board ground.

* Connector pins omitted from this table are not connected on the Eval110 cPHY Board and are reserved for future use.

5.2 Auxiliary Connector

The *AUX* connector J33 is a 12-pin, Wuerth Electronics ZIF WR-FPC connector (part number 68711214522) that is designed to be mated with a flat, flexible ribbon cable. The *AUX* connector definition is provided in Table 5-2.

TABLE 5-2: AUXILIARY CONNECTOR DEFINITION

Pin #	Net Name	Description / Notes
1	***AUX_$\overline{ATT}$***	Auxiliary attached signal - connects to I/O expander channel P23 with a weak pull-up resistor. Should be tied directly to ground on the auxiliary PCB/device.
2	***AUX_SX***	Auxiliary data signal - connects to pin 2 of *AUX CONFIG* header (J11). A shunt can be used on J11 to connect this signal to either the INIC Streaming Port or the EHC I^2S Port. Refer to Section 10.2 for more information.
3		Unused signal - connects to TP34.
4	***GND***	Main board ground.
5	***MAIN_3V3***	Main board 3.3 V switched power supply.
6	***12VP_SW***	Main board 12 V protected and switched battery power.
7	***12VP_SW***	Main board 12 V protected and switched battery power.
8	***MAIN_3V3***	Main board 3.3 V switched power supply.
9	***GND***	Main board ground.
10	***PERIPH_SDA***	I^2C Data line - connects to the *Board Peripheral Bus* I^2C bus
11	***PERIPH_SCL***	I^2C Clock line - connects to the *Board Peripheral Bus* I^2C bus
12	***AUX_$\overline{INT}$***	Auxiliary interrupt signal - connects to EHC RD12.

5.3 Off-Board Applications

The *DAUGHTERBOARD* connector includes signals for both I^2C buses and the MediaLB 6-pin bus signals, thereby permitting a variety of application possibilities when an external PCB is attached. One such example is an external controller that replaces the on-board EHC. When the EHC is placed in *Stand-Alone* mode, an external device is capable of controlling INIC and certain peripheral ICs such as the IOC and PwrMgr.

The *DAUGHTERBOARD* connector can also be used to extend the feature set of the board while still using the on-board EHC. For example, a daughterboard featuring an OS85621 *Video I/O Companion* device [11] or the KLR83012 *Fully-Integrated Wireless Audio/Voice Transceiver* device [12] can be attached to add additional audio and/or video sourcing and sinking capabilities to the application.

The *AUX* connector is intended to support an external device that is managed by the on-board EHC. Possible implementations include I/O feature set expansion such as a remote display board (with a UART interface) or for use in LFST applications, as described in Section 10.2.

5.4 MediaLB 6-Pin Terminator Board

Whenever the Eval110 cPHY Board is operated without an expansion board connected to the *DAUGHTERBOARD* connector, a specialized plug-in board (AIS14007) must be attached to J21 to properly terminate the MediaLB 6-pin interface. Refer to Section 6.7 for more information.

6.0 INTELLIGENT NETWORK INTERFACE CONTROLLER (INIC)

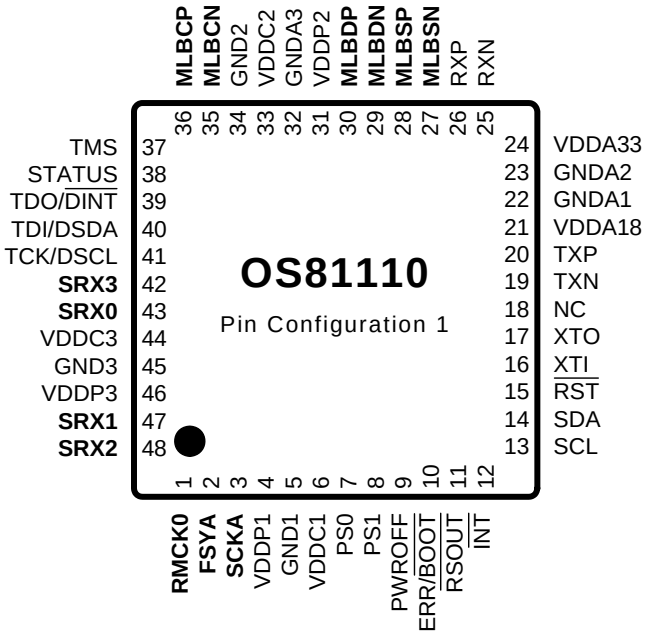
The Eval110 cPHY Board utilizes an OS81110 MOST150 (INIC) device [1] (U1) to communicate over the MOST150 Network. For proper operation with Eval110 cPHY Board hardware, the OS81110 is set for *Pin Configuration 1* (shown in Figure 6-1).

By default, INIC powers up with the I^2C Control Port enabled and is ready for access by an I^2C bus master device (e.g. EHC). Alternatively, R284 can be installed (and R285 removed) to configure INIC for MediaLB access following power-up/reset. Refer to Section 6.7 and Section 9.4.1 for more information on Eval110 cPHY Board MediaLB and I^2C communication interfaces.

When *Stand-Alone* mode is enabled (see Section 9.2), the EHC should disable its communication interfaces, allowing the INIC to be controlled remotely across the network or by an off-board device through the *MOST CONTROL* header (J17) or the *DAUGHTERBOARD* connector (J21).

As required by the OS81110, a 384×Fs (18.432 MHz) external crystal (Y3) is provided on the board, supporting a 48 kHz MOST150 Network frame rate.

FIGURE 6-1: OS81110 INIC



6.1 INIC Configuration String

To support the standard EHC application code available for the Eval110 cPHY Board, the *INIC Configuration String* is pre-programmed by Microchip. The Eval110 cPHY Board is shipped with the following *INIC Configuration String* settings, where settings that differ from the INIC Factory defaults are shown in bold:

- `NBMIN.NodeAddress.NodeAddress = 0xFFFF`
- `NBMIN.GroupAddress.GroupAddress = 0x3C8`
- `NBMIN.RetryParameters.RetryTime = 11`
- `NBMIN.RetryParameters.RetryNumbers = 6`
- `INIC.VersionInfo.ConfString = 0.0.0`
- **`INIC.RMCK.Divider = 256Fs`**
- **`INIC.RemoteAccess.AccessMode = True`**
- `INIC.WatchdogMode.AutoShutDownDelay = 65535 ms`
- `INIC.Bandwidth.AssignBWInit = 80`
- `INIC.DeviceMode.DeviceMode = Slave`
- **`INIC.RBDOptions.Options = 0x0`**
- `INIC.NIStartUpMode.Mode = 0x0`
- **`INIC.PortConfiguration.PortVariantCfg = Configuration 1`**
- **`INIC.PortConfiguration.MediaLBClockCfg = 2048Fs`**
- **`INIC.PortConfiguration.SerialInterfaceCfg = DualInOut`**
- `INIC.PortConfiguration.DefPort = INT_Select`
- `INIC.PortConfiguration.CPCfg.I2CSlaveAddress = 0x40`
- `INIC.AddressConfig.Mode = 0x0`
- `INIC.SCMConfig.SCMCfg = 0x0`
- `INIC.SCMConfig.SCMCfg2 = 0x0`
- **`INIC.PMIConfig.Config = 0x1C`**
- **`INIC.PMIConfig.TimePwrOff = 60 s`**
- `INIC.UseStatusPin = True`
- `INIC.CustomRMCK = 0x0`

The *INIC Configuration String* can be overwritten via the I^2C Control Port (either by the EHC or by an external device through the *MOST CONTROL* header, J17). Updating via the Control Port is described in the INIC Flash Guide Application Note [13]. Additionally, the *INIC Configuration String* can be written through the Debug Port, as described in Section 6.2.

6.2 Flash and Debug

The Eval110 cPHY Board provides the *INIC DEBUG* header (J31) for connecting the *INIC Explorer Interface Tool* [14]. In addition to viewing and writing the *INIC Configuration String*, *INIC Explorer* can be used to update the OS81110 Flash memory (program code) and to view real-time debug information (via PC software). Debugging capabilities include:

- Exploring internal INIC properties and states during normal operation,
- Viewing internal INIC states and routing configurations (sockets and handles) graphically,
- Creating an INIC data memory snapshot as a file dump, and
- Viewing FBlock `INIC` and FBlock `NetBlock` status.

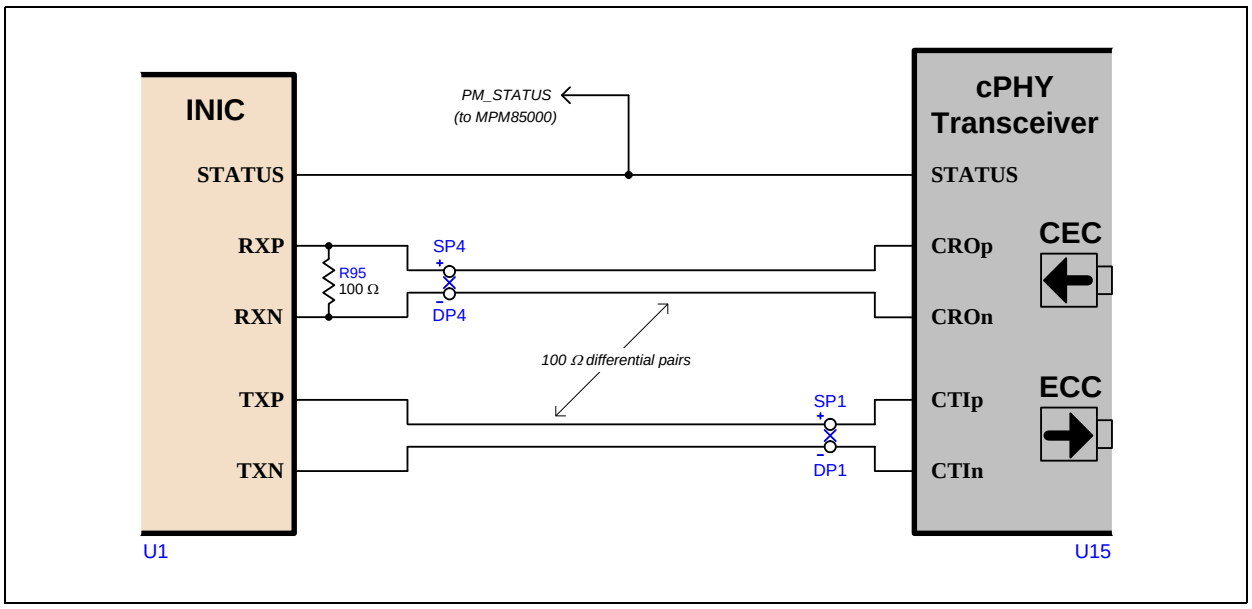
6.3 Network Port

The OS81110 Network Port is connected to a *MOST150 Coaxial Transceiver* (cPHY Transceiver, U15). The transmit and receive lines between INIC and the cPHY transceiver are *low-voltage differential signal* (LVDS) pairs, which are implemented on the Eval110 cPHY Board as impedance-controlled (100 Ω) transmission lines.

The cPHY transceiver activity indicator output is connected to the INIC **STATUS** pin and is used by INIC to optimize network startup and shutdown sequences.

Figure 6-2 shows the OS81110 Network Port implementation on the Eval110 cPHY Board.

FIGURE 6-2: INIC NETWORK PORT



For more information on the cPHY Transceiver device, refer to Chapter 7.0.

6.4 Control Port

The INIC Control Port operates as an I^2C bus slave (address 40h/41h) and supports asynchronous packet and control message exchange with the EHC. The INIC hardware interrupt (**INT** pin) is used to notify the external controller that INIC requires service. By default, the ***INIC_INT*** signal (connected to EHC RD7) on the Eval110 cPHY Board is pulled-up (through R285) to automatically enable the Control Port at power-up/reset. Alternatively, a pull-down resistor can be installed at R284 (requires R285 removed) to enable the MediaLB Port at power-up/reset.

Typically, the EHC application code implements an I^2C bus master and uses Port Message Protocol to configure and control the INIC. Refer to Section 9.4.1 for more information on the I^2C communication busses on the Eval110 cPHY Board.

6.5 Power Management Interface

The PwrMgr uses its Power Management interface to convey board power information to INIC. Using **PS0** and **PS1**, four different power states can be conveyed (including over-voltage and under-voltage conditions), as defined in the MOST Specification 3.0 [7]. This specification defines the four general power states; however, the exact voltage levels and thresholds for each state are configurable and typically defined by the OEM's system integrator. INIC recognizes transitions between these power states and responds to the PwrMgr (using **PWROFF**) when it is ready to be powered down. For more information on the configuration and use of the power management interface, refer to the MPM85000 Automotive Power Management Device Data Sheet [5].

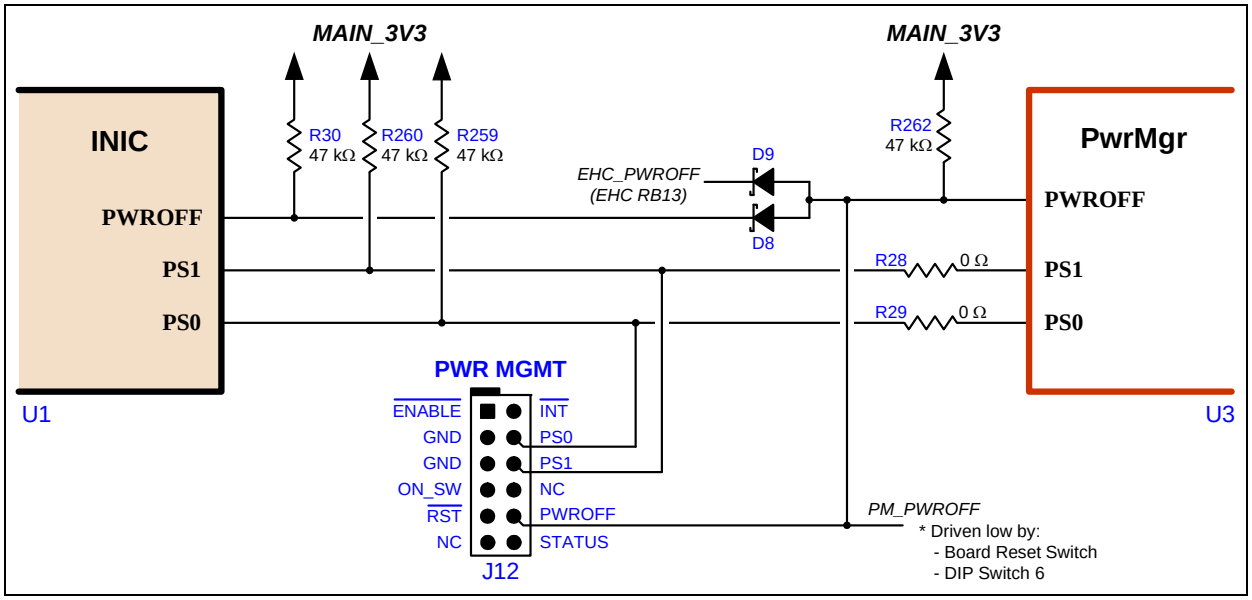
The Eval110 cPHY Board connects the power management interfaces of the PwrMgr and INIC with a hardware option that allows the EHC to hold **PWROFF** low if the application requires additional time before the board enters the *Sleep Power State*. The EHC application code may use the ***EHC_PWROFF*** (***RB13***) signal to override **PWROFF** and prevent board power-down.

DIP switch 6 (S2) provides a hardware override option which disables power management. When the switch is closed, board power-down is prevented by forcing the PwrMgr **PWROFF** pin low via ***PM_PWROFF***.

> **Note:** With default *INIC Configuration String* settings, **PS[1:0]** must *not* be in the U_{Low} state (**PS[1:0]**=11b) in order for INIC to be active on the network.

Figure 6-3 provides an overview of the Eval110 cPHY Board power management interface.

FIGURE 6-3: POWER MANAGEMENT INTERFACE

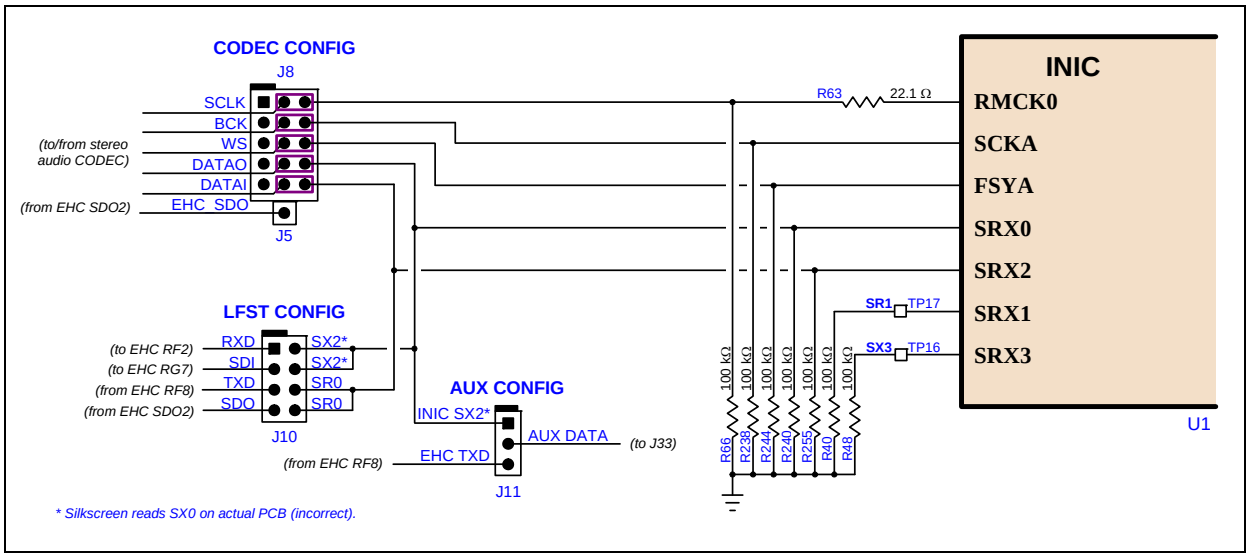


Refer to Chapter 11.0 for more information about power management on the Eval110 cPHY Board.

6.6 INIC Streaming Port

The INIC Streaming Port is used by external devices (e.g. stereo audio CODEC) to source/sink streaming data with low overhead. When the using the OS81110 Streaming Port is configured for `DualInOut` operation, four data pins are available (two inputs and two outputs). However, the Eval110 cPHY Board is designed to only use two of the four data pins: one serial input (**SR0**) and one serial output (**SX2**). These two serial data pins are typically connected (with shunts) to the stereo audio CODEC at *CODEC CONFIG* (J8). Refer to Section 10.1 for more information on the CODEC device. The INIC Streaming Port connection options on the Eval110 cPHY Board are shown in Figure 6-4.

FIGURE 6-4: INIC STREAMING PORT CONNECTION OPTIONS



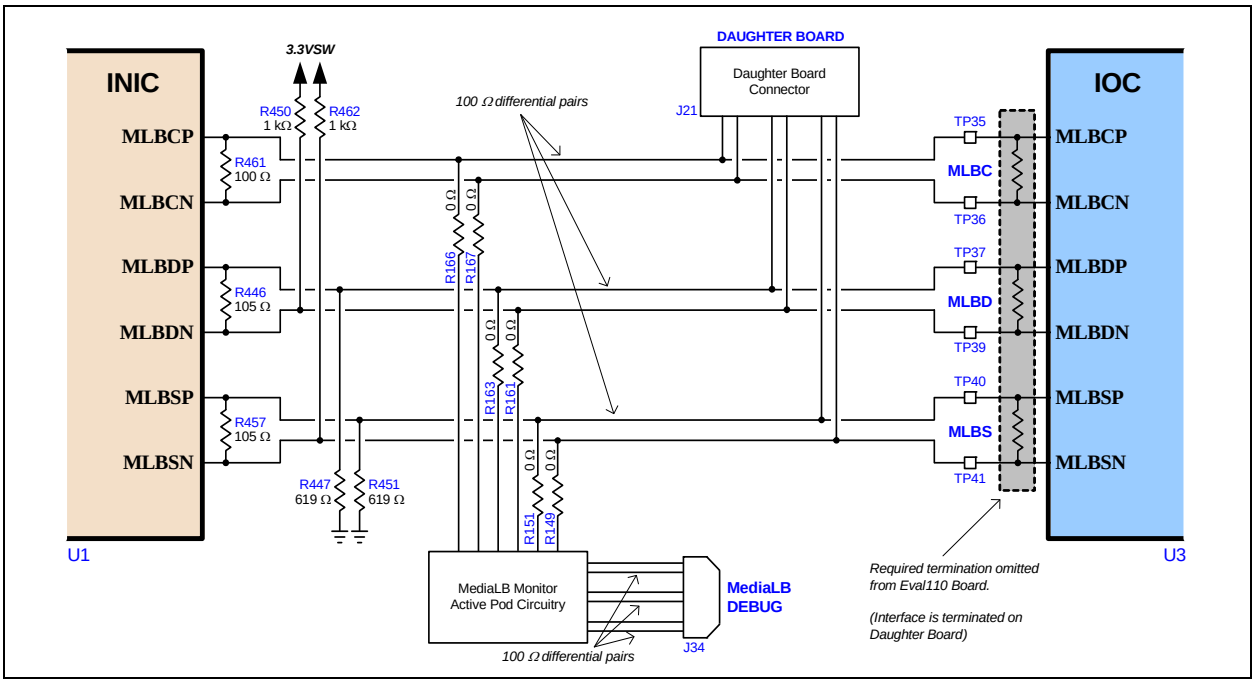
As shown above, INIC Streaming Port signals can also be connected to the EHC through the *LFST CONFIG* (J10) header. Additionally, the INIC serial output pin can be routed to an external device connected to the *AUX* (J33) header by placing a shunt between pins 1 and 2 of *AUX CONFIG* (J11). These alternative connection options can be used to transport low bandwidth digital signals across the MOST150 Network, as described in Section 10.2.

6.7 MediaLB 6-Pin Port

The OS81110 MediaLB 6-Pin Port is used to exchange MOST Network data types with other on-board devices (e.g. EHC or IOC) using the protocol defined in the MediaLB Specification [15]. When communication is enabled, the INIC MediaLB Port functions as the *MediaLB Controller*, providing real-time access to all supported MOST150 data types. The IOC MediaLB Port functions as a *MediaLB Device* and supports routing of MediaLB data to other ports used by the application (e.g. SPI Port, Streaming Port). The MediaLB interface is used in higher performance applications, where the IOC is used to bridge communication between INIC and the EHC and/or the expanded streaming audio capabilities of the IOC are required.

Figure 6-5 illustrates the MediaLB 6-pin interface on the Eval110 cPHY Board.

FIGURE 6-5: MediaLB 6-PIN CONNECTION DIAGRAM



MediaLB 6-pin debugging capabilities are provided on the Eval110 cPHY Board via the *MediaLB DEBUG* connector (J34). Integrated circuitry on the Eval110 cPHY Board (referred to as the *MediaLB Monitor Active Pod Circuitry*) enables real-time analysis and debugging of the MediaLB interface by the MediaLB Monitor tool [16]. Contact Microchip for more information regarding MediaLB analysis and debugging tools.

For more information on the MediaLB physical layer and link layer, refer to the MediaLB Specification [15].

The MediaLB 6-pin interface is also routed to the *DAUGHTER BOARD* (J21) connector. This header allows communication with an off-board MediaLB Device. Possible off-board implementations include daughterboards featuring the *OS85621 Video I/O Companion* device [11] or an FPGA implementation of the OS62420 MediaLB device [17]. Refer to Section 5.3 for more information on supplemental hardware connections (e.g. daughterboards) on the Eval110 cPHY Board.

Note:	As shown in Figure 6-5, the termination resistors at the IOC device are not included on the Eval110 cPHY Board. The OS81110 MediaLB interface is routed to the IOC using a pass-through technique such that the end of the bus is located at the daughterboard connector. All daughterboard designs must include the MediaLB termination resistors. Whenever the Eval110 cPHY Board is operated without an expansion board connected to the *DAUGHTERBOARD* connector, a specialized plug-in board (AIS14007) must be attached to J21 to properly terminate the MediaLB 6-pin interface.

7.0 MOST150 COAXIAL TRANSCEIVER (cPHY)

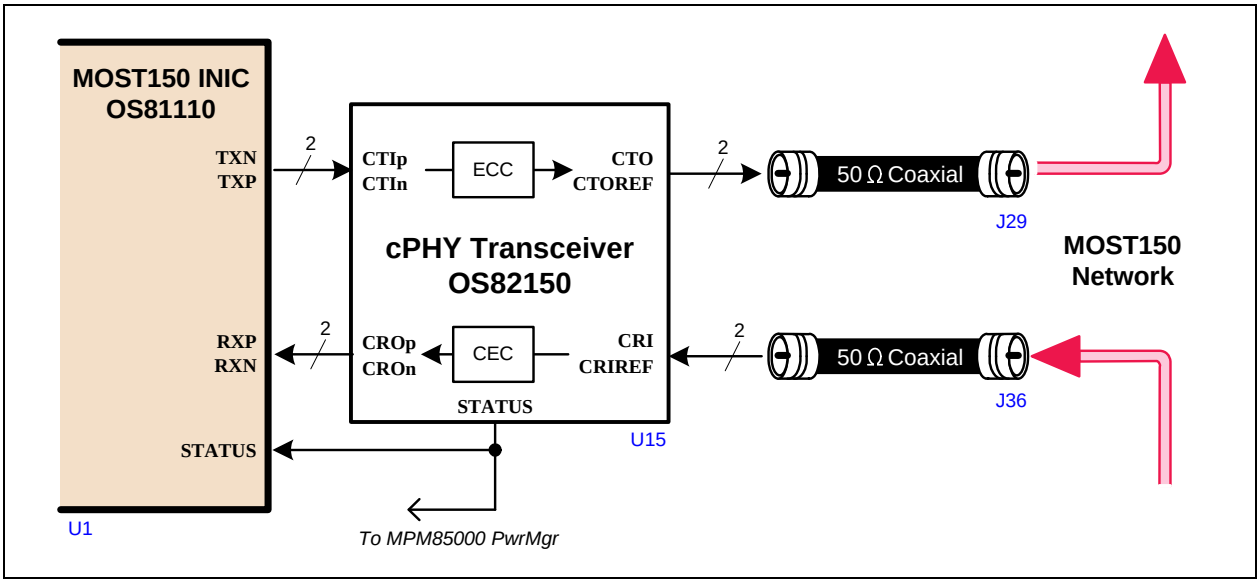
The Eval110 cPHY Board supports connection to a MOST150 network through the *cPHY TX* (J29) and *cPHY RX* (J36) jacks (Rosenberger 59S20X-40ML5-Z) using 50 Ω shielded coaxial cable (RTK031, or equivalent) with FAKRA automotive SMB female plugs (IMS 4100.SMBA.2Z10.039, or equivalent).

The INIC Network Port transmit and receive interfaces utilize low-voltage differential signaling (LVDS). The OS82150 *MOST150 Coaxial Transceiver* (cPHY) device [2] includes both an electrical-to-coax converter (ECC) and a coax-to-electrical converter (CEC) to drive the coax cable and equalize the incoming signal.

The cPHY Transceiver is powered from the 3.3 V continuous supply (*CONT_3V3*) sourced by the PwrMgr and supports a low-power mode of operation (i.e. the *Sleep Power State*). The device also includes an activity detector (**STATUS** output signal, connected to PwrMgr) to support wakeup and interrupt events based on MOST150 network activity detection at SP3. Refer to Section 11.2 "Wakeup and Interrupt Events" for more information.

An overview of the cPHY Transceiver is shown below in Figure 7-1.

FIGURE 7-1: cPHY TRANSCEIVER CONNECTION DIAGRAM



8.0 I/O COMPANION (IOC)

The Eval110 cPHY Board provides an OS85650 I/O Companion (IOC) device [4] (U2) to provide a high-speed link between the EHC peripherals and the MOST Network. The IOC device can route both synchronous (e.g. audio/video) and asynchronous (e.g. packet) data streams. An optional *Digital Transmission Content Protection* (DTCP) coprocessor is also available. When supported by the Eval110 cPHY Board application code, the IOC device is typically used to:

- Exchange data with INIC over the MediaLB 6-pin interface,
- Route between MediaLB 6-pin interface and SPI Port (interface to EHC),
- Route between MediaLB 6-pin interface and Streaming Port (interface to audio CODEC),
- Route between MediaLB 6-pin interface and TSI Port (interface to off-board device),
- Encrypt/Decrypt synchronous and/or isochronous data streams, and
- Support full *Authentication and Key Exchange* (AKE), as defined by the DTCP Specification [18].

8.1 Configuration and Debug

The OS85650 IOC contains two memory spaces used for configuration: *One-Time Programmable* (OTP) memory and RAM-based *Configuration Memory* (Cfg Memory). Neither the OTP memory nor the Cfg memory on the IOC is configured by default. When EHC application code is available that utilizes the IOC, the Microchip IOC Configuration Software [19] should be used to configure OTP and Cfg Memory appropriately for the desired functionality by:

- directly configuring OTP memory using the *INIC Explorer* tool via the *IOC DEBUG* header (J30), or
- generating a list of IOCMs for EHC applications to send to configure OTP memory and/or Cfg Memory.

The Eval110 cPHY Board provides a resistor population option to set the default state of the IOC **DBG** pin. This pin sets the initial mode of operation for the IOC Debug Port. By default, R344 is populated and the IOC Debug Port is set for JTAG mode. Alternatively, R270 can be installed (and R344 removed) to configure the IOC Debug Port for I^2C mode. Refer to the OS85650/2 I/O Companion Data Sheet [4] and the Microchip IOC Configuration Software [19] for more information on using and configuring the IOC.

8.2 Control Port

The IOC Control Port operates as an I^2C bus slave (address 48h/49h) and supports message-based communication with the EHC. The IOC hardware interrupt (**INT** pin) is used to notify the external controller that the IOC requires service. The ***IOC_INT*** signal is connected to EHC RD4 on the Eval110 cPHY Board.

Typically, the EHC application code implements an I^2C bus master and uses Port Message Protocol to configure and control the IOC. Refer to Section 9.4.1 for more information on the I^2C communication busses on the Eval110 cPHY Board.

8.3 MediaLB Ports

The OS85650 IOC device includes two MediaLB Ports, namely a MediaLB 3-pin Port and a MediaLB 6-pin Port. The IOC MediaLB Ports are 3-wire (single-ended) and 6-wire (differential) hardware interfaces used to exchange MOST Network data types with other on-board devices (e.g. INIC or EHC) using the protocol defined in the MediaLB Specification [15].

The Eval110 cPHY Board provides a 6-pin MediaLB interface between INIC and the IOC with the IOC functioning as a *MediaLB Device* that supports routing of MediaLB data to other ports used by the application (e.g. Streaming Port). See Section 6.7 for more information (including a connection diagram) regarding the MediaLB 6-pin implementation on the Eval110 cPHY Board.

The IOC MediaLB 3-pin Port is not used on the Eval110 cPHY Board.

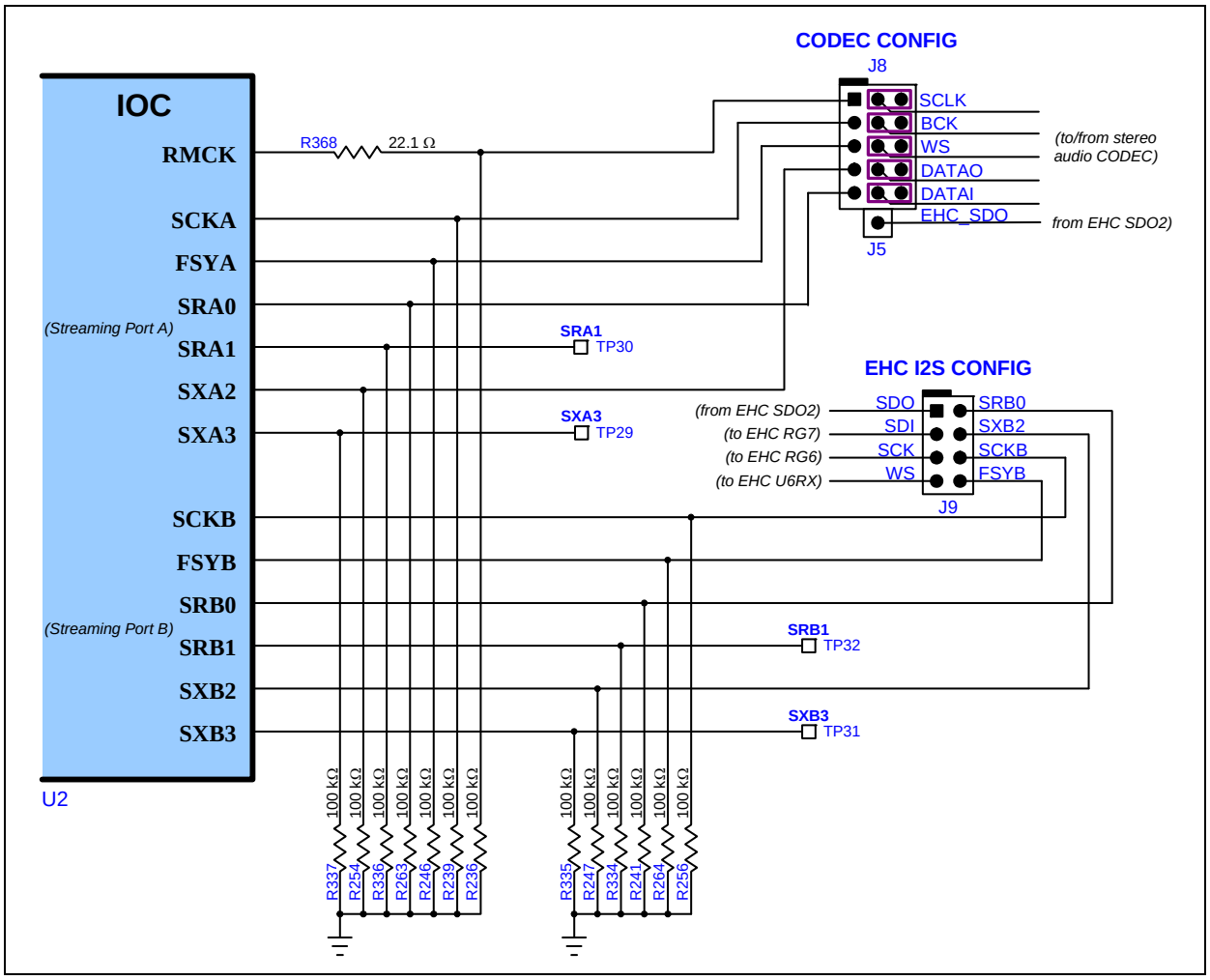
8.4 HBI Port

The OS85650 IOC device includes a high speed parallel interface called the *Host Bus Interface* (HBI); however, this interface is not connected to the EHC on the Eval110 cPHY Board. The IOC HBI Port is available for use with an external device through the *IOC HBI* header (J19).

8.5 Streaming Ports

The two IOC Streaming Ports are used to further extend the network streaming source/sink capabilities of the Eval110 cPHY Board. The IOC's integrated DTCP coprocessor can optionally be used by application code to encrypt/decrypt protected synchronous data streams. The Eval110 cPHY Board is designed to utilize two of the four available serial data pins on each IOC Streaming Port. The serial data pins for Streaming Port A (**SRA0** for receive and **SXA2** for transmit) and clock pins can be connected (with shunts) to the stereo audio CODEC at *CODEC CONFIG* (J8). IOC Streaming Port connection options on the Eval110 cPHY Board are shown in Figure 8-1.

FIGURE 8-1: IOC STREAMING PORT CONNECTION OPTIONS



As shown above, the serial data pins for Streaming Port B (**SRB0** for receive and **SXB2** for transmit) and the associated clock signals can be connected to the EHC (with shunts) at *EHC I2S CONFIG* (J9). Refer to Section 6.6 for more information.

The unused IOC Streaming Port serial data pins (**SRA1**, **SXA3**, **SRB1** and **SXB3**) are accessible via through-hole test-points.

8.6 SPI Ports

The IOC offers up to two SPI Ports; however, the Eval110 cPHY Board connections are configured such that only SPI Port 0 is available for use. SPI Port 1 is unavailable due to pin conflicts with TSI Port 1 (see Section 8.7). In addition to the 4 typical SPI protocol signals (clock, chip select, MOSI and MISO), IOC SPI Port 0 also includes a hardware interrupt (**$\overline{\text{SINT0}}$** pin, connected to EHC RD11) that the EHC can monitor to check the IOC's availability for an SPI transaction.

When IOC SPI Port 0 is enabled, it operates as an SPI bus slave that can exchange asynchronous data packets (i.e. MDPs or MEPs) at a rate of up to 25 Mbps. Typically, the EHC application code implements an SPI bus master for packet data exchange with the IOC. Alternatively, an off-board SPI master can access the IOC via the *IOC SPI* (J15) header.

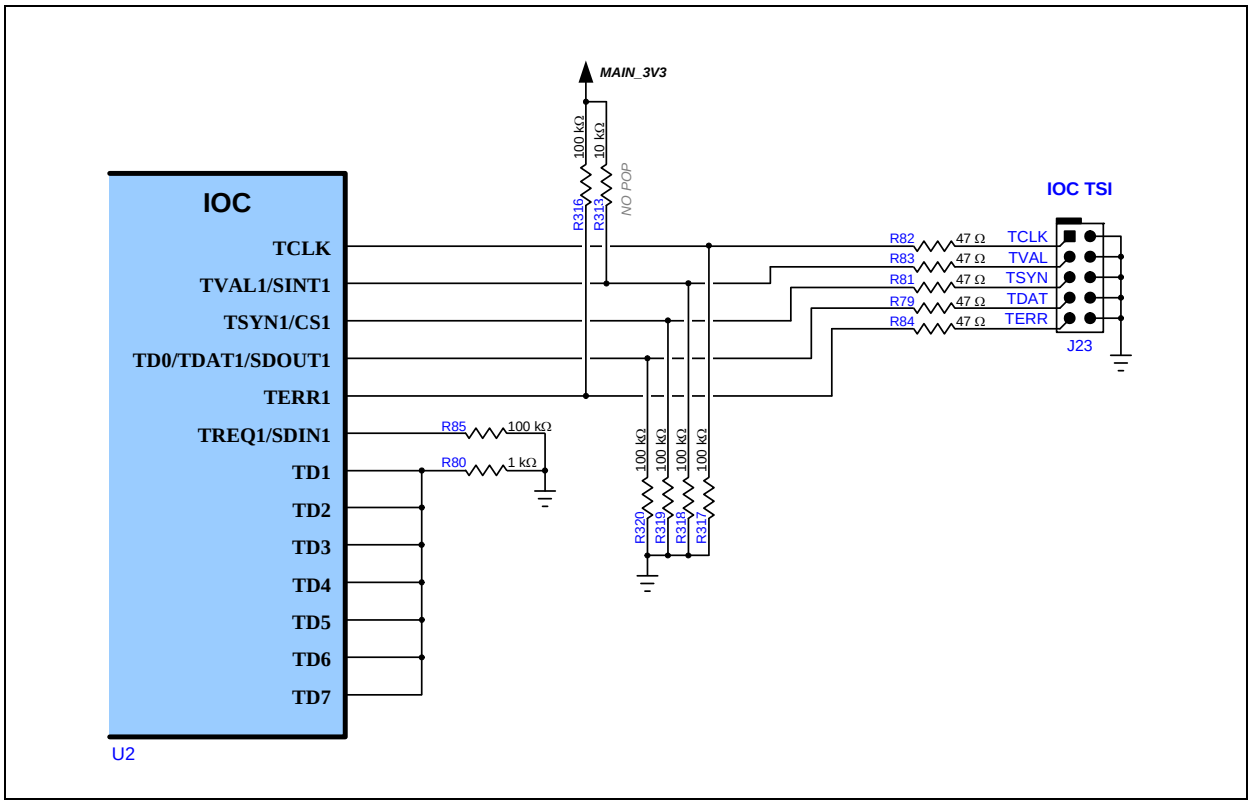
Refer to Section 9.4.5 for more information (including a connection diagram) on the EHC SPI implementation on the Eval110 cPHY Board.

8.7 TSI Ports

The IOC offers up to two TSI Ports; however, the Eval110 cPHY Board connections are configured such that only TSI Port 1 is available for use. TSI Port 0 is unavailable due to pin conflicts with SPI Port 0 (see Section 8.6). Although TSI Port 1 can operate in both serial and parallel mode, only serial mode operation is supported on the Eval110 cPHY Board.

TSI Port 1 can be configured for either TSI stream transmission (master mode) or TSI stream reception (slave mode). The Eval110 cPHY Board does not contain any integrated devices capable of TSI stream exchange with the IOC; therefore an external device is required for all TSI implementations. The Eval110 cPHY Board provides the *IOC TSI* (J23) header (2 mm pitch) to support connection to off-board devices. The IOC TSI Port 1 connections are shown below in Figure 8-2.

FIGURE 8-2: IOC TSI PORT HEADER CONNECTIONS



9.0 EXTERNAL HOST CONTROLLER (EHC)

The on-board EHC ($U4_{2B-3C}$) is a 121-pin BGA PIC32MX795F512L [3] 32-bit microcontroller. This device provides 512 kbytes of on-chip Flash program memory and 128 kbytes of SRAM. The EHC is powered by the 3.3 V switched supply (*MAIN_3V3*), while an internal regulator generates the 1.8 V power required for core logic and integrated memory of the EHC. The main internal clock is derived from the 12 MHz external crystal (Y201), while a 32.768 kHz crystal (Y2) provides the clock source for an internal *Real Time Counter* (RTC).

9.1 PIC32 Configuration Bits

The PIC32 processor has several configuration settings to select options like which oscillator to use at startup, how to set up the PLL to provide the desired CPU clock rate, how the watchdog timer behaves and other settings. The Configuration Bits are described in Section 28 of the PIC32MX5XX/6XX/7XX 32-Bit Microcontrollers Family Data Sheet [3].

The MPLAB X IDE from Microchip provides a built in wizard to help with setting the configuration bits. The wizard is selected from the *Tools -> PIC Memory Views -> Configuration Bits* menu selection. The user selects the desired options, and the wizard generates a *configuration_bits.c* file to include in the project. The configuration bits will then be set according to the settings in the file each time the application is run.

The contents of the *configuration_bits.c* file are show below. Many settings are left at the default value. The main settings configured are to select the 12 MHz external crystal as the clock source, and to scale the 12 MHz clock up to 80 MHz for the CPU clock. Additionally, the peripheral clocks are set to 1/2 the CPU clock rate, and the watchdog timer is disabled.

EXAMPLE 9-1: CONFIGURATION_BITS .C

```
// PIC32MX795F512L Configuration Bit Settings
#include <p32xxxx.h>
// DEVCFG3
// USERID = No Setting
#pragma config FSRSSEL = PRIORITY_7     // SRS Select (SRS Priority 7)
#pragma config FMIIEN = ON              // Ethernet RMII/MII Enable (MII Enabled)
#pragma config FETHIO = ON              // Ethernet I/O Pin Select (Default Ethernet I/O)
#pragma config FCANIO = ON              // CAN I/O Pin Select (Default CAN I/O)
#pragma config FUSBIDIO = ON            // USB USID Selection (Controlled by the USB Module)
#pragma config FVBUSONIO = ON           // USB VBUS ON Selection (Controlled by USB Module)

// DEVCFG2
#pragma config FPLLIDIV = DIV_3         // PLL Input Divider (3x Divider)
#pragma config FPLLMUL = MUL_20         // PLL Multiplier (20x Multiplier)
#pragma config UPLLIDIV = DIV_3         // USB PLL Input Divider (3x Divider)
#pragma config UPLLEN = ON              // USB PLL Enable (Enabled)
#pragma config FPLLODIV = DIV_1         // System PLL Output Clock Divider (PLL Divide by 1)

// DEVCFG1
#pragma config FNOSC = PRIPLL           // Oscillator Selection Bits (Primary Osc w/PLL (XT+,HS+,EC+PLL))
#pragma config FSOSCEN = ON             // Secondary Oscillator Enable (Enabled)
#pragma config IESO = ON                // Internal/External Switch Over (Enabled)
#pragma config POSCMOD = HS             // Primary Oscillator Configuration (HS osc mode)
#pragma config OSCIOFNC = OFF           // CLKO Output Signal Active on the OSCO Pin (Disabled)
#pragma config FPBDIV = DIV_2           // Peripheral Clock Divisor (Pb_Clk is Sys_Clk/2)
#pragma config FCKSM = CSDCMD           // Clock Switching and Monitor Selection (Clock Switch Disable, FSCM Disabled)
#pragma config WDTPS = PS1048576        // Watchdog Timer Postscaler (1:1048576)
#pragma config FWDTEN = OFF             // Watchdog Timer Enable (WDT Disabled (SWDTEN Bit Controls))

// DEVCFG0
#pragma config DEBUG = ON               // Background Debugger Enable (Debugger is enabled)
#pragma config ICESEL = ICS_PGx1        // ICE/ICD Comm Channel Select (ICE EMUC1/EMUD1 pins shared with PGC1/PGD1)
#pragma config PWP = OFF                // Program Flash Write Protect (Disable)
#pragma config BWP = OFF                // Boot Flash Write Protect bit (Protection Disabled)
#pragma config CP = OFF                 // Code Protect (Protection Disabled)
```

9.2 Stand-Alone Mode

A *Stand-Alone* mode should be provided in any EHC application code written for the Eval110 cPHY Board. When this mode is enabled, the EHC should not interact with INIC, the IOC, or any other on-board devices in any way. In *Standard Applications*, this entails disabling the I^2C bus master functionality and tri-stating all I/O pins. When *Stand-Alone* mode is enabled, an off-board EHC is permitted to access the INIC and IOC devices (typically as a external I^2C bus master) through the *MOST CONTROL* (J17) header. Utilizing the Eval110 cPHY Board in this manner provides software developers a hardware reference platform, which enables hardware development with the target EHC before a complete platform is available.

The Eval110 cPHY Board provides the *BOARD OPTIONS* (S2) 8-position dip switch for setting various firmware options. The EHC typically reads the states of the DIP switches during initialization (i.e. immediately following power-up/reset). Microchip application code typically uses one of the DIP switches to indicate whether or not the EHC should operate in *Stand-Alone* mode.

9.3 EHC Flash and Debug

The Eval110 cPHY Board supports several methods of updating and debugging EHC application code. To simply update the application in Flash memory, the installed serial bootloader can be used along with the Microchip PIC32UBL programming utility and a prebuilt HEX file. For debugging as well as loading new applications, the MPLAB X IDE can be used with one of the Microchip debug tools. The applications themselves provide a lot of debug text output via the on-board CommBridge device (U11) which permits following the application execution with a terminal program on the PC through a standard USB connection. Power management should be disabled (DIP Switch 6 closed) when programming the EHC to prevent the board from powering-down inadvertently.

9.3.1 FLASHING FROM PC VIA USB

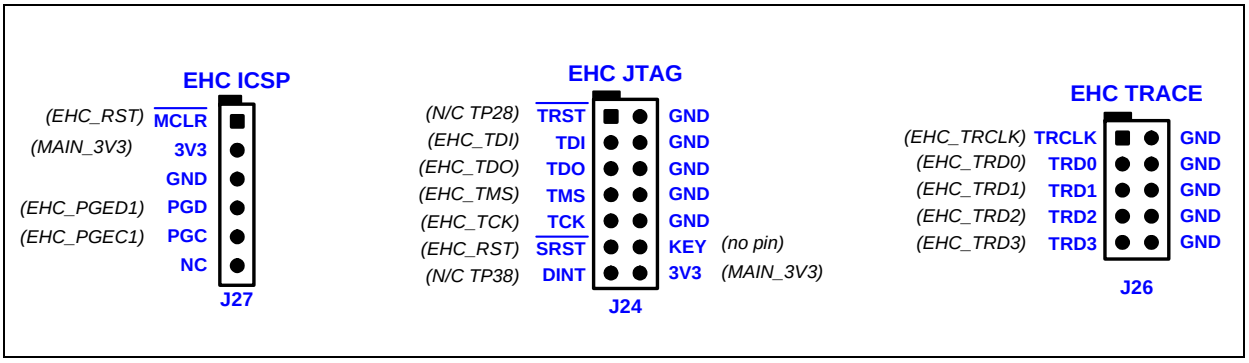
The Eval110 cPHY Board is shipped with the PIC32 Serial Bootloader in Flash memory. This bootloader is available from Microchip and is described in AN1388 PIC32 Bootloader Application Note [20]. The bootloader permits application code updates using the on-board CommBridge. A PC running the Microchip PIC32UBL Flasher Software [21] utility connects to the Eval110 cPHY Board *CB USB* (J7) connector and transmits the firmware image to the CommBridge over a virtual COM port. Then the image is serially programmed into the EHC flash through the UART2 interface.

Note:	Flashing the EHC from the PC through the CommBridge allows Eval110 cPHY Board application code to be updated without the use of any Microchip hardware tools.

To enter the bootloader, the *EHC DFU* (S10) button must be pressed while an EHC reset is performed using either the *EHC RESET* (S6) switch or the *BOARD RESET* (S9) switch. An orange LED (D206) next to the *EHC DFU* button flashes to indicate the bootloader is waiting for commands. If this LED does not flash, either the switches were not pressed properly, or the bootloader is not present.

9.3.2 EHC HARDWARE DEBUG PORTS

FIGURE 9-1: EHC DEBUG AND JTAG HEADERS



The Eval110 cPHY Board supports all of the current Microchip debug tools including the *PICKit3, ICD3*, and *RealICE*. All three emulators can use the standard ICSP programming and debug interface at J27, however, the *ICD3* and *RealICE* will require a cable adapter to convert from the 6 pin RJ45 phone jack on the tool to the straight 6 pin header at J27. The PICKit3 can plug directly onto the J27 header.

For more sophisticated debugging, the Eval110 cPHY Board also supports the full JTAG and Trace Debug features of the PIC32. These interfaces require the use of the *RealICE* debugger along with its JTAG interface board and I/O Port trace cable. The JTAG header is at J24, and the Trace Debug header is at J26. Using these interfaces along with the *RealICE* debugger enables real time instruction trace collection, real time watch, stopwatch, and logic probe inputs and outputs.

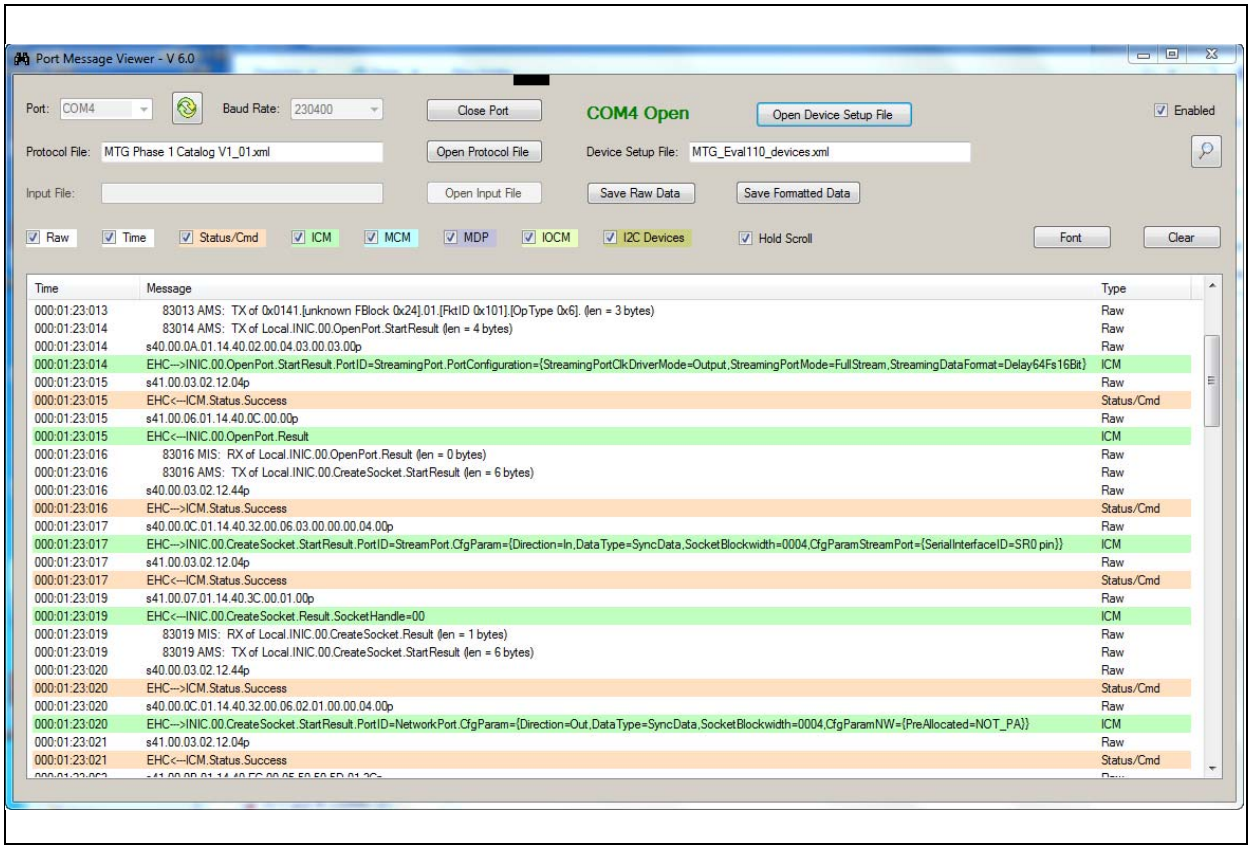
Note:	Caution: When the EHC is programmed using any of the emulators, the EHC's internal bootloader will be erased. This is not a problem as long as the emulator is used for all subsequent programming and debugging. The original bootloader application is available from Microchip and can be reinstalled to re-enable serial flashing through the CommBridge.

9.3.3 DEBUG PRINT STATEMENTS VIA USB

The on-board CommBridge supports transmission of debug print information from the EHC to the PC via a USB connection. Debug information can be viewed on the PC using a terminal application such as Hyperterminal, Tera Term or the Microchip Port Message Viewer PC software [22]. The EHC uses the UART2 interface to send debug information to the CommBridge.

Some excerpts from the debug output of a typical application are shown below. Included in the debug output are messages from the application as it runs, the output of the NetServices™ Trace Module, and the output of a virtual I^2C spy that shows all of the I^2C traffic between the EHC and all of the peripherals including the port messages going to INIC. The Port Message Viewer program can show this output as well as interpret the port messages into a more readable format as shown in Figure 9-2. An example of the raw debug output code is shown in Example 9-2.

FIGURE 9-2: PORT MESSAGE VIEWER INTERPRETED OUTPUT



EXAMPLE 9-2: RAW DEBUG OUTPUT EXAMPLE

```
********************************************************************************
********************************************************************************
Microchip/SMSC
MOST ToGo Master
V2.1.1 MOST 150
********************************************************************************
********************************************************************************
...
Starting main loop
***** Power Management Task Init *****
000:00:00:005 > TASK PMGT: ECLSM Node Class Slot = 1
000:00:00:005 > HALPWR: Reset cause = HAL_PWR_RESET_CAUSE_EXTERNAL_RESET_PIN
000:00:00:005> s11.00.11.0Ap
000:00:00:005> s11.01.11.00p
000:00:00:005> s11.02.11.00p
000:00:00:006> s11.FD.11.08p
000:00:00:006> s11.FE.11.5Dp
000:00:00:006> s11.FF.11.84p
000:00:00:006 > DRVPM: Power Manager IC Version: 08:5D:84
000:00:00:006> s11.0F.11.10p
000:00:00:006 > DRVPM: Powered up due to ON_SW
...
***** Power Management Task Init Finished *****
...
***** MOST Task Init *****
000:00:00:074 >
***** Starting MSMM *****
000:00:00:074 >         74 MNS:  Init
000:00:00:074 >         74 MNS:  Init phase state machine goes into state [state 0x00].
000:00:00:074 >         74 MNS:  Reset phase state machine goes into state [state 0x00].
000:00:00:074 >         74 MNS:  Init of MOST NetServices V3.0.5Distrib    PMS, MIS, MNS, wAMS, wMCS, vMSV, wSCM
000:00:00:075 >         75 MNS:  Init phase state machine goes into state [state 0x08].
000:00:00:076 >
***** MOST Task Init Finished *****
000:00:00:076 > ECLSM: SSEQI wakeup started at 000:00:00:011.
000:00:00:076> s41.00.03.02.1A.80p
000:00:00:077> s40.00.03.02.18.80p
000:00:00:077> s41.00.03.02.1A.90p
000:00:00:078 >         78 MNS:  Init phase state machine goes into state [state 0x09].
000:00:00:078 >         78 MNS:  Init phase state machine goes into state [state 0x0B].
000:00:00:078 >         78 AMS:  TX of Local.INIC.00.EHCIState.Get (len = 0 bytes)
000:00:00:079> s40.00.06.01.14.30.01.00.00p
000:00:00:079> s41.00.03.02.12.04p
000:00:00:080> s41.00.08.01.14.30.0C.00.02.00.00p
000:00:00:080 >         80 MIS:  RX of Local.INIC.00.EHCIState.Status (len = 2 bytes)
000:00:00:080 >         80 MNS:  Transition into EHCIState Protected, cause: Reset.
000:00:00:080 >         80 MNS:  Reset phase state machine goes into state [state 0x00].
000:00:00:080 >         80 MNS:  EHCIState state machine goes into state Protected.
000:00:00:081 >         81 MNS:  Init phase state machine goes into state [state 0x0B].
000:00:00:081 >         81 MNS:  Reset phase state machine goes into state [state 0x04].
000:00:00:081 >         81 MNS:  Reset phase state machine goes into state [state 0x0C].
000:00:00:082> s40.00.03.02.12.44p
000:00:00:082 >         82 MNS:  Reset phase state machine goes into state [state 0x1C].
000:00:00:083 >         83 MNS:  Reset phase state machine goes into state [state 0x5C].
000:00:00:083 >         83 MNS:  Init phase state machine goes into state [state 0x8B].
000:00:00:083 >         83 MNS:  Reset phase state machine goes into state [state 0xDC].
000:00:00:084 >         83 MNS:  Reset phase state machine goes into state [state 0xFFFF].
000:00:00:084 >         84 AMS:  TX of Local.INIC.00.EHCIState.Set (len = 2 bytes)
000:00:00:084 >         84 AMS:  TX of Local.INIC.00.WatchdogMode.SetGet (len = 5 bytes)
000:00:00:085> s40.00.08.01.14.30.00.00.02.01.02p
000:00:00:085> s41.00.03.02.12.04p
000:00:00:086> s40.00.0B.01.14.30.A2.00.05.00.FF.FF.FF.FFp
000:00:00:086> s41.00.03.02.12.04p
000:00:00:086> s41.00.08.01.14.50.EC.00.02.00.00p
000:00:00:087 >         87 MIS:  RX of Local.INIC.00.PMIState.Status (len = 2 bytes)
000:00:00:087> s40.00.03.02.12.44p
000:00:00:088> s41.00.0D.01.14.30.AC.00.07.00.FF.FF.FF.FF.FF.FFp
000:00:00:089 >         89 MIS:  RX of Local.INIC.00.WatchdogMode.Status (len = 7 bytes)
000:00:00:089> s41.00.0D.06.04.00.00.01.01.00.00.2C.00.02.04.00p
000:00:00:090 >         90 MIS:  RX of Local.NetBlock.00.NodePositionAddress.Status (len = 2 bytes)
000:00:00:090> s40.00.03.02.12.44p
000:00:00:090> s40.00.03.02.02.44p
000:00:00:091 > ECLSM: SSEQI tEWU pulse 1 ended at 000:00:00:091.
000:00:00:091> s41.00.0D.06.04.00.00.01.01.00.00.3C.00.02.FF.FFp
000:00:00:092 >         92 MIS:  RX of Local.NetBlock.00.NodeAddress.Status (len = 2 bytes)
000:00:00:092> s40.00.03.02.02.44p
000:00:00:093> s41.00.0D.06.04.00.00.01.01.00.00.4C.00.02.03.C8p
000:00:00:094 >         93 MIS:  RX of Local.NetBlock.00.GroupAddress.Status (len = 2 bytes)
....
000:00:00:114> s41.00.1A.01.14.20.0C.00.14.00.00.08.11.10.10.04.00.01.02.05.14.04.15.00.00.00.01.08.04p
000:00:00:115 >        115 MIS:  RX of Local.INIC.00.VersionInfo.Status (len = 20 bytes)
000:00:00:115 >        115 MNS:  Found INIC OS81110 Rev.D V1.2.5
000:00:00:115 >        115 MNS:  Init phase state machine goes into state [state 0x8F].
...000:00:00:124 >        123 AMS:  TX of Local.INIC.00.EHCIState.Set (len = 1 bytes)
000:00:00:124> s41.00.07.01.14.20.6C.00.01.01p
000:00:00:124 >        124 MIS:  RX of Local.INIC.00.BIST.Status (len = 1 bytes)
000:00:00:125> s40.00.07.01.14.30.00.00.01.02p
000:00:00:125> s41.00.03.02.12.04p
000:00:00:125> s40.00.03.02.12.44p
000:00:00:127> s41.00.07.01.14.30.0C.00.01.02p
000:00:00:127 >        127 MIS:  RX of Local.INIC.00.EHCIState.Status (len = 1 bytes)
000:00:00:127 >        127 MNS:  EHCIState state machine goes into state Attached.
********************************************************************************
000:00:00:128> Most NetServices initialization complete
********************************************************************************
```

9.4 EHC Peripherals

The EHC includes numerous integrated peripherals available for use by the application code. The following sections provide an overview of the available hardware connections on the Eval110 cPHY Board for each EHC peripheral. Refer to the PIC32MX5XX/6XX/7XX 32-Bit Microcontrollers Family Data Sheet [3] for more information on these peripheral interfaces.

9.4.1 I²C COMMUNICATION

The Eval110 cPHY Board implements two separate I²C communication buses [23]. The EHC acts as the bus master for both buses. The *MOST Control Bus* includes the INIC and IOC as slave devices. In *Standard Application* code, all communication between the EHC and INIC/IOC occurs via Port Message exchange with the INIC and IOC Control Ports. This interface can be used to configure INIC and the IOC (at power-up or after reset) based on the EHC application code. The *Board Peripheral Bus* is also mastered by the EHC and includes various peripheral slave devices used by the application. Signals for both buses appear at various headers for connection to off-board devices. The full device listing for each I²C bus is provided in Table 9-1.

TABLE 9-1: ON-BOARD I²C SLAVE DEVICES

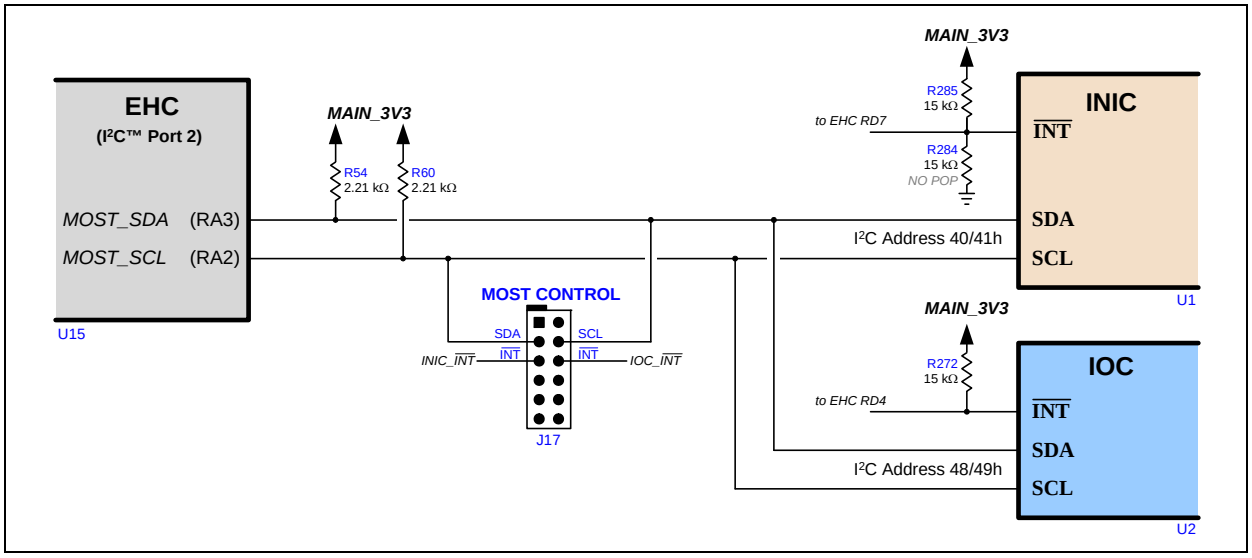
Slave Device	Address *	Description
MOST Control Bus - I²C Port 2		
Microchip OS81110 INIC	40h/41h	MOST150 network interface controller; the EHC can configure INIC through its I²C Control Port using *INIC Control Messages* (ICMs).
Microchip OS85650 IOC	48h/49h	I/O port expansion for INIC; the EHC can configure the IOC through its I²C Control Port using *I/O Control Messages* (IOCMs).
Board Peripheral Bus - I²C Port 4		
Microchip MPM85000 PwrMgr	10h/11h	MOST Network-compliant power management device; manages and controls board power while indicating power status and wakeup events to the EHC.
NXP UDA1380 CODEC	30h/31h	Stereo audio CODEC; Provides an analog line and headphone output with software volume control capability.
Texas Instruments TCA6424 I/O Expander	44h/45h	24-bit GPIO port expansion for the EHC; supports reset and interrupt functionality.
Microchip EEPROM 24LC32AT	A0h/A1h	Connected to the IOC Debug Port for storing optional configuration information. The EHC can program configuration data into this device. (Note: this device is isolated from the rest of the bus with a bus switch (U21) to avoid a multi-master conflict in case a debug tool is plugged into the IOC debug header.)

* Addresses listed in this table are provided in 8-bit format: the 7 most significant bits represent the actual slave address and the least significant bit is the read/write bit.

9.4.1.1 I²C Port 2 - MOST Control Bus

Figure 9-3 shows the I²C connections for the *MOST Control Bus* on the Eval110 cPHY Board.

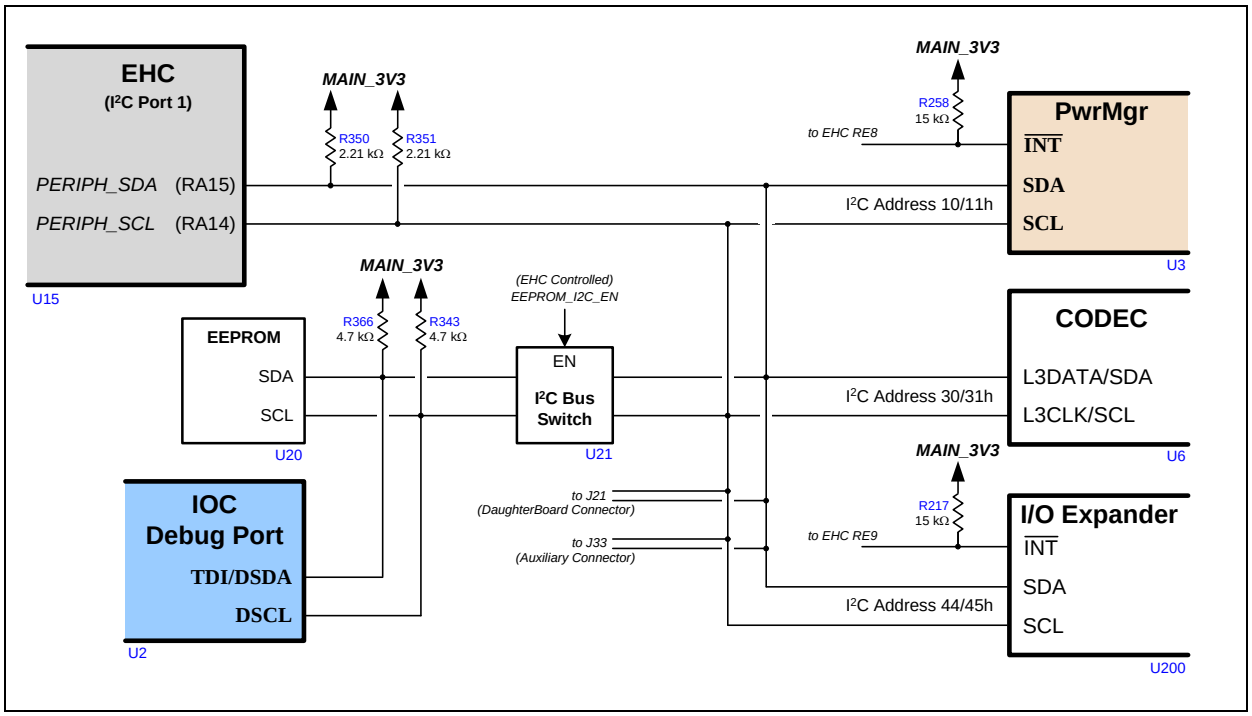
FIGURE 9-3: MOST CONTROL I²C BUS



9.4.1.2 I²C Port 1 - Board Peripheral Bus

Figure 9-4 shows the I²C connections for the *Board Peripheral Bus* on the Eval110 cPHY Board.

FIGURE 9-4: PERIPHERAL I²C BUS.



Note:	When *Stand-Alone* mode (see Section 9.2) is enabled, the EHC should disable its I²C interfaces. This allows an external I²C master to access slave devices on both buses.

An external I^2C slave device with a unique address can be connected to the Eval110 cPHY Board *MOST Control Bus* via the *MOST CONTROL* header (J17), or to the *Board Peripheral Bus* via the, *DAUGHTER BOARD* (J21) or *AUX* (J33) headers. In these scenarios, EHC applications may be written to support communication with the device; however, the I^2C clock speed may need to be lowered as a result of the extra capacitance added by the off-board device.

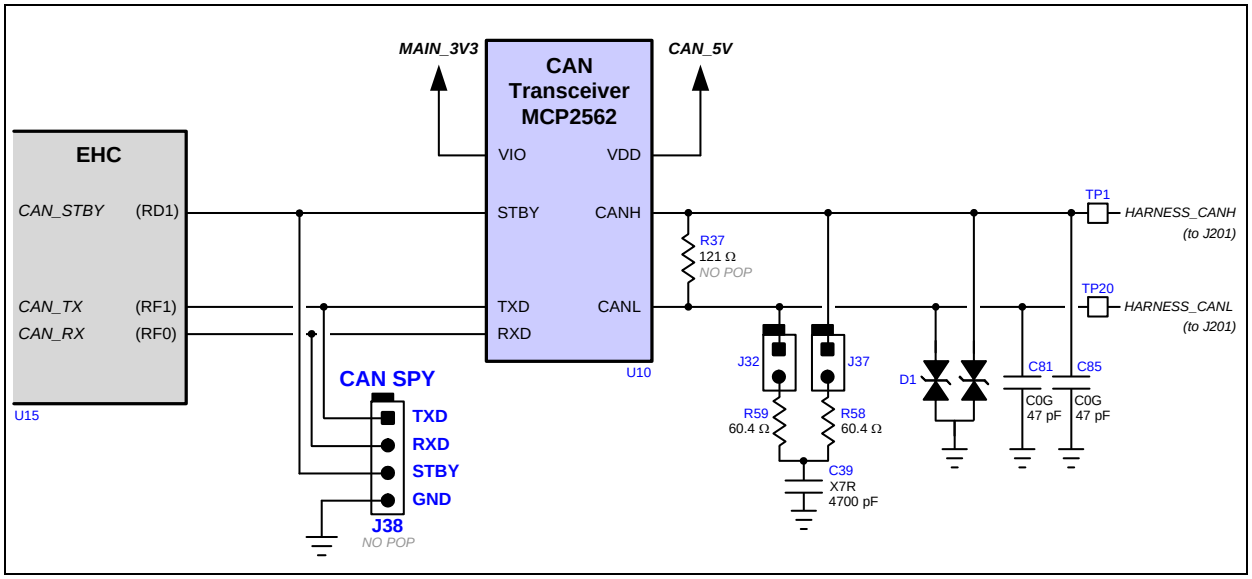
9.4.2 CAN INTERFACE

The Eval110 cPHY Board supports CAN bus gateway applications using the Microchip MCP2562 *High-Speed CAN Transceiver* device [24] connected to the EHC's CAN interface. This CAN transceiver (U10) is fully-compliant with the CAN physical layer specification [25].

An on-board charge pump device (U18) supplies 5 V power to the main CAN supply voltage pin (VDD). The CAN transceiver also offers a dedicated VIO supply pin allowing the interface signals (to the EHC) to operate from the *MAIN 3V3* supply rail. The CAN transceiver is connected to the EHC's CAN interface with two unidirectional data lines (***CAN_TX*** and ***CAN_RX***). Additionally, the EHC uses a GPIO signal (***CAN_STBY***) to set transceiver operational mode.

The CAN interface connection diagram is shown in Figure 9-5.

FIGURE 9-5: CAN INTERFACE



Note: The CAN transceiver STBY pin contains an internal pull-up resistor to VIO.

9.4.3 UART INTERFACES

9.4.3.1 UART Port 4 - LIN/ECL

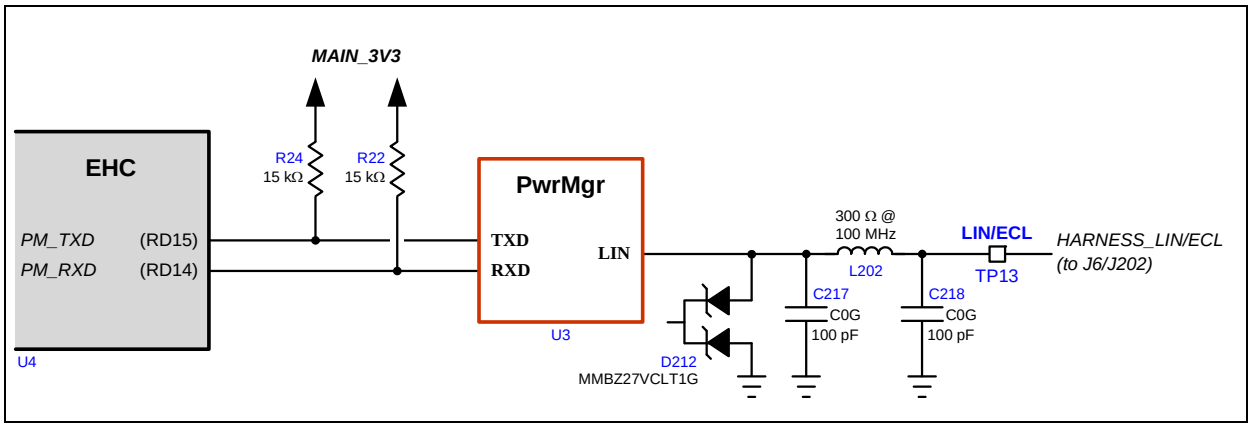
The EHC's UART Port 4 interface is connected to the MPM85000 PwrMgr device (U3) and may be used by the standard application code to implement either Local Interconnect Network (LIN) Specification [26] communication or *MOST ECL* (MOST Electrical Control Line Specification [8]) communication. The LIN/ECL line can be controlled/monitored in the following ways:

- Using the MPM85000 **TXD** and **RXD** hardware pins (connected to the EHC UART Port 4 interface), or
- Via the MPM85000 Control Port (*LIN Control Register*), accessible through the EHC I^2C *Board Peripheral Bus*.

Refer to the MOST INIC Hardware Concepts Technical Bulletin [10] and MOST Electrical Control Line Specification [8] for more information on LIN/ECL communication between network nodes.

The connections for the EHC UART Port 4 interface are shown below in Figure 9-6.

FIGURE 9-6: UART PORT 4 INTERFACE



9.4.3.2 UART Port 2 - CommBridge

The EHC's UART Port 2 interface is connected to the CommBridge for flashing new application code and for debug print functionality. See Section 9.3.3 and Section 12.0 for more information.

9.4.3.3 UART Port 1 - Aux/Misc

The EHC's UART Port 1 interface is connected to various headers on the Eval110 cPHY Board. Depending on the application code, several different options exist for using this interface. The transmit signal (*EHC_TXD*, connected to EHC RF8) can be used for *Low Frequency Signal Tunneling* (LFST) applications by connecting it to an INIC streaming port via the *LFST CONFIG* jumpers at J10. Alternatively, it can be routed an off-board device such as a display connected to the *AUX* header (J33) via the *AUX CONFIG* jumper at J11. Refer to Section 10.0 for more information on LFST applications and the required hardware connections.

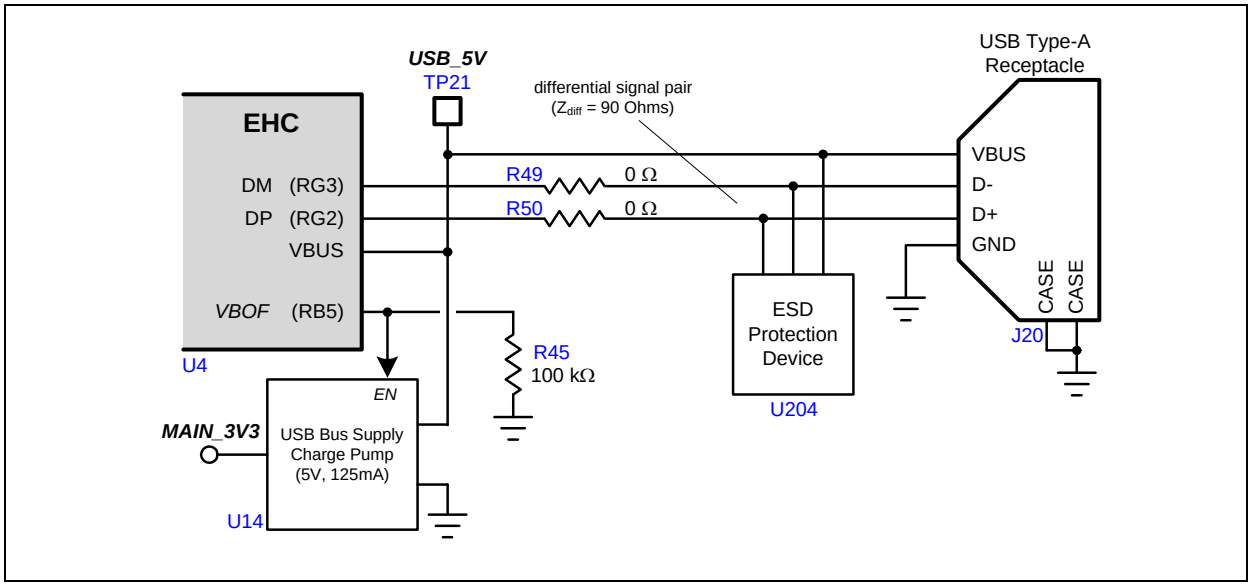
9.4.4 USB

The Eval110 cPHY Board provides a type A USB receptacle connected to the EHC USB port. EHC application code can use this connector to implement a USB host that has access to a variety of peripheral devices (e.g. mass storage applications) attached to the Eval110 cPHY Board. 5 V bus power (up to 125 mA) is provided for attached devices by an on-board charge pump regulator (U14). The EHC USB port also includes a 3-wire ESD suppression device rated for ±15 kV. Figure 9-7 illustrates the hardware interface between the EHC and the *EHC USB* connector (J20).

FIGURE 9-7: USB INTERFACE

9.4.5 SERIAL PERIPHERAL INTERFACE (SPI) PORTS

SPI is a synchronous serial data communication protocol over which a controller (e.g. EHC) can exchange data with various slave devices. The controller generates a universal clock and communicates with slave devices using two unidirectional data signals. Each slave device also has a dedicated chip select signal to prevent data collisions on the bus.

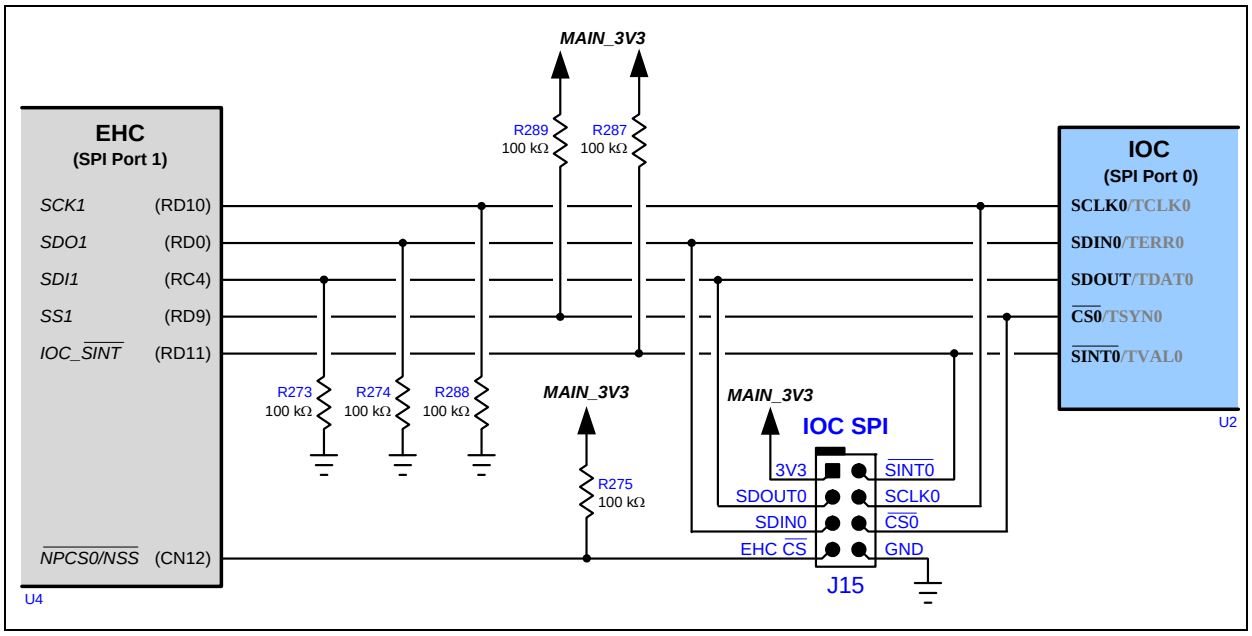


9.4.5.1 SPI Port 1

The EHC SPI Port 1 is connected to the IOC's SPI Port 0. Using this communication interface, the EHC and the IOC can exchange asynchronous data packets (i.e. MDPs, MEPs) at a rate of up to 25 Mbps. The *IOC SPI* header (J15) is also provided to permit EHC connection to an off-board SPI slave device. Alternatively, an off-board SPI master device can be connected to J15 for packet data exchange with the IOC. In this scenario, the EHC may also be configured as an SPI slave.

The connections for the EHC SPI Port 1 are shown in Figure 9-8.

FIGURE 9-8: EHC SPI PORT 1 CONNECTIONS



9.4.6 SPI PORT 2 STREAMING AUDIO

The EHC SPI module includes an *Audio Protocol Interface Mode* (Section 23 in the PIC32 Family Reference Manual [27]) which provides a 4-wire, bidirectional, synchronous, digital audio link with external audio devices. The format of the digital data is compatible with some of the I^2S formats supported by INIC or the OS85650 I/O Companion

(IOC) on the Eval110 cPHY Board. The EHC application code must run the port in slave mode operation where the serial bit clock SCK2 (also known as BCLK) and the word select clock SS2 (also called LRCK or FSY) are driven by an external master (i.e. the IOC), so that the audio data is synchronous to the MOST Network.

The EHC SPI Port 2 can optionally be connected to the IOC Streaming Port B (with jumper shunts) using the *EHC I2S CONFIG* header (J9), as shown in Figure 8-1. This connection permits an audio source application on the EHC to exchange streaming audio data over the MOST Network. In this scenario, the IOC acts as an I^2S-to-MediaLB bridge between the EHC and the INIC.

Additionally, the EHC's SPI module may be used in *Low Frequency Signal Tunneling* (LFST) applications. Use of the EHC SPI module in *Audio Protocol Interface Mode* is further described in Section 10.0.

9.5 GPIO Reference

Table 9-2 provides a list of all EHC GPIO connections on the Eval110 cPHY Board. The GPIO channels are divided into the register groupings as defined by the PIC32 GPIO architecture. For exact hardware connections on each EHC GPIO pin, refer to the **Appendix E: "Layout Plots"** and **Appendix D: "Schematics"**.

TABLE 9-2: EHC GPIO REFERENCE

Pin Name	GPIO #	Pin #	Net Name	EHC Peripheral	Description / Notes	Component
Register Bank A (s19)						
RA0	GPIO00	G3	***EHC_TMS***	JTAG	EHC JTAG interface test mode select input	U4-G
RA1	GPIO01	J6	***EHC_TCK***	JTAG	EHC JTAG interface test clock input	U4-G
RA2	GPIO02	H11	***MOST_SCL***	I^2C 2	MOST I^2C Bus clock signal	U4-G
RA3	GPIO03	G10	***MOST_SDA***	I^2C 2	MOST I^2C Bus serial data signal	U4-G
RA4	GPIO04	G11	***EHC_TDI***	JTAG	EHC JTAG interface test data input	U4-G
RA5	GPIO05	G9	***EHC_TDO***	JTAG	EHC JTAG interface test data output	U4-G
RA6	GPIO06	C5	***EHC_TRCLK***	TRACE	EHC Instruction Trace Clock	U4-F
RA7	GPIO07	B5	***EHC_TRD3***	TRACE	EHC Instruction Trace Data 3	U4-E
RA9	GPIO09	L2	***INIC_$\overline{RST}$***	GPIO	INIC reset signal	U4-H
RA10	GPIO10	K3			Open Pin	U4-H
RA14	GPIO14	E11	***PERIPH_SCL***	I^2C 4	Peripheral I^2C Bus clock signal	U4-F
RA15	GPIO15	E8	***PERIPH_SDA***	I^2C 4	Peripheral I^2C Bus serial data signal	U4-F
Register Bank B (s19)						
RB0	GPIO16	K2	***EHC_PGED1***	PGED1	EHC Programming Data	U4-H
RB1	GPIO17	K1	***EHC_PGEC1***	PGEC1	EHC Programming Clock	U4-H
RB2	GPIO18	J2	***EHC_DFU***	GPIO	EHC Device Firmware Update indicator signal: 0 - Boot mode, bootloader expecting flash commands 1 - EHC bootloader jumps to application (default)	U4-G
RB3	GPIO19	J1	***EHC_DFU_LED***	GPIO	LED Flashing indicates DFU mode	U4-G
RB4	GPIO20	H2			Open Pin	U4-G
RB5	GPIO21	H1	***USB_VBUS_EN***	VBUSON	Control signal for USB 5 V charge pump (U14)	U4-G
RB6	GPIO22	L1	***CODEC_RST***	GPIO	Audio CODEC reset signal	U4-H
RB7	GPIO23	J3			Open Pin	U4-G
RB8	GPIO24	K4	***IOC_DBG***	GPIO	IOC debug configuration signal	U4-H
RB9	GPIO25	L4	***INIC_ERR/$\overline{BOOT}$***	GPIO	INIC error indicator; boot mode enable pin	U4-H
RB10	GPIO26	L5	***IOC_$\overline{RST}$***	GPIO	IOC reset signal	U4-H
RB11	GPIO27	J5			Open Pin	U4-G
RB12	GPIO28	J7			Open Pin	U4-H

TABLE 9-2: EHC GPIO REFERENCE (CONTINUED)

Pin Name	GPIO #	Pin #	Net Name	EHC Peripheral	Description / Notes	Component
RB13	GPIO29	L7	***EHC_PWROFF***	GPIO	PwrMgr power-down signal: 0 - EHC is holding ECU power on 1 - EHC is not holding ECU power on	U4-H
RB14	GPIO30	K7	***CB_$\overline{READY}$***	GPIO	CommBridge ready signal; connected to MCP2200 GP3	U4-H
RB15	GPIO31	L8	***EHC_$\overline{NPCS0/NSS}$***	SPI 1	SPI chip select signal for off-board device (attached to J15); EHC SPI slave select signal for external controller	U4-H
Register Bank C (s19)						
RC1	GPIO33	D1			Open Pin	U4-F
RC2	GPIO34	E4			Open Pin	U4-F
RC3	GPIO35	E2			Open Pin	U4-F
RC4	GPIO36	E1	***IOC_SDOUT0***	SPI 1	SPI data output signal for IOC (EHC MISO)	U4-F
RC12	GPIO44	F9	***EHC_XIN0***	OSC	12 MHz crystal input for EHC main clock	U4-G
RC13	GPIO45	C10	***EHC_XIN32***	SOSC	32.768 kHz crystal input for EHC RTC clock	U4-F
RC14	GPIO46	B11	***EHC_XOUT32***	SOSC	32.768 kHz crystal output for EHC RTC clock	U4-E
RC15	GPIO47	F11	***EHC_XOUT0***	OSC	12 MHz crystal output for EHC main clock	U4-G
Register Bank D (s19)						
RD0	GPIO48	D9	***IOC_SDIN0***	SPI 1	SPI data input signal for IOC (EHC MOSI)	U4-F
RD1	GPIO49	A11	***CAN_STBY***	GPIO	CAN PHY mode configuration signal	U4-E
RD2	GPIO50	A10			Open Pin	U4-E
RD3	GPIO51	B9			Open Pin	U4-E
RD4	GPIO52	C8	***IOC_$\overline{INT}$***	GPIO	IOC interrupt signal	U4-F
RD5	GPIO53	B8			Open Pin	U4-E
RD6	GPIO54	D7	***DC_I/O_$\overline{INT}$***	GPIO	DaughterBoard I/O Expander interrupt signal	U4-F
RD7	GPIO55	C7	***INIC_$\overline{INT}$***	GPIO	INIC interrupt signal	U4-F
RD8	GPIO56	E9	***EHC_SWA***	GPIO	Debounced output (from U210) of tactile switch, SWA	U4-F
RD9	GPIO57	E10	***IOC_$\overline{CS0}$***	SPI 1	SPI chip select signal for IOC	U4-F
RD10	GPIO58	D11	***IOC_SCLK0***	SPI 1	SPI clock signal for IOC	U4-F
RD11	GPIO59	C11	***IOC_$\overline{SINT0}$***	GPIO	IOC SPI Port interrupt signal	U4-F
RD12	GPIO60	A9	***AUX_$\overline{INT}$***	GPIO	Interrupt signal for external device attached to J33	U4-E
RD13	GPIO61	D8	***DC_$\overline{INT}$***	GPIO	DaughterBoard interrupt signal	U4-F
RD14	GPIO62	L9	***PM_RXD***	UART 4	PwrMgr ECL/LIN receive data signal	U4-H
RD15	GPIO63	K9	***PM_TXD***	UART 4	PwrMgr ECL/LIN transmit data signal	U4-H
Register Bank E (s19)						
RE0	GPIO64	A4	***DC_$\overline{READY}$***	GPIO	DaughterBoard ready signal: 0 - external device (at J21) is ready for access 1 - device (at J21) is not ready for access	U4-E
RE1	GPIO65	B4			Open Pin	U4-E
RE2	GPIO66	B3			Open Pin	U4-E
RE3	GPIO67	A2	***DC_$\overline{RST}$***	GPIO	DaughterBoard reset signal	U4-E
RE4	GPIO68	A1	***IOC_ERROR***	GPIO	IOC error indicator (not locked)	U4-E
RE5	GPIO69	D3			Open Pin	U4-F

TABLE 9-2: EHC GPIO REFERENCE (CONTINUED)

Pin Name	GPIO #	Pin #	Net Name	EHC Peripheral	Description / Notes	Component
RE6	GPIO70	C1	***EHC_SWB***	GPIO	Debounced output (from U210) of tactile switch, SWB	U4-E
RE7	GPIO71	D2			Open Pin	U4-F
RE8	GPIO72	G1	***PM_$\overline{INT}$***	GPIO	PwrMgr interrupt signal	U4-G
RE9	GPIO73	G2	***I/O_EXP_$\overline{INT}$***	GPIO	I/O Expander interrupt signal	U4-G
Register Bank F (s19)						
RF0	GPIO80	B6	***CAN_RX***	CAN 1	EHC CAN Interface channel 1 receive signal	U4-E
RF1	GPIO81	A6	***CAN_TX***	CAN 1	EHC CAN Interface channel 1 transmit signal	U4-E
RF2	GPIO82	K11	***EHC_RXD***	UART 1	EHC UART receive data signal (for LFST and auxiliary applications)	U4-H
RF3	GPIO83	K10	***USB_ID***	USB	ID Pin for USB	U4-D
RF4	GPIO84	L10	***CB_TXD***	UART 2	CommBridge UART transmit data signal (EHC RXD)	U4-H
RF5	GPIO85	L11	***CB_RXD***	UART 2	CommBridge UART receive data signal (EHC TXD)	U4-H
RF8	GPIO88	J10	***EHC_TXD***	UART 1	EHC UART transmit data signal (for LFST and auxiliary applications)	U4-H
RF12	GPIO92	K6	***CB_RTS***	UART 2	CommBridge UART Request To Send	U4-H
RF13	GPIO93	L6	***CB_CTS***	UART 2	CommBridge UART Clear To Send	U4-H
Register Bank G (s19)						
RG0	GPIO96	A5			Open Pin	U4-E
RG1	GPIO97	E6			Open Pin	U4-F
RG2	GPIO98	H10	***USB_D+***	USB	USB Differential Data Pin	U4-D
RG3	GPIO99	J11	***USB_D-***	USB	USB Differential Data Pin	U4-D
RG6	GPIO102	E3	***EHC_I2S_SCK***	SPI 2	EHC I^2S Port serial data bit clock	U4-F
RG7	GPIO103	F4	***EHC_I2S_SDI***	SPI 2	EHC I^2S Port serial data input	U4-G
RG8	GPIO104	F2	***EHC_I2S_SDO***	SPI 2	EHC I^2S Port serial data output	U4-G
RG9	GPIO105	F3	***EHC_I2S_WS***	SPI 2	EHC I^2S Port word select / TDM frame sync	U4-G
RG12	GPIO108	C3	***EHC_TRD1***	TRACE	EHC Instruction Trace Data 1	U4-E
RG13	GPIO109	A3	***EHC_TRD0***	TRACE	EHC Instruction Trace Data 0	U4-E
RG14	GPIO110	C4	***EHC_TRD2***	TRACE	EHC Instruction Trace Data 2	U4-E
RG15	GPIO111	B2			Open Pin	U4-E

9.6 I/O Expander

The Eval110 cPHY Board includes a 24-bit TCA6424AR I^{2}C Port Expander device (U200) that provides the EHC with additional GPIO capabilities. The I/O expander resides at address 44/45h on the EHC's peripheral I^{2}C bus. The I/O expander includes reset and interrupt functionality: the reset pin is tied directly to the ***EHC_$\overline{RST}$*** line and the device will alert the EHC of a change on any of its input pins by asserting the ***I/O_EXP_$\overline{INT}$*** signal (connected to EHC pin RE9). Table 9-3, below, describes the 24 I/O channels on the I/O expander.

TABLE 9-3: I/O EXPANDER SIGNAL REFERENCE

Pin Name	Pin #	Net Name	Description / Notes	Component
Gate B: I/O Expander (U200) Bank 0 (s21)				
P00	1		8-position DIP switch (*BOARD OPTIONS*), DIP switch 1	S2
P01	2		8-position DIP switch (*BOARD OPTIONS*), DIP switch 2	S2
P02	3		8-position DIP switch (*BOARD OPTIONS*), DIP switch 3	S2
P03	4		8-position DIP switch (*BOARD OPTIONS*), DIP switch 4	S2
P04	5		8-position DIP switch (*BOARD OPTIONS*), DIP switch 5	S2
P05	6		8-position DIP switch (*BOARD OPTIONS*), DIP switch 6	S2
P06	7		8-position DIP switch (*BOARD OPTIONS*), DIP switch 7	S2
P07	8		8-position DIP switch (*BOARD OPTIONS*), DIP switch 8	S2
Gate C: I/O Expander (U200) Bank 1 (s21)				
P10	9		16-position coded rotary switch (*ID*), bit 0	S1
P11	10		16-position coded rotary switch (*ID*), bit 1	S1
P12	11		16-position coded rotary switch (*ID*), bit 2	S1
P13	12		16-position coded rotary switch (*ID*), bit 3	S1
P14	13	***$\overline{LED1}$***	Control signal for *EHC LED 1* (green)	D203
P15	14	***$\overline{LED2}$***	Control signal for *EHC LED 2*, (yellow)	D202
P16	15	***$\overline{LED3}$***	Control signal for *EHC LED 3*, (orange)	D201
P17	16	***$\overline{LED4}$***	Control signal for *EHC LED 4*, (red)	D200
Gate D: I/O Expander (U200) Bank 2 (s21)				
P20	17	***EEPROM_I2C_EN***	Control signal for I^{2}C bus switch: • 0 - EHC peripheral I^{2}C bus isolated from IOC Debug Port (default) • 1 - EHC peripheral I^{2}C bus connected to IOC Debug Port (allows EHC to program IOC configuration data into EEPROM)	U21
P21	18		Unused pin - connected to TP4	
P22	19		Unused pin - connected to TP46	
P23	20	***AUX_$\overline{ATT}$***	External device attached signal for *AUX* connector	J33
P24	21	***REM_PWR_EN***	Control signal for high-side switch for remote power: • 0 - switch off (remote devices not powered) • 1 - switch on (*12VP_SW* power connected to pin 1	U201 J200
P25	22	***REM_PWR_STATUS***	Fault status output from remote power high-side switch	U201
P26	23		Unused pin - connected to TP3	
P27	24	***DC_$\overline{ATT}$***	External device attached signal for *DAUGHTERBOARD* header	U21

10.0 AUDIO AND LOW FREQUENCY SIGNAL TUNNELING (LFST)

The Eval110 cPHY Board supports applications that route streaming audio data between the network and local audio jacks. On-board jumper options permit a variety of network streaming source/sink implementations between the INIC/IOC and the stereo audio CODEC for A/D and D/A conversion.

The Eval110 cPHY Board also supports *Low Frequency Signal Tunneling* (LFST) over the MOST Network's synchronous channel. LFST can be used to transport UART data, IR data, and other low frequency digital signals over the network thereby eliminating the need for additional dedicated wiring.

10.1 Stereo Audio CODEC

The Eval110 cPHY Board implements network audio source/sink capabilities with NXP's *UDA130 Stereo Audio CODEC* [28]. The CODEC device (U6) includes an ADC which provides a network audio source by converting analog input (blue jack, J2) to digital I^2S format. The CODEC also includes a DAC which provides a network audio sink by converting streaming network audio data (in digital I^2S format) to analog output. The DAC is capable of driving headphones (lime green jack, J3). The EHC application code can manage the CODEC over the peripheral I^2C bus (address 30/31h), providing initial configuration as well as volume, base, treble and mute control.

To support a MOST Network audio source channel, EHC application code can provide an FBlock `AuxIn`. Using this FBlock, an audio channel between the INIC or IOC Streaming Port and the CODEC's ADC (e.g. 16-bit, I^2S format) could be setup and managed over the network.

Similarly, to support a MOST Network audio sink channel, EHC application code can provide an FBlock `AudioAmp`. Using this FBlock, an audio channel between the INIC or Streaming Port and the CODEC's DAC (e.g. 16-bit, I^2S format) could be setup and managed over the network.

In MOST150 systems, audio data exchanged over the network must be synchronous to the MOST Network frame rate (Fs). Therefore, the CODEC is operated in clock slave mode (i.e. the CODEC bit clock and word clock signals are inputs). The INIC or IOC Streaming Port bit clock and frame sync signals should be configured as outputs. Additionally, the CODEC system clock input should be connected to the recovered master clock synchronization signal (either *INIC_RMCK* or *IOC_RMCK*).

> **Note:** Once the audio clocks are properly configured and connected (via J8, *CODEC CONFIG*), the EHC must ensure the CODEC reset line (***CODEC_RST***, connected to EHC RB6) is high for proper operation.

10.1.1 DAC CONTROL

The DAC supports mute and volume control from 0 dB to -78 dB attenuation (in 0.25 dB steps). The ADC supports mute and volume control from -63.5 dB to 24 dB attenuation (in 0.5 dB steps). Typically, application code uses 2 dB steps from the network.

For DAC volume control, the 16 bit, *Master Volume Control* register (address 10h) is used, in which the upper byte (**MVCR[7:0]**) controls the right channel and the lower byte (**MVCL[7:0]**) controls the left channel. For 2 dB steps, the byte values change by 8 for each channel, as shown in Table 10-1.

TABLE 10-1: DAC VOLUME TRANSLATION

Volume	Network Value	MVCR/MVCL	Comments
0 dB	20h	00h/00h	Maximum value
-2 dB	1Fh	08h/08h	
-4 dB	1Eh	10h/10h	
-12 dB	1Ah	30h/30h	Power-up default
-76 dB	02h	F0h/F0h	
-78 dB	01h	F8h/F8h	
Mute	00h	FCh/FCh	Minimum value; exception to algorithm

For DAC mute control, application code typically uses the *Master Mute* bit in register address 13h. This bit (**MTM**) is set when Mute is `On` and cleared when Mute is `Off` (Note: **MT2** is always set when writing **MTM**).

For DAC Bass (boost) control, application code should use register address 12h, where **BBL[3:0]** controls the left channel and **BBR[3:0]** controls the right channel. The mapping is directly proportional with one DAC Bass bit movement for every one network value, with a range of 0 to 9 (+18 dB). This range covers both DAC Bass sets.

For DAC Treble (boost) control, application code should use the same register address (12h); **TRL[1:0]** controls the left channel and **TRR[1:0]** controls the right channel. The mapping is directly proportional with one DAC Treble bit movement for every one network value, with a range of 0 to 3 (+6 dB).

10.1.2 ADC CONTROL

For ADC volume control (if supported), application code should use the 16 bit, *Decimator Volume Control* register (address 20h), where the upper byte (**ML_DEC[7:0]**) controls the left channel and the lower byte (**MR_DEC[7:0]**) controls the right channel. For 2 dB steps, the byte values change by 4 for each channel, as shown in Table 10-2.

TABLE 10-2: ADC VOLUME TRANSLATION

Volume	Network Value	ML_DEC/MR_DEC	Comments
24 dB	2Ch	30h/30h	Maximum value
2 dB	21h	04h/04h	
0 dB	20h	00h/00h	Power-up default
-2 dB	19h	FCh/FCh	
-62 dB	01h	84h/84h	
Mute	00h	80h/80h	Minimum value

For ADC mute control, application code should use the *Decimator Mute* bit in register address 21h. This bit (**MT_ADC**) is set when Mute is `On` and cleared when Mute is `Off`.

For ADC `InputGainOffset()` (if supported), the application code should use the *PGA Gain* bits in register address 21h, where **PGA_GAINCTRLR[3:0]** controls the right channel and **PGA_GAINCTRLL[3:0]** controls the left channel. Since `InputGainOffset()` is specified in dB, and the CODEC step size is 3 dB, every increment of the CODEC gain value from the network is multiplied by 3.

TABLE 10-3: ADC INPUTGAINOFFSET MAPPING

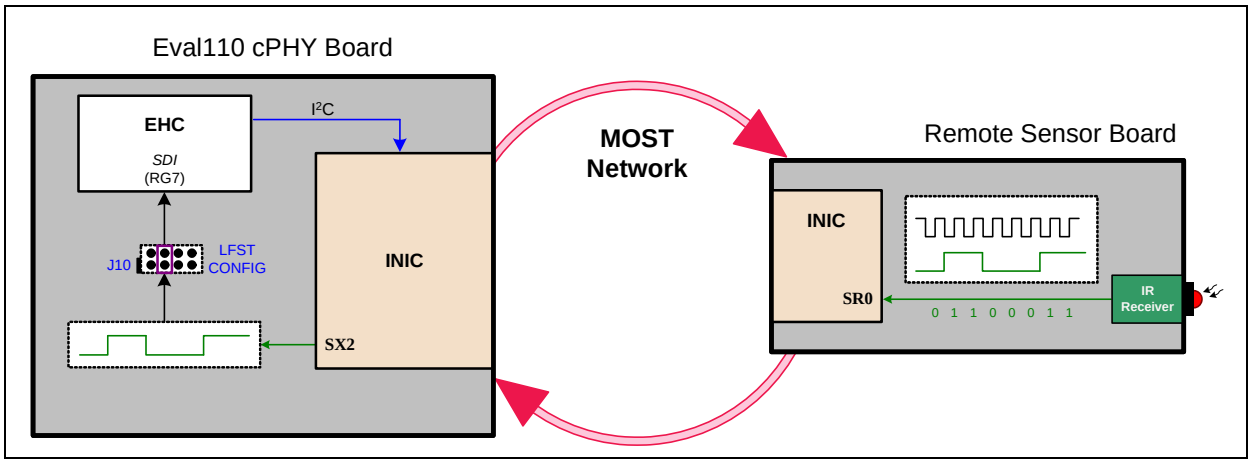
Volume	Network Value	PGA_GAINCTRLR/L	Comments
0 dB	20h	00h/00h	Maximum value
-2 dB	1Fh	08h/08h	
-4 dB	1Eh	10h/10h	
-12 dB	1Ah	30h/30h	Power-up default
-76 dB	02h	F0h/F0h	
-78 dB	01h	F8h/F8h	
Mute	00h	FCh/FCh	Minimum value; exception to algorithm

10.2 Low Frequency Signal Tunneling

The Eval110 cPHY Board supports *Low Frequency Signal Tunneling* (LFST) over the MOST Network's synchronous channel. LFST is used to transport low frequency digital signals (e.g. UART or IR data) over the network thereby eliminating the need for additional dedicated wiring.

Figure 10-1 shows a typical LFST application running in a system with an Eval110 cPHY Board. A digital bitstream from an IR receiver (at the remote sensor node) is oversampled at an INIC Streaming Port input pin. The data is transmitted over the MOST Network synchronous channel using 1 byte of bandwidth and then regenerated locally at an INIC Streaming Port output pin. The *LFST CONFIG* jumper (J10) is configured to connect the regenerated bitstream to an EHC input pin so the signal can be decoded by the application.

FIGURE 10-1: LFST TYPICAL APPLICATION

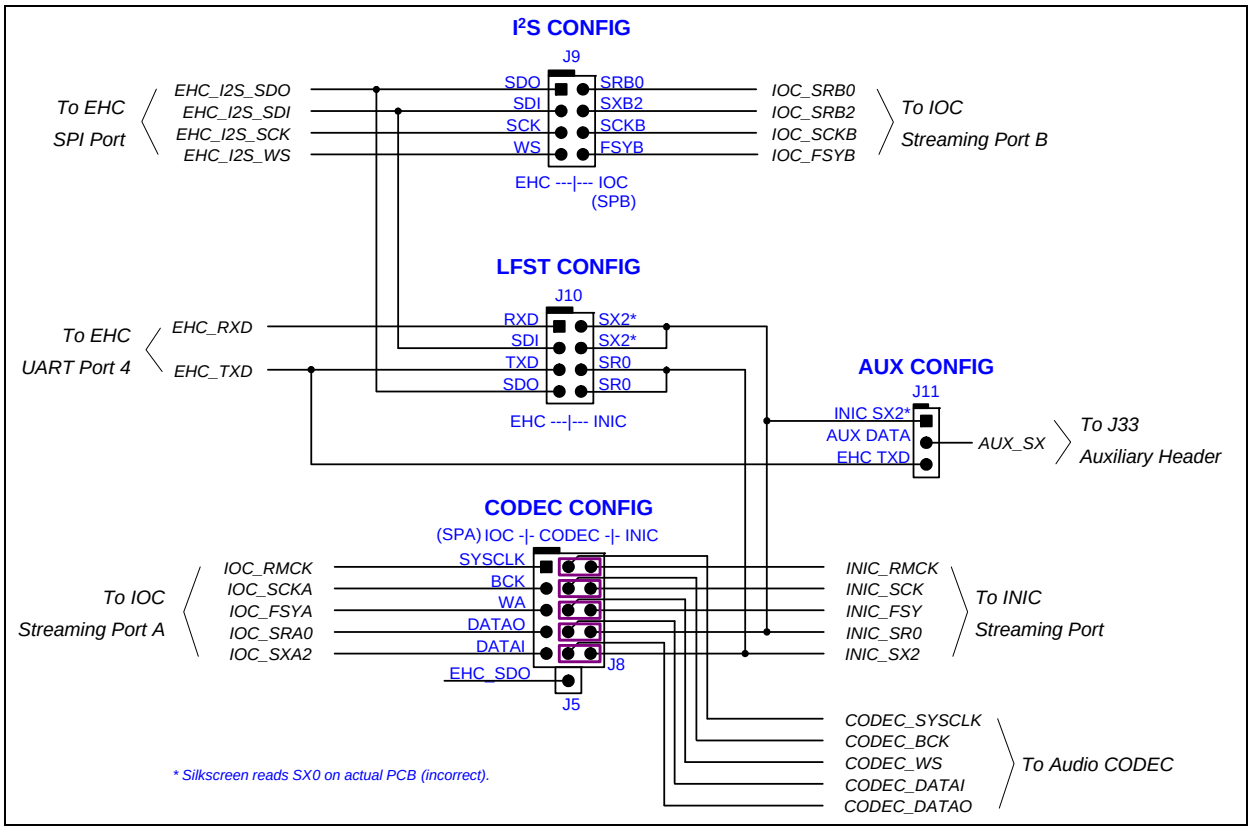


Various connection options exist on the Eval110 cPHY Board to support both the sourcing and sinking of LFST data streams to/from the network using serial data pins at the INIC Streaming Port. LFST data streams can be exchanged with the EHC using the *LFST CONFIG* header (J10), as shown in Figure 6-4. Also, the INIC serial data output pin can be connected to an off-board device (connected to the *AUX* header, J33) by configuring jumper options at the *AUX CONFIG* header (J11). Note that the *AUX CONFIG* header can also be used to connect an EHC UART transmit pin to an external device attached to J33.

10.3 Hardware Connection Options

The Eval110 cPHY Board provides several of jumper options to support a variety of streaming audio and low frequency signal tunneling applications. A full overview of the hardware connection options is provided in Figure 10-2, below.

FIGURE 10-2: AUDIO AND LFST CONNECTION OPTIONS



11.0 POWER MANAGEMENT

The Eval110 cPHY Board integrates MPM85000 Power Management [5] (PwrMgr) (U3), which is a MOST Network-compliant power management device. On the Eval110 cPHY Board, the PwrMgr and external circuitry support:

- Status outputs connected to an external power management interface (EHC or INIC),
- Control signal for switching 12 V power to the application regulators,
- Reset generator output connected to the board reset circuitry,
- Wakeup signaling via Local Interconnect Network (LIN) [26] or MOST Electrical Control Line (ECL) [8]
- MOST150 cPHY network activity detection at *SP3*,
- Detection and qualification of local application wakeup events using **ON_SW** and **STATUS** inputs,
- I^2C slave port for status monitoring and configuration by the EHC,
- Temperature monitoring and reporting, and
- Low-power operation (*Sleep Power State*) - <100 µA total quiescent current from main 12 V supply (*VBATT*).

Power management functionality is enabled by hardware when DIP switch 6 is *OPEN* (default). When enabled, the PwrMgr controls 12 V protected and switched board power (*12VP_SW*). The PwrMgr powers-down the board based on the state of its **PWROFF** input pin, which can be influenced by the EHC, INIC, or both. The Eval110 cPHY Board is designed to support all three options; however, the INIC exclusively influences board power-down by default.

> **Note:** To initially power the Eval110 cPHY Board, the main board power switch (S3) must be *ON* and the main board power supply (e.g. supplied through the *BOARD POWER* connector (J6) and measured at the PwrMgr **VPRO** pin) must be above the minimum *Power On Voltage*, as defined in Appendix A: "Operating Conditions" on page 50.

11.1 Sleep Power State

The Eval110 cPHY Board supports a *Sleep Power State* (defined in the MOST Specification 3.0 [7]) in which the PwrMgr places the board in a low power mode of operation. This is accomplished when the PwrMgr releases the ***ENABLE*** signal (pulled high on the board), disabling the 12 V input power (*12VP_SW*) to the 3.3 V and 1.8 V application regulators. Disabling these supplies powers-down INIC, the EHC, and other board devices.

During normal operation, the PwrMgr attempts to enter the *Sleep Power State* when wakeup/interrupt events are not present. On the Eval110 cPHY Board, the EHC may optionally hold-off the *Sleep Power State* by either driving the ***EHC_PWROFF*** signal low or setting the PwrMgr **HOLD** bit (MPM85000 *Voltage Control Register*, 0x06).

As part of its monitoring and diagnostic functionality, the PwrMgr may also force the Eval110 cPHY Board into the *Sleep Power State* in certain under-voltage conditions. See the MPM85000 Automotive Power Management Device Data Sheet [5] for more information.

When the PwrMgr enters the *Sleep Power State*, current consumption is minimized with the switched supplies disabled; however, the PwrMgr continues to monitor board power/status and outputs a 3.3 V continuous micro-regulated supply (*CONT_3V3*). The Eval110 cPHY Board remains in the *Sleep Power State* until a wakeup event (described in Section 11.2 "Wakeup and Interrupt Events") is recognized by the PwrMgr's internal logic.

11.2 Wakeup and Interrupt Events

When the Eval110 cPHY Board is in the *Sleep Power State*, the PwrMgr continues to monitor power/status on the board. The PwrMgr exits the *Sleep Power State* (e.g. drives ***ENABLE*** low to restore 12 V switched power) when the power supply is within the *Power On Voltage* range and a qualified wakeup event is recognized, which includes:

- *WAKE/SLEEP* switch pressed (S5),
- cPHY network activity detected at *SP3*, or
- ECL activity (MOST Electrical Control Line Specification [8]) is detected (low-level is detected on ***PM_ECL/LIN*** from the *LIN/ECL* connector J202).

If one of the above wakeup events occurs during normal operation (not in the *Sleep Power State*), it is considered an interrupt event. The PwrMgr informs the EHC of an interrupt event by driving the ***PM_INT*** signal low (EHC RE8).

For EHC application code that supports power management, recognition of an interrupt event is likely to trigger a read of the MPM85000 *Initial Wake Event Register* (0Fh), which indicates the reason the Eval110 cPHY Board exited the *Sleep Power State*. Operation as either a *Power Master* or *Power Slave* determines how wakeup and interrupt events are handled by the application.

Note:	The EHC application code can disable PwrMgr detection of individual wakeup and interrupt events via register settings, as needed.

11.3 Other Circuitry

The Eval110 cPHY Board uses resistor installation options to control the default state of MPM85000 **WAKEHI** configuration pin. By default, R35 is present (R27 not installed) and the pin is set high. If R35 is removed and R27 is installed, the pin will be set low.

- If **WAKEHI** is sampled high at initial power-up, the board will not exit the *Sleep Power State* in the $U_{Critical}$ region.
- If **WAKEHI** is sampled low at initial power-up, the board will exit the *Sleep Power State* in $U_{Critical}$.

Refer to the MPM85000 Automotive Power Management Device Data Sheet [5] for more information on the MPM85000 *Allowed Wakeup Range* and using the **WAKEHI** pin to set the default state of the **CR.WAKECV** bit.

The ***PM_$\overline{RST}$*** reset signal (controlled by the PwrMgr **$\overline{RESET}$** output pin) is used to reset the entire Eval110 cPHY Board. This signal, as well as the *BOARD_RESET* switch (S9), force the ***PM_PWROFF*** signal low, which prevents the Eval110 cPHY Board from entering the *Sleep Power State* during the reset period.

11.4 Disabling Power Management

The Eval110 cPHY Board uses a hardware override mechanism to allow the power management circuitry to be disabled (via DIP Switch 6) during EHC programming or debugging.

When DIP switch 6 is *CLOSED*, all shutdown capabilities of the power management circuitry are overridden by clamping the ***PM_PWROFF*** signal to ground through D4. With power management disabled in this manner, the Eval110 cPHY Board is prevented from entering the *Sleep Power State*.

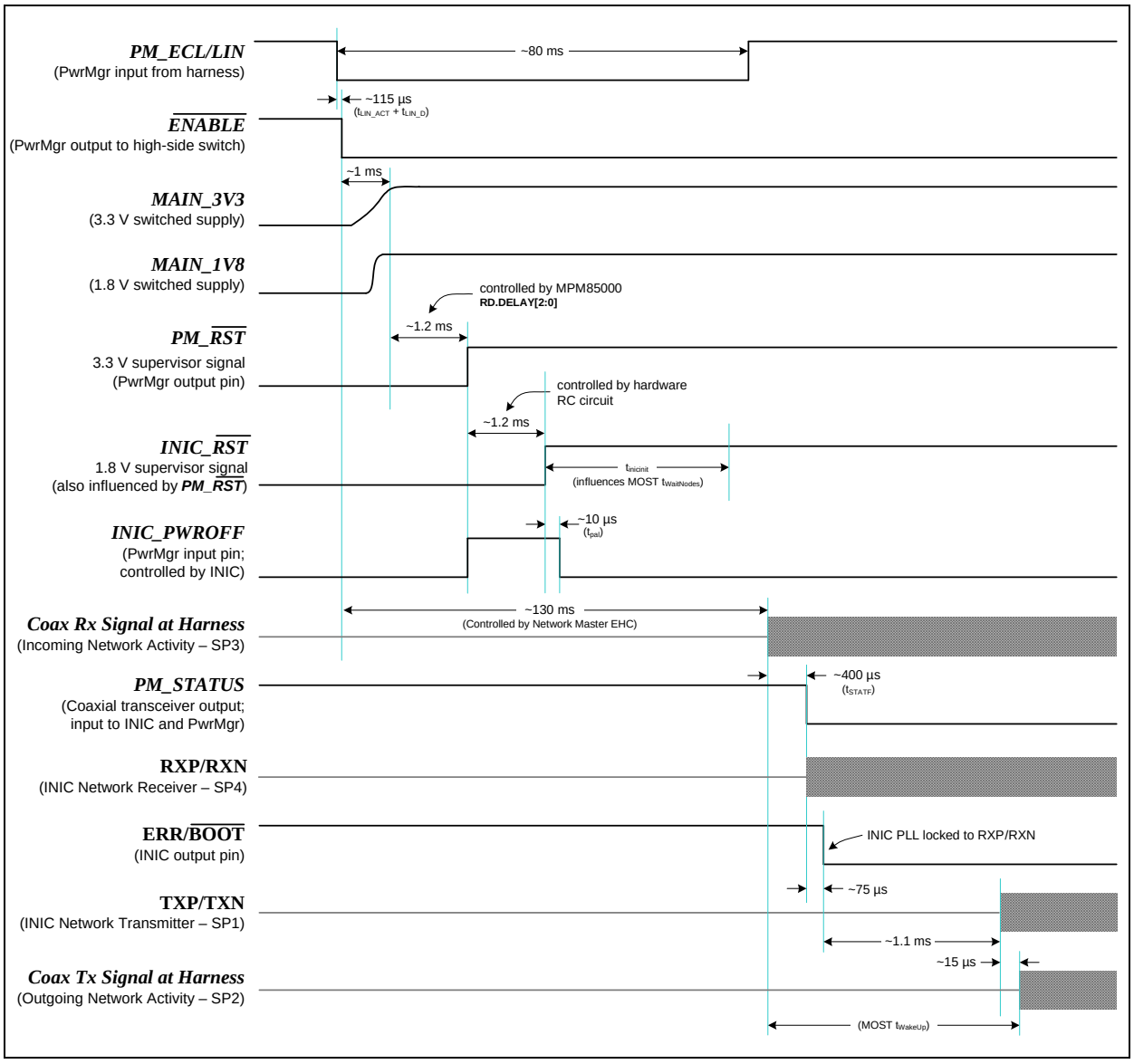
11.5 Typical Power Scenarios

When Eval110 cPHY Board power management is enabled, the following figures provide *typical* power-up and power-down sequencing of a timing-slave node from the *Sleep Power State*. These figures are *typical*, in that some variances may be observed with different EHC application code. These figures show Eval110 cPHY Board power scenarios when standard EHC application code (provided by Microchip) is used. Refer to the MOST ToGo Architecture and Implementation Guide [6] for more information on specific firmware implementations.

11.5.1 WAKEUP DUE TO ECL ACTIVITY

Figure 11-1 illustrates how the Eval110 cPHY Board (configured as a timing-slave) wakes from the *Sleep Power State* as a result of the ***PM_ECL/LIN*** line being pulled low via the *LIN/ECL* connector (J202). In this scenario, INIC (not the EHC) controls the PwrMgr **PWROFF** pin

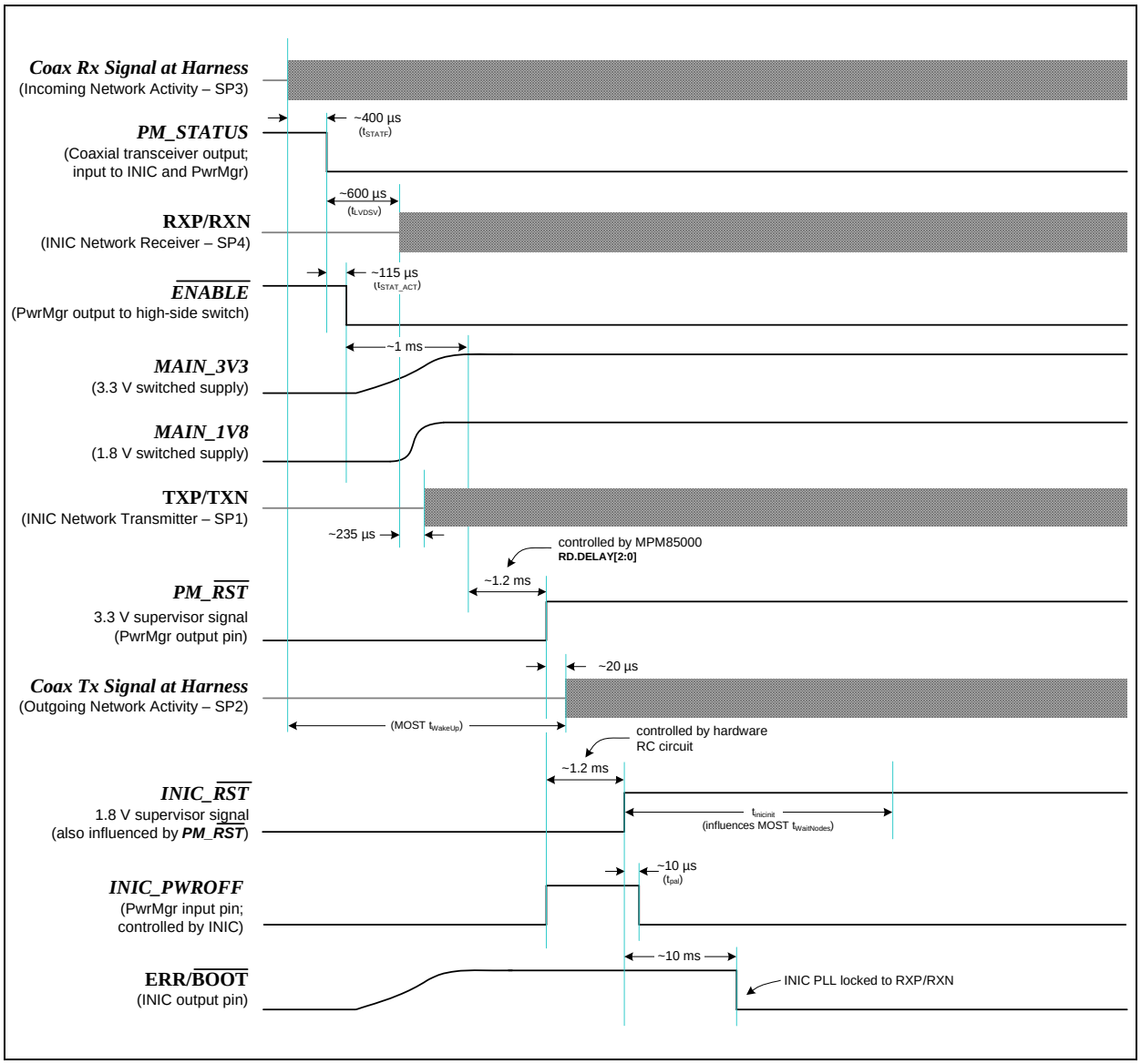
FIGURE 11-1: POWER SLAVE - WAKEUP DUE TO ECL ACTIVITY



11.5.2 WAKEUP DUE TO NETWORK ACTIVITY

Figure 11-2 illustrates how the Eval110 cPHY Board (configured as a timing-slave) wakes from the *Sleep Power State* as a result of MOST150 cPHY network activity. In this scenario, INIC (not the EHC) controls the PwrMgr **PWROFF** pin.

FIGURE 11-2: POWER SLAVE - WAKE DUE TO NETWORK ACTIVITY

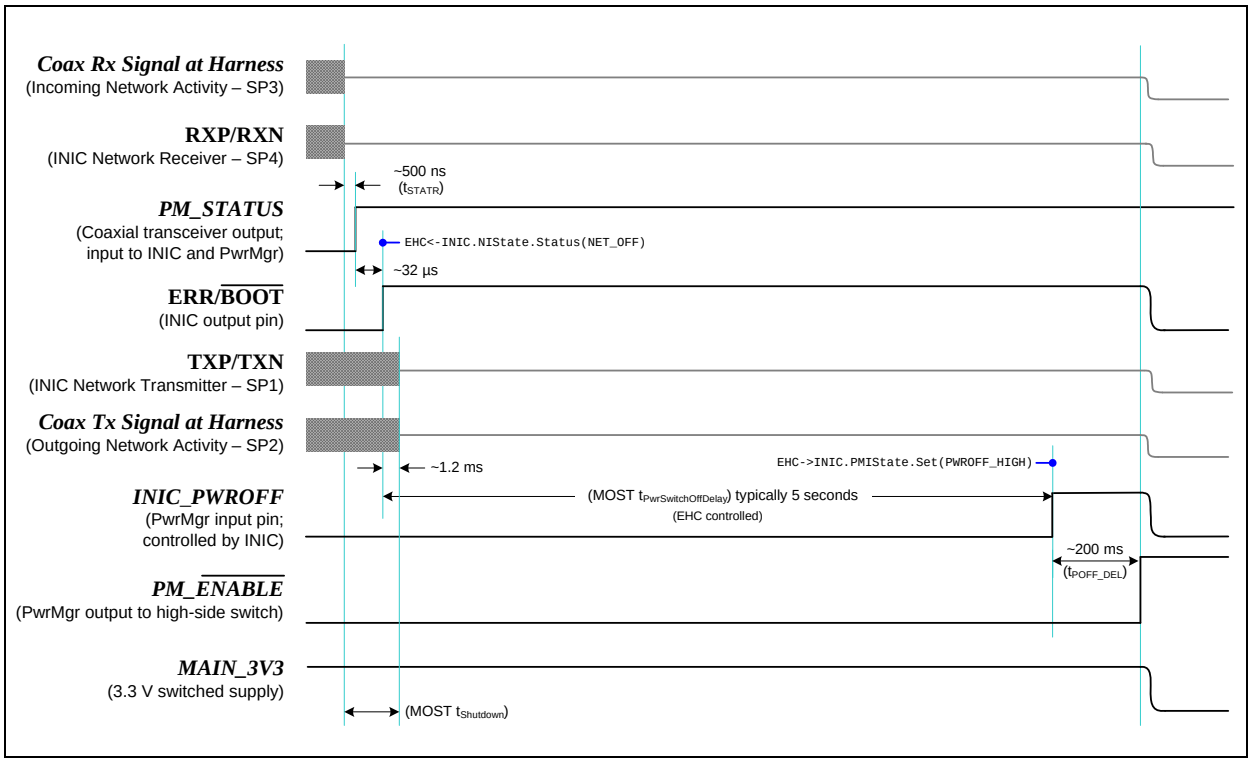


11.5.3 POWER DOWN

Figure 11-3 illustrates how the Eval110 cPHY Board (configured as a timing-slave) returns to the *Sleep Power State*. In this scenario, INIC controls the PwrMgr **PWROFF** pin; however, it does so based on commands received from the EHC. By sending `INIC.PMIState.Set(PWROFF_HIGH)`, the EHC can control when INIC releases **PWROFF**. This allows the EHC to keep the board from powering down (e.g. entering the *Sleep Power State*) until the application is ready.

Allowing INIC to control the PwrMgr **PWROFF** line, with the EHC managing INIC is a more robust architecture than allowing the EHC to manage the **PWROFF** line directly. Refer to the MOST INIC Hardware Concepts Technical Bulletin [10] for more information on this scenario.

FIGURE 11-3: POWER SLAVE - POWER DOWN SEQUENCE



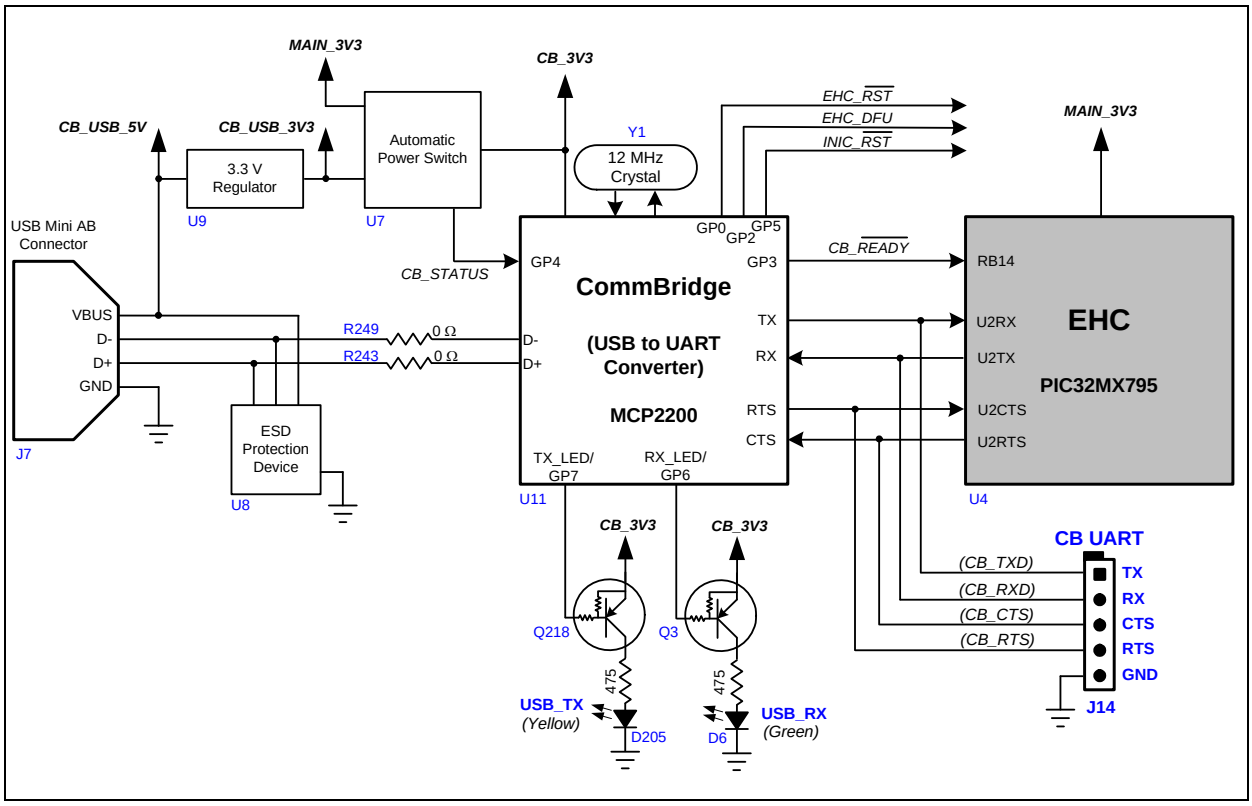
12.0 MCP2200 COMMBRIDGE

The Eval110 cPHY Board includes an integrated communications bridge (CommBridge) to facilitate application firmware updates and obtaining status and debug information from the EHC application. The CommBridge is used to interface the board to a PC while preserving the USB port of the EHC for use as a mass storage device.

The CommBridge device (U11) itself is a MCP2200 Microchip USB to UART Serial Converter, which enables USB connectivity in applications that have a UART interface. The device runs from 3.3 V power (*CB_3V3*) which can be derived from the USB VBUS or from the main 3.3 V supply (*MAIN_3V3*). The main internal clock is derived from the 12 MHz external crystal (Y1). The MCP2200 also has some GPIO pins and an internal EEPROM that can be accessed from PC applications across the USB interface. The MCP2200 implements a composite USB device with a CDC class device to carry the UART traffic, and a HID device to access the EEPROM and I/O pins. The CDC class means that on the PC side, the EHC UART traffic appears as a simple serial port. See the MCP2200 USB 2.0 to UART Protocol Converter with GPIO Data Sheet [29] for full details

An overview of the Eval110 cPHY Board CommBridge is shown in Figure 12-1.

FIGURE 12-1: COMMBRIDGE OVERVIEW



The Eval110 cPHY Board implements an automatic power switch (U7) to control the CommBridge power source. If the board is connected to a PC with a USB cable via J7, the CommBridge always runs from the external USB power (even when the board is in the *Sleep Power State*). If the external supply is removed, the CommBridge automatically switches over to the *MAIN_3V3* supply. The ***CB_STATUS*** signal conveys the state of the power switch to the CommBridge.

Since the CommBridge remains powered while the rest of the application is in the *Sleep Power State*, it must not be driving any of its GPIOs if power is removed from the EHC to avoid inadvertent currents across power domains. To accomplish this, the ***CB_STATUS*** signal from the power switch goes to a CommBridge GPIO which can be checked by a PC application before driving any of the I/O pins that go to the EHC.

The CommBridge USART2 interface is connected to the EHC. The CommBridge sends data using the ***CB_TXD*** signal. The EHC transmits debug print information to the CommBridge (for transmission to the PC over USB) using the ***CB_RXD*** signal.

The CommBridge is also capable of loading application code images into EHC flash memory. Refer to Section 9.3.1 "Flashing from PC via USB" for more information.

12.1 CommBridge GPIO Reference

Table 12-1 provides a list of all CommBridge GPIO connections on the Eval110 cPHY Board. As mentioned, the PC application should not configure any of the GPIO outputs until it is verified that the *MAIN_3V3* power is on by checking ***CB_STATUS*** and/or *MAIN_3V3* inputs.

TABLE 12-1: COMMBRIDGE GPIO REFERENCE

Pin Name	Pin #	Net Name	Description / Notes	Component
MCP2200 CommBridge (U11) GPIO (s23)				
GP0/SSPND	13	***EHC_$\overline{RST}$***	GPIO output the PC application can reset the EHC. Note: the SSPND functionality is not used or enabled.	U11
GP1/USBCFG	12	***MAIN_3V3***	GPIO input the PC application can check for main 3.3 V power. Note: the USBCFG functionality is not used or enabled.	U11
GP2	11	***EHC_DFU***	GPIO output used by the PC application to put the EHC into bootloader mode for programming.	U11
GP3	6	***CB_$\overline{READY}$***	Not used - should be left unconfigured	U11
GP4	5	***CB_STATUS***	GPIO input used by the PC application to check if the CommBridge is powered by USB bus power or by *MAIN_3V3*.	U11
GP5	4	***INIC_$\overline{RST}$***	GPIO output the PC application can use to hold INIC in reset during a firmware update.	U11
GP6/RXLED	3	***CB_USB_RXLED***	The RXLED functionality is enabled. This pin drives the green USB RX LED D6	U11
GP7/TXLED	2	***CB_USB_TXLED***	The TXLED functionality is enabled. This pin drives the yellow USB TX LED D205	U11

APPENDIX A: OPERATING CONDITIONS

Values specified below assume Fs = 48 kHz and PwrMgr default register values, unless otherwise noted. Voltages specified below are measured on the board edge at *VBATT* (TP2) and do not consider losses found in power supply cabling. Values in this table are typical and measured at room temperature.

TABLE A-1: OPERATING SPECIFICATIONS

Description	Min	Typ	Max	Units	Conditions
Power Connector (J6)					
Continuous Operating Range [1] [2] [3]	6.72	14.14	26.00	V	
Power On Voltage [3]	9.15 6.65			V V	R27 removed; R35 installed (default) R27 installed; R35 removed
Power Consumption		3.00		W	
Normal Operating Current [4]		212		mA	*VBATT* = 14.14 V; *VPRO* = 13.5 V
Sleep Power State Current		56		µA	*VBATT* = 13.65 V; *VPRO* = 13.5 V
Voltage Drop due to Load Dump Circuitry [5]		0.64 0.15		V V	Normal Operation Sleep Power State
Audio Input Jack (J2)					
CODEC Full-Scale Input			2.00	V_{RMS}	
Audio Output Jack (J3)					
CODEC Full-Scale Output		0.75		V_{RMS}	R_L = 16 Ω
Miscellaneous					
Ambient Temperature	0		70	°C	

Note 1: Operation at DC voltages above the maximum value will result in increased power consumption due to various protection diodes turning on.

2: The *Continuous Operating Range* does not consider over-voltage transients and under-voltage dropouts that may occur in automotive environments. The Eval110 cPHY Board contains typical load-dump circuitry designed to pass *Test Level IV (max.)* for all transient pulses defined for 12 V automotive systems in the *ISO 7637-2:2004* [30] test specification.

3: With typical EHC application code, if the operating voltage falls below 6.72 V after initial power-up, the Eval110 cPHY Board enters the *Sleep Power State* when power management is enabled. If power management is disabled, the *Sleep Power State* is not supported. While in the *Sleep Power State*, the operating voltage must rise above the minimum *Power On Voltage* before the Eval110 cPHY Board will exit the *Sleep Power State* in response to a permitted wakeup event.

4: The *Normal Operating Current* specification is based on an Eval110 cPHY Board *Standard Application*, as defined in Section 1.2.1 "Standard Application". The board is a MOST Network timing-master configured for audio sourcing/sinking using standard EHC application code.

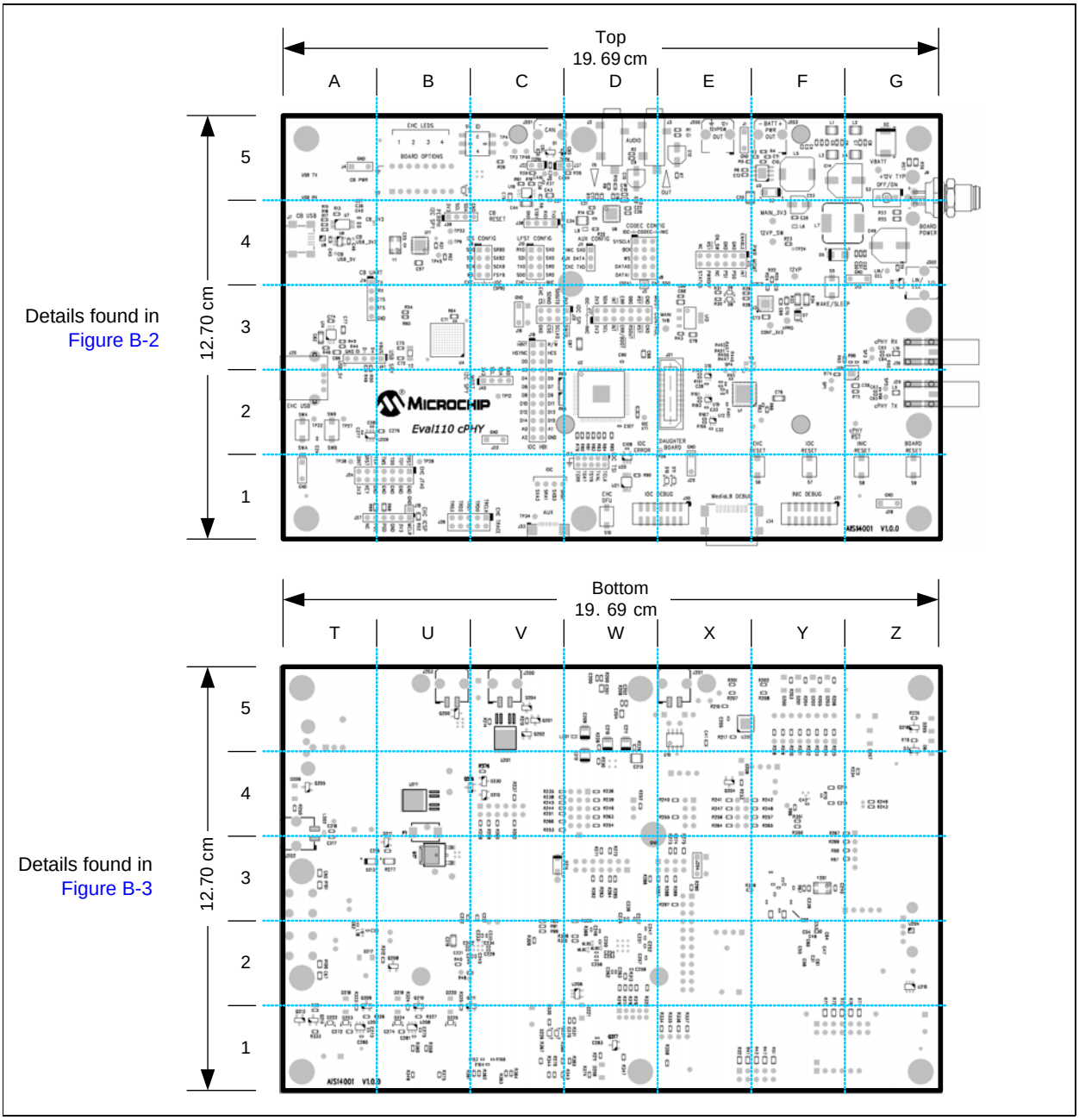
5: Voltage thresholds used to control board power-up and power-down are measured at the PwrMgr (*VPRO*). Therefore, when considering programmable PwrMgr threshold values, the user must take $V_{LoadDump}$ into consideration, which is defined as the difference between *VPRO* and *VBATT* due to various series components.

APPENDIX B: PCB DETAILS

The board layout plots utilize a grid system for locating components, jumpers and test points on the board. As illustrated in Figure B-1, the top grid column begins the alphabet on the long edge of the board, and the bottom grid column stops at the end of the alphabet. This allows user to immediately determine which side of the board a particular jumper or component is located.

Refer to Appendix E: "Layout Plots" and Appendix D: "Schematics" for detailed information

FIGURE B-1: BOARD DIMENSIONS AND GRID



Throughout this document, the following conventions are used to help locate components on the board:

- 1-5 are used on both sides of the board as the vertical locator,
- A-G are used as the top side horizontal locator, and
- T-Z are used as the bottom side horizontal locator.

FIGURE B-2: ASSEMBLY DRAWING TOP

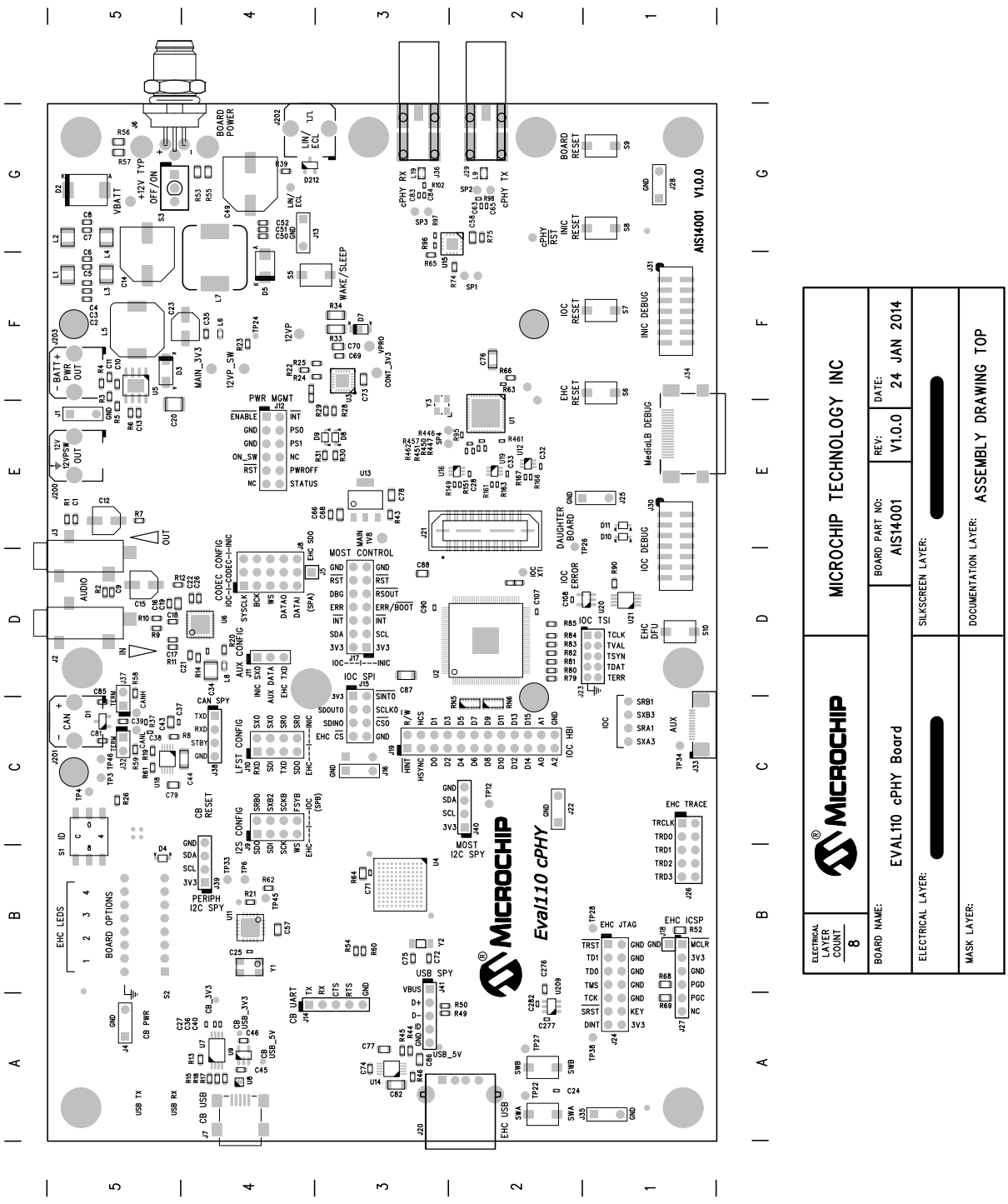
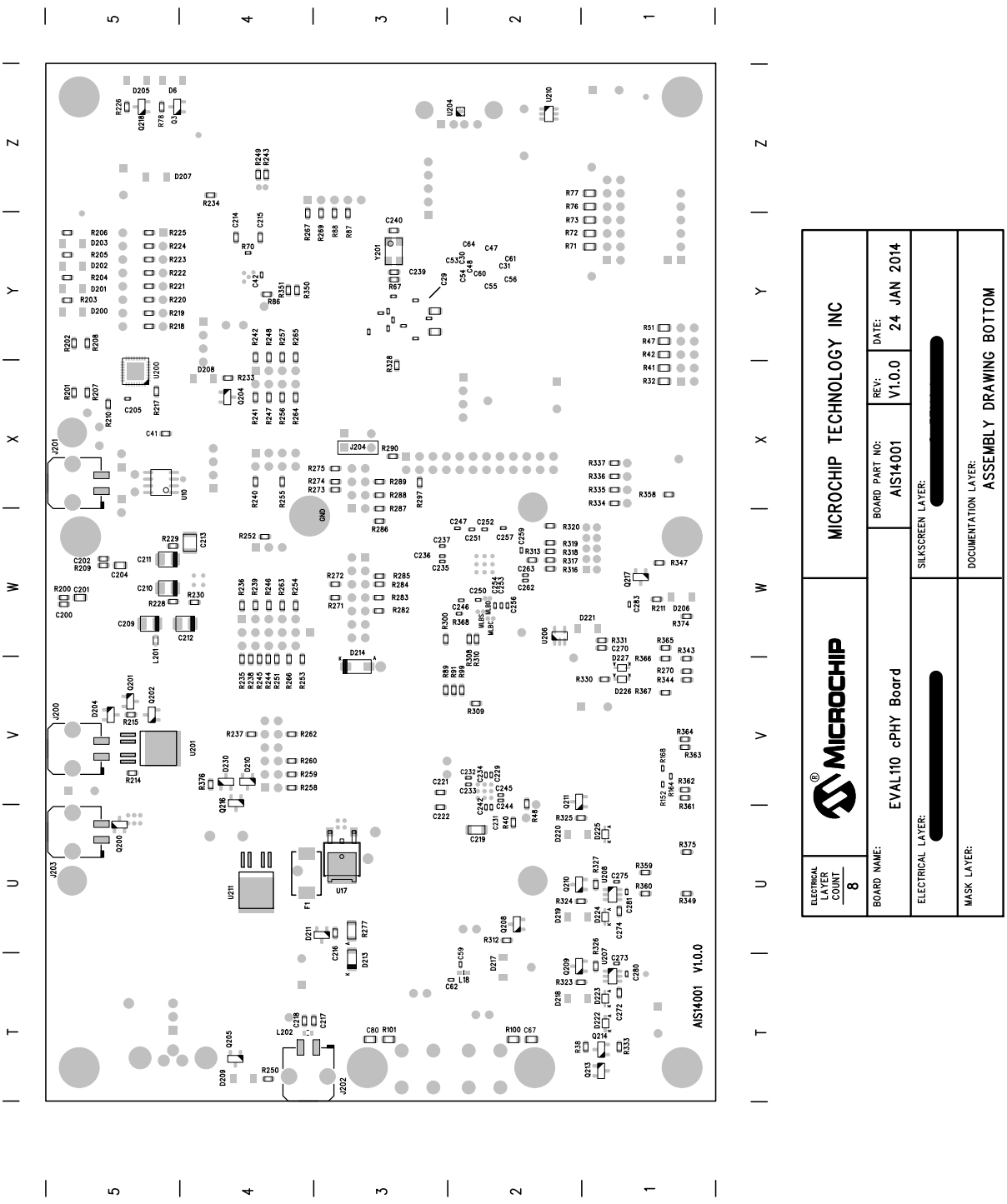


FIGURE B-3: ASSEMBLY DRAWING BOTTOM



APPENDIX C: COMPONENT PLACEMENT

C.1 Connectors, Headers, Jumpers, Switches & Test Points

Table C-1 provides assistance in locating connectors, headers, jumpers, switches, and test points on the Eval110 cPHY Board.

Jumper and Test Point component types are defined as follows:

- C - *Connector/Jack*
  Allows for specific connection by a mating device on external tool, equipment, or cable.
- H - *Header*
  Allows connections via fly-wires and accommodates connections to oscilloscope, logic analyzer, or multimeter.
- J - *Jumper*
  Uses shorting jumpers (shunts) to make connections. Uses 0.1 " spacing, unless noted otherwise.
- SW - *Switch*
  User-controllable mechanical switch (e.g. DIP, push-button).
- TP - *Test Point*
  Allows connection to oscilloscope or multimeter. Can be differential, wire-loop or through-hole.

TABLE C-1: CONNECTORS, HEADERS, JUMPERS, SWITCHES, & TEST POINTS

Type	Ref Des	Silkscreen	Description	Sheet # *	Board Location †
TP	DP1	SP1	Differential Test Point for INIC **TXP** and **TXN** (LVDS)	s5	2F
TP	DP2	SP2	Test Point for cPHY CTO signal and reference	s5	2G
TP	DP3	SP3	Test Point for cPHY CRI signal and reference	s5	3G
TP	DP4	SP4	Differential Test Point for INIC **RXP** and **RXN** (LVDS)	s5	2E-3E
TP	J1	GND	Ground Loop	s25	5E
C	J2	AUDIO IN	CODEC Line In Jack (3.5 mm, light blue)	s16	5D
C	J3	AUDIO OUT	CODEC Headphone Jack (3.5 mm, lime green)	s16	5D-5E
TP	J4	GND	Ground Loop	s25	5A
J	J5	EHC SDO	Serial Streaming Data from EHC	s17	3D-4D
C	J6	BOARD POWER	Main Power Connector (Binder 09-3419-82-03)	s1	4G-5G
C	J7	CB USB	CommBridge USB Connector (USB Mini-AB Connector)	s23	4A
J	J8	CODEC CONFIG	CODEC Configuration Header	s17	4D
J	J9	I2S CONFIG	EHC I^2S Configuration Header	s17	4C
J	J10	LFST CONFIG	LFST Configuration Header	s17	4C
J	J11	AUX CONFIG	AUX Configuration Header	s17	4D
H	J12	PWR MGMT	Power Management Header	s3	4E
TP	J13	GND	Ground Loop	s25	4G
H	J14	CB UART	CommBridge UART Header (NO POP)	s23	3A-4A
H	J15	IOC SPI	IOC SPI Header	s10	3C-3D
TP	J16	GND	Ground Loop	s25	3C
H	J17	MOST CONTROL	MOST Control Header	s13	3D
J	J18	GND	Ground Test Point to hold EHC in reset with J27	s18	1B
H	J19	IOC HBI	IOC HBI Header	s11	2C-3C
C	J20	EHC USB	EHC USB Connector (USB Type A Receptacle)	s20	2A-3A
C	J21	DAUGHTER BOARD	High-Speed Connector for attaching secondary application PCB (QSH-020-01-L-D-DP-A)	s15	2D-3E
TP	J22	GND	Ground Loop	s25	2C

* Sheet # corresponds to schematic sheet pages shown in Figure D-1 through Figure D-25.

† The board location refers to the grid coordinate system shown in Figure B-2 and Figure B-3.

TABLE C-1: CONNECTORS, HEADERS, JUMPERS, SWITCHES, & TEST POINTS (CONTINUED)

Type	Ref Des	Silkscreen	Description	Sheet # *	Board Location †
C	J23	IOC TSI	IOC TSI Connector (5x2 position, 2mm pitch)	s10	1D
H	J24	EHC JTAG	EHC JTAG Debug and Programming Port (keyed)	s18	1A-1B
TP	J25	GND	Ground Loop	s25	1E-2E
H	J26	EHC TRACE	EHC Instruction Trace Header	s18	1B-1C
H	J27	EHC ICSP	EHC Programming and Debug ICSP Header	s18	1A-1B
TP	J28	GND	Ground Loop	s25	1G
C	J29	cPHY TX	MOST150 Coaxial Transmit Jack (59S20X-40ML5-Y, universal fit, SMB)	s5	2G
C	J30	IOC DEBUG	IOC Debug Header (7x2 position, 2mm pitch, shrouded)	s14	1D-1E
C	J31	INIC DEB UG	INIC Debug Header (7x2 position, 2mm pitch, shrouded)	s14	1F
J	J32	TERM CANL	Terminates CANL line, when shunted	s6	5C
C	J33	AUX	AUX Connector (Wuerth 68711214522)	s15	1C
C	J34	MEDIALB DEBUG	MediaLB Debug Connector (Samtec HDMI HDMR-19-02-S-SM)	s12	1E-1F
TP	J35	GND	Ground Loop	s25	1A
C	J36	cPHY RX	MOST150 Coaxial Receive Jack (Rosenberger SMB, universal fit, 59S20X-40ML5-Y)	s5	3G
J	J37	TERM CANH	Terminates CANH line, when shunted	s6	5C-5D
H	J38	CAN SPY	EHC CAN Interface Header (NO POP)	s6	4C
H	J39	PERIPH I2C SPY	EHC Peripheral I2C Bus Header (NO POP)	s19	4B-4C
H	J40	MOST I2C SPY	EHC MOST I2C Bus Header (NO POP)	s19	2C
H	J41	USB SPY	EHC USB Header (NO POP)	s20	3A-3B
C	J200	12VPSW OUT	12 V Switched Remote Power Connector (Molex 43650-0209)	s24	5V
C	J201	CAN	CAN Connector (Molex 43650-0209)	s24	5X
C	J202	LIN/ECL	LIN/ECL Connector (Molex 43650-0209)	s24	3T-4T
C	J203	BATT PWR OUT	12 V Continuous Remote Power Connector (Molex 43650-0209)	s24	5U
TP	J204	GND	Ground Loop	s25	3X
SW	S1	ID	16-position Rotary Switch	s21	5B-5C
SW	S2	BOARD OPTIONS	8-position DIP Switch	s21	5B
SW	S3	OFF/ON	Toggle Switch for Main Board Power	s1	5G
SW	S5	WAKE/SLEEP	Push-Button Switch for PwrMgr **ON_SW** pin; controls board power-up/power-down.	s3	3F-4F
SW	S6	EHC RESET	Push-Button Switch for EHC Reset	s4	1F
SW	S7	IOC RESET	Push-Button Switch for IOC Reset	s4	1F
SW	S8	INIC RESET	Push-Button Switch for INIC Reset	s4	1G
SW	S9	BOARD RESET	Push-Button Switch for Board Reset	s4	1G
SW	S10	EHC DFU	Push-Button Switch to EHC DFU Enable	s20	1D
SW	SWA	SWA	General Purpose EHC Push-Button Switch (with hardware debounce device)	s20	2A
SW	SWB	SWB	General Purpose EHC Push-Button Switch (with hardware debounce device)	s20	2A

* Sheet # corresponds to schematic sheet pages shown in Figure D-1 through Figure D-25.

† The board location refers to the grid coordinate system shown in Figure B-2 and Figure B-3.

TABLE C-1: CONNECTORS, HEADERS, JUMPERS, SWITCHES, & TEST POINTS (CONTINUED)

Type	Ref Des	Silkscreen	Description	Sheet # *	Board Location †
TP	TP1	CANH	CANH Signal (at CAN Harness)	s24	5C
TP	TP2	VBATT	Battery Voltage (at Power Connector / Board Edge)	s1	5G
TP	TP3		Unused I/O Expander Pin P2.6	s21	5C
TP	TP4		Unused I/O Expander Pin P2.1	s21	5C
TP	TP5	CB_3V3	CommBridge 3.3 V Supply (output from power switch)	s22	4A
TP	TP6		CommBridge USB Tx LED	s23	4B
TP	TP7	12VP	Continuous 12 V Power (Protected and Filtered)	s1	4F
TP	TP8	MAIN_3V3	Main Board 3.3 V Switched Power Supply	s2	4F
TP	TP9	CB USB_3V3	CommBridge USB Bus Power Regulated 3.3 V Supply	s22	4A
TP	TP10	CB USB_5V	CommBridge USB 5 V Bus Power	s23	4A
TP	TP11	CONT_3V3	PwrMgr Continuous 3.3 V Micropower Supply	s3	4F
TP	TP12		EHC DFU Enable Signal	s20	2C
TP	TP13	LIN/ECL	LIN/ECL Signal (at LIN/ECL harness)	s24	4G
TP	TP14	VPRO	PwrMgr **VPRO** pin (for input power monitoring)	s3	3F
TP	TP15	MAIN 1V8	Main Board 1.8 V Switched Power Supply	s2	3E
TP	TP16		INIC **SRX3** Pin (unused)	s8	2E
TP	TP17		INIC **SRX1** Pin (unused)	s8	2F
TP	TP18		CommBridge USB D- Signal	s23	4Z
TP	TP19		CAN Transceiver 5 V Power Supply	s6	5X
TP	TP20	CANL	CANL Signal (at CAN harness)	s24	5C
TP	TP21	USB_5V	EHC USB 5 V Bus Power	s20	3A
TP	TP22	SWA	Debounced Output of EHC Push-Button Switch, SWA	s20	2A
TP	TP23	IOC XTI	IOC **XTI** Pin	s9	2D
TP	TP24		Status Signal for Main Power High-Side Switch	s1	4F
TP	TP25	12VP_SW	Switched 12 V Power (Protected and Filtered)	s1	4F
TP	TP26		Unused Signal for *DAUGHTER BOARD* Connector (J21)	s15	2D-2E
TP	TP27	SWB	Debounced Output of EHC Push-Button Switch, SWB	s20	2A
TP	TP28		Unused $\overline{\text{TRST}}$ Signal on EHC JTAG Header (J24)	s18	1B
TP	TP29	IOC SXA3	IOC Streaming Port A **SXA3** Pin (unused)	s10	1C
TP	TP30	IOC SRA1	IOC Streaming Port A **SRA1** Pin (unused)	s10	1C
TP	TP31	IOC SXB3	IOC Streaming Port B **SXB3** Pin (unused)	s10	1C
TP	TP32	IOC SRB1	IOC Streaming Port B **SRB1** Pin (unused)	s10	1C
TP	TP33		CommBridge USB Rx LED	s23	4B
TP	TP34		Unused Signal for *AUX* Connector (J33)	s15	1C
TP	TP35	MLBC	MediaLB 6-pin Interface Clock (Positive Differential)	s12	2W
TP	TP36	MLBC	MediaLB 6-pin Interface Clock (Negative Differential)	s12	2W
TP	TP37	MLBD	MediaLB 6-pin Interface Data (Positive Differential)	s12	2W
TP	TP38		Unused DINT Signal on EHC JTAG Header (J24)	s18	1A
TP	TP39	MLBD	MediaLB 6-pin Interface Data (Negative Differential)	s12	2W
TP	TP40	MLBS	MediaLB 6-pin Interface Signal (Positive Differential)	s12	2W
TP	TP41	MLBS	MediaLB 6-pin Interface Signal (Negative Differential)	s12	2W
TP	TP42		CommBridge USB D+ Signal	s23	4Z
TP	TP43		CommBridge Power Automatic Switch Status Signal	s22	4Z

* Sheet # corresponds to schematic sheet pages shown in Figure D-1 through Figure D-25.

† The board location refers to the grid coordinate system shown in Figure B-2 and Figure B-3.

TABLE C-1: CONNECTORS, HEADERS, JUMPERS, SWITCHES, & TEST POINTS (CONTINUED)

Type	Ref Des	Silkscreen	Description	Sheet # *	Board Location †
TP	TP44		CommBridge GP3 Signal	s23	4B
TP	TP45		CommBridge Reset Input Signal	s22	4B
TP	TP46		Unused I/O Expander Pin P2.2	s21	5C
TP	TP47	cPHY $\overline{\text{RST}}$	cPHY Transceiver $\overline{\text{RST}}$ Pin	s5	2G

* Sheet # corresponds to schematic sheet pages shown in Figure D-1 through Figure D-25.

† The board location refers to the grid coordinate system shown in Figure B-2 and Figure B-3.

C.2 Discrete Components

Table C-2 provides assistance in locating integrated circuits, diodes, resistors and crystals on the Eval110 cPHY Board.

> **Note:** The following table only references circuit components mentioned within this User's Guide. All components are listed within the schematic files shown in Figure D-1 through Figure D-25 and on the board assembly drawings Figure B-2 and Figure B-3.

Circuit component types are defined as follows:

- D - *Diodes*
- R - *Resistors*
- U - *Integrated Circuit Devices*
- Y - *Crystals*

TABLE C-2: DISCRETE COMPONENTS

Type	Ref Des	Description	Sheet # *	Board Location †
D	D4	Schottky Diode - DIP SW6 Control of ***PM_PWROFF***	s21	5B
D	D6	LED - Green - USB Rx	s23	5A
D	D10	Schottky Diode - Connects INIC $\overline{\text{RSOUT}}$ to ***EHC_$\overline{\text{RST}}$***	s8	1E
D	D11	Schottky Diode - Connect $\overline{\text{RSOUT}}$ to ***IOC_$\overline{\text{RST}}$***	s8	1E
D	D200	LED - Red - Application LED 4	s25	5Y
D	D201	LED - Orange - Application LED 3	s25	5Y
D	D202	LED - Yellow - Application LED 2	s25	5Y
D	D203	LED - Green - Application LED 1	s25	5Y
D	D205	LED - Yellow - USB Tx	s23	5A
D	D206	LED - Orange - EHC - Firmware Update	s25	1W
D	D207	LED - Red - CommBridge Power	s25	5Z
D	D209	LED - Red - Board Power	s25	4T
D	D217	LED - Green - Network Lock	s25	2T
D	D218	LED - Yellow - INIC Reset	s25	2T
D	D219	LED - Yellow - IOC Reset	s25	2U
D	D220	LED - Yellow - EHC Reset	s25	2U
D	D221	LED - Orange - IOC Error	s25	1W
D	D223	Schottky Diode - Gang INIC Reset with Board Reset	s4	1T
D	D224	Schottky Diode - Gang IOC Reset with Board Reset	s4	1U
D	D225	Schottky Diode - Gang EHC Reset with Board Reset	s4	1U
D	D227	Schottky Diode - Gang EHC Reset with Daughter Card Reset (NO POP)	s15	1V
R	R27	0 Ω Resistor - PwrMgr WAKEHI pull-down (NO POP)	s3	4F
R	R35	0 Ω Resistor - PwrMgr WAKEHI pull-up	s3	4F
R	R270	15 kΩ Resistor - IOC default to I^2C Mode (NO POP)	s11	1V
R	R284	15 kΩ Resistor - INIC MediaLB at Power-Up (NO POP)	s13	3W
R	R285	15 kΩ Resistor - INIC I^2C at Power Up	s13	3W
R	R309	0 Ω Resistor - Daughter Board Reset	s15	2V
R	R344	15 kΩ Resistor - IOC Default to JTAG Mode	s11	1X
U	U1	OS81110 INIC	s5, s7, s8, s12, s13, s14	2E-3E
U	U2	OS85650 IOC	s9, s10, s11, s12, s13, s14	2D-3D

* Sheet # corresponds to schematic sheet pages shown in Figure D-1 through Figure D-25.

† The board location refers to the grid coordinate system shown in Figure B-2 and Figure B-3.

TABLE C-2: DISCRETE COMPONENTS (CONTINUED)

Type	Ref Des	Description	Sheet # *	Board Location †
U	U3	MPM85000 PwrMgr	s3	3F
U	U4	PIC32MX795 EHC	s19	3B
U	U6	UDA1380 Audio CODEC	s18, s19, s20	4D
U	U7	TPS2112 Auto Switching Power Mux	s22	4A
U	U10	MCP2562 CAN Transceiver	s6	5X
U	U11	MCP2200 USB-to-UART Converter (CommBridge)	s22	4B
U	U14	MAX5008 USB Charge Pump for 5 V USB Power	s20	3A
U	U15	OS82150 cPHY Transceiver	s5	2G-3G
U	U18	MAX5008 USB Charge Pump for 5 V CAN Power	s6	5C
U	U21	PCA9517 I2C Repeater	s14	1D
U	U200	TCA6424 I/O Expander	s21	5X
U	U201	VN750 High Side Switch	s24	5V
U	U207	TPS3808 Voltage Supervisor	s4	1T
U	U208	TPS3808 Voltage Supervisor	s4	1U
U	U210	MAX6817 Dual Switch Debouncer	s20	2Z
Y	Y1	12 MHz Crystal - CommBridge Oscillator	s22	4B
Y	Y2	32.768 kHz Crystal Tuning Fork - EHC Secondary Oscillator	s18	3B
Y	Y3	18.432 MHz Crystal - INIC Oscillator	s7	3E
Y	Y201	12 MHz Crystal - EHC Primary Oscillator	s18	3Y

* Sheet # corresponds to schematic sheet pages shown in Figure D-1 through Figure D-25.

† The board location refers to the grid coordinate system shown in Figure B-2 and Figure B-3.

APPENDIX D: SCHEMATICS

The following pages contain the schematic design files for the Eval110 cPHY Board (AIS14001 V1.0.0). Throughout this document, a schematic page is referred to as page sn, where 's' is a literal indicating a schematic page and 'n' is the schematic page number. The following table outlines the major circuitry on each page.

TABLE D-1: SCHEMATIC SHEET LIST

Schematic Page	Sheet Name	Description	User's Guide Page
s1	PWR_MAIN	Main power input and filtering. Main high-side switch.	61
s2	PWR_REGULATORS	3.3 V switching regulator and 1.8 V linear regulator.	62
s3	PWR_MGMT	MPM85000 power management device (PwrMgr).	63
s4	BOARD_RESET	Board reset circuitry.	64
s5	MOST_NTWK	OS82150 MOST150 coaxial transceiver and front-end circuitry.	65
s6	CAN_LIN/ECL	CAN transceiver and LIN/ECL protection/filtering.	66
s7	INIC_PWR_XTAL	OS81110 INIC power pins and crystal oscillator.	67
s8	INIC_MISC	OS81110 INIC miscellaneous signals.	68
s9	IOC_PWR_XTAL	OS85650 IOC power pins and clock input.	69
s10	IOC_TSI_SPI_SP	OS85650 IOC TSI Port, SPI Port, and Streaming Ports.	70
s11	IOC_HBI_MISC	OS85650 IOC HBI Port and miscellaneous signals.	71
s12	MLB_6PIN	MediaLB 6-pin interface and debug circuitry.	72
s13	MOST_CTRL_PORT	OS81110 INIC Control Port and OS85650 IOC Control Port.	73
s14	MOST_DEBUG_PORT	OS81110 INIC Debug Port and OS85650 IOC Debug Port.	74
s15	DAUGHTER_BOARD	Daughter Board connector and Auxiliary connector.	75
s16	AUDIO_CODEC	Stereo audio CODEC device and audio jacks.	76
s17	I2S/LFST_CONFIG	Configuration jumpers for streaming audio and low frequency signal tunneling.	77
s18	EHC_PWR_XTAL	PIC32MX795 EHC power pins, crystals, and debug headers.	78
s19	EHC_PORTS	PIC32MX795 EHC signal ports.	79
s20	EHC_USB	PIC32MX795 EHC USB port and miscellaneous switches.	80
s21	I/O_EXPANDER	Configuration switches and port expander device for EHC.	81
s22	COMM_BRIDGE	USB-to-UART bridge device power supply and clock source.	82
s23	COMM_BRIDGE_I/O	USB-to-UART bridge interface signals.	83
s24	CABLE_HARNESS	Board harness connectors for power, CAN, and LIN/ECL.	84
s25	BOARD_MISC	Board LEDs, standoffs, mounting hardware, and fiducials.	85

Note: Schematics are provided "as is" without any warranty as an example implementation, and are not guaranteed to be suitable for any particular application. Any design using this information should be tested over the full environmental stress conditions of the intended application.

FIGURE D-1: SHEET 1 - PWR_MAIN

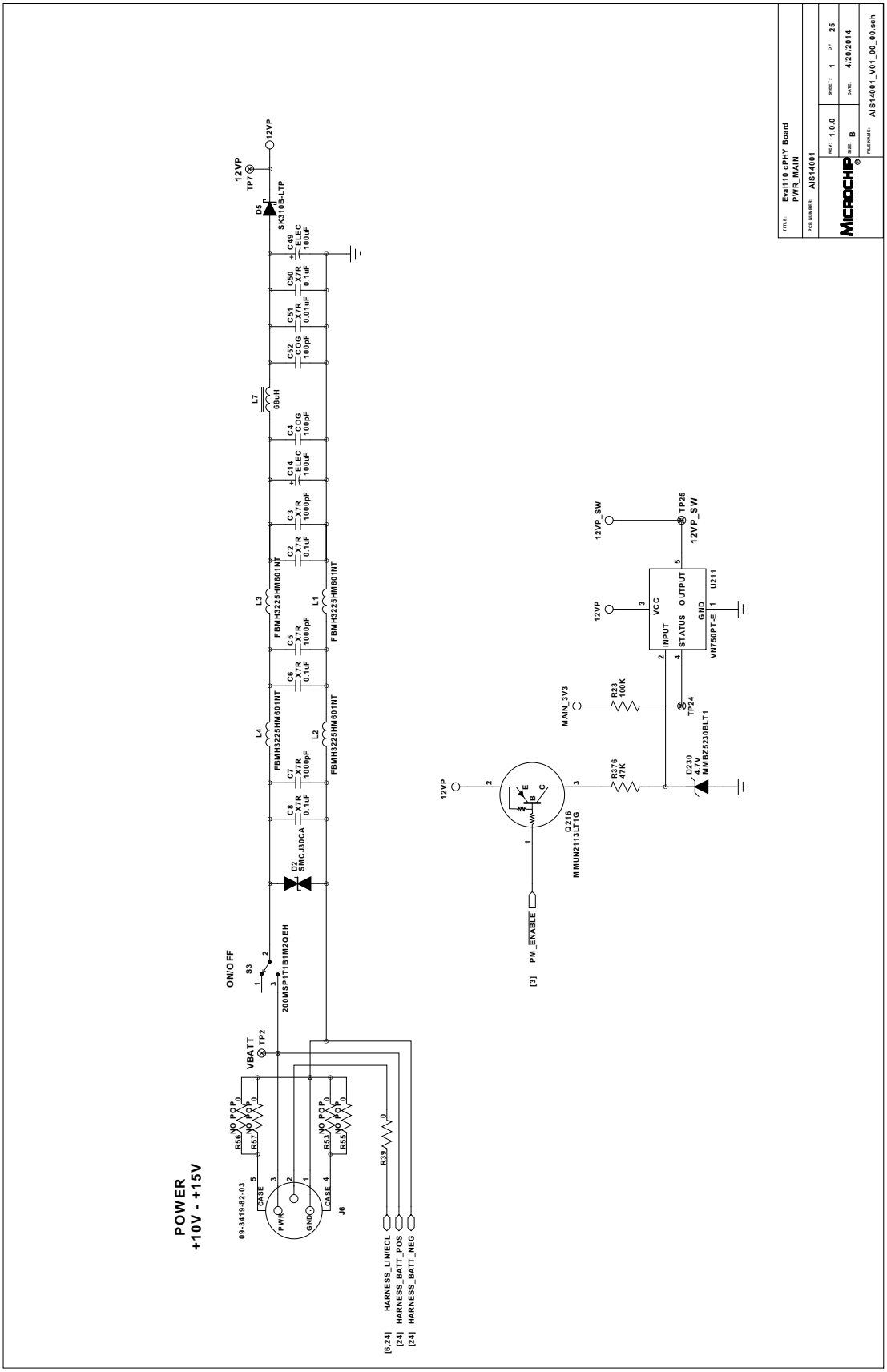


FIGURE D-2: SHEET 2 - PWR_REGULATORS

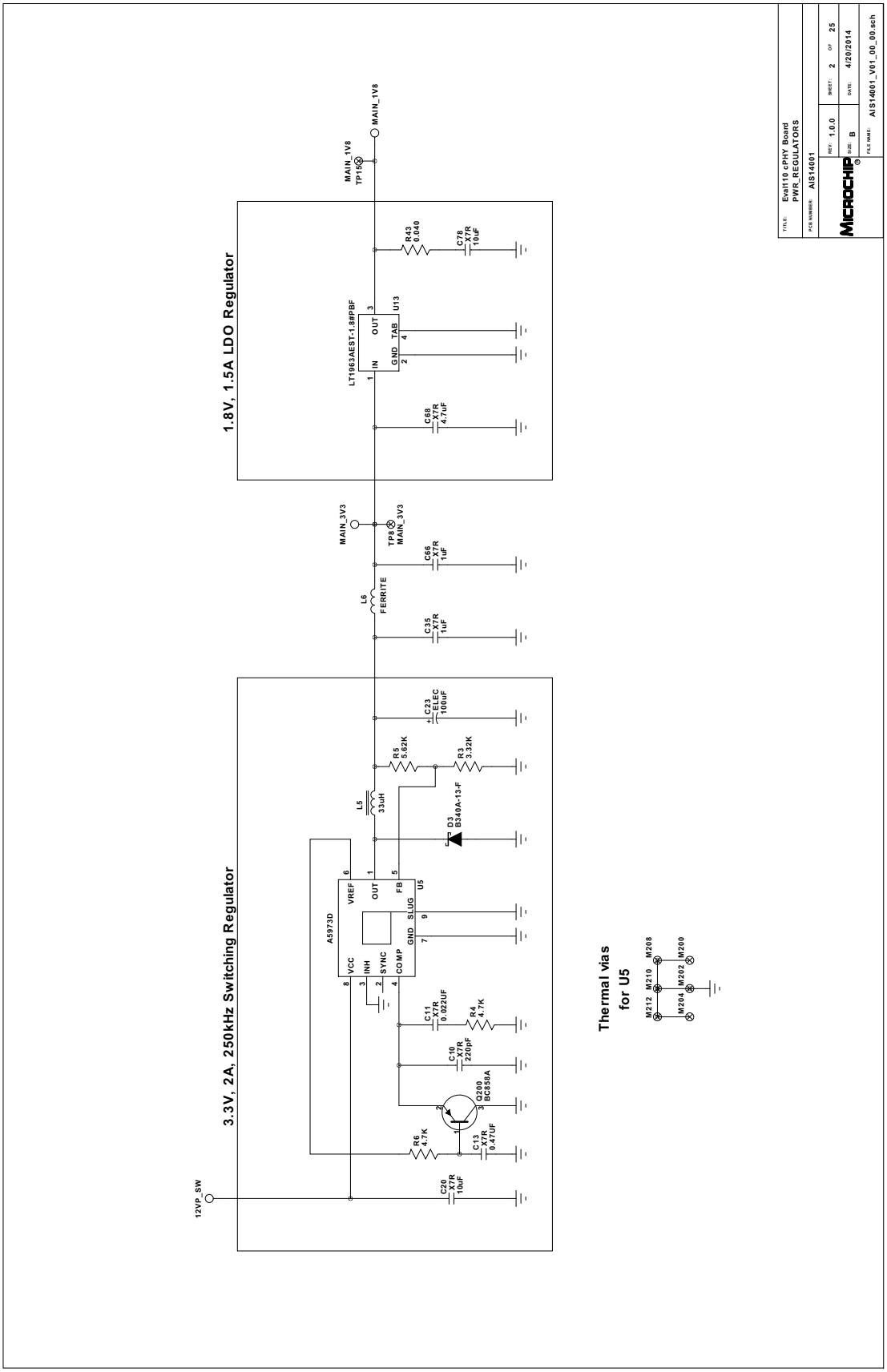


FIGURE D-3: SHEET 3 - PWR_MGMT

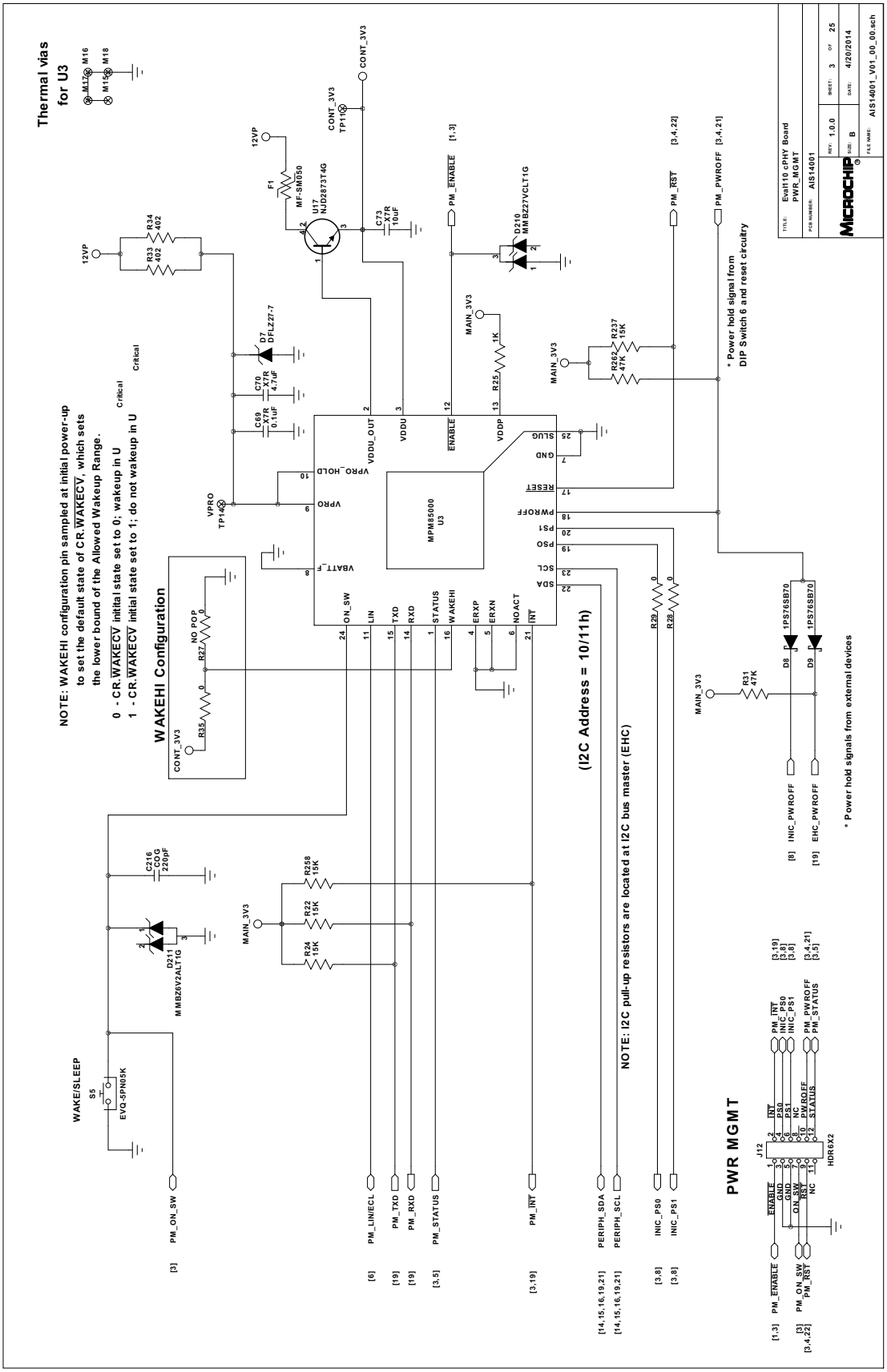


FIGURE D-4: SHEET 4 - BOARD_RESET

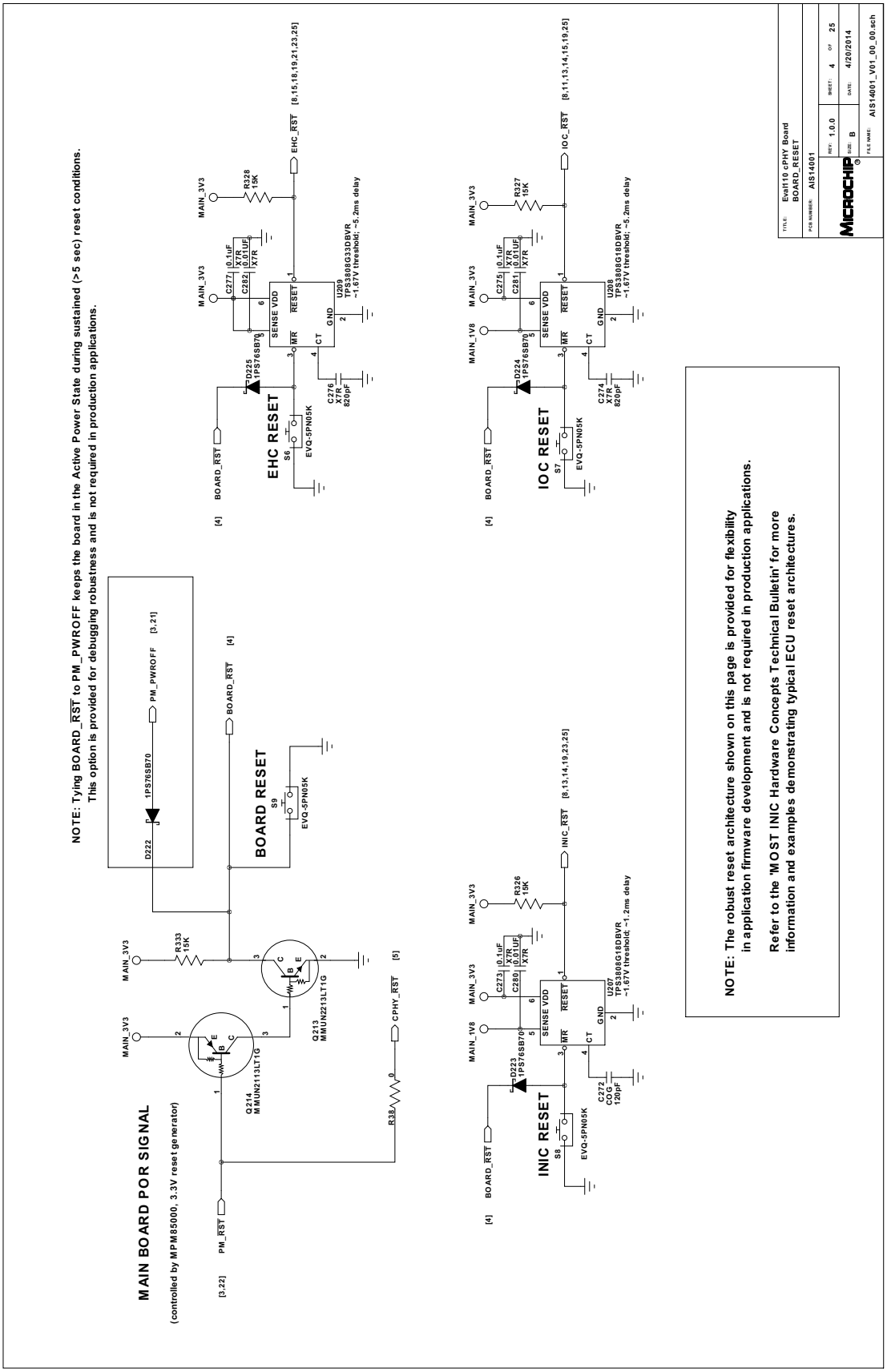


FIGURE D-5: SHEET 5 - MOST_NTWK

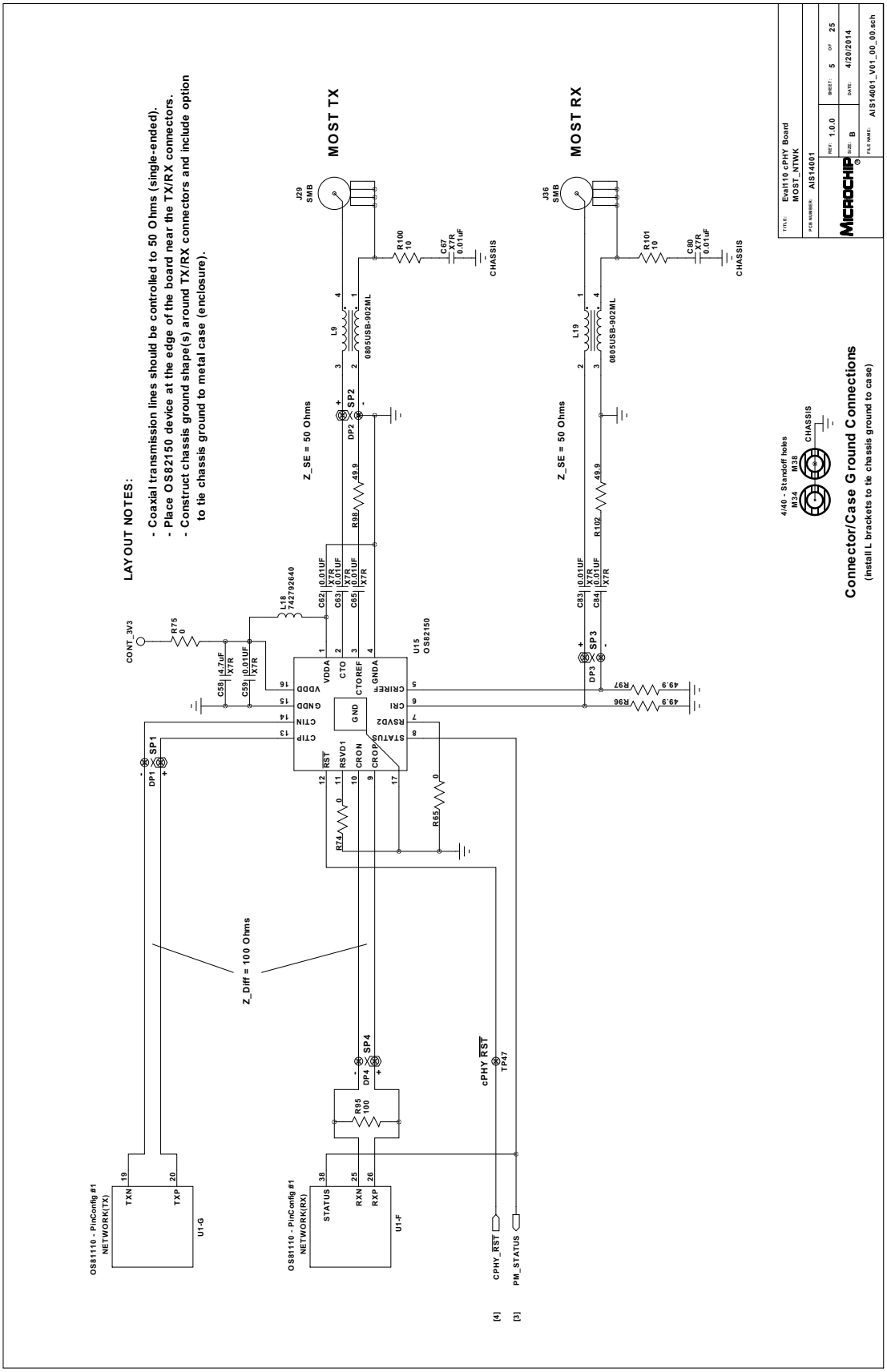


FIGURE D-6: SHEET 6 - CAN_LIN/ECL

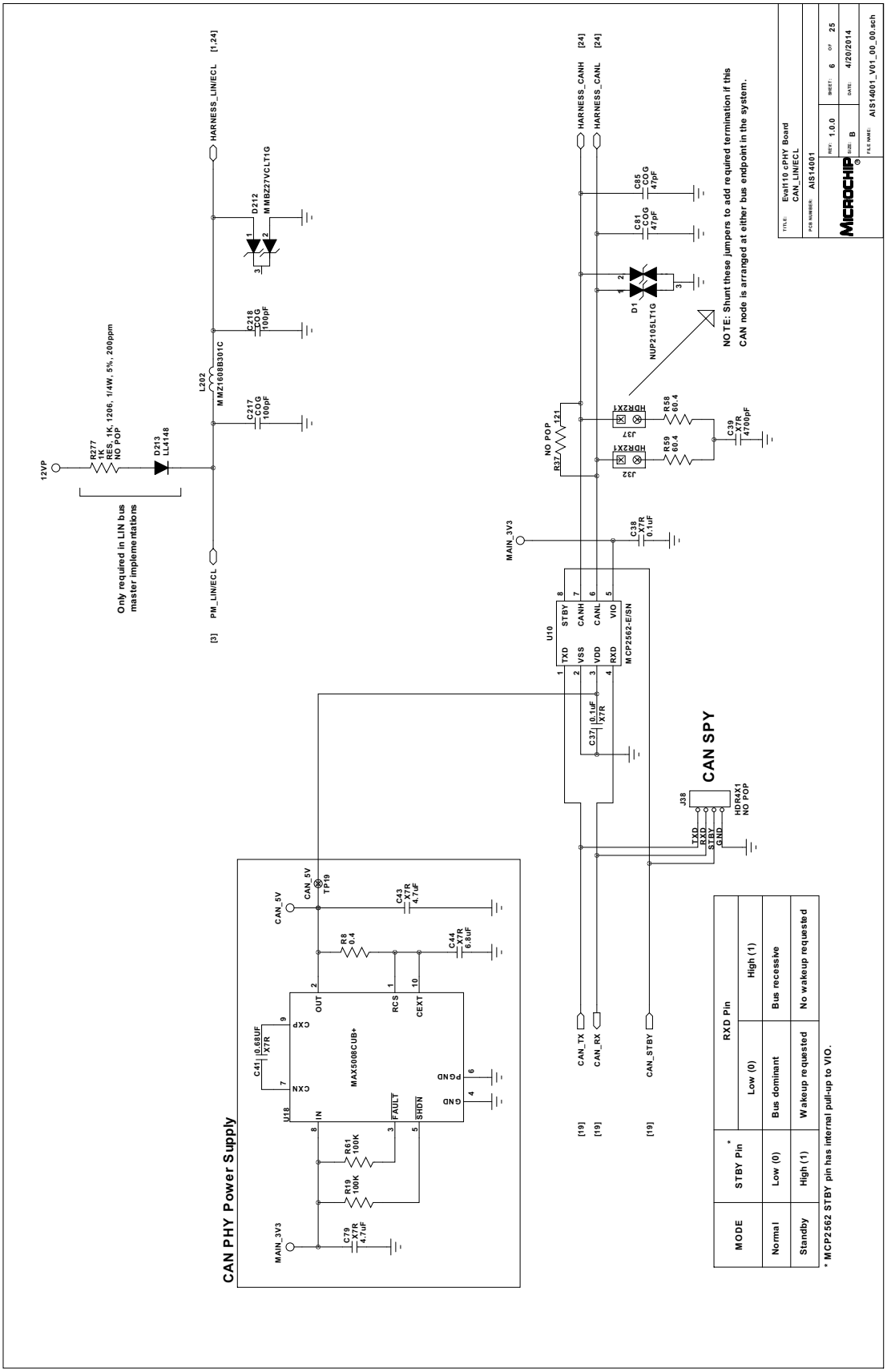


FIGURE D-7: SHEET 7 - INIC_PWR_XTAL

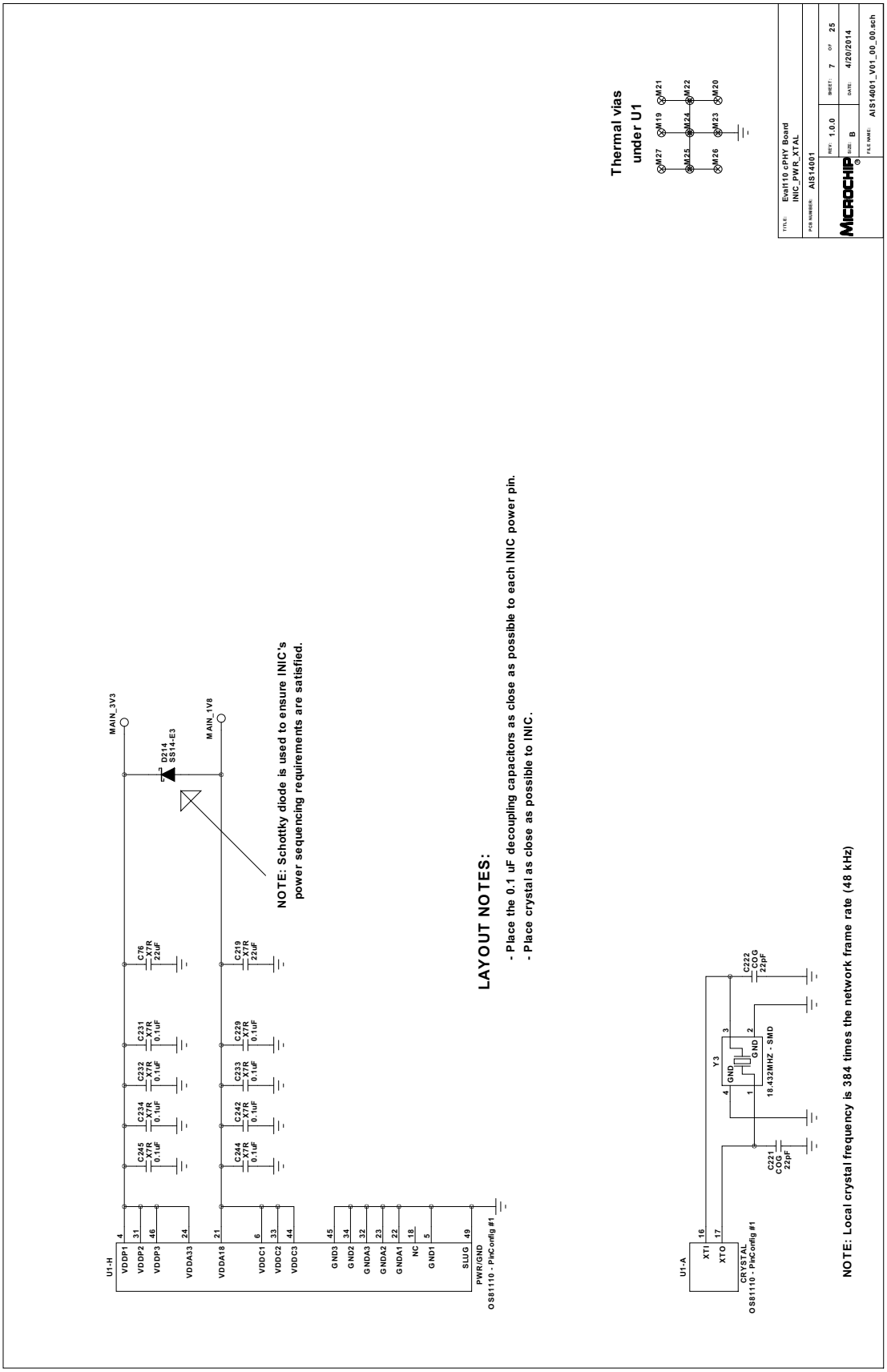


FIGURE D-8: SHEET 8 - INIC_MSC

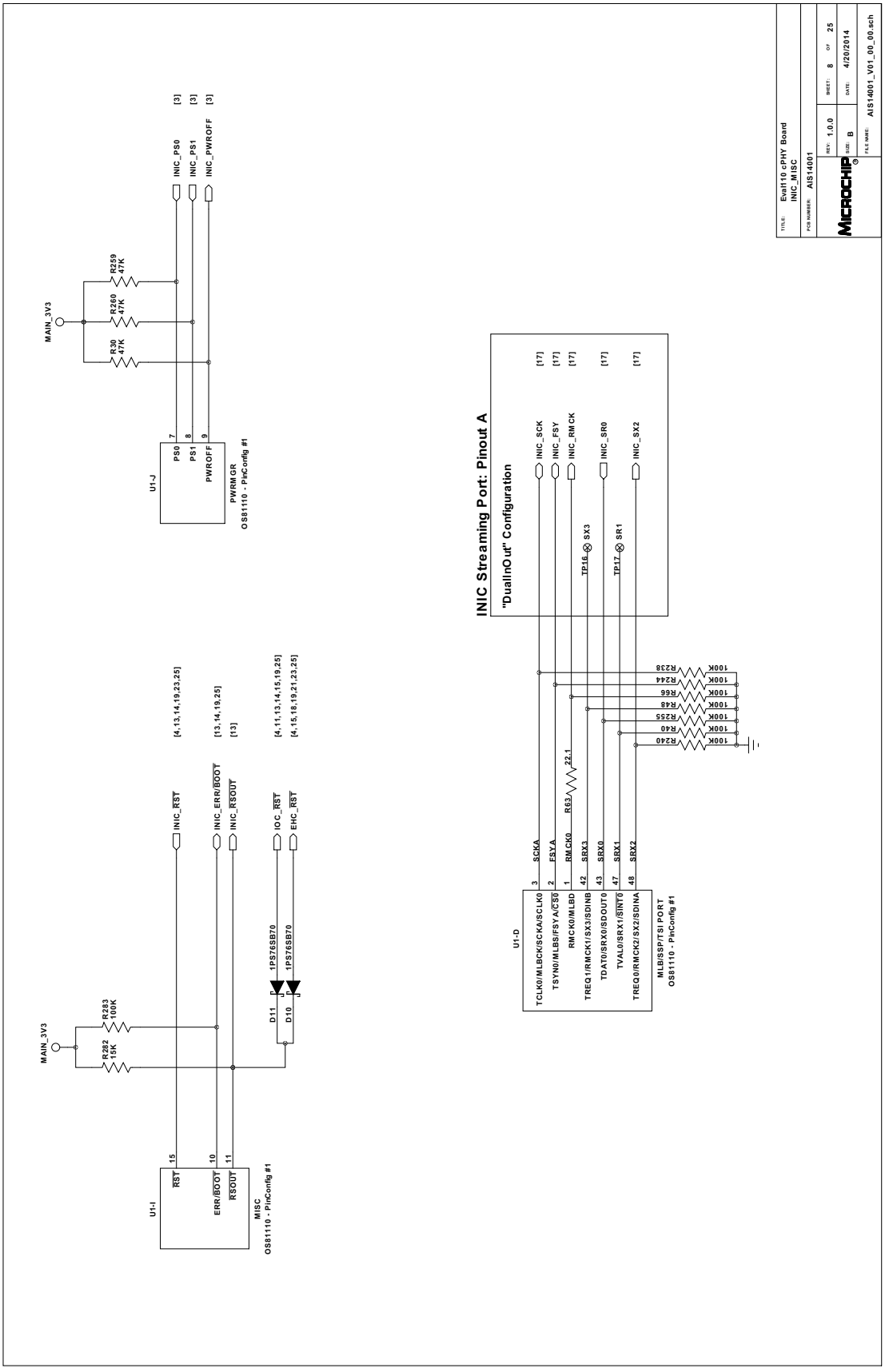


FIGURE D-9: SHEET 9 - IOC_PWR_XTAL

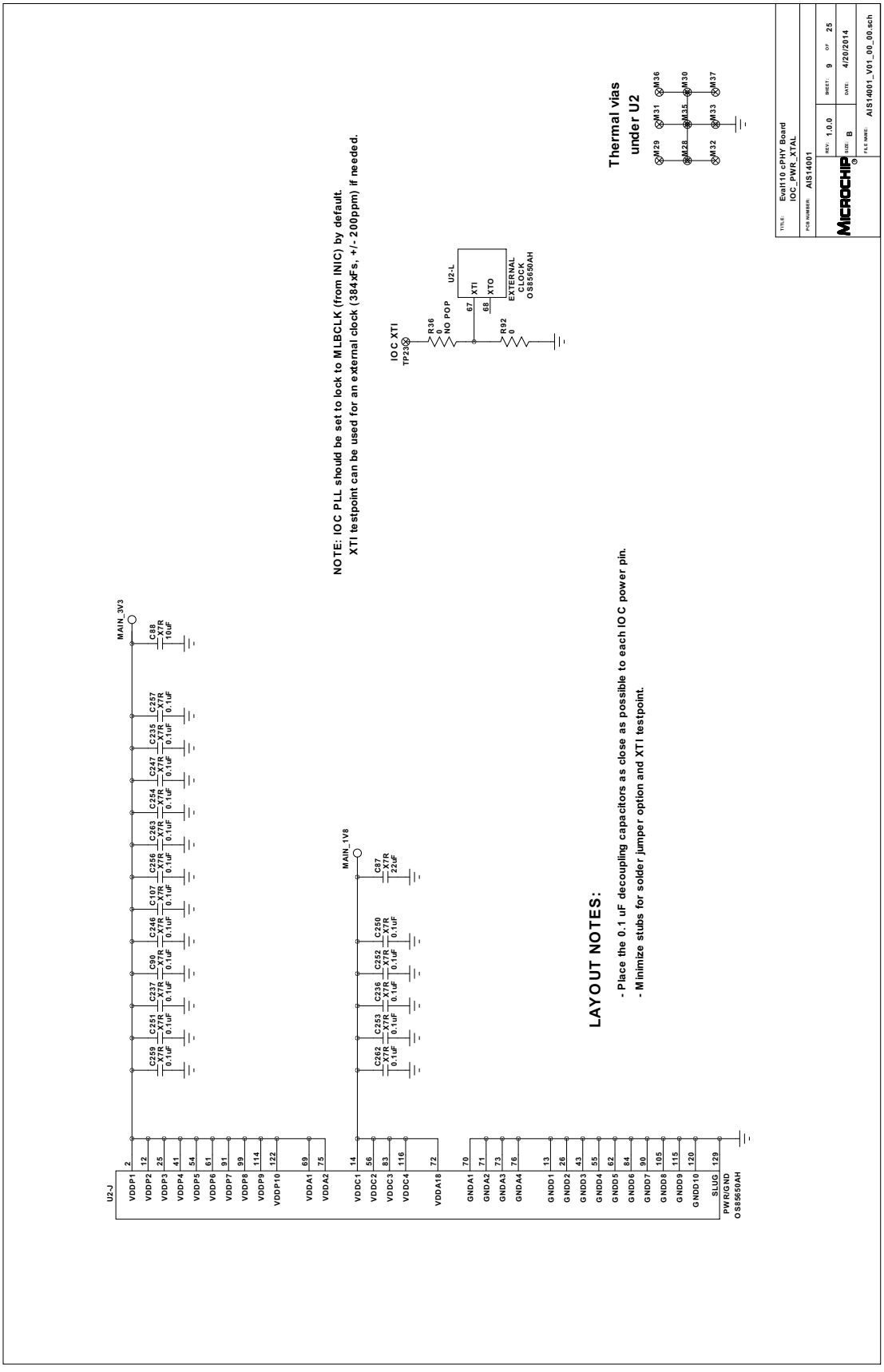


FIGURE D-10: SHEET 10 - IOC_TSI_SPI_SP

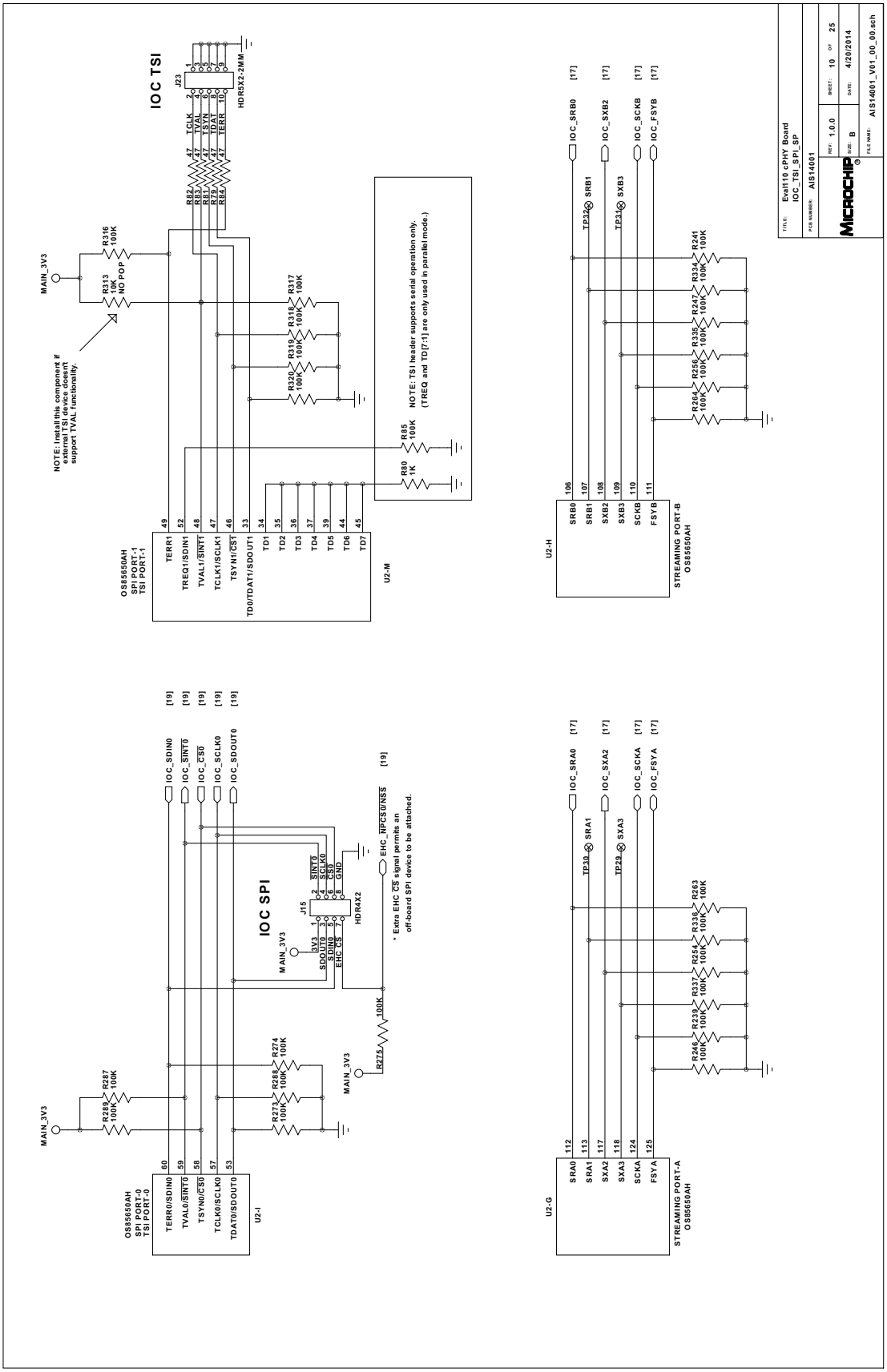


FIGURE D-11: SHEET 11 - IOC_HBI_MISC

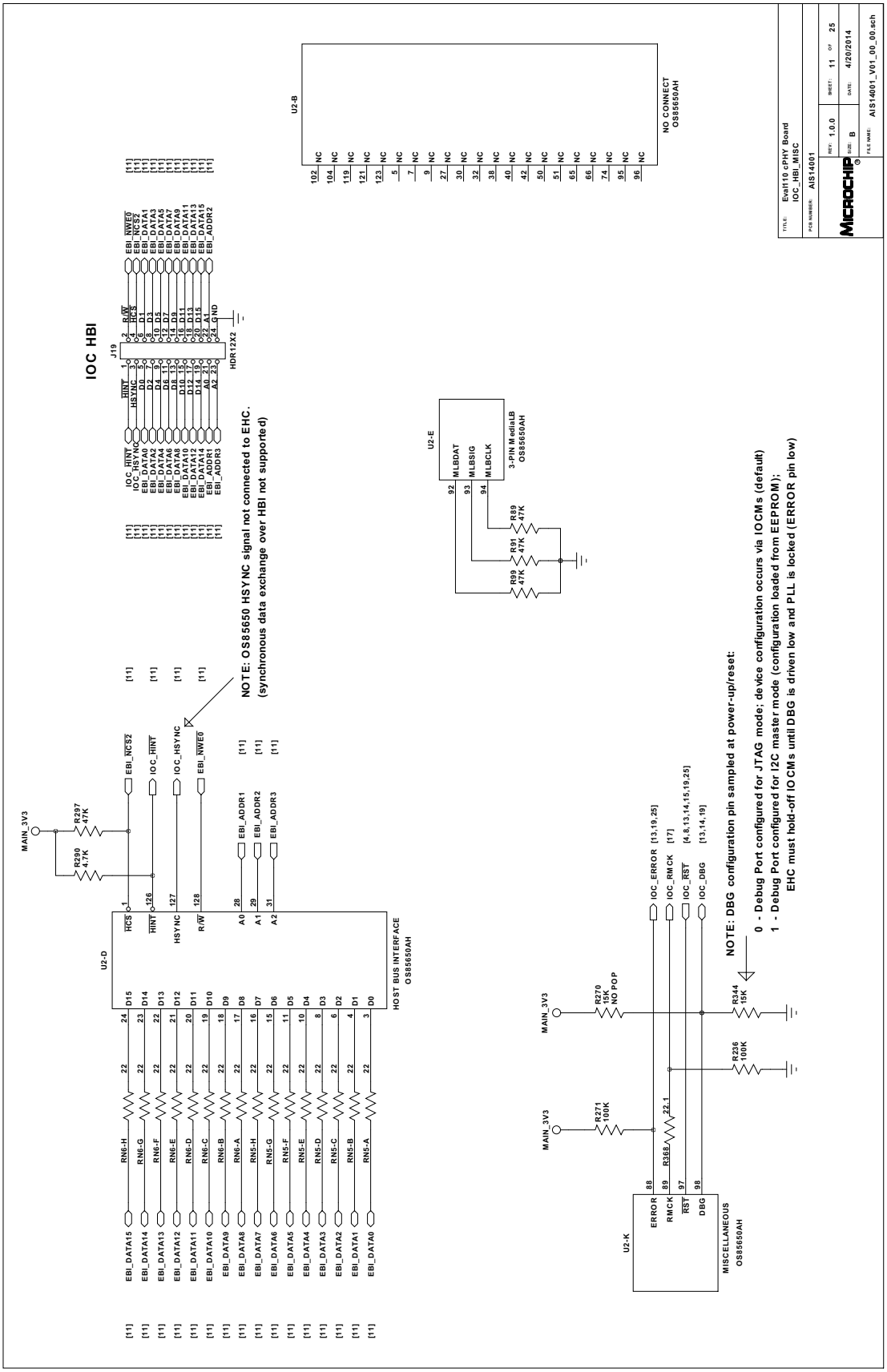


FIGURE D-12: SHEET 12 - MLB_6PIN

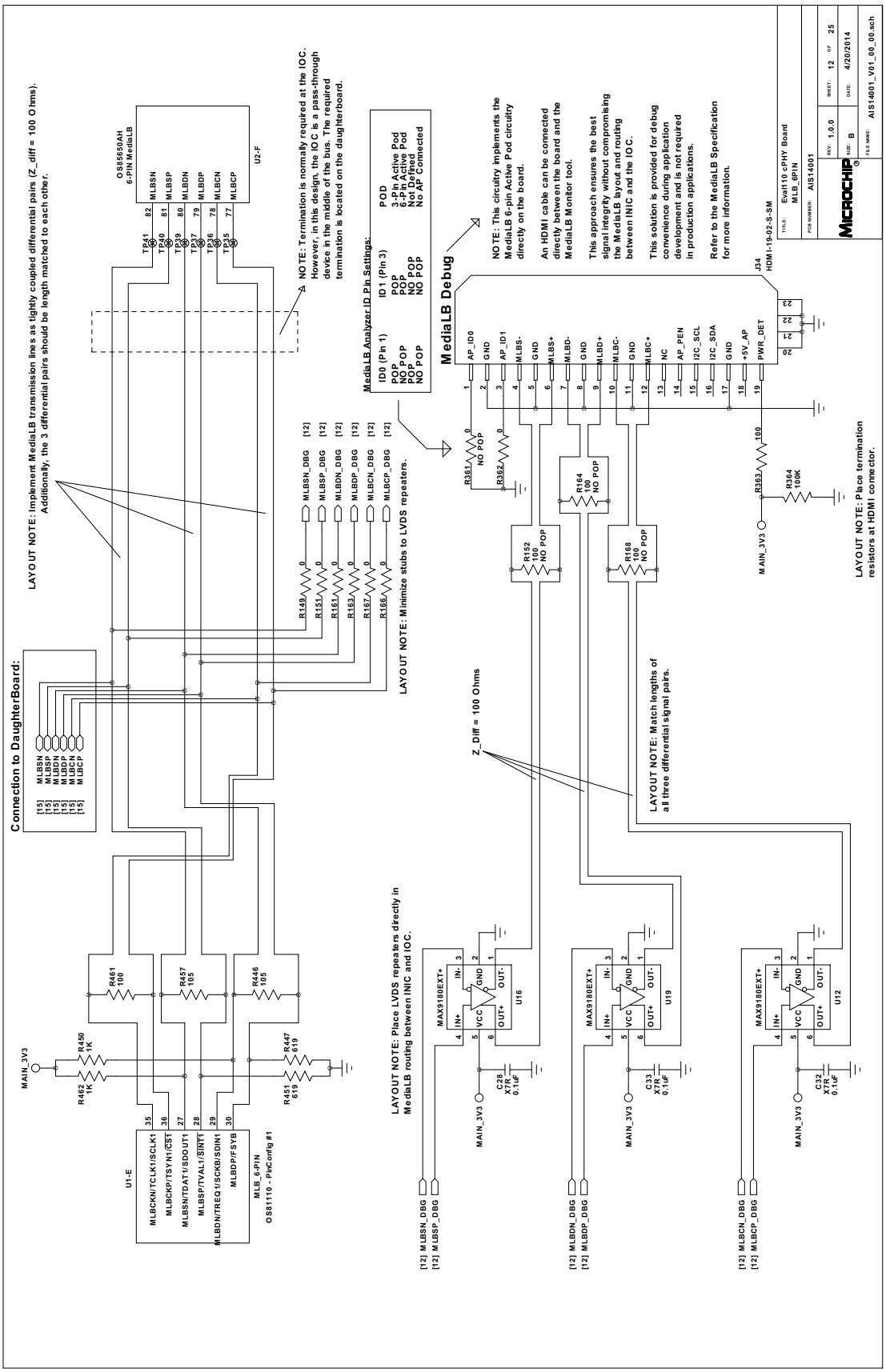


FIGURE D-13: SHEET 13 - MOST_CTRL_PORT

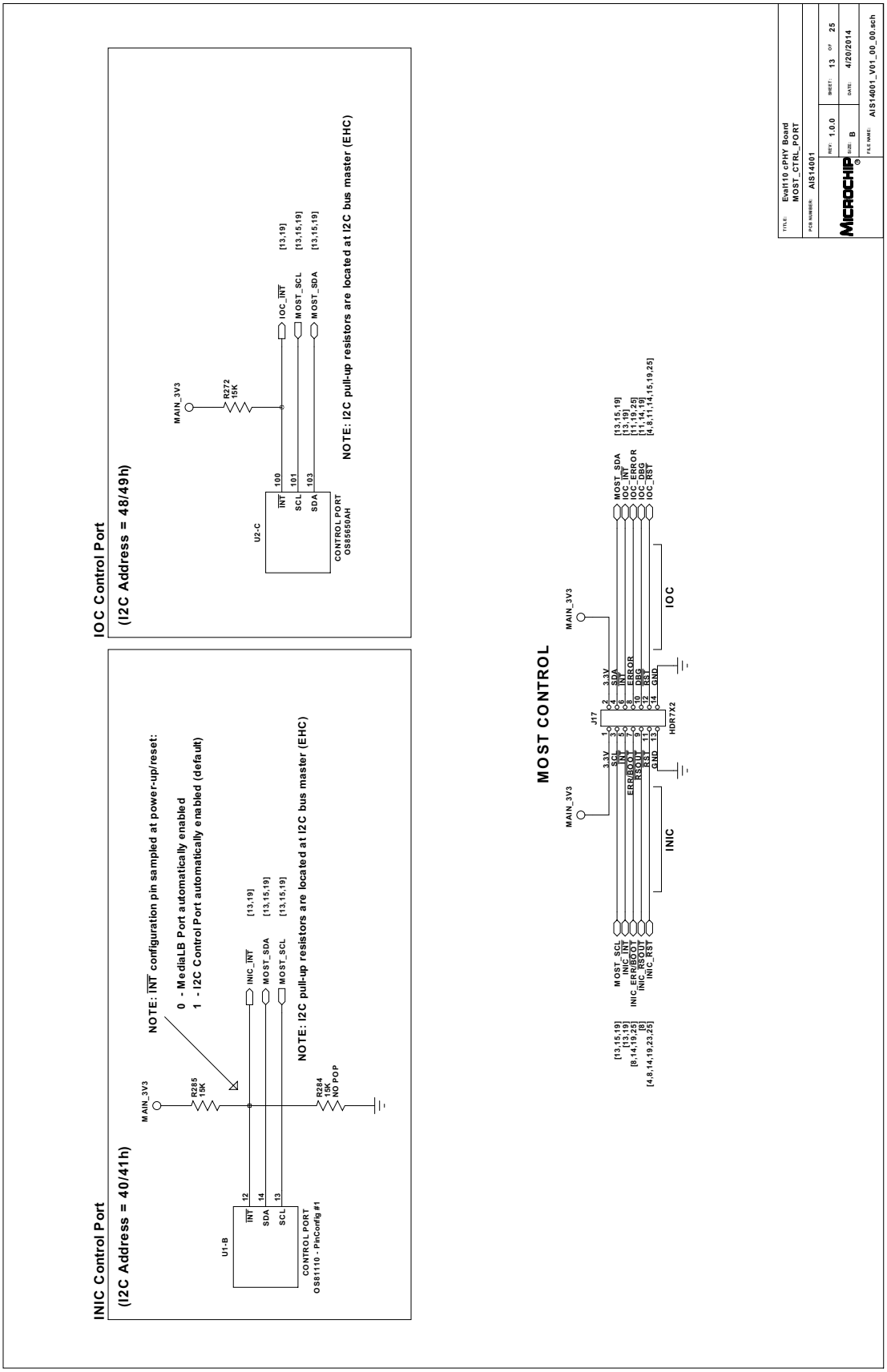


FIGURE D-14: SHEET 14 - MOST_DEBUG_PORT

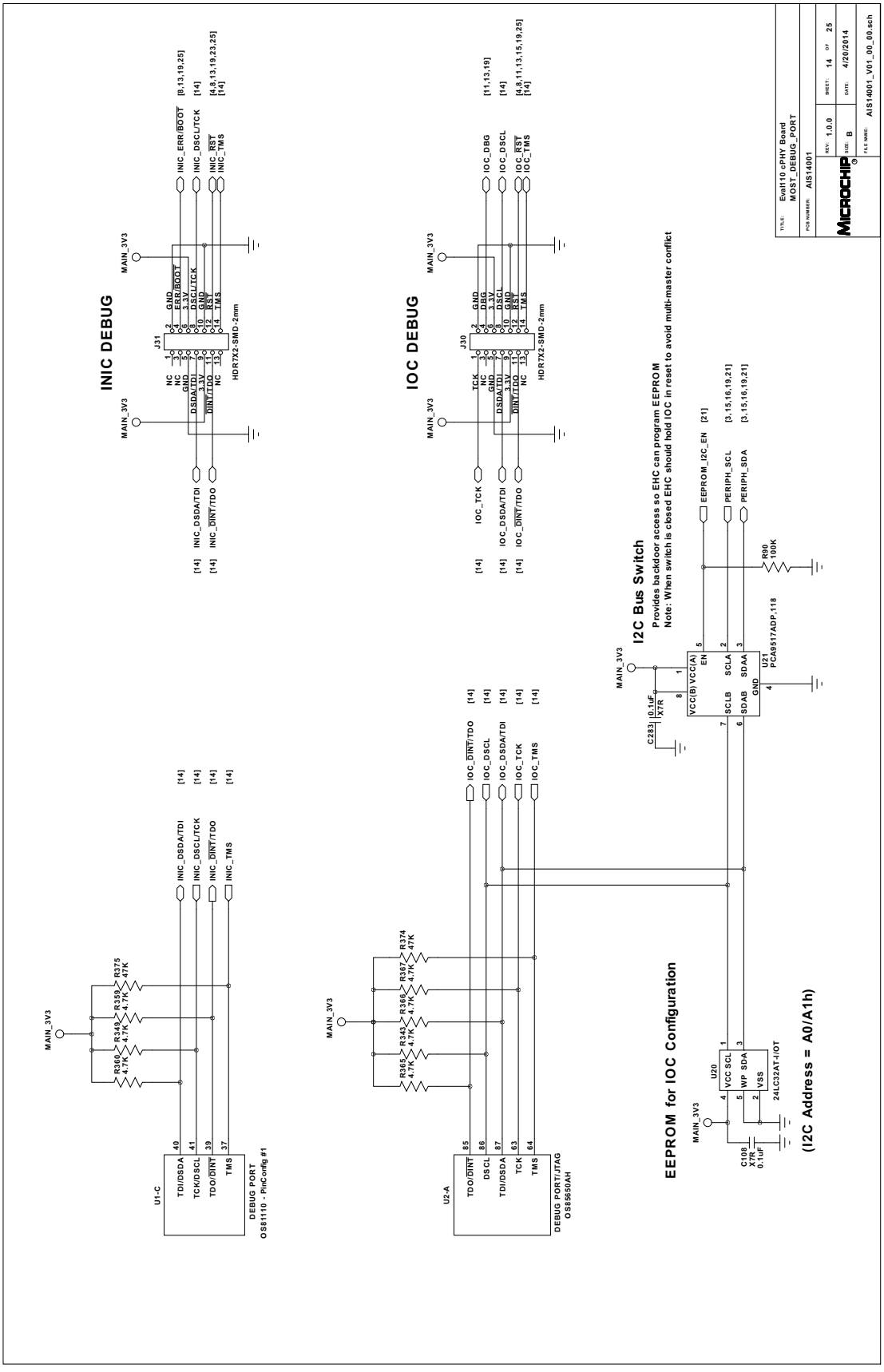


FIGURE D-15: SHEET 15 - DAUGHTER_BOARD

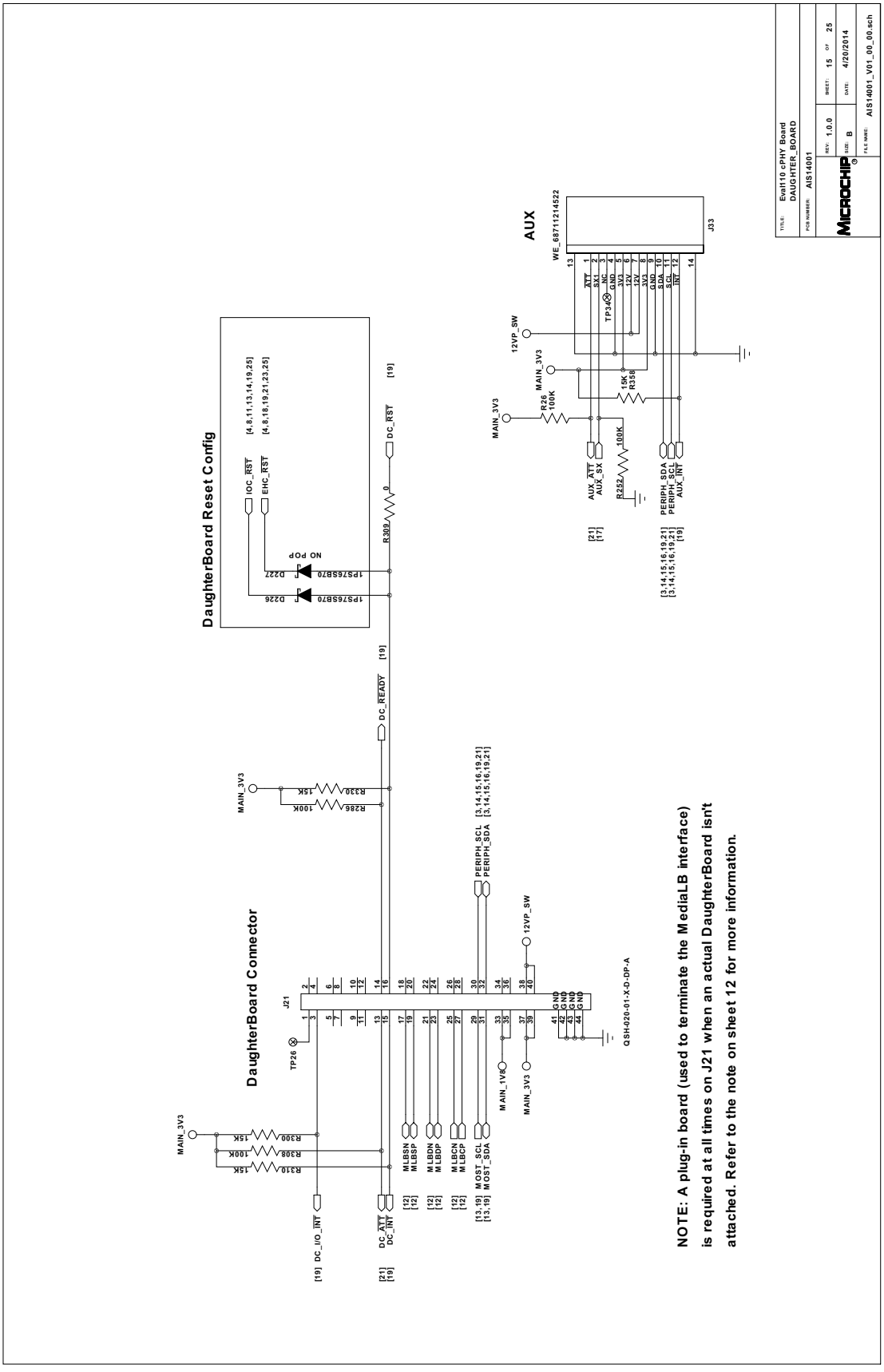


FIGURE D-16: SHEET 16 - AUDIO_CODEC

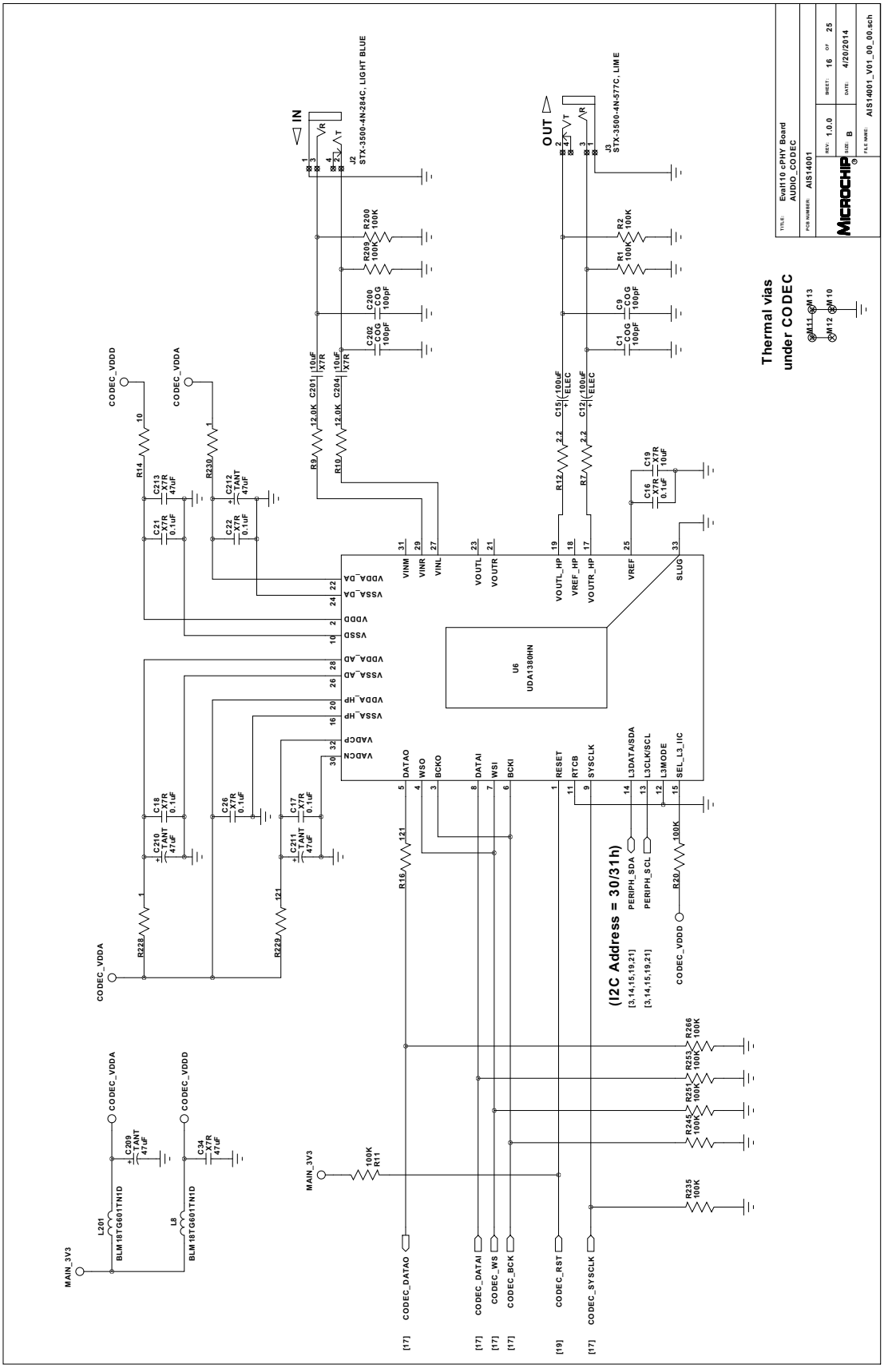


FIGURE D-17: SHEET 17 - I2S/LFST_CONFIG

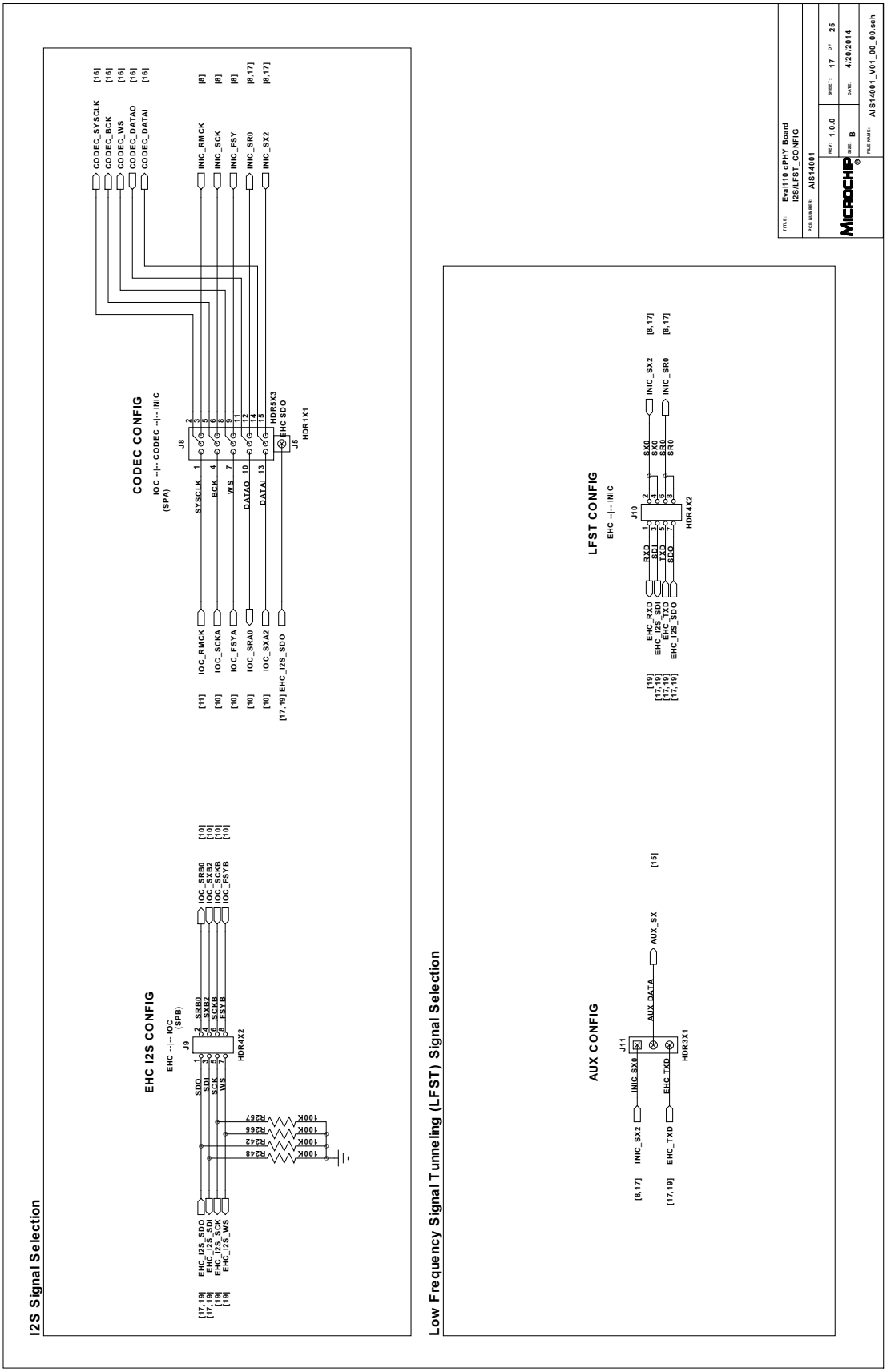


FIGURE D-18: SHEET 18 - EHC_PWR_XTAL

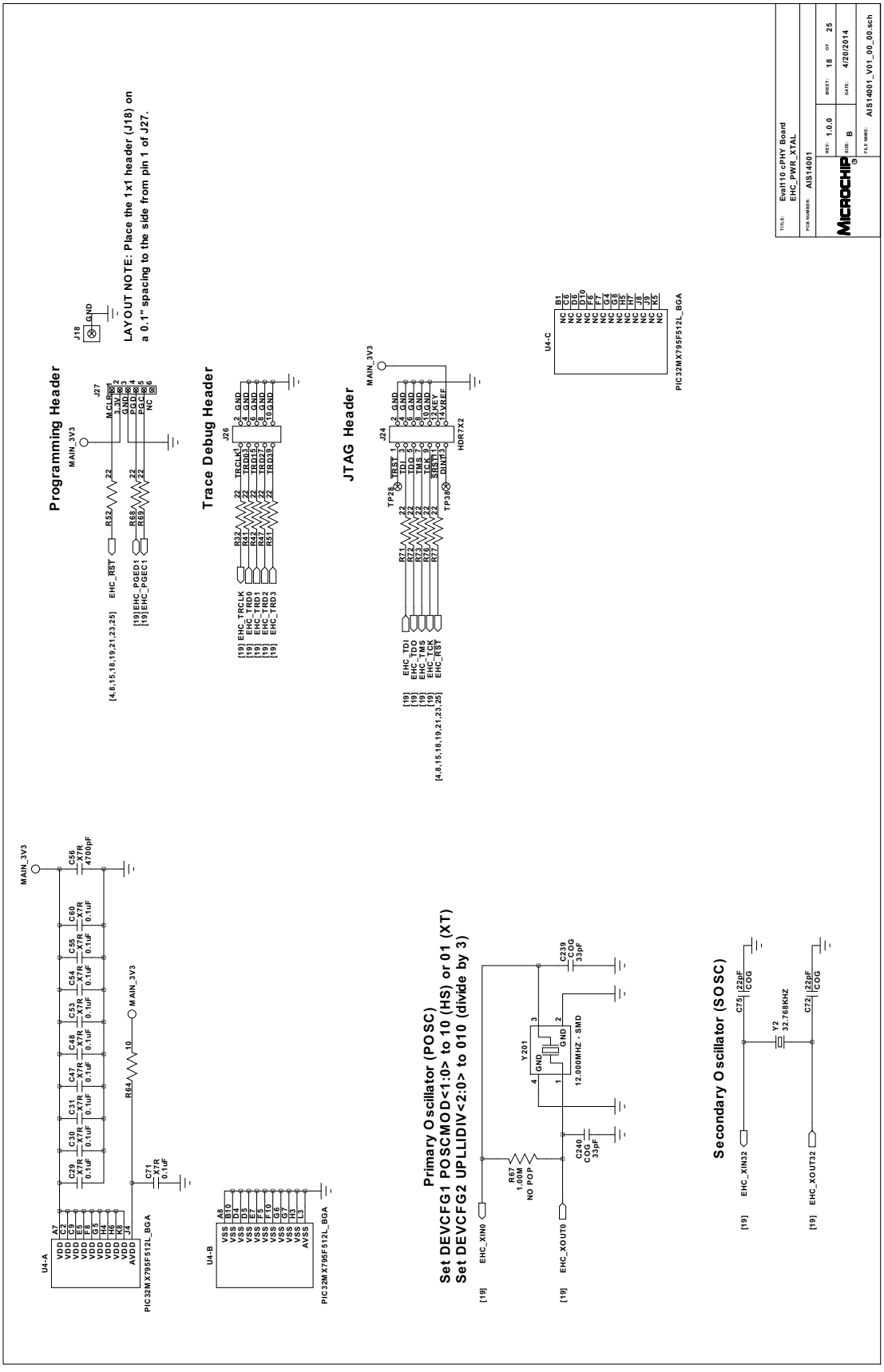


FIGURE D-19: SHEET 19 - EHC_PORTS

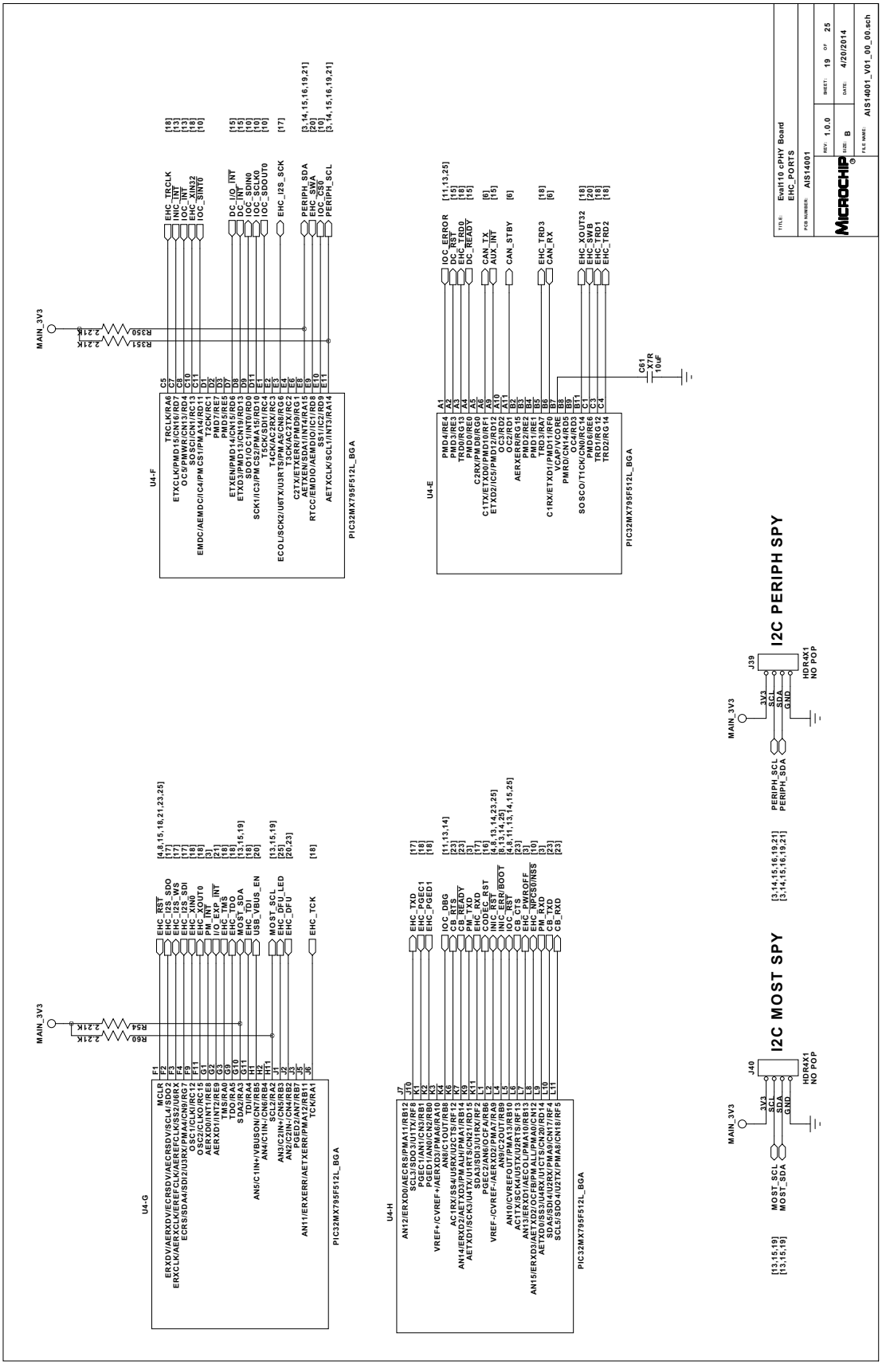


FIGURE D-20: SHEET 20 - EHC_USB

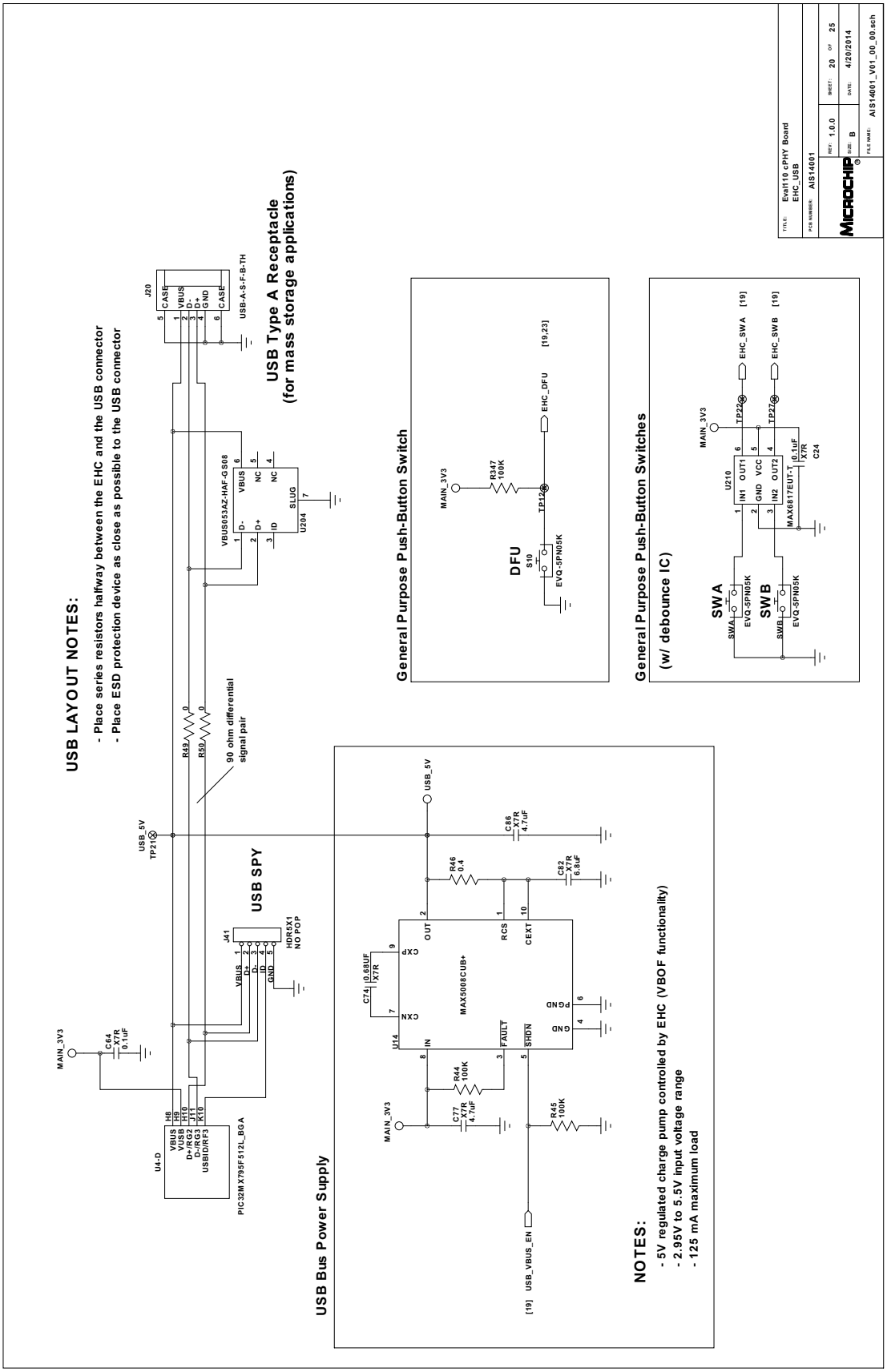


FIGURE D-21: SHEET 21 - I/O_EXPANDER

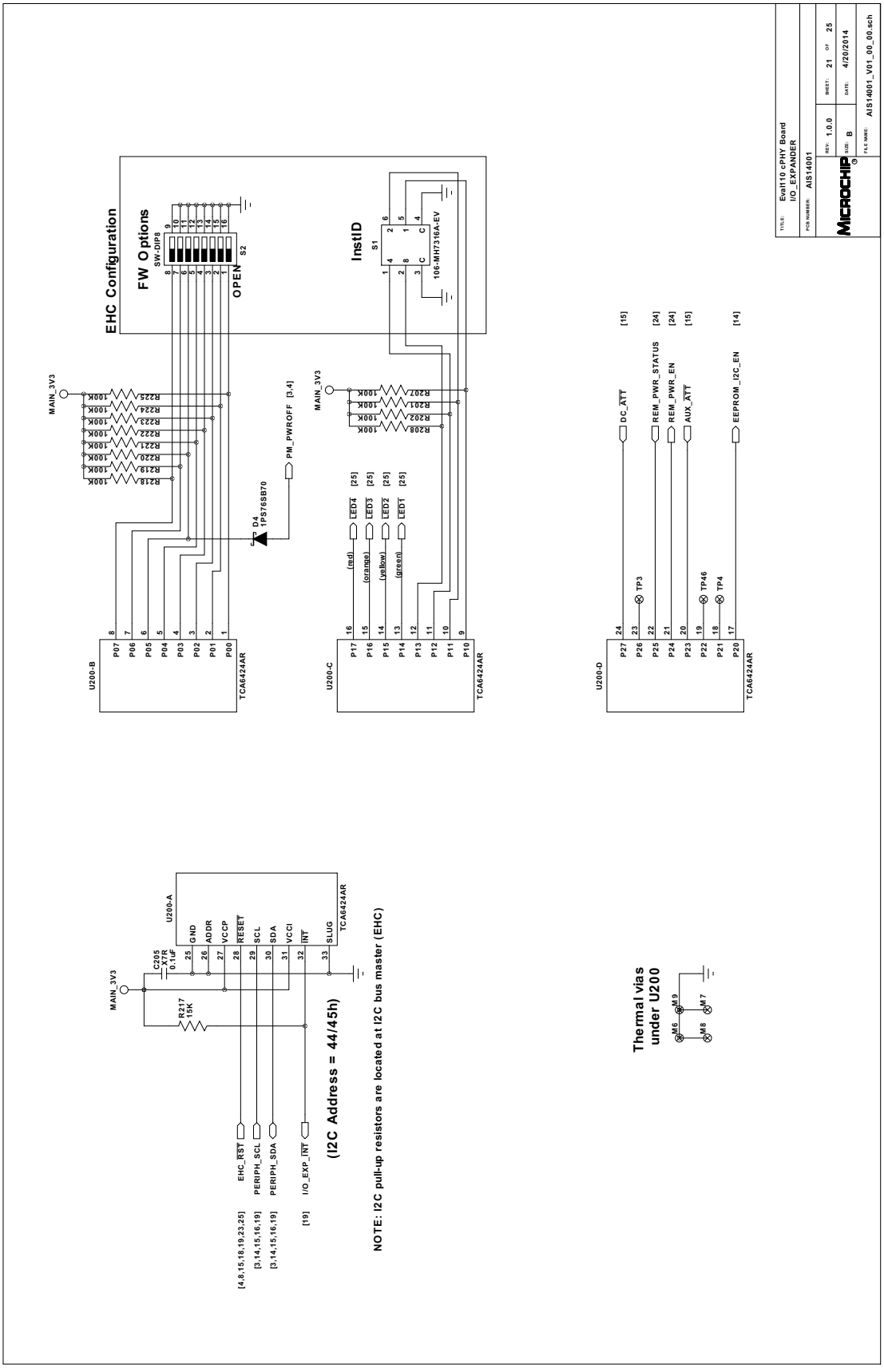


FIGURE D-22: SHEET 22 - COMM_BRIDGE

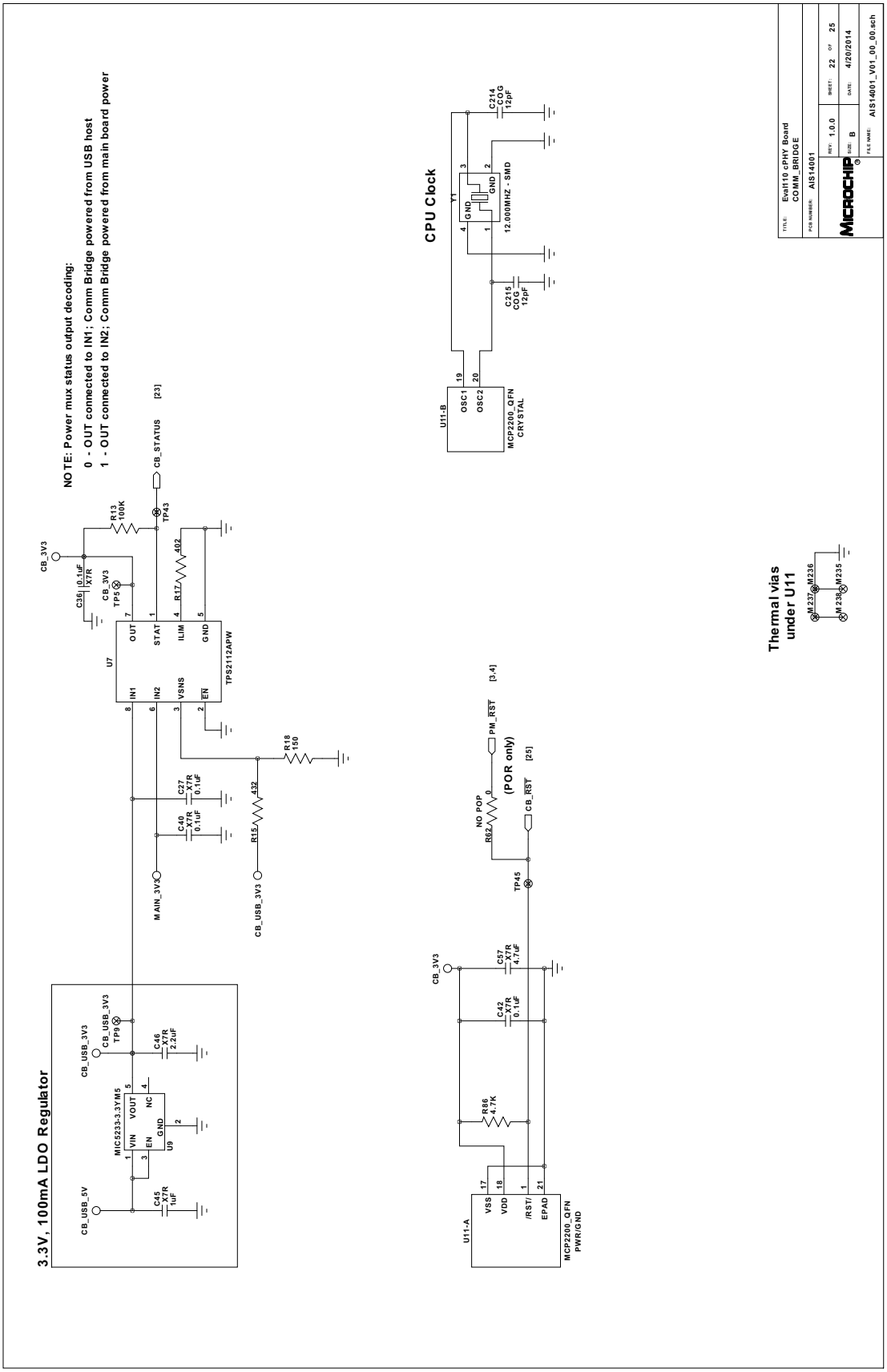


FIGURE D-23: SHEET 23 - COMM_BRIDGE_I/O

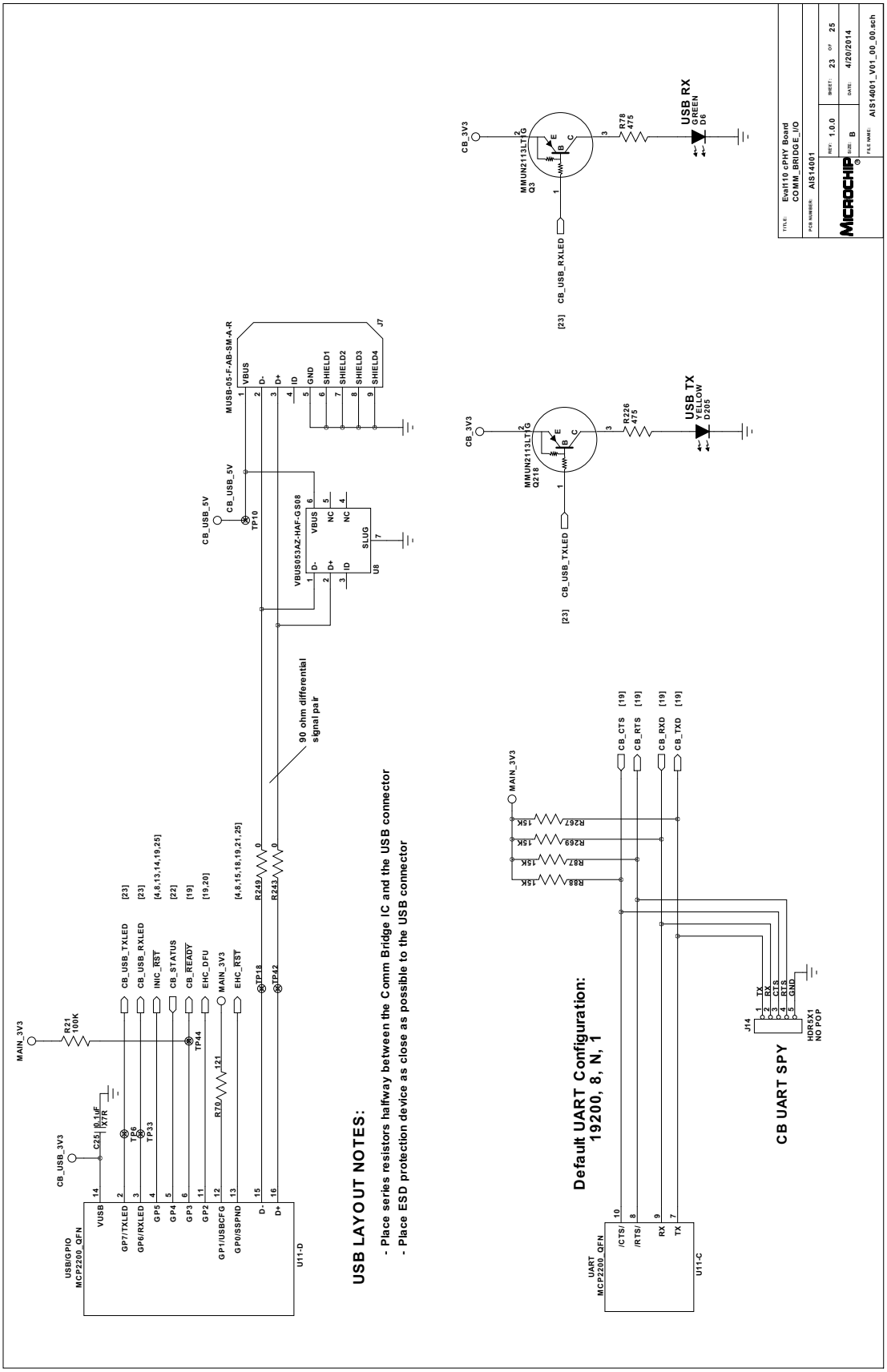


FIGURE D-24: SHEET 24 - CABLE_HARNESS

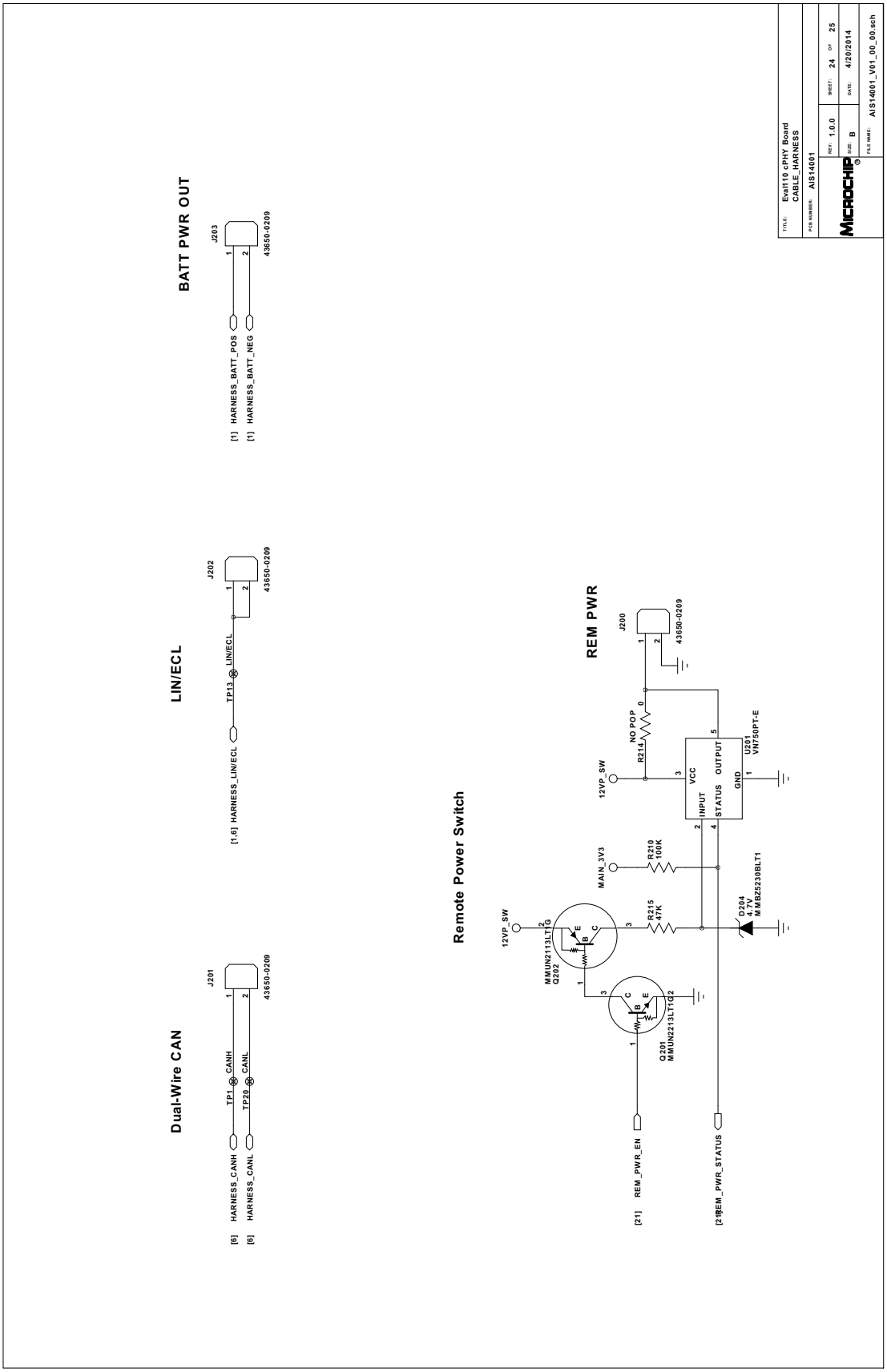
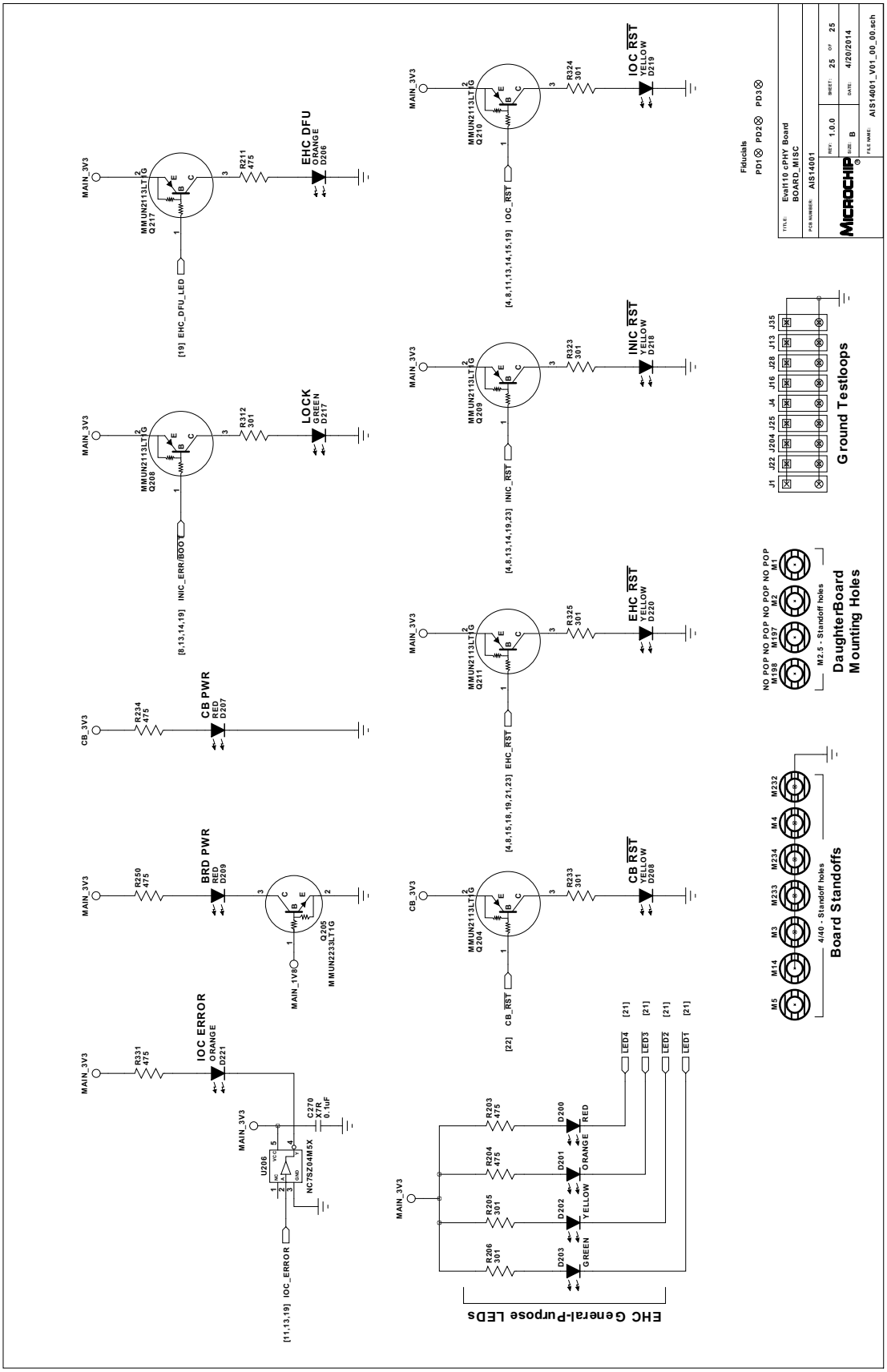


FIGURE D-25: SHEET 25 - BOARD_MISC



APPENDIX E: LAYOUT PLOTS

The following pages contain the layout design files for the Eval110 cPHY Board (AIS14001 V1.0.0). The following table provides an overview of the Eval110 cPHY Board layer stackup.

TABLE E-1: LAYOUT PLOTS OVERVIEW

Layer Number	Layer Name	Description	User's Guide Page
1	SIGNAL - TOP	Top side components and signal routing.	87
2	PLANE - GROUND	Internal ground plane.	88
3	SIGNAL - INNER	Internal signal routing layer.	89
4	PLANE - POWER	Planes for *CB_3V3* and *MAIN_1V8* power nets.	90
5	PLANE - POWER	Plane for *MAIN_3V3* power net.	91
6	SIGNAL - INNER	Internal signal routing layer.	92
7	PLANE - GROUND	Internal ground plane.	93
8	SIGNAL - BOTTOM	Bottom side components and signal routing.	94

Note: Layout plots are provided "as is" without any warranty as an example implementation, and are not guaranteed to be suitable for any particular application. Any design using this information should be tested over the full environmental stress conditions of the intended application.

FIGURE E-1: LAYER 1 (TOP)

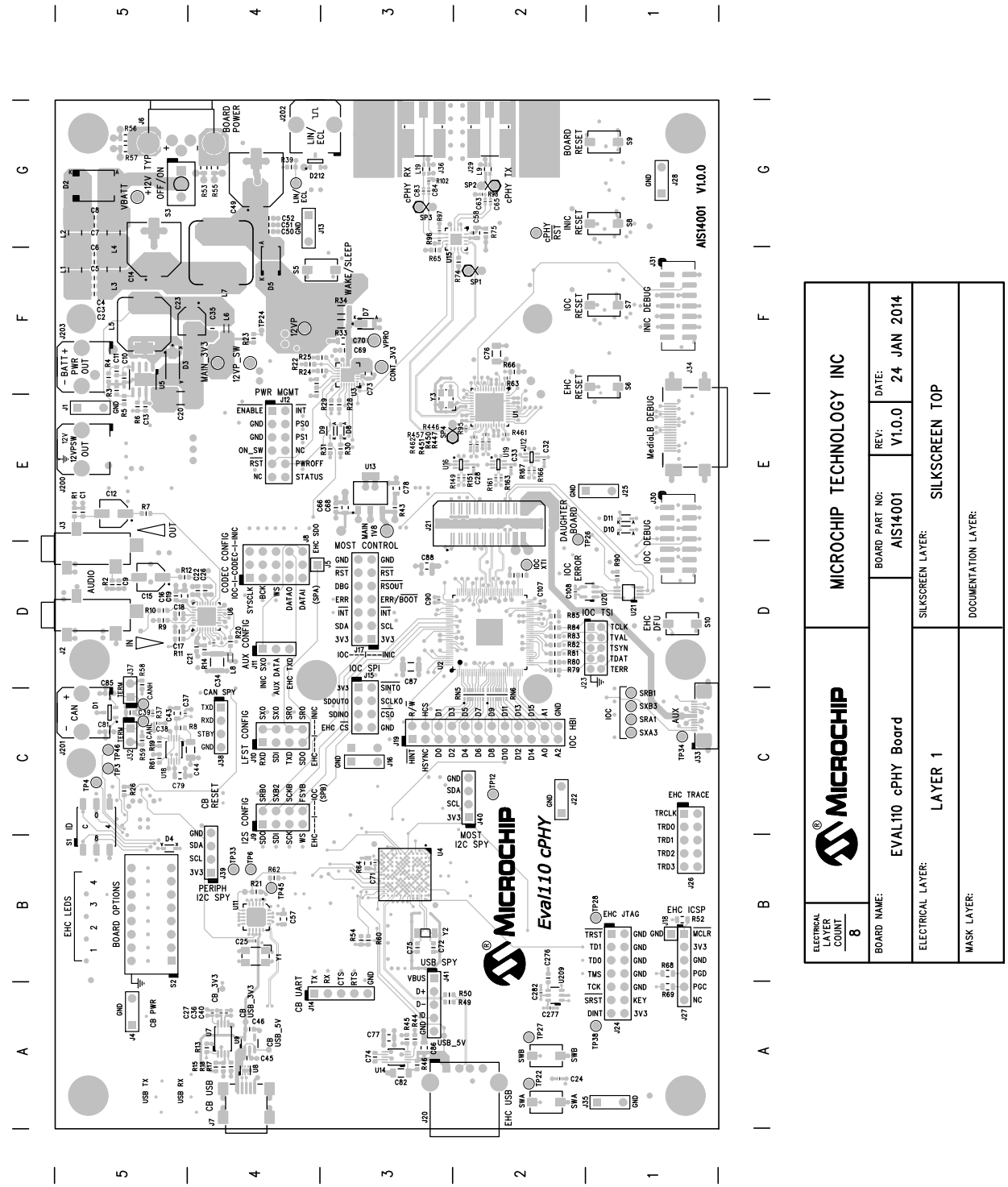


FIGURE E-2: LAYER 2

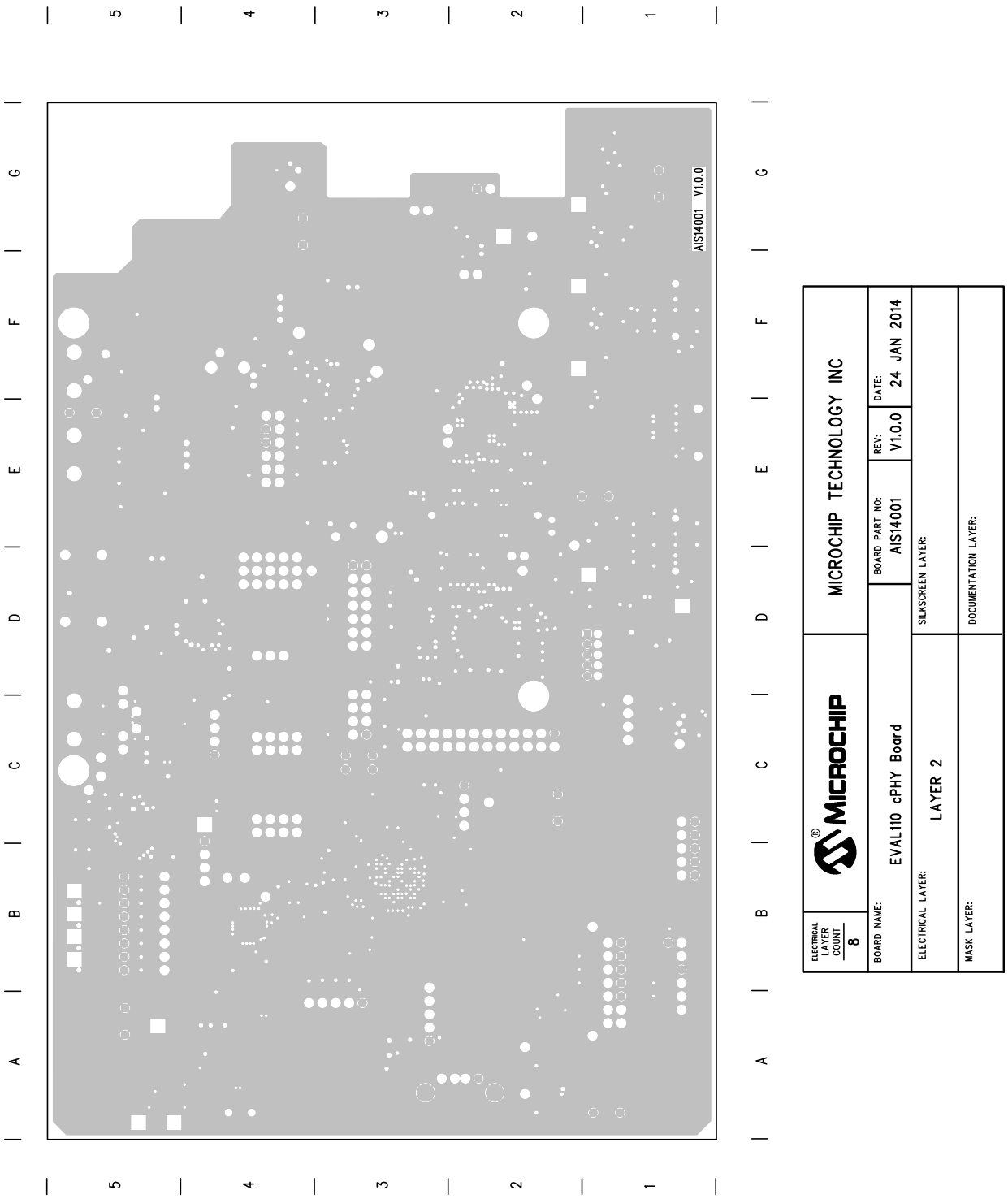


FIGURE E-3: LAYER 3

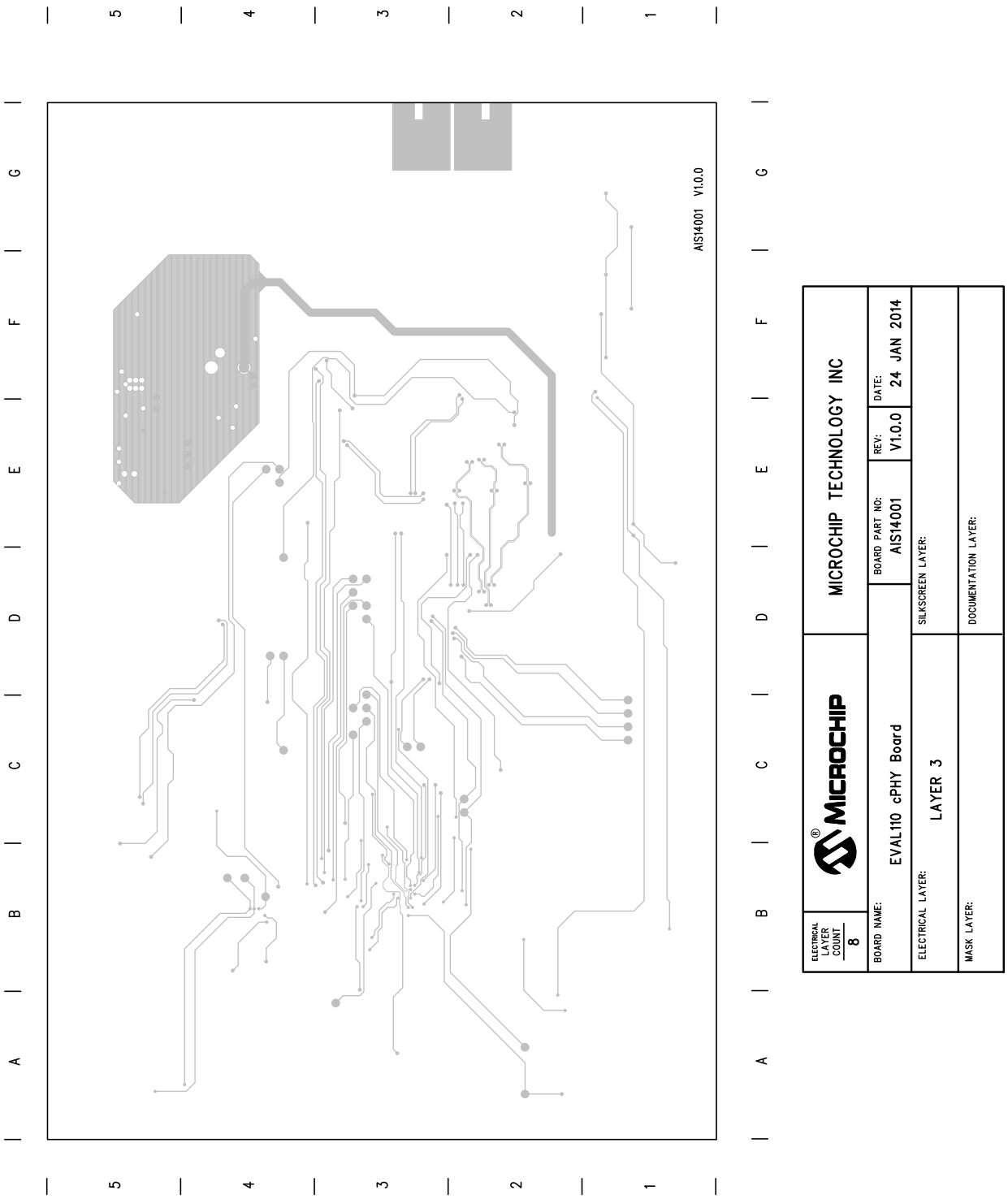


FIGURE E-4: LAYER 4

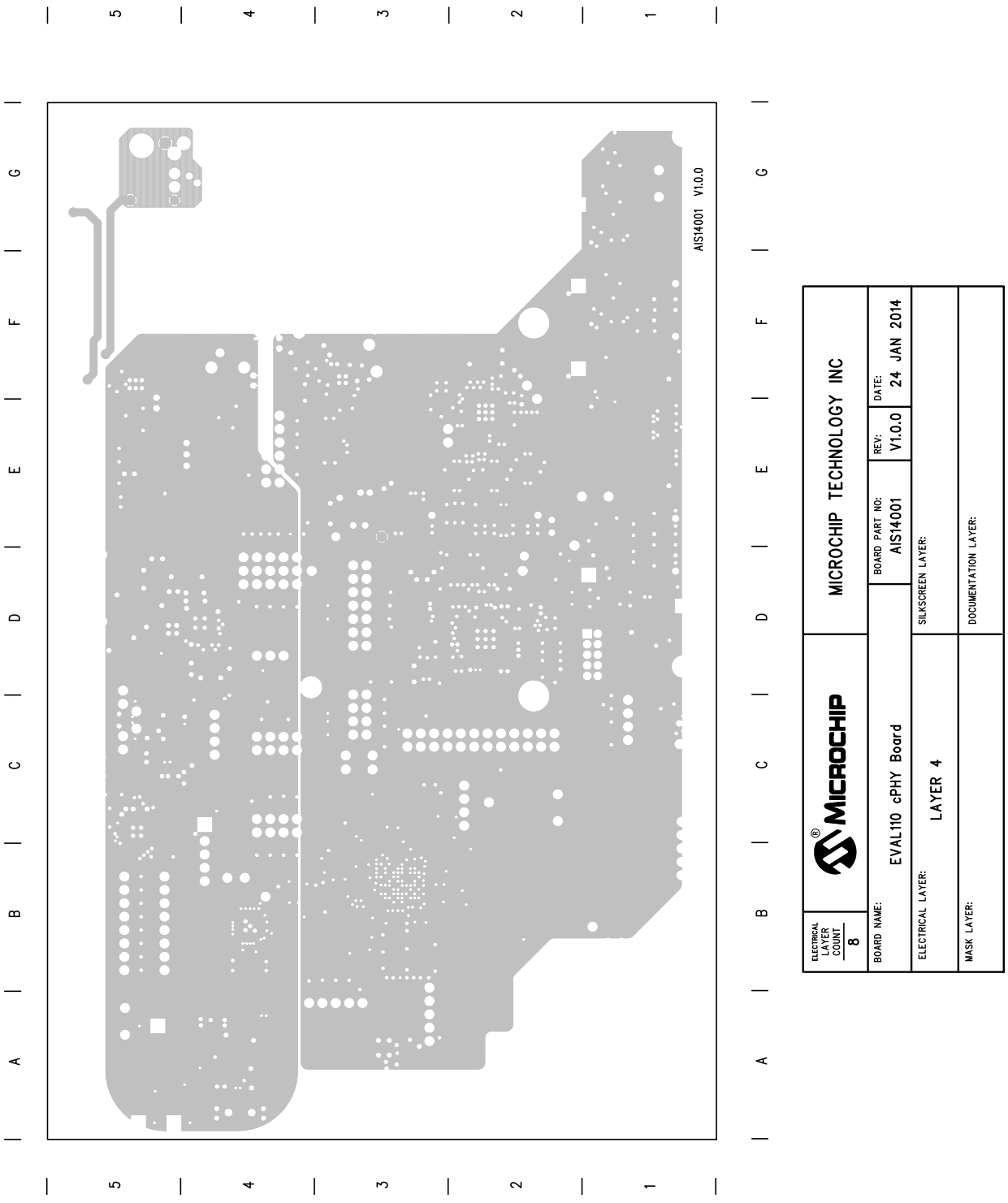


FIGURE E-5: LAYER 5

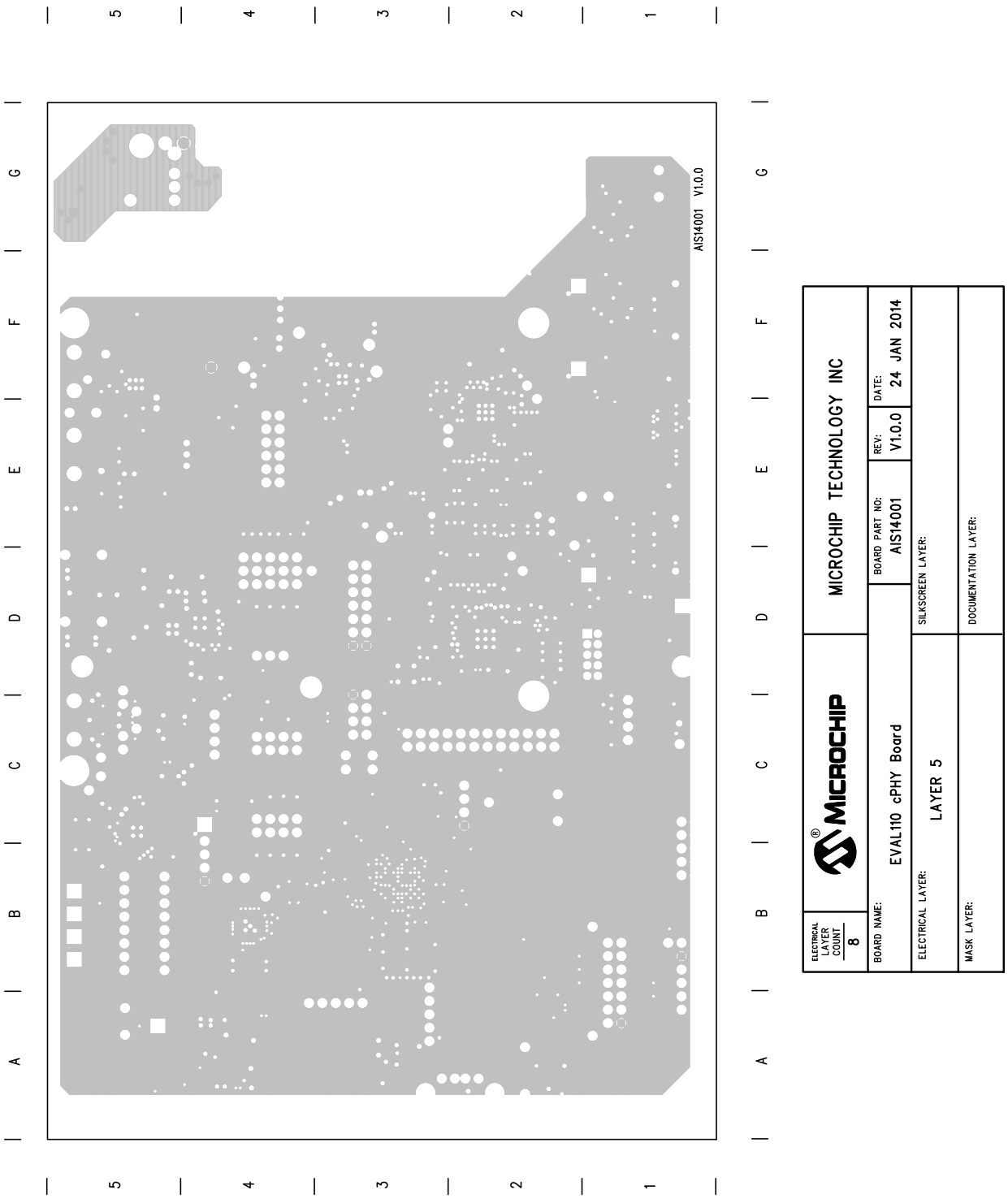


FIGURE E-6: LAYER 6

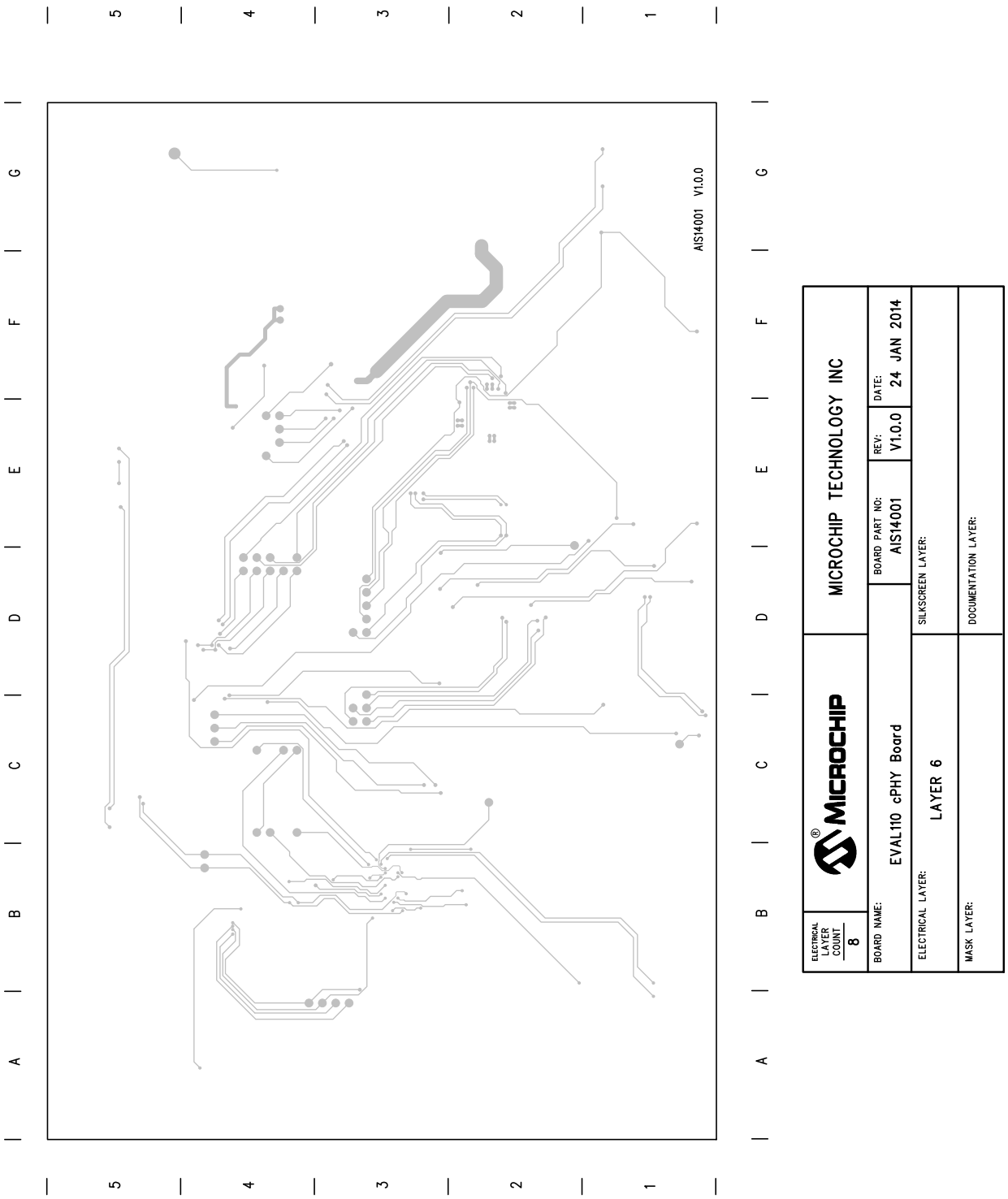


FIGURE E-7: LAYER 7

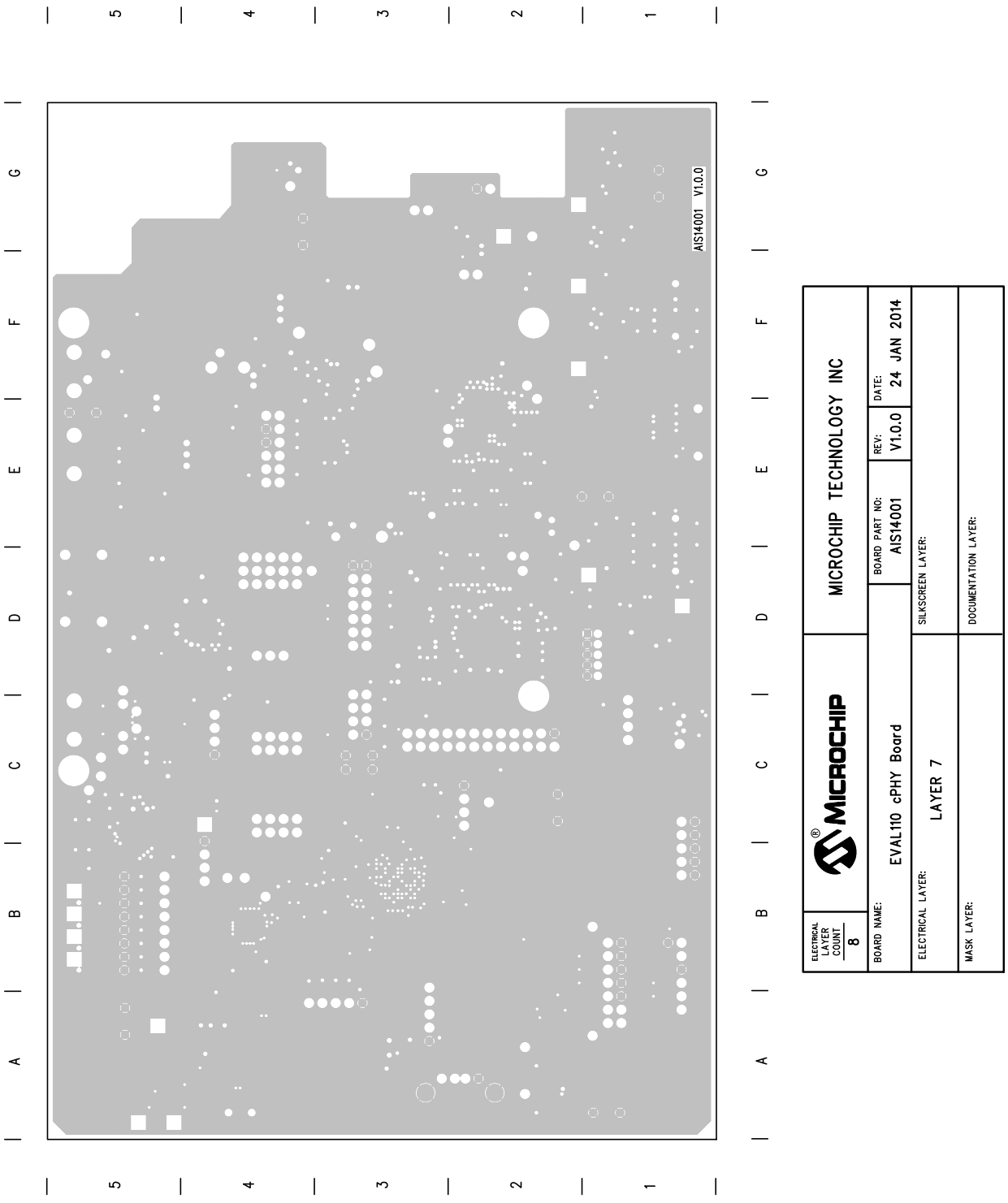
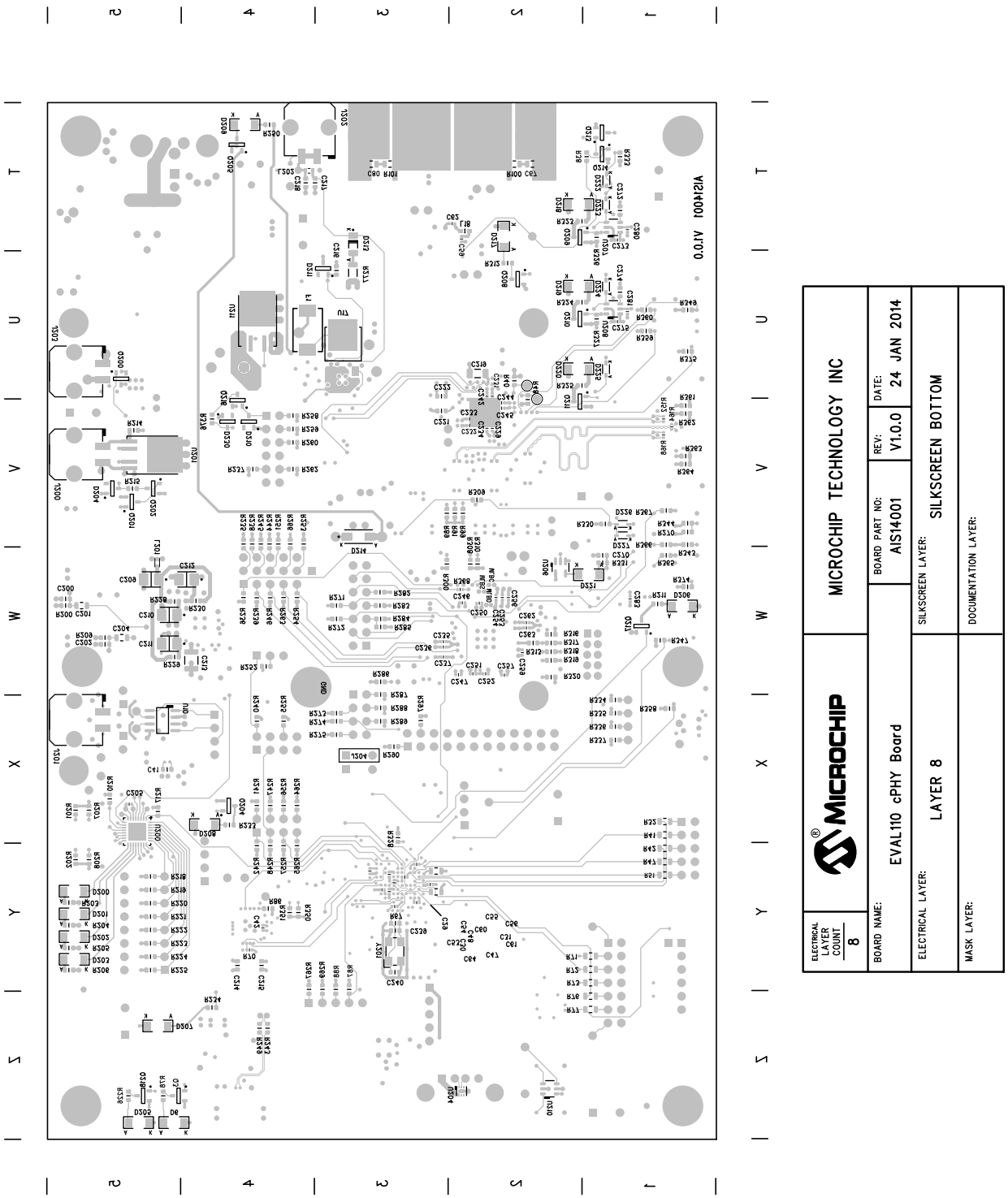


FIGURE E-8: LAYER 8 (BOTTOM)



APPENDIX F: REFERENCES

Documents listed below and referenced within this publication are current as of the release of this publication and may have been reissued with more current information. To obtain the latest releases of Microchip documentation please visit the Microchip website. Please note, some Microchip documentation may require approval. Contact information can be found at www.microchip.com.

All non-Microchip documentation should be retrieved from the applicable website locations listed below. Microchip is not responsible for the update, maintenance or distribution of non-Microchip documentation.

Because the Internet is a constantly changing environment, all Internet links mentioned below and throughout this document are subject to change without notice.

[1] OS81110 MOST150 INIC Data Sheet
DS60001289. Microchip. www.microchip.com.

[2] OS82150 MOST150 Coaxial Transceiver Data Sheet
DS60001225. Microchip. www.microchip.com.

[3] PIC32MX5XX/6XX/7XX 32-Bit Microcontrollers Family Data Sheet
DS60001156. Microchip. www.microchip.com.

[4] OS85650/2 I/O Companion Data Sheet
DS85650AP6. Microchip. www.microchip.com.

[5] MPM85000 Automotive Power Management Device Data Sheet
DS85000AP4. Microchip. www.microchip.com.

[6] MOST ToGo Architecture and Implementation Guide
DS60001272. Microchip. www.microchip.com.

[7] MOST Specification 3.0
Rev. 3.0 E2. MOST Cooperation. www.mostcooperation.com.

[8] MOST Electrical Control Line Specification
Revision 1.1.1. MOST Cooperation. www.mostcooperation.com.

[9] OS81110 MOST150 INIC API User's Manual
Rev 1.8.3-1. Microchip. www.microchip.com.

[10] MOST INIC Hardware Concepts Technical Bulletin
DS60001264. Microchip. www.microchip.com.

[11] OS85621/3 Video I/O Companion Data Sheet
DS60001261. Microchip. www.microchip.com.

[12] KLR83012 Fully-Integrated Wireless Audio/Voice Transceiver Data Sheet
v2.0. Microchip. www.microchip.com.

[13] INIC Flash Guide Application Note
V02_00_XX-5. Microchip. www.microchip.com.

[14] INIC Explorer Interface Tool Specification
V1.6.x-1. Microchip. www.microchip.com.

[15] MediaLB Specification
TB0400AN4V2. Microchip. www.microchip.com.

[16] MediaLB Monitor Adapter User's Manual
V2.0.x-2. Microchip. www.microchip.com.

[17] OS62420 MediaLB Device Interface Macro Data Sheet
DS60001215. Microchip. www.microchip.com.

[18] DTCP Specification
Available under license from the DTLA. www.dtcp.com.

[19] Microchip IOC Configuration Software
Microchip. www.microchip.com.

[20] AN1388 PIC32 Bootloader Application Note
DS01388B. Microchip. www.microchip.com.

[21] PIC32UBL Flasher Software
Jul. 2009. Microchip. www.microchip.com.

[22] Port Message Viewer v6+ User's Guide
DS60001219. Microchip. www.microchip.com.

[23] I^2C-Bus Specification
Rev. 03. NXP (formerly a division of Philips). www.nxp.com.

[24] MCP2562 High-Speed CAN Transceiver
DS25167. Microchip. www.microchip.com.

[25] ISO 11898-5: Road vehicles - Controller area network (CAN)
Part 5: High-speed medium access unit with low-power mode. ISO 11898-5, 2007 International Organization for Standardization. www.iso.org.

[26] Local Interconnect Network (LIN) Specification
Revision 2.2: LIN Consortium. www.lin-subbus.de.

[27] PIC32 Family Reference Manual
Microchip. www.microchip.com.

[28] UDA1380 Stereo Audio CODEC Data Sheet
NXP. www.ics.nxp.com.

[29] MCP2200 USB 2.0 to UART Protocol Converter with GPIO Data Sheet
DS22228B. Microchip. www.microchip.com.

[30] ISO 7637-2: Road vehicles - Electrical disturbances from conduction and coupling
Part 2: Electrical transient conduction along supply lines only. ISO 7637-2, May 2004, International Organization for Standardization. www.iso.org.

APPENDIX G: USER'S GUIDE REVISION HISTORY

G.1 Current Document Revision

Revision B (DS60001267B - May, 2013)

- Removal of Confidential designation from document.
- Corrected typical power consumption specification in Table A-1.
- Corrected coaxial cable impedance value in Chapter 7.0.

G.2 Previous Document Revision

Revision A

- Initial release of the OS81110 cPHY Evaluation Board User's Guide (for the AIS14001 V1.0.0 PCB).

APPENDIX H: LIST OF FIGURES

NOTES:

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