AN2717

SAMA5D2 Dynamic Memory Implementation Guidelines

Scope

This application note provides design recommendations for SAMA5D2 series microprocessors regarding PCB layout and software settings to ensure proper device functionality with multiple SDRAM device types.

Reference Documents

- SAMA5D2 Series datasheet (Lit. No. DS60001476). Available on www.microchip.com.
- Technical Note TN-46-14: *Hardware Tips for Point-to-Point System Design Introduction* – Micron Technology Inc. Available on http://www.micron.com.
- Standard IPC-2141: *Controlled Impedance Circuit Boards and High Speed Logic Design*, 1996 – Institute for Interconnection and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062, 847-509-9700

Software Used

- IAR Embedded Workbench for ARM 7.80.1.11873
- SAM-BA 3.2.1
- Altium Designer 18.0.2

Hardware Used

- SAMA5D2-XULT (official demo kit)
- SAMA5D2-PTC-EK (official demo kit)
- MPUx-DRAMx (internal R&D board)

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1. SAMA5D2 DDR Controller Capabilities

The SAMA5D2 series MPU features a Multiport DDR-SDRAM Controller (MPDDRC).

The MPDDRC is a high-bandwidth scrambleable 16-bit or 32-bit Double Data Rate (DDR) multiport memory controller supporting up to 512-Mbyte 8-bank DDR2, DDR3, DDR3L, LPDDR1, LPDDR2 and LPDDR3 devices. Data transfers are performed through a 16/32-bit data bus on one chip select.

The controller operates with the following power supplies:

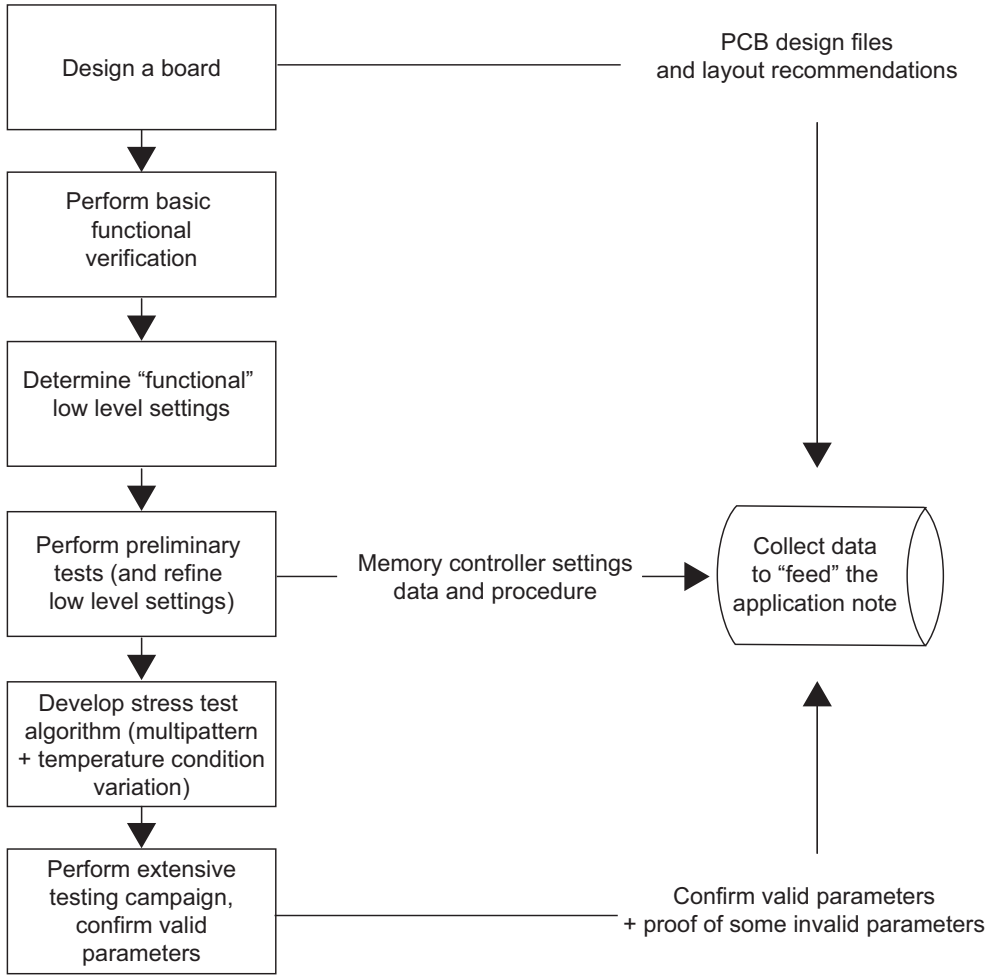
- DDR2, LPDDR1: 1.8V
- DDR3: 1.5V
- DDR3L: 1.35V
- LPDDR2, LPDDR3: 1.2V

This application note covers the implementation of the above-mentioned devices providing layout examples and software support.

2. Our Approach

The essential objective of this application note is to provide SAMA5D2 adopters with practical implementation guidelines and software settings, inferred from actual hardware and extensive tests performed on that hardware:

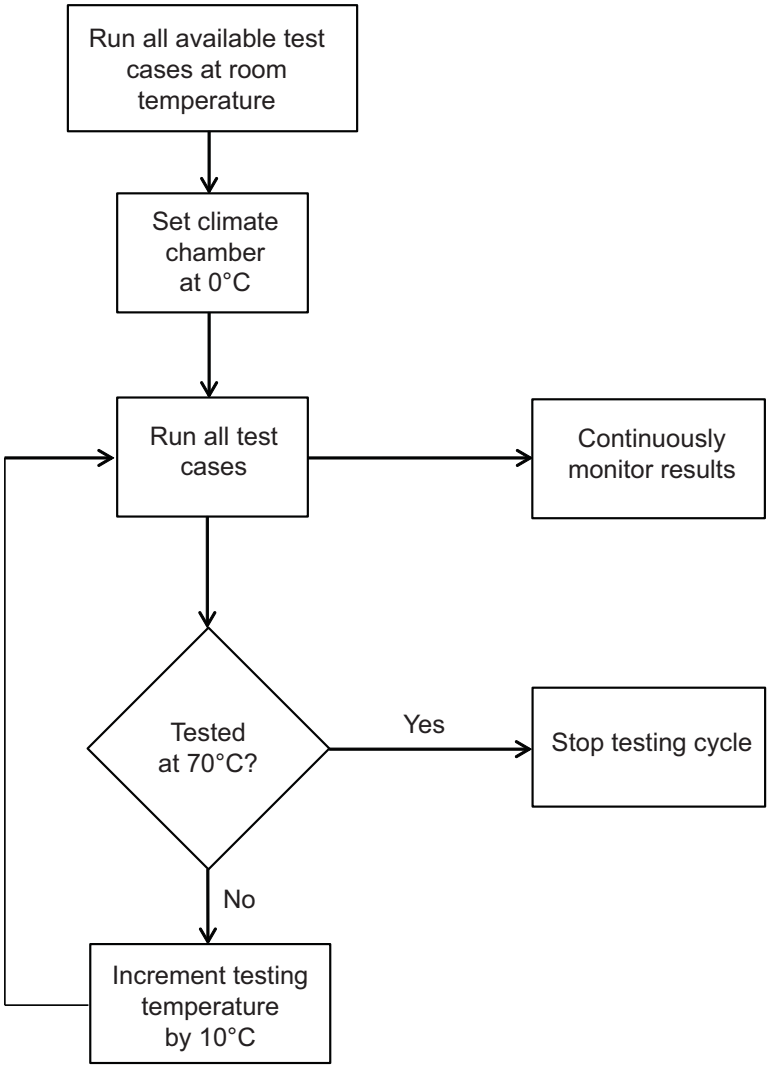
Figure 2-1. Obtaining Optimal Hardware and Software Implementation



To ensure proper functionality of all SDRAM devices supported by the external memory controller (MPDDRC), numerous hardware and software considerations must be taken into account. While low speed circuits have few physical constraints on the PCB, circuits featuring high speed signals do have constraints that must be applied regarding trace length, width and clearance, PCB stacking and length matching. These rules were applied when designing previously released development kits like SAMA5D2-XULT and SAMA5D2-PTC-EK. In addition, a custom board has been designed and produced for the purpose of further testing to ensure proper compatibility of SAMA5D2 MPUs with all supported SDRAM devices, from different manufacturers.

Apart from the boards, several pieces of testing software were developed. See the figure below.

Figure 2-2. Stress Test Algorithm



The table below describes the testing cases.

Table 2-1. Testing Cases

Test Case No.	Description	Purpose
1	Performs pin stuck at high/low test Writes sequential data patterns	Checks data integrity
2	Generates and writes random data	Checks data mismatch, unaligned access
3	Generates and transfers large data buffers	Checks data transfers in memory via DMA controller

All SDRAM devices are tested at a clock frequency of 166 MHz (clock period is 6 ns).

Important: The board that we used for the tests was designed for use in a commercial temperature range, therefore our study is limited to the 0 to +70°C range. This does in no way mean that the components involved - SAMA5D2 and DDR memory – are limited to function in that range. On the contrary, industrial grades are available and work equally well in the extended -40/+85°C range.

We performed such tests using a programmable climatic chamber.

During testing, all test results returned were logged for further analysis.

3. Hardware Aspects

Formerly released development kits containing SDRAM devices can be used as references when designing a new board. Layout examples for SDRAM implementation are provided.

Also, some general guidelines must be followed when routing such devices. Most SDRAM manufacturers provide application notes concerning high speed signal routing, usually offering minimum and recommended constraints for trace width, clearance, length matching, etc. The distances are measured in mils, the usual metric for PCB design, where 1 mil = 0.0254 mm.

The SDRAM controller interface includes:

- Four data byte lanes (see Note 1): DQS[3:0], DQSN[3:0], DQM[3:0], D[31:0]
- ADDR/CMD/CTL signals: BA[2:0], A[13:0], RAS/CAS, CS, CKE, WE, RESETN
- Clock signals: CK/CKn

Here is an exhaustive list of design guidelines for SDRAM signals, grouped by signal types (refer to Technical Note TN-46-14):

- All SDRAM signals:
  - Trace width (see Note 2) for all signals should be 4 mils minimum (0.101 mm) and nominal width should be 6 mils (0.152 mm).
  - The reference power planes must have no splits across any high-speed signal.
  - The impedance of any single-ended signal trace should be 50 ±10% Ω.
  - The impedance of any differential signal trace should be 100 ±10% Ω.
- Data lane signals recommendations:
  - Clearance between two adjacent data signals (includes D, DQS, DQM) should be 8 mils minimum and 12 mils nominal (see Note 2).
  - Signals belonging to the same data byte lane should be routed on the same layer.
  - Trace length difference between signals from the same data byte lane should not exceed 50 mils.
  - Different D byte lanes should be matched within 0.5 inch of each other.
  - DQS/DQSN signal pairs should be routed as differential signals with the length difference between traces not exceeding 20 mils.
  - The length difference between any data byte lane signal and CK/CKn should not exceed 400 mils.
- Address/Control/Clock signals recommendations (see Note 2):
  - Clearance between command/control signals should be 6 mils minimum and 15 mils nominal.
  - Clearance between address signals should be 6 mils minimum and 12 mils nominal.
  - Clearance between address/control and data signals should be at least 20 mils.
  - Clearance between clock signals of the same differential pair should be 4 mils minimum and 6 mils nominal.
  - Clearance between the differential CK/CKn signal and any other signal should be 8 mils minimum and 12 mils nominal.
  - This type of signals should be routed on the same layer.
  - CK/CKn should be routed as differential signals with the length difference between traces not exceeding 20 mils.

– The length difference between any address/control signal and CK/CKn should not exceed 200 mils.

Note:

1. A data byte lane is a group of SDRAM signals which ensures that byte-formatted data are properly transferred between the SDRAM device and controller. It features 8 data signals (D[7:0]), one data mask signal (DQM) and a pair of data strobe signals (DQS/DQSN). An 8-, 16- or 32-bit SDRAM device has one, two or four data byte lanes, respectively.
2. The trace width and clearance values from these recommendations are chosen in order to match the desired impedance of each signal trace in relation with manufacturable PCB parameters, e.g. dielectric height. Consult the PCB manufacturer to accurately optimize these values.

Refer to Micron technical note TN-46-14 “Hardware Tips for Point-to-Point System Design Introduction” for more details.

3.1 SAMA5D2-XULT Development Kit

The SAMA5D2-XULT development kit is built on a 6-layer PCB. The board features a SAMA5D27/BGA289 MPU and two 2-Gbit Micron DDR3L-SDRAM devices (Part No: MT41K128M16JT-125:K).

Figure 3-1. SAMA5D2C-XULT Development Kit

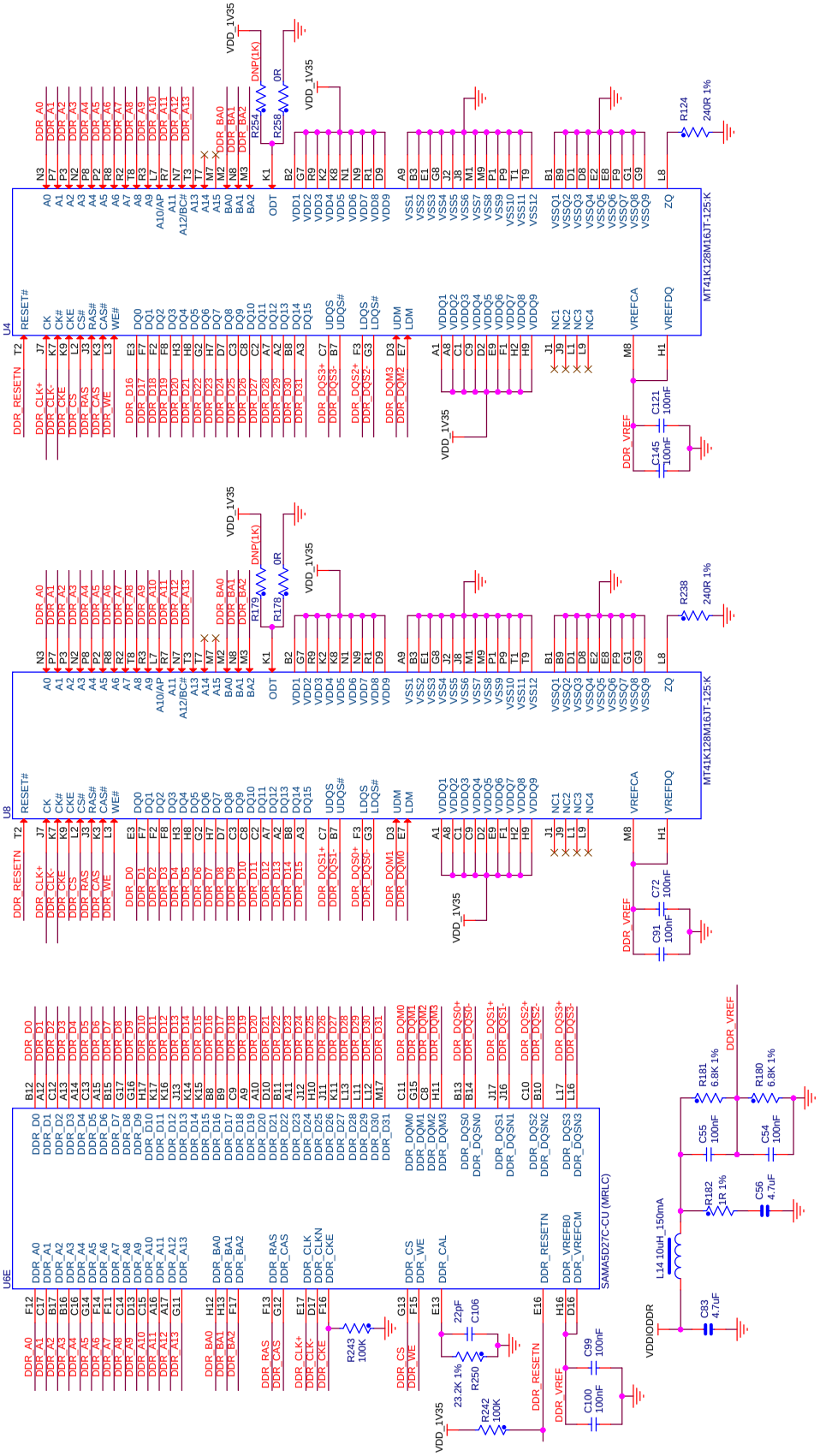
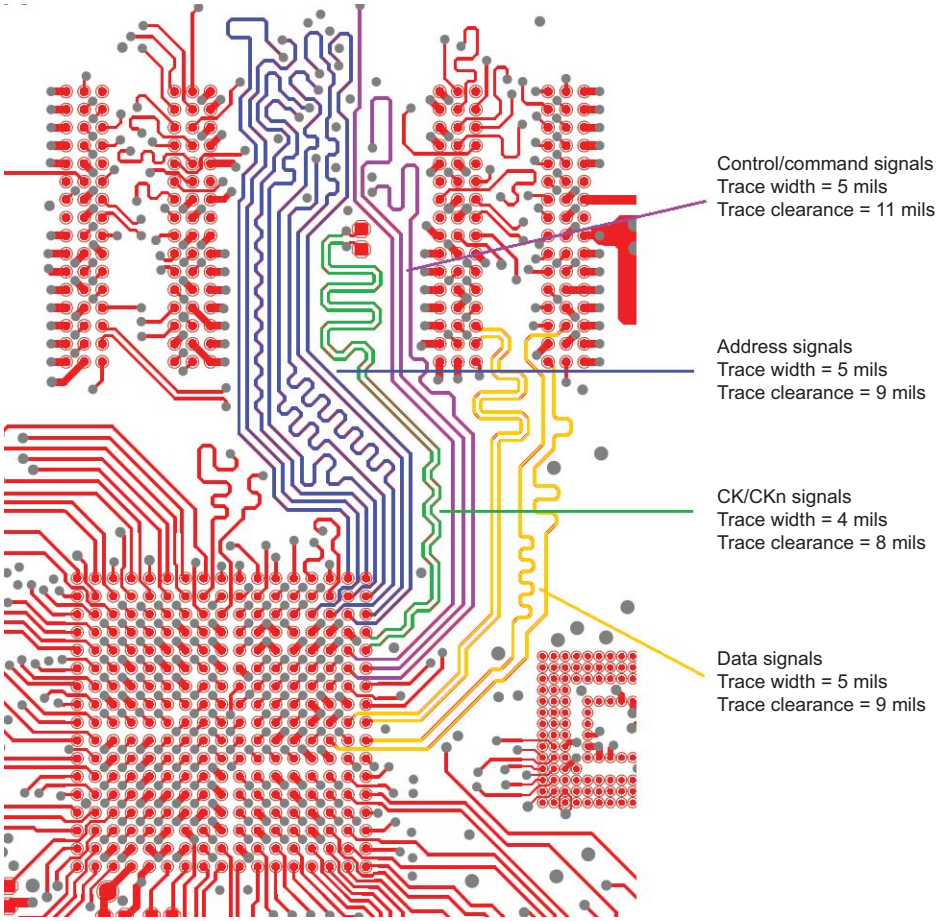
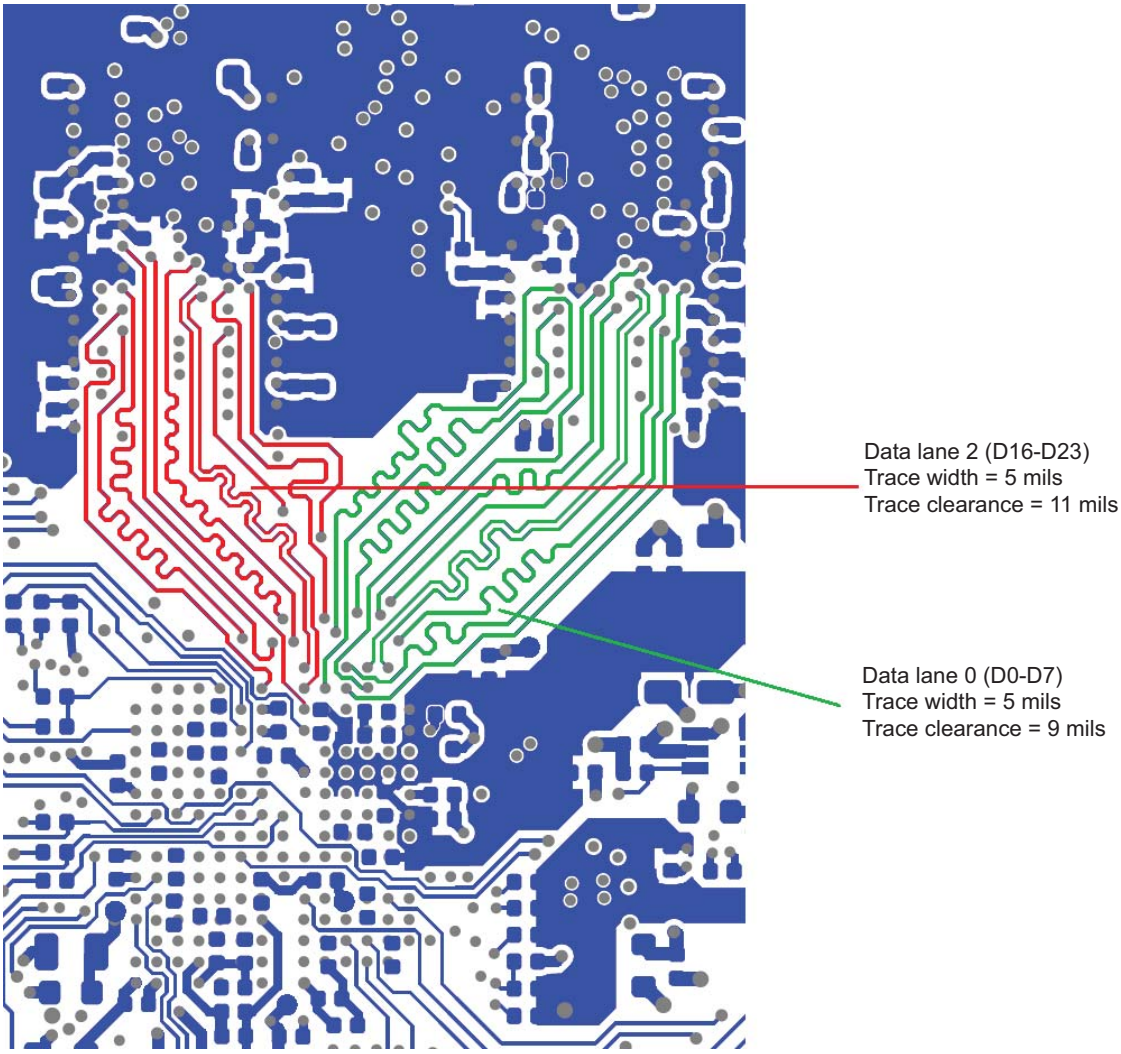


Figure 3-2. SAMA5D2-XULT Layer 1 (Top)



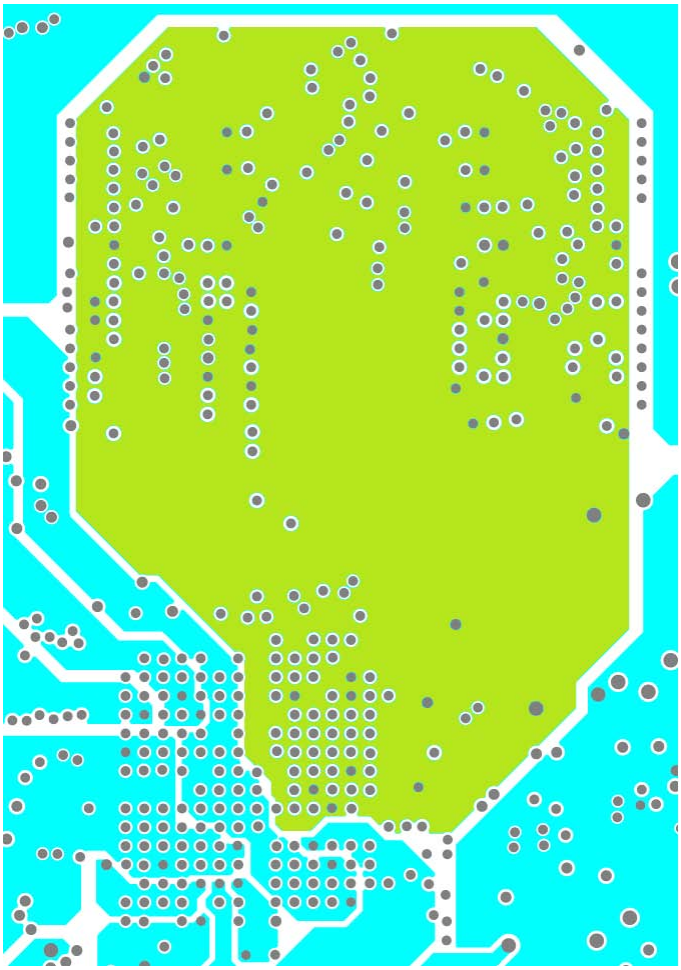
The layout example in the above figure shows the top layer of the board focused on the DDR3-SDRAM routing. Part of the address signals and the differential clock is present on the top layer, with the mentioned trace width and minimum clearance. These values are equal to or above the minimum required. There is also a 30 mils clearance between the control/command and data signals, above the minimum required.

Figure 3-3. SAMA5D2-XULT Layer 6 (Bottom)



The above figure shows the bottom layer of the DDR3-SDRAM layout. Signals from two data lanes are being routed on the bottom layer, belonging to data lane 2 (D16-D23) and data lane 0 (D0-D7), including their respective DQS/DQSn and DQM signals. Trace width used is 5 mils, and the smallest clearance is 9 mils, both values exceeding the minimum required. These traces are tightly matched, the maximum mismatch length not exceeding 7 mils, well below the maximum allowed.

Figure 3-4. SAMA5D2-XULT Layer 5 (VDD)



The above figure shows layer 5 of the board, used as power plane. The highlighted region covers the traces belonging to the DDR3-SDRAM routing and serves as reference plane for the impedance matching of the bottom traces. Also, it contains no splits across any high-speed signal.

The trace impedance for top or bottom layers is calculated using the impedance formula (according to Standard IPC-2141) for a microstrip line:

Equation 1

$$Z_0(\Omega)=\frac{87}{\sqrt{\varepsilon_r+1.41}}ln\left[\frac{5.98H}{(0.8W+T)}\right]$$

Where ε_r is the dielectric constant, H is the dielectric height, W is the trace width and T the trace thickness.

In our case (available in Table SAMA5D2-XULT Detailed PCB Stack-up):

- ε_r = 3.95 for FR-4 dielectric
- H = 3.8207 mils between bottom layer (layer 6) and power plane (layer 5)
- W = 5 mils width for bottom traces
- T = 1.87 mils copper thickness.

Using the above parameters, the trace impedance is calculated to be Z_0 = 51.18 Ω, covered by the ±10% tolerance.

Figure 3-5. SAMA5D2-XULT PCB Stacking

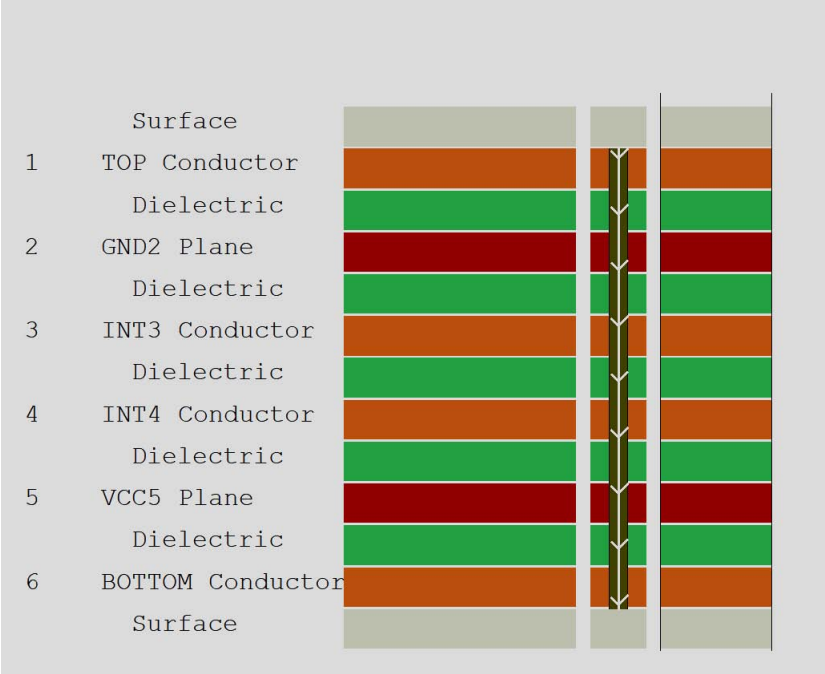


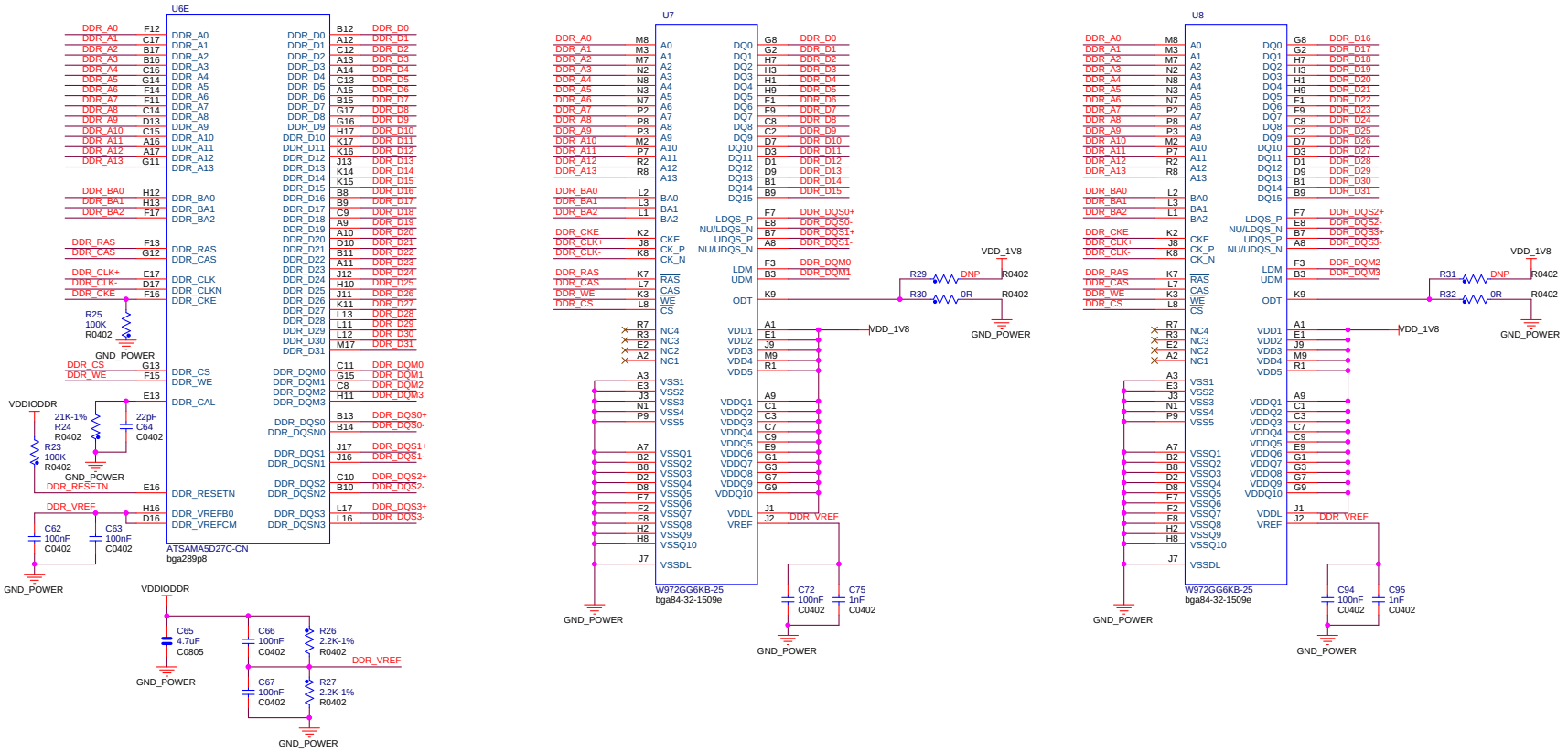
Table 3-1. SAMA5D2-XULT Detailed PCB Stack-up

Layer Name	Type	Material	Thickness [mm]	Thickness [mil]	Dielectric Material	Dielectric Constant
Top Overlay	Overlay	–	–	–	–	–
Top Solder	Solder Mask/ Coverlay	Surface Material	0.01016	0.4	Solder Resist	3.5
TOP	Signal	Copper	0.0475	1.87	–	–
Dielectric1	Dielectric	Core	0.09705	3.8207	FR-4	3.95
GND2	Signal	Copper	0.03048	1.2	–	–
Dielectric2	Dielectric	Core	0.1	3.937	FR-4	3.85
INT3	Signal	Copper	0.03048	1.2	–	–
Dielectric3	Dielectric	Core	0.93484	36.8047	FR-4	3.99
INT4	Signal	Copper	0.03048	1.2	–	–
Dielectric4	Dielectric	Core	0.1	3.937	FR-4	3.85
VCC5	Signal	Copper	0.03048	1.2	–	–
Dielectric5	Dielectric	Core	0.09705	3.8207	FR-4	3.95
BOTTOM	Signal	Copper	0.0475	1.87	–	–

Layer Name	Type	Material	Thickness [mm]	Thickness [mil]	Dielectric Material	Dielectric Constant
Bottom Solder	Solder Mask/ Coverlay	Surface Material	0.01016	0.4	Solder Resist	3.5
Bottom Overlay	Overlay	–	–	–	–	–

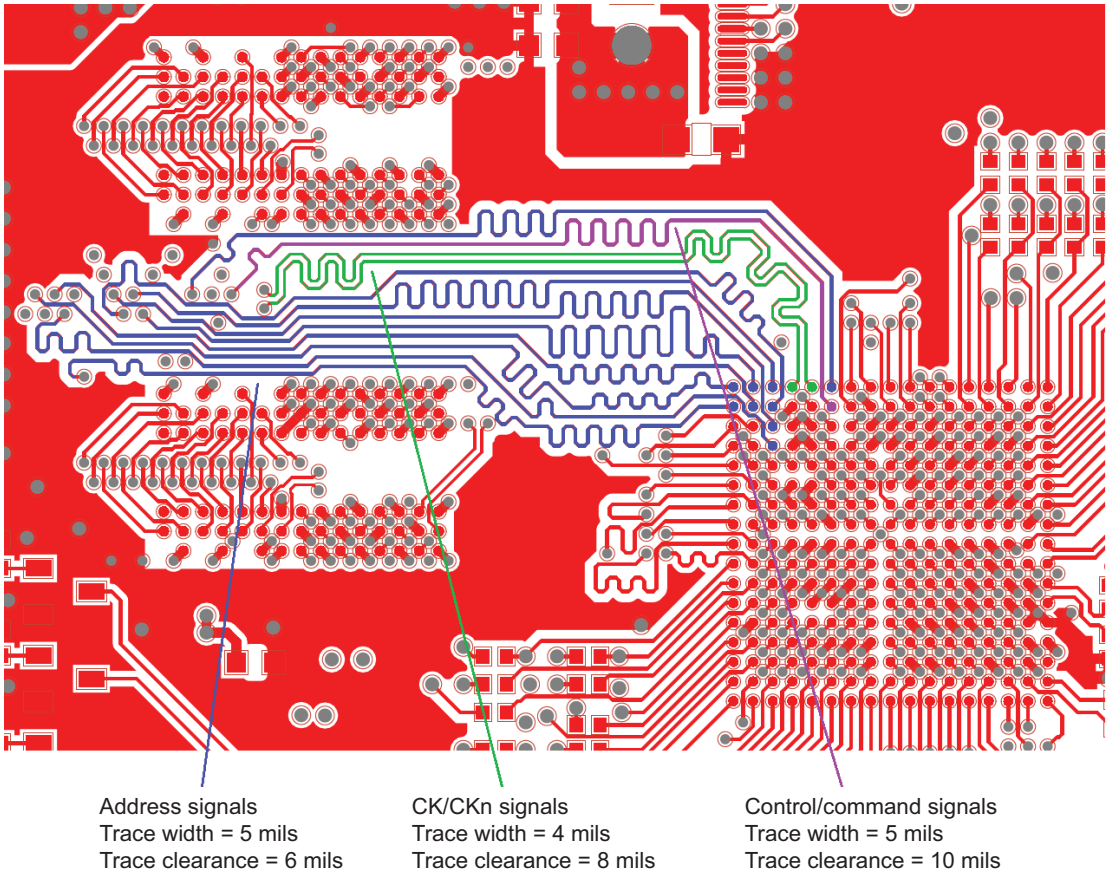
3.2 SAMA5D2-PTC-EK Development Kit

Figure 3-6. SAMA5D2-PTC-EK Development Kit



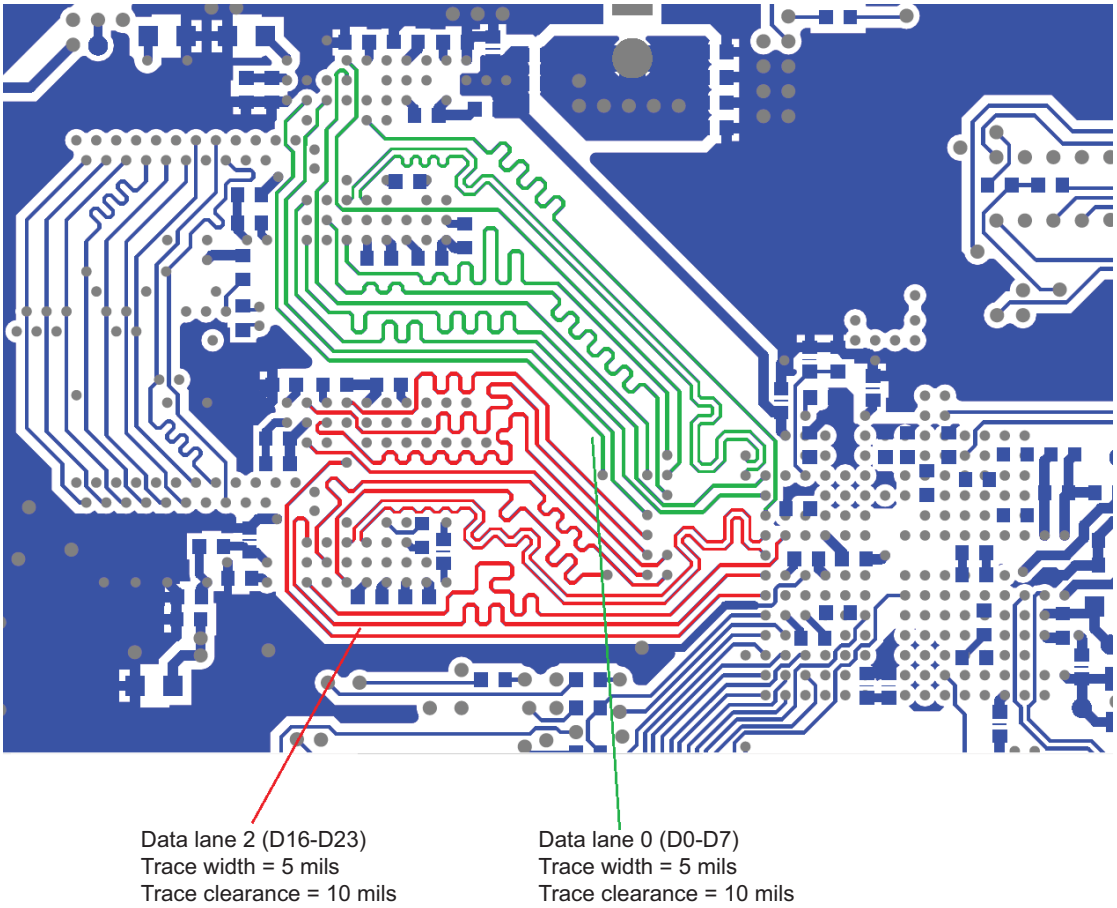
The SAMA5D2-PTC-EK is a development kit built on an 8-layer PCB. The board features a SAMA5D27/ BGA289 MPU and two 2-Gbit Winbond DDR2-SDRAM devices (Part No.: W972GG6KB-25).

Figure 3-7. SAMA5D2-PTC-EK Layer 1 (Top)



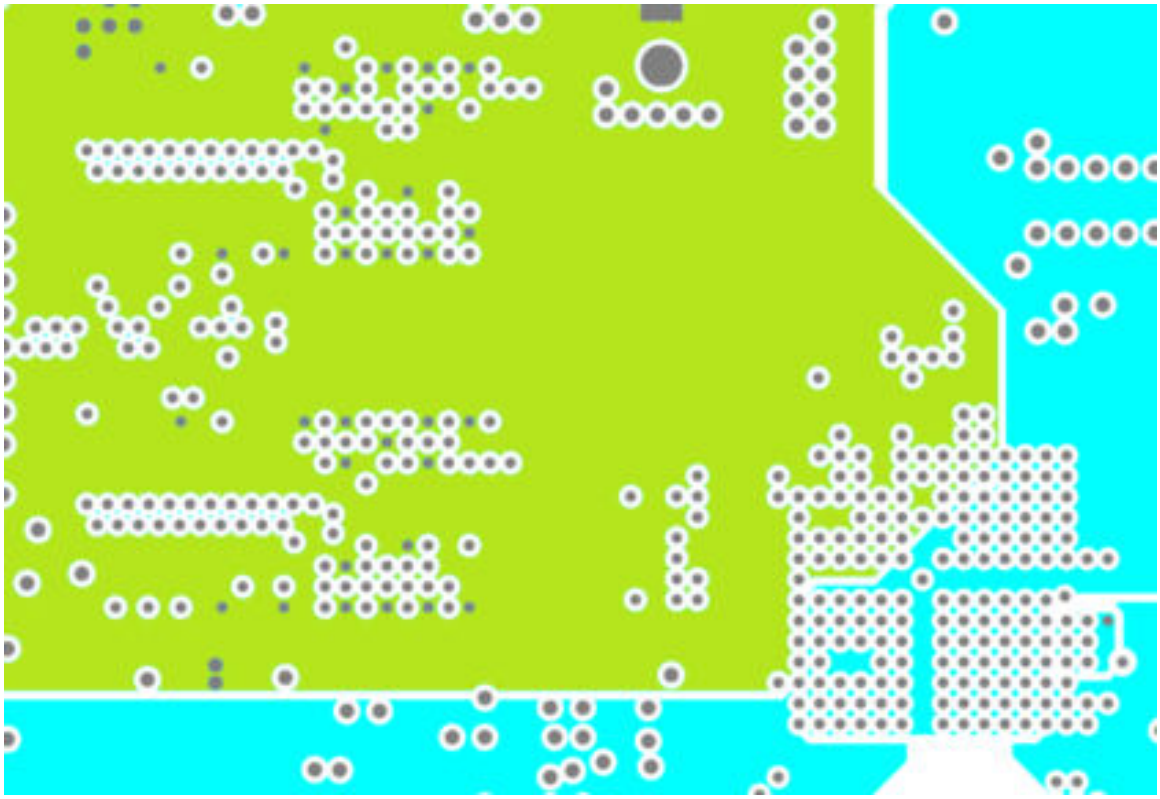
The layout example in the above figure shows the top layer of the board focused on the DDR2-SDRAM routing. Some of the address signals and the differential clock are present on the top layer, with the mentioned trace width and minimum clearance. These values are equal to or above the minimum required. There is also a 10 mils clearance between the CK/CKn signals and any other signal, above the minimum required.

Figure 3-8. SAMA5D2-PTC-EK Layer 8 (Bottom)



The layout example in the above figure shows the bottom layer of the DDR2-SDRAM layout. Signals from two data lanes are being routed on the bottom layer, belonging to data lane 2 (D16-D23) and data lane 0 (D0-D7), including their respective DQS/DQSn and DQM signals. Trace width used is 5 mils, and the clearance is 10 mils, both values exceeding the minimum required. On very short distances (typically the route a path needs to take to escape a dense BGA area), the clearance may go slightly below the minimum required. This is acceptable for dense designs only and shall be applied only if no other solution exists. These signals are also length-matched.

Figure 3-9. SAMA5D2-PTC-EK Layer 5 (VDD)



The above figure shows layer 5 of the board, used as power plane. The highlighted region covers the traces belonging to the DDR2-SDRAM routing and serves as reference plane for the impedance matching of the signals from layer 6 (see layer stack-up). Also, it contains no splits across any high-speed signal.

The trace impedance for inner layer 6 (see the figure below), which is used as signal layer, is calculated using the impedance formula (according to Standard IPC-2141) for an asymmetric stripline:

Equation 2

$$Z_0(\Omega)=\frac{80}{\sqrt{\varepsilon_r}}ln\left[\frac{1.9(2H+T)}{0.8W+T}\right]\left[1-\frac{H}{4H_1}\right]$$

Where ε_r is the dielectric constant, H1 is the dielectric height below the signal layer, H is the dielectric height above the signal layer, W is the trace width and T the trace thickness.

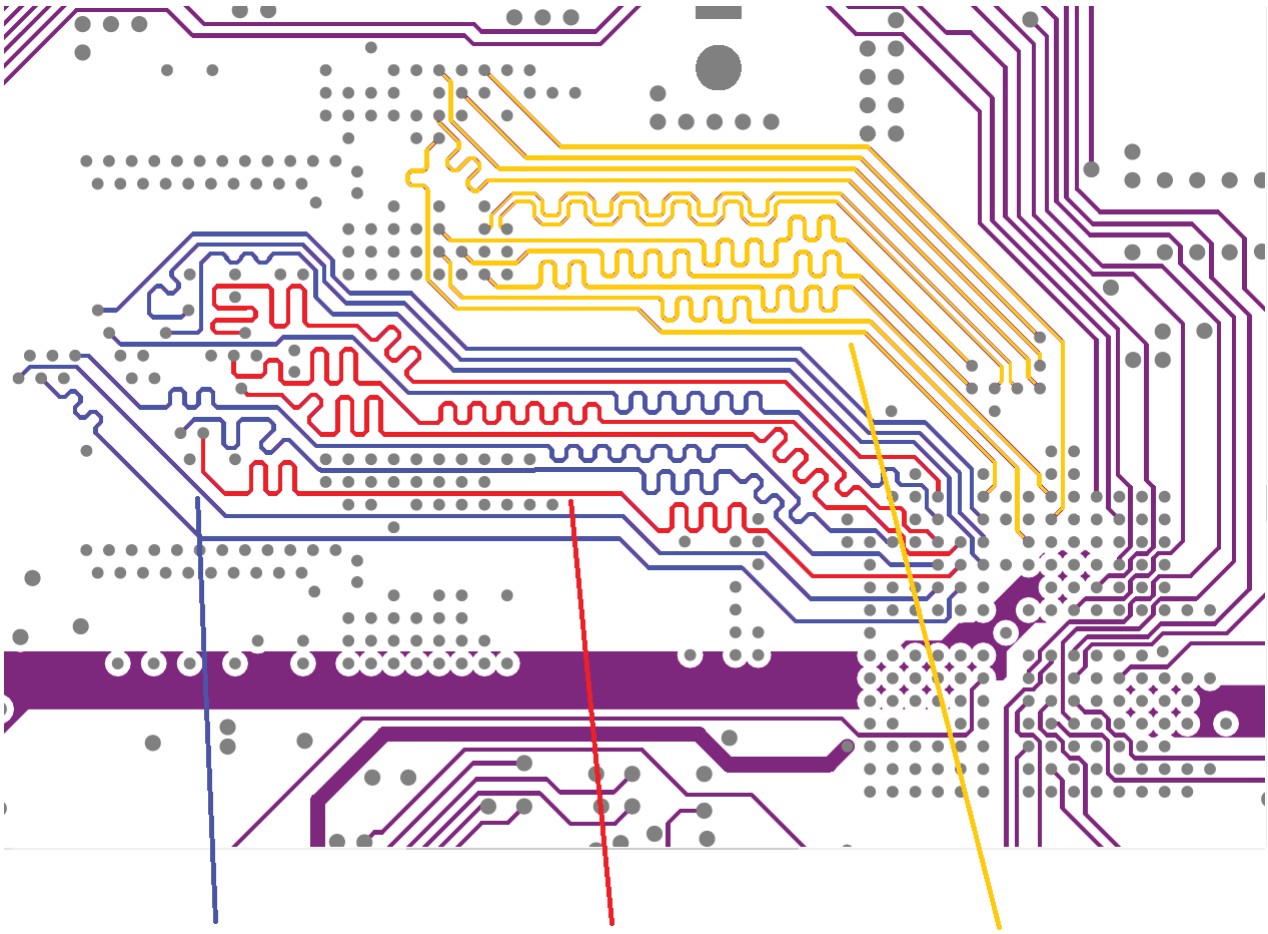
In our case (available in Table SAMA5D2-PTC-EK Detailed PCB Stack-up):

- ε_r = 4.5 for FR-4 dielectric
- H1 = 13.8 mils below layer 6
- H = 5.12 mils above layer 6
- W = 5 mils trace width
- T = 1.38 mils copper thickness.

Using the above parameters, the trace impedance is calculated to be Z0 = 48.26 Ω, covered by the ±10% tolerance.

Applying Equation 1 for traces on top or bottom layer, for the above parameters and a dielectric height H = 3.63 mils, results in a near perfect 49.92 Ω trace impedance.

Figure 3-10. SAMA5D2-PTC-EK Layer 6



All trace widths and clearances shown in the above figure are in accordance with the general design rules.

Figure 3-11. SAMA5D2-PTC-EK PCB Stacking

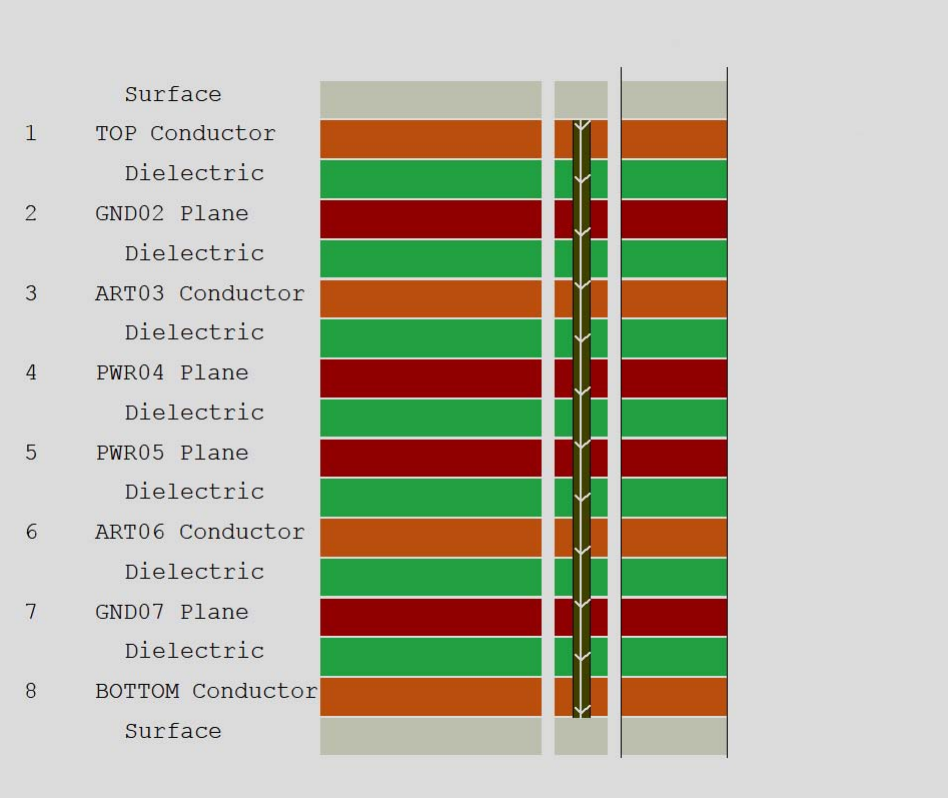


Table 3-2. SAMA5D2-PTC-EK Detailed PCB Stack-up

Layer Name	Type	Material	Thickness [mm]	Thickness [mil]	Dielectric Material	Dielectric Constant
Top Overlay	Overlay	–	–	–	–	–
Top Solder	Solder Mask/ Coverlay	Surface Material	0.01016	0.4	Solder Resist	3.5
TOP	Signal	Copper	0.035052	1.38	–	–
Dielectric1	Dielectric	Core	0.092202	3.63	FR-4	4.5
GND02	Signal	Copper	0.035052	1.38	–	–
Dielectric2	Dielectric	Core	0.130048	5.12	FR-4	4.5
ART03	Signal	Copper	0.035052	1.38	–	–
Dielectric3	Dielectric	Core	0.35052	13.8	FR-4	4.5
PWR04	Signal	Copper	0.035052	1.38	–	–
Dielectric4	Dielectric	Core	0.130048	5.12	FR-4	4.5
PWR05	Signal	Copper	0.035052	1.38	–	–
Dielectric5	Dielectric	Core	0.35052	13.8	FR-4	4.5

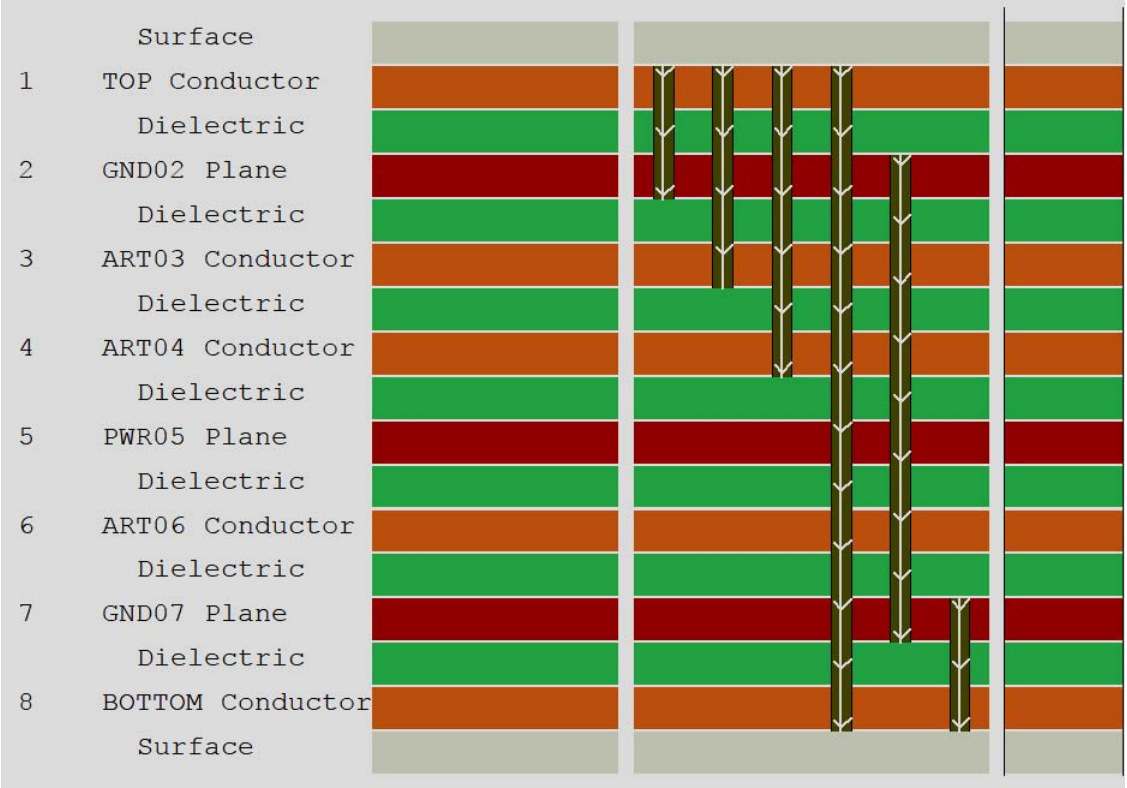
Layer Name	Type	Material	Thickness [mm]	Thickness [mil]	Dielectric Material	Dielectric Constant
ART06	Signal	Copper	0.035052	1.38	–	–
Dielectric6	Dielectric	Core	0.130048	5.12	FR-4	4.5
GND07	Signal	Copper	0.035052	1.38	–	–
Dielectric7	Dielectric	Core	0.092202	3.63	FR-4	4.5
BOTTOM	Signal	Copper	0.035052	1.38	–	–
Bottom Solder	Solder Mask/ Coverlay	Surface Material	0.01016	0.4	Solder Resist	3.5
Bottom Overlay	Overlay	–	–	–	–	–

3.3 SAMA5D24/BGA256 Custom Test Board

This is a custom board solely designed for testing multiple MPU+SDRAM configurations. It features five individual sets of SAMA5D24 MPU paired with 2xDDR3L-SDRAM, 2xDDR2-SDRAM, 2xLPDDR1-SDRAM, 2xLPDDR2-SDRAM and 1xLPDDR3-SDRAM devices. Each set has its own power management integrated circuit (PMIC).

The layer stack-up is shown in the following figure and table. Since all five sets are on the same board, they share the same stack-up.

Figure 3-12. SAMA5D24/BGA256 Custom Test Board Layer Stack-up



Notice the use of blind vias. Considering the very fine 0.4 mm ball pitch of the SAMA5D24, microvias in MPU pads were used. Large through-hole vias were not used in the fan-out of the MPU.

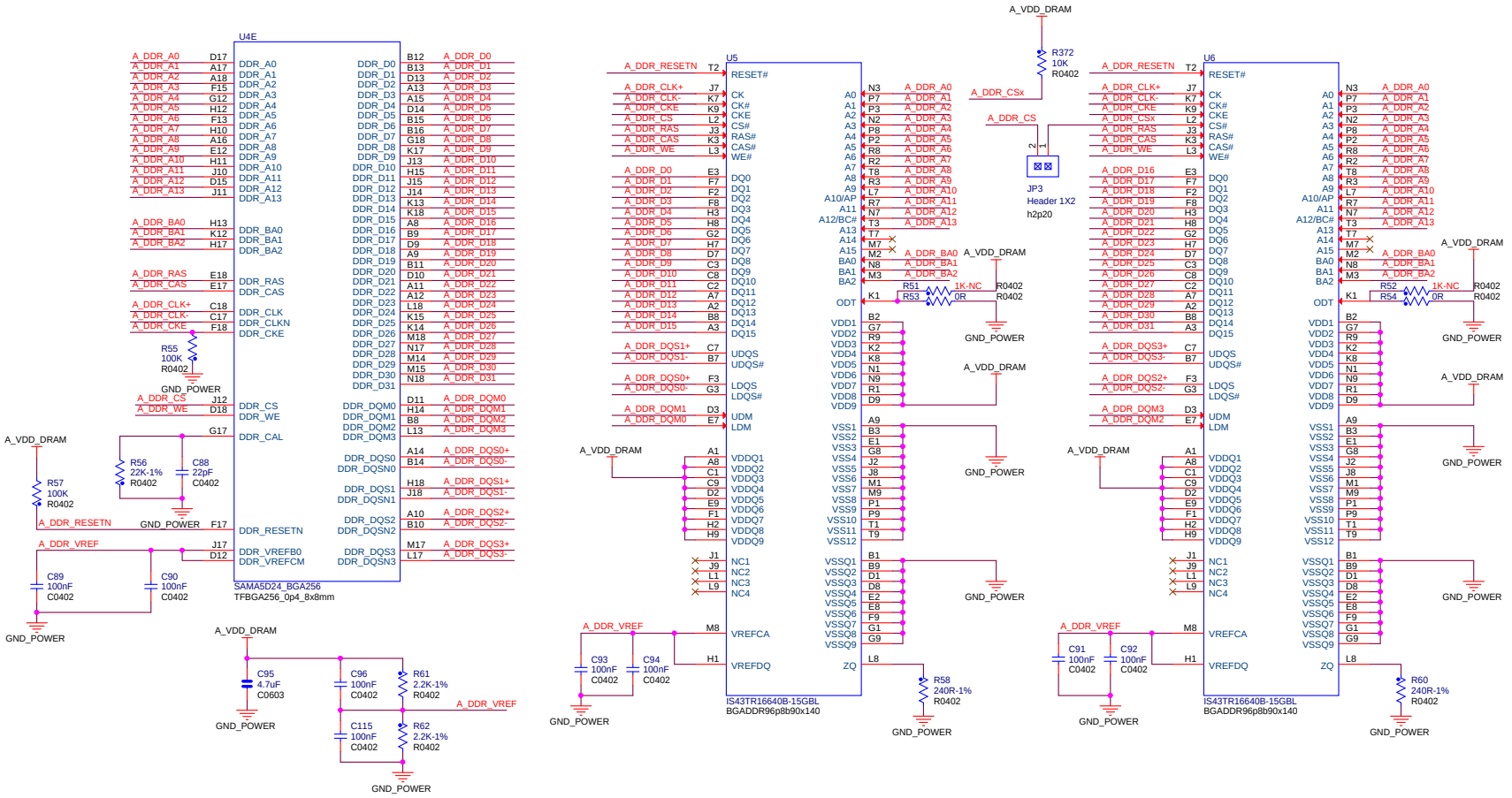
Table 3-3. Detailed Test Board Layer Stack-up

Layer Name	Type	Material	Thickness [mm]	Thickness [mil]	Dielectric Material	Dielectric Constant
Top Overlay	Overlay	–	–	–	–	–
Top Solder	Solder Mask/ Coverlay	Surface Material	0.02	0.79	Solder Resist	3.5
TOP	Signal	Copper	0.035	1.38	–	–
Dielectric1	Dielectric	Prepreg	0.105	4.13	FR-4	4.5
GND02	Signal	Copper	0.018	0.71	–	–
Dielectric2	Dielectric	Core	0.13	5.12	FR-4	4.5
ART03	Signal	Copper	0.018	0.71	–	–
Dielectric3	Dielectric	Prepreg	0.105	4.13	FR-4	4.5
ART04	Signal	Copper	0.018	0.71	–	–
Dielectric4	Dielectric	Core	0.13	5.12	FR-4	4.5
PWR05	Signal	Copper	0.018	0.71	–	–

Layer Name	Type	Material	Thickness [mm]	Thickness [mil]	Dielectric Material	Dielectric Constant
Dielectric5	Dielectric	Prepreg	0.105	4.13	FR-4	4.5
ART06	Signal	Copper	0.018	0.71	–	–
Dielectric6	Dielectric	Core	0.13	5.12	FR-4	4.5
GND07	Signal	Copper	0.018	0.71	–	–
Dielectric7	Dielectric	Prepreg	0.105	4.13	FR-4	4.5
BOTTOM	Signal	Copper	0.035	1.38	–	–
Bottom Solder	Solder Mask/ Coverlay	Surface Material	0.02	0.79	Solder Resist	3.5
Bottom Overlay	Overlay	–	–	–	–	–

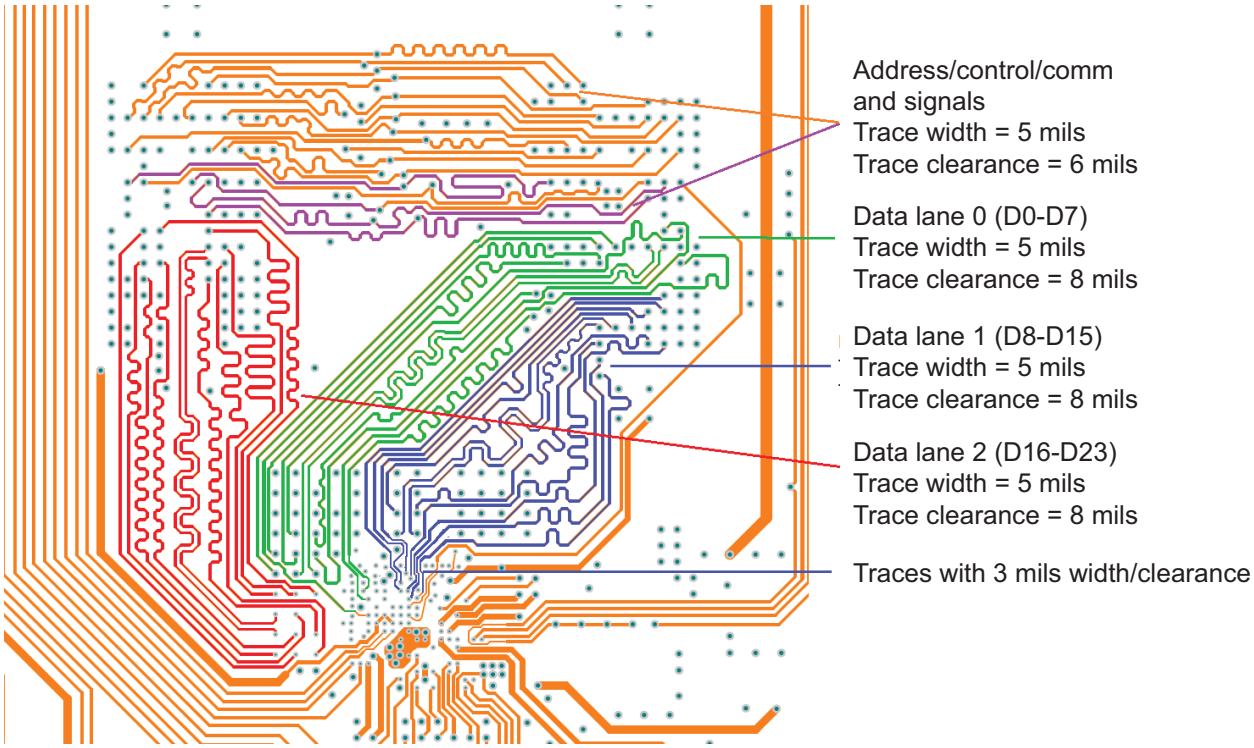
3.3.1 SAMA5D24/BGA256/DDR3L-SDRAM Devices

Figure 3-13. MPUx-DRAMX DDR3L SDRAM Device



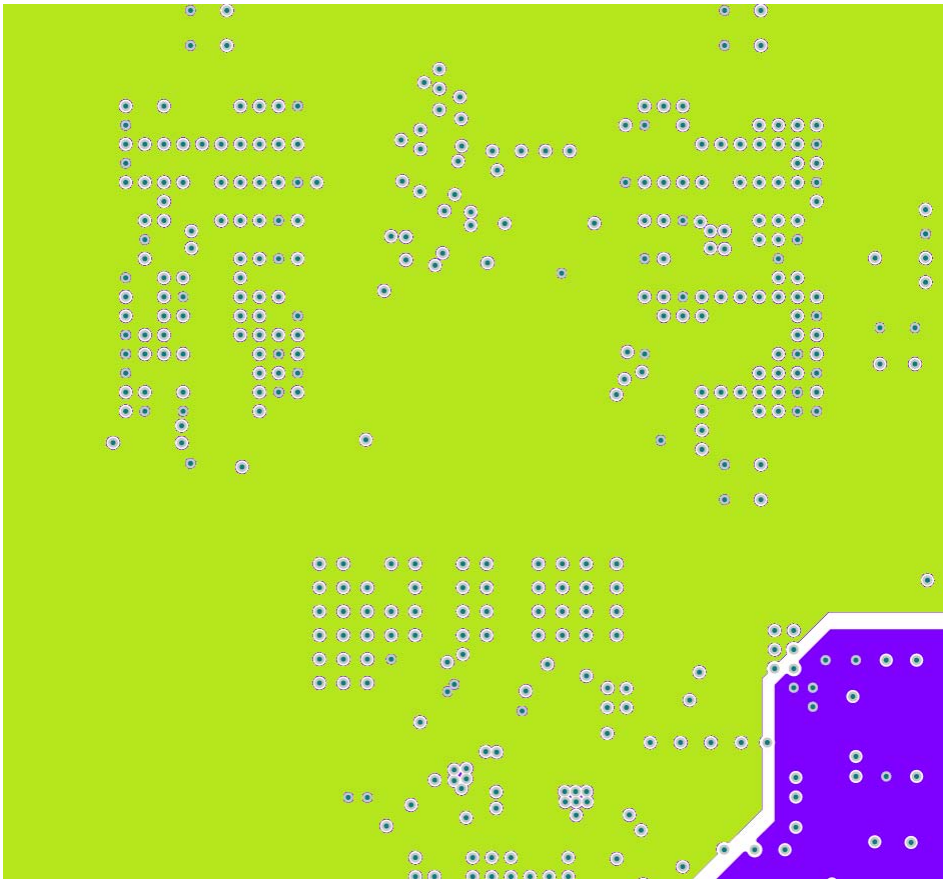
This set features a SAMA5D24/BGA256 MPU and two 1-Gbit ISSI DDR3L-SDRAM devices (Part No.: IS43TR16640B-15GBL).

Figure 3-14. SAMA5D24/BGA256/DDR3L-SDRAM Layer 3



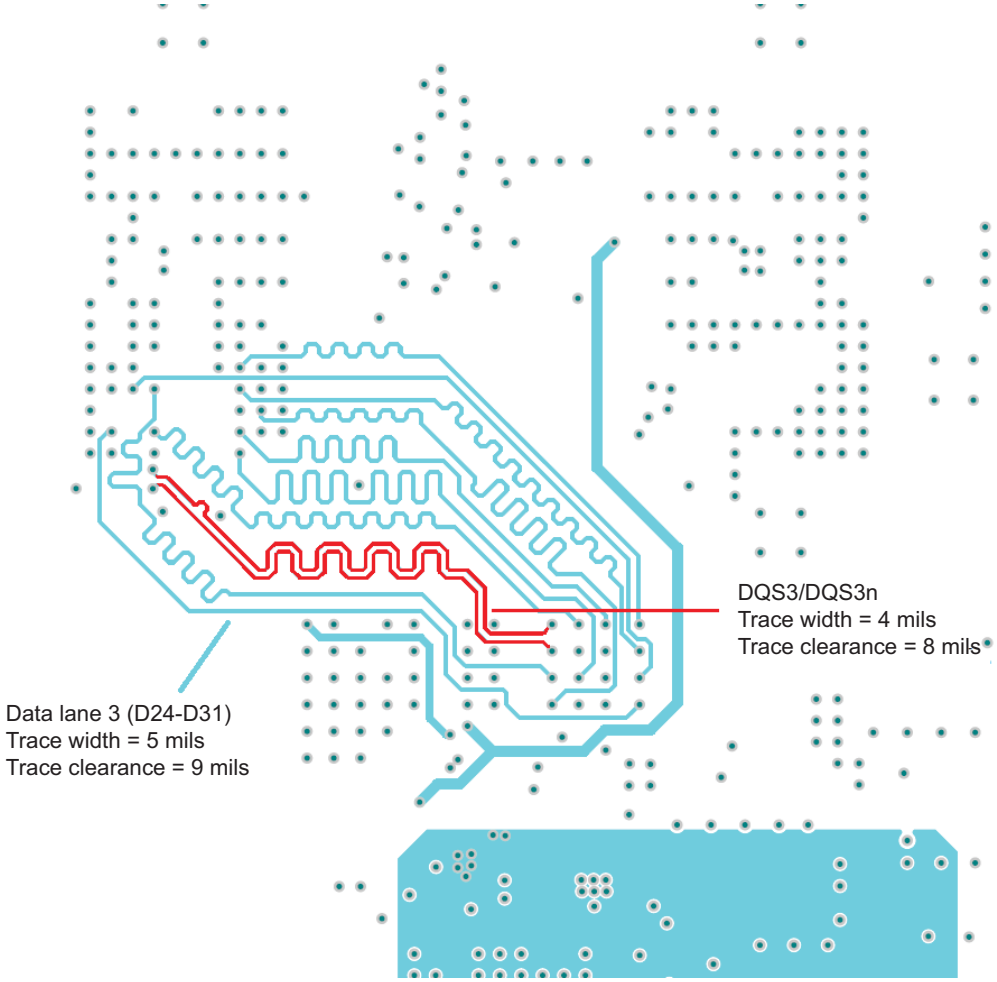
The layout example in the above figure shows layer 3 of the test board focused on the DDR3L-SDRAM configuration. It is used as a signal layer and contains traces for data lane 0..2 and address/control/command signals. Trace width and clearance are in accordance with the minimum required for most of these signals. There are, however, exceptions in the region underneath the MPU, where the 0.4 mm ball pitch does not allow routing of traces wider than 3 mils. In this case, we must violate the 4 mils minimum width rule due to physical constraints.

Figure 3-15. SAMA5D24/BGA256/DDR3L-SDRAM Layer 5



Layer 5 of the test board serves as power plane and is also used as impedance matching reference for the neighboring signal layers (layers 4 and 6). The highlighted region shown in the above figure powers the SDRAM device. It covers a large surface and it does not feature any splits over any high-speed signal, in order to ensure a good signal integrity.

Figure 3-16. SAMA5D24/BGA256/DDR3L-SDRAM Layer 6



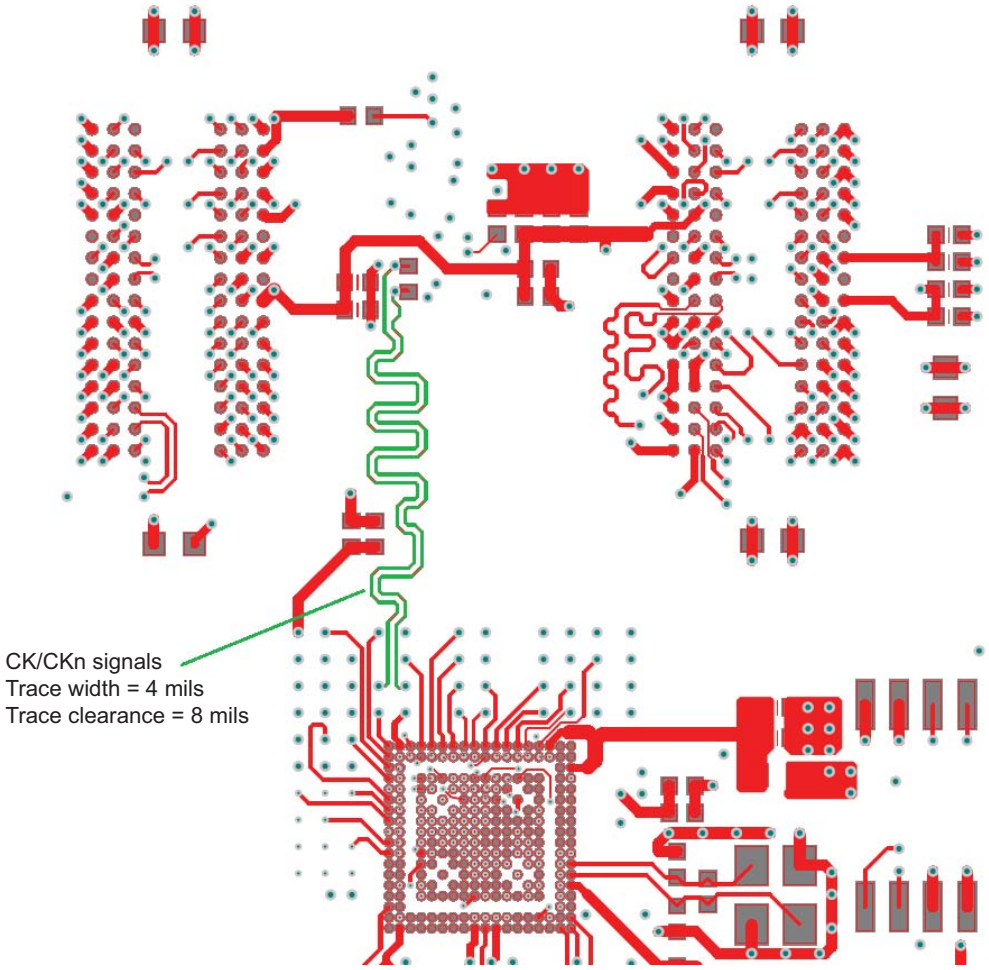
Layer 6 contains signals (see the above figure) belonging to data lane 3. All traces belonging to data lane 3 are tightly matched, with a mismatch of only 15 mils.

To calculate the trace impedance for differential signals located in inner layers, like the DQS/DQSn pair, we recommend using impedance calculators/solvers to speed up the design process. For maximum accuracy, make sure that these tools are in accordance with the IPC-2141 standard.

Using the parameters from Table Detailed Test Board Layer Stack-up, and having the trace width of 4 mils and 8 mils clearance, the trace impedance of differential pair DQS3/DQS3n is calculated to be 94.83 Ω, which is within tolerance.

In the same manner, the CK/CKn differential clock trace impedance can be calculated. The clock signal is routed on the top layer (see the figure below), has a 4 mils width, an 8 mils clearance and 4.13 mils dielectric height, resulting in a 101.73 Ω impedance.

Figure 3-17. SAMA5D24/BGA256/DDR3L-SDRAM Layer 1 (Top)



3.3.2 SAMA5D24/BGA256/DDR2-SDRAM Devices

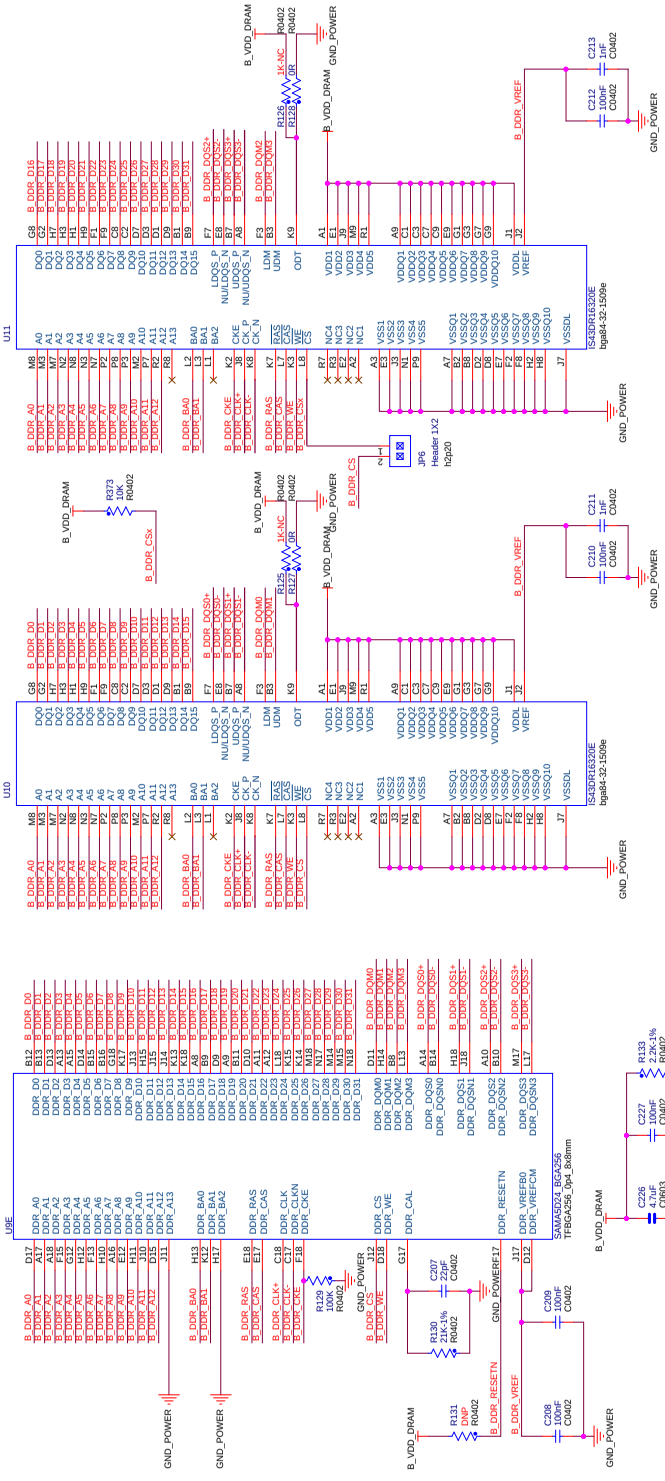
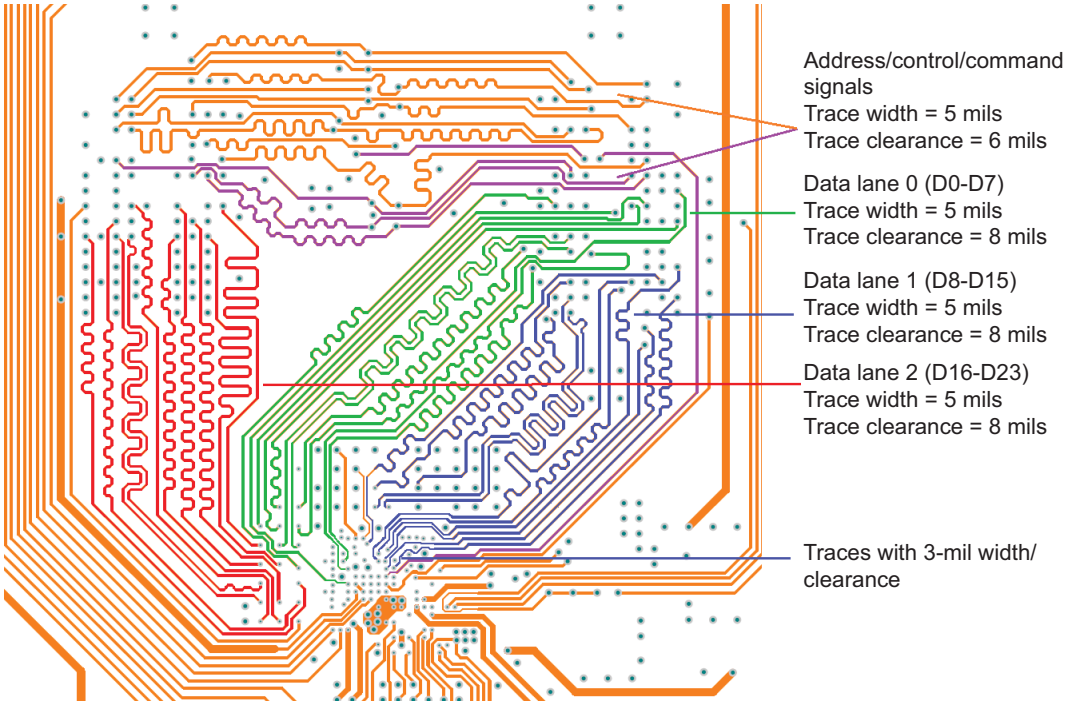


Figure 3-18. MPUx-DRAMx DDR2 Device

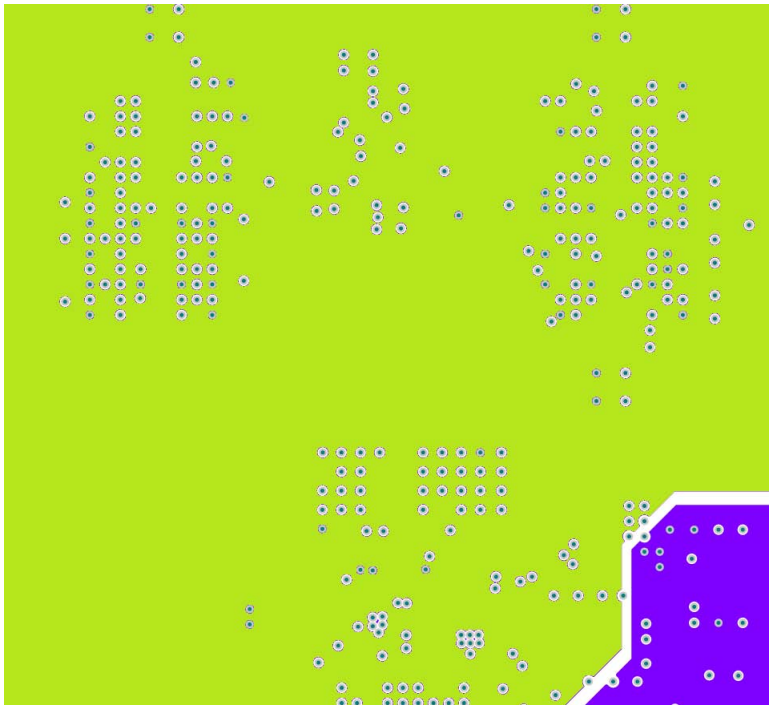
This set features a SAMA5D24/BGA256 MPU and two 512-Mbit ISSI DDR2-SDRAM devices (Part No.: IS43DR16320E-25DBL).

Figure 3-19. SAMA5D24/BGA256/DDR2-SDRAM Layer 3



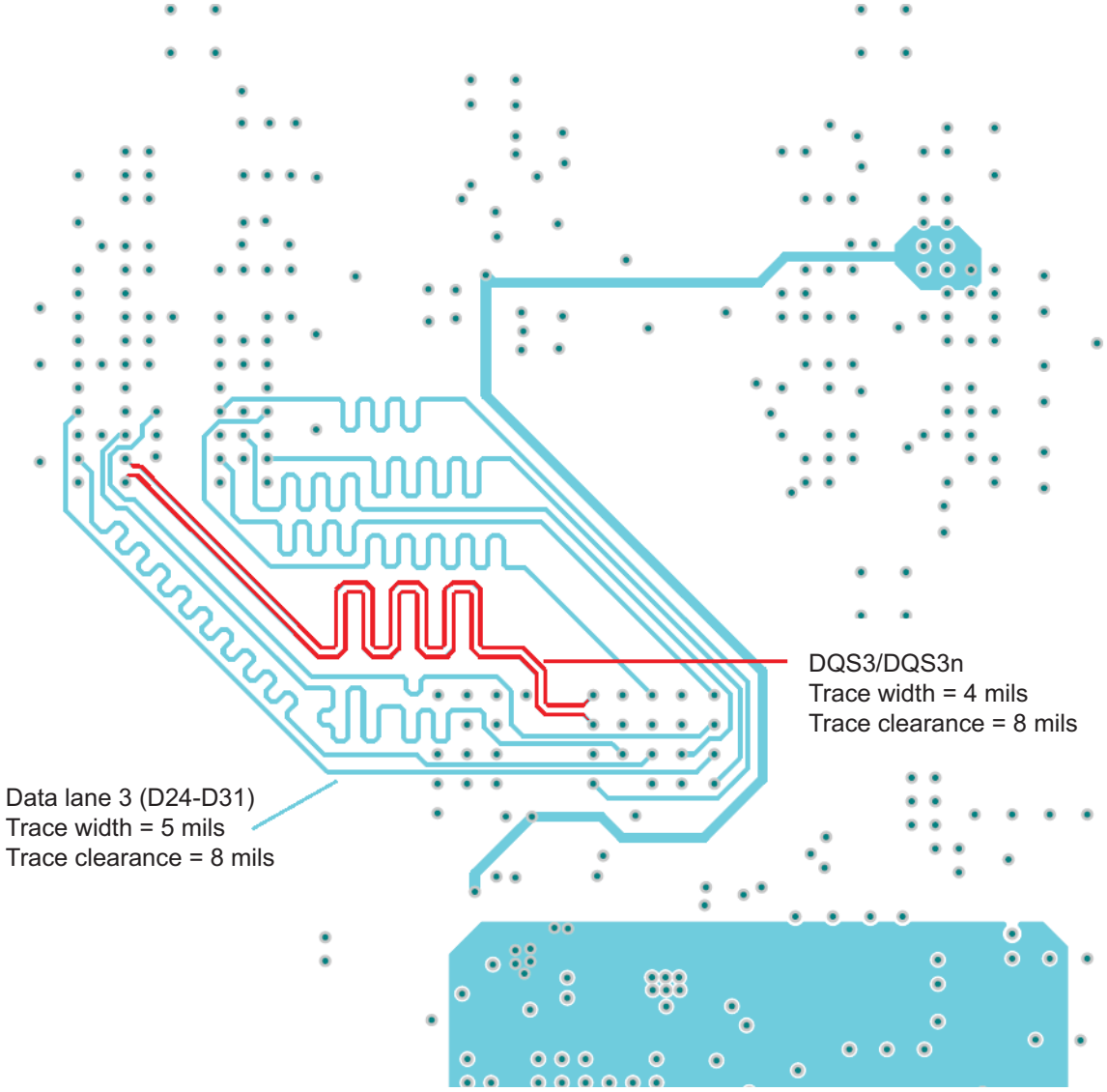
The above figure shows layer 3 of the test board focused on the DDR2-SDRAM configuration. It is used as a signal layer, contains traces for data lane 0..2 and address/control/command signals. Trace width and clearance are in accordance with the minimum required for most of these signals. There are, however, exceptions in the region underneath the MPU, where the 0.4 mm ball pitch did not allow to route traces wider than 3 mils or a larger than 3 mils clearance. In this case we must violate the 4 mils minimum width rule due to physical constraints.

Figure 3-20. SAMA5D24/BGA256/DDR2-SDRAM Layer 5



Layer 5 of the test board serves as power plane and is also used as impedance matching reference for the neighboring signal layers (layers 4 and 6). The highlighted region shown in the above figure powers the SDRAM device. It covers a large surface and it does not feature any splits over any high-speed signal, in order to ensure a good signal integrity.

Figure 3-21. SAMA5D24/BGA256/DDR2-SDRAM Layer 6



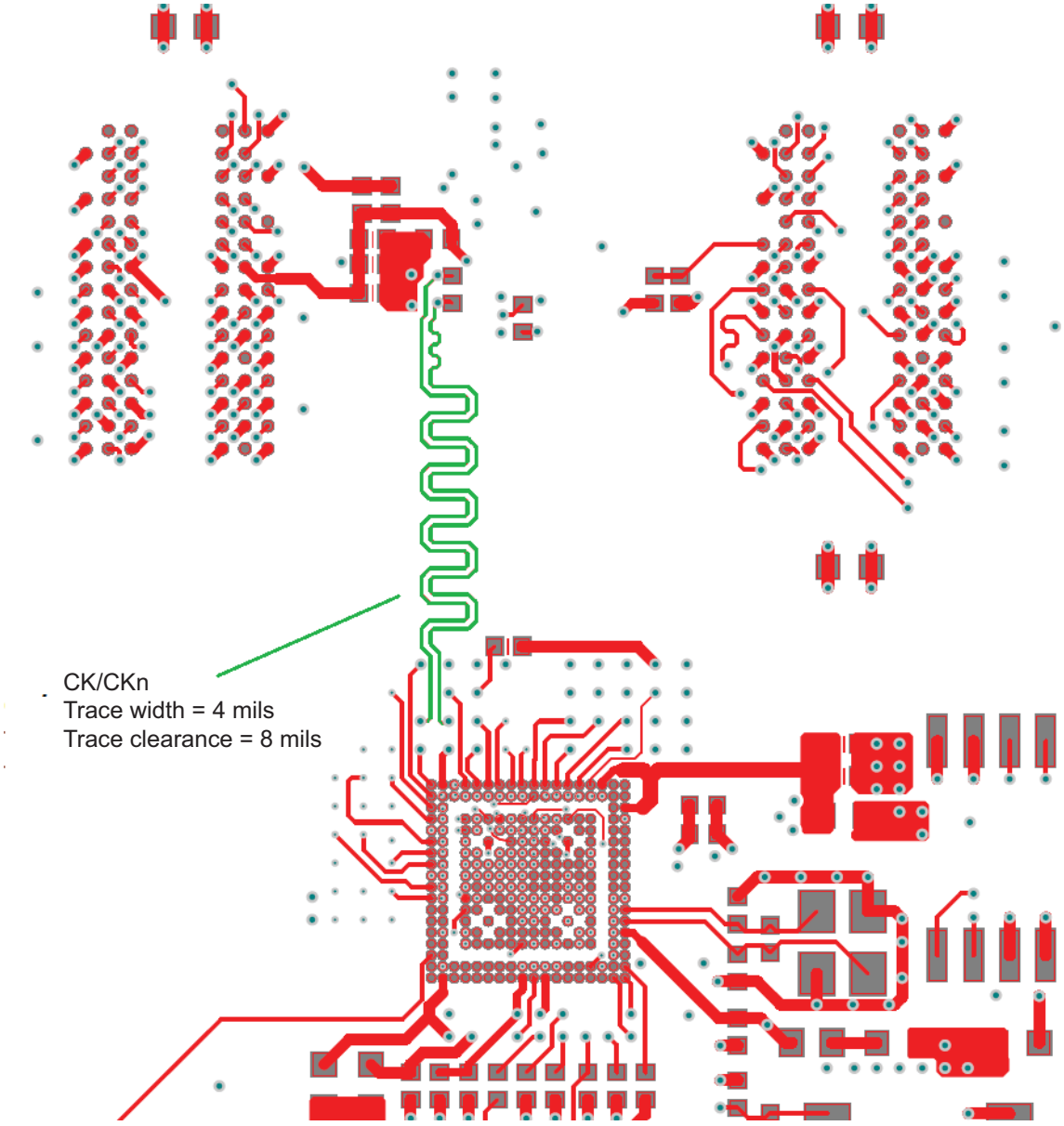
Layer 6 contains signals (see the above figure) belonging to data lane 3. All traces belonging to data lane 3 are tightly matched, with a mismatch of only 17 mils.

To calculate the trace impedance for differential signals located in inner layers, like the DQS/DQSn pair, we recommend using impedance calculators/solvers to speed up the design process. For maximum accuracy, make sure that these tools are in accordance with the IPC-2141 standard.

Using the parameters from Table Detailed Test Board Layer Stack-up, and having the trace width of 4 mils and 8 mils clearance, the trace impedance of differential pair DQS3/DQS3n is calculated to be 94.83 Ω, which is within tolerance.

In the same manner, the CK/CKn differential clock trace impedance can be calculated. The clock signal is routed on the top layer (see the figure below), has a 4 mils width, an 8 mils clearance and a 4.13 mils dielectric height, resulting in a 101.73 Ω impedance.

Figure 3-22. SAMA5D24/BGA256/DDR2-SDRAM Layer 1 (Top)



3.3.3 SAMA5D24/BGA256/LPDDR1-SDRAM Devices

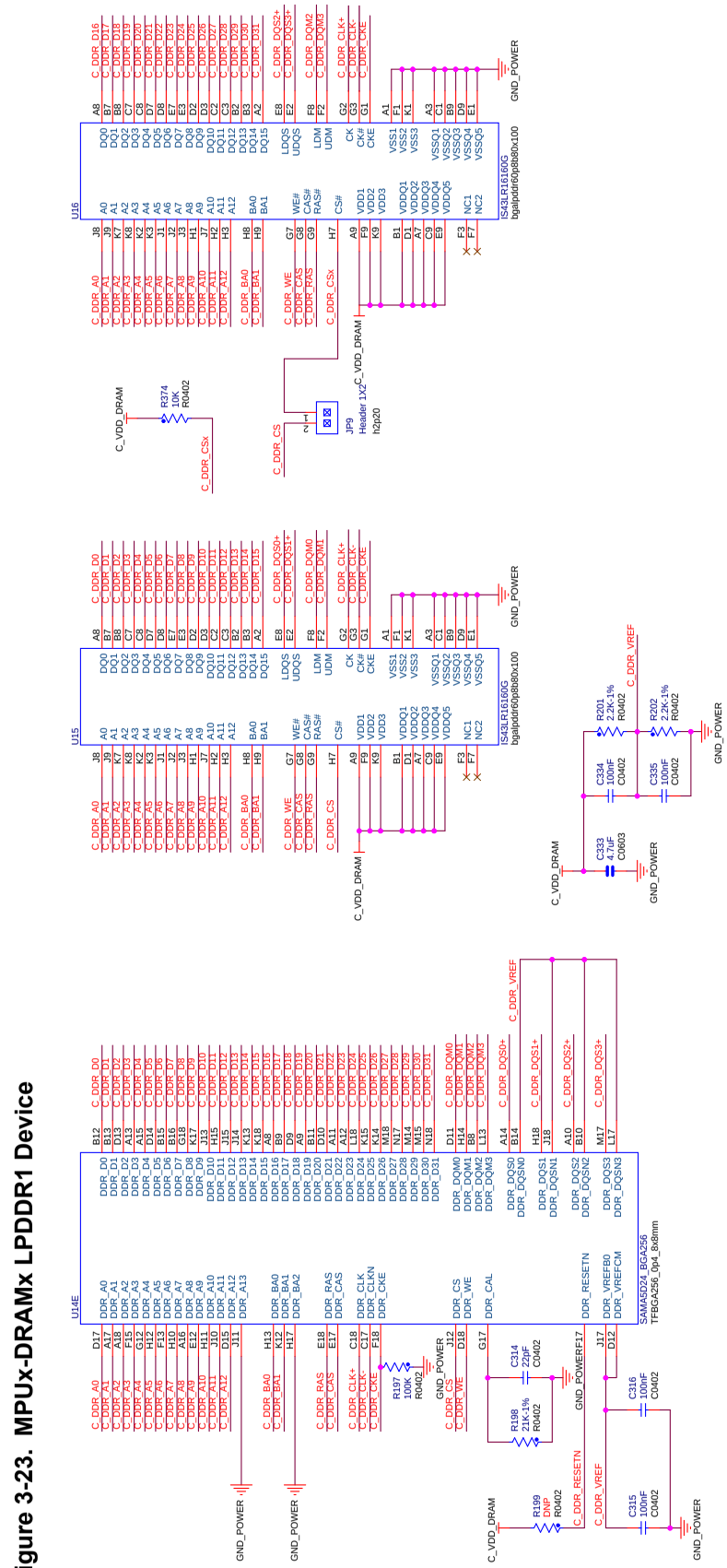
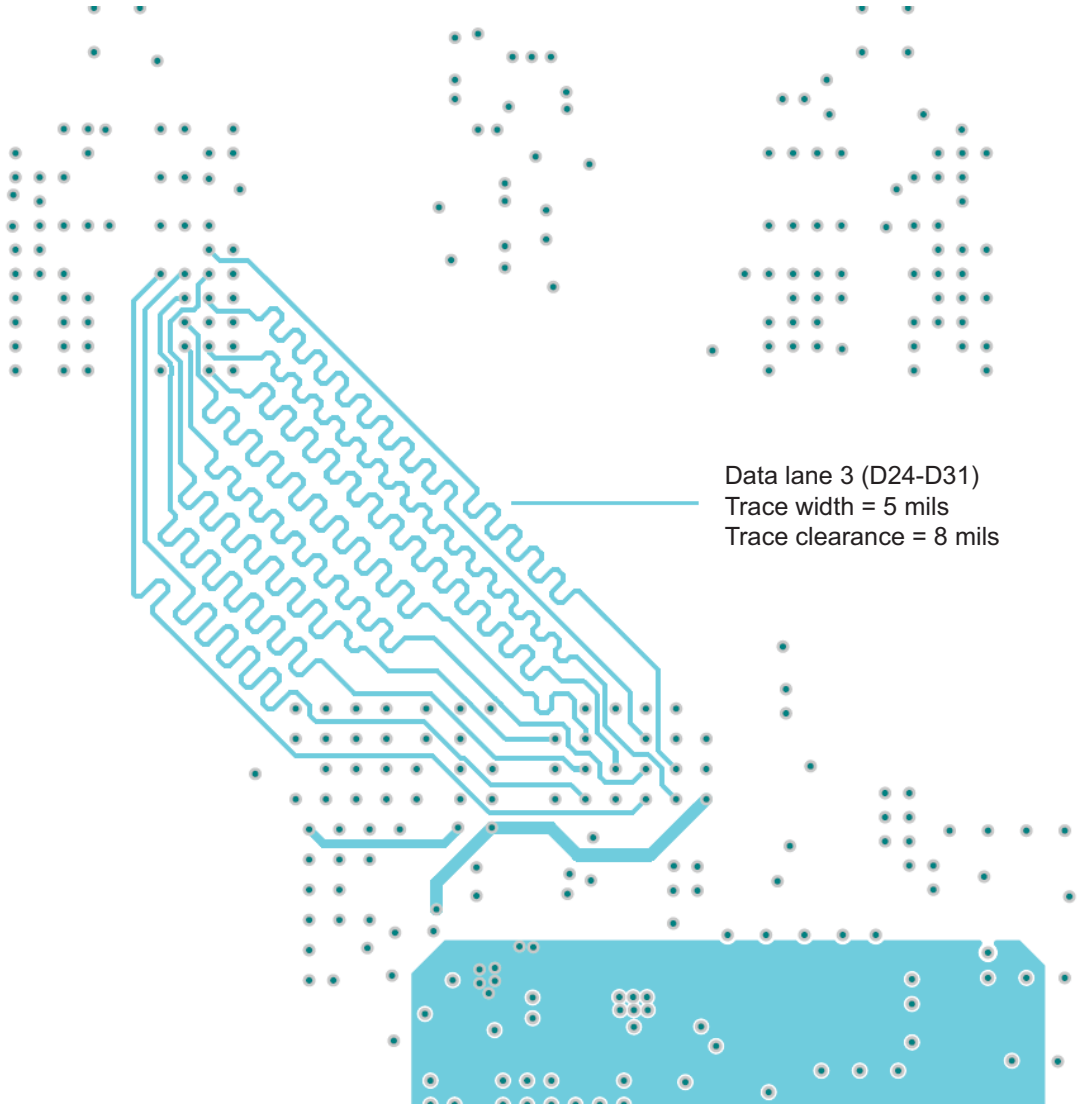


Figure 3-23. MPUx-DRAMx LPDDR1 Device

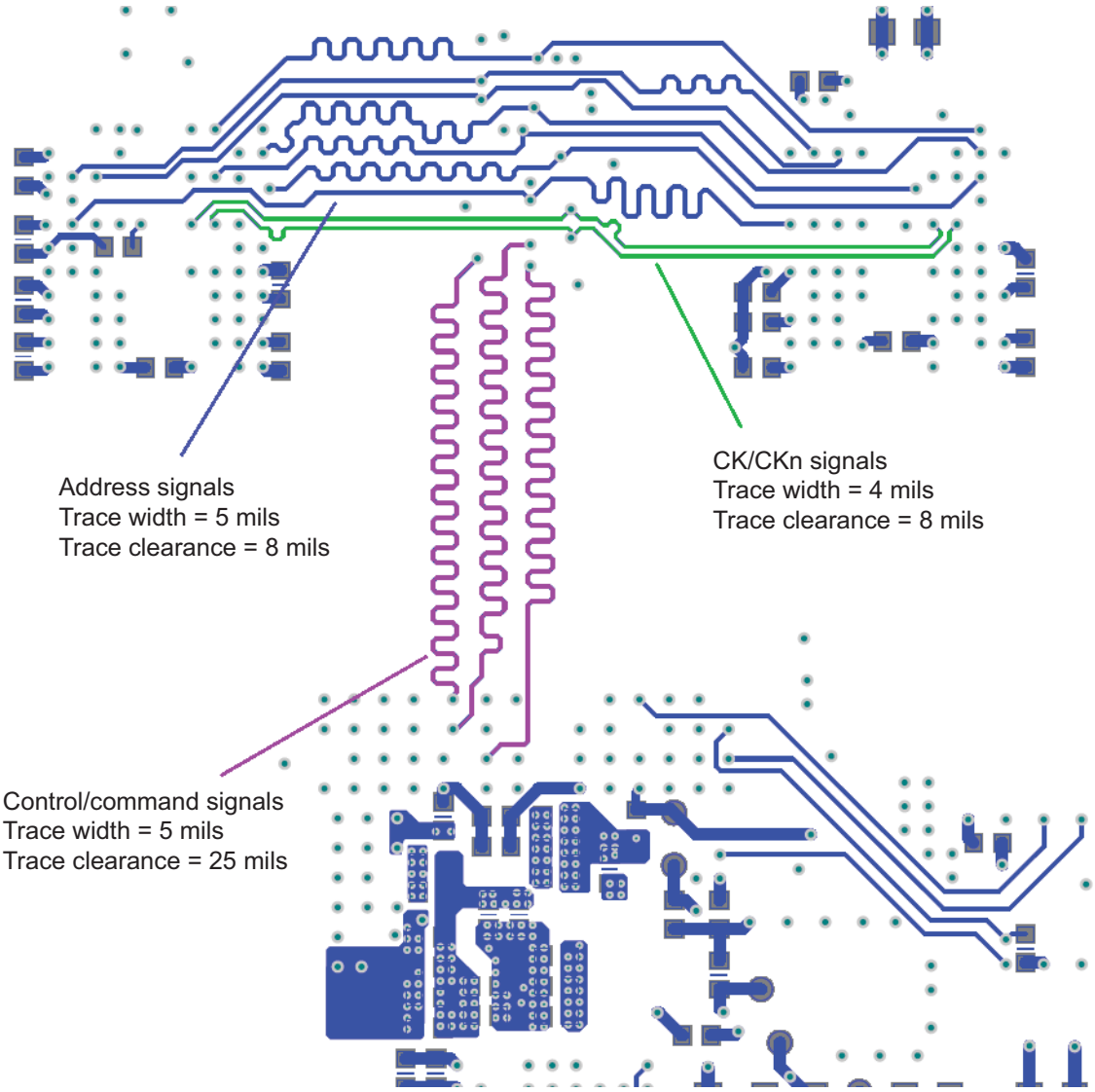
This set features a SAMA5D24/BGA256 MPU and two 256-Mbit ISSI LPDDR1-SDRAM devices (Part No.: IS43LR16160G-6BLI).

Figure 3-24. SAMA5D24/BGA256/LPDDR1-SDRAM Layer 6



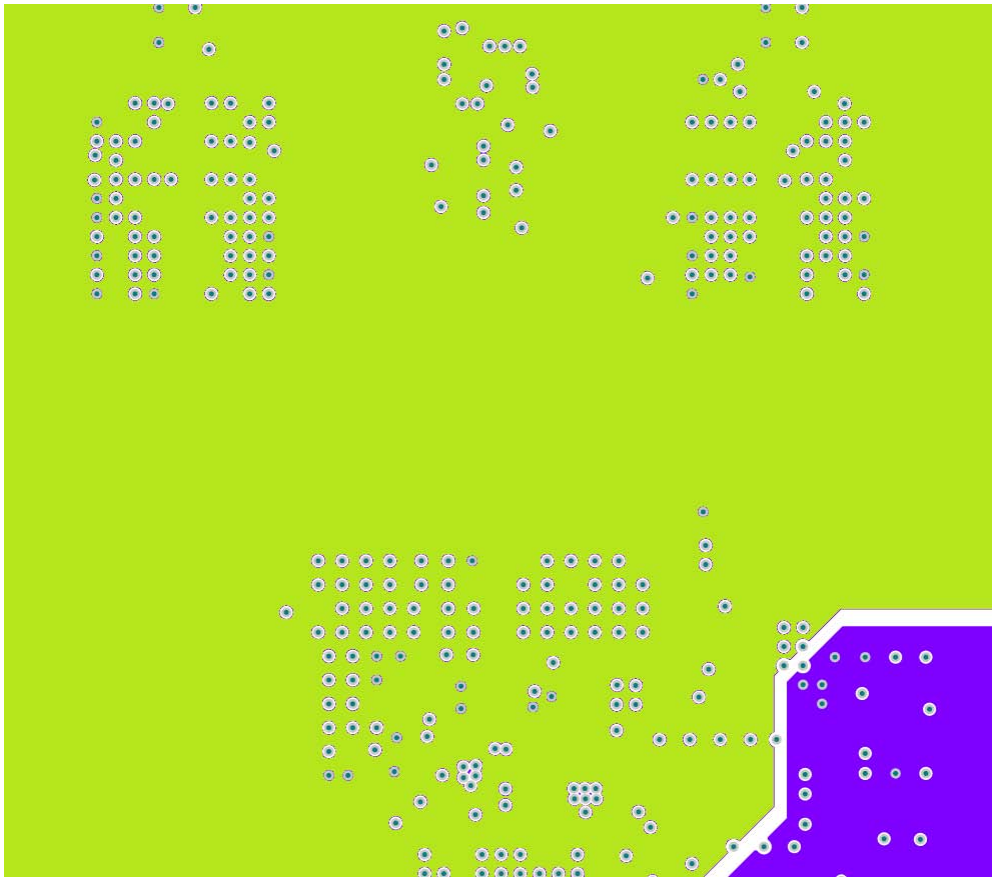
The layout example in the above figure shows layer 6 of the layout centered on the LPDDR1-SDRAM set. On this layer, the data lane 3 (D24-D31) signals have been routed, with the commented trace width and clearance, in accordance with the general routing rules. The route length mismatch within the data lane is 17 mils, well below the maximum 50 mils mismatch.

Figure 3-25. SAMA5D24/BGA256/LPDDR1-SDRAM Layer 8 (Bottom)



The above figure shows the bottom layer of the test board, centered on the LPDDR1-SDRAM device with the indicated trace width and clearance.

Figure 3-26. SAMA5D24/BGA256/LPDDR1-SDRAM Layer 5



Layer 5 of the test board serves as power plane and is also used as impedance matching reference for the neighboring signal layers (layers 4 and 6). The highlighted region shown in the above figure powers the SDRAM device. It covers a large surface and it does not feature any splits over any high-speed signal, in order to ensure a good signal integrity.

3.3.4 SAMA5D24/BGA256/LPDDR2-SDRAM Devices

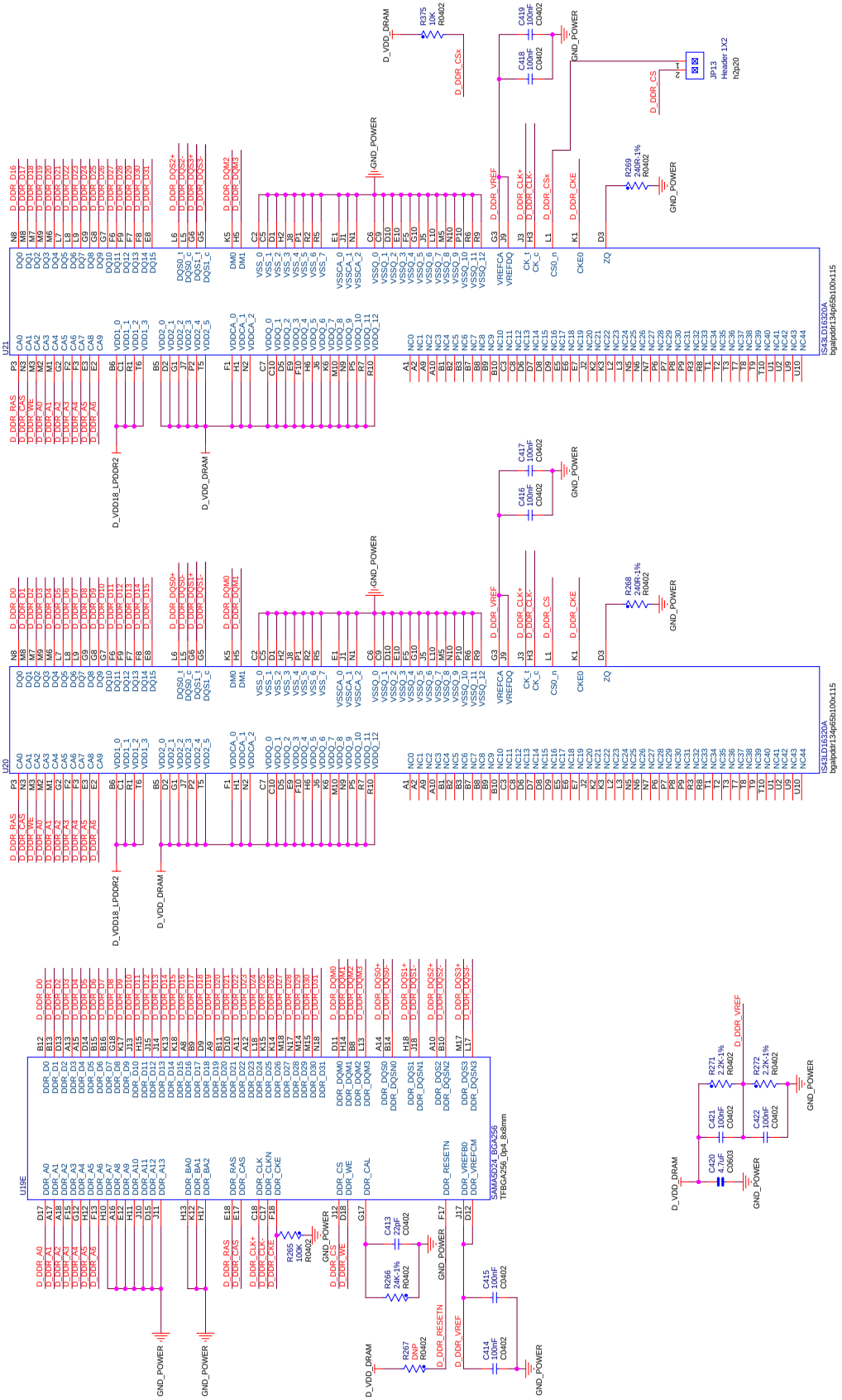
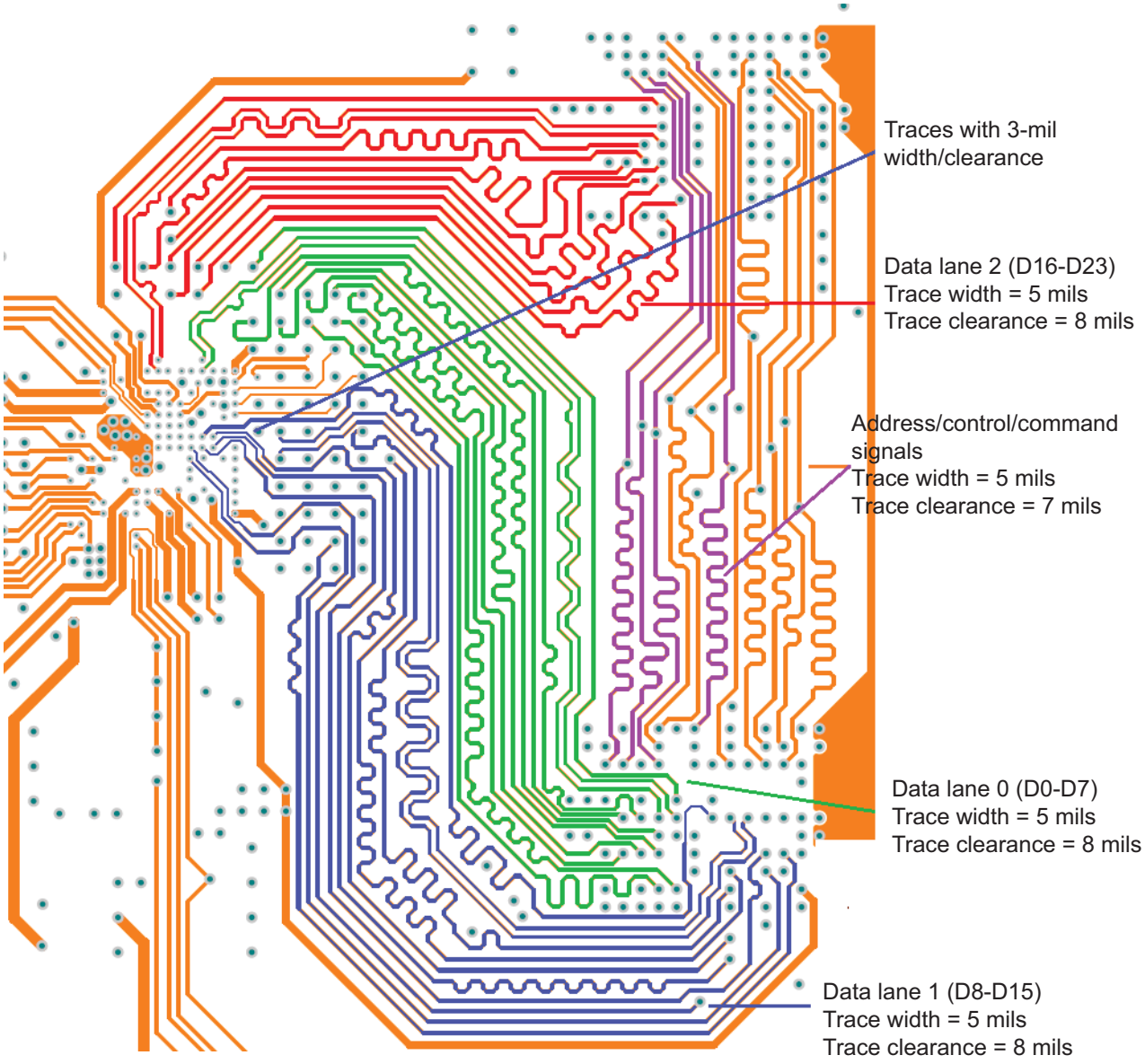


Figure 3-27. MPUx-DRAMx LPDDR2 Device

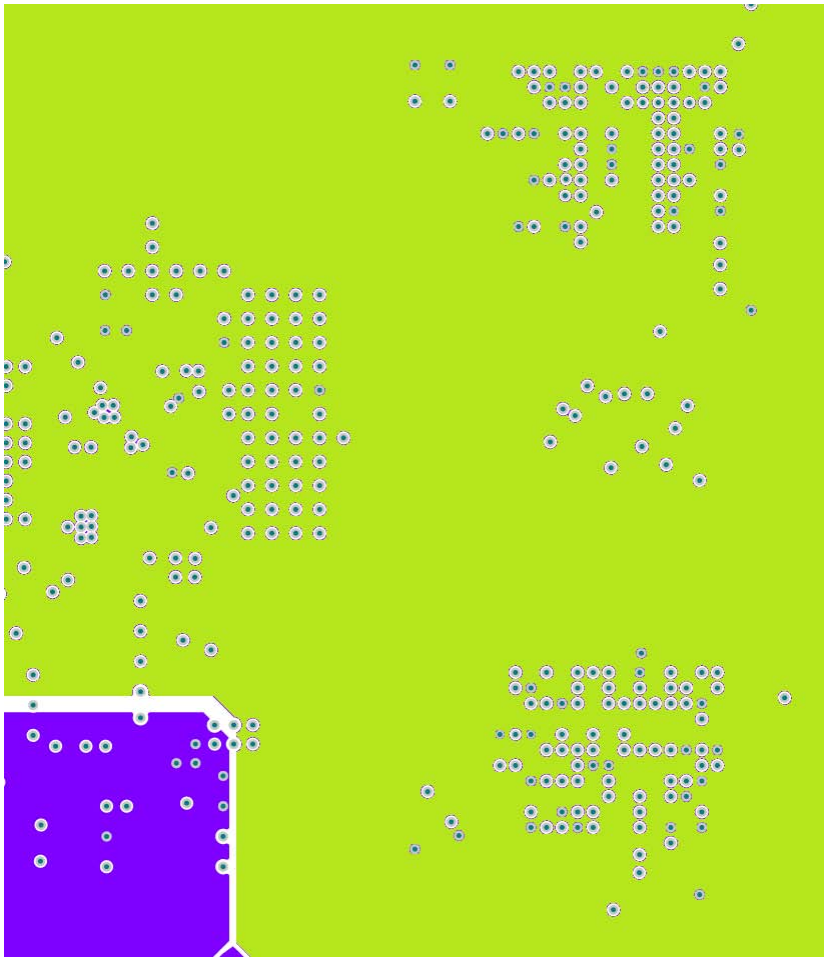
This set features a SAMA5D24/BGA256 MPU and two 512-Mbit ISSI LPDDR2-SDRAM devices (Part No.: IS43LD16320A-25BLI).

Figure 3-28. SAMA5D24/BGA256/LPDDR2-SDRAM Layer 3



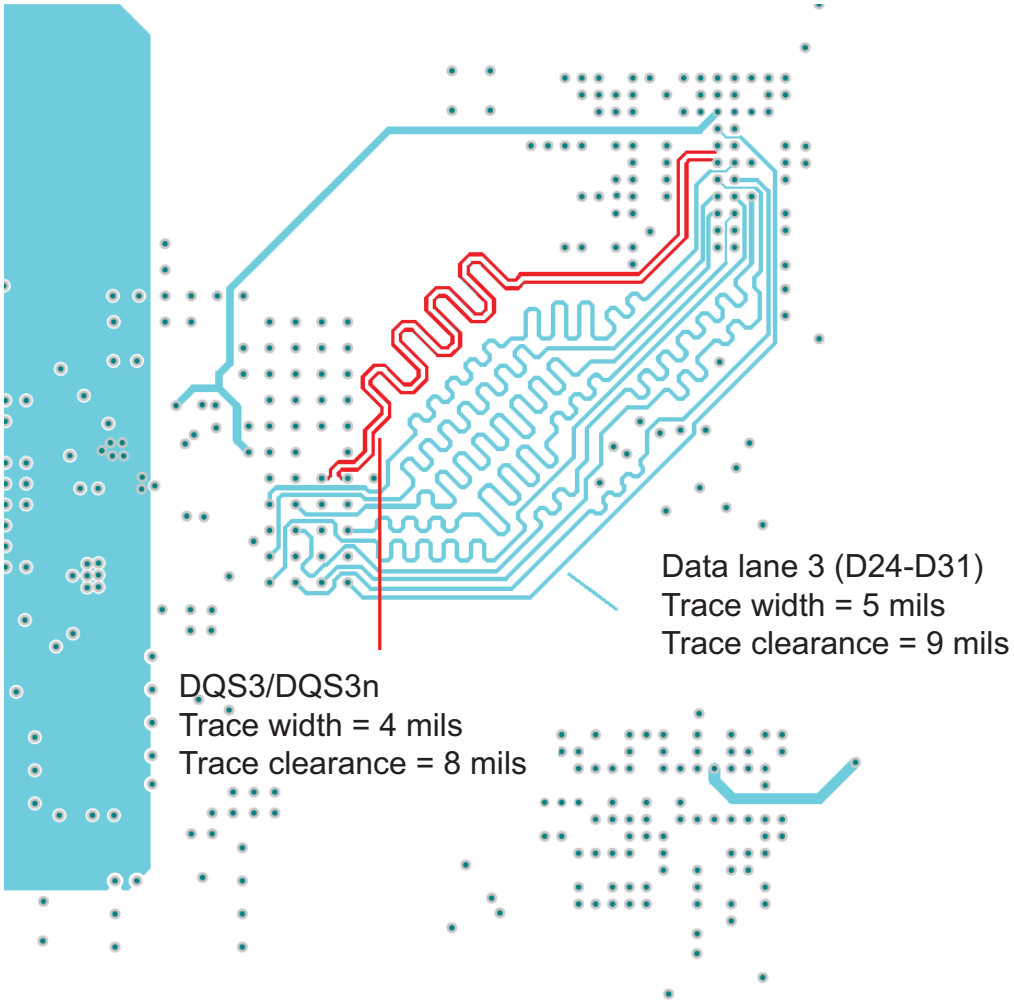
The above figure shows layer 3 of the test board focused on the LPDDR2-SDRAM configuration. It is used as a signal layer, contains traces for data lane 0..2 and address/control/command signals. Trace width and clearance are in accordance with the minimum required for most of these signals. There are, however, exceptions in the region underneath the MPU, where the 0.4 mm ball pitch does not allow to route traces wider than 3 mils or a larger than 3 mils clearance. In this case, we must violate the 4 mils minimum width rule due to physical constraints.

Figure 3-29. SAMA5D24/BGA256/LPDDR2-SDRAM Layer 5



Layer 5 of the test board serves as power plane and is also used as impedance matching reference for the neighboring signal layers (layers 4 and 6). The highlighted region shown in the above figure powers the SDRAM device. It covers a large surface and it does not feature any splits over any high-speed signal, in order to ensure a good signal integrity.

Figure 3-30. SAMA5D24/BGA256/LPDDR2-SDRAM Layer 6



Layer 6 contains signals (see the above figure) belonging to data lane 3. All traces belonging to data lane 3 are tightly matched, with a mismatch of only 17 mils.

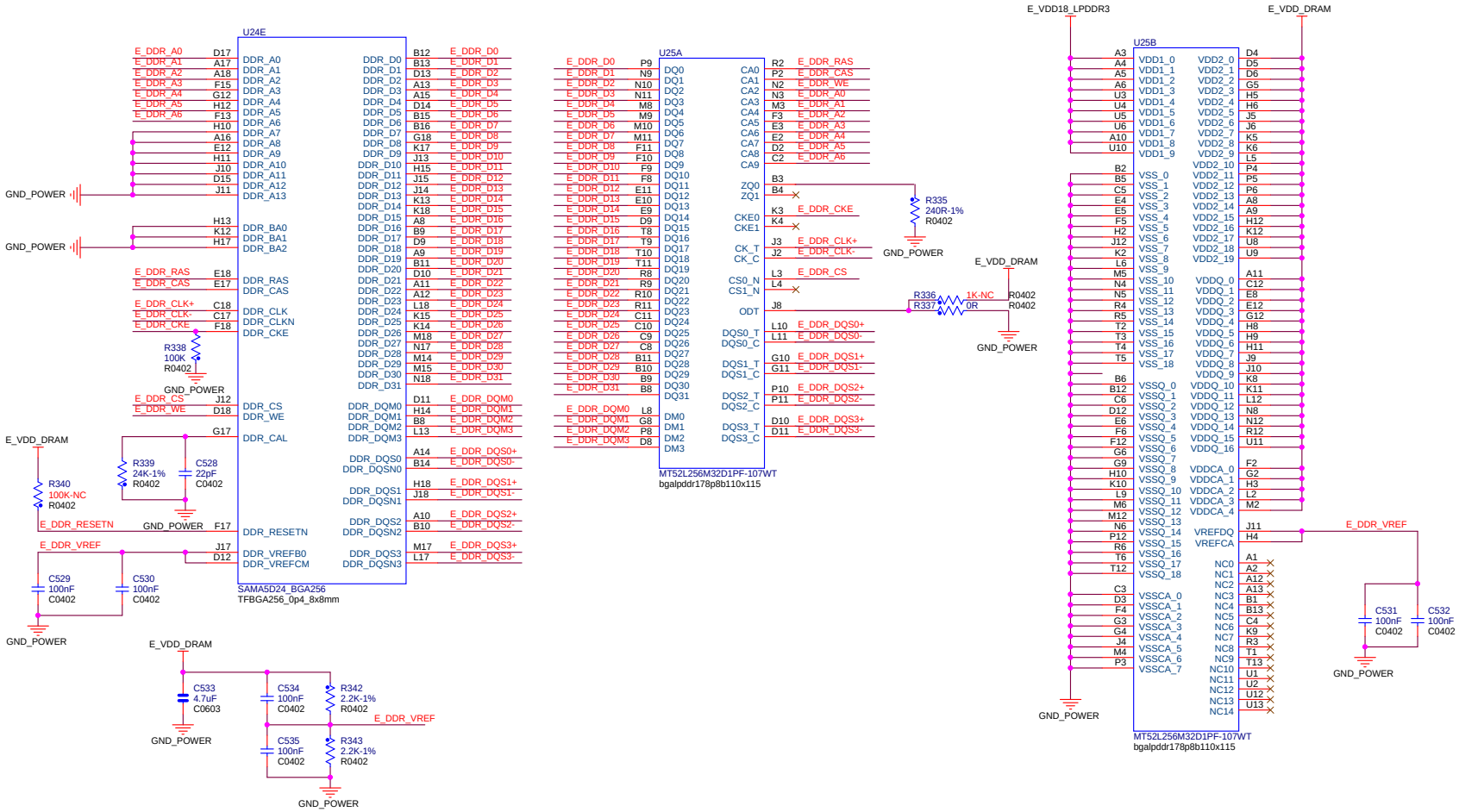
To calculate the trace impedance for differential signals located in inner layers, like the DQS/DQSn pair, impedance calculators/solvers are recommended to be used to speed up the design process. For maximum accuracy, make sure that these tools are in accordance with the IPC-2141 standard.

Using the parameters from Table Detailed Test Board Layer Stack-up, and having the trace width of 4 mils and a 8 mils clearance, results for differential pair DQS3/DQS3n in a trace impedance of 94.83 Ω, which is within tolerance.

In the same manner, the CK/CKn differential clock trace impedance can be calculated. The clock signal is routed on the top layer (see Figure SAMA5D24/BGA256/DDR2-SDRAM Layer 1 (Top)), has a 4 mils width, 8 mils clearance and 4.13 mils dielectric height, resulting in a 101.73 Ω impedance.

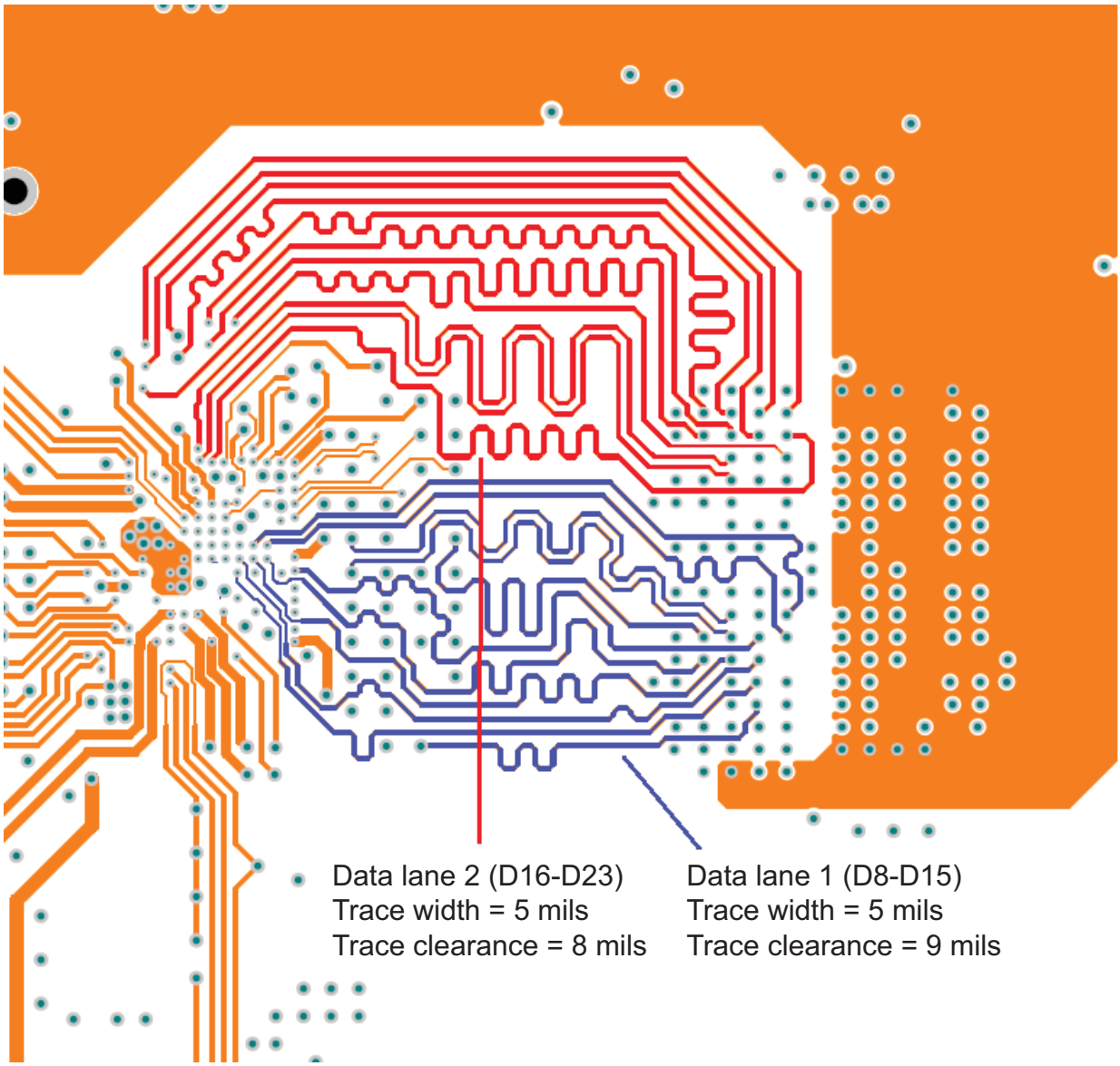
3.3.5 SAMA5D24/BGA256/LPDDR3-SDRAM Devices

Figure 3-31. MPUx-DRAMx LPDDR3 Device



This set features a SAMA5D24/BGA256 MPU and one 8-Gbit Micron LPDDR3-SDRAM device (Part No.: MT52L256M32D1PF-107WT).

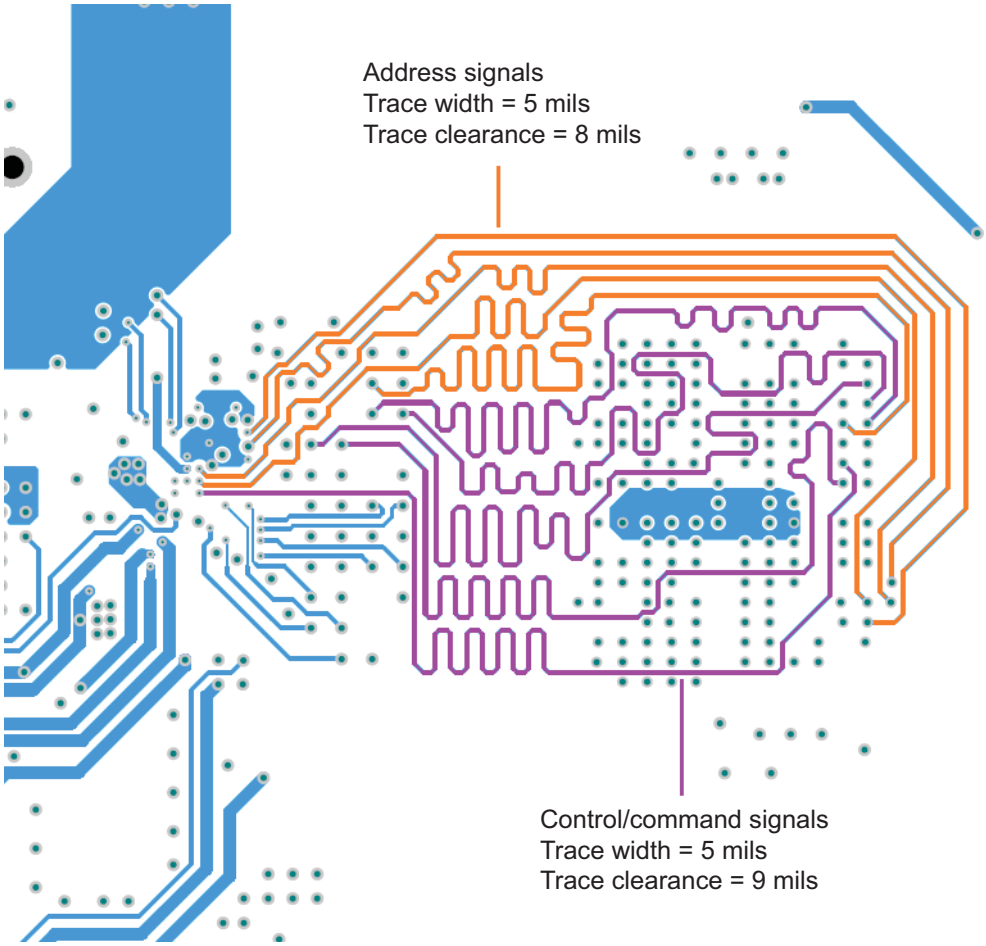
Figure 3-32. SAMA5D24/BGA256/LPDDR3-SDRAM Layer 3



The above figure shows layer 3 of the test board focused on the LPDDR3-SDRAM configuration. It is used as a signal layer, and contains traces for data lanes 1 and 2. Trace width and clearance are in accordance with the minimum required for most of these signals. There are, however, exceptions in the region underneath the MPU, where the 0.4-mm ball pitch does not allow to route traces wider than 3 mils. In this case, it is allowed to go below the 4 mils minimum because of high signal density.

Traces belonging in each data lane are tightly matched, with a 14-mils length mismatch for data lane 1 and a 34-mils mismatch for data lane 2. The DQS1/DQS1n and DQS2/DQS2n differential signals are also very precisely matched with a mismatch between signals from the same pair of 1 mil, respectively 3.2 mils.

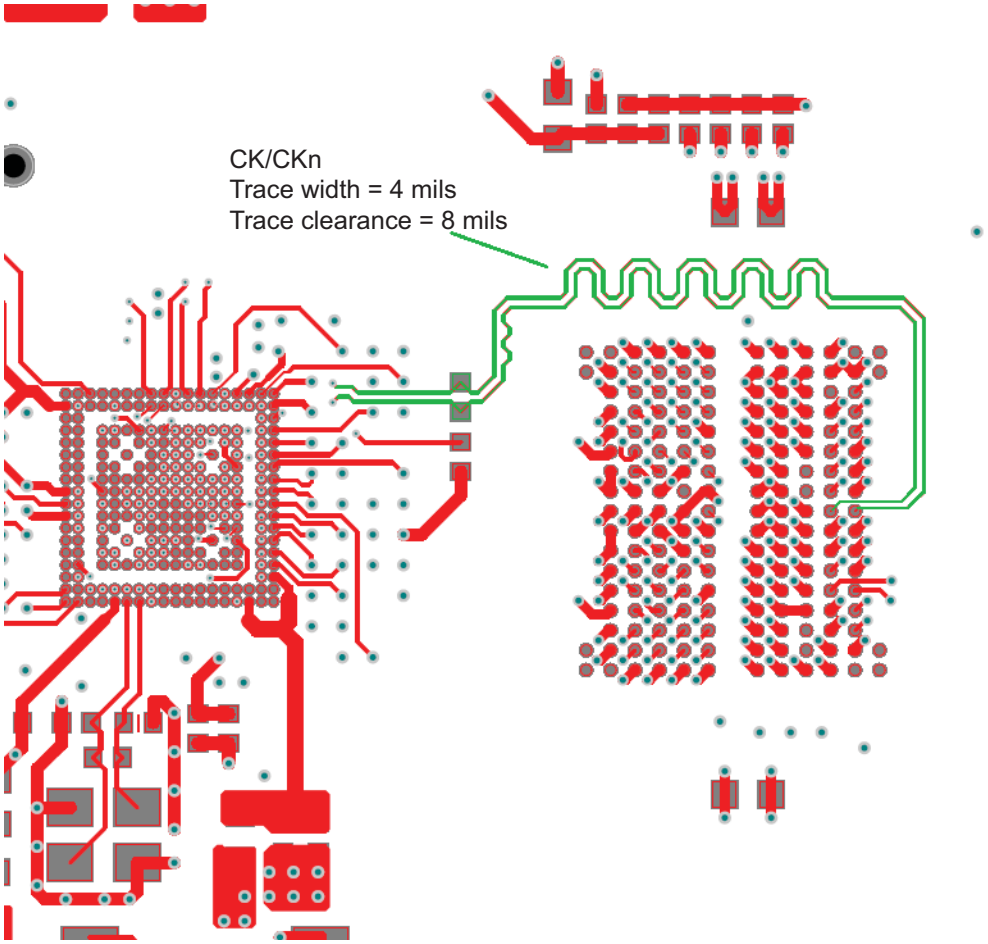
Figure 3-33. SAMA5D24/BGA256/LPDDR3-SDRAM Layer 4



The above figure shows layer 4 of the test board, centered on the LPDDR3-SDRAM device. It is used as signal layer and contains both address and control/command signals. The trace width and clearance size are in accordance with the general routing rules.

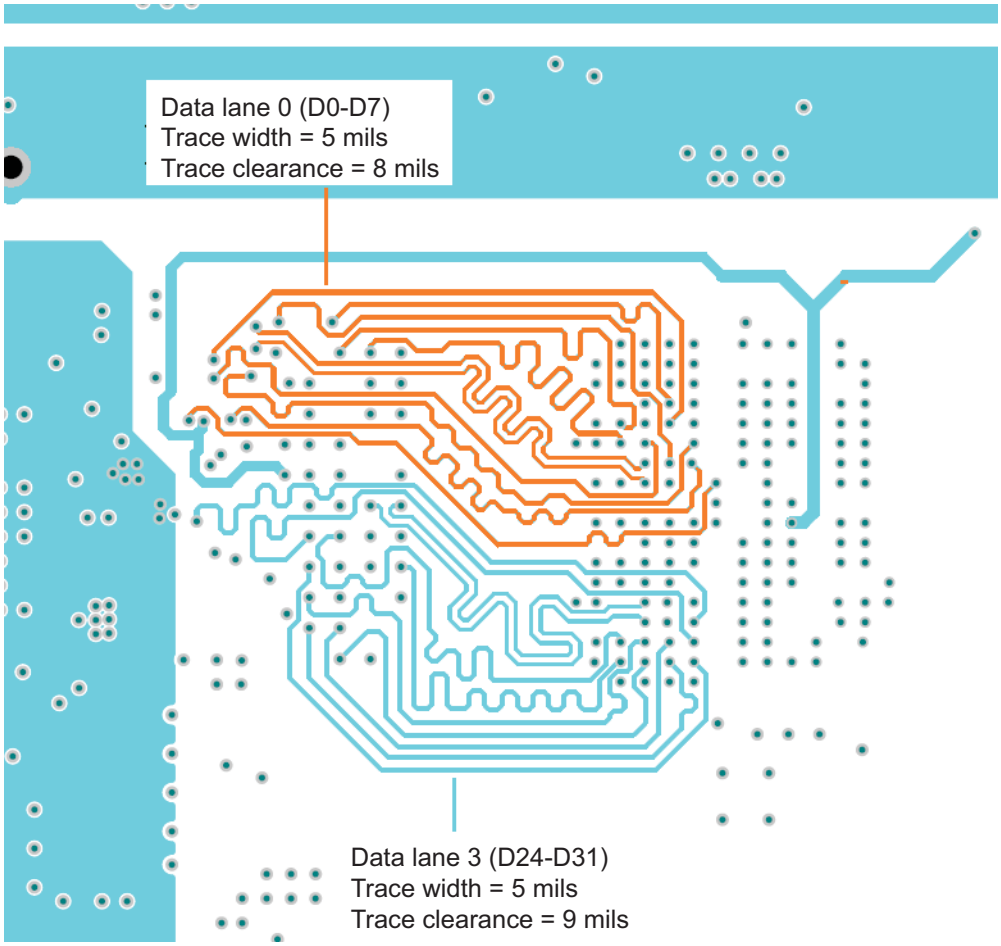
The trace impedance can be calculated using the stripline impedance formula (Equation 2) or using a specialized calculator. Applying the formula results in a trace impedance Z0 = 48.17 Ω.

Figure 3-34. SAMA5D24/BGA256/LPDDR3-SDRAM Layer 1 (Top)



The above figure shows the top layer of the test board centered on the LPDDR3-SDRAM device. The differential CK/CKn signals are routed on this layer, with the commented trace width and clearance. The differential pair impedance is 101.73 Ω, very close to the 100 Ω target.

Figure 3-35. SAMA5D24/BGA256/LPDDR3-SDRAM Layer 6



The above figure shows layer 6, where data lanes 0 and 3 from the LPDDR3-SDRAM are routed.

The target impedance for DQS0/DQS0n and DQS3/DQS3n differential pairs is 100 Ω. Using an impedance calculator resulted in a value of 98.16 Ω. All power layers provide an unslotted reference plane to maintain a good signal integrity.

4. Software Aspects

4.1 On-board SDRAM Device(s) Initialization Sequence

Every DDR-SDRAM type has a specific initialization sequence that must be performed after system powerup. The required steps are a sequence of electrical patterns, executed by software by the microprocessor and applied to the memory device through the embedded DRAM controller (“MPDDRC”).

These settings are detailed in section “Multiport DDR-SDRAM Controller (MPDDRC)” of the SAMA5D2 series datasheet. They are explained in a straightforward sequential manner below, for each kind of memory device. After the last step in the initialization sequence is issued, the SDRAM device is fully functional.

The tables in the following subchapters describe each initialization step with the necessary action (what needs to be done), the registers involved in that action, and the settings (values) to be written in the register fields.

Software support is provided with drivers and examples in the form of a software package.

4.1.1 DDR3-SDRAM/DDR3L-SDRAM Initialization

The initialization sequence is performed by software. The DDR3-SDRAM devices are initialized by the sequence described in the table below.

Note: These settings were verified as functional for the Micron MT52L256M32D1PF-107WT device. Application to other brands should be verified against their respective datasheets.

Table 4-1. DDR3-SDRAM/DDR3L-SDRAM Initialization

Step	Action	Register	Setting
1	Program the memory device type	MPDDRC_MD	MD = 4 (for DDR3), DBW = 0 (32 bits)
2	Program the shift sampling value	MPDDRC_RD_DATA_PATH	Section 4.2 SDRAM Controller Configuration provides values for these fields. These values depend on the DDR clock.
3	Program DDR3-SDRAM features	MPDDRC_CR MPDDRC_TPR0 MPDDRC_TPR1 MPDDRC_TPR2	
4	Issue a NOP command(4)	MPDDRC_MR	MODE = 1
5	500 µs delay(1)	–	–
6	Issue a NOP command(4)	MPDDRC_MR	MODE = 1
7	Issue an EMRS2 cycle(2)	MPDDRC_MR	MODE = 5
8	Issue an EMRS3 cycle(2)	MPDDRC_MR	MODE = 5
9	Issue an EMRS1 cycle(2)	MPDDRC_MR	MODE = 5
10	Write a ‘1’ to the DLL bit	MPDDRC_CR	DLL = 1

Step	Action	Register	Setting
11	Issue a Mode Register Set (MRS) cycle(3)	MPDDRC_MR	MODE = 3
12	Issue a Calibration command (MRS) (3)	MPDDRC_MR	MODE = 6
13	Provide a Normal Mode command(4)	MPDDRC_MR	MODE = 0
14	Write the refresh rate in COUNT field	MPDDRC_RTR	COUNT = Trefi/Tck

Note:

1. To issue a delay:
   - disable interrupts;
   - compute a deadline = ROUND_INT_DIV((timer_channel_freq/1000)*count, 1000), where count is the delay in µs;
   - start a timer and wait for the timer to reach the deadline;
   - enable interrupts.
2. To issue an Extended Mode Register Set (EMRS) cycle, after setting the MODE field to 5, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Then perform a write access to the DDR3-SDRAM device so that the BA[2:0] signals are set as follows:
   - BA[2] is set to 0, BA[1] is set to 0, BA[0] is set to 1 for EMRS1.
   - BA[2] is set to 0, BA[1] is set to 1, BA[0] is set to 0 for EMRS2.
   - BA[2] is set to 0, BA[1] is set to 1, BA[0] is set to 1 for EMRS3.
     The address at which the write access is issued in order to acknowledge the command needs to be calculated so that the BA[2:0] signals are in the right state for an EMRS cycle.
3. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to acknowledge the command so that BA[2:0] signals are set to 0 (write at BASE_ADDRESS_DDR).
4. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access at any address to acknowledge the command.

Refer to chapter ”Multiport DDR-SDRAM Controller (MPDDRC)” of the SAMA5D2 series datasheet for more information.

4.1.2 DDR2-SDRAM Initialization

The initialization sequence is generated by software. The DDR2-SDRAM devices are initialized by the following sequence:

Table 4-2. DDR2-SDRAM Initialization

Step	Action	Register	Setting
1	Program the memory device type	MPDDRC_MD	MD = 6 (for DDR2), DBW = 0 (32 bits)
2	Program the shift sampling value	MPDDRC_RD_DATA_PATH	Section 4.2 SDRAM Controller Configuration provides values for these

Step	Action	Register	Setting
3	Program DDR2-SDRAM features	MPDDRC_CR MPDDRC_TPR0 MPDDRC_TPR1 MPDDRC_TPR2	fields. These values depend on the DDR clock.
4	Issue a NOP command(4)	MPDDRC_MR	MODE = 1
5	200 µs delay(1)	–	–
6	Issue a NOP command(4)	MPDDRC_MR	MODE = 1
7	Issue an All Banks Precharge command(4)	MPDDRC_MR	MODE = 2
8	Issue an EMRS2 cycle(2)	MPDDRC_MR	MODE = 5
9	Issue an EMRS3 cycle(2)	MPDDRC_MR	MODE = 5
10	Issue an EMRS1 cycle(2)	MPDDRC_MR	MODE = 5
11	2 µs delay(1)	–	–
12	Write a ‘1’ to the DLL bit	MPDDRC_CR	DLL = 1
13	Issue a Mode Register Set (MRS) cycle(3)	MPDDRC_MR	MODE = 3
14	Issue an All Banks Precharge command(4)	MPDDRC_MR	MODE = 2
15	Provide two autorefresh (CBR) cycles(4)	MPDDRC_MR	MODE = 4
16	Write a ‘0’ to the DLL bit	MPDDRC_CR	DLL = 0
17	Issue a Mode Register Set (MRS) cycle(3)	MPDDRC_MR	MODE = 3
18	Configure the OCD field to 7	MPDDRC_CR	OCD = 7
19	Issue an EMRS1 cycle(2)	MPDDRC_MR	MODE = 5
20	Configure the OCD field to 0	MPDDRC_CR	OCD = 0
21	Issue an EMRS1 cycle(2)	MPDDRC_MR	MODE = 5
22	Provide a Normal Mode command(4)	MPDDRC_MR	MODE = 0
23	Write the refresh rate in COUNT field	MPDDRC_RTR	COUNT = Trefi/Tck

Note:

1. To issue a delay:
   - disable interrupts;
   - compute a deadline = ROUND_INT_DIV((timer_channel_freq/1000)*count, 1000), where count is the delay in µs;

- start a timer and wait for the timer to reach the deadline;
- enable interrupts.

2. To issue an Extended Mode Register Set (EMRS) cycle, after setting the MODE field to 5, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Then perform a write access to the DDR2-SDRAM device so that the BA[1:0] signals are as follows:
   - BA[1] is set to 0, BA[0] is set to 1 for EMRS1;
   - BA[1] is set to 1, BA[0] is set to 0 for EMRS2;
   - BA[1] is set to 1, BA[0] is set to 1 for EMRS3.
     The address at which the write access is issued in order to acknowledge the command needs to be calculated so that the BA[1:0] signals are in the right state for an EMRS cycle.
3. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to acknowledge the command so that BA[2:0] signals are set to 0 (write at BASE_ADDRESS_DDR).
4. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access at any address to acknowledge the command.

Refer to chapter ”Multiport DDR-SDRAM Controller (MPDDRC)” of the SAMA5D2 series datasheet for more information.

4.1.3 LPDDR1-SDRAM Initialization

The initialization sequence is generated by software. The low-power DDR1-SDRAM devices are initialized by the following sequence:

Table 4-3. LPDDR1-SDRAM Initialization

Step	Action	Register	Setting
1	Program the memory device type	MPDDRC_MD	MD = 3 (for LPDDR1), DBW = 0 (32 bits)
2	Program the shift sampling value	MPDDRC_RD_DATA_PATH	Section 4.2 SDRAM Controller Configuration provides values for these fields. These values depend on the DDR clock.
3	Program LPDDR1-SDRAM features	MPDDRC_CR MPDDRC_TPR0 MPDDRC_TPR 1	
4	Program TCR, PASR and DS	MPDDRC_LPR	–
5	Issue a NOP command(4)	MPDDRC_MR	MODE = 1
6	200 µs delay(1)	–	–
7	Issue a NOP command(4)	MPDDRC_MR	MODE = 1
8	Issue an All Banks Precharge command(4)	MPDDRC_MR	MODE = 2
9	Provide two autorefresh (CBR) cycles(4)	MPDDRC_MR	MODE = 4
10	Issue an EMRS cycle(2)	MPDDRC_MR	MODE = 5
11	Issue a Mode Register Set (MRS) cycle(3)	MPDDRC_MR	MODE = 3

Step	Action	Register	Setting
12	Provide a Normal Mode command(4)	MPDDRC_MR	MODE = 0
13	Write the refresh rate in COUNT field	MPDDRC_RTR	COUNT = Trefi/Tck

Note:

1. To issue a delay:
   - disable interrupts;
   - compute a deadline = ROUND_INT_DIV((timer_channel_freq/1000)*count, 1000), where count is the delay in µs;
   - start a timer and wait for the timer to reach the deadline;
   - enable interrupts.
2. To issue an Extended Mode Register Set (EMRS) cycle, after setting the MODE field to 5, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Then perform a write access to the LPDDR1-SDRAM device so that the BA[1] signal is set to 1 and BA[0] is set to 0. The address at which the write access is issued in order to acknowledge the command needs to be calculated so that the BA[1:0] signals are in the right state for an EMRS cycle.
3. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to acknowledge the command so that BA[2:0] signals are set to 0 (write at BASE_ADDRESS_DDR).
4. After setting the MODE field, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access at any address to acknowledge the command.

Refer to chapter "Multiport DDR-SDRAM Controller (MPDDRC)" of the SAMA5D2 series datasheet for more information.

4.1.4 LPDDR2-SDRAM/LPDDR3-SDRAM Initialization

The initialization sequence is generated by software. The low-power DDR2-SDRAM and low-power DDR3-SDRAM devices are initialized by the following sequence:

Table 4-4. LPDDR2-SDRAM/LPDDR3-SDRAM Initialization

Step	Action	Register	Setting
1	Program the memory device type	MPDDRC_MD	MD = 7 (for LPDDR2), MD = 5 (for LPDDR3), DBW = 0 (32 bits)
2	Program the shift sampling value	MPDDRC_RD_DATA_PATH	Section 4.2 SDRAM Controller Configuration provides values for these fields. These values depend on the DDR clock.
3	Program LPDDR2-SDRAM features	MPDDRC_CR MPDDRC_TPR0 MPDDRC_TPR 1	
4	Program DS, SEG_MASK and BK_MASK_PASR	MPDDRC_LPDDR23_LPR	–
5	Issue a NOP command(2)	MPDDRC_MR	MODE = 1
6	1 µs delay(1)	–	–

Step	Action	Register	Setting
7	Issue a NOP command(2)	MPDDRC_MR	MODE = 1
8	200 µs delay(1)	–	–
9	Issue a Reset command(2)	MPDDRC_MR	MODE = 7, MRS = 63
10	500 µs delay(1)	–	––
11	Issue a Calibration command(2)	MPDDRC_CR MPDDRC_MR	ZQ = 3, after command ack ZQ = 2 MODE = 7, MRS = 10
12	Issue a Mode register Write command(2)	MPDDRC_MR	MODE = 7, MRS = 1
13	Issue a Mode register Write command(2)	MPDDRC_MR	MODE = 7, MRS = 2
14	Issue a Mode register Write command(2)	MPDDRC_MR	MODE = 7, MRS = 3
15	Issue a Mode register Write command(2)	MPDDRC_MR	MODE = 7, MRS = 16
16	Write ‘1’ to bits 17 and 16 in SFR_DDRCFG	SFR_DDRCFG	Bit 17 = 1, Bit 16 = 1
17	Issue a NOP command(2)	MPDDRC_MR	MODE = 1
18	Issue a Mode register Read command(2)	MPDDRC_MR	MODE = 7, MRS = 5
19	Issue a Mode register Read command(2)	MPDDRC_MR	MODE = 7, MRS = 6
20	Issue a Mode register Read command(2)	MPDDRC_MR	MODE = 7, MRS = 8
21	Issue a Mode register Read command(2)	MPDDRC_MR	MODE = 7, MRS = 0
22	Provide a Normal Mode command(2)	MPDDRC_MR	MODE = 0
23	Write ‘0’ to bits 17 and 16 in SFR_DDRCFG	SFR_DDRCFG	Bit 17 = 0, Bit 16 = 0
24	Write the refresh rate in COUNT field	MPDDRC_RTR	COUNT = Trefi/Tck

Note:

1. To issue a delay:
   - disable interrupts;
   - compute a deadline = ROUND_INT_DIV((timer_channel_freq/1000)*count, 1000), where count is the delay in µs;

– start a timer and wait for the timer to reach the deadline;
– enable interrupts.

2. After setting the MODE and MRS fields, read MPDDRC_MR and add a memory barrier assembler instruction just after the read. Perform a write access at any address to acknowledge the command.

Refer to chapter ”Multiport DDR-SDRAM Controller (MPDDRC)” of the SAMA5D2 series datasheet for more information.

4.2 SDRAM Controller Configuration

After the memory devices on board have been configured, the memory controller itself must be configured in order to match the characteristics of the devices.

In order to “dialog” properly with an SDRAM device, several values have to be set in the MPDDRC register fields (e.g. asynchronous timing, number of columns, rows, banks, etc). The SDRAM device datasheet provides most of the necessary settings for a correct setup. Some parameters like the number of columns, rows and banks are independent from the system setup and are device-specific. The timing settings (Trc, Tras, etc.) depend on system parameters like DDR clock, therefore they should be carefully gathered from the SDRAM datasheet.

Software support is provided with drivers and examples in the form of a software package.

Description is given below for each type of board used for this study.

Note: In the following tables, “(unchanged)” means that the value should remain the same as before (i.e., the value should be kept unchanged from previous or reset value).

4.2.1 SAMA5D2-XULT DDR3L-SDRAM Software Settings

The SAMA5D2 board features a SAMA5D27/BGA289 MPU and two 2-Gbit Micron DDR3L-SDRAM devices (Part No.: MT41K128M16JT-125:K). The DDR clock runs at 166 MHz.

Table 4-5. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	4	DDR3-SDRAM
DBW: Data Bus Width(1)	0	Data bus width is 32 bits

Table 4-6. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	10 bits to define the column number
NR: Number of Row Bits	3	14 bits to define the row number
CAS: CAS Latency(4)	5	DDR3 CAS Latency 5
DLL: Reset DLL	(unchanged)	Used only during powerup sequence
DIC_DS: Output Driver Impedance Control (Drive Strength)	1	Weak drive strength (DDR2) - RZQ/7 (34 [NOM], DDR3)
DIS_DLL: Disable DLL	1	Disable DLL
ZQ: ZQ Calibration	(unchanged)	Not available for DDR3-SDRAM

Field	Setting	Setting Details
OCD: Off-chip Driver	(unchanged)	Not available for DDR3-SDRAM
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled
LC_LPDDR1: Low-cost Low-power DDR1	(unchanged)	Not available for DDR3-SDRAM
NB: Number of Banks	1	8 banks
NDQS: Not DQS	(unchanged)	Not available for DDR3-SDRAM
DECOD: Type of Decoding	1	Interleaved
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-7. MPDDRC_TPR0 Register Settings

Field	Setting(2)	Setting Details
TRAS: Active to Precharge Delay	35 ns	-
TRCD: Row to Column Delay	14 ns	-
TWR: Write Recovery Delay	15 ns	-
TRC: Row Cycle Delay	49 ns	-
TRP: Row Precharge Delay	14 ns	-
TRRD: Active BankA to Active BankB	Max (6 ns, 4 ck)	-
TWTR: Internal Write to Read Delay	Max (8 ns, 4 ck)	-
TMRD: Load Mode Register Command to Activate or Refresh Command	4 ck	-

Table 4-8. MPDDRC_TPR1 Register Settings

Field	Setting(2)	Setting Details
TRFC: Row Cycle Delay	160 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	170 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	0	Not used in DLL Off mode
TXP: Exit Powerdown Delay to First Command	Max (24 ns, 10 ck)	-

Table 4-9. MPDDRC_TPR2 Register Settings

Field	Setting(2)	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	(unchanged)	Not available for DDR3-SDRAM
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	(unchanged)	Not available for DDR3-SDRAM

Field	Setting[2]	Setting Details
TRPA: Row Precharge All Delay	(unchanged)	Not available for DDR3-SDRAM
TRTP: Read to Precharge	Max (8 ns, 4 ck)	-
TFAW: Four Active Windows	40 ns	-

Table 4-10. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data[4]	2	Sampling point is shifted by two cycles

Table 4-11. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	DDR3 serial impedance line = 55 ohms
TZQIO: IO Calibration	100	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	(unchanged)	Not available for DDR3-SDRAM

Table 4-12. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count3	1297	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	(unchanged)	Not available for DDR3-SDRAM
REF_PB: Refresh Per Bank	(unchanged)	Not available for DDR3-SDRAM

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

   For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

   Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

   Trefi [µs] = (Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

   If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

   then COUNT = (64/8192)*166*1000 = 1297

4. In the case of DDR3-SDRAM devices, the field CAS must be set to 5, and the field SHIFT_SAMPLING must be set to 2. The DLL Off mode sets the CAS Read Latency (CRL) and the CAS Write Latency (CWL) to 6. The latency is automatically set by the controller.

Table 4-13. SAMA5D2-XULT DDR3L-SDRAM Register Settings

Register name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000004
MPDDRC_CR	0xF000C008	0x00D0055D
MPDDRC_TPR0	0xF000C00C	0x44439336
MPDDRC_TPR1	0xF000C010	0x0A001D1B
MPDDRC_TPR2	0xF000C014	0x00072000
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000002
MPDDRC_IO_CALIBR	0xF000C034	0x00876504
MPDDRC_RTR	0xF000C004	0x00000511

4.2.2 SAMA5D2-PTC-EK DDR2-SDRAM Software Settings

The SAMA5D2 board features a SAMA5D27/BGA289 MPU and two 2-Gbit Winbond DDR2-SDRAM devices (Part No.: W972GG6KB-25). The DDR clock runs at 166 MHz.

Table 4-14. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	6	DDR2-SDRAM
DBW: Data Bus Width(1)	0	Data bus width is 32 bits

Table 4-15. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	10 bits to define the column number
NR: Number of Row Bits	3	14 bits to define the row number
CAS: CAS Latency	3	DDR2 CAS Latency 3
DLL: Reset DLL	(unchanged)	Used only during powerup sequence
DIC_DS: Output Driver Impedance Control (Drive Strength)	0	Normal drive strength (DDR2) - RZQ/6 (40 [NOM], DDR3)
DIS_DLL: Disable DLL	1	Disable DLL
ZQ: ZQ Calibration	(unchanged)	Not available for DDR2-SDRAM
OCD: Off-chip Driver	(unchanged)	Used only during powerup sequence
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled

Field	Setting	Setting Details
LC_LPDDR1: Low-cost Low-power DDR1	(unchanged)	Not available for DDR2-SDRAM
NB: Number of Banks	1	8 banks
NDQS: Not DQS	1	Not DQS is disabled
DECOD: Type of Decoding	1	Interleaved
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-16. MPDDRC_TPR0 Register Settings

Field	Setting(2)	Setting Details
TRAS: Active to Precharge Delay	45 ns	-
TRCD: Row to Column Delay	13 ns	-
TWR: Write Recovery Delay	15 ns	-
TRC: Row Cycle Delay	58 ns	-
TRP: Row Precharge Delay	13 ns	-
TRRD: Active BankA to Active BankB	10 ns	-
TWTR: Internal Write to Read Delay	8 ns	-
TMRD: Load Mode Register Command to Activate or Refresh Command	2 ck	-

Table 4-17. MPDDRC_TPR1 Register Settings

Field	Setting(2)	Setting Details
TRFC: Row Cycle Delay	195 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	205 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	200 ck	-
TXP: Exit Powerdown Delay to First Command	2 ck	-

Table 4-18. MPDDRC_TPR2 Register Settings

Field	Setting(2)	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	2 ck	-
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	8 ck	-
TRPA: Row Precharge All Delay	21 ns	-
TRTP: Read to Precharge	8 ns	-
TFAW: Four Active Windows	45 ns	-

Table 4-19. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data	1	Sampling point is shifted by one cycle

Table 4-20. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	DDR2 serial impedance line = 52 ohms
TZQIO: IO Calibration	101	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	1	Calibration is enabled

Table 4-21. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count(3)	1297	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	(unchanged)	Not available for DDR2-SDRAM
REF_PB: Refresh Per Bank	(unchanged)	Not available for DDR2-SDRAM

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

   For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

   Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

   Trefi [µs] = Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

   If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

   then COUNT = (64/8192)*166*1000 = 1297

Table 4-22. SAMA5D2-PTC-EK DDR2-SDRAM Register Settings

Register Name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000006
MPDDRC_CR	0xF000C008	0x00F0043D
MPDDRC_TPR0	0xF000C00C	0x2443A338

Register Name	Register Address	Contents Value
MPDDRC_TPR1	0xF000C010	0x02C82321
MPDDRC_TPR2	0xF000C014	0x00082482
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000001
MPDDRC_IO_CALIBR	0xF000C034	0x00876514
MPDDRC_RTR	0xF000C004	0x00000511

4.2.3 SAMA5D24/BGA256/DDR3L-SDRAM Software Settings

The SAMA5D24/BGA256/DDR3L-SDRAM set is part of a larger test board built on an 8-layer PCB. The board features a SAMA5D24/BGA256 MPU and two 1-Gbit ISSI DDR3L-SDRAM devices (Part No.: IS43TR16640B-15GBL). The DDR clock runs at 166 MHz.

Table 4-23. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	4	DDR3-SDRAM
DBW: Data Bus Width(1)	0	Data bus width is 32 bits

Table 4-24. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	10 bits to define the column number
NR: Number of Row Bits	2	13 bits to define the row number
CAS: CAS Latency(4)	5	DDR3 CAS Latency 5
DLL: Reset DLL	(unchanged)	Used only during powerup sequence
DIC_DS: Output Driver Impedance Control (Drive Strength)	1	Weak drive strength (DDR2) - RZQ/7 (34 [NOM], DDR3)
DIS_DLL: Disable DLL	1	Disable DLL
ZQ: ZQ Calibration	(unchanged)	Not available for DDR3-SDRAM
OCD: Off-chip Driver	(unchanged)	Not available for DDR3-SDRAM
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled
LC_LPDDR1: Low-cost Low-power DDR1	(unchanged)	Not available for DDR3-SDRAM
NB: Number of Banks	1	8 banks
NDQS: Not DQS	(unchanged)	Not available for DDR3-SDRAM
DECOD: Type of Decoding	1	Interleaved
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-25. MPDDRC_TPR0 Register Settings

Field	Setting[2]	Setting Details
TRAS: Active to Precharge Delay	36 ns	-
TRCD: Row to Column Delay	12 ns	-
TWR: Write Recovery Delay	15 ns	-
TRC: Row Cycle Delay	48 ns	-
TRP: Row Precharge Delay	12 ns	-
TRRD: Active BankA to Active BankB	Max (6 ns, 4 ck)	-
TWTR: Internal Write to Read Delay	Max (8 ns, 4 ck)	-
TMRD: Load Mode Register Command to Activate or Refresh Command	4 ck	-

Table 4-26. MPDDRC_TPR1 Register Settings

Field	Setting[2]	Setting Details
TRFC: Row Cycle Delay	110 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	120 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	0	Not used in DLL Off mode
TXP: Exit Powerdown Delay to First Command	Max (24 ns, 10 ck)	-

Table 4-27. MPDDRC_TPR2 Register Settings

Field	Setting[2]	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	(unchanged)	Not available for DDR3-SDRAM
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	(unchanged)	Not available for DDR3-SDRAM
TRPA: Row Precharge All Delay	(unchanged)	Not available for DDR3-SDRAM
TRTP: Read to Precharge	Max (8 ns, 4 ck)	-
TFAW: Four Active Windows	45 ns	-

Table 4-28. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data[4]	2	Sampling point is shifted by two cycles

Table 4-29. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	DDR3 serial impedance line = 55 ohms
TZQIO: IO Calibration	100	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	(unchanged)	Not available for DDR3-SDRAM

Table 4-30. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count(3)	1297	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	(unchanged)	Not available for DDR3-SDRAM
REF_PB: Refresh Per Bank	(unchanged)	Not available for DDR3-SDRAM

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

   For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

   Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

   Trefi [µs] = (Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

   If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

   then COUNT = (64/8192)*166*1000 = 1297
4. In the case of DDR3-SDRAM devices, the field CAS must be set to 5, and the field SHIFT_SAMPLING must be set to 2. The DLL Off mode sets the CAS Read Latency (CRL) and the CAS Write Latency (CWL) to 6. The latency is automatically set by the controller.

Table 4-31. SAMA5D24/BGA256/DDR3L-SDRAM Register Settings

Register Name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000004
MPDDRC_CR	0xF000C008	0x00D00559
MPDDRC_TPR0	0xF000C00C	0x44428326
MPDDRC_TPR1	0xF000C010	0x0A001413

Register Name	Register Address	Contents Value
MPDDRC_TPR2	0xF000C014	0x00084000
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000002
MPDDRC_IO_CALIBR	0xF000C034	0x00876504
MPDDRC_RTR	0xF000C004	0x00000511

4.2.4 SAMA5D24/BGA256/DDR2-SDRAM Software Settings

The SAMA5D24/BGA256/DDR2-SDRAM set is part of a larger test board built on an 8-layer PCB. The board features a SAMA5D24/BGA256 MPU and two 512-Mbit ISSI DDR2-SDRAM devices (Part No.: IS43DR16320E-25DBL). The DDR clock runs at 166 MHz.

Table 4-32. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	6	DDR2-SDRAM
DBW: Data Bus Width(1)	0	Data bus width is 32 bits

Table 4-33. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	10 bits to define the column number
NR: Number of Row Bits	2	13 bits to define the row number
CAS: CAS Latency	3	DDR2 CAS Latency 3
DLL: Reset DLL	(unchanged)	Used only during powerup sequence
DIC_DS: Output Driver Impedance Control (Drive Strength)	0	Normal drive strength (DDR2) - RZQ/6 (40 [NOM], DDR3)
DIS_DLL: Disable DLL	1	Disable DLL
ZQ: ZQ Calibration	(unchanged)	Not available for DDR2-SDRAM
OCD: Off-chip Driver	(unchanged)	Used only during powerup sequence
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled
LC_LPDDR1: Low-cost Low-power DDR1	(unchanged)	Not available for DDR2-SDRAM
NB: Number of Banks	0	4 banks
NDQS: Not DQS	0	Not DQS is enabled
DECOD: Type of Decoding	1	Interleaved
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-34. MPDDRC_TPR0 Register Settings

Field	Setting(2)	Setting Details
TRAS: Active to Precharge Delay	40 ns	-
TRCD: Row to Column Delay	15 ns	-
TWR: Write Recovery Delay	15 ns	-
TRC: Row Cycle Delay	55 ns	-
TRP: Row Precharge Delay	15 ns	-
TRRD: Active BankA to Active BankB	10 ns	-
TWTR: Internal Write to Read Delay	8 ns	-
TMRD: Load Mode Register Command to Activate or Refresh Command	2 ck	-

Table 4-35. MPDDRC_TPR1 Register Settings

Field	Setting(2)	Setting Details
TRFC: Row Cycle Delay	105 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	115 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	200 ck	-
TXP: Exit Powerdown Delay to First Command	2 ck	-

Table 4-36. MPDDRC_TPR2 Register Settings

Field	Setting2	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	2 ck	-
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	2 ck	-
TRPA: Row Precharge All Delay	15 ns	-
TRTP: Read to Precharge	8 ns	-
TFAW: Four Active Windows	45 ns	-

Table 4-37. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data	1	Sampling point is shifted by one cycle

Table 4-38. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	DDR2 serial impedance line = 52 ohms
TZQIO: IO Calibration	101	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	1	Calibration is enabled

Table 4-39. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count(3)	1297	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	(unchanged)	Not available for DDR2-SDRAM
REF_PB: Refresh Per Bank	(unchanged)	Not available for DDR2-SDRAM

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

   For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

   Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

   Trefi [µs] = Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

   If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

   then COUNT = (64/8192)*166*1000 = 1297

Table 4-40. SAMA5D24/BGA256/DDR2-SDRAM Register Settings

Register Name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000006
MPDDRC_CR	0xF000C008	0x00C00539
MPDDRC_TPR0	0xF000C00C	0x2223A337
MPDDRC_TPR1	0xF000C010	0x02C81412
MPDDRC_TPR2	0xF000C014	0x00082322
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000001

Register Name	Register Address	Contents Value
MPDDRC_IO_CALIBR	0xF000C034	0x00876514
MPDDRC_RTR	0xF000C004	0x00000511

4.2.5 SAMA5D24/BGA256/LPDDR1-SDRAM Software Settings

The SAMA5D24/BGA256/LPDDR1-SDRAM set is part of a larger test board built on an 8-layer PCB. The board features a SAMA5D24/BGA256 MPU and two 256-Mbit ISSI LPDDR1-SDRAM devices (Part No.: IS43LR16160G-6BLI). The DDR clock runs at 166 MHz.

Table 4-41. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	3	LPDDR1-SDRAM
DBW: Data Bus Width(1)	0	Data bus width is 32 bits

Table 4-42. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	9 bits to define the column number
NR: Number of Row Bits	2	13 bits to define the row number
CAS: CAS Latency	3	LPDDR1 CAS Latency 3
DLL: Reset DLL	(unchanged)	Used only during powerup sequence
DIC_DS: Output Driver Impedance Control (Drive Strength)	(unchanged)	Not available for LPDDR1-SDRAM
DIS_DLL: Disable DLL	(unchanged)	Not available for LPDDR1-SDRAM
ZQ: ZQ Calibration	(unchanged)	Not available for LPDDR1-SDRAM
OCD: Off-chip Driver	(unchanged)	Not available for LPDDR1-SDRAM
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled
LC_LPDDR1: Low-cost Low-power DDR1	0	Any LPDDR1 density except 2 banks
NB: Number of Banks	0	4 banks
NDQS: Not DQS	(unchanged)	Not available for LPDDR1-SDRAM
DECOD: Type of Decoding	0	Sequential
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-43. MPDDRC_TPR0 Register Settings

Field	Setting(2)	Setting Details
TRAS: Active to Precharge Delay	42 ns	-
TRCD: Row to Column Delay	18 ns	-
TWR: Write Recovery Delay	15 ns	-
TRC: Row Cycle Delay	60 ns	-
TRP: Row Precharge Delay	18 ns	-
TRRD: Active BankA to Active BankB	12 ns	-
TWTR: Internal Write to Read Delay	1 ck	-
TMRD: Load Mode Register Command to Activate or Refresh Command	2 ck	-

Table 4-44. MPDDRC_TPR1 Register Settings

Field	Setting(2)	Setting Details
TRFC: Row Cycle Delay	70 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	120 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	120 ns	-
TXP: Exit Powerdown Delay to First Command	1 ck	-

Table 4-45. MPDDRC_TPR2 Register Settings

Field	Setting(2)	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	(unchanged)	Not available for LPDDR1-SDRAM
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	(unchanged)	Not available for LPDDR1-SDRAM
TRPA: Row Precharge All Delay	(unchanged)	Not available for LPDDR1-SDRAM
TRTP: Read to Precharge	2 ck	-
TFAW: Four Active Windows	(unchanged)	Not available for LPDDR1-SDRAM

Table 4-46. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data	1	Sampling point is shifted by one cycle

Table 4-47. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	LPDDR1 serial impedance line = 52 ohms
TZQIO: IO Calibration	101	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	1	Calibration is enabled

Table 4-48. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count(3)	1297	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	(unchanged)	Not available for LPDDR1-SDRAM
REF_PB: Refresh Per Bank	(unchanged)	Not available for LPDDR1-SDRAM

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

   For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

   Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

   Trefi [µs] = Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

   If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

   then COUNT = (64/8192)*166*1000 = 1297

Table 4-49. SAMA5D24/BGA256/LPDDR1-SDRAM Register Settings

Register Name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000003
MPDDRC_CR	0xF000C008	0x00800539
MPDDRC_TPR0	0xF000C00C	0x2123A337
MPDDRC_TPR1	0xF000C010	0x0114140C
MPDDRC_TPR2	0xF000C014	0x00082322
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000001

Register Name	Register Address	Contents Value
MPDDRC_IO_CALIBR	0xF000C034	0x00876514
MPDDRC_RTR	0xF000C004	0x00000511

4.2.6 SAMA5D24/BGA256/LPDDR2-SDRAM Software Settings

The SAMA5D24/BGA256/LPDDR2-SDRAM set is part of a larger test board built on an 8-layer PCB. The board features a SAMA5D24/BGA256 MPU and two 512-Mbit ISSI LPDDR2-SDRAM devices (Part No.: IS43LD16320A-25BLI). The DDR clock runs at 166 MHz.

Table 4-50. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	7	LPDDR2-SDRAM
DBW: Data Bus Width(1)	0	Data bus width is 32 bits

Table 4-51. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	10 bits to define the column number
NR: Number of Row Bits	2	13 bits to define the row number
CAS: CAS Latency	3	LPDDR2 CAS Latency 3
DLL: Reset DLL	(unchanged)	Not available for LPDDR2-SDRAM
DIC_DS: Output Driver Impedance Control (Drive Strength)	(unchanged)	Not available for LPDDR2-SDRAM
DIS_DLL: Disable DLL	(unchanged)	Not available for LPDDR2-SDRAM
ZQ: ZQ Calibration	(unchanged)	Used only during powerup sequence
OCD: Off-chip Driver	(unchanged)	Not available for LPDDR2-SDRAM
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled
LC_LPDDR1: Low-cost Low-power DDR1	(unchanged)	Not available for LPDDR2-SDRAM
NB: Number of Banks	0	4 banks
NDQS: Not DQS	(unchanged)	Not available for LPDDR2-SDRAM
DECOD: Type of Decoding	0	Sequential
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-52. MPDDRC_TPR0 Register Settings

Field	Setting(2)	Setting Details
TRAS: Active to Precharge Delay	42 ns	-
TRCD: Row to Column Delay	18 ns	-
TWR: Write Recovery Delay	15 ns	-
TRC: Row Cycle Delay	60 ns	-
TRP: Row Precharge Delay	18 ns	-
TRRD: Active BankA to Active BankB	10 ns	-
TWTR: Internal Write to Read Delay	8 ns	-
TMRD: Load Mode Register Command to Activate or Refresh Command	2 ck	-

Table 4-53. MPDDRC_TPR1 Register Settings

Field	Setting(2)	Setting Details
TRFC: Row Cycle Delay	90 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	100 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	(unchanged)	Not available for LPDDR2-SDRAM
TXP: Exit Powerdown Delay to First Command	8 ns	-

Table 4-54. MPDDRC_TPR2 Register Settings

Field	Setting(2)	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	(unchanged)	Not available for LPDDR2-SDRAM
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	(unchanged)	Not available for LPDDR2-SDRAM
TRPA: Row Precharge All Delay	18 ns	Equivalent to tRPAB
TRTP: Read to Precharge	8 ns	-
TFAW: Four Active Windows	50 ns	-

Table 4-55. MPDDRC_LPDDR23_LPR Register Settings

Field	Setting	Setting Details
BK_MASK_PASR: Bank Mask Bit/PASR	0	Refresh is enabled
SEG_MASK: Segment Mask Bit	0	Segment is refreshed
DS: Drive Strength	2	40 ohms typical

Table 4-56. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data	1	Sampling point is shifted by one cycle

Table 4-57. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	LPDDR2 serial impedance line = 60 ohms
TZQIO: IO Calibration	101	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	(unchanged)	Not available for LPDDR2-SDRAM

Table 4-58. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count[3]	649	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	0	Adjust refresh rate is not enabled
REF_PB: Refresh Per Bank	0	Refresh all banks during autorefresh operation

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

   For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

   Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

   Trefi [µs] = Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

   If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

   then COUNT = (64/8192)*166*1000 = 1297

Table 4-59. SAMA5D24/BGA256/LPDDR2-SDRAM Register Settings

Register Name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000007
MPDDRC_CR	0xF000C008	0x00800539

Register Name	Register Address	Contents Value
MPDDRC_TPR0	0xF000C00C	0x2223A337
MPDDRC_TPR1	0xF000C010	0x0800110F
MPDDRC_TPR2	0xF000C014	0x00092300
MPDDRC_LPDDR23_LPR	0xF000C028	0x02000000
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000001
MPDDRC_IO_CALIBR	0xF000C034	0x00876504
MPDDRC_RTR	0xF000C004	0x00000289

Important: For LPDDR2/LPDDR3 devices, certain sequences shall be used to power off these devices. Uncontrolled power-off sequences are destructive and can be applied only up to 400 times in the life of the device. Make sure to respect those sequences to guarantee a long functional life for your system. Refer to the manufacturer's datasheet for the proper way to power off the devices. Typically these rely upon an early detection of power failure and achieve a timely power-off sequence through the execution of a high priority interrupt.

4.2.7 SAMA5D24/BGA256/LPDDR3-SDRAM Software Settings

The SAMA5D24/BGA256/LPDDR3-SDRAM set is part of a larger test board built on an 8-layer PCB. The board features a SAMA5D24/BGA256 MPU and one 8-Gbit(4) Micron LPDDR3-SDRAM device (Part No.: MT52L256M32D1PF-107WT). The DDR clock runs at 166 MHz.

Table 4-60. MPDDRC_MD Register Settings

Field	Setting	Setting Details
MD: Memory Device	5	LPDDR3-SDRAM
DBW: Data Bus Width[1]	0	Data bus width is 32 bits

Table 4-61. MPDDRC_CR Register Settings

Field	Setting	Setting Details
NC: Number of Column Bits	1	10 bits to define the column number
NR: Number of Row Bits	3	14 bits to define the row number
CAS: CAS Latency	3	LPDDR3 CAS Latency 3
DLL: Reset DLL	(unchanged)	Not available for LPDDR3-SDRAM
DIC_DS: Output Driver Impedance Control (Drive Strength)	(unchanged)	Not available for LPDDR3-SDRAM
DIS_DLL: Disable DLL	(unchanged)	Used only during powerup sequence
ZQ: ZQ Calibration	(unchanged)	Used only during powerup sequence
OCD: Off-chip Driver	(unchanged)	Not available for LPDDR3-SDRAM

Field	Setting	Setting Details
DQMS: Mask Data is Shared	0	DQM is not shared with another controller
ENRDM: Enable Read Measure	0	DQS/DDR_DATA phase error correction is disabled
LC_LPDDR1: Low-cost Low-power DDR1	(unchanged)	Not available for LPDDR3-SDRAM
NB: Number of Banks	1	8 banks
NDQS: Not DQS	(unchanged)	Not available for LPDDR3-SDRAM
DECOD: Type of Decoding	0	Sequential
UNAL: Support Unaligned Access	1	Unaligned access is supported

Table 4-62. MPDDRC_TPR0 Register Settings

Field	Setting(2)	Setting Details
TRAS: Active to Precharge Delay	42 ns	-
TRCD: Row to Column Delay	max (18 ns, 3 ck)	-
TWR: Write Recovery Delay	max (15 ns, 3 ck)	-
TRC: Row Cycle Delay	60 ns	-
TRP: Row Precharge Delay	max (18 ns, 3 ck)	-
TRRD: Active BankA to Active BankB	max (10 ns, 2 ck)	-
TWTR: Internal Write to Read Delay	max (8 ns, 4 ck)	-
TMRD: Load Mode Register Command to Activate or Refresh Command	max (14 ns, 10 ck)	-

Table 4-63. MPDDRC_TPR1 Register Settings

Field	Setting(2)	Setting Details
TRFC: Row Cycle Delay	210 ns	-
TXSNR: Exit Self-refresh Delay to Non-Read Command	220 ns	-
TXSRD: Exit Self-refresh Delay to Read Command	(unchanged)	Not available for LPDDR3-SDRAM
TXP: Exit Powerdown Delay to First Command	max (8 ns, 2 ck)	-

Table 4-64. MPDDRC_TPR2 Register Settings

Field	Setting(2)	Setting Details
TXARD: Exit Active Power Down Delay to Read Command in Mode “Fast Exit”	(unchanged)	Not available for LPDDR3-SDRAM
TXARDS: Exit Active Power Down Delay to Read Command in Mode “Slow Exit”	(unchanged)	Not available for LPDDR3-SDRAM

Field	Setting(2)	Setting Details
TRPA: Row Precharge All Delay	18 ns	Equivalent to tRPAB
TRTP: Read to Precharge	max (8 ns, 4 ck)	-
TFAW: Four Active Windows	max (50 ns, 8 ck)	-

Table 4-65. MPDDRC_LPDDR23_LPR Register Settings

Field	Setting	Setting Details
BK_MASK_PASR: Bank Mask Bit/PASR	0	Refresh is enabled
SEG_MASK: Segment Mask Bit	0	Segment is refreshed
DS: Drive Strength	2	40 ohm typical

Table 4-66. MPDDRC_RD_DATA_PATH Register Settings

Field	Setting	Setting Details
SHIFT_SAMPLING: Shift Sampling Point of Data	2	Sampling point is shifted by two cycles

Table 4-67. MPDDRC_IO_CALIBR Register Settings

Field	Setting	Setting Details
RDIV: Resistor Divider, Output Driver Impedance	4	LPDDR3 serial impedance line = 57 ohms
TZQIO: IO Calibration	101	TZQIO = (DDRCK × 600e-9) + 1
EN_CALIB: Enable Calibration	(unchanged)	Not available for LPDDR3-SDRAM

Table 4-68. MPDDRC_RTR Register Settings

Field	Setting	Setting Details
COUNT: MPDDRC Refresh Timer Count3	649	Value needs to be computed
ADJ_REF: Adjust Refresh Rate	0	Adjust refresh rate is not enabled
REF_PB: Refresh Per Bank	0	Refresh all banks during autorefresh operation

Note:

1. If using one 32-bit data bus width SDRAM device or two 16-bit devices, set the Data Bus Width to 32 bits (DBW = 0). If only one 16-bit data bus width SDRAM device is used, set the Data Bus Width to 16 bits (DBW = 1).
2. If timing values are given in nanoseconds, they must be converted in clock cycles and rounded up. Tcycles = Tns/Tck, where Tcycles is the timing value in clock cycles, Tns is the timing value in nanoseconds and Tck is the DDR clock period.
   Eg: If Fck = 166 MHz, then Tck = 1/Fck = 6 ns

   If Tns = 35 ns, then Tcycles = 35/6 = 6 clock cycles
3. The value in the COUNT field needs to be computed.
   COUNT = Trefi/Tck

For Trefi = 7.8 µs and Tck = 6 ns results in COUNT = 1300

Trefi can also be calculated if the Refresh Window [ms] and Refresh Cycles are given (in SDRAM datasheet).

Trefi [µs] = Refresh Window [ms]/Refresh Cycles)*Fck [MHz]*1000

If Refresh Window = 64 ms, Refresh Cycles = 8192 and Fck = 166 MHz,

then COUNT = (64/8192)*166*1000 = 1297

4. The memory controller is unable to use the whole capacity of the 8-Gbit memory device (supports 4 Gbits maximum). An 8-Gbit device was mounted for procurement facility reasons. With the current settings, the usage of half of this capacity is achievable.

Table 4-69. SAMA5D24/BGA256/LPDDR3-SDRAM Register Settings

Register Name	Register Address	Contents Value
MPDDRC_MD	0xF000C020	0x00000005
MPDDRC_CR	0xF000C008	0x0090053D
MPDDRC_TPR0	0xF000C00C	0xA423A337
MPDDRC_TPR1	0xF000C010	0x02002523
MPDDRC_TPR2	0xF000C014	0x00094400
MPDDRC_LPDDR23_LPR	0xF000C028	0x02000000
MPDDRC_RD_DATA_PATH	0xF000C05C	0x00000002
MPDDRC_IO_CALIBR	0xF000C034	0x00876504
MPDDRC_RTR	0xF000C004	0x00000289

Important: For LPDDR2/LPDDR3 devices, certain sequences shall be used to power off these devices. Uncontrolled power-off sequences are destructive and can be applied only up to 400 times in the life of the device. Make sure to respect those sequences to guarantee a long functional life for your system. Refer to the manufacturer's datasheet for the proper way to power off the devices. Typically these rely upon an early detection of power failure and achieve a timely power-off sequence through the execution of a high priority interrupt.

5. Setting Recommendations

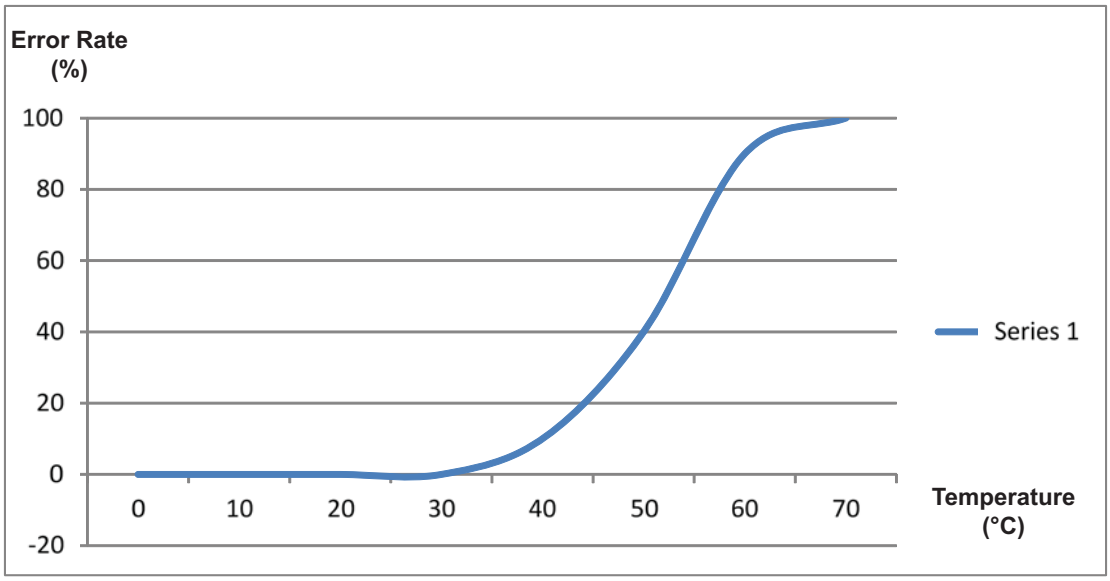
Setting the memory with default parameter values and timings, often “quickly” inferred from the manufacturer’s datasheets, may pass all tests at room temperature and over their nominal operating temperature range. But when one pushes the tests further - e.g. by varying the temperature as we did in this study - behavioral problems are likely to appear.

We verified this by deliberately varying some correct settings to “borderline” values, where the system remains functional at room temperature, but then gradually fails when the temperature rises.

A setting that appears to work by default might prove incorrect. Always thoroughly research the manufacturer’s datasheet and application notes for the correct settings and double check all of them while paying attention to the system parameters (like DDR clock). Tests have proven that carelessness may result in product failures after deploying to the field.

The chart below is a rough representation of the error rate during testing versus board temperature. It depends on the number of parameters set at borderline values, so an accurate representation is hard to predict and can be determined by testing. It can also vary from one type of SDRAM to another, but the behavior is approximately the same. Some setting values can trigger errors at just above room temperature while others can trigger errors only at the maximum operating temperature.

Figure 5-1. Error Rate vs Temperature



An error is identified when data read from the SDRAM is different from the known written data during testing. An error occurs faster at higher temperatures, when the error rate is high. At lower temperatures, errors may occur even after more than half of the memory capacity is tested without issues.

The table below contains some examples of timing parameters with borderline values having the most impact over the error rate. These timings are:

- t_{rcd} - Row Address to Column Address Delay
- t_{rp} - Row Precharge Delay
- t_{rfc} - Row Refresh Cycle Delay

At room temperature, all tests pass with the timings at pass values and all tests fail at fail values. Always check the SDRAM datasheet to obtain the optimal settings.

Table 5-1. Pass and Fail Values for t_{rcd}, t_{rp} and t_{rfc} Timings

Timings	DDR3		DDR2		LPDDR1		LPDDR2		LPDDR3	
	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail
t_{rcd}[ns]	7	6	7	6	13	12	7	6	7	6
t_{rp}[ns]	7	6	7	6	7	6	7	6	7	6
t_{rfc}[ns]	73	72	67	66	40	35	60	61	115	114

6. Conclusion

This application note presented a set of recommended guidelines for PCB routing of different types of SDRAM devices, as well as layout examples and software settings. It also showed that the proper functionality of an SDRAM device can be broken if apparent good settings are being made. This is the reason why it is critical to always follow the manufacturer’s datasheet and application notes.

7. Revision History

7.1 Rev. A - 06/2018

This is the initial released version of this application note.

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